

/media/saverio/OS/Users
/Saverio/Desktop/SE/git
/Andrea/FPGA/MyIntGPIO/MyIntGPIO.sdk
/provaINTRGpio/src/myIntGPIO2.h



```
graph TD; A["/media/saverio/OS/Users  
/Saverio/Desktop/SE/git  
/Andrea/FPGA/MyIntGPIO/MyIntGPIO.sdk  
/provaINTRGpio/src/myIntGPIO2.h"] --> B[xil_types.h]; A --> C[xstatus.h]; A --> D[xil_io.h];
```

xil_types.h

xstatus.h

xil_io.h