Компилируем проект, запоминаем кол-во ресурсов и времянки.

Flow Status	Successful - Sat Oct 26 23:47:46 2024
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Standard Edition
Revision Name	DE10_LITE_GSensor
Top-level Entity Name	DE10_LITE_GSensor
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	186 / 49,760 (< 1 %)
Total registers	114
Total pins	101 / 360 (28 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	1 / 4 (25 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

Slow 1200mV 85C Model Fmax Summary

<<Filter>>

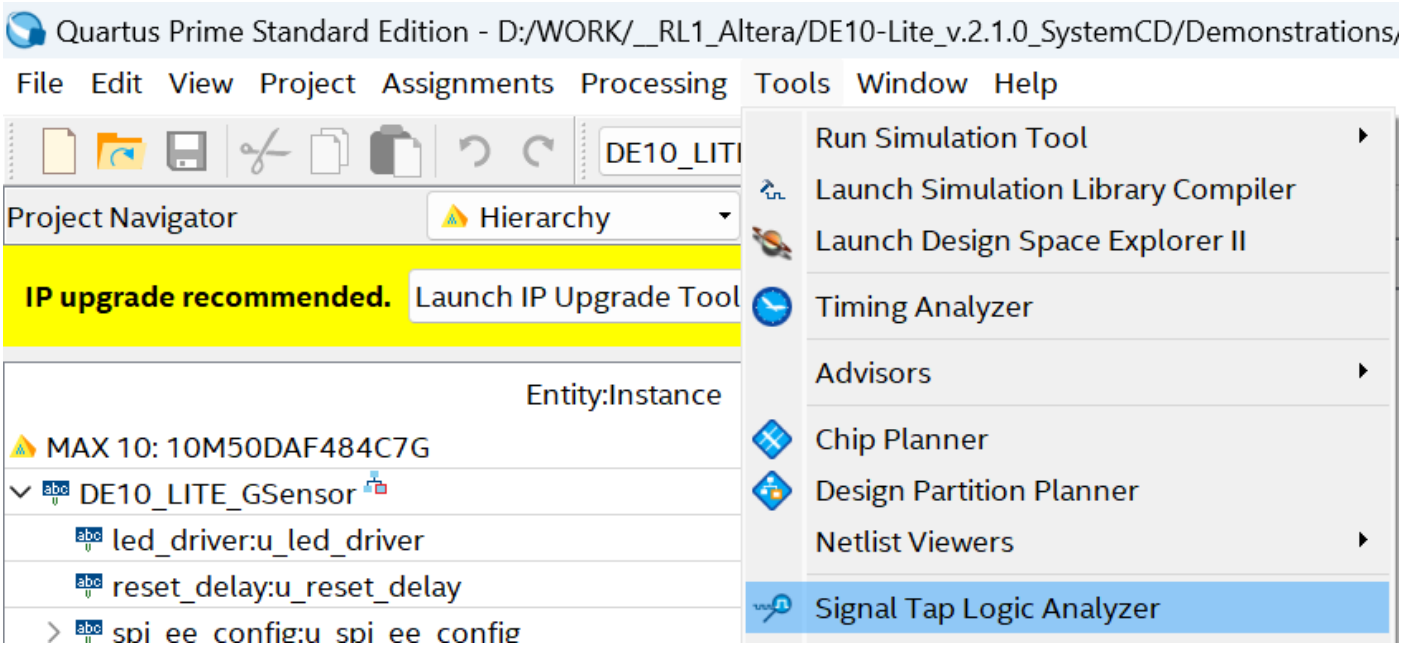
	Fmax	Restricted Fmax	Clock Name
1	217.39 MHz	217.39 MHz	u_spi_pll|altpll_component|auto_generated|pll1|clk[0]
2	223.71 MHz	223.71 MHz	MAX10_CLK1_50

Slow 1200mV 0C Model Fmax Summary

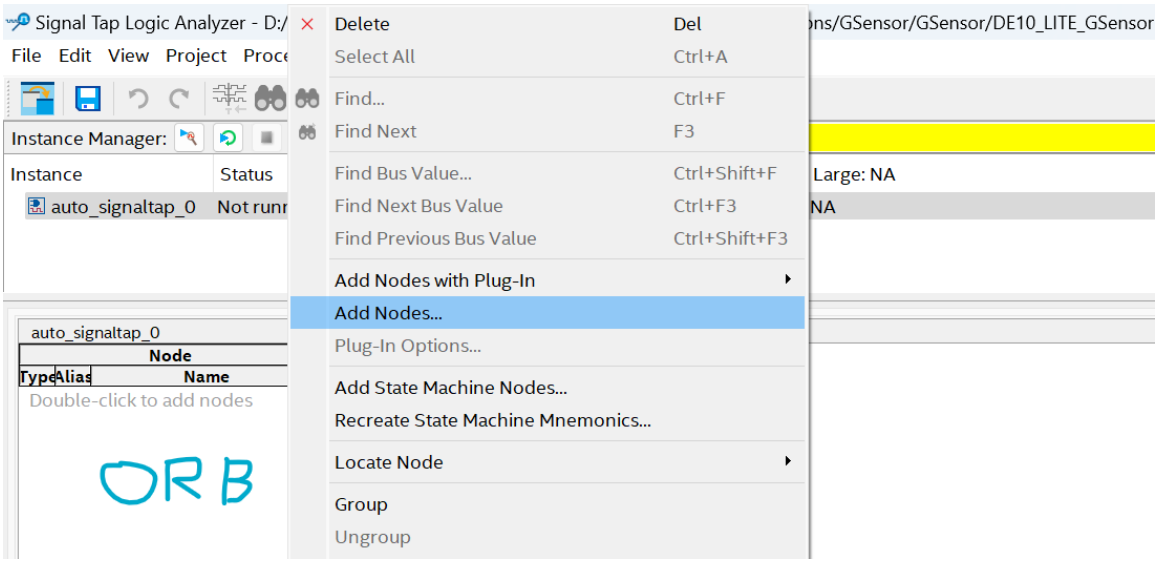
<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	238.89 MHz	238.89 MHz	u_spi_pll|altpll_component|auto_generated|pll1|clk[0]	
2	242.72 MHz	242.72 MHz	MAX10_CLK1_50	

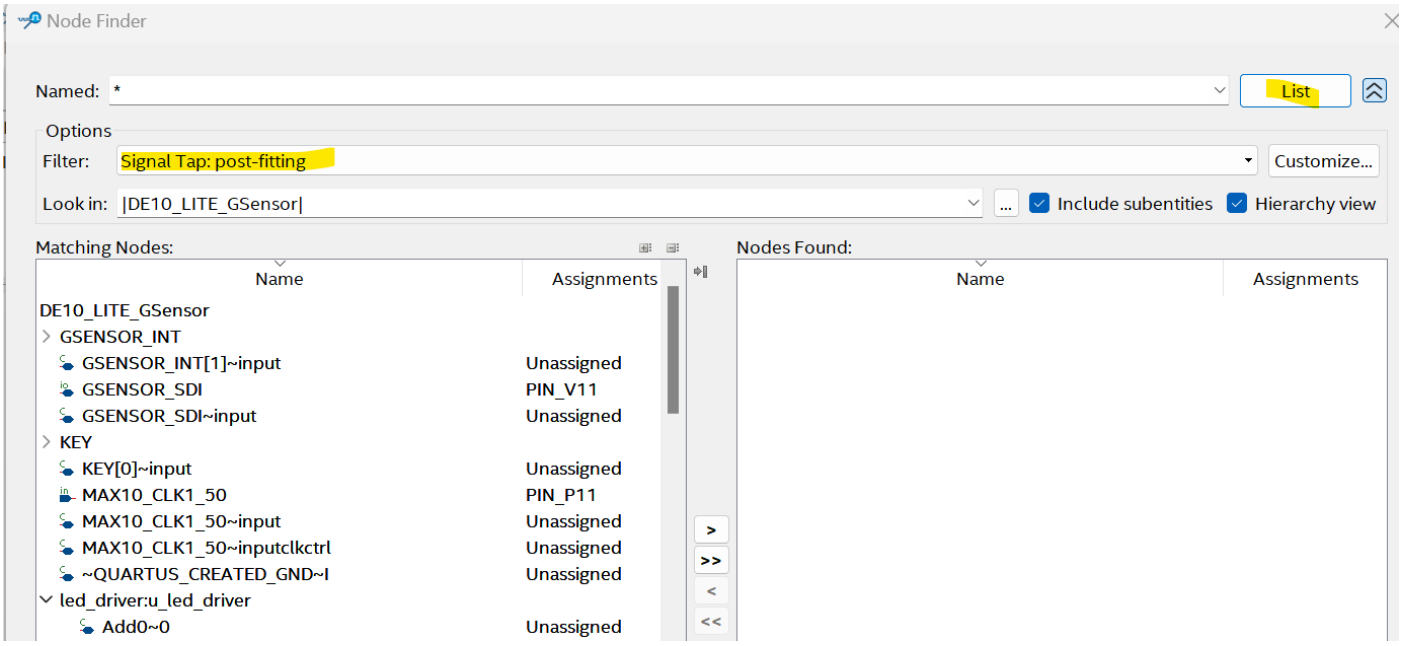
Открываем Signal Tap Logic Analyzer:



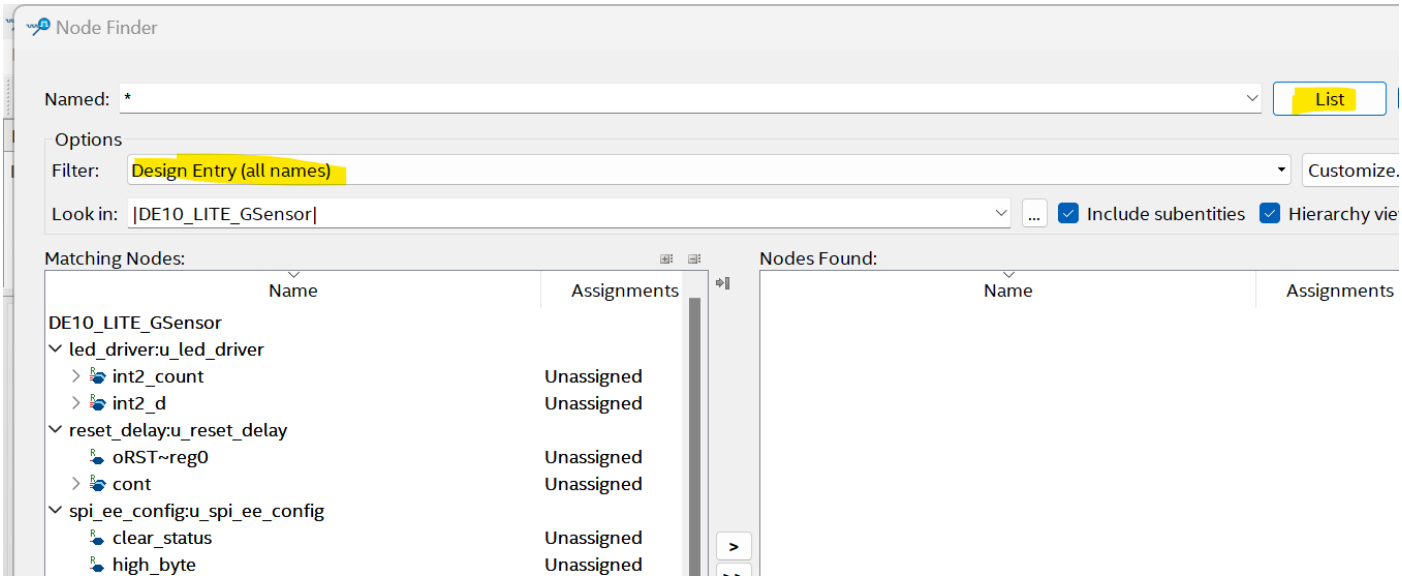
Правой кнопкой мышки – добавляем узлы:



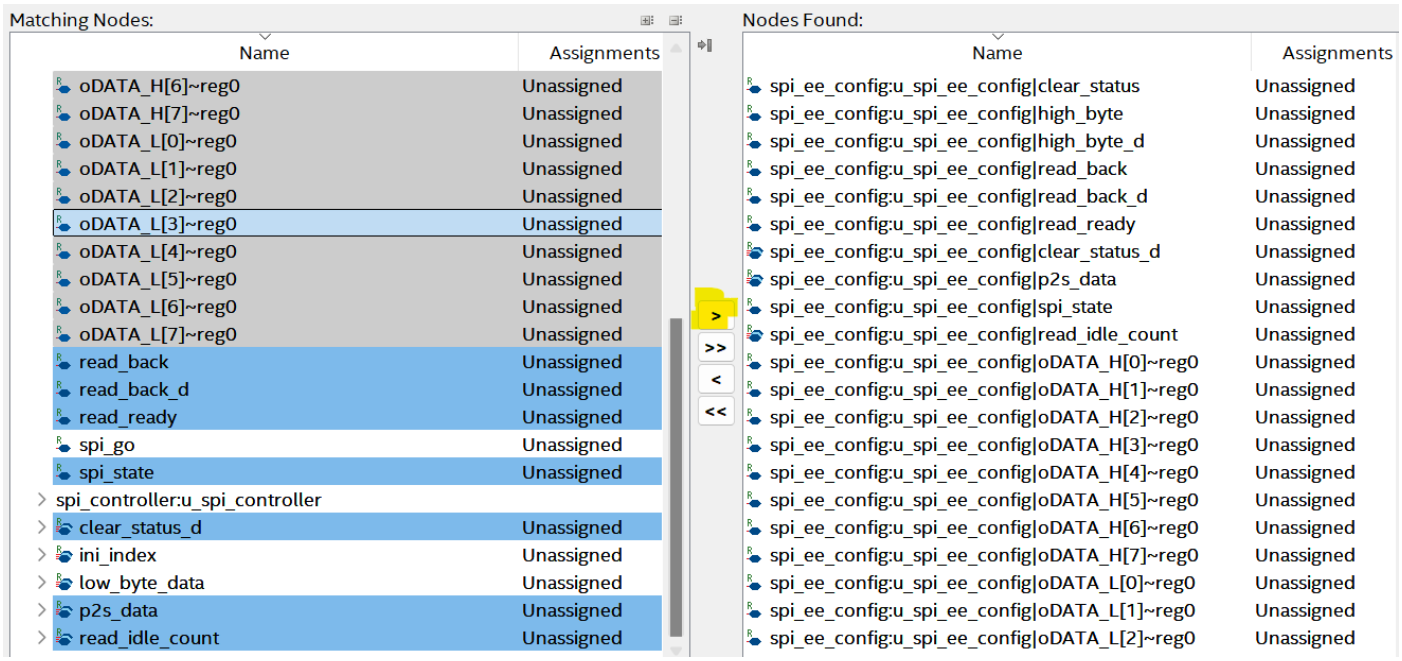
Вот так корявые имена:



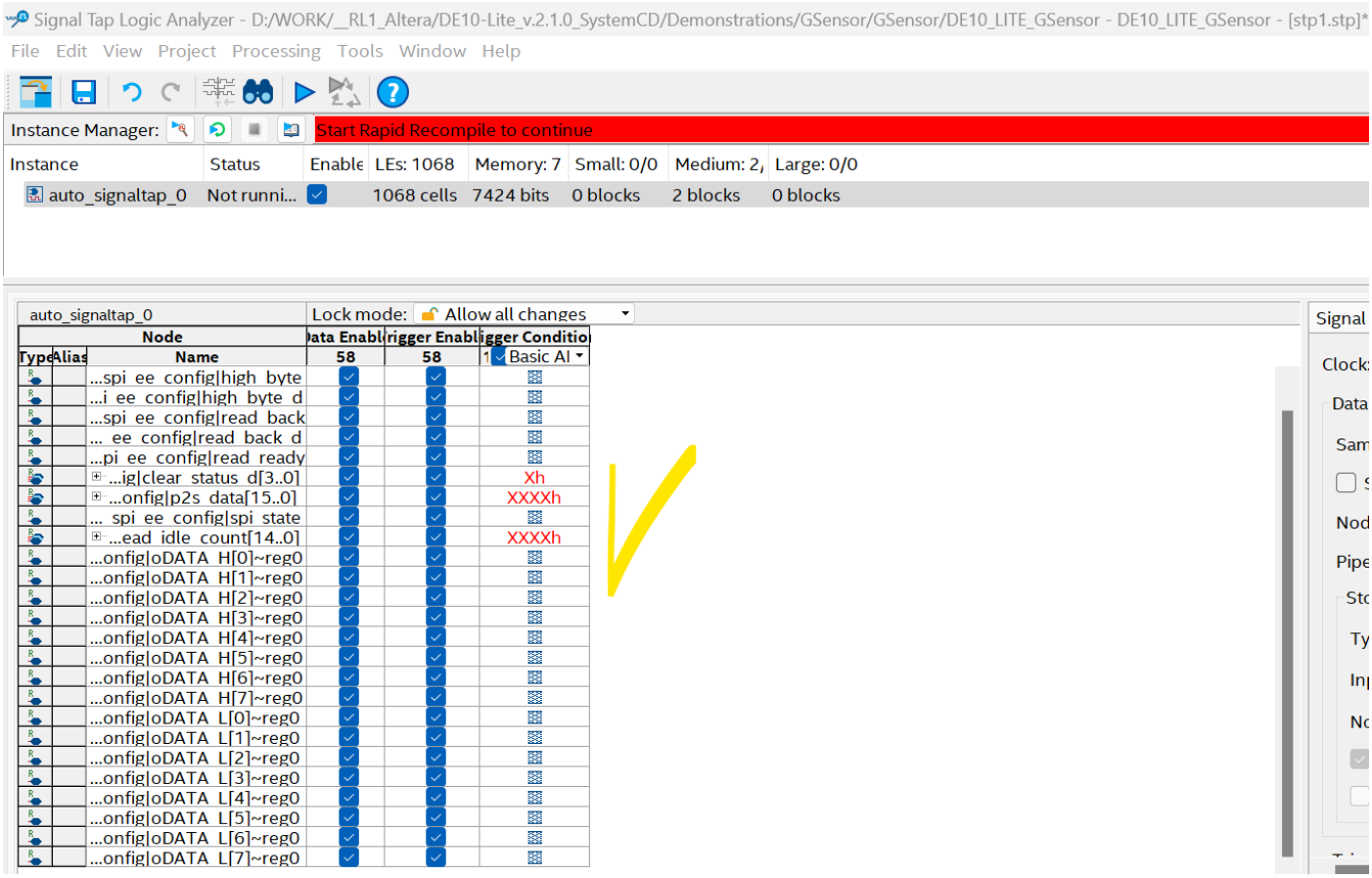
Вот так хорошие имена:



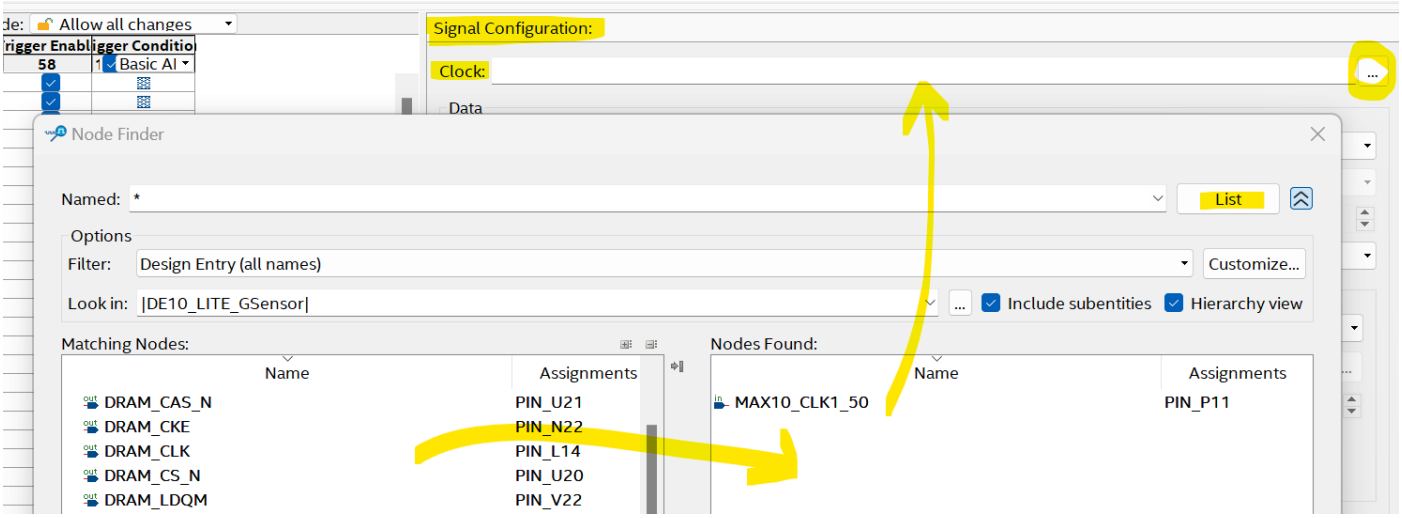
Добавляем сигналы для просмотра:



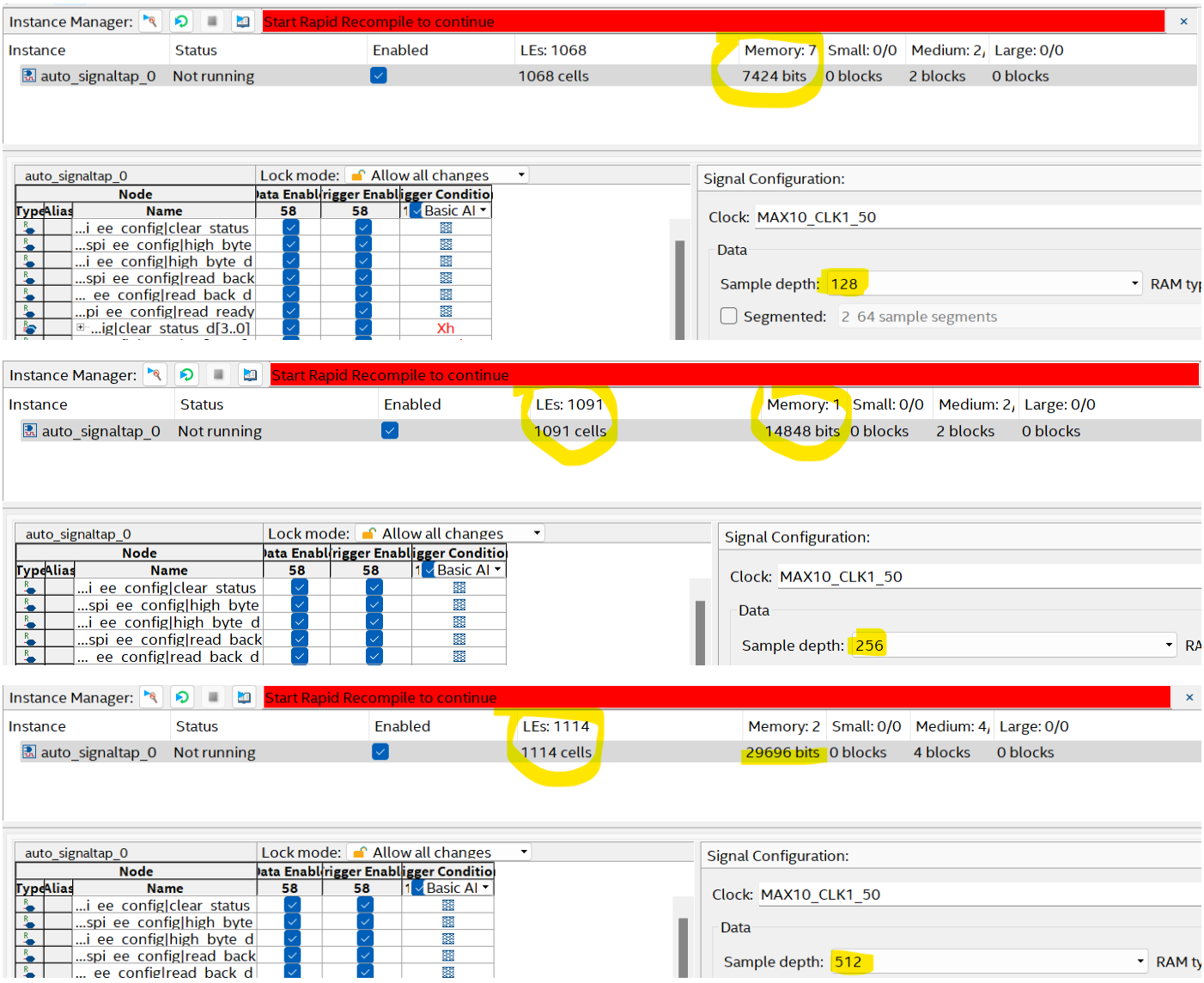
Видим:

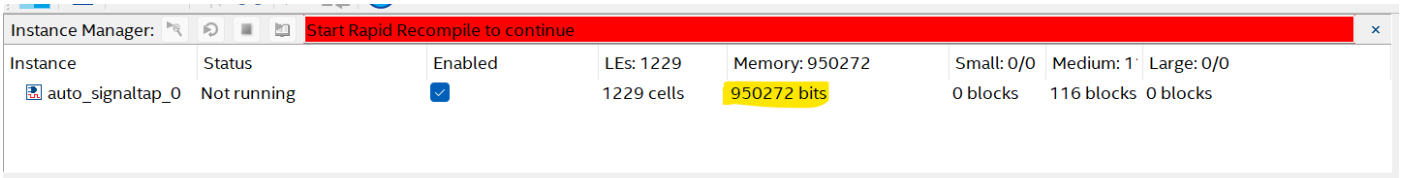


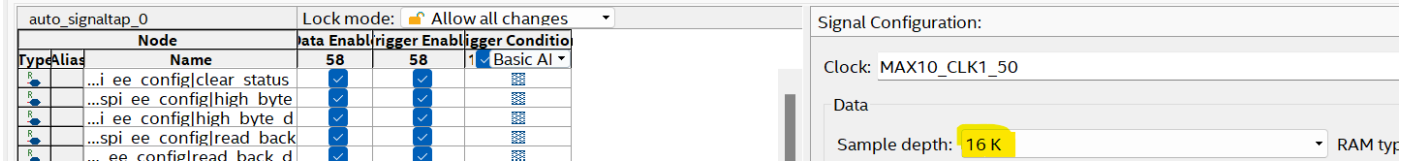
Выбираем сигнал тактирования SignalTap:



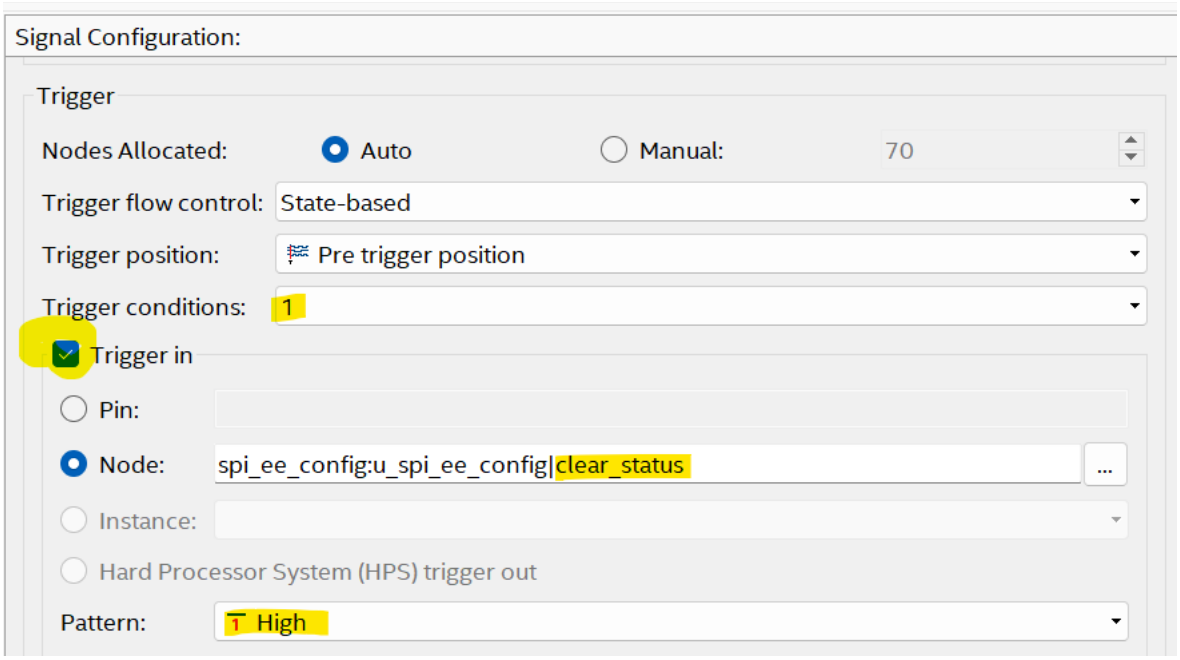
Выбираем глубину выборки... Чем больше глубина, тем больше BRAM юзается:



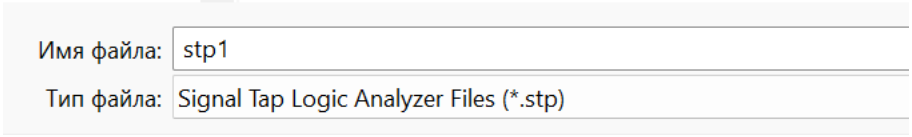




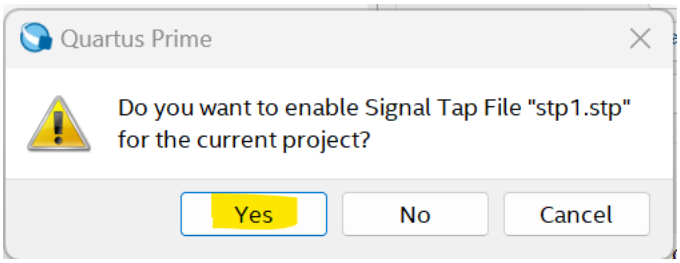
Настраиваем условие запуска Signal Tap:



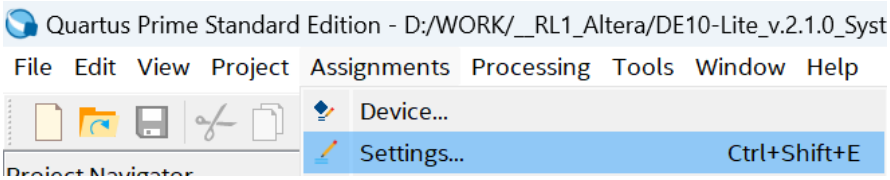
Сохраняем:

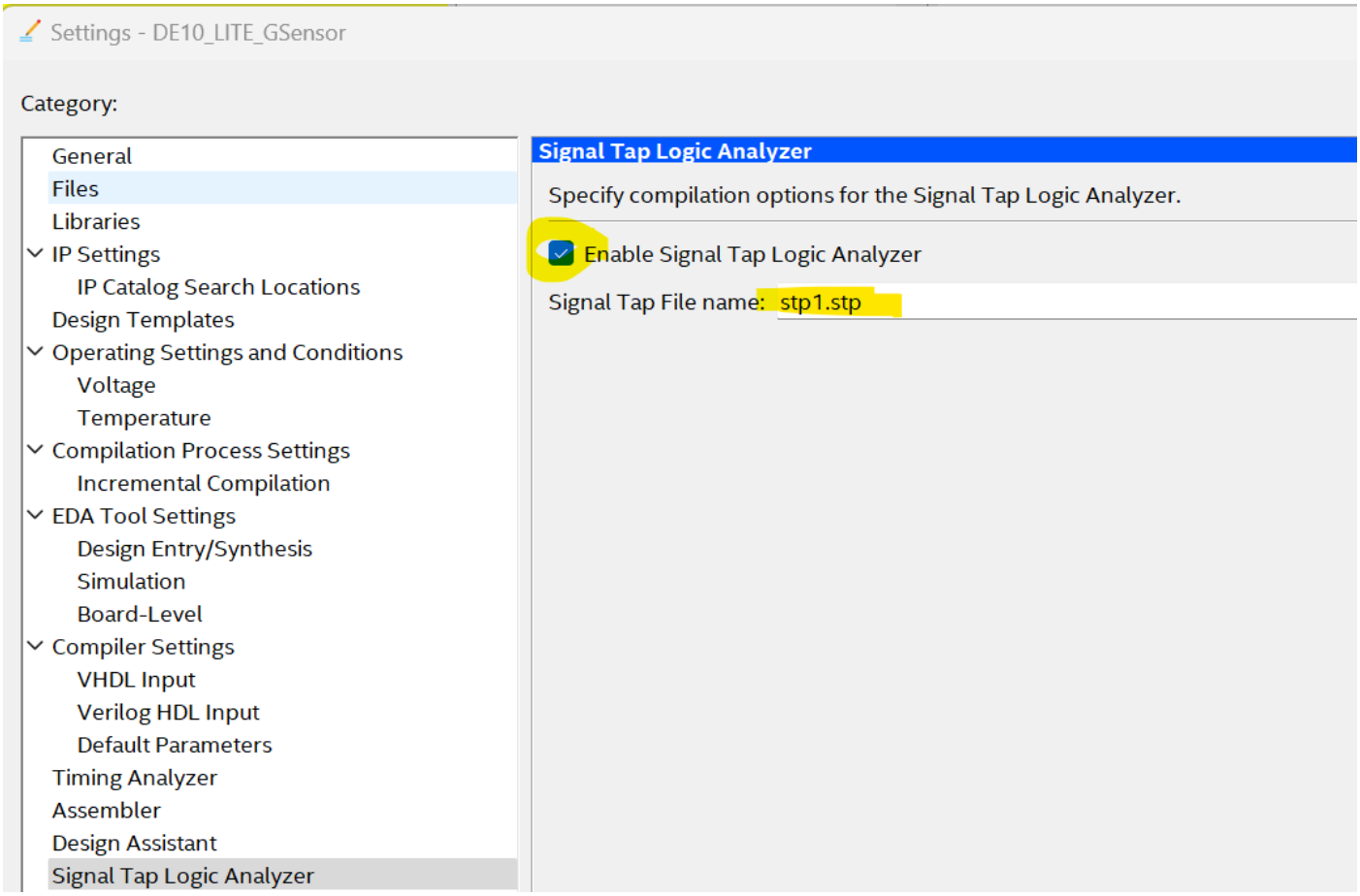


Соглашаемся добавить в проект:



Проверяем:





Компилим и смотрим на ресурсы:

Flow Summary

<<Filter>>

Flow Status	Successful - Sun Oct 27 00:17:09 2024
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Standard Edition
Revision Name	DE10_LITE_GSensor
Top-level Entity Name	DE10_LITE_GSensor
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	1,560 / 49,760 (3 %)
Total registers	1314
Total pins	101 / 360 (28 %)
Total virtual pins	0
Total memory bits	1,146,880 / 1,677,312 (68 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	1 / 4 (25 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

Стало:

Slow 1200mV 85C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name
1	72.66 MHz	72.66 MHz	altera_reserved_tck
2	111.11 MHz	111.11 MHz	MAX10_CLK1_50
3	208.81 MHz	208.81 MHz	u_spi_pll|altpll_component|auto_generated|pll1|clk[0]

Было:

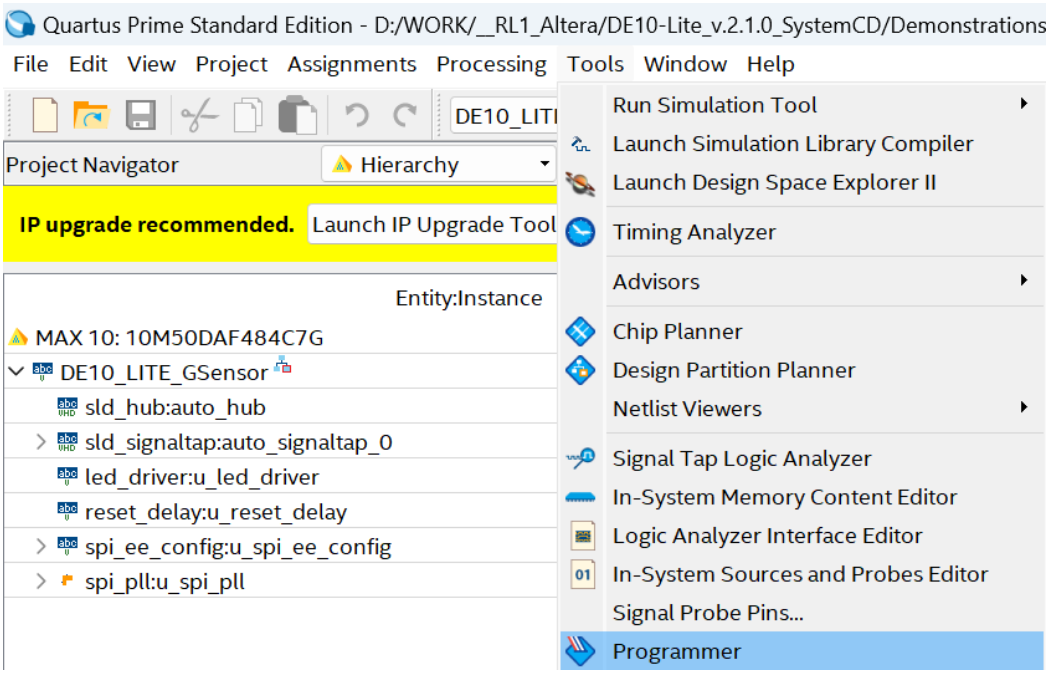
Slow 1200mV 85C Model Fmax Summary

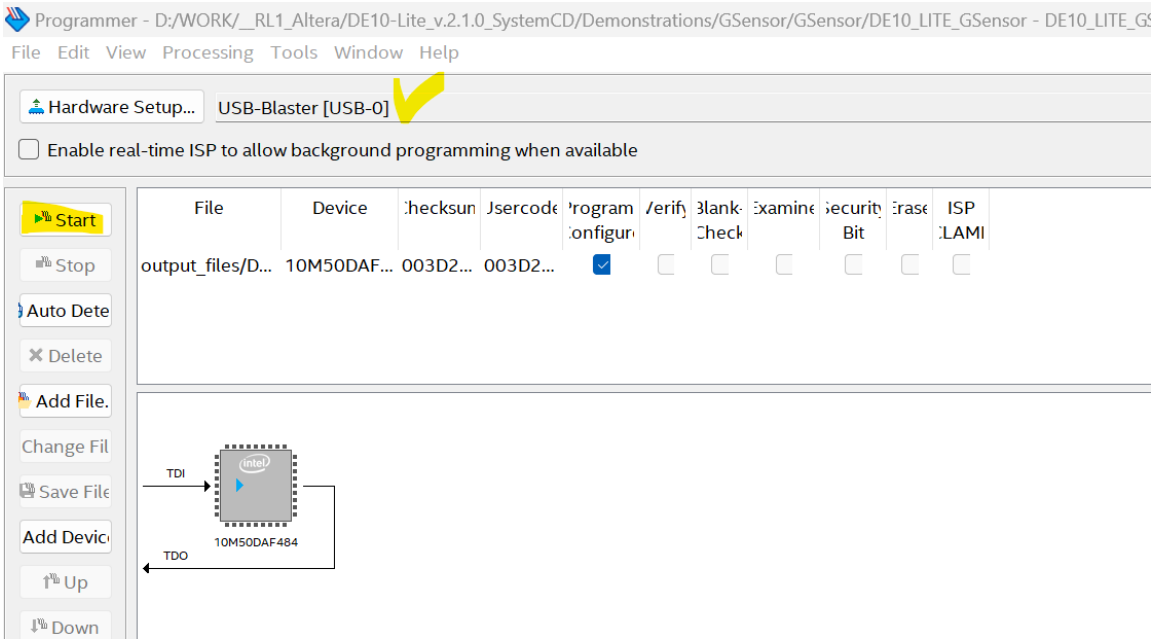
<<Filter>>

	Fmax	Restricted Fmax	Clock Name
1	217.39 MHz	217.39 MHz	u_spi_pll|altpll_component|auto_generated|pll1|clk[0]
2	223.71 MHz	223.71 MHz	MAX10_CLK1_50

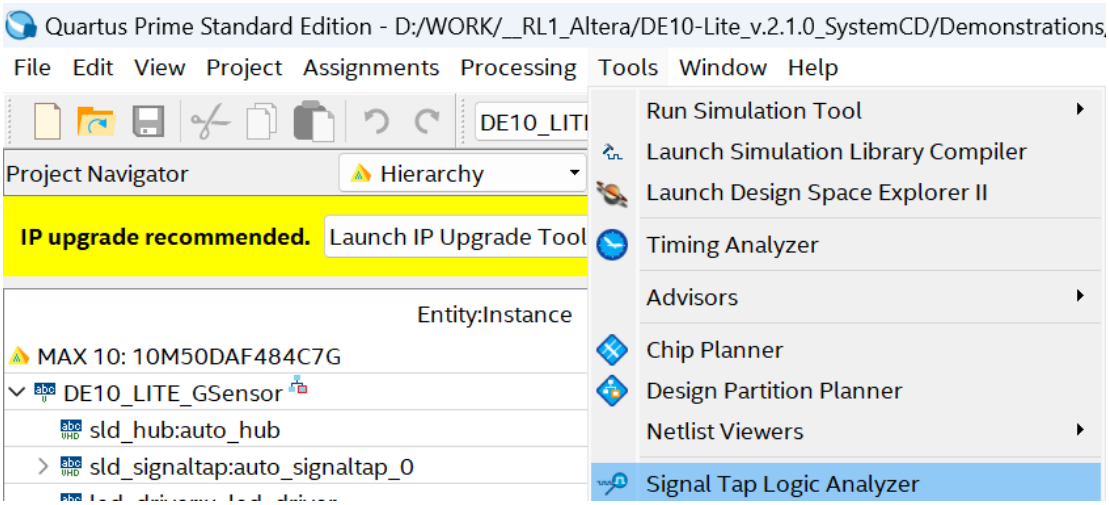
Макс частота работы схемы упала с 217 до 208 МГц

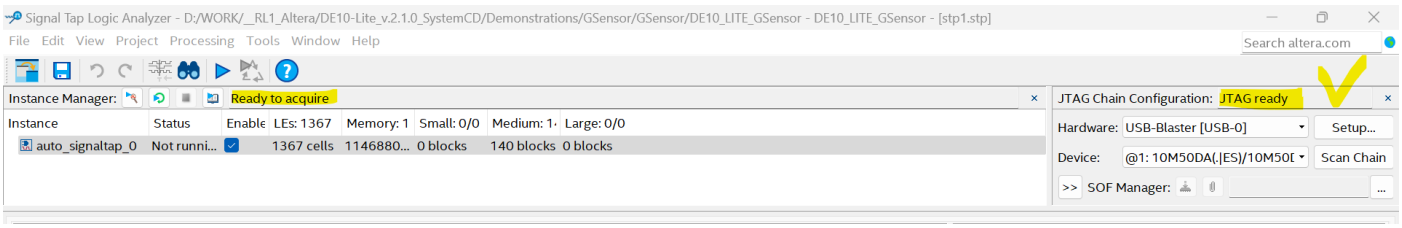
Зашиваем плату:

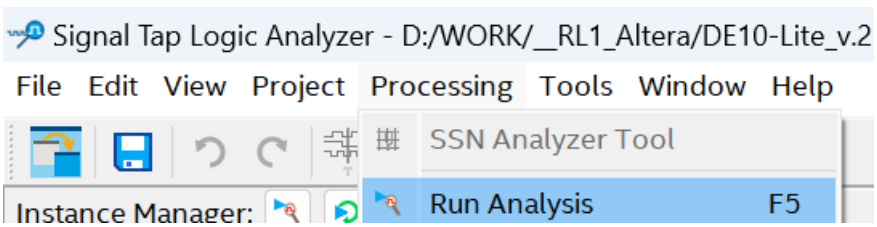


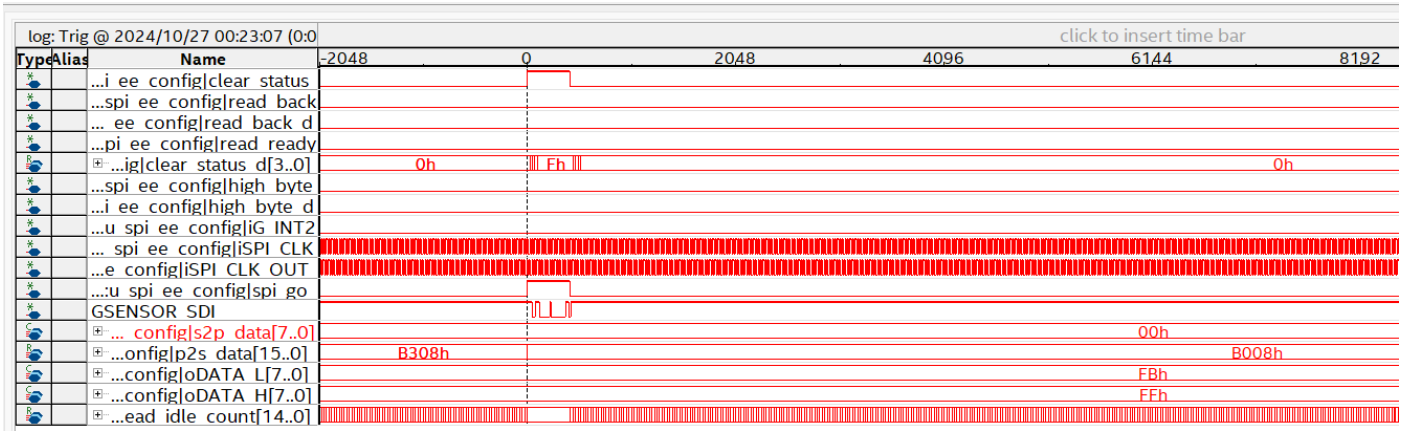


Запускаем Signal_Tap:

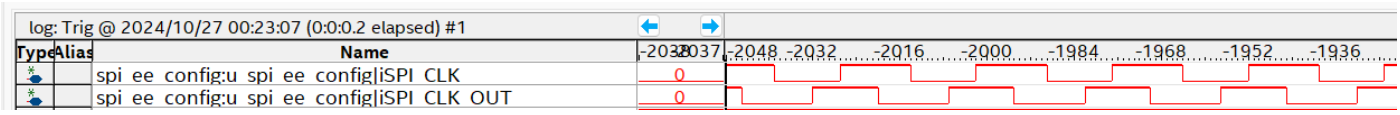


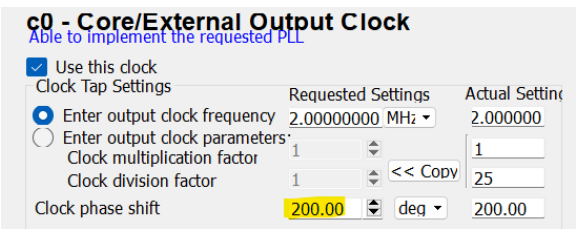


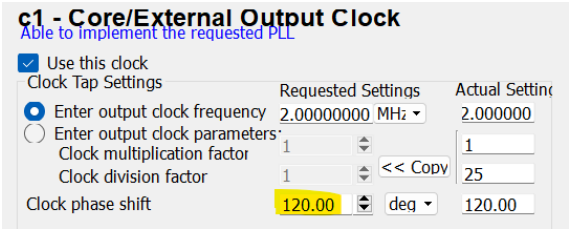




Смотрим что у нас с клоками

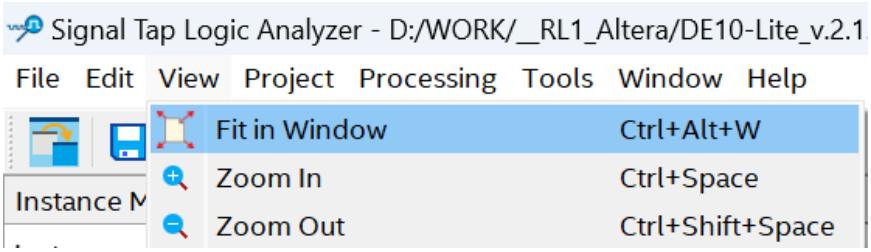




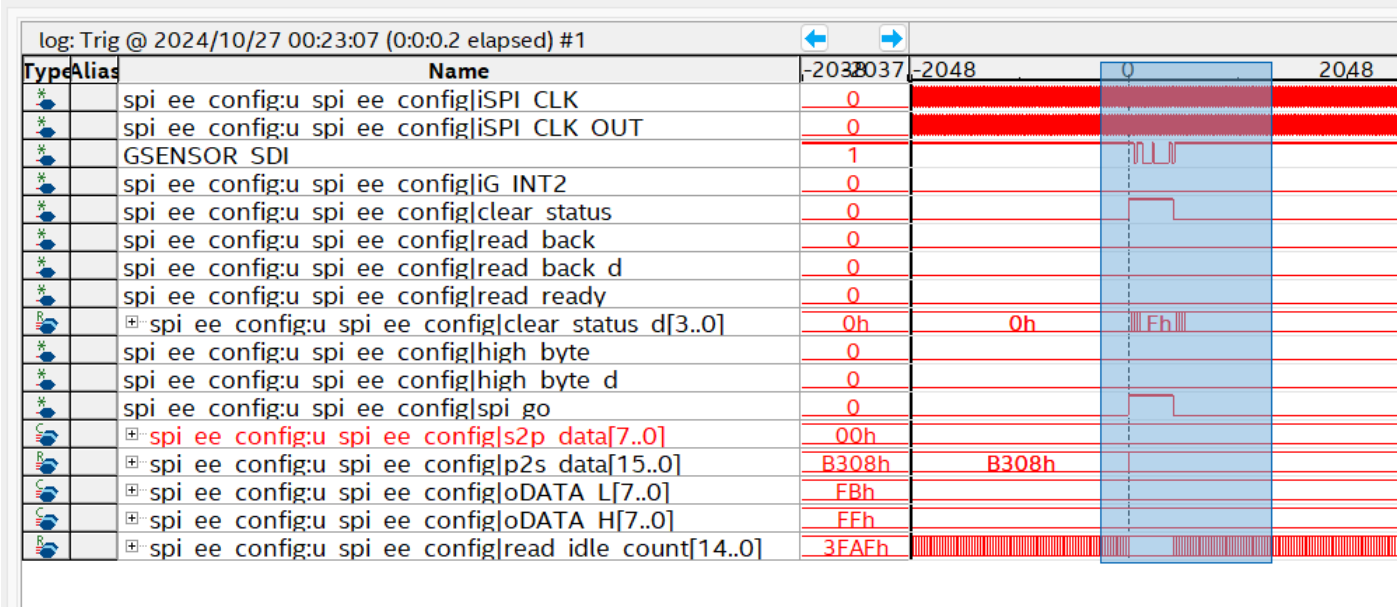


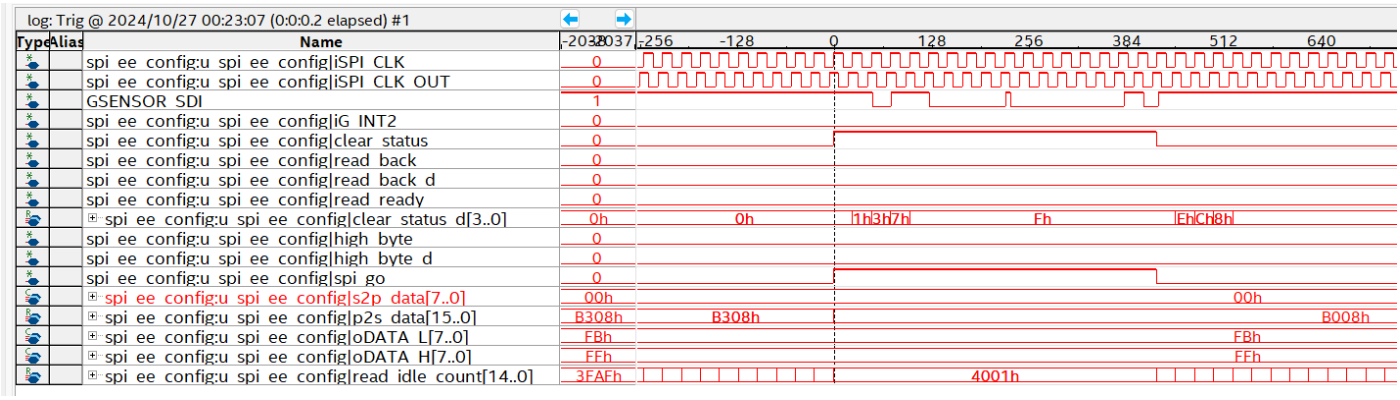

```
102  //  PLL
103  spi_pll     u_spi_pll
104  (
105      .areset  (dly_rst),
106      .inclk0  (MAX10_CLK1_50),
107      .c0      (spi_clk),       // 2MHz
108      .c1      (spi_clk_out)    // 2MHz phase shift
109  );
```

Управление зумом:



Мышкой можно выделить зону для увеличения:





Что мы видим?

1) INT2 = 0, не было прерывания от акселя
2) А вот в счетчике N-й бит стал равен = 1, значит это «чтение по таймауту», когда счетчик досчитал
3) Вот стадия считывания регистра источника прерываний
4) Ну и запуск SPI транзакции для этого считывания
   P2S_data = 0xB008

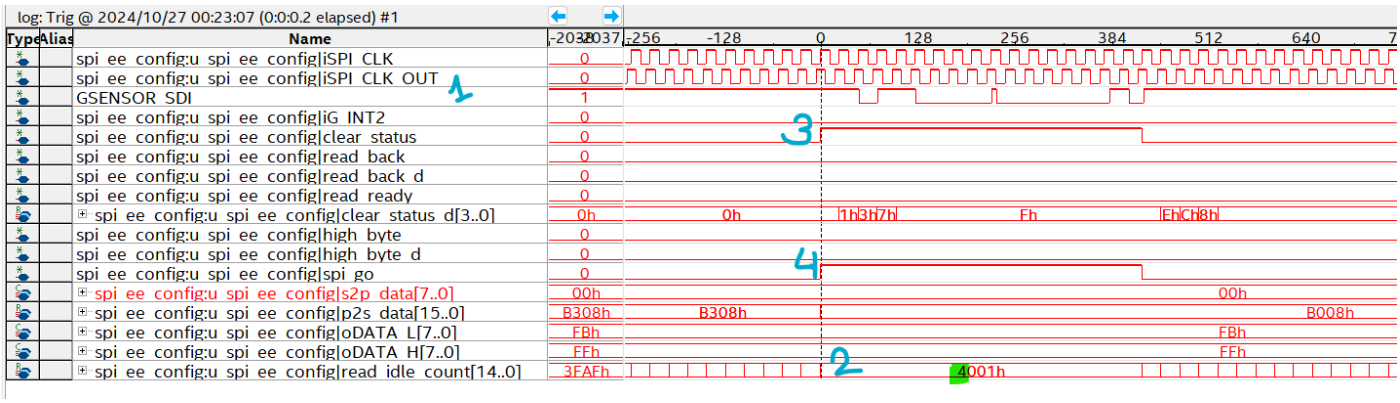


Figure 5 shows the timing diagram for SPI Mode 3. In this mode, the clock polarity is 1, which indicates that the idle state of the clock signal is high. The clock phase in this mode is 1, which indicates that the data is sampled on the rising edge (shown by the orange dotted line) and the data is shifted on the falling edge (shown by the dotted blue line) of the clock signal.

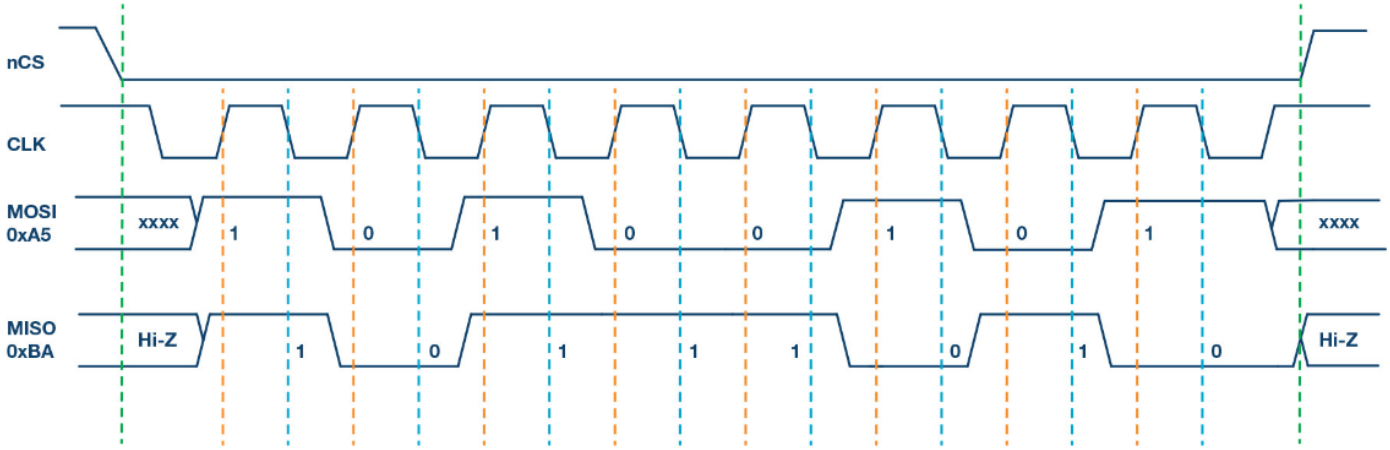
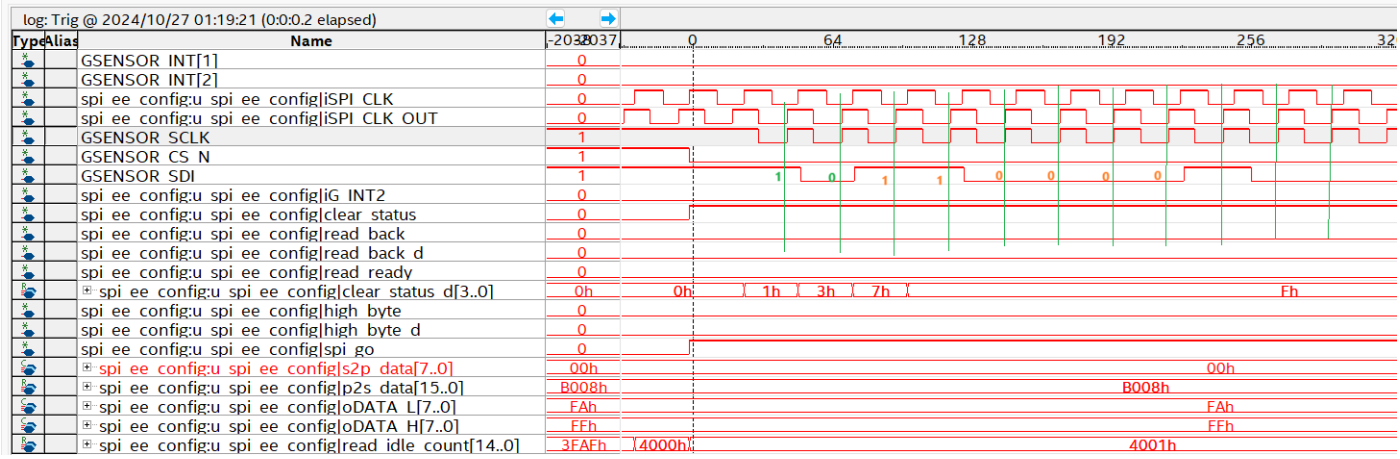


Figure 5. SPI Mode 3, CPOL = 1, CPHA = 1: CLK idle state = high, data sampled on the rising edge and shifted on the falling edge.

Т.е. аксель (слейв) засчелкивает данные по фронту своего клока, и засчелкивает 10_110000, Read Mode, MB = 0, reg_addr = 0x30 (interrupt source)



Вот чтение данных ускорения: