

Компилируем проект, запоминаем кол-во ресурсов и времянки.

Flow Status	Successful - Sat Oct 26 23:47:46 2024
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Standard Edition
Revision Name	DE10_LITE_GSensor
Top-level Entity Name	DE10_LITE_GSensor
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	186 / 49,760 (< 1 %)
Total registers	114
Total pins	101 / 360 (28 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	1 / 4 (25 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

Slow 1200mV 85C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name
1	217.39 MHz	217.39 MHz	u_spi_pll altpll_component auto_generated pll1 clk[0]
2	223.71 MHz	223.71 MHz	MAX10_CLK1_50

Slow 1200mV 0C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	238.89 MHz	238.89 MHz	u_spi_pll altpll_component auto_generated pll1 clk[0]	
2	242.72 MHz	242.72 MHz	MAX10_CLK1_50	

Открываем Signal Tap Logic Analyzer:

Quartus Prime Standard Edition - D:/WORK/_RL1_Altera/DE10-Lite_v.2.1.0_SystemCD/Demonstrations,

File Edit View Project Assignments Processing Tools Window Help

DE10_LITE

Project Navigator Hierarchy

IP upgrade recommended. Launch IP Upgrade Tool

Entity:Instance

MAX 10: 10M50DAF484C7G

DE10_LITE_GSensor

led_driver:u_led_driver

reset_delay:u_reset_delay

spi ee config:u_spi ee config

Run Simulation Tool

Launch Simulation Library Compiler

Launch Design Space Explorer II

Timing Analyzer

Advisors

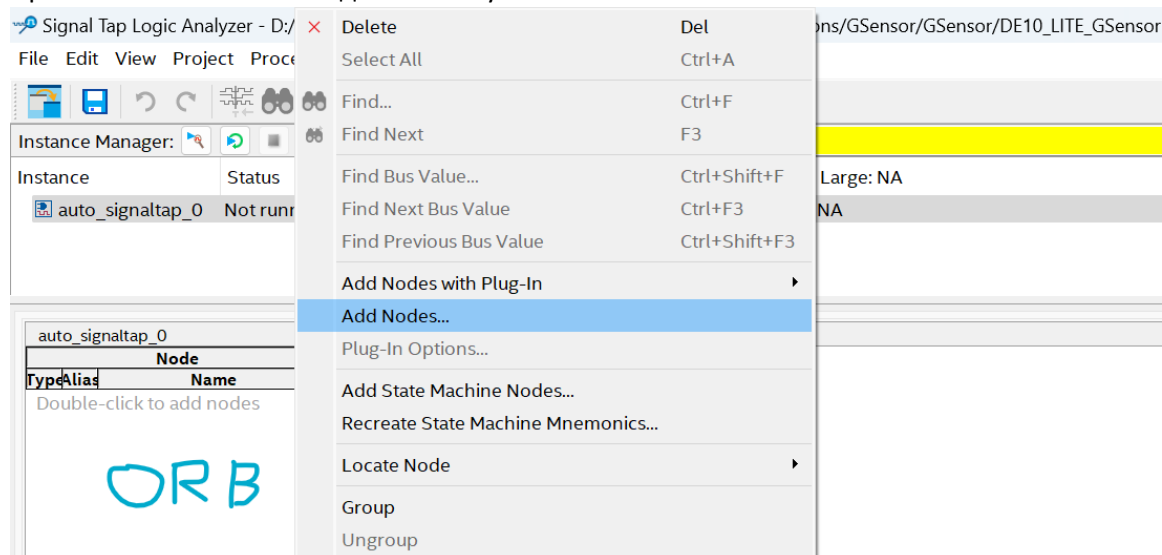
Chip Planner

Design Partition Planner

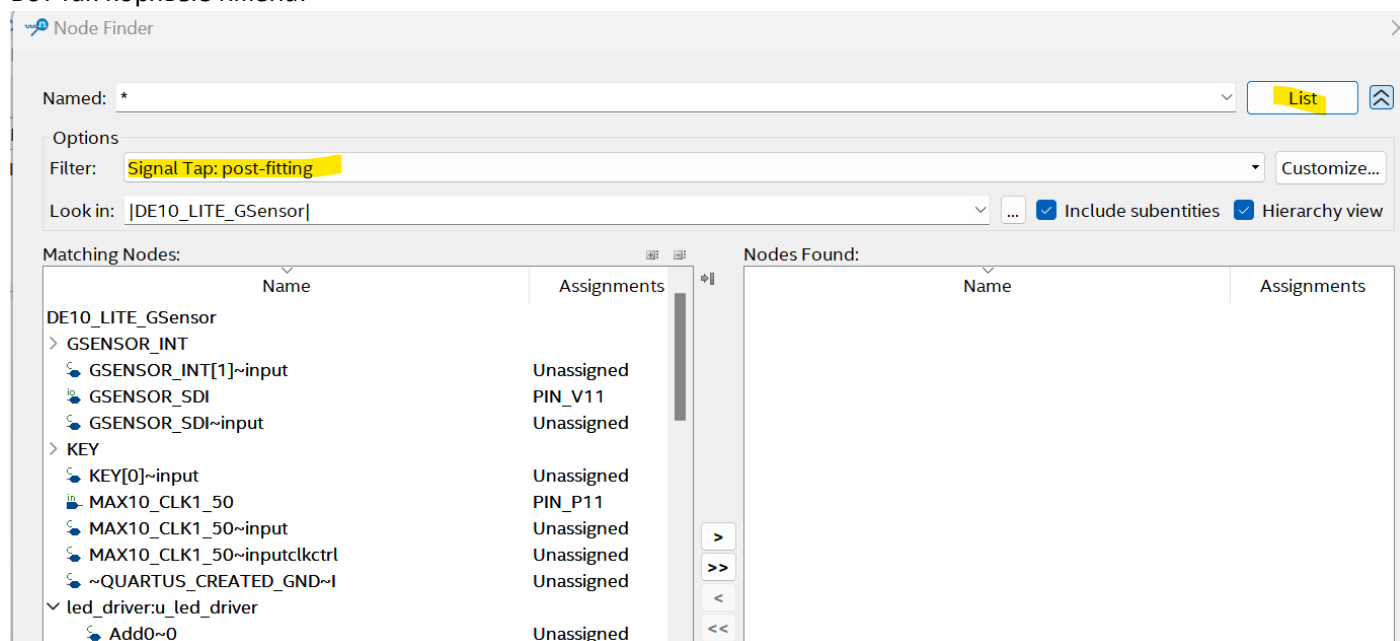
Netlist Viewers

Signal Tap Logic Analyzer

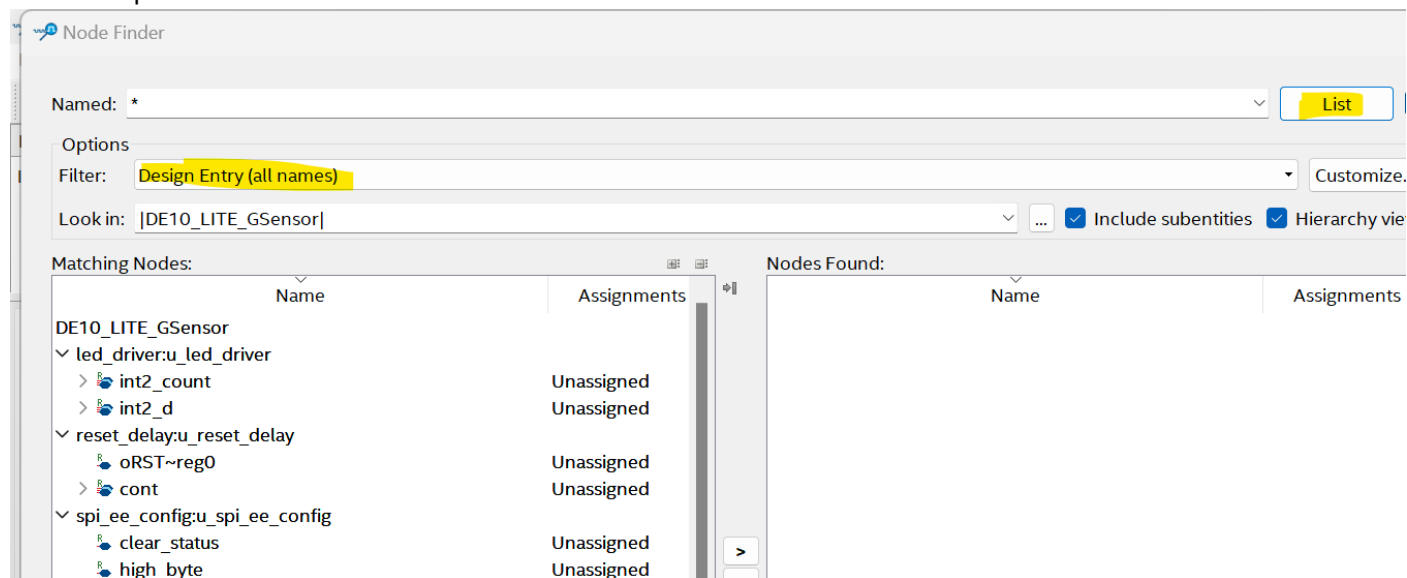
Правой кнопкой мышки – добавляем узлы:



Вот так корявые имена:



Вот так хорошие имена:



Добавляем сигналы для просмотра:

Matching Nodes:		Nodes Found:	
Name	Assignments	Name	Assignments
oDATA_H[6]~reg0	Unassigned	spi_ee_config:u_spi_ee_config clear_status	Unassigned
oDATA_H[7]~reg0	Unassigned	spi_ee_config:u_spi_ee_config high_byte	Unassigned
oDATA_L[0]~reg0	Unassigned	spi_ee_config:u_spi_ee_config high_byte_d	Unassigned
oDATA_L[1]~reg0	Unassigned	spi_ee_config:u_spi_ee_config read_back	Unassigned
oDATA_L[2]~reg0	Unassigned	spi_ee_config:u_spi_ee_config read_back_d	Unassigned
oDATA_L[3]~reg0	Unassigned	spi_ee_config:u_spi_ee_config read_ready	Unassigned
oDATA_L[4]~reg0	Unassigned	spi_ee_config:u_spi_ee_config clear_status_d	Unassigned
oDATA_L[5]~reg0	Unassigned	spi_ee_config:u_spi_ee_config p2s_data	Unassigned
oDATA_L[6]~reg0	Unassigned	spi_ee_config:u_spi_ee_config spi_state	Unassigned
oDATA_L[7]~reg0	Unassigned	spi_ee_config:u_spi_ee_config read_idle_count	Unassigned
read_back	Unassigned	spi_ee_config:u_spi_ee_config oDATA_H[0]~reg0	Unassigned
read_back_d	Unassigned	spi_ee_config:u_spi_ee_config oDATA_H[1]~reg0	Unassigned
read_ready	Unassigned	spi_ee_config:u_spi_ee_config oDATA_H[2]~reg0	Unassigned
spi_go	Unassigned	spi_ee_config:u_spi_ee_config oDATA_H[3]~reg0	Unassigned
spi_state	Unassigned	spi_ee_config:u_spi_ee_config oDATA_H[4]~reg0	Unassigned
spi_controller:u_spi_controller		spi_ee_config:u_spi_ee_config oDATA_H[5]~reg0	Unassigned
clear_status_d	Unassigned	spi_ee_config:u_spi_ee_config oDATA_H[6]~reg0	Unassigned
ini_index	Unassigned	spi_ee_config:u_spi_ee_config oDATA_H[7]~reg0	Unassigned
low_byte_data	Unassigned	spi_ee_config:u_spi_ee_config oDATA_L[0]~reg0	Unassigned
p2s_data	Unassigned	spi_ee_config:u_spi_ee_config oDATA_L[1]~reg0	Unassigned
read_idle_count	Unassigned	spi_ee_config:u_spi_ee_config oDATA_L[2]~reg0	Unassigned

Видим:

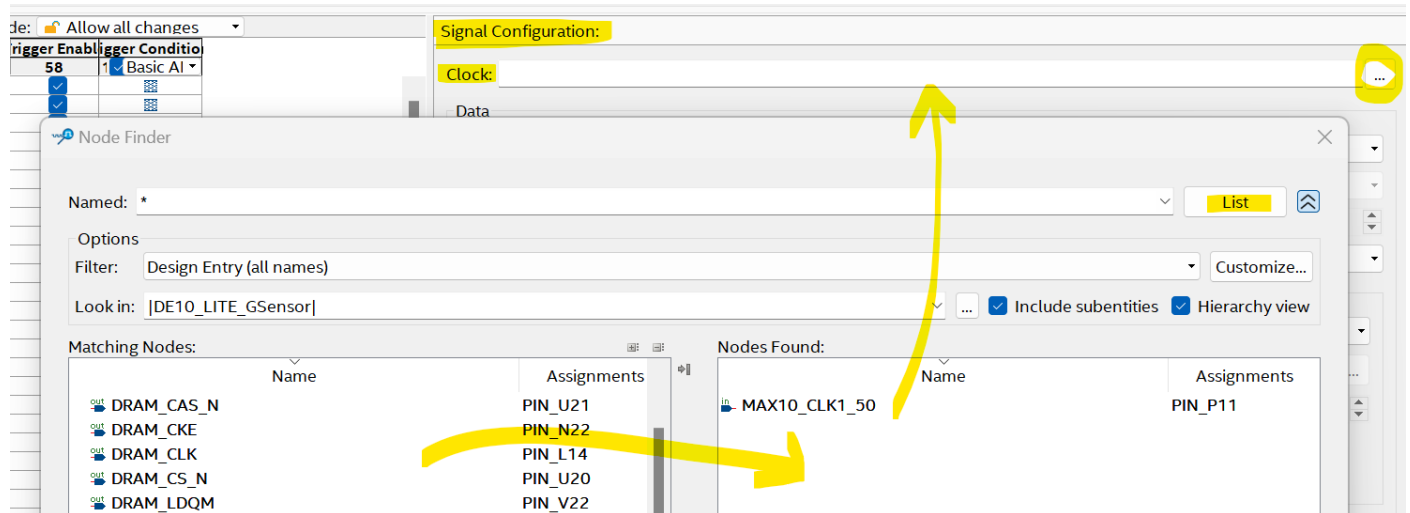
Signal Tap Logic Analyzer - D:\WORK_RL1_Altera\DE10-Lite_v2.1.0_SystemCD\Demonstrations\GSensor\GSensor\DE10_LITE_GSensor - DE10_LITE_GSensor - [stp1.stp]*

File Edit View Project Processing Tools Window Help

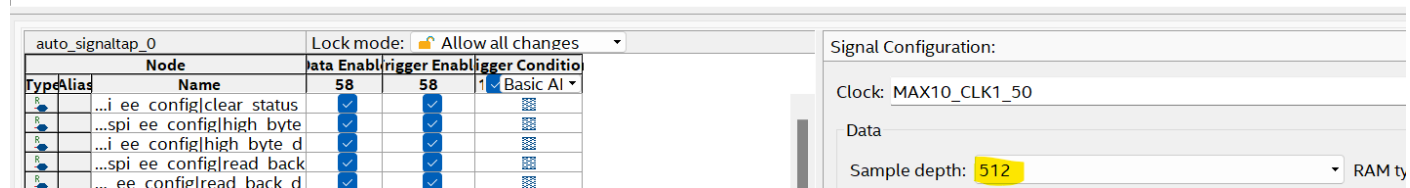
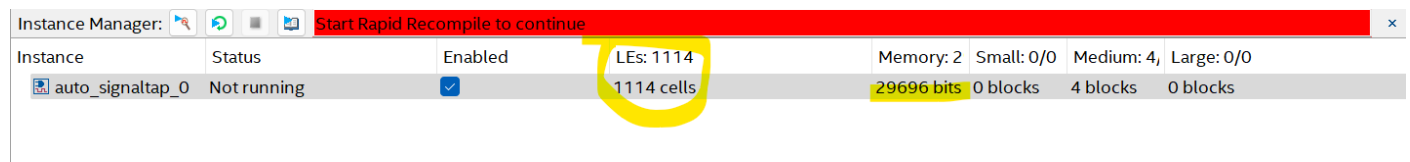
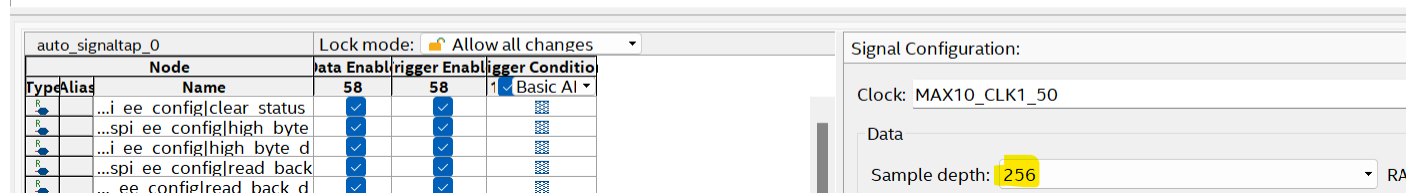
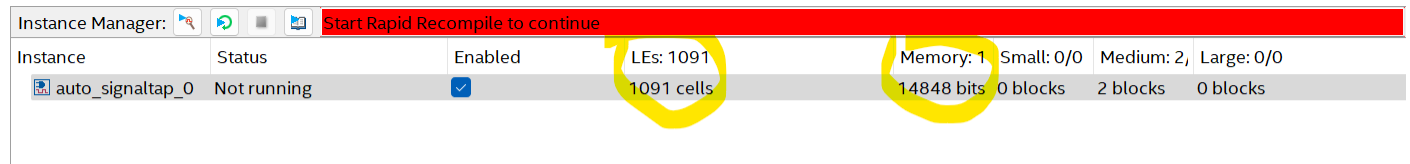
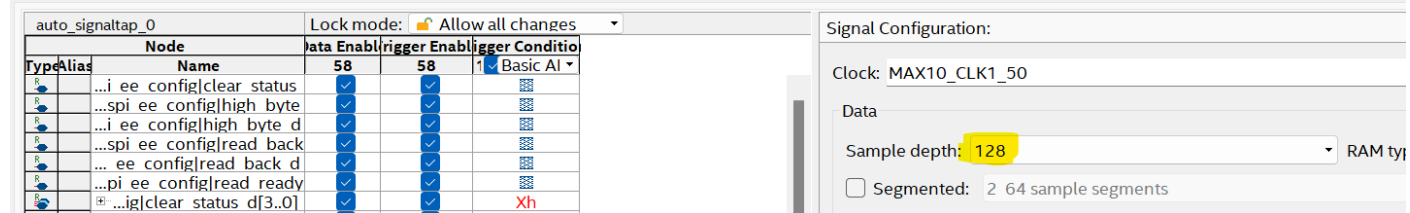
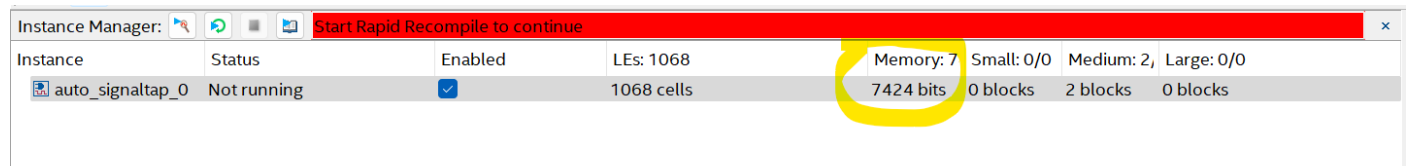
Instance Manager:		Start Rapid Recompile to continue				
Instance	Status	Enable	LEs: 1068	Memory: 7	Small: 0/0	Medium: 2, Large: 0/0
auto_signaltap_0	Not runni...	<input checked="" type="checkbox"/>	1068 cells	7424 bits	0 blocks	2 blocks 0 blocks

auto_signaltap_0		Lock mode: Allow all changes				Signal
Type	Alias	Name	58	58	1	Basic AI
		...spi_ee_config high byte	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...i_ee_config high byte d	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...spi_ee_config read back	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...ee_config read back d	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...pi_ee_config read ready	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...ig clear status d[3..0]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Xh
		...onfig p2s_data[15..0]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	XXXXXh
		...spi_ee_config spi_state	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...ead idle count[14..0]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	XXXXXh
		...onfig oDATA_H[0]~reg0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...onfig oDATA_H[1]~reg0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...onfig oDATA_H[2]~reg0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...onfig oDATA_H[3]~reg0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...onfig oDATA_H[4]~reg0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...onfig oDATA_H[5]~reg0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...onfig oDATA_H[6]~reg0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...onfig oDATA_H[7]~reg0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...onfig oDATA_L[0]~reg0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...onfig oDATA_L[1]~reg0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...onfig oDATA_L[2]~reg0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...onfig oDATA_L[3]~reg0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...onfig oDATA_L[4]~reg0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...onfig oDATA_L[5]~reg0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...onfig oDATA_L[6]~reg0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
		...onfig oDATA_L[7]~reg0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	

Выбираем сигнал тактирования SignalTap:



Выбираем глубину выборки... Чем больше глубина, тем больше BRAM юзается:



Instance Manager: Start Rapid Recompile to continue

Instance	Status	Enabled	LEs: 1229	Memory: 950272	Small: 0/0	Medium: 1	Large: 0/0
auto_signaltap_0	Not running	<input checked="" type="checkbox"/>	1229 cells	950272 bits	0 blocks	116 blocks	0 blocks

auto_signaltap_0 Lock mode: Allow all changes

Type	Alias	Name	58	58	1	Basic AI
...	...	ee_config clear_status	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
...	...	ee_config high_byte_d	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
...	...	ee_config high_byte_d	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
...	...	ee_config read_back	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
...	...	ee_config read_back_d	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

Signal Configuration:

Clock: MAX10_CLK1_50

Data

Sample depth: 16 K RAM type

Настраиваем условие запуска Signal Tap:

Signal Configuration:

Trigger

Nodes Allocated: ☒ Auto ☐ Manual: 70

Trigger flow control: State-based

Trigger position: Pre trigger position

Trigger conditions: 1

☒ Trigger in

☐ Pin:

☒ Node: spi_ee_config:u_spi_ee_config|clear_status

☐ Instance:

☐ Hard Processor System (HPS) trigger out

Pattern: High

Сохраняем:

Имя файла: stp1

Тип файла: Signal Tap Logic Analyzer Files (*.stp)

Соглашаемся добавить в проект:

Quartus Prime

Do you want to enable Signal Tap File "stp1.stp" for the current project?

Yes No Cancel

Проверяем:

Quartus Prime Standard Edition - D:/WORK/_RL1_Altera/DE10-Lite_v.2.1.0_Syst

File Edit View Project Assignments Processing Tools Window Help

Device... Settings... Ctrl+Shift+E

Settings - DE10_LITE_GSensor

Category:

- General
- Files
- Libraries
- IP Settings
 - IP Catalog Search Locations
- Design Templates
- Operating Settings and Conditions
 - Voltage
 - Temperature
- Compilation Process Settings
 - Incremental Compilation
- EDA Tool Settings
 - Design Entry/Synthesis
 - Simulation
 - Board-Level
- Compiler Settings
 - VHDL Input
 - Verilog HDL Input
 - Default Parameters
- Timing Analyzer
- Assembler
- Design Assistant
- Signal Tap Logic Analyzer

Signal Tap Logic Analyzer

Specify compilation options for the Signal Tap Logic Analyzer.

☒ Enable Signal Tap Logic Analyzer

Signal Tap File name: stp1.stp

Компилим и смотрим на ресурсы:

Flow Summary	
<<Filter>>	
Flow Status	Successful - Sun Oct 27 00:17:09 2024
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Standard Edition
Revision Name	DE10_LITE_GSensor
Top-level Entity Name	DE10_LITE_GSensor
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	1,560 / 49,760 (3 %)
Total registers	1314
Total pins	101 / 360 (28 %)
Total virtual pins	0
Total memory bits	1,146,880 / 1,677,312 (68 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	1 / 4 (25 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

Стало:

Slow 1200mV 85C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name
1	72.66 MHz	72.66 MHz	altera_reserved_tck
2	111.11 MHz	111.11 MHz	MAX10_CLK1_50
3	208.81 MHz	208.81 MHz	u_spi_pll altpll_component auto_generated pll1 clk[0]

Было:

Slow 1200mV 85C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name
1	217.39 MHz	217.39 MHz	u_spi_pll altpll_component auto_generated pll1 clk[0]
2	223.71 MHz	223.71 MHz	MAX10_CLK1_50

Макс частота работы схемы упала с 217 до 208 МГц

Зашиваем плату:

Quartus Prime Standard Edition - D:/WORK/_RL1_Altera/DE10-Lite_v.2.1.0_SystemCD/Demonstrations

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Hierarchy

IP upgrade recommended. Launch IP Upgrade Tool

Entity:Instance

MAX 10: 10M50DAF484C7G

DE10_LITE_GSensor

- sld_hub:auto_hub
- > sld_signaltap:auto_signaltap_0
- led_driver:u_led_driver
- reset_delay:u_reset_delay
- > spi_ee_config:u_spi_ee_config
- > spi_pll:u_spi_pll

Run Simulation Tool

Launch Simulation Library Compiler

Launch Design Space Explorer II

Timing Analyzer

Advisors

Chip Planner

Design Partition Planner

Netlist Viewers

Signal Tap Logic Analyzer

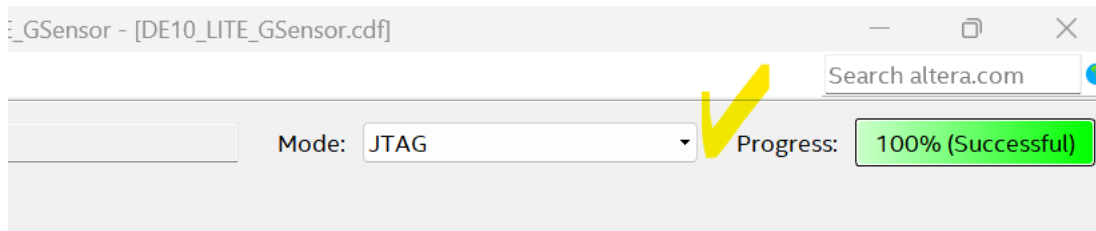
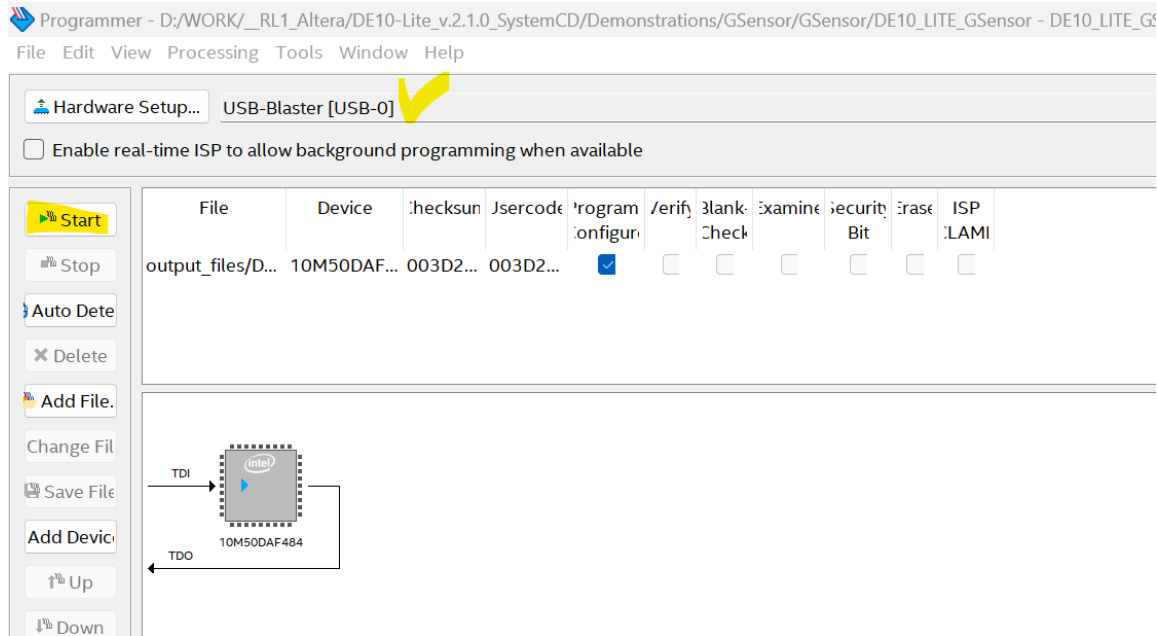
In-System Memory Content Editor

Logic Analyzer Interface Editor

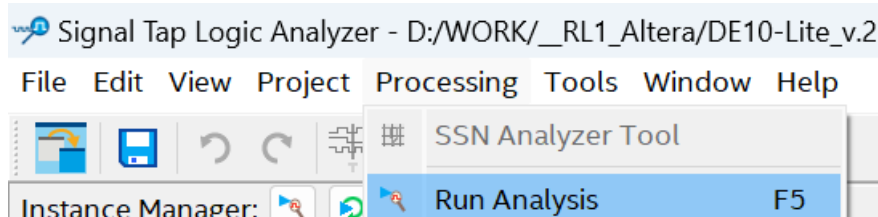
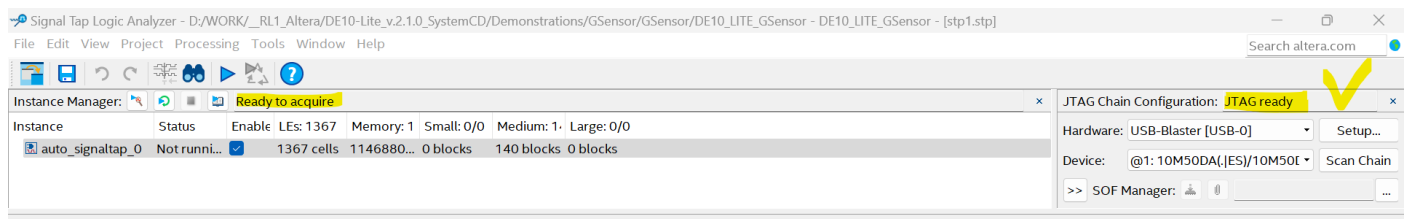
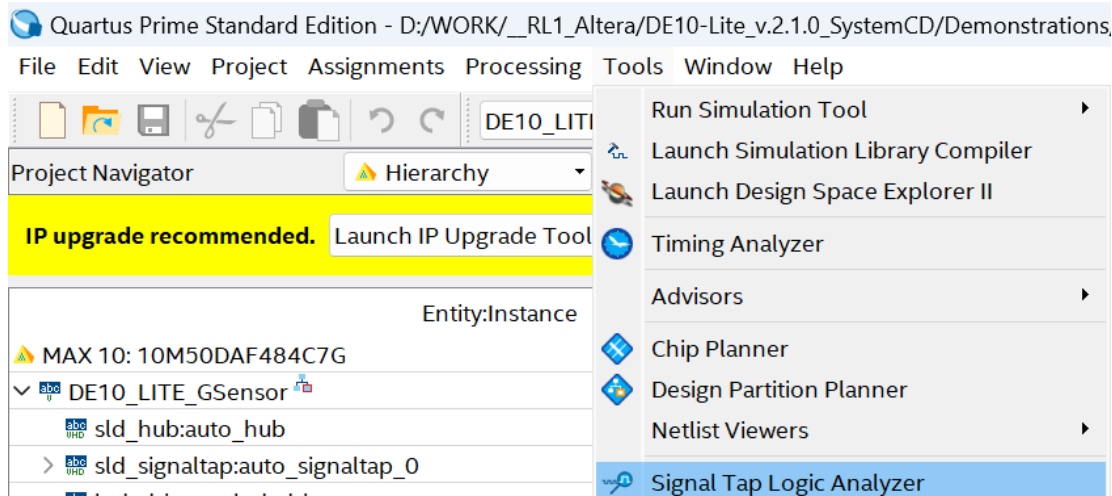
In-System Sources and Probes Editor

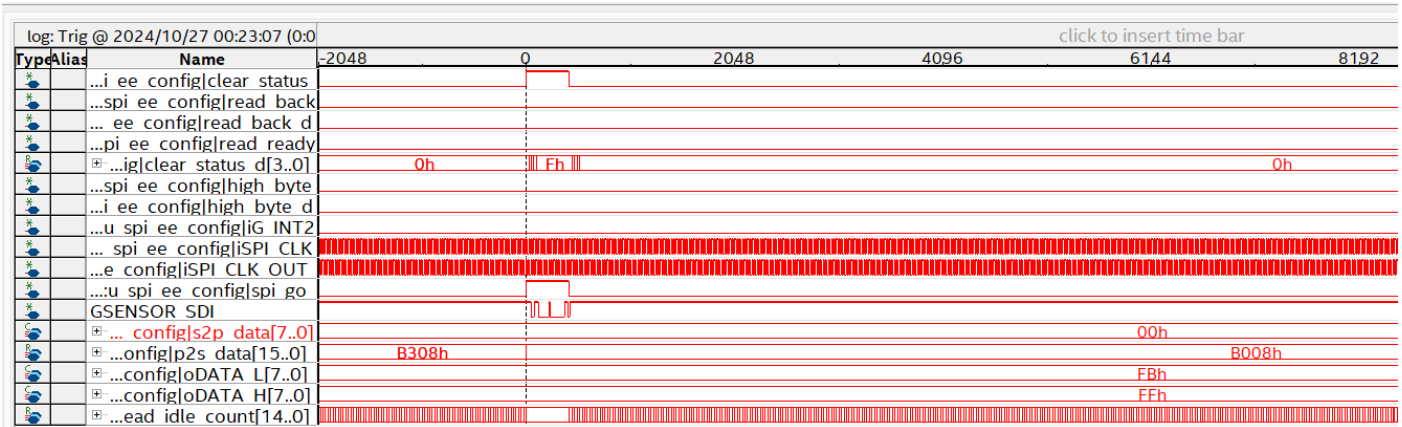
Signal Probe Pins...

Programmer

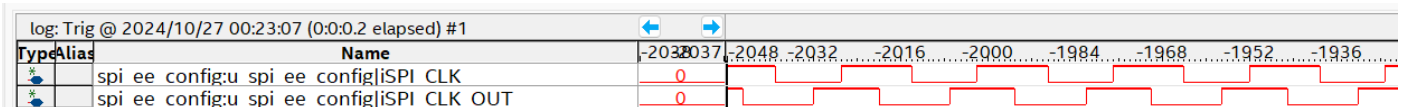


Запускаем Signal_Tap:





Смотрим что у нас с клоками



c0 - Core/External Output Clock

Ability to implement the requested PLL

☒ Use this clock

Clock Tap Settings

☒ Enter output clock frequency 2.00000000 MHz Actual Setting 2.00000000
☐ Enter output clock parameters
 Clock multiplication factor 1 Actual Setting 1
 Clock division factor 1 << Copy 25
 Clock phase shift 200.00 deg 200.00

c1 - Core/External Output Clock

Ability to implement the requested PLL

☒ Use this clock

Clock Tap Settings

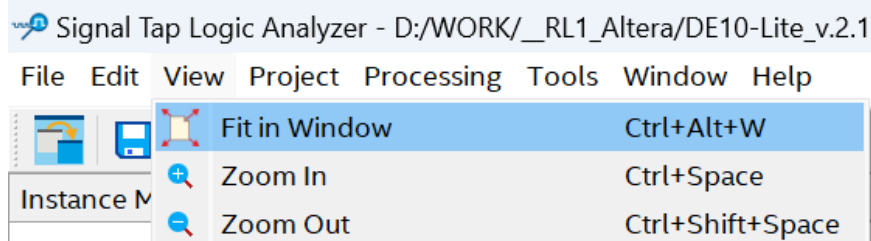
☒ Enter output clock frequency 2.00000000 MHz Actual Setting 2.00000000
☐ Enter output clock parameters
 Clock multiplication factor 1 Actual Setting 1
 Clock division factor 1 << Copy 25
 Clock phase shift 120.00 deg 120.00

```

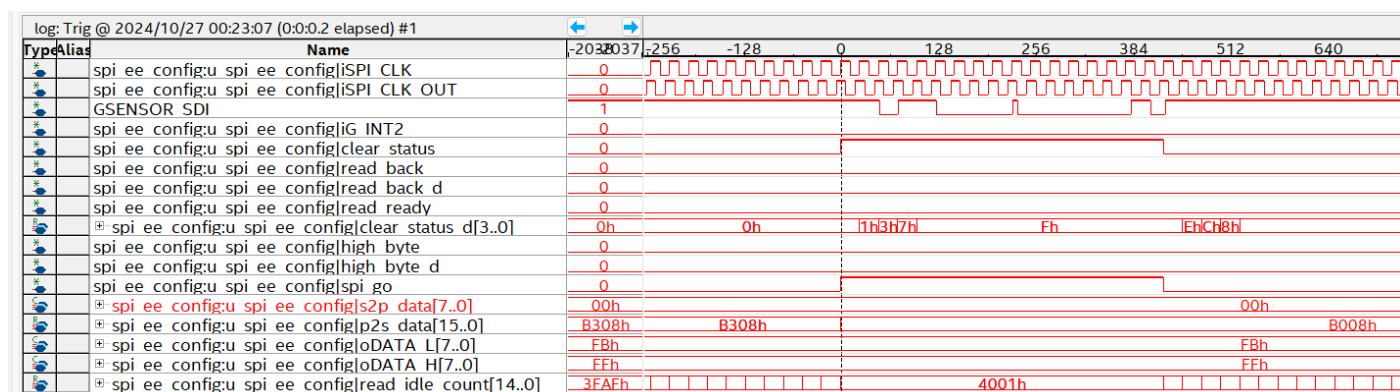
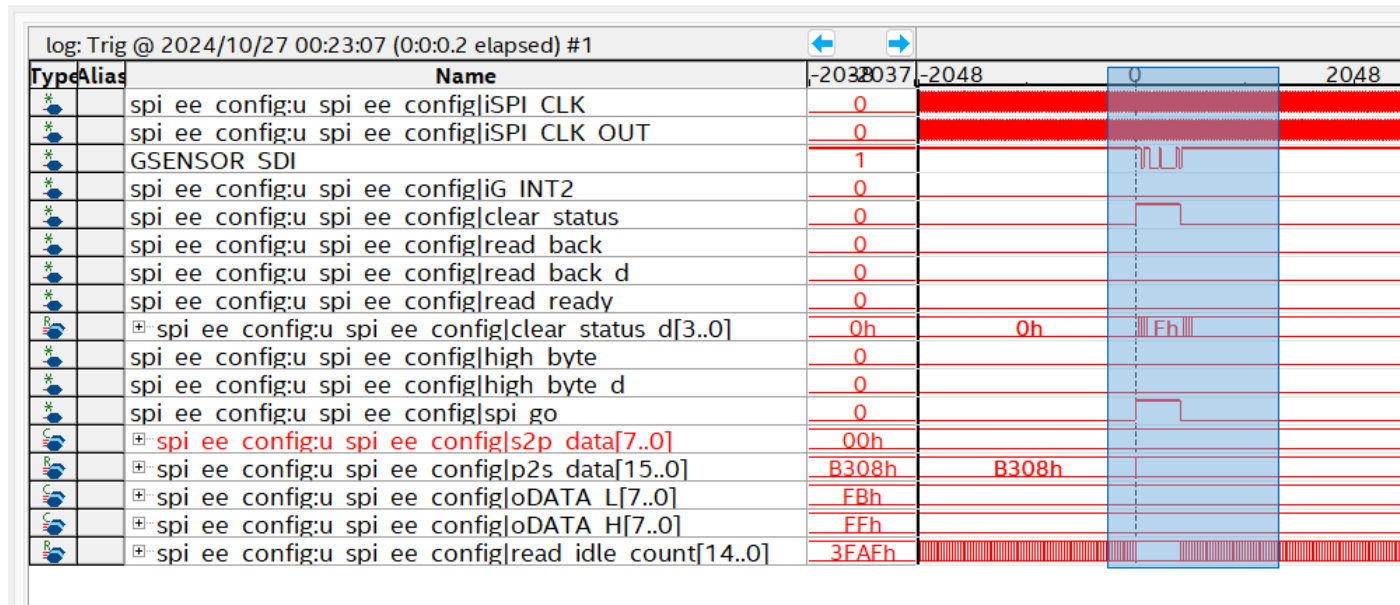
102 // PLL
103 spi_pll u_spi_pll
104 (
105     .areset (dly_rst),
106     .inc1k0 (MAX10_CLK1_50),
107     .c0      (spi_clk), // 2MHz
108     .c1      (spi_clk_out) // 2MHz phase shift
109 );

```

Управление зумом:



Мышкой можно выделить зону для увеличения:



Что мы видим?

- 1) INT2 = 0, не было прерывания от акселя
- 2) А вот в счетчике N-й бит стал равен = 1, значит это «чтение по таймауту», когда счетчик досчитал
- 3) Вот стадия считывания регистра источника прерываний
- 4) Ну и запуск SPI транзакции для этого считывания

P2S_data = 0xB008

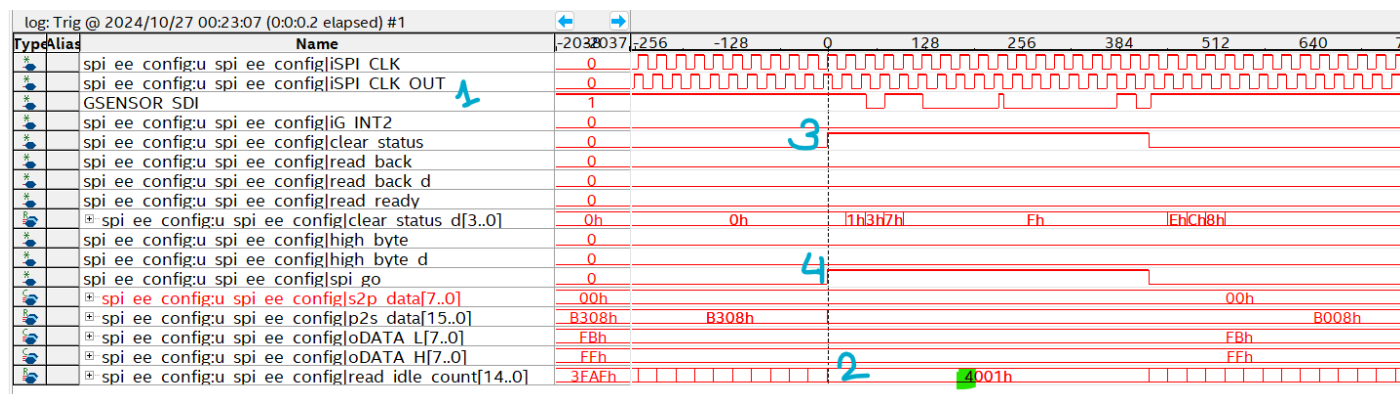


Figure 5 shows the timing diagram for SPI Mode 3. In this mode, the clock polarity is 1, which indicates that the idle state of the clock signal is high. The clock phase in this mode is 1, which indicates that the data is sampled on the rising edge (shown by the orange dotted line) and the data is shifted on the falling edge (shown by the dotted blue line) of the clock signal.

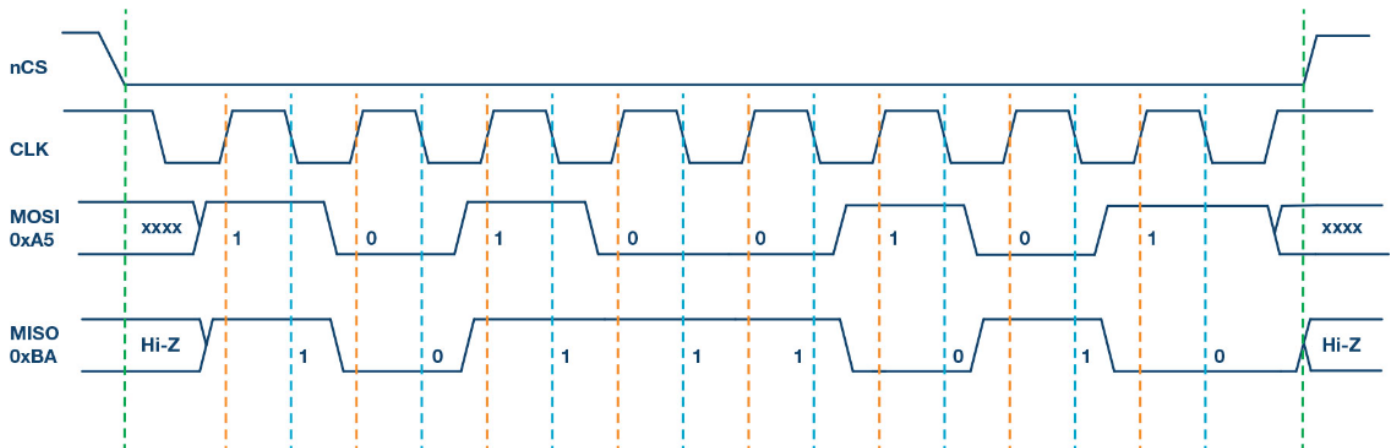
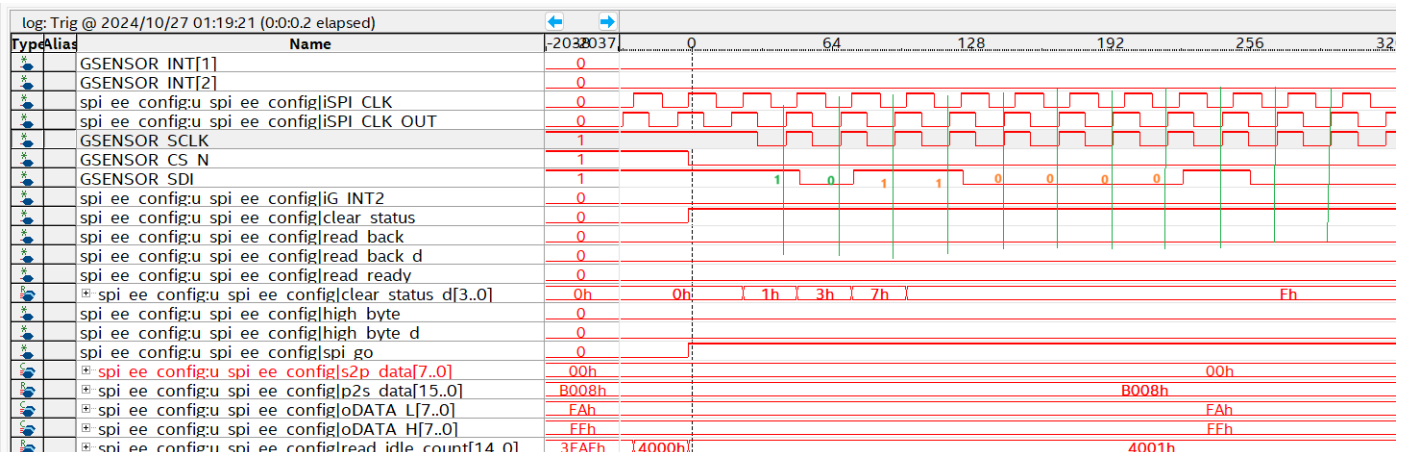


Figure 5. SPI Mode 3, CPOL = 1, CPHA = 1: CLK idle state = high, data sampled on the rising edge and shifted on the falling edge.

Т.е. аксель (слейв) засчелкивает данные по фронту своего клона, и засчелкивает 10_110000, Read Mode, MB = 0, reg_addr = 0x30 (interrupt source)



Вот чтение данных ускорения:

