

New Project Wizard

EDA Tool Settings

Specify the other EDA tools used with the Quartus Prime software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entr...	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	Verilog HDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

Project Navigator

Files

Files

frame1020_to_1024.v

Frame1020_to_1024_v1.tb.v

frame1020_to_1024_run_sim.do

Settings - Frame1020_to_1024_v1

Category: Device/Board...

General

Files

Libraries

IP Settings

IP Catalog Search Locations

Design Templates

Operating Settings and Conditions

Voltage

Temperature

Compilation Process Settings

Incremental Compilation

EDA Tool Settings

Design Entry/Synthesis

Simulation

Board-Level

Compiler Settings

VHDL Input

Verilog HDL Input

Default Parameters

Timing Analyzer

Assembler

Design Assistant

Signal Tap Logic Analyzer

Logic Analyzer Interface

Power Analyzer Settings

SSN Analyzer

Simulation

Specify options for generating output files for use with other EDA tools.

Tool name: ModelSim-Altera

☐ Run gate-level simulation automatically after compilation

EDA Netlist Writer settings

Format for output netlist: Verilog HDL

Time scale: 1 ps

Output directory: simulation/modelsim

☐ Map illegal HDL characters

☐ Enable glitch filtering

Options for Power Estimation

☐ Generate Value Change Dump (VCD) file script

Script Settings...

Design instance name:

More EDA Netlist Writer Settings...

NativeLink settings

☐ None

☒ Compile test bench: Test Benches...

☐ Use script to set up simulation:

☐ Script to compile test bench:

Test Benches

Specify settings for each test bench.

Existing test bench settings:

Name	Level Moc	Sign Instan	Run For	Test Bench File(s)
------	-----------	-------------	---------	--------------------

New...

Edit...

Delete

New Test Bench Settings

Create new test bench settings.

Test bench name:

Top level module in test bench:

☐ Use test bench to perform VHDL timing simulation

Design instance name in test bench:

Simulation period

☒ Run simulation until all vector stimuli are used

☐ End simulation at: s

Test bench and simulation files

File name: ...

File Name	Library	HDL Version
Frame1020_to_1024_v1_tb.v		Default

Test Benches

Specify settings for each test bench.

Existing test bench settings:

Name	Top Level Module	Design Instance	Run For	Test Bench File(s)
Frame1020_to_1024_v1_tb	Frame1020_to_1024_v1_tb	NA		Frame1020_to_1024_...

NativeLink settings

☐ None

☒ Compile test bench:

☒ Use script to set up simulation: ...

☐ Script to compile test bench: ...

Если теперь запустить на компиляцию, то файл тестбенча он тоже компилирует и проверяет

Run Simulation Tool

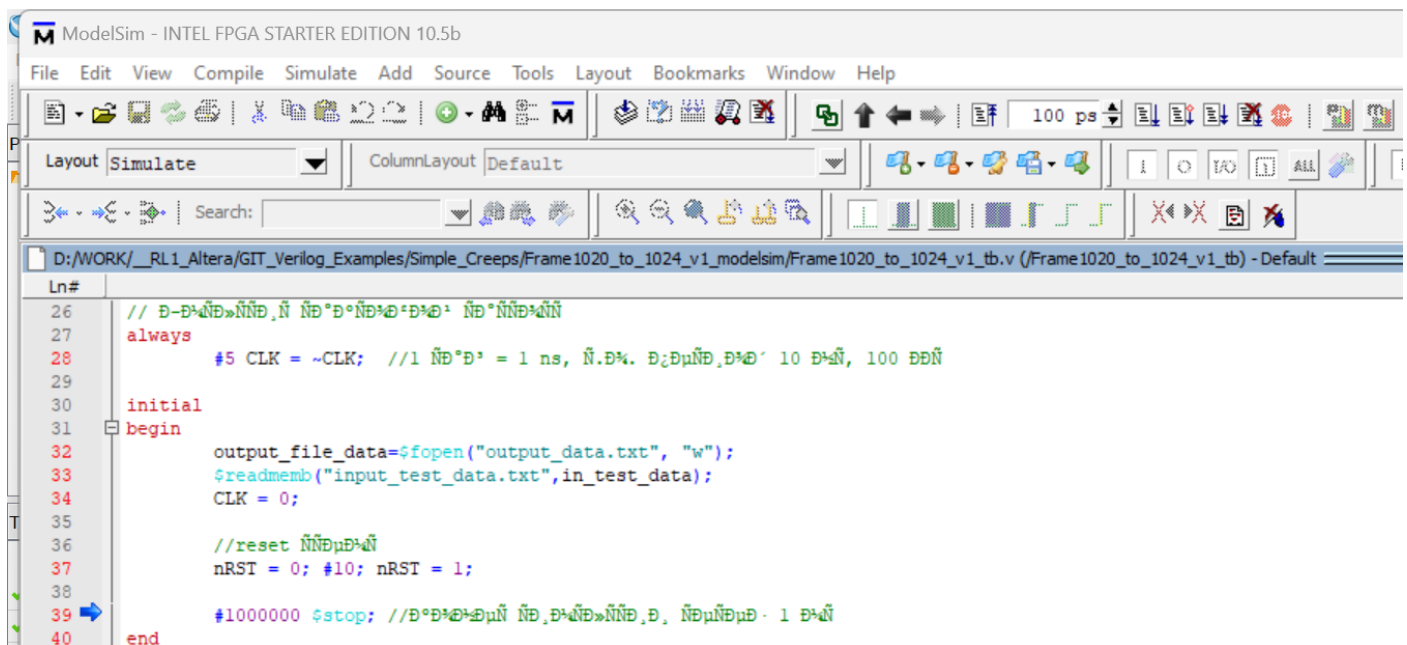
RTL Simulation

Message

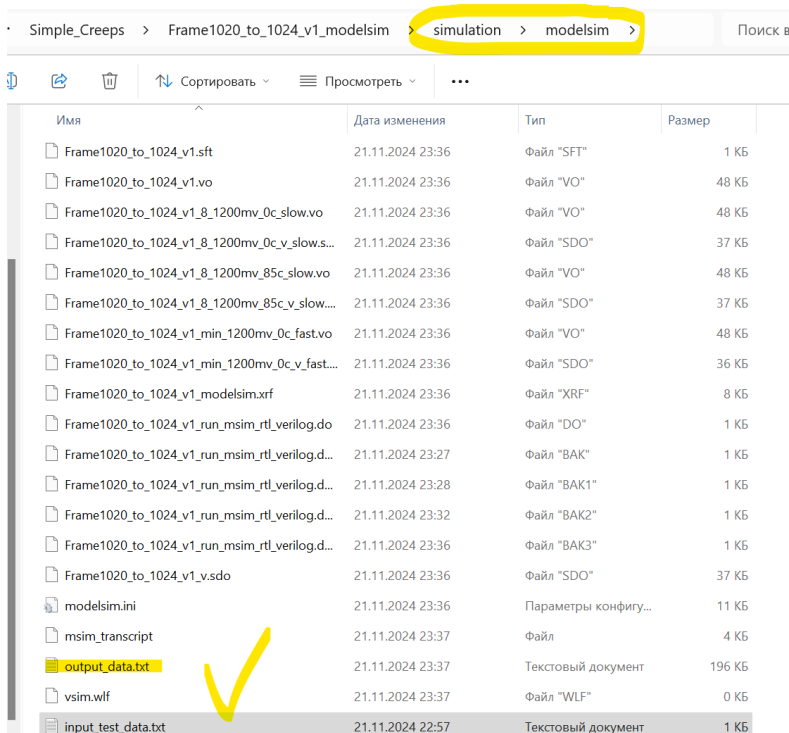
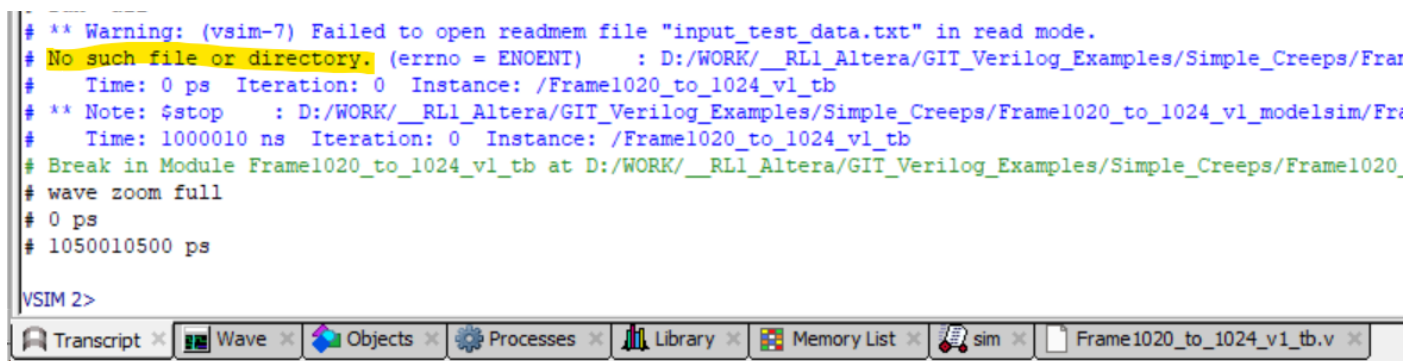
```

Running Quartus Prime Analysis & Synthesis
Command: quartus_map --read_settings_files=on --write_settings_files=off Frame1020_to_1024_v1 -c Frame10
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the glo
20030 Parallel compilation is enabled and will use 16 of the 16 processors detected
12021 Found 1 design units, including 1 entities, in source file frame1020_to_1024.v
12021 Found 1 design units, including 1 entities, in source file frame1020_to_1024_v1_tb.v
10161 Verilog HDL error at Frame1020_to_1024_v1_tb.v(28): object "clk" is not declared. Verify the object name
10161 Verilog HDL error at Frame1020_to_1024_v1_tb.v(32): object "file_data" is not declared. Verify the objec
10161 Verilog HDL error at Frame1020_to_1024_v1_tb.v(34): object "clk" is not declared. Verify the object name
10161 Verilog HDL error at Frame1020_to_1024_v1_tb.v(42): object "clk" is not declared. Verify the object name
Quartus Prime Analysis & Synthesis was unsuccessful. 4 errors, 1 warning
293001 Quartus Prime Full Compilation was unsuccessful. 6 errors, 1 warning
  
```

_Altera/GIT_Verilog_Examples/Simple_Creeps/Frame1020_to_1024_v1_modelsim/Frame1



Моделсим может не найти файл входных данных, ошибкой это не будет... Надо располагать файл или в папке simulation/modelsim, или в пути указывать на 2 уровня выше.



Важно проверять, как он считывает входные данные из файла

```
33 initial
34 begin
35     output_file_data=fopen("output_data.txt", "w");
36     //$readmemb("input_test_data.txt",in_test_data); //ищет файл в папке /simulation/modelsim
37     $readmemb("../input_test_data_2.txt",in_test_data); //ищет файл на одном уровне с исходниками
38
39     //тест чтения из файла -> читает верно
40     $display("in_data:");
41     for (i=0; i < 4; i=i+1)
42         $display("%d:%h",i,in_test_data[i]);
43
44 # run -all
45 # in_data:
46 #
47 #         0:1
48 #         1:1
49 #         2:1
50 #         3:1
```

Возникли трудности с тем, как менять индекс данных. Заработал такой вариант:

```
33 initial
34 begin
35     output_file_data=fopen("output_data.txt", "w");
36     //$readmemb("input_test_data.txt",in_test_data);
37     $readmemb("../input_test_data_2.txt",in_test_data);
38
39     //тест чтения из файла -> читает верно
40     $display("in_data:");
41     for (i=0; i < 4; i=i+1)
42         $display("%d:%h",i,in_test_data[i]);
43
44     CLK = 0;
45
46     //reset схемы
47     nRST = 0; #10; nRST = 1;
48
49     //-----
50     in_data_cntr = 0;
51     repeat(64) //скок в файле входных векторов
52     begin
53         #10;
54         in_data_cntr = in_data_cntr + 1'd1;
55     end
56     //-----
57
58     #1000 $stop; //конец симуляции через 1 мкс
59 end
60
61 always @(in_data_cntr)
62 begin
63     IN = in_test_data[in_data_cntr];
64     $display ("%d] IN=%d", in_data_cntr, IN);
65 end
```

Теперь рассмотрим такую связку: выставляем IN, проверяем OUT:

```
61 always @(in_data_cntr)
62 begin
63     IN = in_test_data[in_data_cntr];
64     $display ("%d] IN=%d", in_data_cntr, IN);
65 end
66
67 always @(posedge CLK)
68 begin
69     $fwrite(output_file_data,"%b ",OUT);
70     $display ("%d] CLK_pe: OUT=%d", in_data_cntr, OUT);
71 end
72
73 always @(negedge CLK)
74 begin
75     $display ("%d] CLK_ne: OUT=%d", in_data_cntr, OUT); //работает
76     $display ("-----");
77 end
```

```

# [      x] CLK_ne: OUT=x
# -----
# [      x] CLK_pe: OUT=x
# [      0] CLK_ne: OUT=x
# -----
# [      0] IN=1
# [      0] CLK_pe: OUT=x
# [      1] CLK_ne: OUT=0
# -----
# [      1] IN=1
# [      1] CLK_pe: OUT=0
# [      2] CLK_ne: OUT=1
# -----
# [      2] IN=1
# [      2] CLK_pe: OUT=1
# [      3] CLK_ne: OUT=0
# -----
# [      3] IN=1
# [      3] CLK_pe: OUT=0

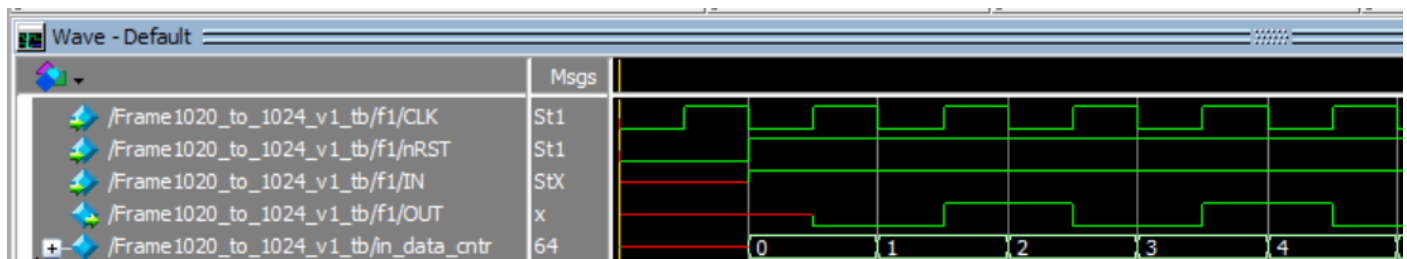
```

20_to_1024_run_sim.do x abc frame1020_to_1024.v x abc Frame

```

1 add wave /Frame1020_to_1024_v1_tb/f1/CLK
2 add wave /Frame1020_to_1024_v1_tb/f1/nRST
3 add wave /Frame1020_to_1024_v1_tb/f1/IN
4 add wave /Frame1020_to_1024_v1_tb/f1/OUT
5 add wave /Frame1020_to_1024_v1_tb/in_data_cntr
6 view structure
7 view signals
8 run -all
9 wave zoom full

```

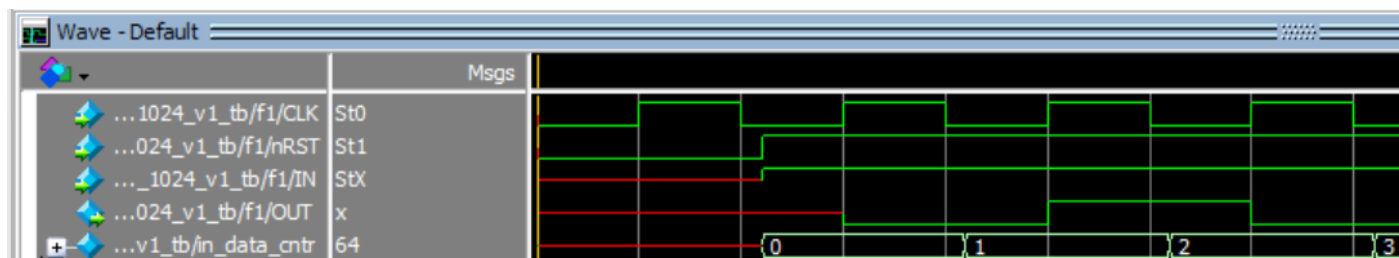


Меняем 10 на 11

```

33 initial
34 begin
35     output_file_data=$fopen("output_data.txt", "w");
36     //$readmemb("input_test_data.txt",in_test_data);
37     $readmemb("../input_test_data_2.txt",in_test_data);
38
39     //тест чтения из файла -> читает верно
40     $display("in_data:");
41     for (i=0; i < 4; i=i+1)
42         $display("%d:%h",i,in_test_data[i]);
43
44     CLK = 0;
45
46     //reset схемы
47     nRST = 0; #11; nRST = 1;
48
49     //-----
50     in_data_cntr = 0;
51     repeat(64) //скок в файле входных векторов
52     begin
53         #10;
54         in_data_cntr = in_data_cntr + 1'd1;
55     end
56     //-----

```



Теперь четко стало:

```
# -----
# [ 0] IN=1
# [ 0] CLK_pe: OUT=x
# [ 0] CLK_ne: OUT=0
# -----
# [ 1] IN=1
# [ 1] CLK_pe: OUT=0
# [ 1] CLK_ne: OUT=1
# -----
# [ 2] IN=1
# [ 2] CLK_pe: OUT=1
# [ 2] CLK_ne: OUT=0
# -----
# [ 3] IN=1
# [ 3] CLK_pe: OUT=0
# [ 3] CLK_ne: OUT=1
# -----
```