SAVYASACHI JHA

Dublin, Ireland

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Education

University College Dublin   Dublin, Ireland

BE, Electronic Engineering, 3.95/4.20 GPA   Sep 2015 – May 2019

- Bachelor of Engineering Scholarship (for achieving a top 3 GPA among 293 peers)
- College of Engineering Global Excellence Scholarship (for achieving all As in school-leaving exams)
- Thesis: Design of Ultra-Low Power DTC in 28 nm CMOS (supervisor: Prof. Robert Bogdan Staszewski)

Relevant coursework:

- Mixed-Signal Integrated Circuits[†] • Analog Integrated Circuits • RF Electronics • Wireless Systems
- Advanced Digital Signal Processing • Digital Communication • Digital Systems Laboratory
- Embedded Systems[†] • Data Structures & Algorithms • Control Theory;   [†]Semester 2

University of Illinois at Urbana-Champaign   Urbana, USA

Student Exchange, Electrical and Computer Engineering   Aug 2017 - May 2018

Technical Skills

Hardware: Cadence (Incisive, NCSim, Virtuoso, Spectre), Verilog, SystemVerilog, FPGA, Quartus, oscilloscope

Software: C++, C, MATLAB, Python, SVN, Git, Linux, Valgrind, Visual Studio, R, RStudio, HTML5, CSS3

Relevant Work Experience

S3 Semiconductors   Dublin, Ireland

IC Design Intern   Jun 2018 – Aug 2018

- Designed, verified, and documented RTL design in Verilog for pipelined fixed-point FIR filter, having configurable order and signal bit lengths, using Cadence tools in a Linux environment
- Wrote MATLAB script to generate filter coefficients based on required specifications, convert real number coefficients into customizable Q-format signed binary numbers for dumping into filter, read output of filter to evaluate and display FFT of filtered signal, and estimate gate count of designed microarchitecture
- Designed biasing circuit in 180 nm node, from transistor-level schematic capture to layout, physical verification (LVS/DRC), parasitic extraction and post-layout PVT simulations, using Cadence tools.

Projects

UIUC Digital Systems Laboratory   Urbana, USA

sLC3.2 microprocessor ISA RTL design, verification, and implementation on FPGA   Feb 2018 – Mar 2018

- Implemented, verified, and documented RTL design in SystemVerilog, for the simplified Little Computer 3.2 instruction set architecture on the Altera Cyclone IV FPGA (DE2 board), using ModelSim and Quartus
- Used TimeQuest and PowerPlay tools to analyze power consumption and maximum operating frequency

UIUC Data Structures and Algorithms   Urbana, USA

Object-oriented program for linked-memory manipulation   Dec 2017 – Dec 2017

- Wrote functions in C++ to manipulate templated linked-memory objects, using Valgrind for testing memory leakage and SVN for version control in a Linux environment

Intel IRIS National Science Fair   Bengaluru, India

Extinguishing fires using sound waves   Oct 2013 – Dec 2013

- Presented research poster on self-directed research, in a team of 2, to top Indian scientists (IITs, ISRO); received Bronze medal (top 30/2000+) and letter of commendation from the Prime Minister of India

Leadership and Volunteering

UCD Student Recruitment   Dublin, Ireland
Student Ambassador   Sep 2016 – Present
- Delivered several campus tours to prospective students, visiting international students, and alumni
- Answered questions from prospective students and connected them to relevant resources

UCD Literary & Historical Society / College Debating Union   Dublin, Ireland
Public Speaking Training Officer   Apr 2016 – May 2017
- Started and ran public speaking training program for UCD's largest student society
- Researched public speaking, created training curriculum, conducted workshops, invited and hosted experts, and increased turnout by 50% in 4 weeks using social media marketing

National Association for the Blind   New Delhi, India
Teaching Assistant   Apr 2013 – Dec 2014
- Built pen which makes tactile drawings to assist hands-on learning for visually impaired students
- Taught visually-impaired students and proactively identified problems in pedagogy

Other Work Experience

Eversheds Sutherland   Dublin, Ireland
Dispute Resolution and Litigation Intern   May 2017 – Aug 2017
- Drafted research memos for client queries on injunctive relief, guarantee discharge, and multi-jurisdictional agency disputes, by researching relevant case law using legal databases
- Memos used to instruct arguing counsel and advise solicitors in the firm's UK and Ireland offices
- Drafted paper on 3rd party funding of international arbitration, in a team of 4 solicitors, and wrote articles analyzing the enforceability of mediation settlement agreements under the Mediation Act 2017, and the emerging alternative dispute avoidance and resolution options in the Irish construction industry
- Researched prospective clients by liaising with chambers of commerce in the US and in Ireland

RailTel Corporation   Gurgaon, India
Network Operations Centre Summer Intern   Jul 2016 – Aug 2016
- Reported on telecom technologies like Pulse Code Modulation, TDM/WDM, and optical fiber cables
- Shadowed engineers in SDH equipment R&D lab and optical-fiber Network Operations Centre

Tata Motors   Pune, India
Hybrid Electric Vehicle Engineering Summer Intern   Jun 2016 – Jun 2016
- Monitored charge-discharge testing and studied State of Health measurement of lead-acid batteries for application in mild-hybrid electric vehicles
- Prepared study report on hybrid electric vehicle technology

Interests and Languages

Debating and Negotiation
- National top 10 speaker at the National Maidens Debate at UCD, 2016
- Quarter-finalist at UCD Student Legal Service Negotiation Competition, 2015

Music
- Baritone at Illini Awaaz a capella: national top 6 group at Jeena a capella competition at UT Austin, 2017
- Plectrum guitarist: distinction in Grade 2 plectrum guitar examination conducted by Trinity College London

Languages:
- English (bilingual fluency)
- Hindi (bilingual fluency)