SAVYASACHI JHA

Dublin, Ireland
+353 89 256 5244
savyasachi.jha@ucdconnect.ie
linkedin.com/in/savyajha | github.com/savya-jha

Education

University College Dublin — **Dublin, Ireland**
Bachelor of Engineering, Electronic Engineering, 3.95/4.20 GPA — Sep 2015 – May 2019

- Bachelor of Engineering Scholarship (for achieving a top 3 GPA among 293 peers)
- College of Engineering Global Excellence Scholarship (for achieving all As in school-leaving exams)

University of Illinois at Urbana-Champaign — **Champaign, USA**
Student Exchange, Electrical and Computer Engineering — Aug 2017 - May 2018

Relevant coursework:
Mixed-Signal Integrated Circuits[†], Analog Integrated Circuits[†], Semiconductor Electronics, Digital & Embedded Systems[†], Digital Signal Processing, Digital Communication[†], Wireless Systems[†], Electromagnetics, RF Electronics, Data Structures & Algorithms, Control Theory, ([†]finishing May 19)

Relevant Work Experience

S3 ASIC Semiconductors — **Dublin, Ireland**
IC Design Intern — Jun 2018 – Aug 2018

- Developed and verified RTL design in Verilog for pipelined fixed-point FIR filter with configurable number of taps and data bit lengths, using Cadence tools in a Linux environment
- Wrote MATLAB script to generate tap coefficients based on filtering requirements, as customizable Q-format signed binary numbers for dumping into filter, and display FFT of filtered signal
- Simulated mixed-signal blocks and completed full analog IC design flow, from schematic capture to layout, physical verification, parasitic extraction, and post-layout simulation using Cadence tools

Projects

UIUC Digital Systems Laboratory — **Champaign, USA**
sLC3.2 microprocessor RTL design, verification, and implementation on FPGA — Feb 2018 – Mar 2018

- Implemented and verified RTL design in SystemVerilog, in a team of 2, for simplified Little Computer 3.2 instruction set architecture on the Cyclone IV FPGA (DE2 board), using ModelSim and Altera Quartus II

UIUC Data Structures and Algorithms — **Champaign, USA**
Object-oriented program for linked-memory manipulation — Dec 2017 – Dec 2017

- Wrote functions in C++ to manipulate templated linked-memory objects, using Valgrind for testing memory leakage and SVN for version control in a Linux environment

UCD Communication Systems — **Dublin, Ireland**
Link- and application layer communication protocol — Jan 2016 – May 2016

- Designed and implemented server-side application layer protocol in C for file transfer over TCP/IP
- Implemented link layer protocol with error checking and data encoding in C for file transfer over cable

Intel IRIS National Science Fair — **Bengaluru, India**
Extinguishing fires using sound waves — Oct 2013 – Dec 2013

- Presented research poster on self-directed research, in a team of 2, to top Indian scientists (IITs, ISRO); received Bronze medal (top 30/2000+) and letter of commendation from the Prime Minister of India

Technical Skills

Hardware: Cadence Incisive, Cadence Virtuoso, Verilog, SystemVerilog, FPGA, Quartus, oscilloscope
Software: C++, C, Python, MATLAB, SVN, Git, Linux, Valgrind, Visual Studio, R, RStudio, HTML5, CSS3

Leadership and Volunteering

UCD College Debating Union (L&H) — **Dublin, Ireland**
Public Speaking Training Officer — Apr 2016 – May 2017

- Started and ran public speaking training program for UCD's largest student society (6000+)
- Led workshops, hosted experts, and increased turnout by 50% in 4 weeks using social media marketing

UCD Student Recruitment — **Dublin, Ireland**
Student Ambassador — Sep 2016 – Apr 2017

- Led campus tours for prospective students and worked in team of 20+ ambassadors to run various events

National Association for the Blind — **New Delhi, India**
Teaching Assistant — Apr 2013 – Dec 2014

- Built pen which makes tactile drawings to assist hands-on learning for visually impaired students

Other Work Experience

Eversheds Sutherland — **Dublin, Ireland**
Litigation and Dispute Resolution Intern — May 2017 – Aug 2017

- Drafted research memos for client queries on injunctive relief, guarantee discharge, and multi-jurisdictional agency disputes, by analyzing case law using legal databases
- Memos were used to instruct arguing counsel or advise solicitors in the firm's UK and Ireland offices
- Drafted paper on 3rd party funding of international arbitration, in a team of 4 solicitors, and wrote articles analyzing the enforceability of mediation settlement agreements under the Mediation Act 2017, and the emerging alternative dispute avoidance and resolution options in the Irish construction industry

RailTel Corporation — **Gurgaon, India**
Network Operations Centre Summer Intern — Jul 2016 – Aug 2016

- Reported on telecom technologies like Pulse Code Modulation, TDM/WDM, and optical fiber cables
- Shadowed engineers in SDH equipment R&D lab and optical-fiber Network Operations Centre

Tata Motors — **Pune, India**
Hybrid Electric Vehicle Engineering Summer Intern — Jun 2016 – Jun 2016

- Monitored charge-discharge testing and studied State of Health measurement of lead-acid batteries for application in mild-hybrid electric vehicles

Interests and Languages

Debating and Negotiation

- National top 10 speaker at the National Maidens Debate at UCD, 2016
- Quarter-finalist at UCD SLS Negotiation Competition, 2015

Music

- Baritone at Illini Awaaz a capella: national top 6 group at Jeena a capella competition at UT Austin, 2017
- Plectrum guitarist: distinction in Grade 2 plectrum guitar examination conducted by Trinity College London

Languages:

- English (bilingual fluency)
- Hindi (bilingual fluency)