SAWANT VAISHNAVI DILIP

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EDUCATION

M. Tech (Electronic Design and Technology)
National Institute of Technology, Calicut • Kerala, India • 2025 • **CGPA:** 8.84/10.00

B. Tech (Electronics & Telecommunication)
Government College of Engineering, Karad • Karad, Maharashtra • 2021 • **CGPA:** 8.60/10.00

PROFESSIONAL EXPERIENCE

Co/op Intern in AMD — January 2025 - July 2025, Bangalore
- Contributed to NBIO–IOHUBSS client design by integrating multiple IPs to meet project milestones.
- Executed design quality checks including connectivity, lint, CDC, and synthesis.
- Automated workflows by developing scripts (Python, Bash, TCL)
  - To extract tool configurations and shared components from sources files, eliminating manual updates and improving efficiency.
  - For credit alignment and synchronization across multiple IP blocks, enabling seamless flow control and preventing buffer overflows in credit-based protocols.
- Refined RTL code and implemented logic optimizations addressing timing closure and resource utilization in complex multi-IP environments.

TECHNICAL PROFECIENCY / SKILLS

- **Technical Skills:** Verilog, System Verilog, Perl, Python, Bash, TCL, VHDL, STA.
- **Tools:** Xilinx Vivado, Cadence Genus, NanoEdge AI Studio, STM32 Cube IDE, Verdi.

PUBLICATION

Hardware-Efficient Matrix Multiplication using Tiled Singular Value Decomposition
- Presented paper at VLSI Design and Test (VDAT) 2025 Conference: *"Hardware-Efficient Matrix Multiplication using Tiled Singular Value Decomposition"* – introduced two novel architectures based on the Hestenes-Jacobi algorithm, achieving up to 90% area and power reduction in Cadence Genus (GPDK 90nm @100 MHz) (Accepted for publication)

PROJECTS

Hardware-Efficient Matrix Multiplication using Tiled Singular Value Decomposition — (May 2024 - Dec 2024)
- Designed and implemented two novel hardware architectures using Tiled Singular Value Decomposition (TSVD) to accelerate matrix multiplication for deep neural network (DNN) workloads.
- Integrated the Hestenes-Jacobi algorithm to compute SVD coefficients and maximize data reuse, reducing off-chip memory access.
- Achieved major hardware optimizations:
  - *Hestenes-Tile Fusion Architecture: ~75% area, 77% power, and 69% gate count reduction.*
  - *Hybrid SVD-Tiled Architecture: ~90% reduction in area, power, and gates, with improved latency and throughput.*
- Validated and synthesized designs in Cadence Genus (GPDK 90nm, 100 MHz), ensuring functionality and performance efficiency.
- Developed a hardware-efficient matrix multiplication framework leveraging TSVD, improving computational throughput while minimizing resource utilization for DNN acceleration.

Implementation of Asynchronous FIFO in Verilog — (May 2024 - Dec 2024)
- Designed Asynchronous FIFO memory in Verilog to facilitate data transfer between different clock domains using Gray Pointers.
- Validated functionality and implementation through synthesis and simulation.

Wallace Tree Multiplier — (Jan 2024 - May 2024)
- Designed Wallace Tree Multiplier using basic gates for multiplication of two integers each of 4 bits in Cadence Virtuoso Software and verified its performance.

Classification Of Handwritten Digits — (Aug 2023 - Dec 2023)
- Developed and tested a model to recognize handwritten digits using Singular Value Decomposition Algorithm.

Elevator Predictive Maintenance using STM32 Microcontroller — (Aug 2023 - Dec 2023)
- Developed a prototype which predicts the health status of an elevator by analysing the vibrations of elevator.
- Successfully created and tested predictive model using 6-axis motion sensor (MPU6050) interfaced with STM32 Microcontroller.

CERTIFICATIONS

NPTEL Certifications in - Control system, Signal and system, Digital Electronics.

EXTRA CURRICULAR ACTIVITIES

Coordinator

- Coordinator of Robo-War event in Avishkar held at Government College of Engineering, Karad (State Level Event) (2017-18).

AWARDS & HONORS

Nurturing Brilliance Cummins Scholarship by Cummins India Ltd.

- Awarded the prestigious Nurturing Brilliance Cummins Scholarship (2018-2021) by Cummins India, recognizing meritorious students across engineering disciplines.

LANGUAGES

Engilsh, Hindi, Marathi.