SAWANT VAISHNAVI DILIP | M230932EC

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ACADEMIC DETAILS

Qualification	University/Board	Institute	Year of Completion	CGPA/%
M. Tech (Electronic Design and Technology)	NIT Calicut	National Institute of Technology, Calicut	2025	8.84/10.00
B. Tech (Electronics & Telecommunication)	Shivaji University	Government College of Engineering, Karad	2021	8.60/10.00
XII (HSC)	Maharashtra State Board	Shri Balaji Madhyamik Vidyalaya & Jr College, Ichalkaranji	2017	79.38%
X (SSC)	Maharashtra State Board	Kanya Shala, Shirala	2015	89.80%

TECHNICAL PROFICIENCY

- Verilog, System Verilog, Verdi, Perl, Python.

INTERNSHIPS

- **Co/op Intern At AMD | Jan-July 2025**
  Contributed to NBIO – IOHUBSS client design for milestone by integrating various IP's . Also Performed necessary Design quality checks such as connectivity, lint, CDC and synthesis check.
  Developed a Python automation script to retrieve tool configurations and shared components from multiple sources files, eliminating manual value updates and improving workflow efficiency.
  Developed robust automation scripts in Python, Bash, and TCL to manage credit alignment and synchronization across multiple IP blocks with diverse communication channels, ensuring seamless flow control and preventing buffer overflow in credit-based protocols.

PROJECTS

- **Hardware-Efficient Matrix Multiplication using Tiled Singular Value Decomposition | 2023-2025**
  Designed and implemented two novel hardware architectures using Tiled Singular Value Decomposition (TSVD) to accelerate matrix multiplication for DNN workloads.
  Integrated the Hestenes-Jacobi algorithm to compute SVD coefficients and enhance data reuse, minimizing off-chip memory access.
  Achieved significant optimizations:
  Hestenes-Tile Fusion Architecture: ~75% area, 77% power, and 69% gate count reduction.
  Hybrid SVD-Tiled Architecture: ~90% reduction in area, power, and gates; improved latency and throughput.
  Validated functionality and synthesized the design using Cadence Genus with GPDK 90nm technology, operating at 100 MHz.
  Platform used: Xilinx Vivado, Cadence Genus, Jupyter Notebook.
- **Implementation of Asynchronous FIFO in Verilog | 2024**
  Designed Asynchronous FIFO memory in Verilog to facilitate data transfer between different clock domains using Gray Pointers.
  Platform used: Xilinx Vivado
- **Elevator Predictive Maintenance using STM32 Microcontroller | 2023-2024**
  The project aims to create a prototype which predicts the health status of an elevator by analysing the vibrations of elevator. Successfully created and tested predictive model using 6-axis motion sensor (MPU6050) interfaced with STM32 Microcontroller.
  Platform used: NanoEdge AI Studio, STM32 Cube IDE
- **Wallace Tree Multiplier | 2023-2024**
  Designed Wallace Tree Multiplier using basic gates for multiplication of two integers each of 4 bits in Cadence Virtuoso Software and verified its performance.
  Platform used: Cadence Virtuoso.

- **Classification Of Handwritten Digits | 2023-2024**
  Developed and tested a model to recognize handwritten digits using Singular Value Decomposition Algorithm.
  Platform used: Jupyter Notebook

WORKSHOPS

- **Embedded AI Workshop**
  Attended 4 days workshop on ST microcontroller NanoL476RG and its integration with Cube IDE for machine learning analysis.

CERTIFICATIONS

- NPTEL Certification in Signal and system 2019
- NPTEL Certification in Control system 2019
- NPTEL Certification in Digital Electronics 2018

ACHIEVEMENTS

- Awarded a Nurturing Brilliance Cummins Scholarship (2018-2021)
- Presented paper "Automated Process for Credit Updates and Performance Measurements" at AMD Asia Technical Conference 2025 (Internal)
- Paper Presented for technical presentation at VLSI Design and Test (VDAT) 2025 Conference:
  "Hardware-Efficient Matrix Multiplication using Tiled Singular Value Decomposition" - introduced two novel architectures leveraging the Hestenes-Jacobi algorithm, achieving up to 90% area and power reduction in Cadence Genus (GPDK 90nm @ 100 MHz).

EXTRA-CURRICULAR ACTIVITIES

- Worked as Coordinator of Robo-War event in Avishkar (State Level Event) (2017-18)
- Art of Living Volunteer.