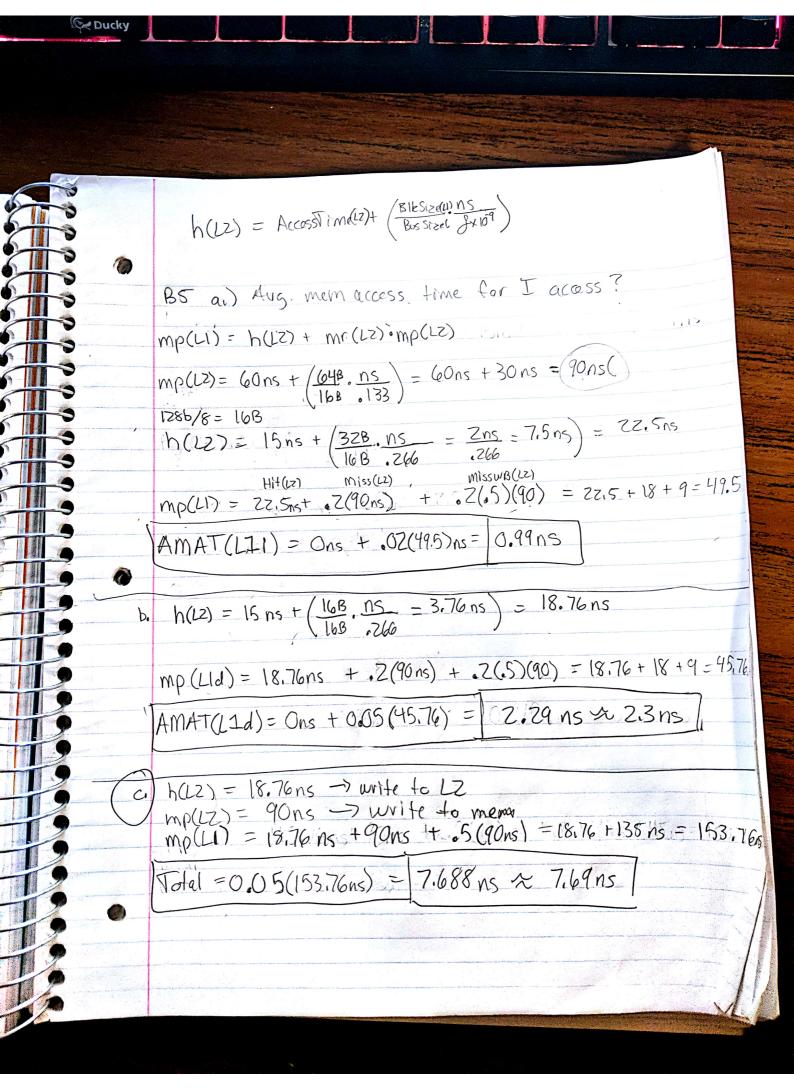
HWZ AMAT = HT + MR.MP CAChe Disayled BI HT= 1c, MA= 110c, DAM = 105c ad MR = 3% = 0.03 HR = 1 -, 63 = 0.97 AMAT = .97(1) + .03(110) = .97 + 3.3 = 4.27 cycles b.) IGB = 109B = 106KB = 103MB, KB=103B 64KB = 6.4x105 = .000064, 1-6.4e5 = .999936 106 KB AMAT= .000064(1) + .999936(110) = 109,993024 = 109,99 cycles c.) Without using locality, the using the cache is actually a little bit slower. So unless you are properly utilizing locality, its better in this case not to use cache di) HTVS RAM: A= 164c=G ARAMYS MP: BC = L 105c = (1-MR)·1c + 110co (M)R) 1050 = 1c - 1cmR + 110c(MR) 104c = 1cmr + 110cmr 104c = MR (111c) MR = 104c = 0.9369 & 0.94 \$ 94% LIIC

ac	Associ	ative	cach	64 B	blks	612B	2000 B
SlZ ales	(64 = 8 Mem Mo-1	\		ICH 7	048/6	4=37	
7		M31					
3	11	7(
u	U	(1					
5	11	U					
6	Ų	VI.	•				
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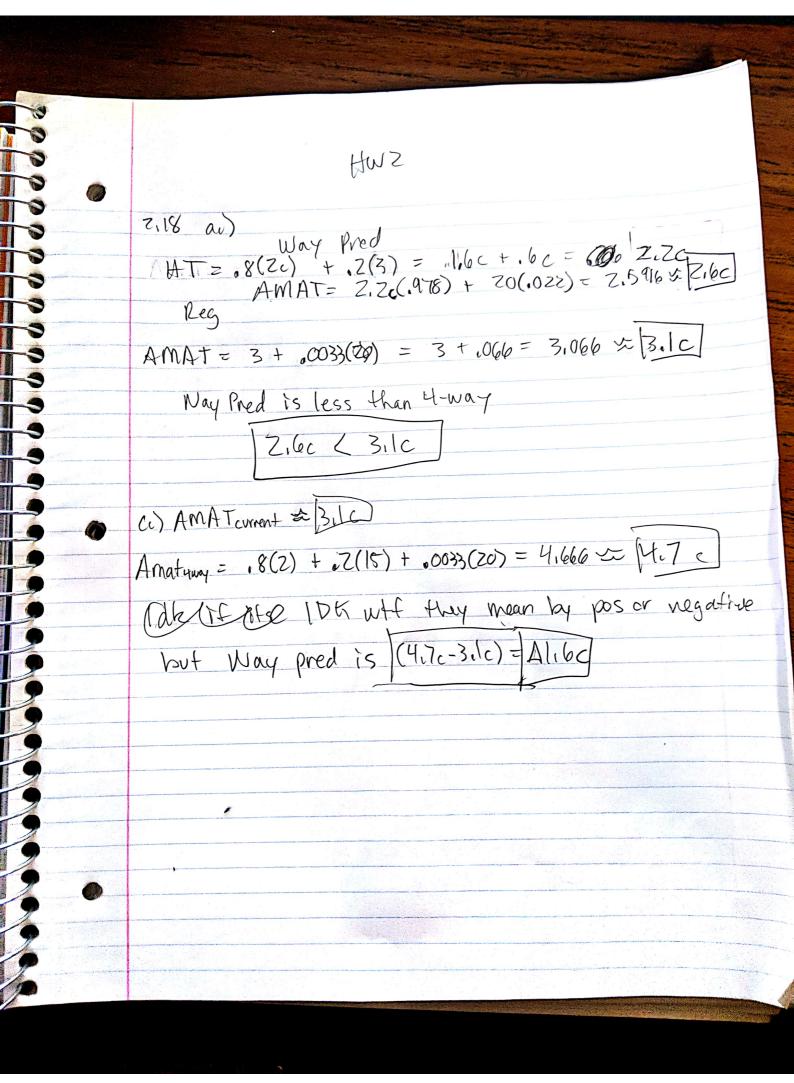
b1)						
Blks	Set	Mem				
0-3	0	Even: Mo, Mz,, m30				
4-7	l	odd: MI, m3,, m31				
	1	•				

J= 1.16Hz, CPT=1.35, Load=20%, Store=10% hit = no penalty LI, i/d cache = Direct Mapped 32KB I cache = 2% miss rate & 32-byte block size deache = 6% miss rate € 16- byte block size L) 95% of all writes have no stalls Z = B12 KB, unifred, 64-byte blocksize, 15 ns access fine -> Ll connection 128-bit bus @ 266 MHz, 128-bit word/cycle -> 80% satisfied without man mem (hit rate?) > 50% are dirty Main Mem = 128-bit wide, 60ns, 1331AHz, one per cycle mp/(L1) = h(LZ) + mr(LZ) · mp(LZ) = 15 ns + . Z(90) = 33ns mp(LZ) = 60ns + (Hc. ns. = 30.075 Zns)64B(8) = 512bits/128/0= 4cycles one cycle = 133(106) cycles 10 sec = 133(103)c = .133 cycles APMAT: = h(L1) + mr(4) + 0 + 62 (33ms



BS. d.) CPI =
$$1.36 + 0.7(2.3)(1.1) + 0.1(7.69)(1.1) + 0$$

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	HWZ	+
2.20 as)	with Gut =	(NSOC)
with =	V20 + 3(16)	= (1680)

bi) Depends on other factors, if miss rate were lower a hit time is the same or faster than yes, it would be.

Zizl ai) le bytes

bi) Non = 16b/4e= 4b/c

Merge = 86/1c = 8 b/c

Speedup = 8/4 = [2 xspeedup]

(i) Misses hold the cache up with blocking but don't with non-blocking.