Q11

Due Nov 11, 2018 at 11:59pm **Points** 100 **Questions** 5
Available until Nov 11, 2018 at 11:59pm **Time Limit** 20 Minutes

This quiz is no longer available as the course has been concluded.

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	16 minutes	100 out of 100

Score for this quiz: **100** out of 100
Submitted Nov 11, 2018 at 9:43pm
This attempt took 16 minutes.

Question 1 — 20 / 20 pts

Compare centralized and distributed shared memory multiprocessors by indicating their differences.

Your Answer:

1. Centralized shared memory uses the same memory for all processors with the same memory access time.

2. Distributed shared memory, each processor has its own memory and because of this, memory access time is not the same. This means faster local memory time but much slower remote memory access time.

In a centralized shared memory MP system, a centralized memory is shared by all processors. All processors has uniform memory access latency.

In a distributed shared memory MP system, each processor has its own memory attached to it. In this case, memory access latencies are non-uniform. It is faster to access local memory, while it takes long er to take the remote memory.

Question 2

20 / 20 pts

Explain the meaning of "shared memory".

Your Answer:

Shared memory is when the address space is shared by all processors/cores.

Shared memory means that a single memory address space is shared by all processors, not the physical locations of the memory.

Question 3

20 / 20 pts

Explain the cache coherence problem, and why it happens.

Your Answer:

Cache coherence problem is when multiple processors are trying to read the same thing in memory and they dont read the correct data from

memory because they read from memory into their private cache too soon, so the value is incorrect at that time.

Cache coherence problem refers to the situation where processors see different values of a memory location that are accessed by multiple processors.

This problem can happen because processors can store local copies of the values of a shared memory location in their private caches, and a processor may access that memory location before it sees the updated value produced by a different processor.

Question 4

20 / 20 pts

List key factor(s) that limit snooping protocols scalable to large number of processors.

Your Answer:

Because the bus cant handle all the requests that are needed with that many processors.

Either one would be fine

- Bus can only handle one request at a time
- Snooping requests are broadcast to all private caches

Question 5

20 / 20 pts

In a snooping protocol using write-invalidate, what happens when a processor writes to a block in its private cache? Assume write hit.

Your Answer:

1. It will first send out an invalid command to all the other processors private cache, invalidating the other copies.

2. It will then update the block and change it to exclusive, that way the correct values are written back to memory and not the old invalid ones from a different processor.

1. The processor will send a invalidate message to all other private cache to make cached copies of the target block be invalid

2. The cache block is then updated, and its state is changed to "Modified" or "Exclusive".

Quiz Score: **100** out of 100