EEL 6764 Principles of Computer Architecture
Homework #6

1 Problems

Total points: 210

1 Complete 5.1 (10 pts each) at the end of Chapter 5

2 For each part of this exercise, assume the initial cache and memory state in Figure 5.38. Each part of this exercise specifies a sequence of one or more CPU operations of the form:

```
P#:  <op> <address> [ <-- <value> ]
```

where `P#` designates the CPU (e.g., P0,0), `<op>` is the CPU operation (e.g., read or write), ¡address¿ denotes the memory address, and `<value>` indicates the new word to be assigned on a write operation. What is the final state (i.e., coherence state, sharers/owners, tags, and data) of the caches and memory after the given sequence of CPU operations has completed? Also, what value is returned by each read operation? (10 pts each)

(a) `P0,0:  read 100`

(b) `P0,0:  read 128`

(c) `P0,0:  write 128 <-- 78`

(d) `P0,0:  read 120`

(e) `P0,0:  read 120;  P1,0:  read 120`

(f) `P0,0:  read 120;  P1,0:  write 120 <-- 80`

(g) `P0,0:  write 120 <-- 80;  P1,0:  read 120`

(h) `P0,0:  write 120 <-- 80;  P1,0:  write 120 <-- 90`

Note: In Figure 5.38, the processor `P0,1` *should be* `P1,0`.

3 Directory protocols are more scalable than snooping proto- cols because they send explicit request and invalidate messages to those nodes that have copies of a block, while snooping protocols broadcast all requests and invalidates to all nodes. Consider the eight-processor system illustrated in Figure 5.37 and assume that all caches not shown have invalid blocks. For each of the sequences below, identify which nodes (chip/processor) receive each request and invalidate. (10 pts each)

(a) `P0,0:  write 100 <-- 80`

(b) `P0,0:  write 108 <-- 88`

(c) `P0,0:  write 118 <-- 90`

(d) `P1,0:  write 128 <-- 98`

4 Show how the basic snooping protocol of Figure 5.7 can be changed for a write-through cache. What is the major hardware functionality that is not needed with a write-through cache compared with a write-back cache? (20 pts)

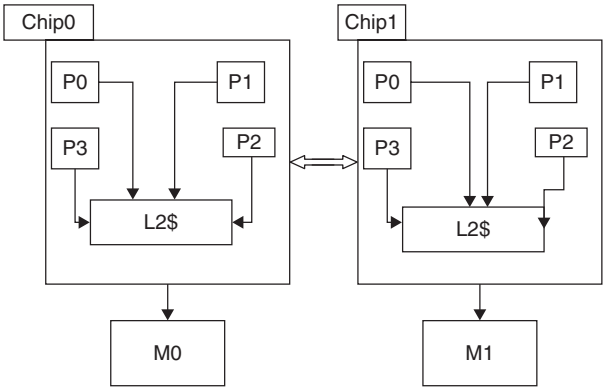

Figure 5.37 Multichip, multicore multiprocessor with DSM.

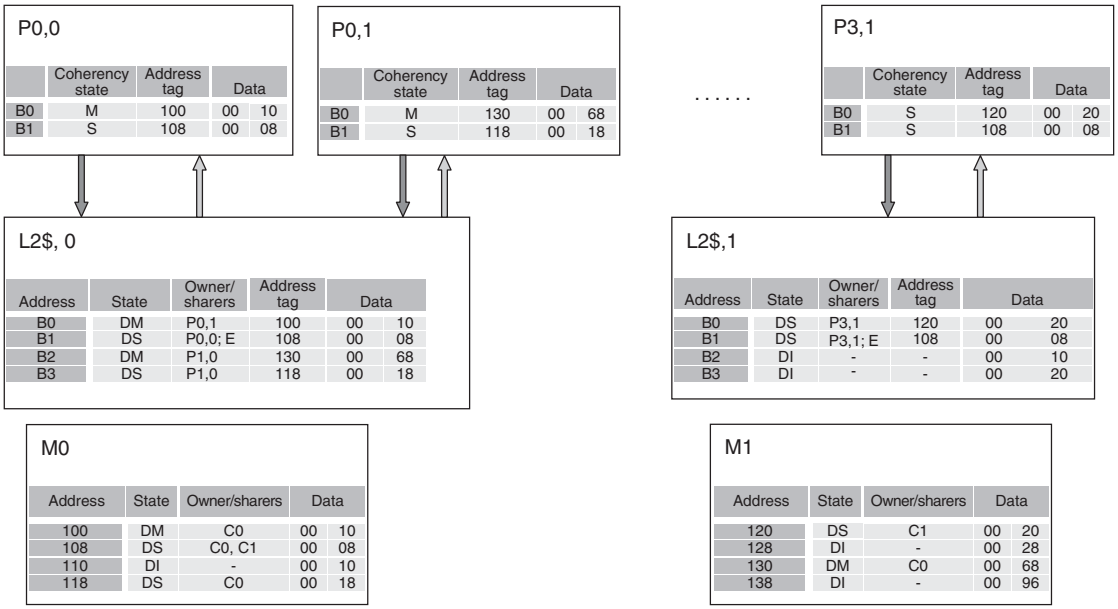

Figure 5.38 Cache and memory states in the multichip, multicore multiprocessor.

2 Requirement

- All homeworks should be done and submitted individually.
- Show all necessary steps to get full points.
- Writing and drawings if necessary must clear and readable. Otherwise, substantial loss of points may occur.
- You must submit your solutions electronically via Canvas.
- The file for your solutions must be in PDF or MS-Word DOCX format.