Q12

Due Nov 26, 2018 at 11:59pm **Points** 90 **Questions** 6
Available until Nov 26, 2018 at 11:59pm **Time Limit** 20 Minutes

This quiz is no longer available as the course has been concluded.

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	15 minutes	89 out of 90

Score for this quiz: **89** out of 90
Submitted Nov 26, 2018 at 11:16pm
This attempt took 15 minutes.

Question 1 — 20 / 20 pts

Give an example program with data parallelism

Your Answer:

Anything involving matrix operations (add, subtract, multiply, etc), like video games.

Possible examples are matrix addition, matrix multiplication, etc.

Question 2 — 19 / 20 pts

In the vector architecture discussed in the class, what are the main components that support data parallel operations?

Your Answer:

1. Vector load and store ICs

2. Vector registers ICs

3. Full Pipeline ICs

vector registers, pipelined or duplicate functional units, vector load/store units,

Question 3

20 / 20 pts

What is the main feature that differentiate the pipelines in vector processors and those used in superscalar processors?

Your Answer:

Superscalars have hazard detection, where Vector doesnt.

The pipeline used in vector architecture does not require hazard detection logic while the pipeline used in superscalar does.

Question 4

5 / 5 pts

Can superscalar processors execute data parallel applications?

Correct!

- (selected) True
- False

Question 5

5 / 5 pts

Can multicore processors execute data parallel applications?

Correct!

- (selected) True
- False

Question 6

20 / 20 pts

What is the purpose of stripe mining?

Your Answer:

With a for loop stop conditional being "n", which may not be known at compile time or larger than max vector length. So it converts the loop so it will work.

Stripe mining is a technique to transform a loop whose iteration is unknown at the compile time or the number of iterations is not same the vector width of the architecture.

Quiz Score: **89** out of 90