HW2 AMAT = HT + MR·MP

B1 HT = 1c, MR = 110c, RAM = 105c (Cache Disabled)

a.) MR = 3% = 0.03

HR = 1 − .03 = 0.97

AMAT = .97(1) + .03(110) = .97 + 3.3 = 4.27 cycles

b.) 1GB = 10^9B = 10^6KB = 10^3MB, KB = 10^3B

$\frac{64KB}{10^6KB} = 6.4 \times 10^{-5} = .000064$, $1 - 6.4e^{-5} = .999936$

AMAT = .000064(1) + .999936(110) = 109.993024 ≈ 109.99 cycles

c.) Without using locality, using the cache is actually a little bit slower. So unless you are properly utilizing locality, its better in this case not to use cache

d.) HT vs RAM: Δ = 104c = G

ΔRAM vs MP: 5c = L

105c = (1 − MR)·1c + 110c(MR)

105c = 1c − 1cMR + 110c(MR)

104c = 1cMR + 110cMR

104c = MR(111c)

$MR = \frac{104c}{111c}$ = 0.9369 ≈ 0.94 ≈ 94%

Hw2

a.) Associative cach 64 B blks 512 B 2000 B

512/64 = 8 Blocks 2048/64 = 32

Blks	Mem
0	m0 - m31
1	m0 - m31
2	" "
3	" "
4	" "
5	" "
6	" "
7	" "

b.)

Blks	set	Mem
0-3	0	Even: m0, m2, ..., m30
4-7	1	Odd : m1, m3, ..., m31

Hw2

$f = 1.1\,GHz$, CPI = 1.35, Load = 20%, Store = 10%

hit = no penalty L1, i/d cache = Direct Mapped 32KB

icache = 2% miss rate & 32-byte block size

dcache = 5% miss rate & 16-byte block size

↳ 95% of all writes have no stalls

L2 = 512 KB, unified, 64-byte blocksize, 15ns access time

↳ L1 connection 128-bit bus @ 266MHz, 128-bit word/$\hat{}_{bus}$cycle

↳ 80% satisfied without main mem (hit rate?)

↳ 50% are dirty

Main Mem = 128-bit wide, 60ns, 133MHz, one per cycle

$mp(L1) = h(L2) + mr(L2) \cdot mp(L2) = 15ns + .2(90) = 33ns$

$mp(L2) = 60ns + \left(\frac{4c}{1} \cdot \frac{ns}{0.133c} = 30.0752ns\right) = 90.0752ns$

64B(8) = 512bits / 128b = 4cycles

$\text{one cycle} = \frac{133(10^6)\,cycles}{sec} \cdot \frac{10^{-9}\,sec}{ns} = \frac{133(10^{-3})\,c}{1ns} = \frac{.133\,cycles}{ns}$

$AMAT = h(L1) + mr(L1)mp(L1) = 0 + .02(33ns) = .66ns$

$$h(L2) = \text{AccessTime}(L2) + \left(\frac{\text{BlkSize}(L1)}{\text{Bus Size}} \cdot \frac{ns}{3\times10^9}\right)$$

B5 a.) Avg. mem access time for I access?

$mp(L1) = h(L2) + mr(L2) \cdot mp(L2)$

$mp(L2) = 60ns + \left(\frac{64B}{16B} \cdot \frac{ns}{.133}\right) = 60ns + 30ns = 90ns$

$128b/8 = 16B$

$h(L2) = 15ns + \left(\frac{32B}{16B} \cdot \frac{ns}{.266} = \frac{2ns}{.266} = 7.5ns\right) = 22.5ns$

$mp(L1) = \overset{Hit(L2)}{22.5ns} + \overset{Miss(L2)}{.2(90ns)} + \overset{MissWB(L2)}{.2(.5)(90)} = 22.5 + 18 + 9 = 49.5$

$AMAT(L1) = 0ns + .02(49.5)ns = 0.99ns$

b. $h(L2) = 15ns + \left(\frac{16B}{16B} \cdot \frac{ns}{.266} = 3.76ns\right) = 18.76ns$

$mp(L1d) = 18.76ns + .2(90ns) + .2(.5)(90) = 18.76 + 18 + 9 = 45.76$

$AMAT(L1d) = 0ns + 0.05(45.76) = 2.29ns \approx 2.3ns$

c.) $h(L2) = 18.76ns \rightarrow$ write to L2

$mp(L2) = 90ns \rightarrow$ write to mem

$mp(L1) = 18.76ns + 90ns + .5(90ns) = 18.76 + 135ns = 153.76$

$Total = 0.05(153.76ns) = 7.688ns \approx 7.69ns$

B5. d.) $CPI = 1.35 + 0.2(2.3)(1.1) + 0.1(7.69)(1.1) + .99(1.1) = 3.7909 \approx \boxed{3.8}$

B9

HW 2

2.18 a.)

Way Pred

HT = .8(2c) + .2(3) = 1.6c + .6c = 2.2c

AMAT = 2.2c(.978) + 20(.022) = 2.5916 ≈ 2.6c

Reg

AMAT = 3 + .0033(20) = 3 + .066 = 3.066 ≈ 3.1c

Way Pred is less than 4-way

2.6c < 3.1c

c.) $AMAT_{current}$ ≈ 3.1c

$Amat_{4way}$ = .8(2) + .2(15) + .0033(20) = 4.666 ≈ 4.7c

Idk if else IDK wtf they mean by pos or negative but Way pred is (4.7c - 3.1c) = 1.6c

HW2

2.20 a) without = 120 c

with = 120 + 3(16)c = 168 c

b) Depends on other factors, if miss rate were lower & hit time is the same or faster than yes, it would be.

2.21 a) 16 bytes

b) Non = 16b/4c = 4 b/c

Merge = 8b/1c = 8 b/c

Speedup = 8/4 = 2 x speedup

c) Misses hold the cache up with blocking but don't with non-blocking.