# Q4

**Due** Sep 16 at 11:59pm **Points** 100 **Questions** 4
**Available** Sep 15 at 12pm - Sep 16 at 11:59pm 1 day **Time Limit** 20 Minutes

## Attempt History

| | Attempt | Time | Score |
|---|---|---|---|
| **LATEST** | Attempt 1 | 11 minutes | 0 out of 100 * |

* Some questions not yet graded

Score for this quiz: **0** out of 100 *
Submitted Sep 16 at 4:51pm
This attempt took 11 minutes.

### Question 1 — Not yet graded / 25 pts

Name two cache optimizations, and show how each one affects the following three factors: hit time, miss rate, and miss penalty

Your Answer:

1. Larger Cache:

HT: Doesnt effect

MR: May increase conflict/capacity misses

MP: Increases miss penalty

2. Higher Associativity:

HT: Increases hit time

MR: Reduces conflict misses

MP: Larger miss penalty

The answers vary depending on the optimizations listed.

## Question 2

**Not yet graded / 25 pts**

What is a virtually addressed but physically tagged cache? What is the purpose of this optimization?

Your Answer:

Virtually addressed but physically tagged can access L1 cache while translating address in parallel. This reduces L1 hit time.

It uses the page offset of virtual address (low order bits) to access L1 cache while the address translation is performed in parallel. It aims to reduce hit time of L1 cache access.

## Question 3

**Not yet graded / 25 pts**

Is the following statement true of false? Briefly explain.

Way prediction is a general optimization for all different cache organizations.

Your Answer:

False. Way prediction only works with associative cache, since it tries to predict the set where data could be. It will not work with direct mapped cache since it goes to a specific block.

It is false as it is used to predict which way in a set should be accessed before the tag comparison completes. Therefore, it is used for associative caches.

## Question 4

**Not yet graded / 25 pts**

What aspects of cache performance does multi-level cache aim to optimize?

Your Answer:

It aims to optimize hit time and miss rate/penalty by splitting up the cache. The L1 cache is small to keep hit time fast and the L2 is larger and captures as many L1 misses & lower miss penalty as it can, this keeps miss rate lower from having to go into main memory effectively lowering avg miss penalty since it has to go into main memory less.

L1 cache: small, simple to reduce hit tim

L2 cache: large and set-associative to reduce miss rate.

Quiz Score: **0** out of 100