Q8

Due Oct 22, 2018 at 11:59pm **Points** 100 **Questions** 5
Available until Oct 22, 2018 at 11:59pm **Time Limit** 20 Minutes

This quiz is no longer available as the course has been concluded.

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	20 minutes	100 out of 100

Score for this quiz: **100** out of 100
Submitted Oct 22, 2018 at 11:57pm
This attempt took 20 minutes.

Question 1 — 20 / 20 pts

Name two branch prediction schemes.

Your Answer:

1. Pipeline Flush

2. Predicted-not-taken

any two from pipeline flush, predict-take, predict-not-taken, delayed branch.

Question 2 — 20 / 20 pts

Assume that branches comprise 20% of all instructions. Also assume that the branch prediction is 80% accurate and incurs a 2 cycle stall on each misprediction. What is the impact of control hazards on the CPI of the pipelined processor? Ignore all other sources of pipeline hazards.

Your Answer:

+0.08

additional 0.2*(1-0.8)*2 = 0.08 stall cycles to the original CPI.

Question 3

20 / 20 pts

Explain what the branch delay slot is.

Your Answer:

The branch delay slot comes from when the branch instruction is ran in MIPS. The branch condition and target is finished at the instruction decode stage instead of the exec stage, so the next instruction needs to be stalled until that completes.

In MIPS pipeline architecture, branch target and branch condition computation finish at the end of the ID stage. Therefore, the following instruction needs to be stalled for 1 cycle. This stalled 1 cycle is the branch delay slot.

Question 4

20 / 20 pts

In class, we know that the branch history table is addressed using the lower K bits of the addresses of the branch instructions. Why so?

Your Answer:

keeps the branch history table smaller by using less bits.

To control the area overhead of the branch history table.

Also, the experiments show that larger tables do not improve prediction accuracy much.

Question 5

20 / 20 pts

Use the hazard detection discussed for the MIPS pipeline implementation to show the logic condition to detect the hazard between the sequence of two instructions below.

ld x1, 45(x2)

add x5, x1, x7

Make sure you use proper pipeline registers and their corresponding components for the answer.

Your Answer:

IF/ID.IR[x1] == ID/EX.IR[x1]

IF/ID.x1 == ID/EX.x1

or

IF/ID.Regs[rs] == ID/EX.Regs[rt]

Quiz Score: **100** out of 100