Q-3

Due Sep 9 at 11:59pm **Points** 100 **Questions** 5
Available Sep 8 at 12pm - Sep 9 at 11:59pm 1 day **Time Limit** 20 Minutes

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	13 minutes	60 out of 100 *

* Some questions not yet graded

Score for this quiz: **60** out of 100 *
Submitted Sep 9 at 11:31pm
This attempt took 13 minutes.

Question 1 — 20 / 20 pts

Which of the following cache set will the block number 10 from main memory go to? Suppose the cache is 2-way set associative with 8 blocks.

- Anywhere
- 0
- 1
- 2 **Correct!**

Question 2 — 20 / 20 pts

Assume a memory access to main memory on a cache miss takes 30 ns and a memory access to the cache on a cache hit takes 1 ns. If 80% of the processor's memory requests result in cache hits, what is the average

memory access time?

- 33
- 24.2
- 7 **Correct!**

1 + 30*0.2 = 1 + 6 = 7

- 1.6

Question 3

20 / 20 pts

Which cache write mechanism allows an updated memory location in the cache to remain out of date in memory until the block containing the updated memory location is replaced in the cache?

- Write-through
- Write-back **Correct!**
- Both
- Neither

Question 4

Not yet graded / 20 pts

Briefly characterize the relation between the number of tag bits in memory addresses and the degree of associativity of a cache.

Your Answer:

The number of associativity divides the number of cache blocks, so indexMax = numCacheBlks / degreeOfAssociativity. So increasing degree of associativity, decreases index bits while increasing tag bits.

The higher the degree of the associativity, larger the number of tag bits in memory addresses.

For fully associative cache, there are no index bits. Other than the block offset bits, all the other bits are for tag.

Question 5

Not yet graded / 20 pts

Briefly explain why the hit time of an associative cache can potential higher than that of a direct mapped cache?

Your Answer:

Hit time increaases, obviously, from overhead from searching tags in N associativity. Wider gates, more wires, more comparisons all equal longer delay times. Misses reduce, but latency is increased for hits compared to direct mapped. The performance increase on most modern applications ,using associative miss reduction, are justified compared to the latency delay of hits on most systems.

In an associative cache, tag comparison must be done before the data can be found within a block using offset, while these two steps can be done in parallel in a DM cache.

Additionally, tag comparison in an associative cache usually takes longer time.

Quiz Score: **60** out of 100