

# Q7

**Due** Oct 14, 2018 at 11:59pm      **Points** 90      **Questions** 5  
**Available** Oct 13, 2018 at 12pm - Oct 14, 2018 at 11:59pm 1 day  
**Time Limit** 15 Minutes

This quiz is no longer available as the course has been concluded.

## Attempt History

	Attempt	Time	Score
LATEST	<a href="#">Attempt 1</a>	11 minutes	75 out of 90

Score for this quiz: **75** out of 90

Submitted Oct 14, 2018 at 11:37pm

This attempt took 11 minutes.

### Question 1

5 / 20 pts

Identify all dependences in the following code with involved instruction numbers and register names.

1: LD      R1, 45(R2)

2: DADD   R5, R6, R7

3: DSUB.   R8, R5, R7

4: OR.     R8, R1, R7

Your Answer:

1. R1

2. R5

3. R5, R8

4. R1, R8

Data dependence: 1 and 4 via R1; 2 and 3 via R5

Name (or output) dependence: 3 and 4 via R8

## Question 2

15 / 15 pts

The following instruction sequence result in a stall in the 5-stage MIPS pipeline. Is that statement true or false?

LD R1, 45(R2)

DADD R5, R6, R7

DSUB. R8, R6, R7

OR. R9, R1, R7

☐ True

☒ False

Correct!

LD write to register file in the first half of a pipeline cycle, while OR reads the register file in the second half of the same pipeline cycle. So there is no conflict.

## Question 3

15 / 15 pts

In following instruction sequence:

Load R2, #60(R3)

Subtract R9, R2, #30

data hazard can be fully eliminated by forwarding (T/F).

☐ True

☒ False

**Correct!**

#### Question 4

15 / 15 pts

What are the three types of pipeline hazards?

Your Answer:

1. Structural
2. Data
3. Control

Structural, data, control/branch)

#### Question 5

25 / 25 pts

What are the three data hazards? Also identify causes of those data hazards.

**Your Answer:**

1. RAR - Read After Write: Caused by “dependence”. Subsequent instruction has actual need for data produced by earlier instruction
2. WAR - Write After Read: Called “anti-dependence”. Can’t occur in in-order pipelines (e.g., our simple MIPS pipeline).
3. WAW - Write After Write: Called “output dependence”. Can’t occur in in-order pipelines (e.g., our simple MIPS pipeline).

Hazard	Data dependence cause
=====	
RAW	true data dependence
WAW	output dependence
WAR	anti dependence

**Quiz Score: 75** out of 90