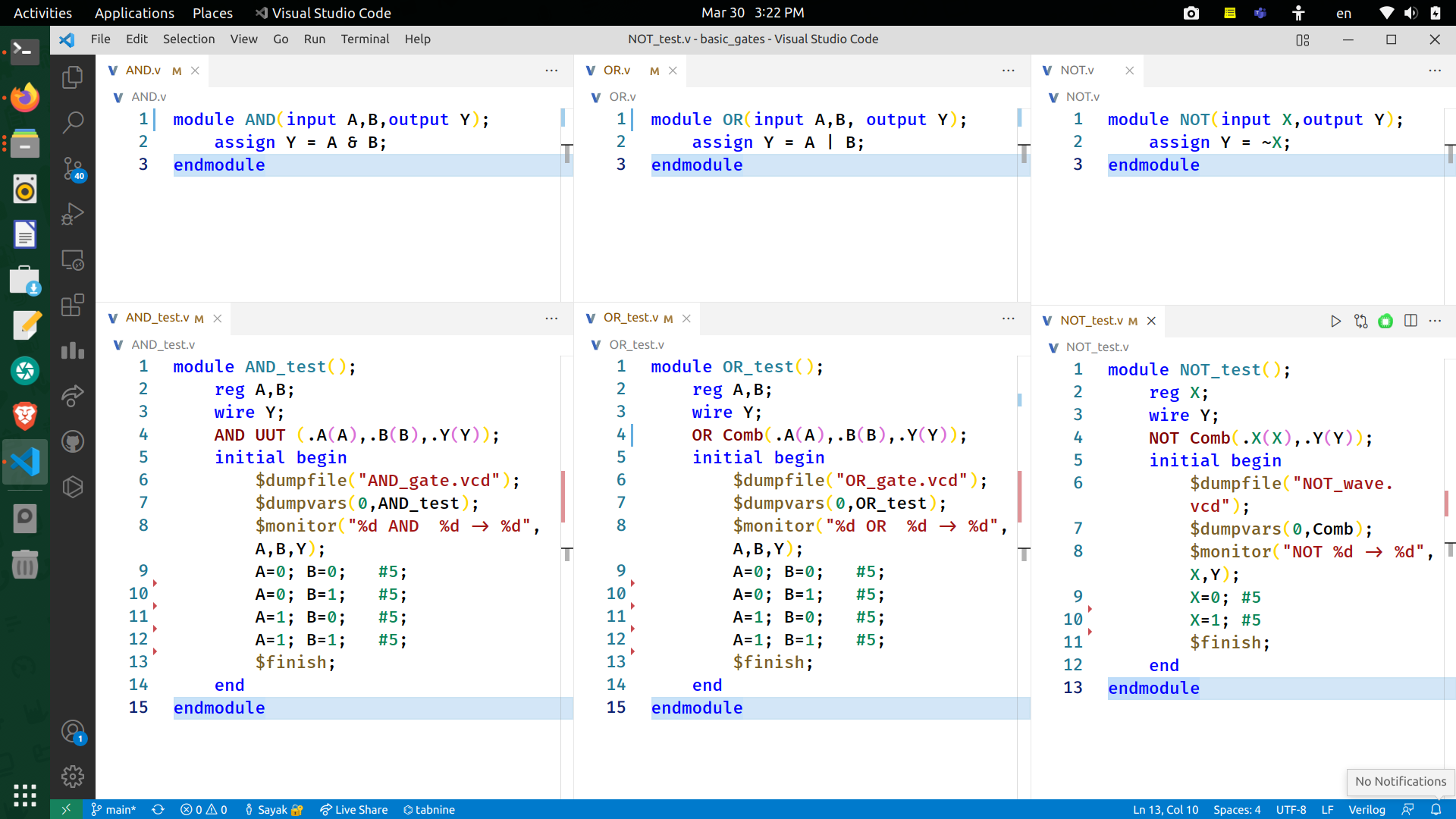
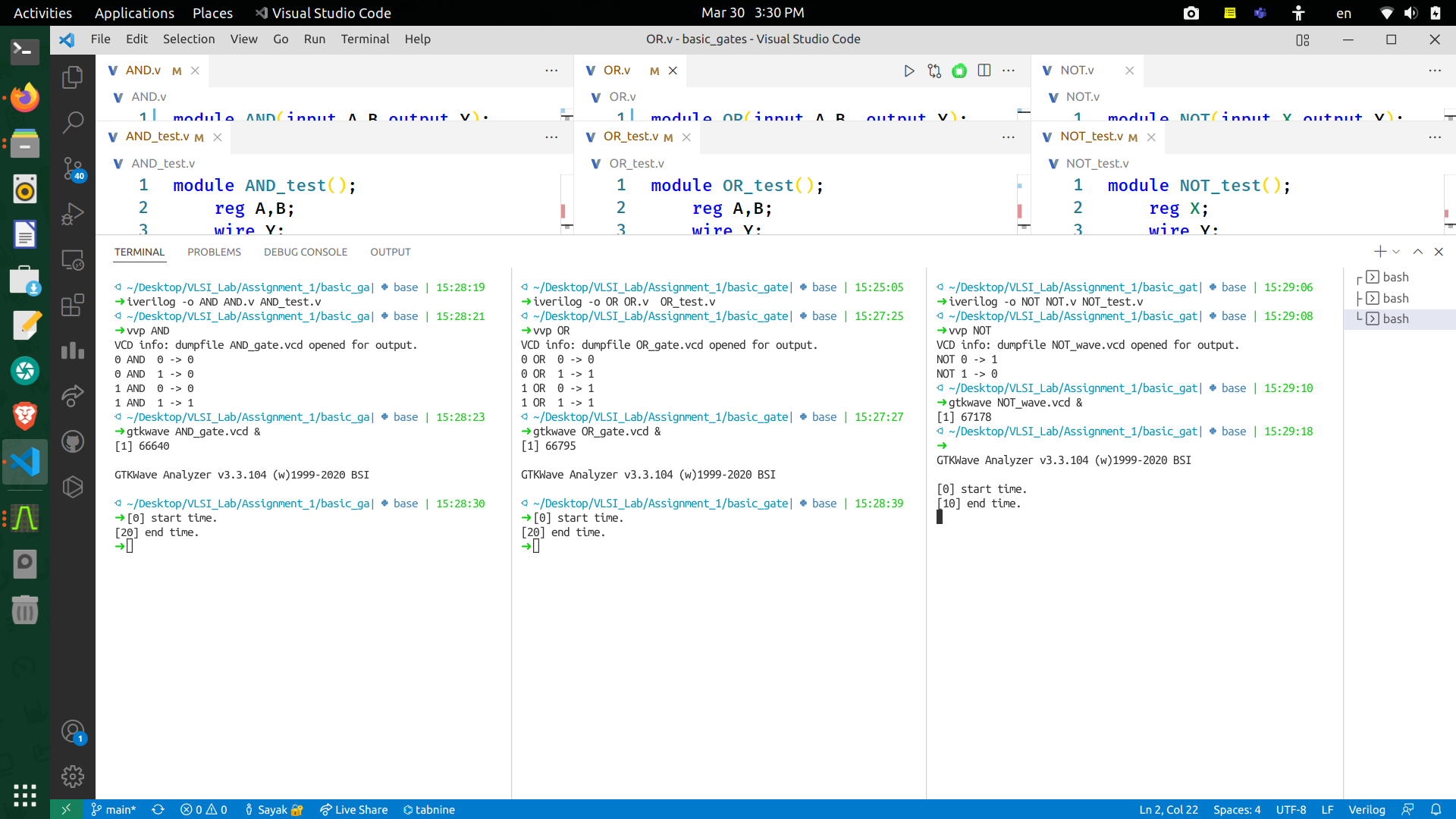
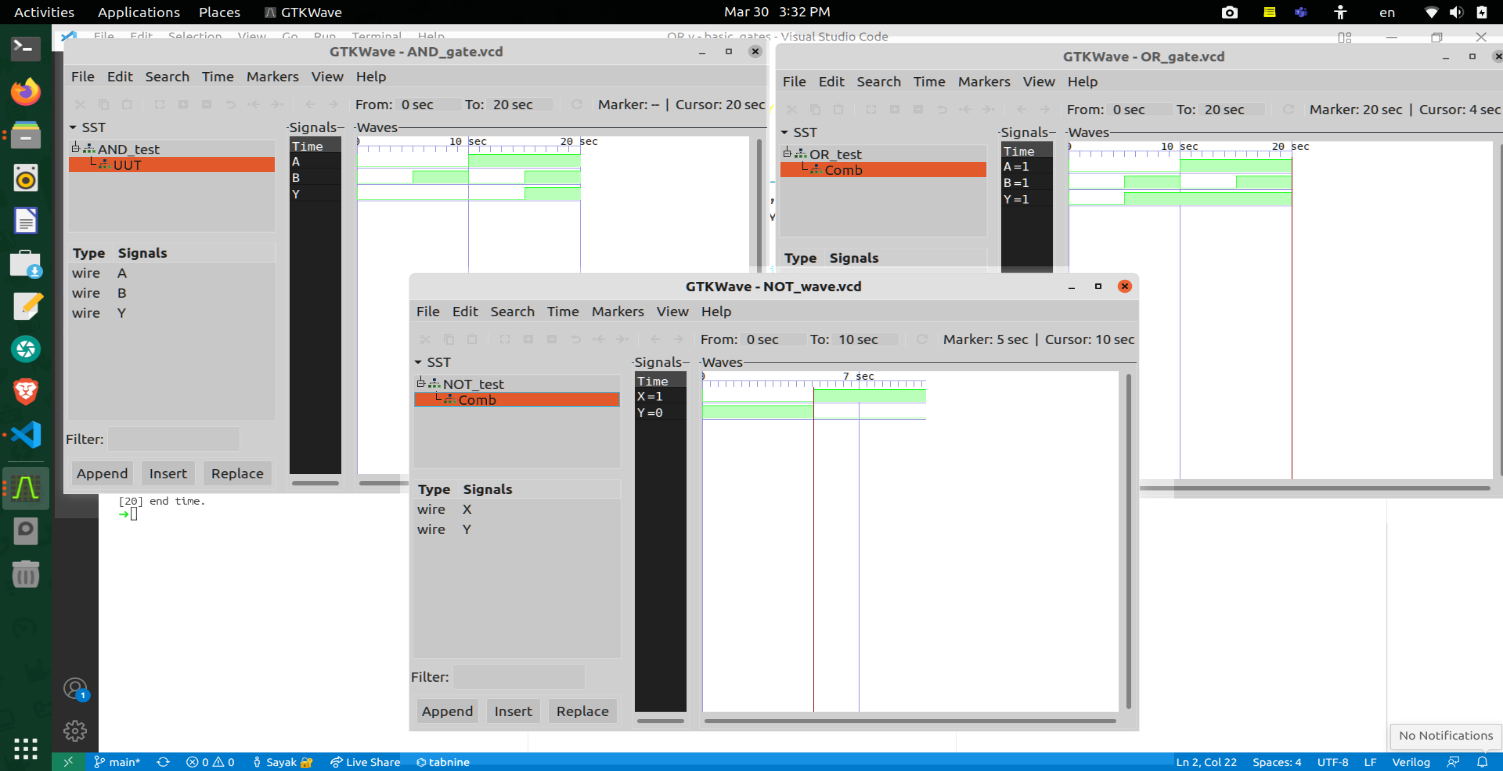
**Observations (Basic Gates):**

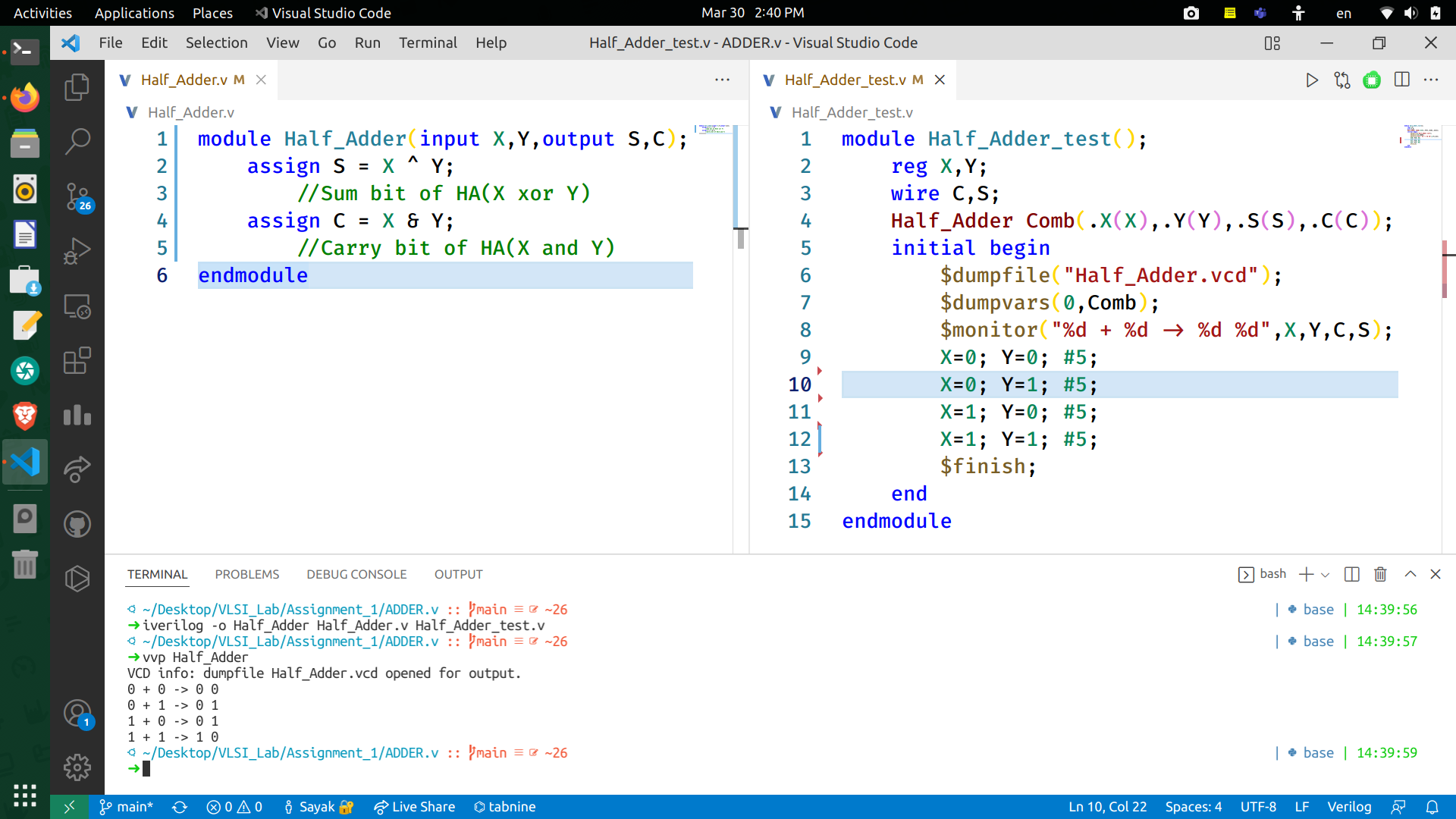
* **RTL Source Code**

(from left to right) Verilog code for AND gate, OR gate and NOT gate

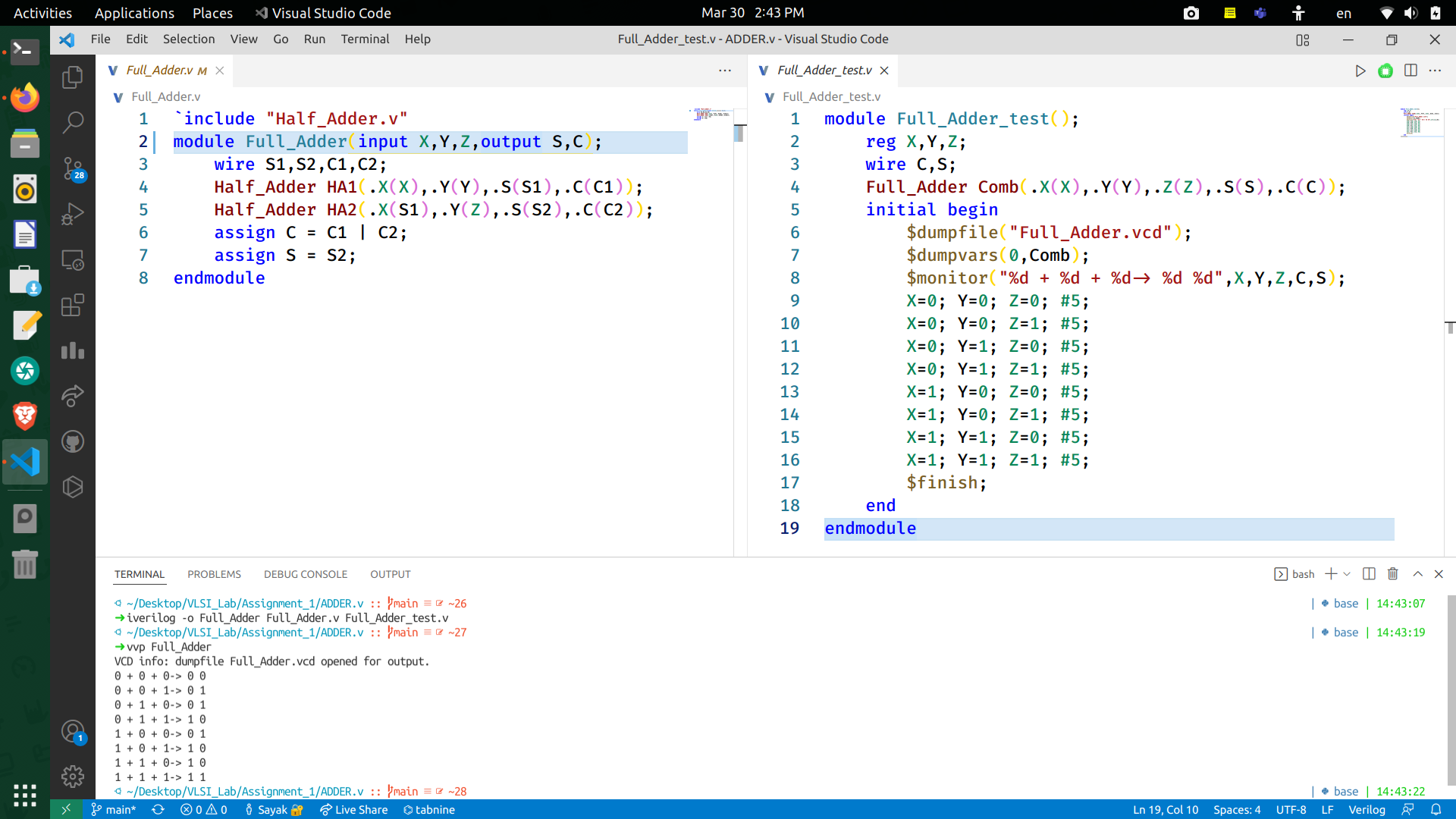
* **GTKwave Output**

(from top-left to right-bottom) gtkWAVE output for AND gate, OR gate and NOT gate

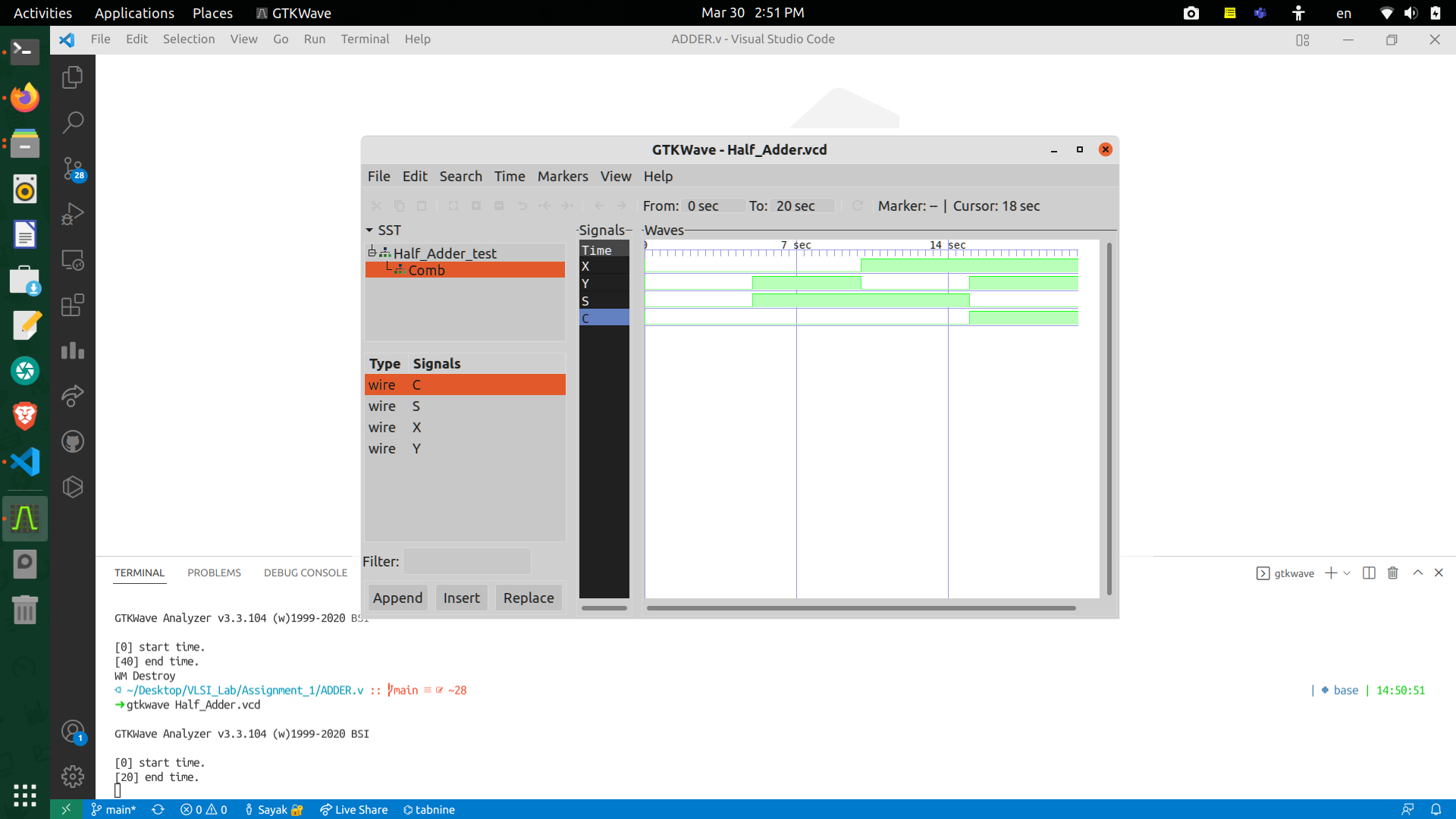
**Observations (Half Adder and Full Adder):**

* **RTL Source Code**

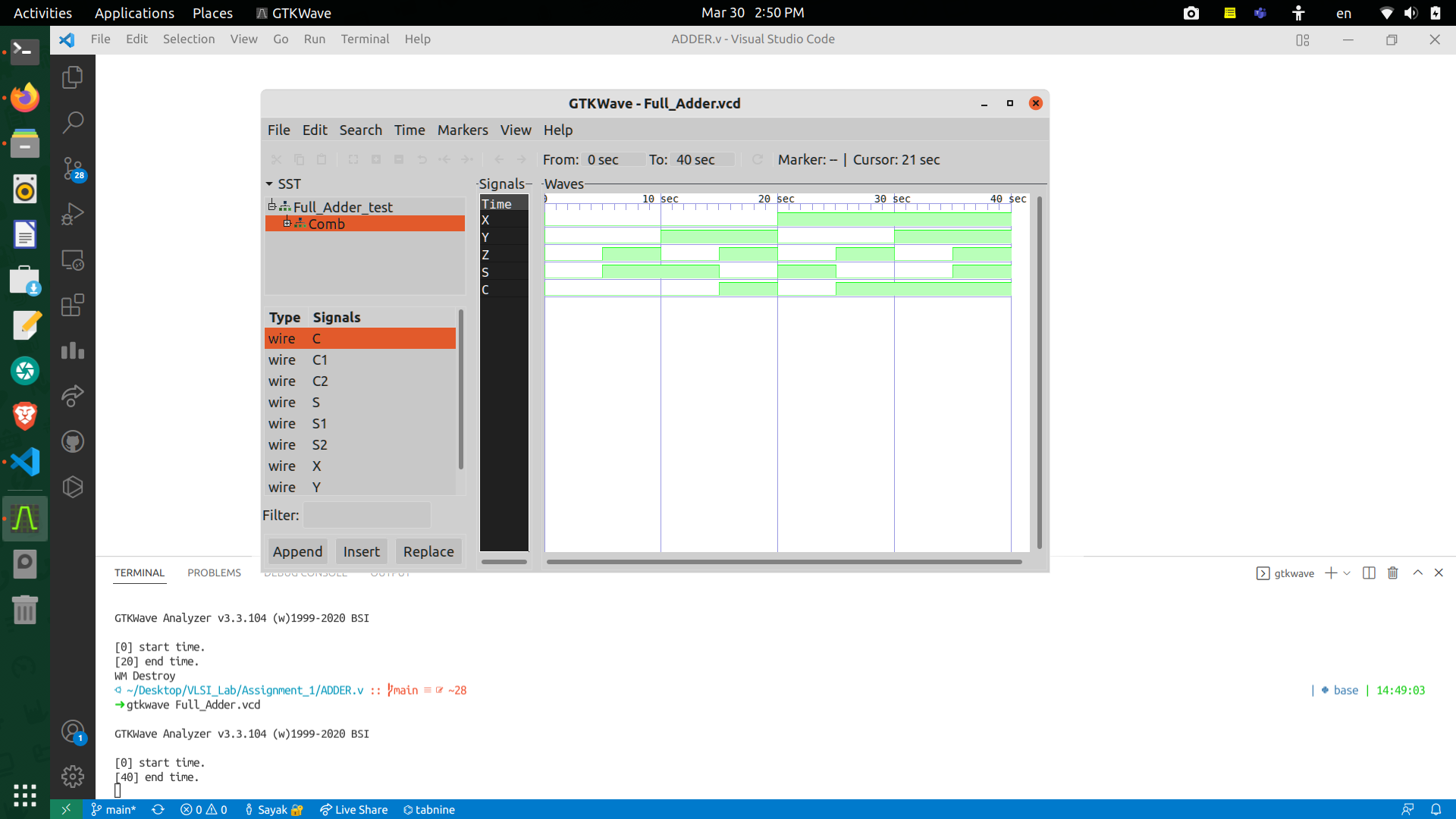
(from left to right) Verilog code for Half Adder and test bench



(from left to right) Verilog code for Full Adder and test bench

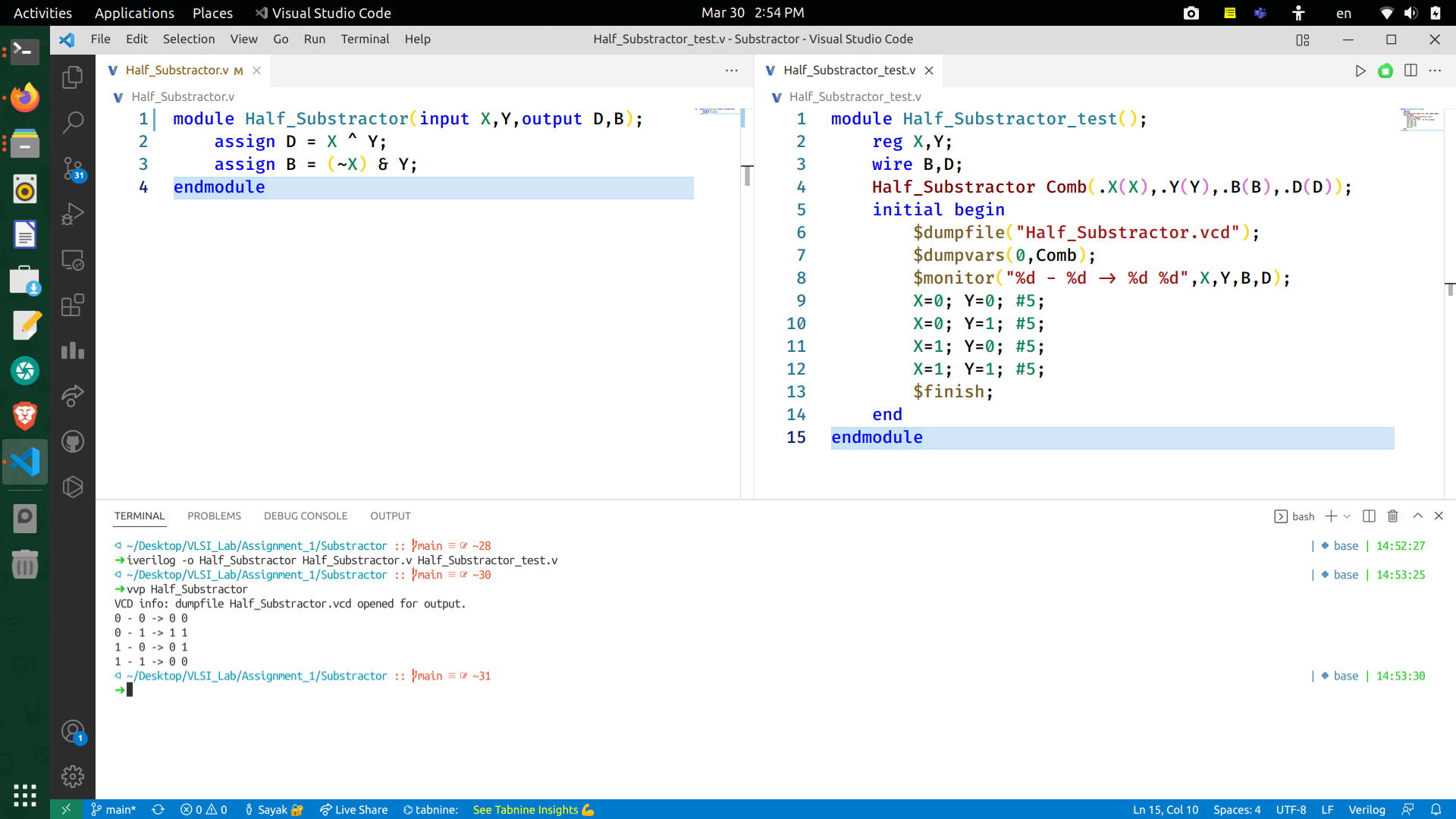
* **GTKwave Output**

gtkWAVE output of Half Adder Circuit

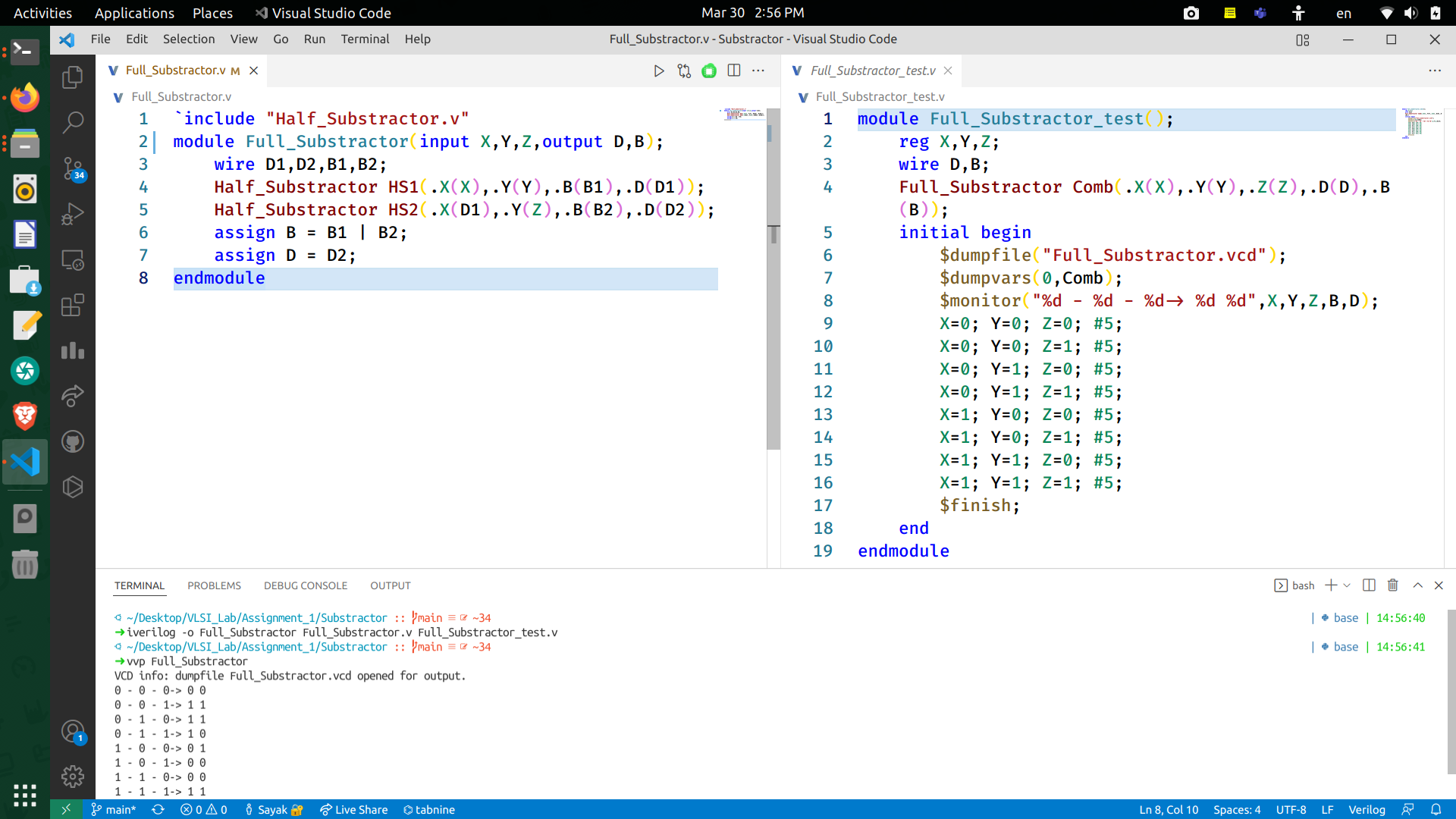


gtkWAVE output of Full Adder Circuit

**Observations (Half Subtractor and Full Subtractor):**

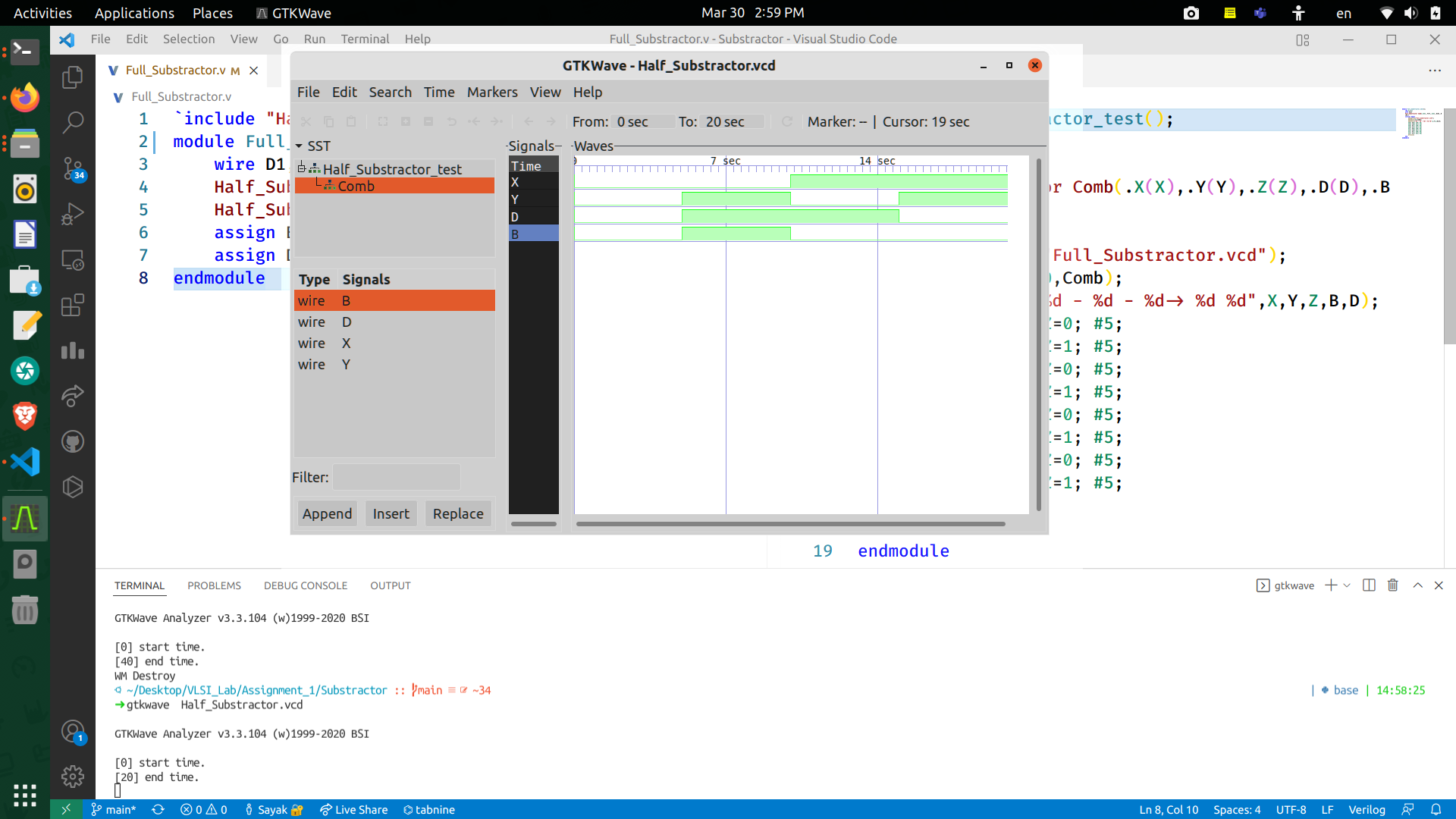
* **RTL Source Code**

(from left to right) Verilog code for Half Subtractor and test bench



(from left to right) Verilog code for Full Subtractor and test bench

* **GTKwave Output**



gtkWAVE output of Half Subtractor Circuit



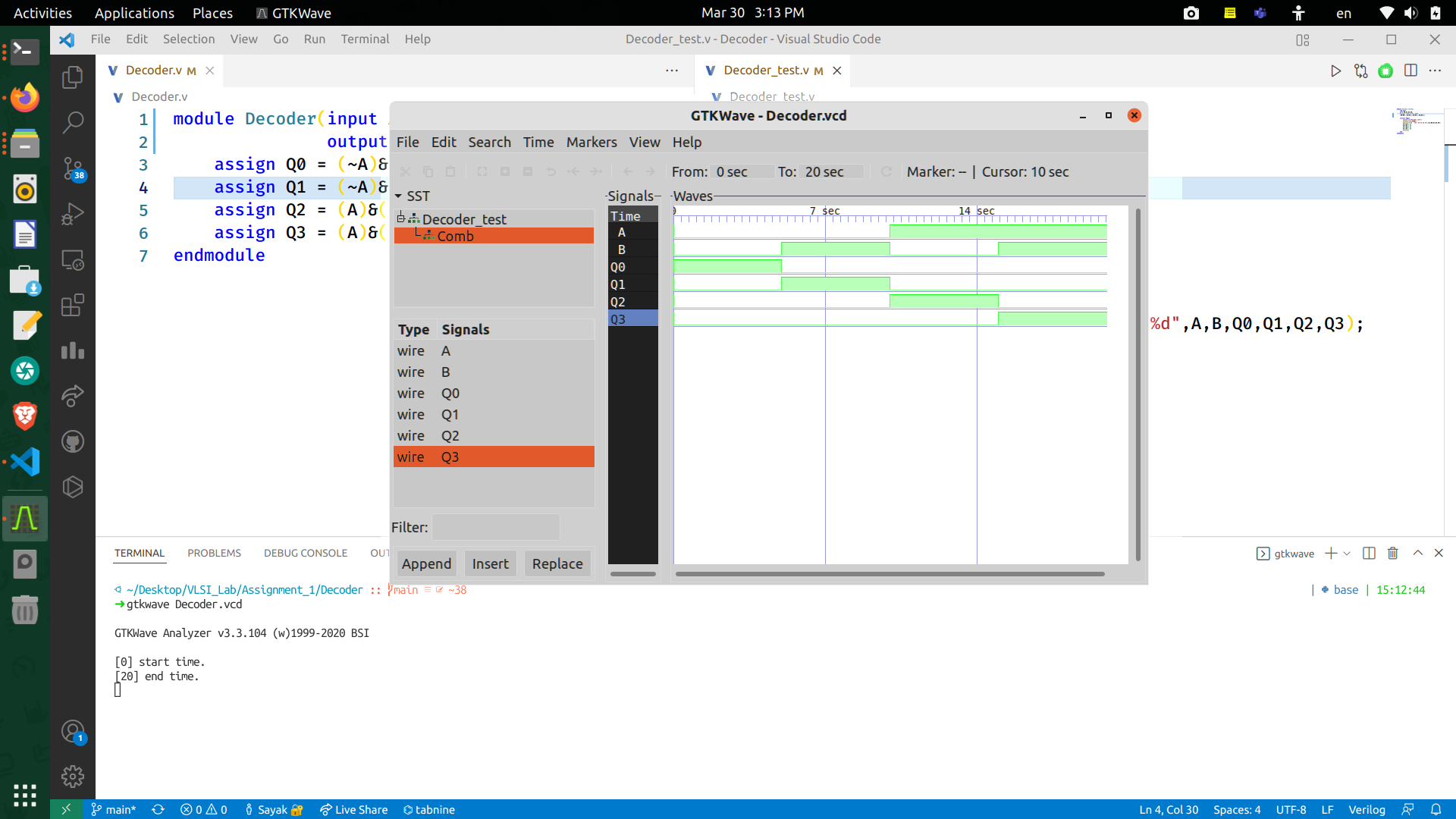
gtkWAVE output of Full Subtractor Circuit

**Observations (2:4 Decoder):**

* **RTL Source Code**



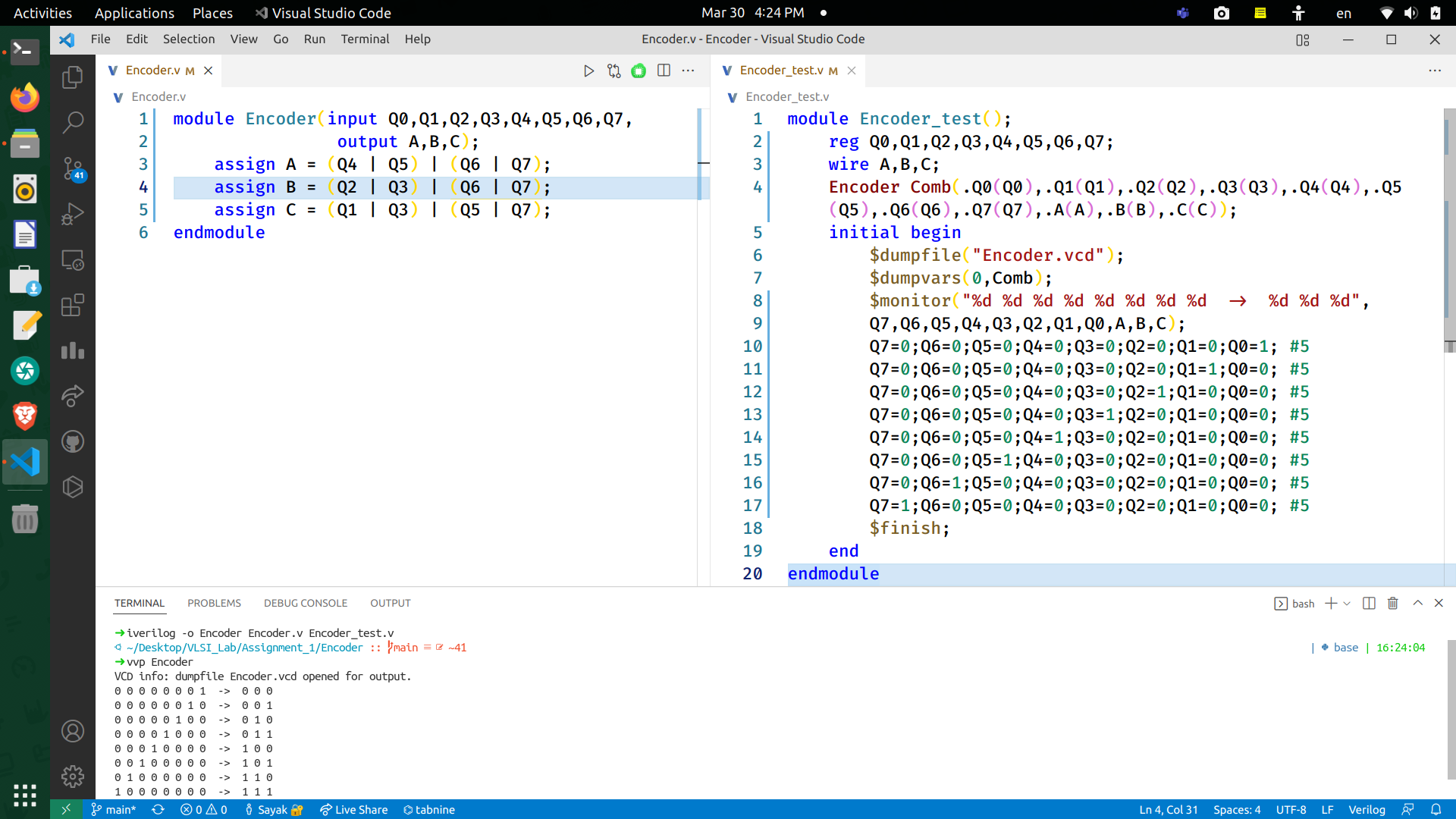
(from left to right) Verilog code for 2:4 Decoder and test bench

* **GTKwave Output**

gtkWAVE output of 2:4 Decoder Circuit

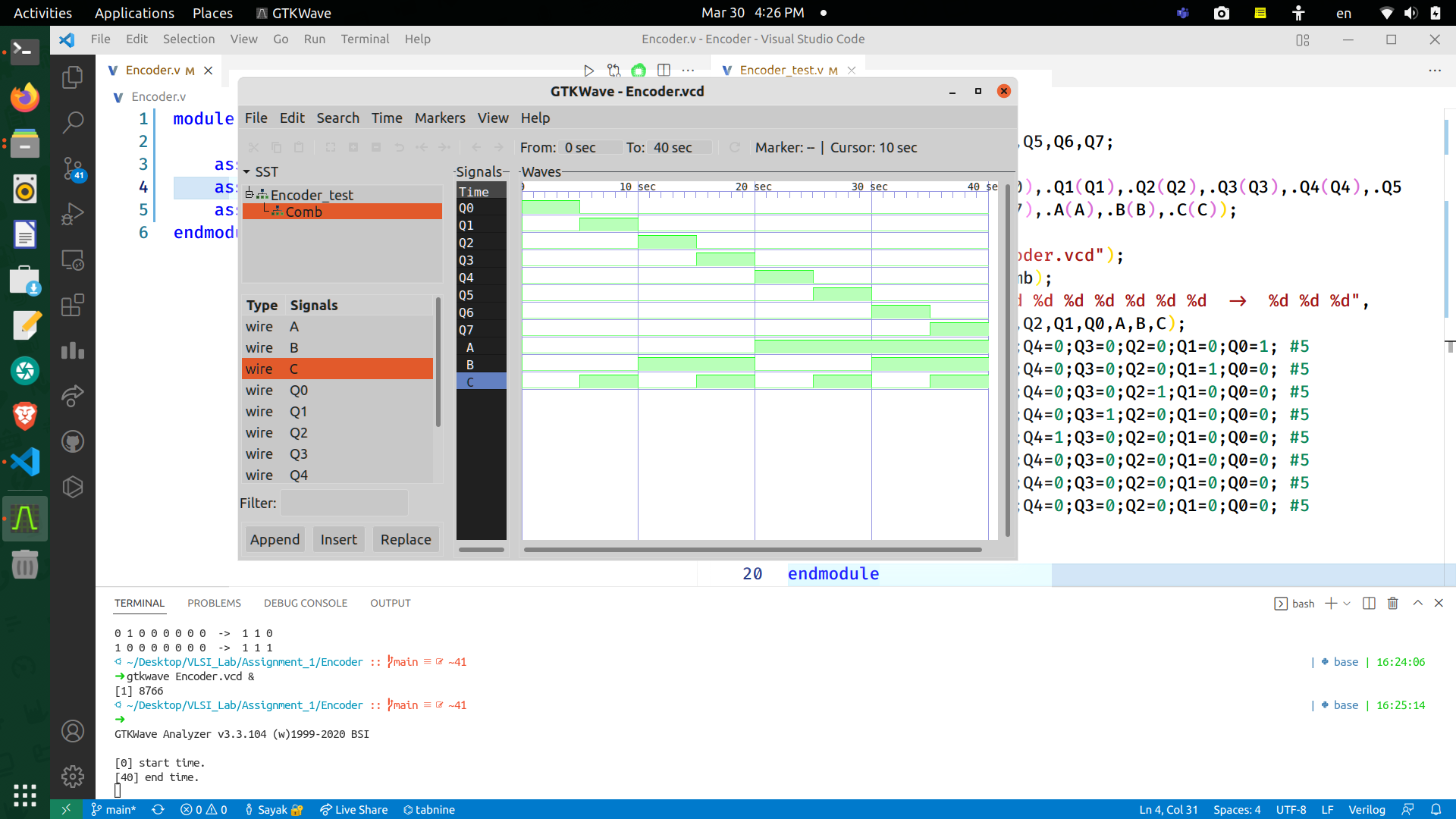
**Observations (8:3 Encoder):**

* **RTL Source Code**



(from left to right) Verilog code for 8:3 Encoder and test bench

* **GTKwave Output**



gtkWAVE output of 8:3 Encoder Circuit