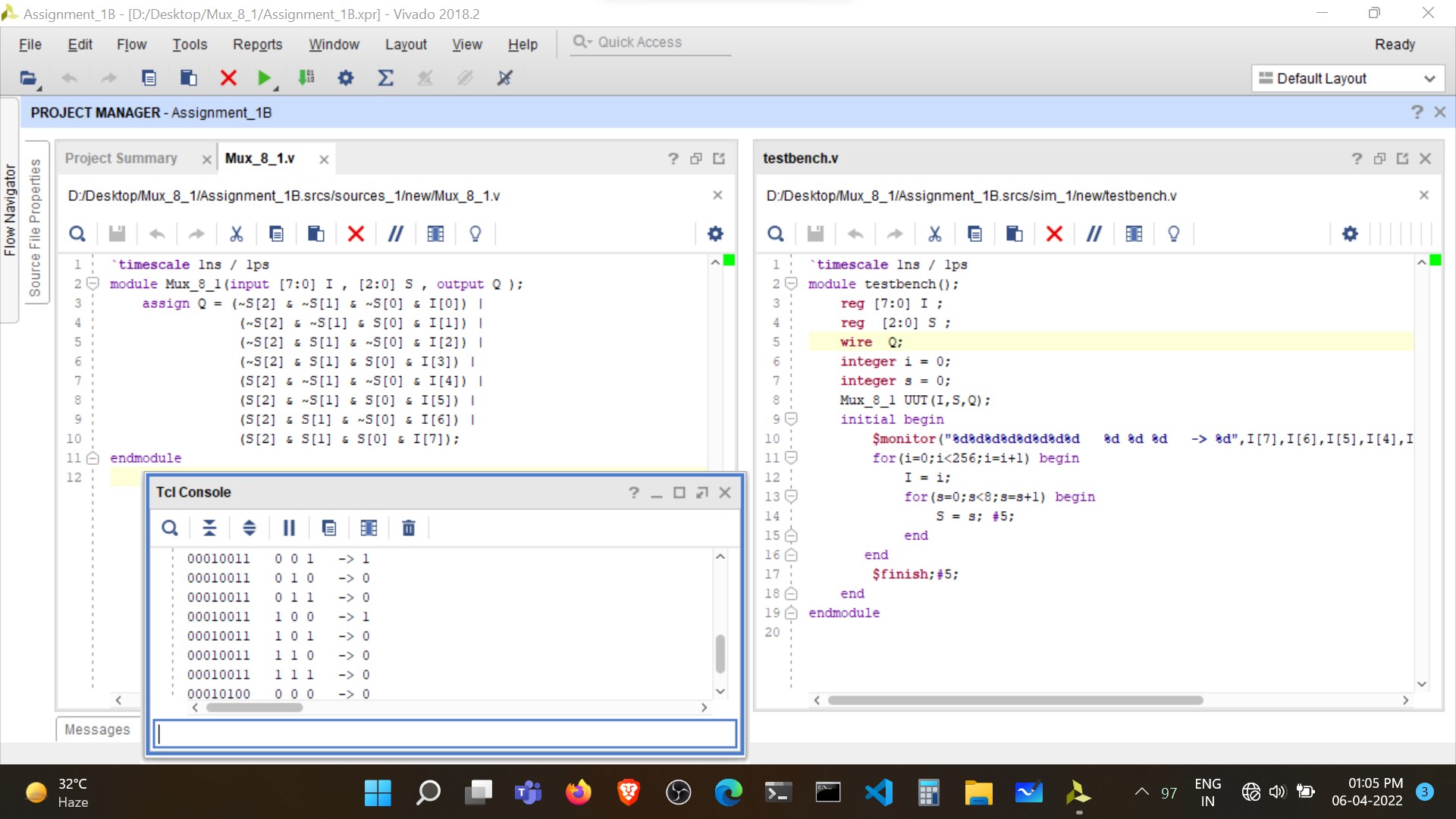
Simulation Results:

* Parity Checker

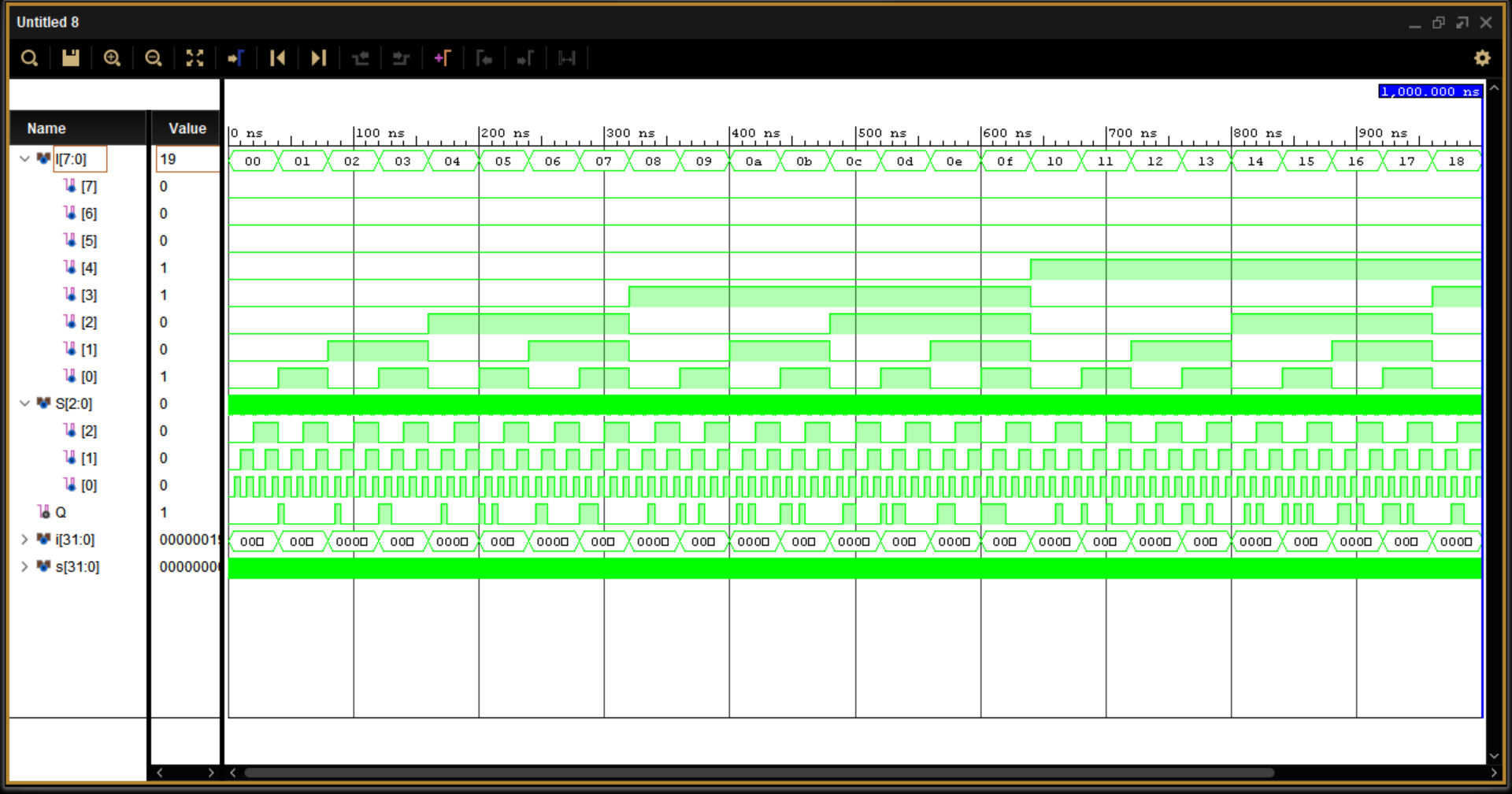
Verilog Code and Test bench for 3-bit Parity Checker



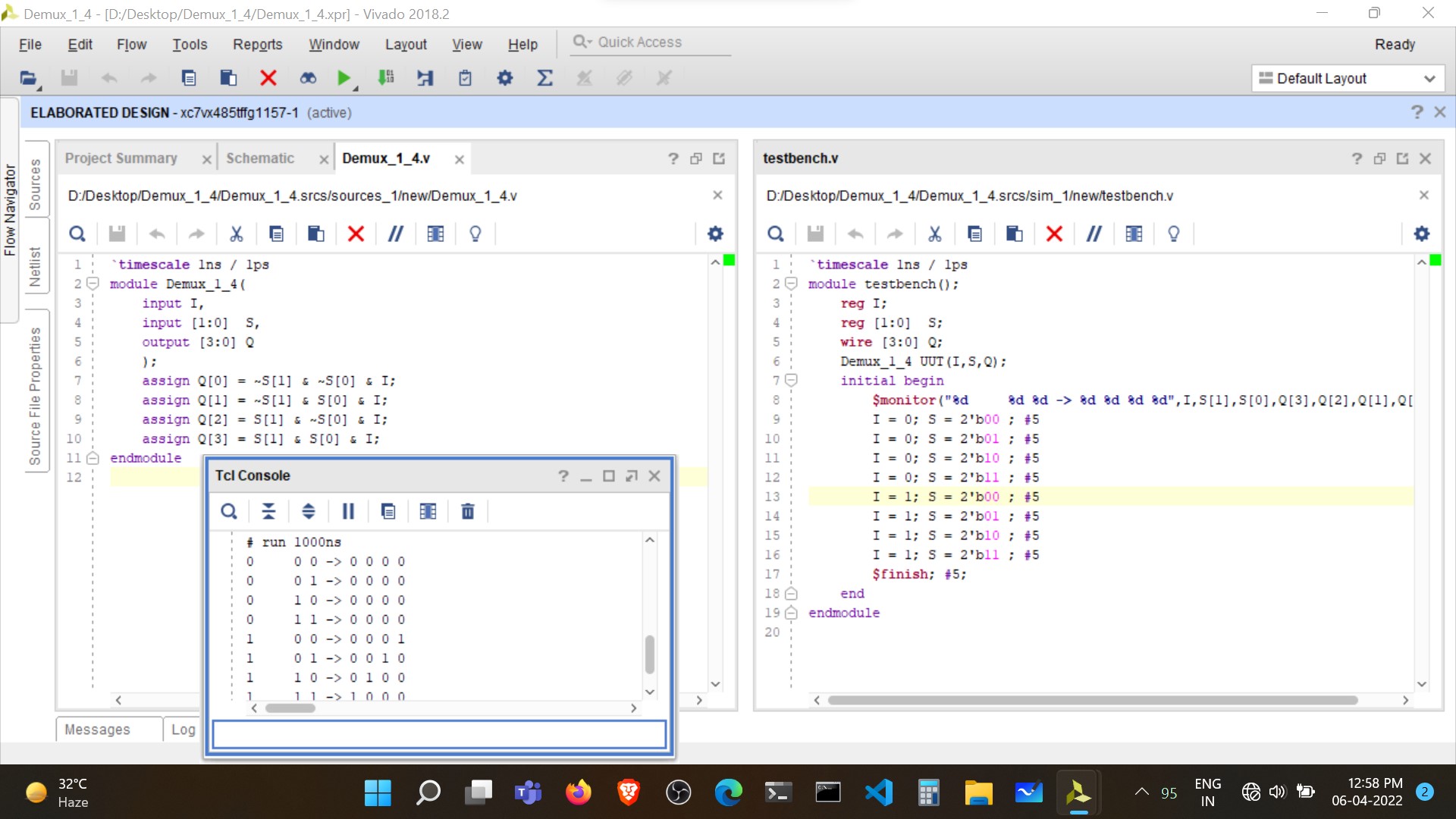
Simulation output of 3-bit parity checker

* 8:1 Multiplexer

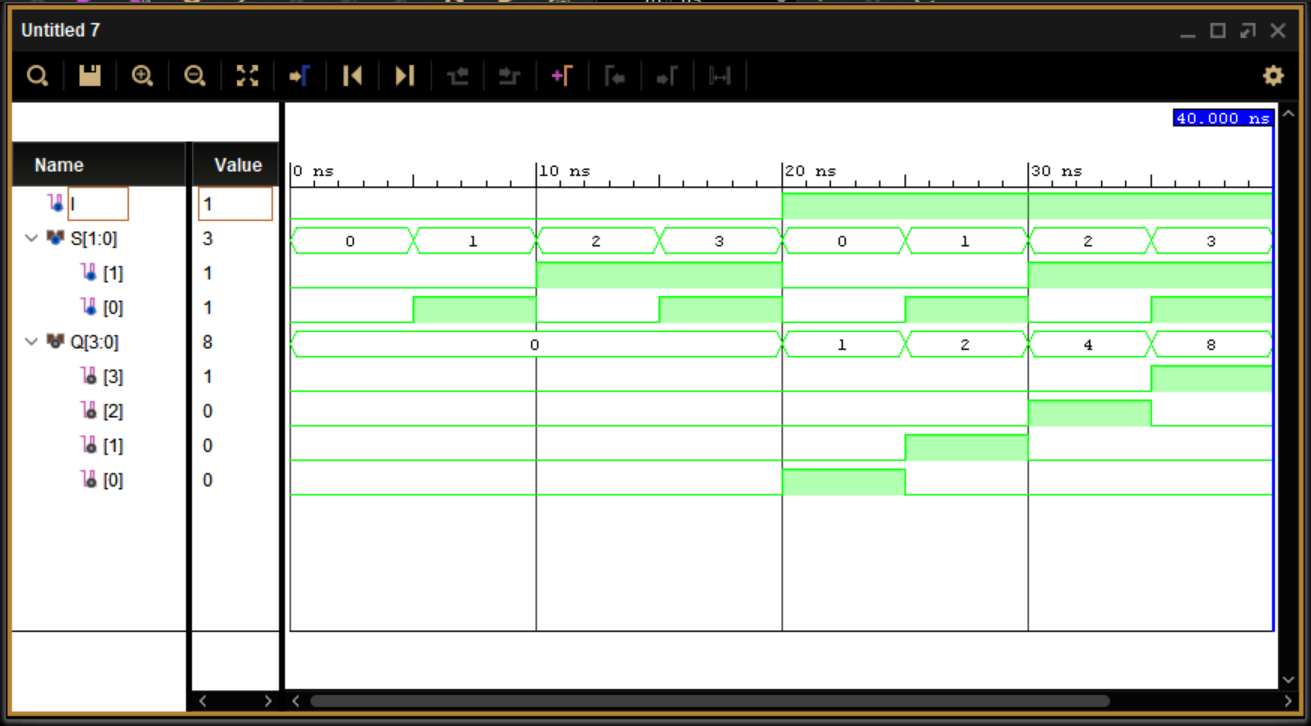
Verilog Code and Test bench for 8-bit MUX



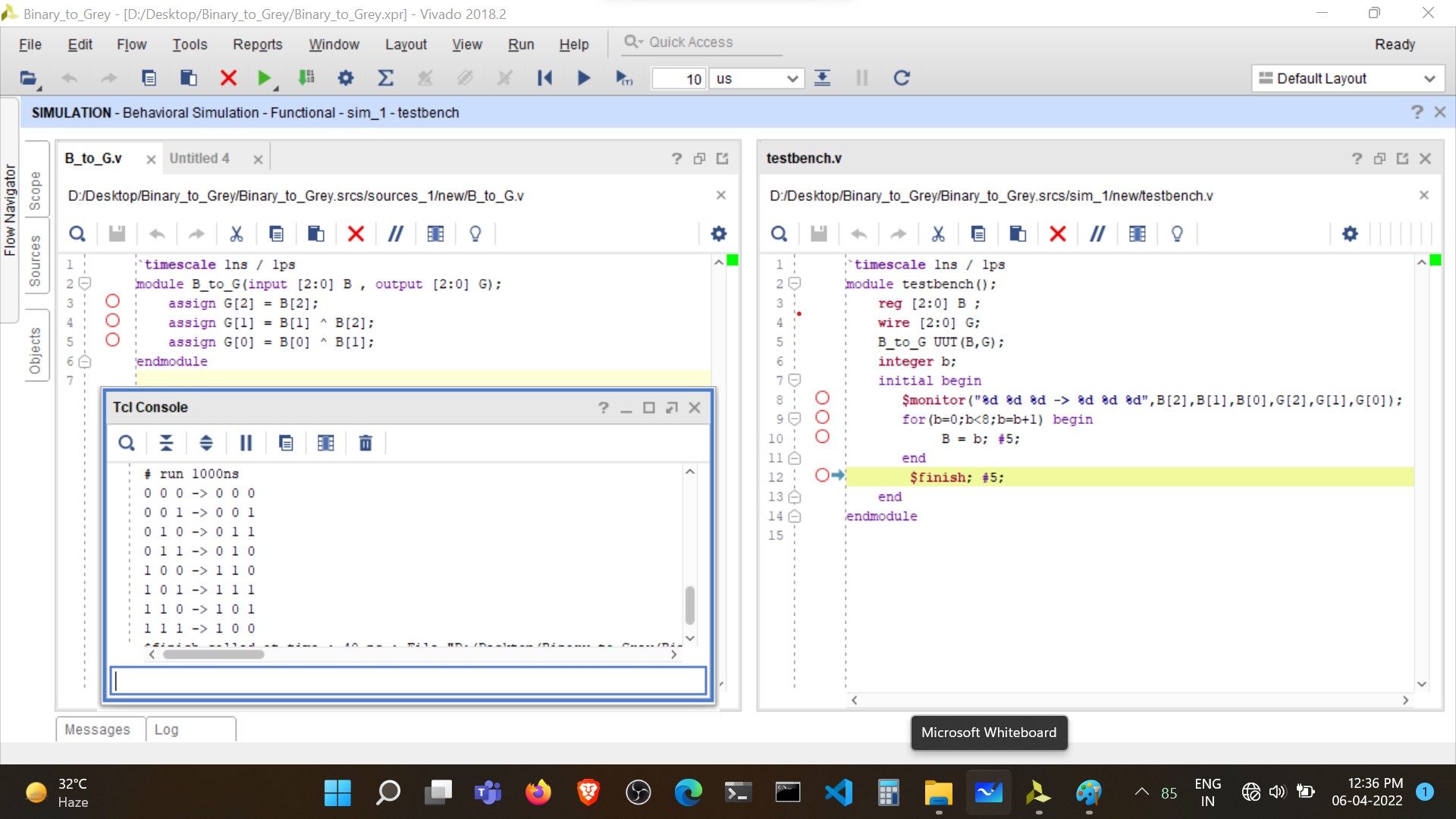
Simulation output 8:1 MUX

* 1:4 De-Multiplexer

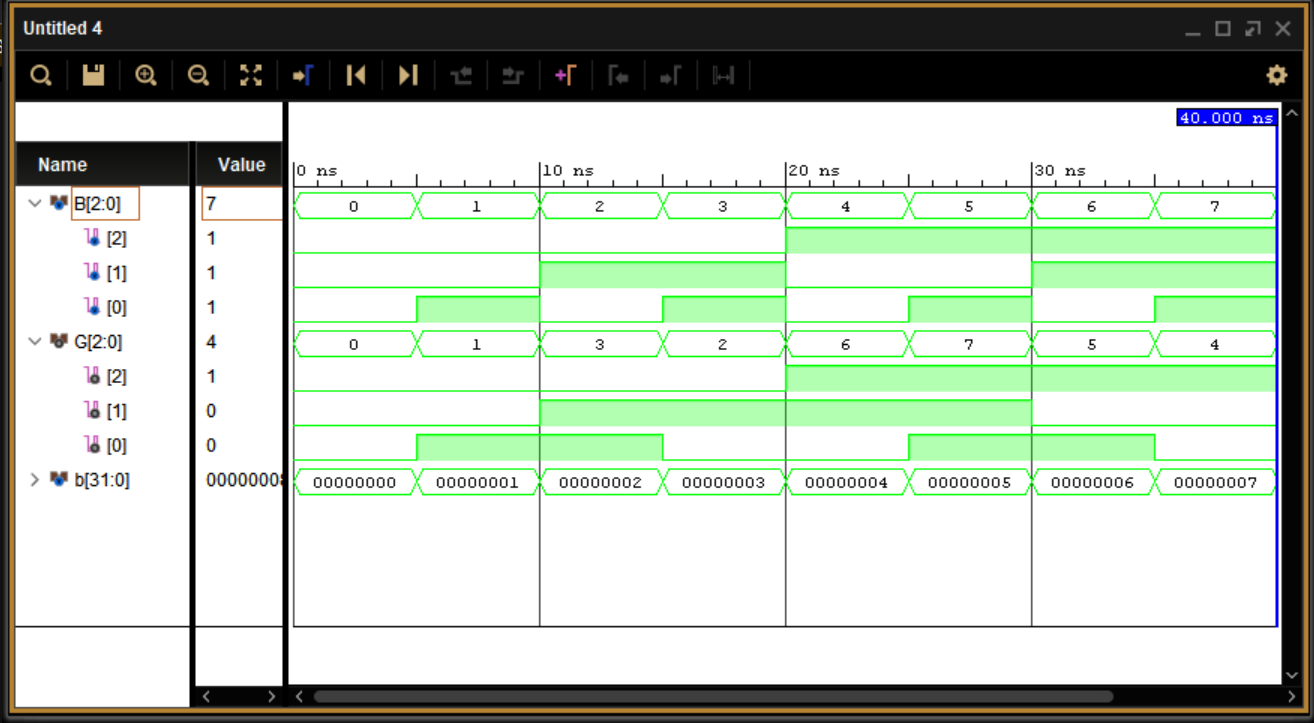
Verilog Code and Test bench for 1:4 De-MUX



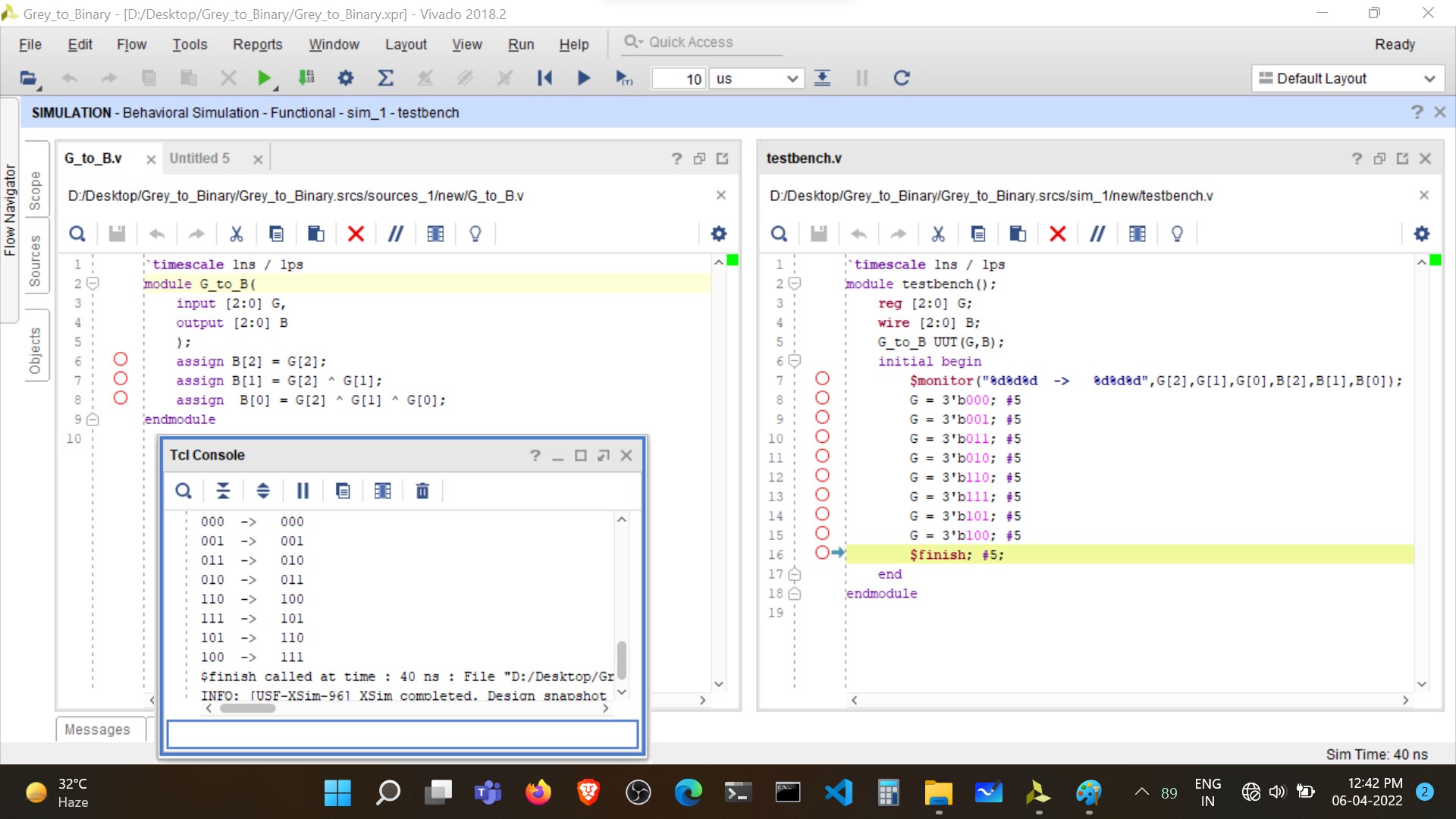
Simulation output of 1:4 De-MUX

* Binary to Gray Converter

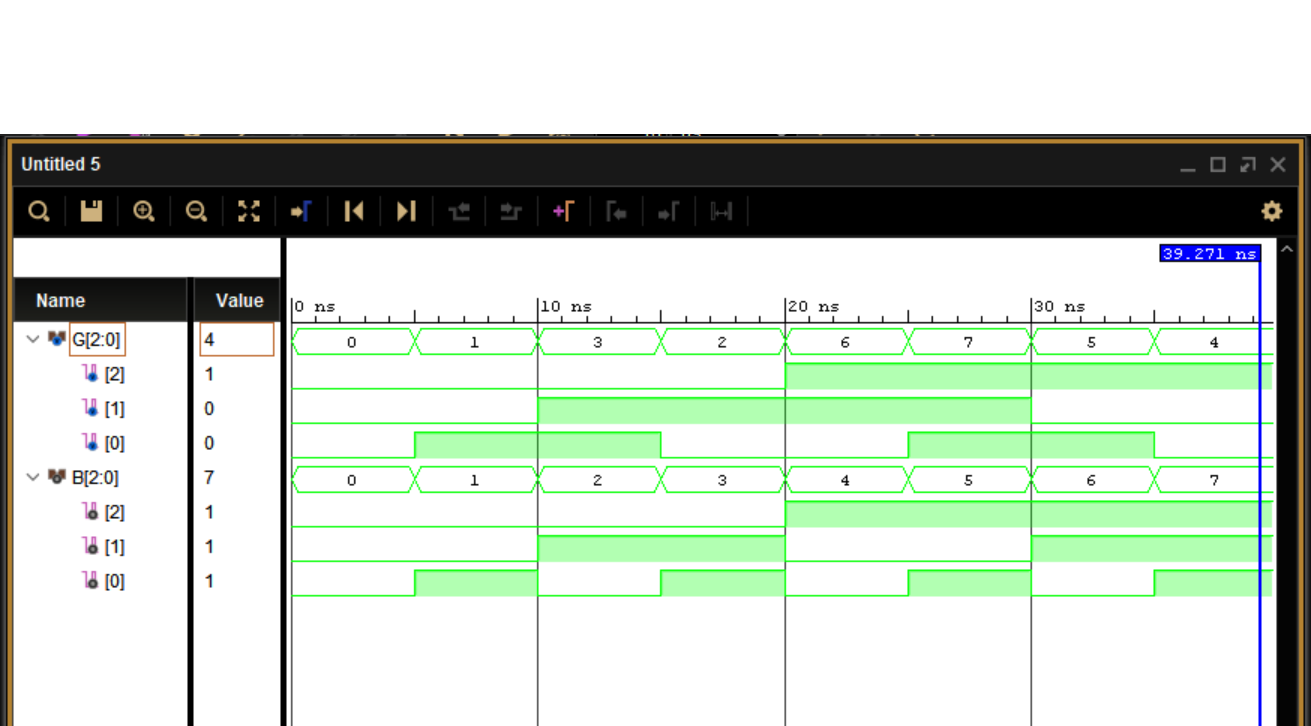
Verilog Code and Test bench of Binary to Gray Converter



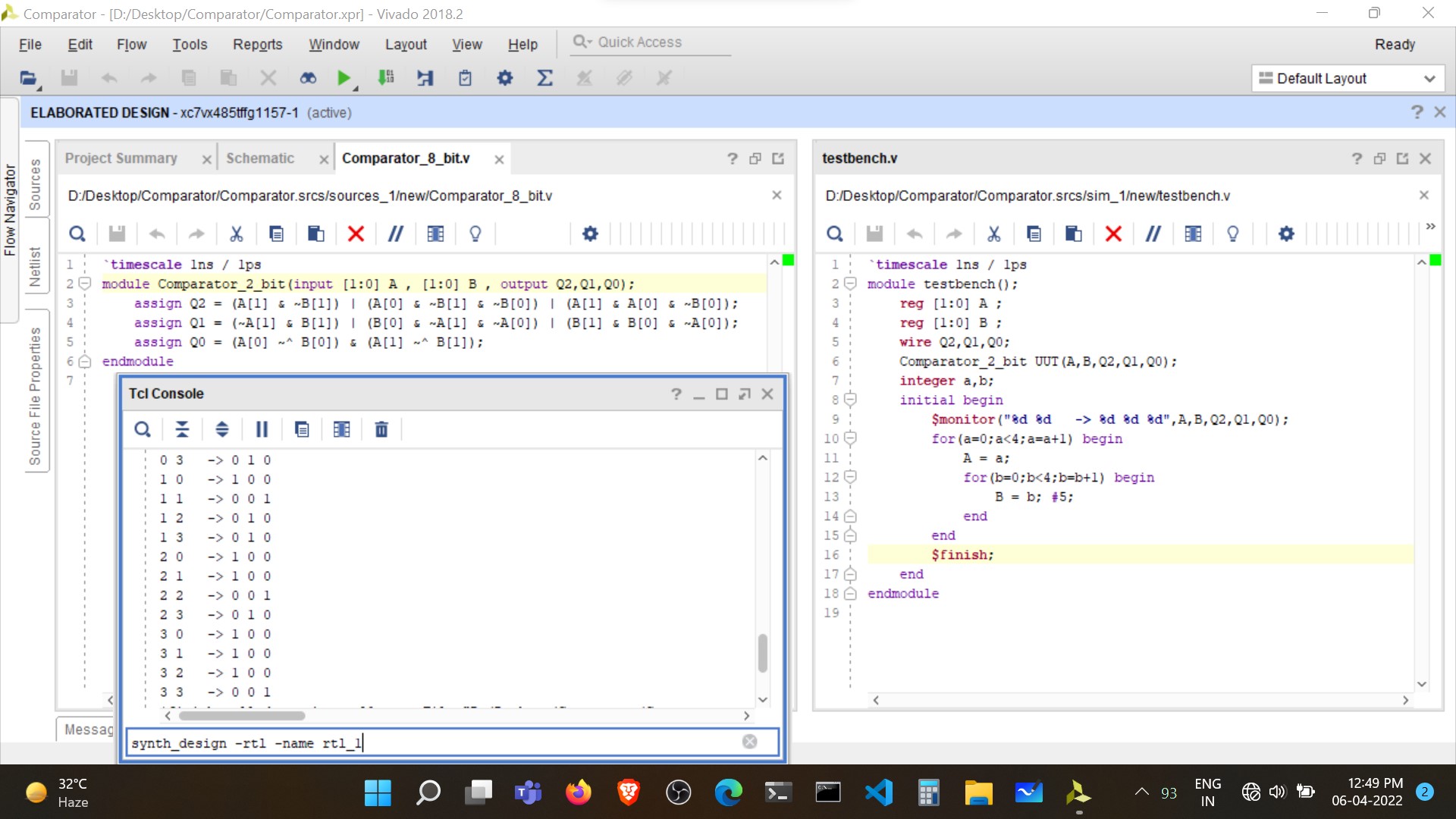
Simulation output of Binary to Gray Converter

* Gray to Binary Converter

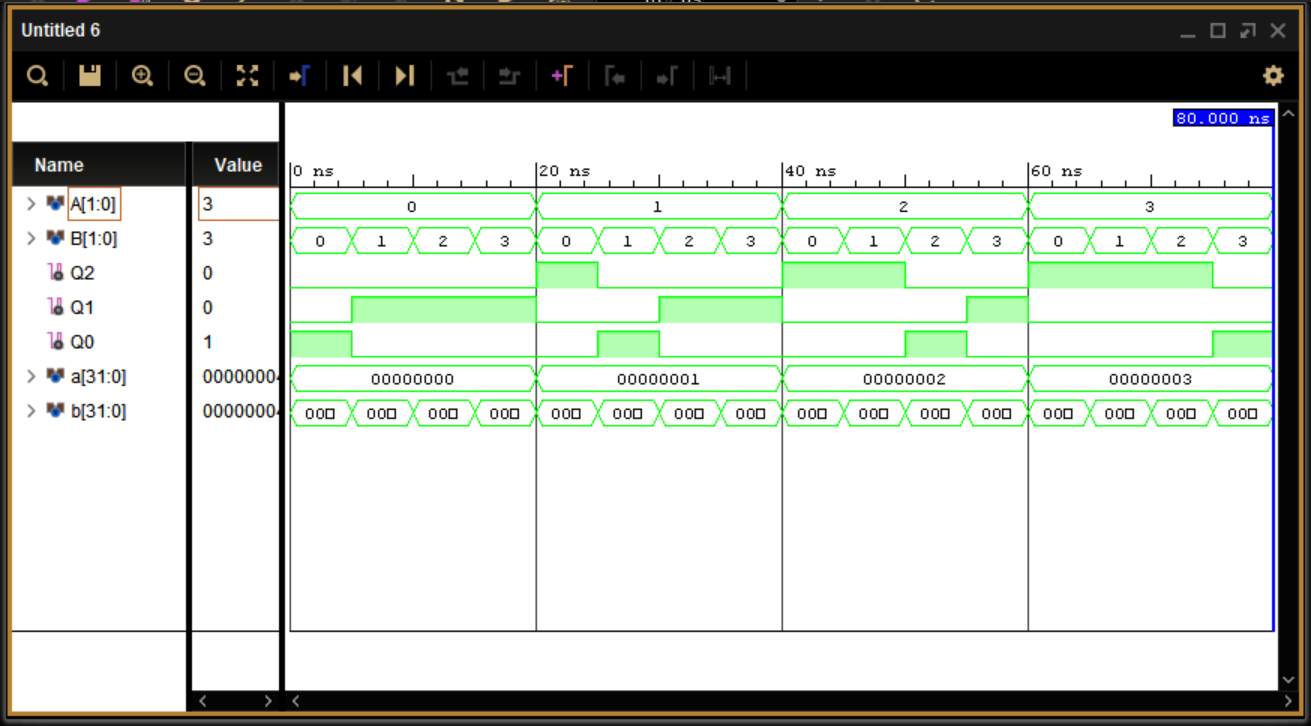
Verilog Code and Test bench for Gray to Binary Converter



Simulation output of Gray to Binary Converter

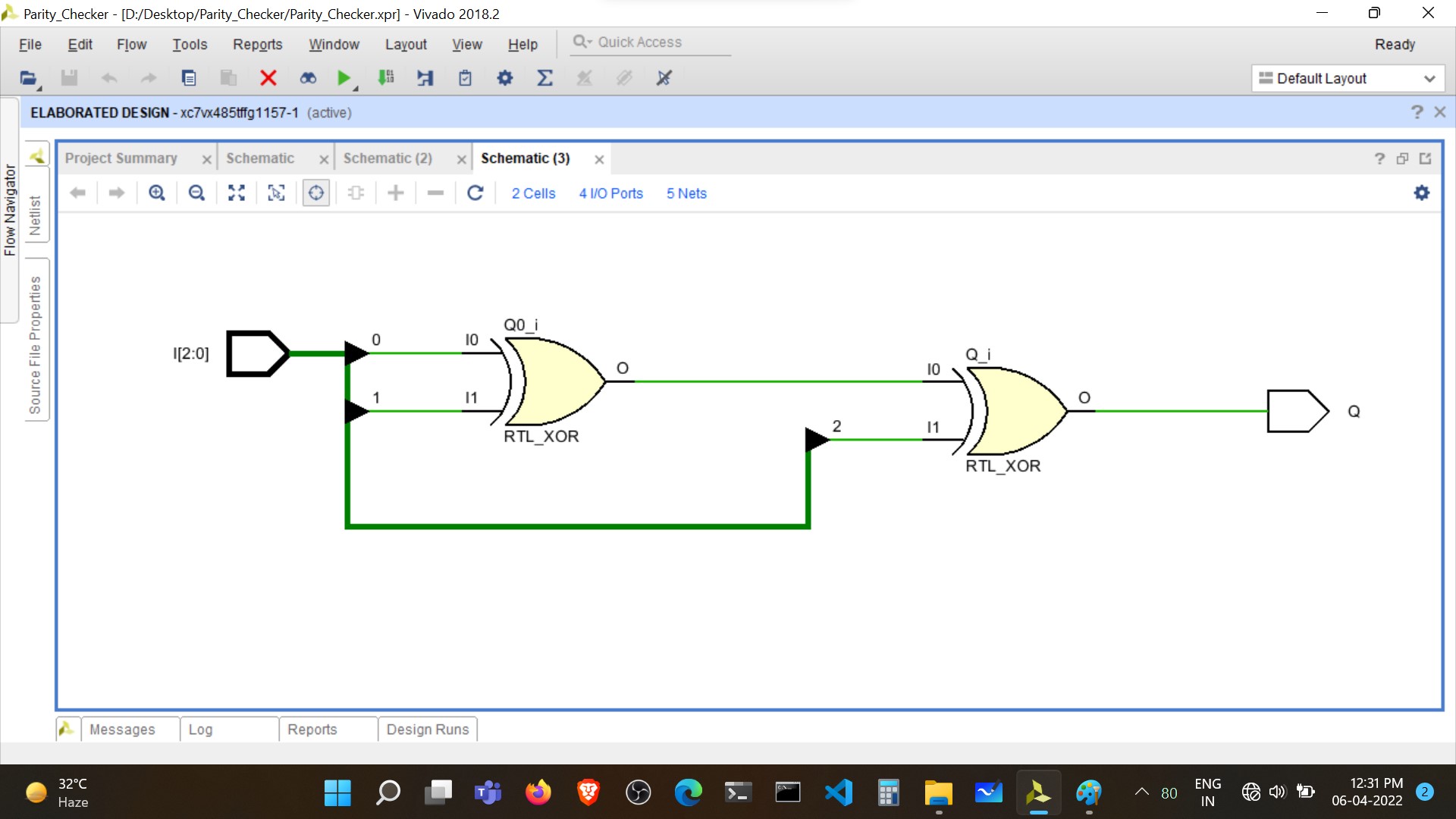
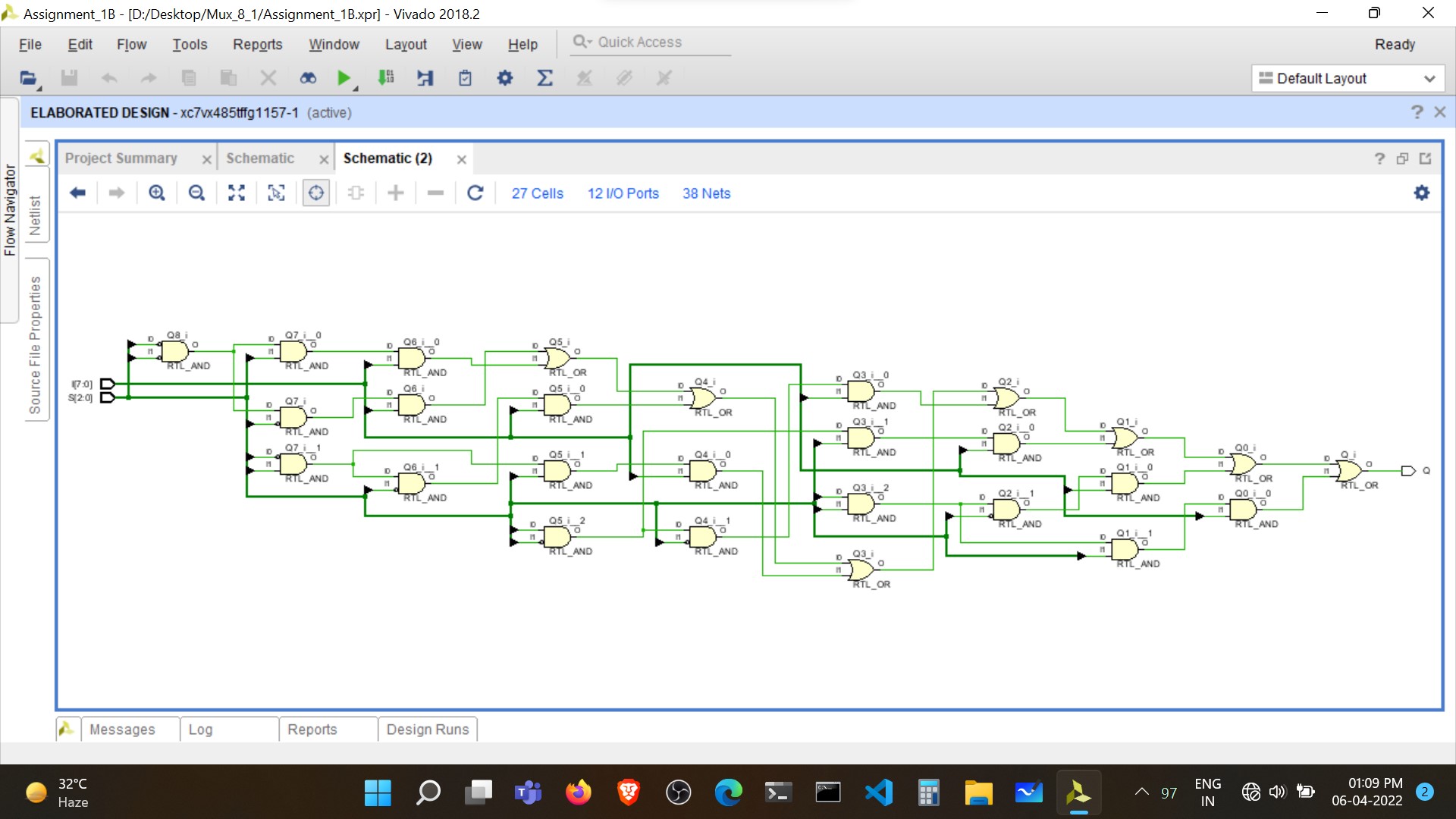
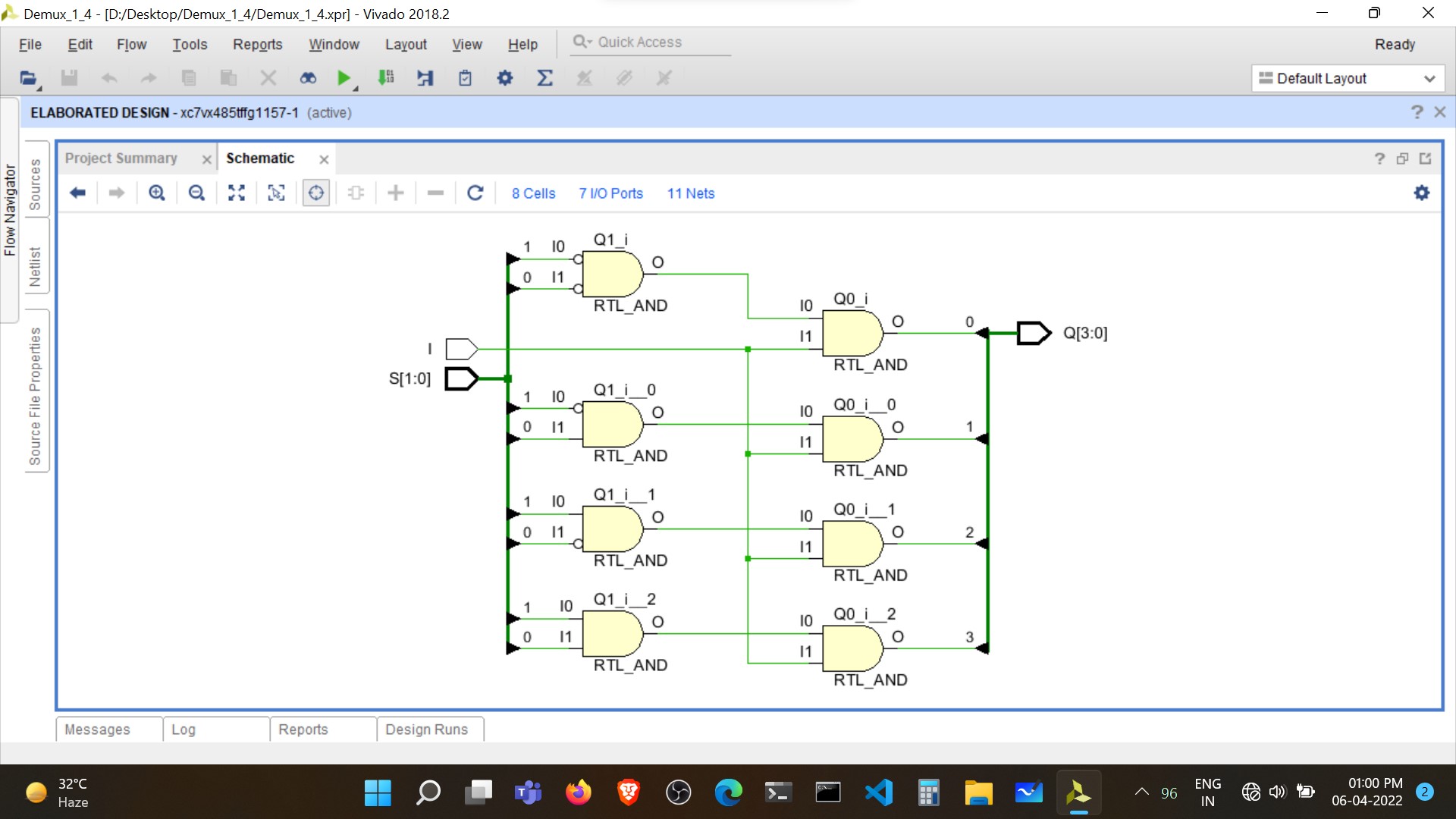
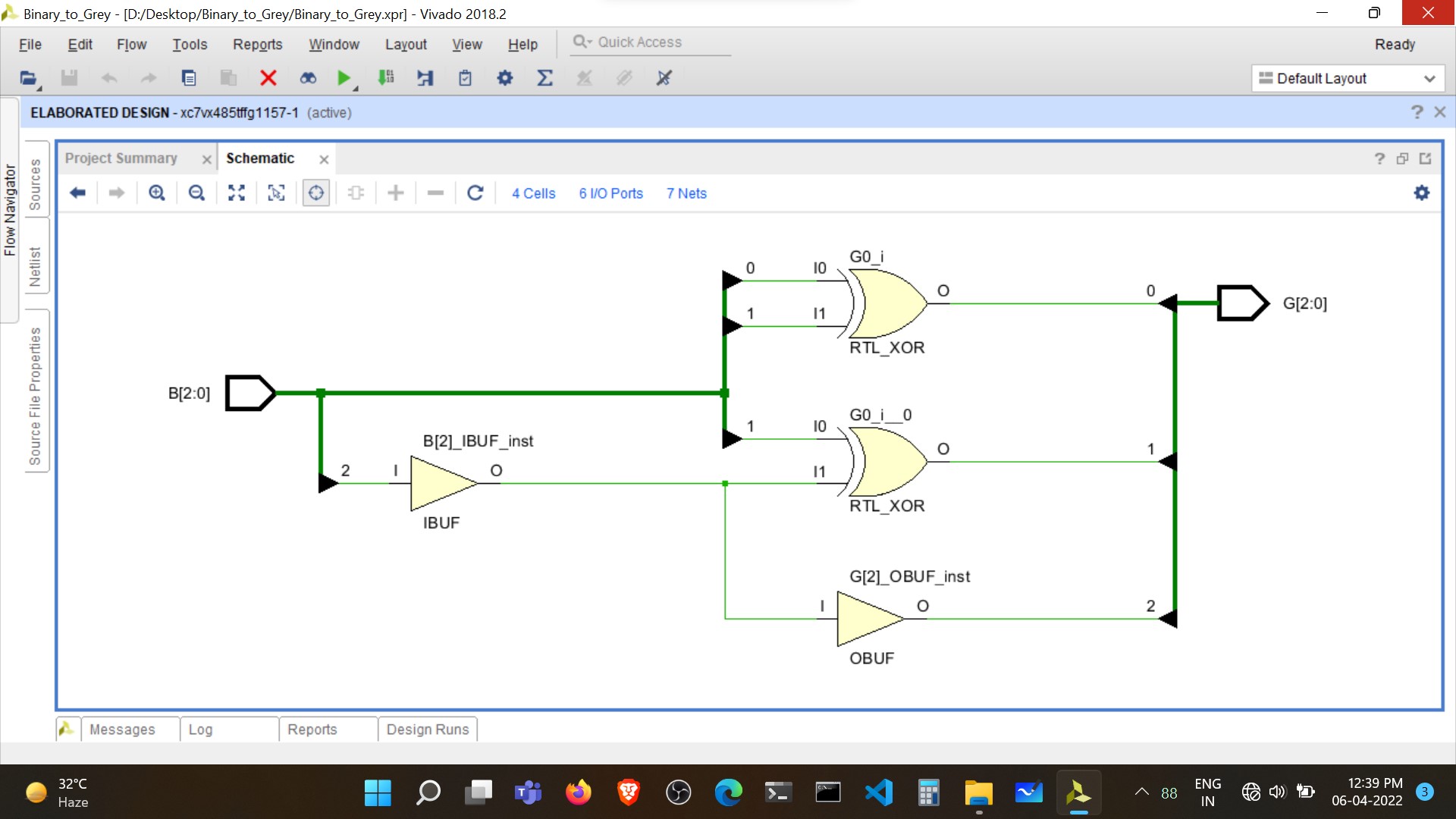
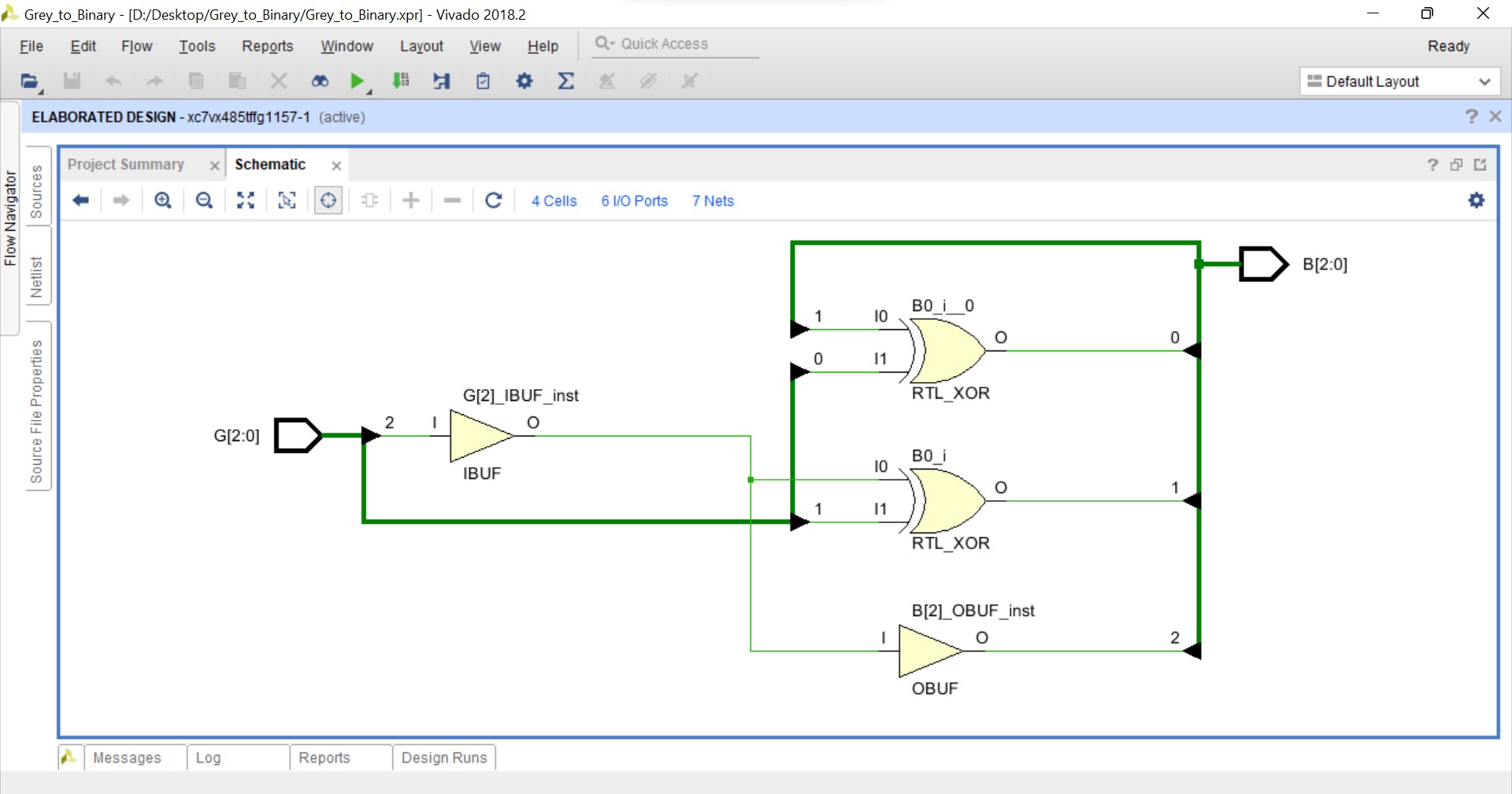
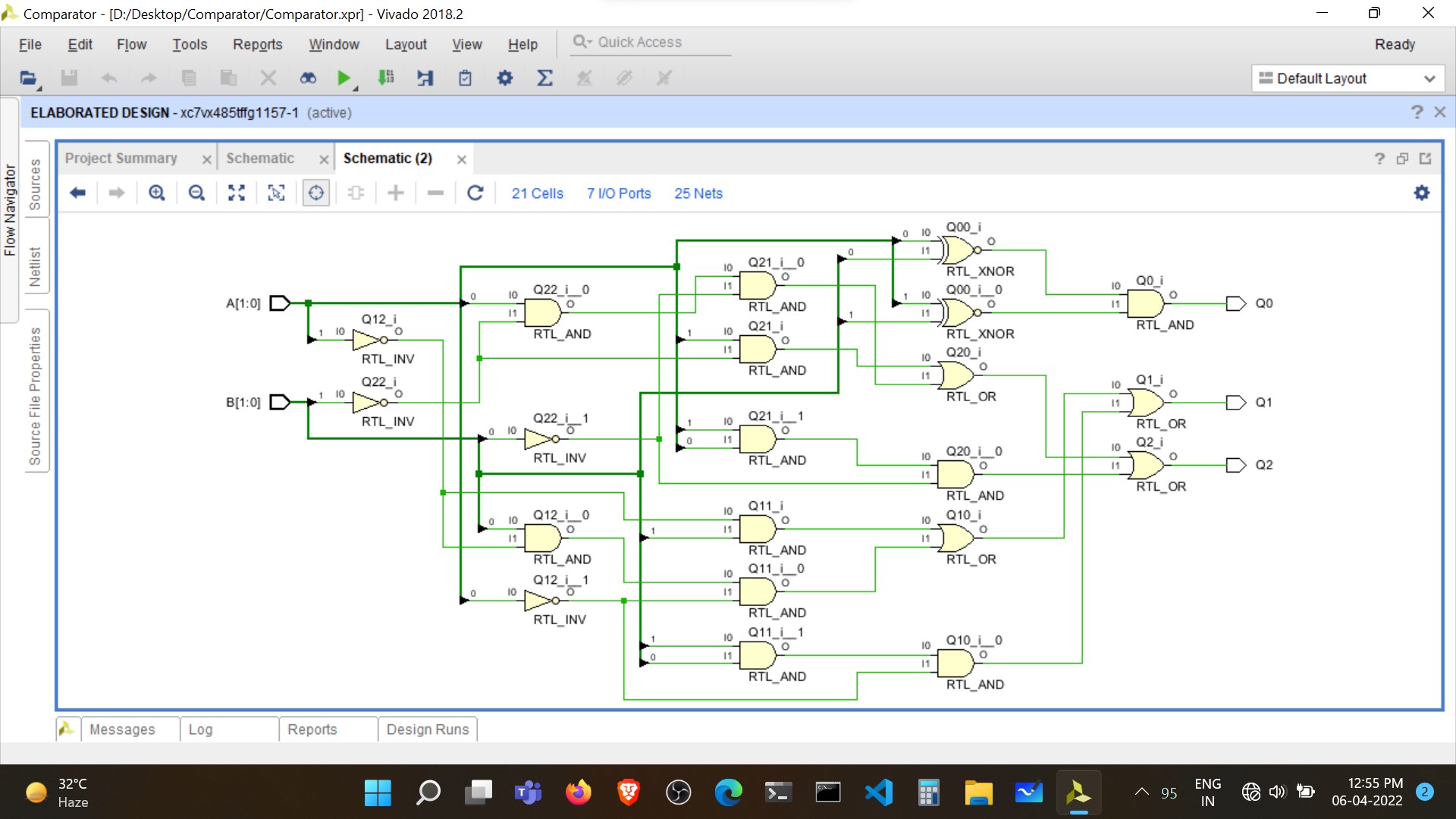
* 2-bit Magnitude Comparator

Verilog Code and Test bench for 2-bit magnitude Comparator



Simulation output of 2-bit magnitude Comparator

Observations:

* Parity Checker
* 8:1 Multiplexer
* 1:4 De-Multiplexer
* Binary to Gray Converter
* Gray to Binary Converter
* 2-bit Magnitude Comparator