**AUTUMN MID SEMESTER EXAMINATION-2023**

**School of Computer Engineering**

**Kalinga Institute of Industrial Technology, Deemed to be University High Performance Computing (HPC)**

**[Subject code: CS-3010]**

**Time: 1 1/2 Hours** **Full Mark: 40**

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***Answer any four Questions including Q.No.1 which is Compulsory. The figures in the margin indicate full marks. Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.***

**Q1.** **[ 2 x 5=10 marks ]**

**A.** Consider two processors **P1** and **P2** executing the same same program. Assume that under identical conditions, for the same input, a program running on **P2** takes 40% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on **P1**. If the clock frequency of **P1** is 2GHZ, then calculate the clock frequency of P2.

**B.** Consider the cache memory which is 5 time faster than main memory and it can be used 85% of the total time then calculate the overall speedup gain by cache memory?

**C.** Represent the machine code for the MIPS instruction **SLT R10, R14, R16** in 12 bit binary. Assume the opcode value for SLT (set to 1 if less than) and Function code in hexadecimal is 0X00 and 0x2A respectively.

**D.** For the code sequence below, state whether it must stall, can avoid stalls using only forwarding, or can execute without stalling or forwarding ?Justify your answer?

**LW R1,8(R2)**
**ADD R2,R1,R1**

**E.** Consider a 5 stage pipeline processor operating with ideal CPI is 1clock cycle which allow all the instructions except the branch instructions. Processor stops the fetching of the following instructions after the branch instructions until the branch target address is available in the pipeline. In the pipeline, the branch target address is available when the instruction is completed (at last stage).Program contains 60% branch instructions among them 60% are conditional branch in which 60% does not satisfy the condition. When the condition is false, then the following instructions are overlapped. Calculate the pipeline speedup?

**Q2.**

**A.** Briefly, Explain different MIPS instruction format (R type, I type, and J type) with examples from each type? **[5 marks]**

**B.** For a given computer system, following are the different type of instructions supported by machine. The number of clock cycle taken for each of load, store, ALU, branch and Jump instruction are 5, 4, 3, 3 and 2 clock cycle respectively. If a program has 40% ALU instructions,20% load instructions, 20% store instructions, 18% branch instructions and 2% Jump instructions. If the program has 5000 instructions and the speed of the computer is 3.25GHZ, calculate the overall CPI and time taken to execute the program. **[5 marks]**

**Q3.**

**A.** Distinguish between RISC and CISC? Briefly, explain the 7 dimensions of Instruction set architecture with suitable examples.

**[5 marks]**

**B.** Consider the following instructions sequence **[5 marks]**

**I1: LW R2, 0(R1)**
**I2: LW R1, 8(R3)**
**I3: SUB R3, R1, R2**
**I4: ADD R3, R2, R1**
**I5: ADDI R4, R3, 8**
**I5: SW R3,32(R1)**

Identify the Read after write hazard. Assume the 5-stage MIPS pipeline without forwarding and each stage takes 1 cycle. Instead of inserting nops, let the processor stall on hazards. How many times does the processor stall ? calculate the total number of clock cycle required to execute the above instructions without operand forwarding?

**Q4.**

**A.** What is branch hazard ?Discuss Delayed Branch resolution techniques for eliminating branch hazard **[5marks]**

**B.** Consider the following instructions:-

**LW R1, 8(R11)**
**ADD R1, R5, R1**
**SW R1, 8(R11)**
**LW R1, 16(R15)**
**BEQ R1, R12, Label**
**ADDI R1, R1, 8**
**OR R1, R12, R17**
**Label: SW R10, 16(R8)**
**SUBI R4, R4, 8**

Find out the independent instruction which can be scheduled into the delayed slot for branch taken. Draw time phase diagram to calculate the total number of clock cycle required to execute the above instructions with operand forwarding for the taken branch. Assume the value of R1 and R12 is 20 while executing **BEQ (Branch if Equal)** instruction and branch decision is done in decode stage in a 5 stage MIPS pipeline processor. **[5marks]**

**Q5.**

**A.** Explain static branch prediction and dynamic branch predictions schemes and provide details for each of them? **[5 marks]**

**B.** The outcome of a branch is **T, T, T, T, T, NT** and this pattern is repeated 4 times by an outer loop. Find out the no of miss and correct predictions using 2-bit predictor scheme. Assuming the initial state is strongly not taken (**NT**) and 2 bits counter value is $\mathbf{00}_2$. **[5 marks]**

*** Best of Luck ***