Qn. Set Code-1

Semester: 5th
Programme: B.Tech
Branch/Specialization: CSE

AUTUMN END SEMESTER EXAMINATION-2022

5th Semester B.Tech

HIGH PERFORMANCE COMPUTING

CS3010

(For 2021 (L.E), 2020 & Previous Admitted Batches)

Time: 3 Hours | Full Marks: 50

Answer any SIX questions.
Question paper consists of four SECTIONS i.e. A, B, C and D.
Section A is compulsory.
Attempt minimum one question each from Sections B, C, D.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

SECTION-A

1. Answer the following questions. [1 × 10]

(a) Find out the overall speed up in the below given scenario: 70% of the computation is not subjected to improvement, but rest of computation makes the portion affected twice as fast.

(b) What hardware implementation exists in MIPS to avoid structural hazard while referencing memory and register?

(c) Consider the execution of a program of 10000 instructions by a pipeline processor with a clock rate of 25MHz. Assume that the instruction pipeline has 5 stages and that one instruction is issued per clock cycle. What are the efficiency and throughput of this pipelined processor?

(d) Consider the following high level program where s is an integer array.

```
for(int i=0; i<10,i=i+2)
{
    s[i]=s[i]+5;
}
```

Write down the actual outcome of the branch instruction used. Find out the number of miss and correct predictions using 1-bit predictor where the initial state is NT.

(e) Differentiate between write allocate and no-write allocate policy.

(f) Consider a pipeline processor with Ideal CPI of 1.0. Assume that 40% are conditional instruction and 5 % are unconditional instruction present in the instruction mix of a benchmark program. It is found that the branch prediction accuracy of the pipeline is 50% and each misprediction causes 2 stall cycle delays in the pipeline. Find the depth of the pipeline in order to achieve a speedup gain of 6 times with respect to a non-pipelined processor.

(g) Explain two disadvantages of static scheduling.

(h) The scalar processor has 5 pipeline stages, Draw the time space diagram of both super scalar and super pipelined machine where super scalar processor having degree 2 executes a program of 6 instructions and the same program by a super pipelined having degree 3.

(i) Explain WAR and WAW hazard with suitable example.

(j) What is cache coherence problem in a multi processor?

SECTION-B

2. (a) A MIPS program consists of four instructions whose machine code in hexadecimal form is given below [4]

958000A
016D6020
018E7822
AE0F0000

Write down the corresponding assembly language MIPS instruction. The opcode of load, store, add and sub is 35, 43, 32 and 34 in integers. The mnemonics or short word for load, store, add and sub is LD, SD, DADD and DSUB respectively.

(b) Consider the following MIPS instructions:- [4]

```
LD      R1, 09(R10)
LD      R2,10(R9)
DADD    R3,R1,R2
SD      R3,08(R8)
LD      R4,11(R7)
J       4
SD      R5,12(R4)
OR      R6,R4,R5
```

Find out total number of clock cycles required to complete the execution without operand forwarding. And also find total no cycles required if operand forwarding is used.

3. (a) What are the techniques employed for scheduling the branch delayed slot? Explain with examples [4]

(b) Consider the following MIPS instructions: [4]

```
LD R1,0(R2)
LD R3,0(R4)
DADD R5,R3,R4
SD R5,0(R6)
LD R7,0(R8)
LD R9,0(R10)
DSUB R11,R7,R9
SD R11,0(R12)
```

Find out total number of clock cycles required to complete the execution if operand forwarding is used. And also find total no cycles required if rescheduling is used.

SECTION-C

4. (a) How register renaming is used to resolve WAW and WAR? Explain with suitable example for each hazard. [4]

(b) Assume we have a computer where the CPI is 1.0 when all memory accesses are hits. The only data references are loads and stores, and they are 40% of the program. There are 10 misses in 1000 instructions. If the miss penalty is 50 cycles, how much faster would the computer be if all instructions are cache hits and secondly also find if all instructions are misses. [4]

5. (a) Discuss the functionality of different stages while executing an instruction in Tomasulo's approach with a neat diagram. [4]

(b) Consider a memory system with 2-level cache organization, L1 cache has a hit-time of 1 cycle and L2 cache has a hit-time of 10 cycles and miss penalty of 200 cycles. In the context of 1000 memory references, 50 misses occurs in L1 and the global miss rate of L2 is 3%. assuming 1.5 memory references per instruction and ideal CPI of 1, compute average memory access time and average stall cycles per iinstruction. [4]

6. (a) How miss penalty is reduced by giving priority to read misses over writes? Explain with suitable example. [4]

(b) Consider the following MIPS instructions [4]

```
Loop : L.D F0,0(R1)
       L.D F1,0(R2)
       ADD.D F3,F1,F2
       S.D F3,0(R3)
       DADDUI R1,R1,#-8
       DADDUI R2,R2,#-8
       DADDUI R3,R3,#-8
       BNE R1,R4,Loop
```

The latency between dependent instructions (1 cycle for L.D and ADD.D, 2 cycles for ADD.D and S.D) exists. Suppose a VLIW that could issue two memory operations, two FP operations and one Integer operations in every clock cycle. Unroll the loop 7 times, find out the number of cycles issued per iteration.

SECTION-D

7. (a) Explain the Snoopy Protocol. How coherence problem is handled on a Write-Back Cache using Invalidation Protocol. Explain with State Machine diagram considering both CPU requests for each Cache Block and Bus requests for each Cache Block. [4]

   (b) A processor is connected with a memory having size 1K x word and the cache having 32 blocks. The main memory block has 8 words. Find out the following first for direct mapped and secondly for 4-way set associative cache [4]
   1. Address lay out used by cache
   2. Size of cache
   3. How many memory blocks has same cache block / set positions

8. (a) Two applications are run on a computer with two processors. First application is utilizing 80% of the resources and the second application needs 20% of the resources. Given that 70% of the first application is parallelizable, how much speed-up would be achieved if this application is run in isolation? How much overall system speed-up would be achieved if 70% of the first application is parallelizable but second application is not parallelizable. [4]

   (b) Discuss the different types of multi processors with neat diagram. [4]

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