Qn. Set Code-1

Semester: 5th
Programme: B.Tech
Branch/Specialization: CSE

AUTUMN END SEMESTER EXAMINATION-2023

5th Semester B.Tech

HIGH PERFORMANCE COMPUTING

CS 3010

(For 2022 (L.E), 2021 & Previous Admitted Batches)

Time: 3 Hours Full Marks: 50

Answer any SIX questions.
Question paper consists of four SECTIONS i.e. A, B, C and D.
Section A is compulsory.
Attempt minimum one question each from Sections B, C, D.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

SECTION-A

1. Answer the following questions. [1 × 10]

(a) Consider your travel trip from a place A to place B that goes through mountains and desert. On the mountain, you must walk and it will take 20 hours. But the last 200 kilometers in the desert, you can either walk or drive a car. The distances covered by walk and car is 4 kilometers per hour and 50 kilometers per hour respectively. Find out the speed up in the desert with respect to walk and overall speed up gained using car.

(b) Figure out any two features of MIPS instruction set that fulfills RISC characteristics.

(c) The MIPS processor having operand forwarding facilities executes following ALU type instructions whose machine codes in hex are given below

0C01000F

0041180F

The function field of one instruction is 0x0F that performs multiplication and the opcode field of other is 0x03 that performs addition with immediate data. Find the destination registers and their content.

(d) Consider the following MIPS instructions executing in program order

I1 DADD R2,R2,R3

I2 LD R3,0(R4)

I3 SD R3,0(R5)

I4 DMUL R2,R6,R7

Identify anti and output dependencies that exists among the instructions.

(e) Find the percentage of accuracy using 2-bit prediction scheme where the actual outcomes of a branch instruction is T,NT,T,NT,T,NT and the initial state is NT(strongly not taken).

(f) What is the importance of dirty bit in write back cache?

(g) A memory system has a cache, main and virtual memory. If the hit rate of cache is 70% and the hit rate of main memory is 75%. Find out average memory access time, if it takes 5 cycles to access cache memory, 10 cycles to access main memory and 50 cycles to access virtual memory?

(h) Explain Compulsory, Capacity and Conflict misses in Cache.

(i) Differentiate between super scalar and super pipelined processor.

(j) What is Cache Coherence in multi processor system?

SECTION-B

2. (a) Derive the expression for pipeline speed up, throughput and efficiency. [4]

(b) Consider the following MIPS instructions:- [4]

```
LD R1,10(R10)
OR R9,R1,R2
LD R5,30(R6)
MUL R3,R5,R4
DADD R6,R1,R5
DIV R7,R3,R6
SD R7,16(R3)
```

Find out total number of clock cycles required to complete the execution for the above sequence without operand and also with operand forwarding.

3. (a) Consider a program consists of 50 ALU, 30 LOAD and 20 STORE instructions. ALU, LOAD and STORE take 1, 4 and 4 cycles each. Find out CPI. The clock frequency has been incremented by 25% and this implies a CPI increment of ALU instructions of 50% and LOAD instructions of 25% while the remaining instructions are executed with the same CPI. Find out the new CPI. [4]

(b) How branch hazard is resolved with flushing, branch untaken and branch taken techniques? Explain with suitable time space diagram. [4]

SECTION-C

4. (a) Consider the following MIPS instructions [4]

```
Loop :  L.D F0,0(R1)
        L.D F2.0(R2)
        ADD.D F4,F0,F2
        S.D  F4, 0(R3)
```

DADDUI R1,R1,#-8

DADDUI R2,R2,#-8

DADDUI R3,R3,#-8

BNE R1,R4,Loop

The latency between L.D and ADD.D instructions is 2 cycles and same with ADD.D and S.D. Unroll the loop 2 times, find out the cycles issued per iteration. Reschedule the unrolled code and also find out the no of cycles issued per iteration.

(b) Differentiate between static and dynamic scheduling. How register renaming is used to resolve WAW and WAR hazard? Explain with example. [4]

5. (a) Consider a multilevel cache organization, where there are 50 misses from 1000 memory references in the first-level cache and 25 misses in the second-level cache. Assume that miss penalty from the L2 cache to memory is 200 clock cycles, the hit time of the L2 cache is 20 clock cycles, the hit time of LI is 1 clock cycle, and there are 1.5 memory references per instruction. Find out the Local and Global Miss Rates? What is the Average Memory Access Time and Average Stall Cycles per Instruction? Ignore the impact of Writes. [4]

(b) Explain the function of Instruction queue, reservation station, load and store buffer, functional units, address unit, CDB and FP Registers in Tomasualo structure with neat diagram. [4]

6. (a) A four-way Set Associative Cache consists of 128 blocks with a block size of 64 memory words. In the main memory the CPU generates a 20-bit address of a memory word. What are the number of bits in the TAG, SET and WORD field respectively? [4]

How is a memory block found if it is in the cache? Explain with help of the above specifications.

(b) Explain two methods used for reducing the Cache Miss Penalty [4]

SECTION-D

7. (a) Consider the following instructions [4]

L.D	F6,34(R2)
L.D	F2,45(R3)
MUL.D	F0,F2,F4
SUB.D	F8,F6,F2
DIV.D	F10,F0,F6
ADD.D	F6,F8,F2

There are 1 integer, 2 multipliers, 1 divider, 1 adder units available. The scenario is

1.Two loads and SUB have finished write register stage.

2.MUL and ADD have finished read operands stage.

3.DIV has issued.

Using scoreboard technique, find out instruction status, functional unit status and write register status.

(b) Differentiate between tightly and loosly coupled multiprocessors. Discuss UMA,NUMA and COMA with neat diagram. [4]

8. (a) Explain the Snoopy Protocol. How coherence problem is handled on a Write-Back Cache using Invalidation Protocol. Explain with State Machine diagram considering both CPU requests for each Cache Block and Bus requests for each Cache Block. [4]

(b) Assume you have a computer having CPI=1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores, and these total 40% of the instructions. If the miss penalty is 20 clock cycles and the total no of misses in 1000 instructions is 25,how much faster would the computer be if all instructions were cache hits? Also find out the times CPI is increased if there is no cache. [4]

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