pr5 - Pipelined Processor with Forwarding Simulator

1 Lab Assignment 5

In this lab, you will simulate a pipelined RISC-V processor which supports forwarding and resolves the target PC (in the case of control-flow modifying instructions) by the end of the decode stage where possible. Follow the instructions given below to achieve the same.

Instructions

1. Extend the command-line switch `proc` to accept a third value `FPipelinedProcessor` (in addition to the earlier to values). You will have to continue to instantiate the appropriate processor depending on the command-line switch passed.
2. Implement all the forwarding mechanisms.
3. Modify the code in such a way that the target PC is resolved in the decode stage itself. Note that there should be only one wrong-path instruction when control-flow modifying instructions are encountered.
4. Rest of the code should be unchanged such as the earlier statistics on number of instructions and number of clock cycles should continue to be written to `stats.out`.
5. Push your changes to the `'main'` branch at regular intervals.