pr5 - Single Cycle Processor Simulator

1 Lab Assignment 3 (Graded)

In this lab, you will be given a simulator which simulates a single cycle RISC-V processor. You are required to go through the code and make the appropriate modifications to it (as indicated by the `TODO` tags placed in the code). You can ignore the `FIXME` tags in the code, and pay attention to the `NOTE` tags.

Instructions

1. Merge the code from the `'lab3'` branch of your respective git repositories into the `'main'` branch. Please note that we will evaluate only the changes that you push to the `'main'` branch.
2. The `check_sequence.sh` script in the `pr5/tests/` folder is merely a sanity check. We will run several other checks (against various other assembly programs) for final evaluation.
3. THE CODE GIVEN TO YOU COULD HAVE OTHER ERRORs or BUGs in it. Some of these errors could be due to differing versions of Python. Some of these errors/bugs could be due to oversight (or intentional traps laid down) by the Instructor. These errors/bugs may not be triggered by the `check_sequence.sh`. However, these errors may trouble you in the future labs. Hence, fix the errors as you spot them. Write more test cases if required. Remember, you are responsible for your submission (including the correctness of parts of code that the Instructor gave you).
4. Push your changes to the `'main'` branch at regular intervals.