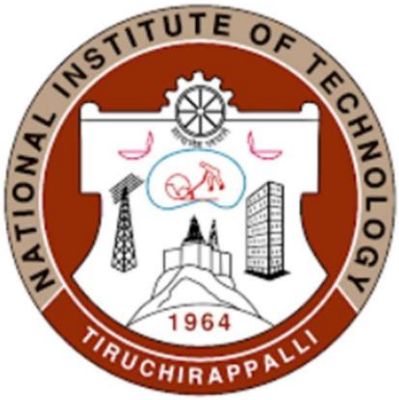
Department of Electronics and Communication Engineering

National Institute of Technology, Tiruchirappalli - 620015



ECLR11

DIGITAL ELECTRONICS LABORATORY

Mini Project

Faculty: Dr. R. Malmathanraj

Mini Project title: 4 Bit Cyber Lock (Simulation)

Section: ECE-A.

Prepared by:

Righas P (108122089)

Sayan Bose (108122101)

Shriram J (108122109)

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4 Bit Cyber Lock (Simulation)

Objective:

To design a circuit that determines the 4-bit password of a system, using an optimized Linear Search Algorithm.

Abstract:

The 4-Bit cyber lock is a digital circuit which can also be considered as a Password Detector. Our project aims at presenting a small model of how an actual password hacking system would look like.

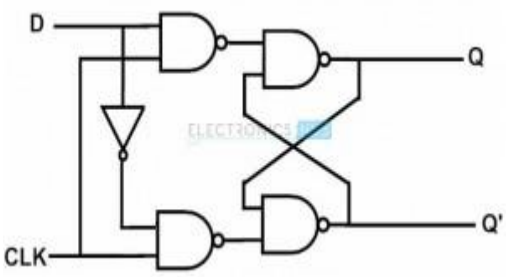
There are many instances in real life, where Police need an efficient password hacking system which they can use in cracking a password combination in order to decrypt a file or document. The given simulation model presents a small demo of how the password hacking system works. Even though our project uses only a 4 Bit password, the system can be conveniently expanded to work for higher order bits as well, without fail.

Components Required:

Sr. No	Name	Specifications	Quantity
1	D Flip Flop	IC 7474	4
2	Quad 2 input AND Gate	IC 7408	2
3	Quad 3 input AND Gate	IC 7411	2
4	Quad 2 Input OR Gate	IC 7432	1
5	Quad 3 Input OR Gate	IC 744075	1

6	Logic State Selectors	-	4
7	LEDs		2
8	4 Bit Magnitude Comparator	IC 7485	1
9	JK Flip Flop	IC 7476	5
10	Logic Probes	-	4
11	Connecting Wires	-	As Required

1. **D Flip Flop (IC 7474)**
   D flip-flop, also known as a data flip-flop or delay flip-flop, is a sequential digital logic circuit that has one data input (D), one clock input (CLK), and one output (Q). The output Q simply follows the input D on the rising edge of the clock CLK. In other words, the D flip-flop stores the value of the data input D until the next rising edge of the clock, at which point it transfers the value of D to the output Q.



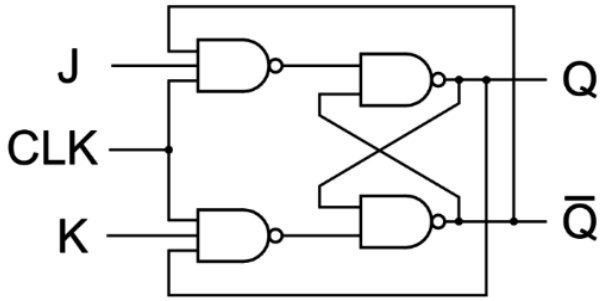
1. **Quad 2/3 input AND Gate (IC 7408/ IC 7411)**
   An AND gate is a basic digital logic gate that implements logical conjunction (∧) from mathematical logic. It has multiple inputs and one output. The output is HIGH only if all inputs are HIGH. Otherwise, the output is LOW.

2. **Quad 2/3 input AND Gate (IC 7432/ IC 744075)**
   An AND gate is a basic digital logic gate that implements logical conjunction (∧) from mathematical logic. It has multiple inputs and one

output. The output is HIGH only if all inputs are HIGH. Otherwise, the output is LOW.

3. **JK Flip Flop (IC 7485)**

JK flip-flop, also known as a J-K flip-flop or toggle flip-flop, is a type of sequential logic circuit that has two data inputs (J and K), one clock input (CLK), and one output (Q).



4. **4-Bit Magnitude Comparator (IC 7485)**

A 4-bit magnitude comparator is a combinational circuit that compares two 4-bit binary numbers and determines their relative magnitudes. It has two sets of 4-bit inputs, A and B, and three outputs:

- Greater than (>): This output is high if A is greater than B, and low otherwise.
- Equal to (=): This output is high if A is equal to B, and low otherwise.
- Less than (<): This output is high if A is less than B, and low otherwise.

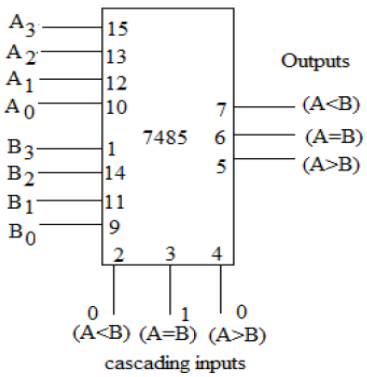


Fig. 2: 4-bit Comparator

Theory:

The 4-Bit Password Detector is made using a 4-Bit comparator, D flip flops, JK flip flops, T flip flops and different set of logic gates like ‘AND’ and ‘OR’.

The most efficient Searching algorithm, Binary Search cannot be applied at any point since we won’t know whether the password we are trying is greater or lesser than the correct password, we will only know if it is correct or not. Hence, the other Searching Algorithm left is Linear Search.

Linear Search Algorithm can also be done using mod-16 counters which produces a sequence from 0000 to 1111, but an Asynchronous counter has a delay and for higher bit sequence, the delay may even cause it to skip a pattern and if we use Synchronous counter, we require more logic gates which increases the cost as the number of bits’ increase.

In this circuit, we achieve Linear Search by using a special 19-bit sequence which when traversed with a window of size 4 will yield all the possible 4-bit sequences. This waveform is passed serially to a Serial In – Parallel out Shift register which compares using a Magnitude Comparator. As soon as the right password combination is found, the clock is terminated, and the password is stored, for future use.

Circuit Explanation and working:

The circuit mainly consists of two parts:

1. Waveform Generator
2. Password Detector

1. **Waveform Generator**
   The special 19-bit sequence is: 0000111100101101000. This sequence can be fed as input using a function generator, the absence of which, a T flip flop and a counter are used to generate the sequence. We may convert a JK flip flop to a T flip flop by providing J=K.

The places at which the sequence change from 0 to 1 or 1 to 0, i.e. toggles are noted. When the counter equals to these place values, the T flip flop must be given HIGH, else it must be LOW.

Writing the excitation table and simplifying it using K-Map, we get the combinational circuit that must be given to the T flip flop. The output of the T flip flop produces the required sequence which is passed serially to the shift register.

The 19 Bit Sequence is:

0	0	0	0	1	1	1	1	0	0	1	0	1	1	0	1	0	0	0

Consider the Window size to be 4 Bits.
Now we create a new sequence to track the number of toggles.

0	0	0	0	1	1	1	1	0	0	1	0	1	1	0	1	0	0	0
New Sequence	1	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0		

The 1's denote the states where bit toggling took place and 0's denote the states where no toggling took place.

Q3 Q2 \ Q1 Q0	0 0	0 1	1 1	1 0
0 0	**1**			
0 1	**1**		**1**	**1**
1 1	**1**			
1 0	**1**		**1**	**1**

The final expression is:

$$T = Q1' Q0' + Q1 Q2 Q3' + Q1 Q2' Q3$$

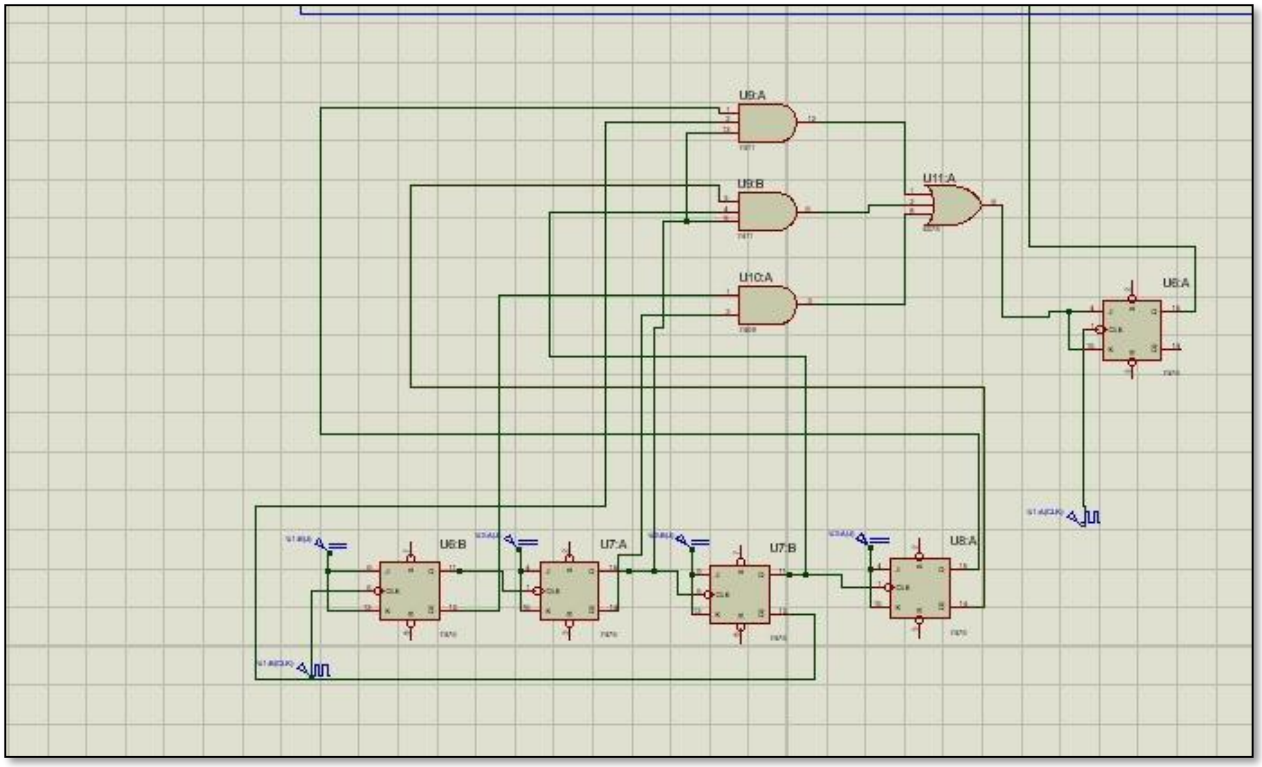
2. **Password Detector**

   This is the primary circuit, which is responsible for tallying each of the 4-Bit combinations with the predefined password in the system, using a 4-Bit magnitude comparator. The speed of the entire circuit is decided by the clock frequency given to the flip flops.

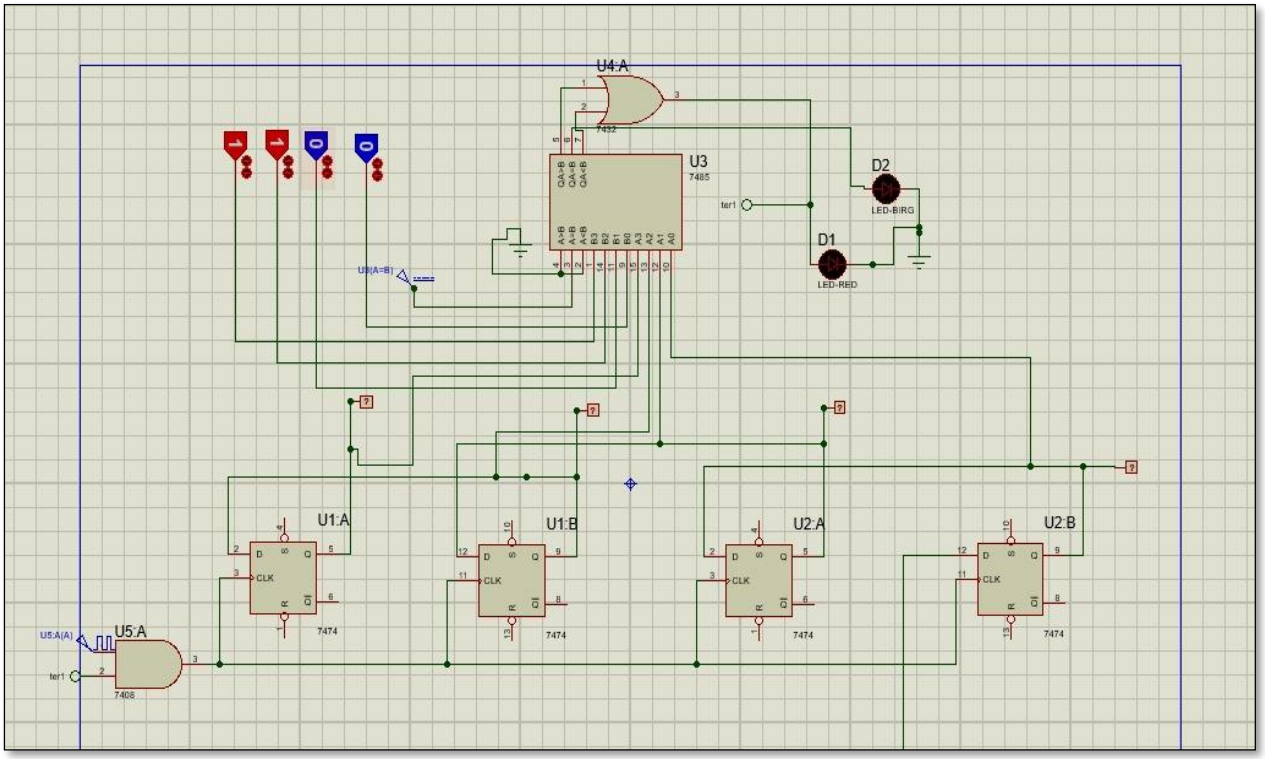
   It uses SIPO shift register having a synchronous clock input. The output of the T flip flop is fed to the input of the SIPO shift register. The inputs are then shifted to each of the cascaded flip flops on every clock pulse. The initial stage of the shift register is 0000, and then it starts displaying the different input combinations. Each of the output of the flip flops is given to the magnitude comparator which then compares each bit with the predefined password of the system. As soon as the pattern matches the A=B terminal goes high and the green LED glows which shows the correct password is detected, until then the red LED glows.

   To store the password once it is detected, the clock generated and the output of Red LED are given to an 'AND' gate which serves as the clock for the shift register. Once the sequence is matched, red LED goes to 0 and the clock to each shift register is 0 and the password is stored on the Shift Registers.

1. **Waveform Generator:**



2. Password Detector:



Conclusion:

From the project, we designed and implemented a 4-Bit cyber lock which helps in the detection of the correct password in an efficient and optimized manner.

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