VLSI Design Lab

Experiment 1 Fibonacci Generator

- **Objective**:
  1. To become familier with hierarchical design in Verilog
  2. To implement a simple Fibonacci Generator shown in Fig.1 in Verilog and verify the design

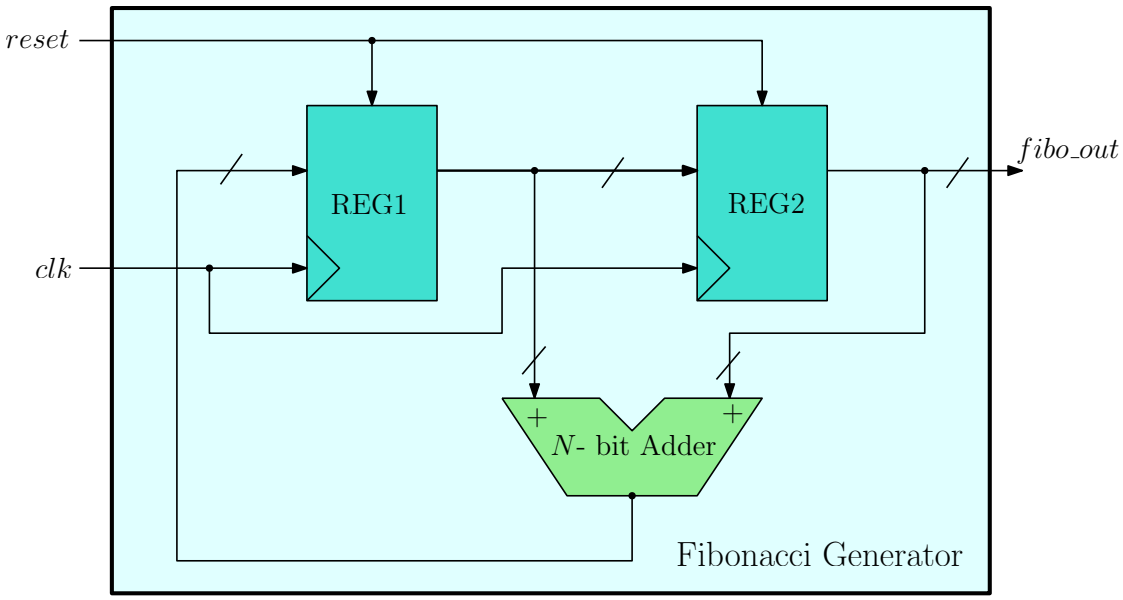

Figure 1: Fibonacci Series Generator Architecture.

- **Experimental procedure**

  1. Design a N-bit Fibonacci generator with both asynchronous reset and synchronous reset in Verilog using an adder and two registers where N is the parameter. You can use simple assign statement to implement the adder
  2. Modify the design by using hierarchy to implement the N-bit adder. Basically you need to design a separate N-bit adder module using ripple carry structure with N full adders and instantiate the N-bit adder in the top level module fibo gen.
  3. Modify the design further by using a separate N-bit register module and instantiating it in the fibo gen. Always follow "connect by name" methodology for hierarchy.
  4. Finally, develop a complete hierarchical structure with a simple full adder and D flip flop as leaf level modules, connecting N full adders in N-bit adder, N flip flops in a N-bit register, connecting 2 N-bit registers and N-bit adder in the top level module fibo gen.
  5. Develop a simple test bench for verifying the DUT.