Ex: 5.1

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{34.5 \text{ pF/m}}{4 \text{ nm}} = 8.625 \text{ fF}/\mu\text{m}^2$$

$\mu_n = 450 \text{ cm}^2/\text{V} \cdot \text{S}$

$k_n' = \mu_n C_{ox} = 388\ \mu\text{A/V}^2$

$V_{OV} = (v_{GS} - V_t) = 0.5 \text{ V}$

$$g_{DS} = \frac{1}{1 \text{ k}\Omega} = k_n' \frac{W}{L} V_{OV} \Rightarrow \frac{W}{L} = 5.15$$

$L = 0.18\ \mu\text{m}$, so $W = 0.93\ \mu\text{m}$

Ex: 5.2 $C_{ox} = \dfrac{\epsilon_{ox}}{t_{ox}} = \dfrac{34.5 \text{ pF/m}}{4 \text{ nm}} = 8.6 \text{ fF}/\mu\text{m}^2$

$\mu_n = 450 \text{ cm}^2/\text{V} \cdot \text{s}$

$k_n' = \mu_n C_{ox} = 387\ \mu\text{A/V}^2$

$$I_D = \frac{1}{2} k_n' \frac{W}{L} V_{OV}^2 = 0.3 \text{ mA}, \quad \frac{W}{L} = 20$$

$\therefore\ V_{OV} = 0.28 \text{ V}$

$V_{DS,\text{ min}} = V_{OV} = 0.28$ V, for saturation

Ex: 5.3 $I_D = \dfrac{1}{2} k_n' \dfrac{W}{L} V_{OV}^2$ in saturation

Change in I_D is:

(a) double L, 0.5

(b) double W, 2

(c) double V_{OV}, $2^2 = 4$

(d) double V_{DS}, no change (ignoring length modulation)

(e) changes (a)–(d), 4

Case (c) would cause leaving saturation if

$V_{DS} < 2V_{OV}$

Ex: 5.4 For saturation $v_{DS} \geq V_{OV}$, so V_{DS} must be changed to $2V_{OV}$

$I_D = \dfrac{1}{2} k_n' \dfrac{W}{L} V_{OV}^2$, so I_D increases by a factor of 4.

Ex: 5.5 $V_{OV} = 0.5$ V

$$g_{DS} = k_n' \frac{W}{L} V_{OV} = \frac{1}{1 \text{ k}\Omega}$$

$$\therefore k_n = k_n' \frac{W}{L} = \frac{1}{1 \times 0.5} = 2 \text{ mA/V}^2$$

For $v_{DS} = 0.5 \text{ V} = V_{OV}$, the transistor operates in saturation, and

$$I_D = \frac{1}{2} k_n' \frac{W}{L} V_{OV}^2 = 0.25 \text{ mA}$$

Similarly, $V_{DS} = 1$ V results in saturation-mode operation and $I_D = 0.25$ mA.

Ex: 5.6 $V_A = V_A' L = 50 \times 0.8 = 40$ V

$$\lambda = \frac{1}{V_A} = 0.025 \text{ V}^{-1}$$

$V_{DS} = 1 \text{ V} > V_{OV} = 0.5 \text{ V}$

$\Rightarrow$ Saturation: $I_D = \dfrac{1}{2} k_n' \dfrac{W}{L} V_{OV}^2 (1 + \lambda V_{DS})$

$$I_D = \frac{1}{2} \times 200 \times \frac{16}{0.8} \times 0.5^2 (1 + 0.025 \times 1)$$

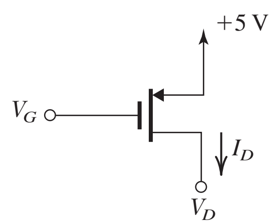
$= 0.51$ mA

$$r_o = \frac{V_A}{I_D} = \frac{40}{0.5} = 80 \text{ k}\Omega$$

where I_D is the value of I_D without channel-length modulation taken into account.

$$r_o = \frac{\Delta V_{DS}}{\Delta I_O} \Rightarrow \Delta I_O = \frac{2 \text{ V}}{80 \text{ k}\Omega} = 0.025 \text{ mA}$$

Ex: 5.7



$V_{tp} = -1$ V

$k_p' = 60\ \mu\text{A/V}^2$

$$\frac{W}{L} = 10 \Rightarrow k_p = 600\ \mu\text{A/V}^2$$

(a) Conduction occurs for $V_{SG} \geq |V_{tp}| = 1$ V

$\Rightarrow V_G \leq 5 - 1 = 4$ V

(b) Triode region occurs for $V_{DG} \geq |V_{tp}| = 1$ V

$\Rightarrow V_D \geq V_G + 1$

(c) Conversely, for saturation

$V_{DG} \leq |V_{tp}| = 1$ V

$\Rightarrow V_D \leq V_G + 1$

(d) Given $\lambda \cong 0$

$$I_D = \frac{1}{2} k_p' \frac{W}{L} |V_{OV}|^2 = 75\ \mu\text{A}$$

$\therefore |V_{OV}| = 0.5 \text{ V} = V_{SG} - |V_{tp}|$

$\Rightarrow V_{SG} = |V_{OV}| + |V_{tp}| = 1.5$ V

$V_G = 5 - |V_{SG}| = 3.5$ V

$V_D \leq V_G + 1 = 4.5$ V

(e) For $\lambda = -0.02\ \text{V}^{-1}$ and $|V_{OV}| = 0.5$ V,

$I_D = 75\ \mu\text{A}$ and $r_o = \dfrac{1}{|\lambda| I_D} = 667\ \text{k}\Omega$

(f) At $V_D = 3$ V, $V_{SD} = 2$ V

$$I_D = \frac{1}{2} k_n' \frac{W}{L} |V_{OV}|^2 (1 + |\lambda||V_{SD}|)$$

$= 75\ \mu\text{A}\ (1.04) = 78\ \mu\text{A}$

At $V_D = 0$ V, $V_{SD} = 5$ V

$I_D = 75\ \mu\text{A}\ (1.10) = 82.5\ \mu\text{A}$

$$r_o = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{3\ \text{V}}{4.5\ \mu\text{A}} = 667\ \text{k}\Omega$$

which is the same value found in (c).

Ex: 5.8

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} V_{OV}^2 \Rightarrow 0.3 = \frac{1}{2} \times \frac{60}{1000} \times \frac{120}{3} V_{OV}^2 \Rightarrow$$

$V_{OV} = 0.5\ \text{V} \Rightarrow V_{GS} = V_{OV} + V_t = 0.5 + 1$

$= 1.5$ V

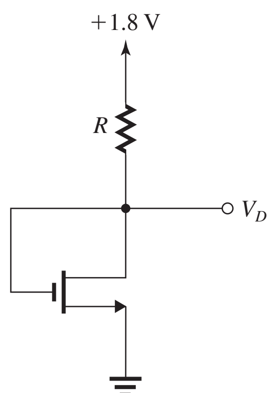
$$V_S = -1.5\ \text{V} \Rightarrow R_S = \frac{V_S - V_{SS}}{I_D}$$

$$= \frac{-1.5 - (-2.5)}{0.3}$$

$R_S = 3.33\ \text{k}\Omega$

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{2.5 - 0.4}{0.3} = 7\ \text{k}\Omega$$

Ex: 5.9



$V_{tn} = 0.5$ V

$\mu_n C_{ox} = 0.4\ \text{mA/V}^2$

$$\frac{W}{L} = \frac{0.72\ \mu\text{m}}{0.18\ \mu\text{m}} = 4.0$$

$\lambda = 0$

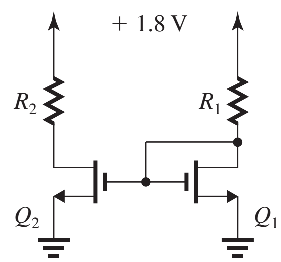
Saturation mode ($v_{GD} = 0 < V_{tn}$):

$V_D = 0.7\ \text{V} = 1.8 - I_D R_D$

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_D - V_{tn})^2 = 0.032\ \text{mA}$$

$$\therefore R = \frac{1.8 - 0.7}{0.032\ \text{mA}} = 34.4\ \text{k}\Omega$$

Ex: 5.10



Since Q_2 is identical to Q_1 and their V_{GS} values are the same,

$I_{D2} = I_{D1} = 0.032$ mA

For Q_2 to operate at the triode–saturation boundary, we must have

$V_{D2} = V_{OV} = 0.2$ V

$$\therefore R_2 = \frac{1.8\ \text{V} - 0.2\ \text{V}}{0.032\ \text{mA}} = 50\ \text{k}\Omega$$

Ex: 5.11 $R_D = 12.4 \times 2 = 24.8\ \text{k}\Omega$

$V_{GS} = 5$ V, assume triode region:

$$\left.\begin{array}{l} I_D = k_n' \dfrac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \dfrac{1}{2}V_{DS}^2\right] \\ I_D = \dfrac{V_{DD} - V_{DS}}{R} \end{array}\right\} \Rightarrow$$

$$\frac{5 - V_{DS}}{24.8} = 1 \times \left[(5 - 1)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$\Rightarrow V_{DS}^2 - 8.08 V_{DS} + 0.4 = 0$

$\Rightarrow V_{DS} = 0.05\ \text{V} < V_{OV} \Rightarrow$ triode region

$$I_D = \frac{5 - 0.05}{24.8} = 0.2\ \text{mA}$$

Ex: 5.12 As indicated in Example 5.6,

$V_D \geq V_G - V_t$ for the transistor to be in the saturation region.

$V_{D\text{min}} = V_G - V_t = 5 - 1 = 4$ V

$$I_D = 0.5\ \text{mA} \Rightarrow R_{D\text{max}} = \frac{V_{DD} - V_{D\text{min}}}{I_D}$$

$$= \frac{10 - 4}{0.5} = 12\ \text{k}\Omega$$

Ex: 5.13

$I_D = 0.32 \text{ mA} = \frac{1}{2}k_n' \frac{W}{L} V_{OV}^2 = \frac{1}{2} \times 1 \times V_{OV}^2$

$\Rightarrow V_{OV} = 0.8 \text{ V}$

$V_{GS} = 0.8 + 1 = 1.8 \text{ V}$

$V_G = V_S + V_{GS} = 1.6 + 1.8 = 3.4 \text{ V}$

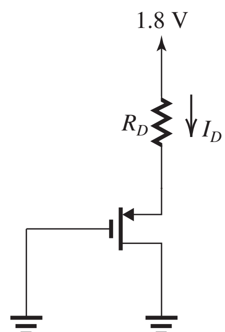
$R_{G2} = \frac{V_G}{I} = \frac{3.4}{1\ \mu\text{A}} = 3.4 \text{ M}\Omega$

$R_{G1} = \frac{5 - 3.4}{1\ \mu\text{A}} = 1.6 \text{ M}\Omega$

$R_S = \frac{V_S}{0.32} = 5 \text{ k}\Omega$

$V_D = 3.4 \text{ V}$, then $R_D = \frac{5 - 3.4}{0.32} = 5 \text{ k}\Omega$

Ex: 5.14



$V_{tp} = -0.4 \text{ V}$

$k_p' = 0.1 \text{ mA/V}^2$

$\frac{W}{L} = \frac{10\ \mu\text{m}}{0.18\ \mu\text{m}} \Rightarrow k_p = 5.56 \text{ mA/V}^2$

$V_{SG} = |V_{tp}| + |V_{OV}|$

$= 0.4 + 0.6 = 1 \text{ V}$

$V_S = +1 \text{ V}$

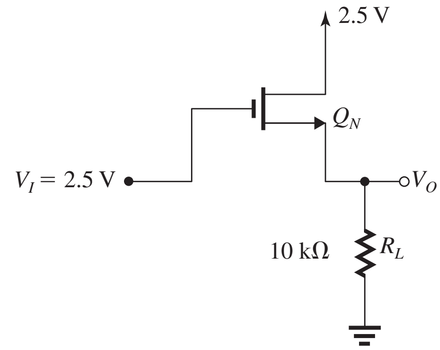
Since $V_{DG} = 0$, the transistor is operating in saturation, and

$I_D = \frac{1}{2}k_p' V_{OV}^2 = 1 \text{ mA}$

$\therefore\ R = \frac{1.8 - 1}{1} = 0.8 \text{ k}\Omega = 800\ \Omega$

Ex: 5.15 $v_I = 0$: since the circuit is perfectly symmetrical, $v_O = 0$ and therefore $V_{GS} = 0$, which implies that the transistors are turned off and $I_{DN} = I_{DP} = 0$.
$v_I = 2.5$ V: if we assume that the NMOS is turned on, then v_O would be less than 2.5 V, and this implies that PMOS is off $(V_{SGP} < 0)$.

$I_{DN} = \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_t)^2$



$I_{DN} = \frac{1}{2} \times 1(2.5 - V_O - 1)^2$

$I_{DN} = 0.5(1.5 - V_O)^2$

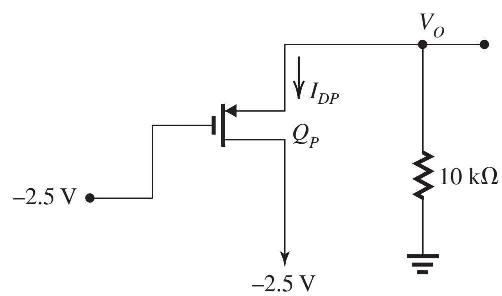
Also: $V_O = R_L I_{DN} = 10 I_{DN}$

$I_{DN} = 0.5(1.5 - 10 I_{DN})^2$

$\Rightarrow 100 I_{DN}^2 - 32 I_{DN} + 2.25 = 0 \Rightarrow I_{DN}$

$= 0.104 \text{ mA}$

$I_{DP} = 0,\ V_O = 10 \times 0.104 = 1.04\text{V}$



$V_I = -2.5$ V: Again if we assume that Q_p is turned on, then $V_O > -2.5$ V and $V_{GS1} < 0$, which implies that the NMOS Q_N is turned off.

$I_{DN} = 0$

Because of the symmetry,

$I_{DP} = 0.104,$

$V_O = -I_{DP} \times 10 \text{ k}\Omega$

$= -1.04 \text{ V}$

Ex: 5.16 $V_t = 0.8 + 0.4\left[\sqrt{0.7 + 3} - \sqrt{0.7}\right]$

$= 1.23 \text{ V}$

Ex: 5.17 $v_{DS\text{min}} = v_{GS} + |V_t|$

$= 1 + 2 = 3 \text{ V}$

$I_D = \frac{1}{2} \times 2\,[1 - (-2)]^2$

$= 9 \text{ mA}$

5.1 $t_{ox} = 2 \sim 10$ nm

$C_{ox} = \dfrac{\epsilon_{ox}}{t_{ox}}$

$\epsilon_{ox} = 34.5$ pF/m

$C_{ox}^{-1} = 58 \sim 290 \text{ m}^2/\text{F} \left(\dfrac{\mu\text{m}^2}{\text{pF}}\right)$

For 10 pF:

Area $= 580 \sim 2900 \ (\mu\text{m}^2)$

so

$d = 24 \sim 54\ \mu$m

5.2 $C_{ox} = 9\ \text{fF}/\mu\text{m}^2,\ V_{OV} = 0.2$ V

$L = 0.36\ \mu$m, $V_{DS} = 0$ V

$W = 3.6\ \mu$m

$Q = C_{ox}.W.L.V_{OV} = 2.33$ fC

5.3 $k'_n = \mu_n C_{ox}$

$$= \frac{\text{m}^2}{\text{V}\cdot\text{s}}\ \frac{\text{F}}{\text{m}^2} = \frac{\text{F}}{\text{V}\cdot\text{s}} = \frac{\text{C/V}}{\text{V}\cdot\text{s}} = \frac{\text{C}}{\text{s}}\ \frac{1}{\text{V}^2}$$

$$= \frac{\text{A}}{\text{V}^2}$$

Since $k_n = k'_n W/L$ and W/L is dimensionless, k_n has the same dimensions as k'_n; that is, A/V^2.

5.4 With v_{DS} small, compared to V_{OV}, Eq. (5.13a) applies:

$$r_{DS} = \frac{1}{(\mu_n C_{ox})\left(\dfrac{W}{L}\right)(V_{OV})}$$

(a) V_{OV} is doubled $\rightarrow r_{DS}$ is halved. factor $= 0.5$

(b) W is doubled $\rightarrow r_{DS}$ is halved. factor $= 0.5$

(c) W and L are doubled $\rightarrow r_{DS}$ is unchanged. factor $= 1.0$

(d) If oxide thickness t_{ox} is halved, and

$C_{ox} = \dfrac{\epsilon_{ox}}{t_{ox}}$

then C_{ox} is doubled. If W and L are also halved, r_{DS} is halved, factor $= 0.5$.

5.5 The transistor size will be minimized if W/L is minimized. To start with, we minimize L by using the smallest feature size,

$L = 0.18\ \mu$m

$$r_{DS} = \frac{1}{k'_n\,(W/L)\,(v_{GS} - V_t)}$$

$$r_{DS} = \frac{1}{k'_n\,(W/L)\,v_{OV}}$$

Two conditions need to met for v_{OV} and r_{DS}

Condition 1:

$$r_{DS,1} = \frac{1}{400 \times 10^{-6}\,(W/L) v_{OV,1}}$$

$= 250 \Rightarrow (W/L)\ v_{OV,1} = 10$

Condition 2:

$$r_{DS,2} = \frac{1}{400 \times 10^{-6}\,(W/L)\ v_{OV,2}}$$

$= 1000 \Rightarrow (W/L)\ v_{OV,2} = 2.5$

If condition 1 is met, condition 2 will be met since the over-drive voltage can always be reduced to satisfy this requirement. For condition 1, we want to decrease W/L as much as possible (so long as it is greater than or equal to 1), while still meeting all of the other constraints. This requires our using the largest possible $v_{GS,1}$ voltage.
$v_{GS,1} = 1.8$ V so $v_{OV,1} = 1.8 - 0.5 = 1.3$ V, and

$$W/L = \frac{10}{v_{OV,1}} = \frac{10}{1.3} = 7.69$$

Condition 2 now can be used to find $v_{GS,2}$

$$v_{OV,2} = \frac{2.5}{W/L} = \frac{2.5}{7.69} = 0.325$$

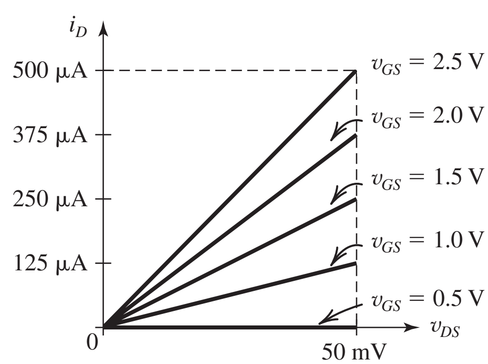
$\Rightarrow v_{GS,2} = 0.825 \text{ V} \Rightarrow 0.825 \text{ V} \le v_{GS} \le 1.8$ V

5.6 $k_n = 5\ \text{mA/V}^2$, $V_{tn} = 0.5$ V,

small v_{DS}

$i_D = k_n (v_{GS} - V_t) v_{DS} = k_n v_{OV} v_{DS}$

$$g_{DS} = \frac{1}{r_{DS}} = k_n v_{OV}$$



This table belongs to Exercise 5.6.

V_{GS} (V)	V_{OV} (V)	g_{DS} (mA/V)	r_{DS} (Ω)
0.5	0	0	∞
1.0	0.5	2.5	400
1.5	1.0	5.0	200
2.0	1.5	7.5	133
2.5	2.0	10	100

5.7 $t_{ox} = 4$ nm, $V_t = 0.5$ V

$L_{\min} = 0.18\ \mu$m, small v_{DS},

$k'_n = 400\ \mu\text{A/V}^2,\ 0 < v_{GS} < 1.8$ V.

$$r_{DS}^{-1} = k'_n\ W/L\ (v_{GS} - V_t) \le 1\ \text{mA/V} = \frac{1}{1\ \text{k}\Omega}$$

$W/L \le 1.92$

$W \le 0.35\ \mu$m

5.8 $r_{ds} = 1/\left.\dfrac{\partial i_D}{\partial v_{DS}}\right|_{v_{DS} = V_{DS}}$

$$= \left[\frac{\partial}{\partial v_{DS}}\left(k_n\left(V_{OV}v_{DS} - \frac{1}{2}v_{DS}^2\right)\right)\right]^{-1}$$

$$= \left[k_n\left(\frac{\partial}{\partial v_{DS}}\right)(v_{OV}v_{DS}) - 1/2\frac{\partial}{\partial v_{DS}}\left(v_{DS}^2\right)\right]^{-1}$$

$$= \left[k_n\left(V_{OV} - \frac{1}{2}\cdot 2V_{DS}\right)\right]^{-1}$$

$$= \frac{1}{k_n\,(V_{OV} - V_{DS})}$$

If $V_{DS} = 0 \Rightarrow r_{ds} = \dfrac{1}{k_nV_{OV}}$

If $V_{DS} = 0.2V_{OV} \Rightarrow r_{ds} = \dfrac{1.25}{V_{OV}}$

If $V_{DS} = 0.5V_{OV} \Rightarrow r_{ds} = \dfrac{1}{k_n\,(V_{OV} - 0.5V_{OV})}$

$$= 1/k_n\,(0.5V_{OV}) = \frac{2}{k_nV_{OV}}$$

If $V_{DS} = 0.8V_{OV} \Rightarrow r_{ds} = \dfrac{1}{k_n\,(V_{OV} - 0.8V_{OV})}$

$$= 1/k_n\,(0.2V_{OV}) = \frac{5}{k_nV_{OV}}$$

If $V_{DS} = V_{OV}$,

$$r_{ds} = \frac{1}{0} \Rightarrow \infty$$

5.9 $V_{DS\ \text{sat}} = V_{OV}$

$V_{OV} = V_{GS} - V_t = 1 - 0.5 = 0.5$ V

$\Rightarrow V_{DS\ \text{sat}} = 0.5$ V

In saturation:

$$i_D = \frac{1}{2}\,k'_n\left(\frac{W}{L}\right)V_{OV}^2 = \frac{1}{2}\,k_nV_{OV}^2$$

$$i_D = \frac{1}{2} \times \frac{4\ \text{mA}}{\text{V}^2} \times (0.5\ \text{V})^2$$

$i_D = 0.5$ mA

5.10 $L_{\min} = 0.25\ \mu$m

$t_{ox} = 6$ nm

$$\mu_n = 460\ \frac{\text{cm}^2}{\text{V}\cdot\text{s}} = 460 \times 10^{-4}\ \frac{\text{m}^2}{\text{V}\cdot\text{s}}$$

(a) $C_{ox} = \dfrac{\epsilon_{ox}}{t_{ox}} = \dfrac{34.5\ \text{pF/m}}{6\ \text{nm}}$

$$= 5.75 \times 10^{-3}\ \frac{\text{F}}{\text{m}^2}\left(\frac{\text{pF}}{\mu\text{m}^2}\right)$$

$k'_n = \mu_nC_{ox} = 265\ \mu\text{A/V}^2$

(b) For $\dfrac{W}{L} = \dfrac{20}{0.25},\ k_n = 21.2\ \text{mA/V}^2$

$\therefore 0.5\ \text{mA} = I_D = \dfrac{1}{2}\,k_nV_{OV}^2$

$V_{OV} = 0.22$ V

$V_{GS} = 0.72$ V

$V_{DS} \ge 0.22$ V

(c) $g_{DS} = \dfrac{1}{100\ \Omega} = k_nV_{OV}$

$\therefore V_{OV} = 0.47$ V.

$V_{GS} = 0.97$ V.

5.11 $V_{tp} = -0.7$ V

(a) $|V_{SG}| = |V_{tp}| + |V_{OV}|$

$= 0.7 + 0.4 = 1.1$ V

$\Rightarrow V_G = -1.1$ V

(b) For the p-channel transistor to operate in saturation, the drain voltage must not exceed the gate voltage by more than $|V_{tp}|$. Thus

$v_{D\max} = -1.1 + 0.7 = -0.4$ V

Put differently, V_{SD} must be at least equal to $|V_{OV}|$, which in this case is 0.4 V. Thus $v_{D\max} = -0.4$ V.

(c) In (b), the transistor is operating in saturation, thus

$$I_D = \frac{1}{2}k_p|V_{OV}|^2$$

$0.5 = \frac{1}{2} \times k_p \times 0.4^2$

$\Rightarrow k_p = 6.25 \text{ mA/V}^2$

For $V_D = -20$ mV, the transistor will be operating in the triode region. Thus

$I_D = k_p\left[v_{SD}|V_{OV}| - \frac{1}{2}v_{SD}^2\right]$

$= 6.25\left[0.02 \times 0.4 - \frac{1}{2}(0.02)^2\right]$

$= 0.05$ mA

For $V_D = -2$ V, the transistor will be operating in saturation, thus

$I_D = \frac{1}{2}k_p|V_{OV}|^2 = \frac{1}{2} \times 6.25 \times 0.4^2 = 0.5$ mA

5.12 $i_D = \frac{1}{2}k_n' \frac{W}{L}|V_{OV}|^2 \qquad k_n' = \mu_n C_{ox}$

For equal drain currents:

$\mu_n C_{ox}\frac{W_n}{L} = \mu_p C_{ox}\frac{W_p}{L}$

$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} = \frac{1}{0.4} = 2.5$

5.13 For small $v_{DS}, i_D \simeq k_n' \frac{W}{L_1}(V_{GS} - V_t)V_{DS}$,

$r_{DS} = \frac{V_{DS}}{i_D} = \frac{1}{k_n' \frac{W}{L}(V_{GS} - V_t)}$

$= \frac{1}{100 \times 10^{-6} \times 20 \times (5 - 0.7)}$

$r_{DS} = 116.3\ \Omega \qquad V_{DS} = r_{DS} \times i_D = 116.3$ mV

For the same performance of a p-channel device:

$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} = 2.5 \Rightarrow \frac{W_p}{L} = \frac{W_n}{L} \times 2.5$

$= 20 \times 2.5 \Rightarrow \frac{W_p}{L} = 50$

5.14 $t_{ox} = 6$ nm, $\mu_n = 460$ cm^2/V·s, $V_t = 0.5$ V, and $W/L = 10$.

$k_n = \mu_n C_{ox}\frac{W}{L} = 460 \times 10^{-4} \times \frac{3.45 \times 10^{-11}}{6 \times 10^{-9}} \times 10$

$= 2.645 \text{ mA/V}^2$

(a) $v_{GS} = 2.5$ V and $v_{DS} = 1$ V

$v_{OV} = v_{GS} - V_t = 2$ V

Thus $v_{DS} < v_{OV} \Rightarrow$ triode region,

$I_D = k_n\left[v_{DS}v_{OV} - \frac{1}{2}v_{DS}^2\right]$

$= 2.645\left[1 \times 2 - \frac{1}{2} \times 1\right] = 4$ mA

(b) $v_{GS} = 2$ V and $v_{DS} = 1.5$ V

$v_{OV} = v_{GS} - V_t = 2 - 0.5 = 1.5$ V

Thus, $v_{DS} = v_{OV} \Rightarrow$ saturation region,

$i_D = \frac{1}{2}k_n v_{OV}^2 = \frac{1}{2} \times 2.645 \times 1.5^2$

$= 3$ mA

(c) $v_{GS} = 2.5$ V and $v_{DS} = 0.2$ V

$v_{OV} = 2.5 - 0.5 = 2$ V

Thus, $v_{DS} < v_{OV} \Rightarrow$ triode region,

$i_D = k_n\left[v_{DS}v_{OV} - \frac{1}{2}v_{DS}^2\right]$

$= 2.645[0.2 \times 2 - \frac{1}{2}0.2^2] = 1$ mA

(d) $v_{GS} = v_{DS} = 2.5$ V

$v_{OV} = 2.5 - 0.5 = 2$ V

Thus, $v_{DS} > v_{OV} \Rightarrow$ saturation region,

$i_D = \frac{1}{2}k_n v_{OV}^2$

$= \frac{1}{2} \times 2.645 \times 2^2 = 5.3$ mA

5.15 See Table on next page.

5.16 $i_D = k_n\left[v_{OV}v_{DS} - \frac{1}{2}v_{DS}^2\right]$

$$\frac{i_D}{k_n} = v_{OV}v_{DS} - \frac{1}{2}v_{DS}^2 \qquad (1)$$

Figure 1 shows graphs for i_D/k_n versus v_{DS} for various values of v_{OV}. Since the right-hand side of Eq. (1) does not have any MOSFET parameters, these graphs apply for any n-channel MOSFET with the assumption that $\lambda = 0$. They also apply to p-channel devices with v_{DS} replaced by v_{SD}, k_n by k_p, and v_{OV} with $|v_{OV}|$. The slope of each graph at $v_{DS} = 0$ is found by differentiating Eq. (1) relative to v_{DS} with $v_{OV} = V_{OV}$ and then substituting $v_{DS} = 0$. The result is

$$\left.\frac{d(i_D/k_n)}{d v_{DS}}\right|_{v_{DS}=0,\ v_{OV}=V_{OV}} = V_{OV}$$

Figure 1 shows the tangent at $v_{DS} = 0$ for the graph corresponding to $v_{OV} = V_{OV3}$. Observe that it intersects the horizontal line $i_D/k_n = \frac{1}{2}V_{OV3}^2$ at $v_{DS} = \frac{1}{2}V_{OV3}$. Finally, observe that the curve representing the boundary between the triode region and the saturation region has the equation

$i_D/k_n = \frac{1}{2}v_{DS}^2$

This table belongs to **5.15**.

L (μm)	0.5	0.25	0.18	0.13
t_{ox} (nm)	10	5	3.6	2.6
$C_{ox}\left(\frac{\text{fF}}{\mu\text{m}^2}\right)$ $\epsilon_{ox} = 34.5$ pF/m	3.45	6.90	9.58	13.3
$k'_n\left(\frac{\mu\text{A}}{\text{V}^2}\right)$ $(\mu_n = 500\ \text{cm}^2/\text{V}\cdot\text{s})$	173	345	479	665
$k_n\left(\frac{\text{mA}}{\text{V}^2}\right)$ for $\frac{W}{L} = 10$	1.73	3.45	4.79	6.65
$A(\mu\text{m}^2)$ for $\frac{W}{L} = 10$	2.50	0.625	0.324	0.169
V_{DD}(V)	5	2.5	1.8	1.3
V_t(V)	0.7	0.5	0.4	0.4
I_D(mA) for $V_{GS} = V_{DS} = V_{DD}$, $I_D = \frac{1}{2}k_n(V_{DD} - V_t)^2$	16	6.90	4.69	2.69
P(mW) $P = V_{DD}I_D$	80	17.3	8.44	3.50
$\frac{P}{A}\left(\frac{\text{mW}}{\mu\text{m}^2}\right)$	32	27.7	26.1	20.7
$\frac{\text{Devices}}{\text{Chip}}$	n	$4n$	$7.72n$	$14.8n$

This figure belongs to **5.16**, part (a).

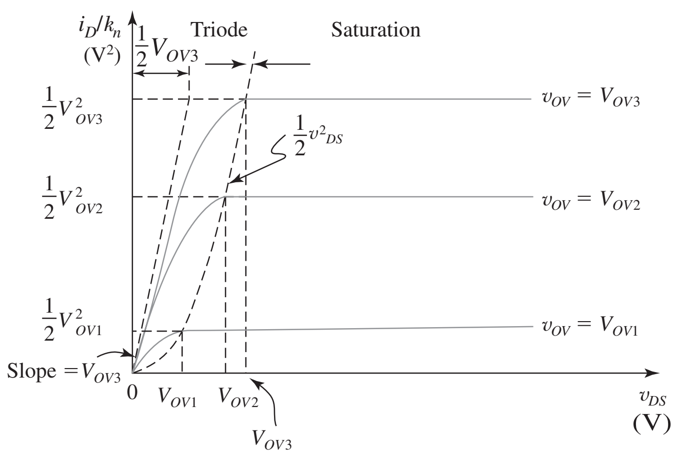


Fig. 1

Figure 2 shows the graph for the relationship

$$i_D/k_n = \frac{1}{2}v^2_{OV}$$

which describes the MOSFETs operation in the saturation region, that is,

$$v_{DS} \geq v_{OV}$$

Here also observe that this relationship (and graph) is universal and represents any MOSFET. The slope at $v_{OV} = V_{OV}$ is

$$\left.\frac{d\,(i_D/k_n)}{d\ v_{OV}}\right|_{v_{OV}=V_{OV}} = V_{OV}$$

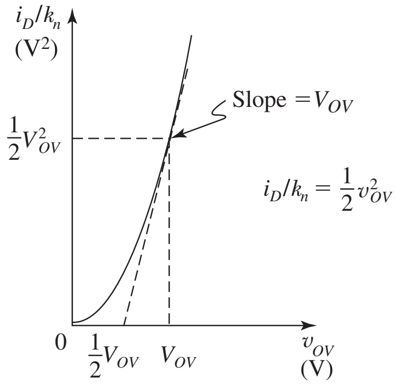


Fig. 2

Replacing k_n by k_p and v_{OV} by $|v_{OV}|$ adapts this graph to PMOS transistors.

5.17 For triode-region operation with v_{DS} small,

$$i_D \simeq k_n(v_{GS} - V_t)v_{DS}$$

Thus

$$r_{DS} \equiv \frac{v_{DS}}{i_D} = \frac{1}{k_n(v_{GS} - V_t)}$$

$$1 = \frac{1}{k_n(1.2 - 0.8)} = \frac{1}{0.4\ k_n}$$

$$\Rightarrow k_n = 2.5 \text{ mA/V}$$

$$r_{DS} = \frac{1}{2.5(V_{GS} - 0.8)} \quad (\text{k}\Omega)$$

$$0.2 = \frac{1}{2.5(V_{GS} - 0.8)}$$

$$\Rightarrow V_{GS} = 2.8 \text{ V}$$

For a device with twice the value of W, k_n will be twice as large and the resistance values will be half as large: 500 Ω and 100 Ω, respectively.

5.18 $V_{tn} = 0.5$ V, $\quad k_n = 1.6$ mA/V^2

$$I_D = 0.05 = \frac{1}{2} \times 1.6 \times V_{OV}^2$$

$$\Rightarrow V_{OV} = 0.25 \text{ V and } V_{DS} \geq 0.25 \text{ V}$$

$$V_{GS} = 0.5 + 0.25 = 0.75 \text{ V}$$

$$I_D = 0.2 = \frac{1}{2} \times 1.6 \times V_{OV}^2$$

$$\Rightarrow V_{OV} = 0.5 \text{ V and } V_{DS} \geq 0.5 \text{ V}$$

$$V_{GS} = 0.5 + 0.5 = 1 \text{ V}$$

5.19 For $V_{GS} = V_{DS} = 1$ V, the MOSFET is operating in saturation,

$$I_D = \frac{1}{2}k_n(V_{GS} - V_t)^2$$

$$0.4 = \frac{1}{2}k_n(1 - V_t)^2 \qquad (1)$$

$$0.1 = \frac{1}{2}k_n(0.8 - V_t)^2 \qquad (2)$$

Dividing Eq. (1) by Eq. (2) and taking square roots gives

$$2 = \frac{1 - V_t}{0.8 - V_t}$$

$$\Rightarrow V_t = 0.6 \text{ V}$$

Substituting in Eq. (1), we have

$$0.4 = \frac{1}{2}k_n \times 0.4^2$$

$$\Rightarrow k_n = 5 \text{ mA/V}^2$$

5.20 $k_n' = 0.4$ mA/V^2 and $V_t = 0.5$ V

For $v_{GS} = v_{DS} = 1.8$ V, the MOSFET is operating in saturation. Thus, to obtain $I_D = 2$ mA, we write

$$2 = \frac{1}{2} \times 0.4 \times \frac{W}{L} \times (1.8 - 0.5)^2$$

$$\Rightarrow \frac{W}{L} = 5.92$$

For $L = 0.18$ μm

$$W = 1.07 \text{ μm}$$

5.21 $i_D = k_n(v_{GS} - V_t)v_{DS}$

$$25 = k_n(1 - V_t) \times 0.05 \qquad (1)$$

$$50 = k_n(1.5 - V_t) \times 0.05 \qquad (2)$$

Dividing Eq. (2) by Eq. (1), we have

$$2 = \frac{1.5 - V_t}{1 - V_t}$$

$$\Rightarrow V_t = 0.5 \text{ V}$$

Substituting in Eq. (1) yields

$$25 = k_n \times 0.5 \times 0.05$$

$$\Rightarrow k_n = 1000 \text{ μA/V}^2$$

For $k_n' = 50$ μA/V^2

$$\frac{W}{L} = 20$$

For $v_{GS} = 2$ V and $v_{DS} = 0.1$ V,

$$i_D = k_n\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

$$= 1\left[(2 - 0.5) \times 0.1 - \frac{1}{2} \times 0.1^2\right]$$

$$= 0.145 \text{ mA} = 145 \text{ μA}$$

For $v_{GS} = 2$ V, pinch-off will occur for

$$v_{DS} = v_{GS} - V_t = 2 - 0.5 = 1.5 \text{ V}$$

and the resulting drain current will be

$$i_D = \frac{1}{2} k_n (v_{GS} - V_t)^2$$

$$= \frac{1}{2} \times 1 \times (2 - 0.5)^2$$

$$= 1.125 \text{ mA}$$

5.22 For the channel to remain continuous,

$$v_{DS} \le v_{GS} - V_t$$

Thus for $v_{GS} = 1.0$ V to 1.8 V and $V_t = 0.4$,

$$v_{DS} \le 1 - 0.4$$

That is, $v_{DS\max} = 0.6$ V.

5.23 $\dfrac{W}{L} = \dfrac{20}{1} = 20 \quad k_n' = 100\ \mu\text{A/V}^2$

$$k_n = k_n' \left(\frac{W}{L} \right) = 100 \times 20 = 2000\ \mu\text{A/V}^2$$

$$= 2 \text{ mA/V}^2$$

For operation as a linear resistance,

$$i_D = k_n (v_{GS} - V_t) v_{DS}$$

and

$$r_{DS} \equiv \frac{v_{DS}}{i_D} = \frac{1}{k_n (v_{GS} - V_t)}$$

$$= \frac{1}{2(v_{GS} - 0.8)}$$

At $v_{GS} = 1.0$ V,

$$r_{DS} = \frac{1}{2(1 - 0.8)} = 2.5 \text{ k}\Omega$$

At $v_{GS} = 4.8$ V,

$$r_{DS} = \frac{1}{2(4.8 - 0.8)} = 0.125 \text{ k}\Omega$$

Thus, r_{DS} will vary in the range of 2.5 kΩ to 125 Ω.

(a) If W is halved, k_n will be halved and r_{DS} will vary in the range of 5 kΩ to 250 Ω.

(b) If L is halved, k_n will be doubled and r_{DS} will vary in the range of 1.25 kΩ to 62.5 Ω.

(c) If both W and L are halved, k_n will remain unchanged and r_{DS} will vary in the original range of 2.5 kΩ to 125 Ω.

5.24 **(a)** Refer to Fig. P5.24. For saturation-mode operation of an NMOS transistor, $v_{DG} \ge -V_{tn}$; thus $v_{DG} = 0$ results in saturation-mode operation. Similarly, for a p-channel MOSFET, saturation-mode operation is obtained for $v_{GD} \ge -|V_{tp}|$, which includes $v_{GD} = 0$. Thus, the diode-connected MOSFETs of Fig. P5.24 have the $i - v$ relationship

$$i = \frac{1}{2} k' \left(\frac{W}{L} \right) (v - |V_t|)^2 \qquad (1)$$

where k' represents k_n' in the NMOS case and k_p' in the PMOS case.

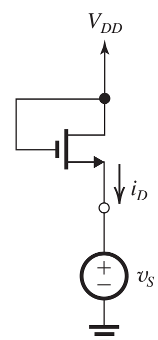
(b) If either of the MOSFETs in Fig. P5.24 is biased to operate at $v = |V_t| + |V_{OV}|$, then its incremental resistance r at the bias point can be obtained by differentiating Eq. (1) relative to v and then substituting $v = |V_t| + |V_{OV}|$ as follows:

$$\frac{\partial i}{\partial v} = k' \left(\frac{W}{L} \right) (v - |V_t|)$$

$$\left. \frac{\partial i}{\partial v} \right|_{v = |V_t| + V_{OV}} = k' \left(\frac{W}{L} \right) V_{OV}$$

$$r = 1 \Big/ \left[\frac{\partial i}{\partial v} \right] = 1 \Big/ \left(k' \frac{W}{L} V_{OV} \right) \qquad \text{Q.E.D}$$

5.25



$$v_{GD} = 0 \Rightarrow \text{saturation}$$

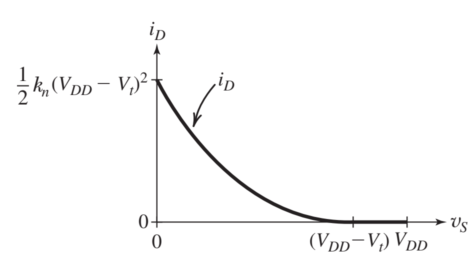
$$i_D = \frac{1}{2} k_n (v_{GS} - V_t)^2$$

$$v_{GS} = V_{DD} - v_S$$

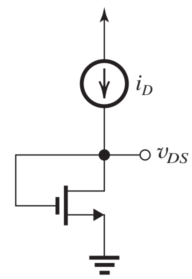
$$\therefore i_D = \frac{1}{2} k_n \left[(V_{DD} - V_t) - v_S \right]^2$$

$$0 \le v_S \le (V_{DD} - V_t)$$

$$i_D = 0,\ v_S \ge (V_{DD} - V_t)$$



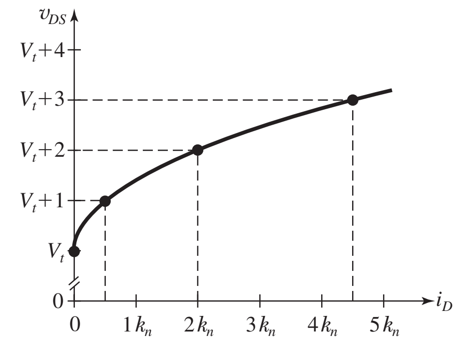
5.26



$v_{DS} = v_{GS}$

$$i_D = \frac{1}{2} k_n (v_{DS} - V_t)^2$$

$$\therefore v_{DS} = \sqrt{\frac{2 i_D}{k_n}} + V_t$$



5.27 $V_{DS} = V_D - V_S \quad V_{GS} = V_G - V_S$

$V_{OV} = V_{GS} - V_t = V_{GS} - 1.0$

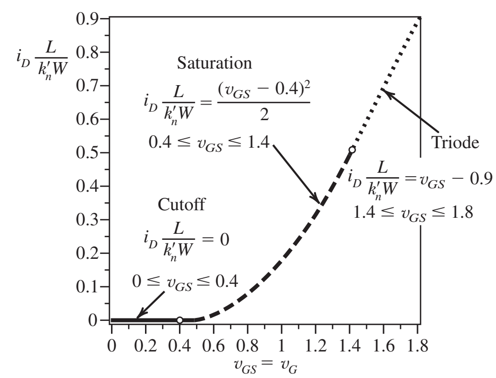
According to Table 5.1, three regions are possible.

Case	V_S	V_G	V_D	V_{GS}	V_{OV}	V_{DS}	Region of operation
a	+1.0	+1.0	+2.0	0	–1.0	+1.0	Cutoff
b	+1.0	+2.5	+2.0	+1.5	+0.5	+1.0	Sat.
c	+1.0	+2.5	+1.5	+1.5	+0.5	+0.5	Sat.
d	+1.0	+1.5	0	+0.5	–0.5	–1.0	Sat.*
e	0	+2.5	1.0	+2.5	+1.5	+1.0	Triode
f	+1.0	+1.0	+1.0	0	–1.0	0	Cutoff
g	–1.0	0	0	+1.0	0	+1.0	Sat.
h	–1.5	0	0	+1.5	+0.5	+1.5	Sat.
i	–1.0	0	+1.0	+1.0	0	+2.0	Sat.
j	+0.5	+2.0	+0.5	+1.5	+0.5	0	Triode

* With the source and drain interchanged.

5.28 The cutoff–saturation boundary is determined by $v_{GS} = V_t$, thus $v_{GS} = 0.4$ V at the boundary.

The saturation–triode boundary is determined by $v_{GD} = V_t$, and $v_{DS} = V_{DD} = 1$ V, and since $v_{GS} = v_{GD} + v_{DS}$, one has $v_{GS} = 0.4 + 1.0 = 1.4$ V at the boundary.



5.29 (a) Let Q_1 have a ratio (W/L) and Q_2 have a ratio $1.03\,(W/L)$. Thus

$$I_{D1} = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (1 - V_t)^2$$

$$I_{D2} = \frac{1}{2} k_n' \left(\frac{W}{L}\right) \times 1.03 \times (1 - V_t)^2$$

Thus,

$$\frac{I_{D2}}{I_{D1}} = 1.03$$

That is, a 3% mismatch in the W/L ratios results in a 3% mismatch in the drain currents.

(b) Let Q_1 have a threshold voltage $V_t = 0.6$ V and Q_2 have a threshold voltage $V_t + \triangle V_t = 0.6 + 0.01 = 0.61$ V.

Thus

$$I_{D1} = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (1 - 0.6)^2$$

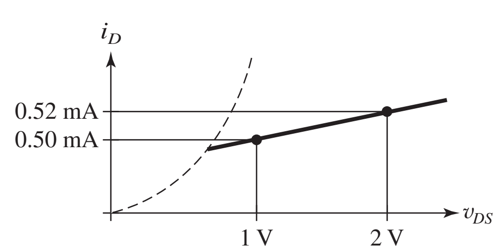
$$I_{D2} = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (1 - 0.61)^2$$

and

$$\frac{I_{D2}}{I_{D1}} = \frac{(1 - 0.61)^2}{(1 - 0.6)^2} = 0.95$$

That is, a 10-mV mismatch in the threshold voltage results in a 5% mismatch in drain currents.

5.30



$$r_o = \left.\frac{\Delta v_{DS}}{\Delta i_D}\right|_{v_{GS}\ \text{const.}} = \frac{1}{0.02} = 50\ \text{k}\Omega$$

$$V_A \cong I_D r_o = 0.5 \times 50 = 25\ \text{V}$$

$$\lambda = \frac{1}{V_A} = 0.04\ \text{V}^{-1}$$

5.31 $r_o = \frac{V_A}{i_D} = \frac{20}{i_D}$, $0.1\ \text{mA} \le i_D \le 1\ \text{mA}$

$\Rightarrow 20\ \text{k}\Omega \le r_o \le 200\ \text{k}\Omega$

$$r_o = \frac{\Delta v_{DS}}{\Delta i_D} \Rightarrow \Delta i_D = \frac{\Delta v_{DS}}{r_o} = \frac{1}{r_o}$$

At $i_D = 0.1$ mA, $\Delta i_D = 5\ \mu\text{A}, \frac{\Delta i_D}{i_D} = 5\%$

At $i_D = 1$ mA, $\Delta i_D = 50\ \mu\text{A}, \frac{\Delta i_D}{i_D} = 5\%$

5.32 $V_A = V_A' L$, where V_A' is completely process dependent. Also, $r_o = \frac{V_A}{i_D}$. Therefore, to achieve desired r_o (which is 5 times larger), we should increase L ($L = 5 \times 1 = 5\ \mu\text{m}$).

To keep I_D unchanged, the $\frac{W}{L}$ ratio must stay unchanged. Therefore:

$W = 5 \times 10 = 50\ \mu\text{m}$ (so $\frac{W}{L}$ is kept at 10)
$V_A = r_o i_D = 100\ \text{k}\Omega \times 0.2\ \text{mA} = 20$ V (for the standard device)

$V_A = 5 \times 20 = 100$ V (for the new device)

5.33 $L = 1.5\ \mu\text{m} = 3\times$ minimum. Thus

$$\lambda = \frac{0.03\ \text{V}^{-1}}{3} = 0.01\ \text{V}^{-1}$$

If v_{DS} is increased from 1 V to 5 V, the drain current will change from

$$I_D = 100\ \mu\text{A} = I_D'(1 + \lambda \times 1) = 1.01\ I_D'$$

to

$$I_D + \Delta I_D = I_D'(1 + \lambda \times 5) = 1.05\ I_D'$$

where I_D' is the drain current without channel-length modulation taken into account. Thus

$$I_D' = \frac{100}{1.01}$$

and

$$100 + \Delta I_D = 1.05\ I_D' = \frac{1.05 \times 100}{1.01} = 104\ \mu\text{A}$$

$\Rightarrow \Delta I_D = 4\ \mu\text{A}$ or 4%

To reduce ΔI_D by a factor of 2, we need to reduce λ by a factor of 2, which can be obtained by doubling the channel length to 3 μm.

5.34 $V_A = V_A' L = 20 \times 1.5 = 30$ V

$$\lambda = \frac{1}{V_A} = \frac{1}{30} = 0.033\ \text{V}^{-1}$$

$$I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{OV}^2 (1 + \lambda V_{DS})$$

$$= \frac{1}{2} \times 0.2 \times \left(\frac{15}{1.5}\right) \times 0.5^2 (1 + 0.033 \times 2)$$

$= 0.267$ mA

$$r_o = \frac{V_A}{\frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{OV}^2} = \frac{30}{\frac{1}{2} \times 0.2 \times \left(\frac{15}{1.5}\right) \times 0.5^2}$$

$= 120\ \text{k}\Omega$

$$\Delta I_D = \frac{\Delta V_{DS}}{r_o} = \frac{1\ \text{V}}{120\ \text{k}\Omega} = 0.008\ \text{mA}$$

5.35 Quadrupling W and L keeps the current I_D unchanged. However, the quadrupling of L increases V_A by a factor of 4 and hence increases r_o by a factor of 4.

Halving V_{OV} results in decreasing I_D by a factor of 4. Thus, this alone increases r_o by a factor of 4. The overall increase in r_o is by a factor of $4 \times 4 = 16$.

5.36 Refer to the circuit in Fig. P5.29 and let $V_{D1} = 2$ V and $V_{D2} = 2.5$ V. If the two devices are matched,

$$I_{D1} = \frac{1}{2} k_n (1 - V_t)^2 \left(1 + \frac{2}{V_A}\right)$$

$$I_{D2} = \frac{1}{2} k_n (1 - V_t)^2 \left(1 + \frac{2.5}{V_A}\right)$$

$$\Delta I_D = I_{D2} - I_{D1} = \frac{1}{2} k_n (1 - V_t)^2 \left(\frac{0.5}{V_A}\right)$$

$$\frac{\Delta I_D}{\frac{1}{2} k_n (1 - V_t)^2} \simeq 0.01 = \frac{0.5}{V_A}$$

$\Rightarrow V_A = 50$ V (or larger to limit the mismatch in I_D to 1%).

If $V_A' = 100\ \text{V}/\mu\text{m}$, the minimum required channel length is 0.5 μm.

5.37

NMOS	1	2	3	4
λ	$0.05\ \text{V}^{-1}$	$0.02\ \text{V}^{-1}$	$0.1\ \text{V}^{-1}$	$0.01\ \text{V}^{-1}$
V_A	20 V	50 V	10 V	100 V
I_D	0.5 mA	2 mA	0.1 mA	0.2 mA
r_o	40 kΩ	25 kΩ	100 kΩ	500 kΩ

5.38

$$k_p = k'_p\left(\frac{W}{L}\right) = 100\ \mu\text{A/V}^2$$

$$V_{tp} = -1\text{ V} \quad \lambda = -0.02\text{ V}^{-1}$$

$$V_G = 0, \quad V_S = +5\text{ V} \Rightarrow V_{SG} = 5\text{ V}$$

$$|V_{OV}| = V_{SG} - |V_{tp}| = 5 - 1 = 4$$

• For $v_D = +4$ V, $v_{SD} = 1\text{ V} < |V_{OV}| \Rightarrow$ triode-region operation,

$$i_D = k_p\left[v_{SD}|V_{OV}| - \frac{1}{2}v_{SD}^2\right]$$

$$= 100\left(1 \times 4 - \frac{1}{2} \times 1\right) = 350\ \mu\text{A}$$

• For $v_D = +2$ V, $v_{SD} = 3\text{ V} < |V_{OV}| \Rightarrow$ triode-region operation,

$$i_D = k_p\left[v_{SD}|V_{OV}| - \frac{1}{2}v_{SD}^2\right]$$

$$= 100\left(3 \times 4 - \frac{1}{2} \times 9\right) = 750\ \mu\text{A}$$

• For $v_D = +1$ V, $v_{SD} = 4\text{ V} = |V_{OV}| \Rightarrow$ saturation-mode operation,

$$i_D = \frac{1}{2}k_p|V_{OV}|^2(1 + |\lambda|v_{SD})$$

$$= \frac{1}{2} \times 100 \times 16(1 + 0.02 \times 4) = 864\ \mu\text{A}$$

• For $v_D = 0$ V, $v_{SD} = 5\text{ V} > |V_{OV}| \Rightarrow$ saturation-mode operation,

$$i_D = \frac{1}{2} \times 100 \times 16(1 + 0.02 \times 5) = 880\ \mu\text{A}$$

• For $v_D = -5$ V, $v_{SD} = 10\text{ V} > |V_{OV}| \Rightarrow$ saturation-mode operation,

$$i_D = \frac{1}{2} \times 100 \times 16(1 + 0.02 \times 10) = 960\ \mu\text{A}$$

5.39 $V_{tp} = 0.8$ V, $\quad |V_A| = 40$ V

$$|v_{GS}| = 3\text{ V}, \quad |v_{DS}| = 4\text{ V}$$

$$i_D = 3\text{ mA}$$

$$|V_{OV}| = |v_{GS}| - |V_{tp}| = 2.2\text{ V}$$

$$|v_{DS}| > |V_{OV}| \Rightarrow \text{ saturation mode}$$

$$v_{GS} = -3\text{ V}$$

$$v_{SG} = +3\text{ V}$$

$$v_{DS} = -4\text{ V}$$

$$v_{SD} = 4\text{ V}$$

$$V_{tp} = -0.8\text{ V}$$

$$V_A = -40\text{ V}$$

$$\lambda = -0.025\text{ V}^{-1}$$

$$i_D = \frac{1}{2}k_p(v_{GS} - V_{tp})^2(1 + \lambda\ v_{DS})$$

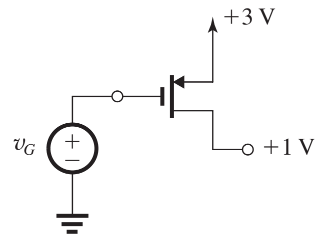
$$3 = \frac{1}{2}k_p[-3 - (-0.8)]^2(1 - 0.025 \times -4)$$

$$\Rightarrow k_p = 1.137\text{ mA/V}^2$$

5.40 PMOS with $V_{tp} = -1$ V

Case	V_S	V_G	V_D	V_{SG}	$\|V_{OV}\|$	V_{SD}	Region of operation
a	+2	+2	0	0	0	2	Cutoff
b	+2	+1	0	+1	0	2	Cutoff–Sat.
c	+2	0	0	+2	1	2	Sat.
d	+2	0	+1	+2	1	1	Sat–Triode
e	+2	0	+1.5	+2	1	0.5	Triode
f	+2	0	+2	+2	1	0	Triode

5.41



$$V_{tp} = -0.5\text{ V}$$

$$v_G = +3\text{ V} \rightarrow 0\text{ V}$$

As v_G reaches +2.5 V, the transistor begins to conduct and enters the saturation region, since v_{DG} will be negative. The transistor continues to operate in the saturation region until v_G reaches 0.5 V, at which point v_{DG} will be 0.5 V, which is equal to $|V_{tp}|$, and the transistor enters the triode region. As v_G goes below 0.5 V, the transistor continues to operate in the triode region.

5.42 Case a, assume, sat,

$$\frac{(1 - V_t)^2}{(1.5 - V_t)^2} = \frac{100}{400} \Rightarrow V_t = 0.5,$$

$$V_{GD} \leq V_t$$

$\therefore$ sat;

Case b — same procedure, except use V_{SG} and V_{SD}.

This table belongs to **5.42**.

Case	Transistor	V_S (V)	V_G (V)	V_D (V)	I_D (μA)	Type	Mode	$\mu C_{ox}\frac{W}{L}$ (μ A/V²)	V_t (V)
a	1	0	1	2.5	100	NMOS	Sat.	800	0.5
		0	1.5	2.5	400		Sat.		
b	2	5	3	–4.5	50	PMOS	Sat.	400	–1.5
		5	2	–0.5	450		Sat.		
c	3	5	3	4	200	PMOS	Sat.	400	–1
		5	2	0	800		Sat.		
d	4	–2	0	0	72	NMOS	Sat.	100	+0.8
		–4	0	–3	270		Triode		

$$\frac{(2-1V_t1)^2}{(3-1V_t1)^2}=\frac{50}{450}\Rightarrow |V_t|=1.5,$$

$V_{GD}\geq -1.5\text{ V}\quad\therefore\text{ sat}$

Case c – $\dfrac{(2-|V_t|)^2}{(3-|V_t|)^2}=\dfrac{200}{800}\Rightarrow |V_t|=1.0,$

$V_{GD}\geq -1.0\text{ V}\quad\therefore\text{sat}$

Case d

$$\frac{\text{sat}\quad \frac{1}{2}k_n(2-V_t)^2}{\text{triode}\; k_n\left[(4-V_t)V_{DS}-\frac{1}{2}V_{DS}^2\right]}=\frac{72}{270}$$

(after failing assumption that both cases are sat.)

5.43 Refer to the circuits in Fig. P5.43.

(a) $V_1=V_{DS}=V_{GS}=1\text{ V}$

(b) $V_2=+1-V_{DS}=1-1=0\text{ V}$

(c) $V_3=V_{SD}=V_{SG}=1\text{ V}$

(d) $V_4=+1.25-V_{SG}=1.25-1=0.25\text{ V}$

Now place a resistor R in series with the drain. For the circuits in (a) and (b) to remain in saturation, V_D must not fall below V_G by more than V_t. Thus,

$IR\leq V_t$

$$R_{\max}=\frac{V_t}{I}=\frac{0.5}{0.1}=5\text{ k}\Omega$$

For the circuits in (c) and (d) to remain in saturation, V_D must not exceed V_G by more than $|V_t|$. Thus

$IR\leq |V_t|$

which yields $R_{\max}=5\text{ k}\Omega$.

Now place a resistor R_S in series with the MOSFET source. The voltage across the current source becomes

(a) $V_{CS}=2.5-V_{DS}-IR_S$ (1)

To keep V_{CS} at least at 0.5 V, the maximum R_S can be found from

$0.5=2.5-1-0.1\times R_{S\max}$

$\Rightarrow R_{S\max}=10\text{ k}\Omega$

$V_1=2.5-0.5=2\text{ V}$

(b) $V_{CS}=1-V_{DS}-IR_S-(-1.5)$

$=2.5-V_{DS}-IR_S$

which is identical to Eq. (1). Thus

$R_{S\max}=10\text{ k}\Omega$

$V_2=-1.5+0.5=-1\text{ V}$

(c) $V_{CS}=2.5-IR_S-V_{SD}$

which yields

$R_{S\max}=10\text{ k}\Omega$

$V_3=2.5-0.5=2\text{ V}$

(d) $V_{CS}=1.25-IR_S-V_{SD}-(-1.25)$

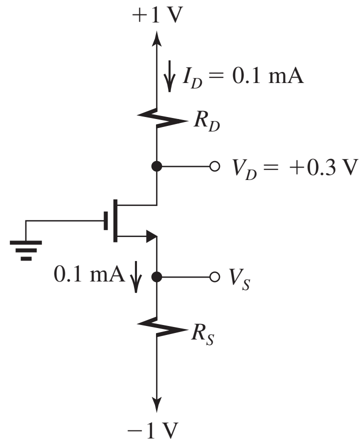
$=2.5-V_{SD}-IR_S$

which yields

$R_{S\max}=10\text{ k}\Omega$

$V_4=-1.25+0.5=-0.75\text{ V}$

5.44



Since $V_{DG} > 0$, the MOSFET is in saturation.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

$$0.1 = \frac{1}{2} \times 0.4 \times \frac{5}{0.4} \times V_{OV}^2$$

$$\Rightarrow V_{OV} = 0.2 \text{ V}$$

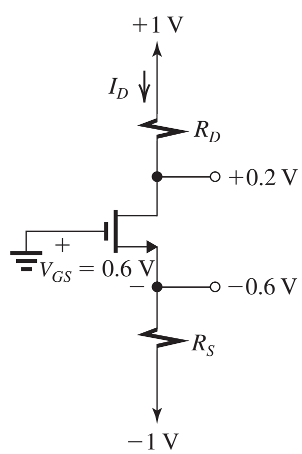
$$V_{GS} = V_t + V_{OV} = 0.5 + 0.2 = 0.7$$

$$V_S = 0 - V_{GS} = -0.7 \text{ V}$$

$$R_S = \frac{V_S - (-1)}{I_D} = \frac{-0.7 + 1}{0.1} = 3 \text{ k}\Omega$$

$$R_D = \frac{1 - V_D}{I_D} = \frac{1 - 0.3}{0.1} = \frac{0.7}{0.1} = 7 \text{ k}\Omega$$

5.45



Since $V_{DG} > 0$, the MOSFET is operating in saturation. Thus

$$I_D = \frac{1}{2}k_n(V_{GS} - V_t)^2$$

$$= \frac{1}{2} \times 4 \times (0.6 - 0.4)^2$$

$$= 0.08 \text{ mA}$$

$$R_D = \frac{1 - V_D}{I_D} = \frac{1 - 0.2}{0.08} = \frac{0.8}{0.08} = 10 \text{ k}\Omega$$

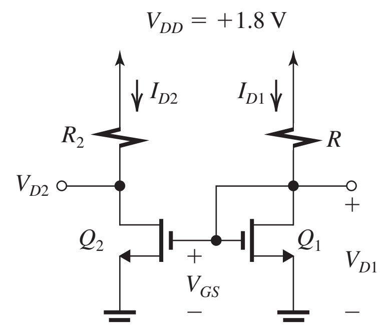
$$R_S = \frac{-0.6 - (-1)}{I_D} = \frac{-0.6 + 1}{0.08} = 5 \text{ k}\Omega$$

For I_D to remain unchanged from 0.08 mA, the MOSFET must remain in saturation. This in turn can be achieved by ensuring that V_D does not fall below V_G (which is zero) by more than V_t (0.4 V). Thus

$$1 - I_D R_{D\max} = -0.4$$

$$R_{D\max} = \frac{1.4}{0.08} = 17.5 \text{ k}\Omega$$

5.46



(a) $I_{D1} = 50\ \mu$A

$$0.05 = \frac{1}{2} \times 0.4 \times \frac{1.44}{0.36} V_{OV}^2$$

$$\Rightarrow V_{OV} = 0.25 \text{ V}$$

$$V_{GS1} = V_t + V_{OV}$$

$$= 0.5 + 0.25 = 0.75 \text{ V}$$

$$V_{D1} = V_{GS1} = 0.75 \text{ V}$$

$$R = \frac{V_{DD} - V_{D1}}{I_{D1}} = \frac{1.8 - 0.75}{0.05} = 21 \text{ k}\Omega$$

(b) Note that both transistors operate at the same V_{GS} and V_{OV}, and

$$I_{D2} = 0.5 \text{ mA}$$

But

$$I_{D2} = \frac{1}{2}k_n\left(\frac{W_2}{L_2}\right)V_{OV}^2$$

$$0.5 = \frac{1}{2} \times 0.4 \times \frac{W_2}{0.36} \times 0.25^2$$

$$\Rightarrow W_2 = 14.4\ \mu\text{m}$$

which is 10 times W_1, as needed to provide $I_{D2} = 10 I_{D1}$. Since Q_2 is to operate at the edge of saturation,

$$V_{DS2} = V_{OV}$$

Thus,

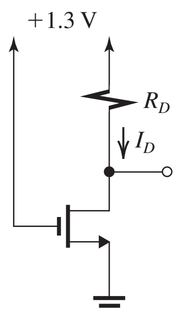
$$V_{D2} = 0.25 \text{ V}$$

and

$$R_2 = \frac{V_{DD} - V_{D2}}{I_{D2}}$$

$$= \frac{1.8 - 0.25}{0.5} = 3.1 \text{ k}\Omega$$

5.47



$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2$$

$$= \frac{1}{2} \times 0.4 \times \frac{W}{L} (1.3 - 0.4)^2$$

$$= 0.162 \left(\frac{W}{L} \right)$$

$$V_D = 1.3 - I_D R_D = 1.3 - 0.162 \left(\frac{W}{L} \right) R_D$$

For the MOSFET to be at the edge of saturation, we must have

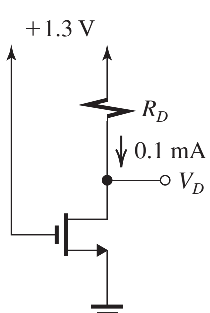
$$V_D = V_{OV} = 1.3 - 0.4 = 0.9$$

Thus

$$0.9 = 1.3 - 0.162 \left(\frac{W}{L} \right) R_D$$

$$\Rightarrow \left(\frac{W}{L} \right) R_D \simeq 2.5 \text{ k}\Omega \qquad \text{Q.E.D}$$

5.48



$$V_{OV} = V_{GS} - V_t$$

$$= 1.3 - 0.4 = 0.9$$

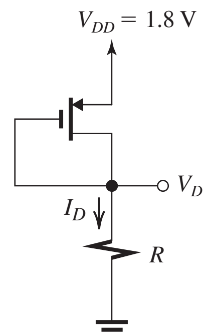
To operate at the edge of saturation, we must have

$$V_D = V_{OV} = 0.9 \text{ V}$$

Thus,

$$R_D = \frac{1.3 - 0.9}{0.1} = 4 \text{ k}\Omega$$

5.49



$$I_D = 180 \ \mu\text{A} \qquad \text{and} \qquad V_D = 1 \text{ V}$$

$$R = \frac{V_D}{I_D} = \frac{1}{0.18} = 5.6 \text{ k}\Omega$$

Transistor is operating in saturation with $|V_{OV}| = 1.8 - V_D - |V_t| = 1.8 - 1 - 0.5 = 0.3$ V:

$$I_D = \frac{1}{2} k_p' \frac{W}{L} |V_{OV}|^2$$

$$180 = \frac{1}{2} \times 100 \times \frac{W}{L} \times 0.3^2$$

$$\Rightarrow \frac{W}{L} = 40$$

$$W = 40 \times 0.18 = 7.2 \ \mu\text{m}$$

5.50 Refer to Fig. P5.50. Both Q_1 and Q_2 are operating in saturation at $I_D = 0.5$ mA. For Q_1,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W_1}{L_1} V_{OV1}^2$$

$$0.5 = \frac{1}{2} \times 0.25 \times \frac{W_1}{L_1} (1 - 0.5)^2$$

$$\Rightarrow \frac{W_1}{L_1} = 16$$

$$W_1 = 16 \times 0.25 = 4 \ \mu\text{m}$$

For Q_2, we have

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W_2}{L_2} \right) V_{OV2}^2$$

$$0.5 = \frac{1}{2} \times 0.25 \times \frac{W_2}{L_2} (1.8 - 1 - 0.5)^2$$

$$\Rightarrow \frac{W_2}{L_2} = 44.4$$

$$W_2 = 44.4 \times 0.25 = 11.1$$

$$R = \frac{2.5 - 1.8}{0.5} = 1.4 \text{ k}\Omega$$

5.51 Refer to the circuit in Fig. P5.51. All three transistors are operating in saturation with $I_D = 90\ \mu\text{A}$. For Q_1,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1}\ (V_{GS1} - V_t)^2$$

$$90 = \frac{1}{2} \times 90 \times \frac{W_1}{L_1}(0.8 - 0.5)^2$$

$$\Rightarrow \frac{W_1}{L_1} = 22.2$$

$$W_1 = 22.2 \times 0.5 = 11.1\ \mu\text{m}$$

For Q_2,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2}\ (V_{GS2} - V_t)^2$$

$$90 = \frac{1}{2} \times 90 \times \frac{W_2}{L_2}(1.5 - 0.8 - 0.5)^2$$

$$\Rightarrow \frac{W_2}{L_2} = 50$$

$$W_2 = 50 \times 0.5 = 25\ \mu\text{m}$$

For Q_3,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W_3}{L_3}\ (V_{GS3} - V_t)^2$$

$$90 = \frac{1}{2} \times 90 \times \frac{W_3}{L_3}(2.5 - 1.5 - 0.5)^2$$

$$\Rightarrow \frac{W_3}{L_3} = 8$$

$$W_3 = 8 \times 0.5 = 4\ \mu\text{m}$$

5.52 Refer to the circuits in Fig. 5.24 (page 282):

$$V_{GS} = 5 - 6I_D$$

$$I_D = \frac{1}{2}k_n'\frac{W}{L}\ (V_{GS} - V_t)^2$$

$$= \frac{1}{2} \times 1.5 \times (5 - 6I_D - 1.5)^2$$

which results in the following quadratic equation in I_D:

$$36I_D^2 - 43.33I_D + 12.25 = 0$$

The physically meaningful root is

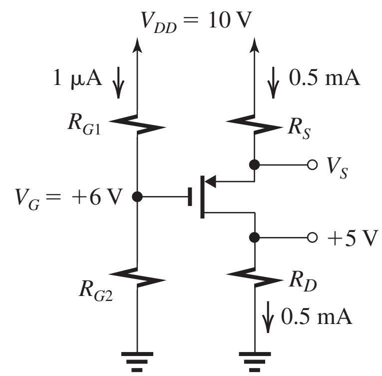
$$I_D = 0.45 \text{ mA}$$

This should be compared to the value of 0.5 mA found in Example 5.6. The difference of about 10% is relatively small, given the large variations in k_n and V_t (50% increase in each). The new value of V_D is

$$V_D = V_{DD} - R_D I_D = 10 - 6 \times 0.45 = +7.3 \text{ V}$$

as compared to +7 V found in Example 5.6. We conclude that this circuit is quite tolerant to variations in device parameters.

5.53



Refer to the circuit in the figure above,

$$R_{G1} = \frac{V_{DD} - V_G}{1\ \mu\text{A}}$$

$$= \frac{10 - 6}{1} = 4 \text{ M}\Omega$$

$$R_{G2} = \frac{6}{1\ \mu\text{A}} = 6 \text{ M}\Omega$$

$$R_D = \frac{5 \text{ V}}{0.5 \text{ mA}} = 10 \text{ k}\Omega$$

To determine V_S, we use

$$I_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)(V_{SG} - |V_t|)^2$$

$$0.5 = \frac{1}{2} \times 4 \times (V_{SG} - 1.5)^2$$

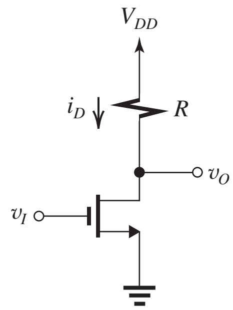
$$\Rightarrow V_{SG} = 2 \text{ V}$$

Thus,

$$V_S = V_G + V_{SG} = 6 + 2 = 8 \text{ V}$$

$$R_S = \frac{10 - 8}{0.5} = 4 \text{ k}\Omega$$

5.54



Assuming linear operation in the triode region, we can write

$$i_D = \frac{v_O}{r_{DS}} = \frac{50\ \text{mV}}{50\ \Omega} = 1\ \text{mA}$$

$$i_D = k_n'\left(\frac{W}{L}\right)(v_{GS} - V_t)v_{DS}$$

$$1 = 0.5 \times \frac{W}{L} \times (1.3 - 0.4) \times 0.05$$

$$\Rightarrow \frac{W}{L} = 44.4$$

$$R = \frac{V_{DD} - v_O}{i_D} = \frac{1.3 - 0.05}{1}$$

$$= 1.25\ \text{k}\Omega$$

5.55 (a) Refer to Fig. P5.55(a): Assuming saturation-mode operation, we have

$$I_D = \frac{1}{2}k_n V_{OV}^2$$

$$2 = \frac{1}{2} \times 4\ V_{OV}^2$$

$$\Rightarrow V_{OV} = 1\ \text{V}$$

$$V_{GS} = |V_t| + V_{OV} = 1 + 1 = 2\ \text{V}$$

$$V_1 = 0 - V_{GS} = -2\ \text{V}$$

$$V_2 = 5 - 2 \times 2 = +1\ \text{V}$$

Since $V_{DG} = +1$ V, the MOSFET is indeed in saturation.

Refer to Fig. P5.55(b): The transistor is operating in saturation, thus

$$I_D = \frac{1}{2}k_n V_{OV}^2$$

$$2 = \frac{1}{2} \times 4 \times V_{OV}^2 \Rightarrow V_{OV} = 1\ \text{V}$$

$$V_{GS} = 2\ \text{V}$$

$$\Rightarrow V_3 = 2\ \text{V}$$

Refer to Fig. P5.55(c): Assuming saturation-mode operation, we have

$$I_D = \frac{1}{2}k_p |V_{OV}|^2$$

$$2 = \frac{1}{2} \times 4 \times |V_{OV}|^2$$

$$\Rightarrow |V_{OV}| = 1\ \text{V}$$

$$V_{SG} = |V_t| + |V_{OV}| = 1 + 1 = 2\ \text{V}$$

$$V_4 = V_{SG} = 2\ \text{V}$$

$$V_5 = -5 + I_D \times 1.5$$

$$= -5 + 2 \times 1.5 = -2\ \text{V}$$

Since $V_{DG} < 0$, the MOSFET is indeed in saturation.

Refer to Fig. P5.55(d): Both transistors are operating in saturation at equal $|V_{OV}|$. Thus

$$2 = \frac{1}{2} \times 4 \times |V_{OV}|^2 \ \Rightarrow |V_{OV}| = 1\ \text{V}$$

$$V_{SG} = |V_t| + |V_{OV}| = 2\ \text{V}$$

$$V_6 = 5 - V_{SG} = 5 - 2 = 3\ \text{V}$$

$$V_7 = +5 - 2\ V_{SG} = 5 - 2 \times 2 = 1\ \text{V}$$

(b) Circuit (a): The 2-mA current source can be replaced with a resistance R connected between the MOSFET source and the −5-V supply with

$$R = \frac{V_1 - (-5)}{2\ \text{mA}} = \frac{-2 + 5}{2} = 1.5\ \text{k}\Omega$$

Circuit (b): The 2-mA current source can be replaced with a resistance R,

$$R = \frac{5 - V_3}{2\ \text{mA}} = \frac{5 - 2}{2} = 1.5\ \text{k}\Omega$$

Circuit (c): The 2-mA current source can be replaced with a resistance R,

$$R = \frac{5 - V_4}{2\ \text{mA}} = \frac{5 - 2}{2} = 1.5\ \text{k}\Omega$$

Circuit (d): The 2-mA current source can be replaced with a resistance R,

$$R = \frac{V_7}{2\ \text{mA}} = \frac{1}{2} = 0.5\ \text{k}\Omega$$

We use the nearest 1% resistor, which is 499 Ω.

5.56 (a) Refer to Fig. P5.56(a): The MOSFET is operating in saturation. Thus

$$I_D = \frac{1}{2}k_n V_{OV}^2$$

$$10 = \frac{1}{2} \times 500 \times V_{OV}^2 \Rightarrow V_{OV} = 0.2\ \text{V}$$

$$V_{GS} = V_t + V_{OV} = 0.8 + 0.2 = 1\ \text{V}$$

$$V_1 = 0 - V_{GS} = -1\ \text{V}$$

(b) Refer to Fig. P5.56(b): The MOSFET is operating in saturation. Thus

$$100 = \frac{1}{2} \times 500 \times V_{OV}^2 \Rightarrow V_{OV} = 0.63 \text{ V}$$

$$V_{GS} = 0.8 + 0.63 = 1.43 \text{ V}$$

$$V_2 = -1.43 \text{ V}$$

(c) Refer to Fig. P5.56(c). The MOSFET is operating in saturation. Thus

$$1 = \frac{1}{2} \times 0.5 \times V_{OV}^2 \Rightarrow V_{OV} = 2 \text{ V}$$

$$V_{GS} = 0.8 + 2 = 2.8 \text{ V}$$

$$V_3 = -2.8 \text{ V}$$

(d) Refer to Fig. P5.56(d). The MOSFET is operating in saturation. Thus

$$10 = \frac{1}{2} \times 500 \times V_{OV}^2 \Rightarrow V_{OV} = 0.2 \text{ V}$$

$$V_{GS} = 0.8 + 0.2 = 1 \text{ V}$$

$$V_4 = 1 \text{ V}$$

(e) Refer to Fig. P5.56(e). The MOSFET is operating in saturation. Thus

$$1 = \frac{1}{2} \times 0.5 \times V_{OV}^2 \Rightarrow V_{OV} = 2 \text{ V}$$

$$V_{GS} = 0.8 + 2 = 2.8 \text{ V}$$

$$V_5 = V_{GS} = 2.8 \text{ V}$$

(f) Refer to Fig. P5.56(f). To simplify our solution, we observe that this circuit is that in Fig. P5.56(d) with the 10-μA current source replaced with a 400-kΩ resistor. Thus $V_G = V_4 = +1$ V and, as a check, $I_D = \dfrac{5-1}{400} = 0.01 \text{ mA} = 10\ \mu\text{A}$.

(g) Refer to Fig. P5.56(g). Our work is considerably simplified by observing that this circuit is similar to that in Fig. P5.56(e) with the 1-mA current source replaced with a 2.2-kΩ resistor. Thus $V_7 = V_5 = 2.8$ V and, as a check, $I_D = \dfrac{5-2.8}{2.2} = 1$ mA.

(h) Refer to Fig. P5.56(h). Our work is considerably simplified by observing that this circuit is similar to that in Fig. P5.56(a) with the 10-μA current source replaced with a 400-kΩ resistor. Thus $V_8 = V_1 = -1$ V and, as a check, $I_D = \dfrac{-1+5}{400} = 0.01 \text{ mA} = 10\ \mu\text{A}$.

5.57 (a) Refer to the circuit in Fig. P5.57(a). Transistor Q_1 is operating in saturation. Assume that Q_2 also is operating in saturation,

$$V_{GS2} = 0 - V_2 = -V_2$$

and

$$V_2 = -2.5 + I_D \times 1$$

$$\Rightarrow I_D = V_2 + 2.5$$

Now,

$$I_D = \frac{1}{2} k_n (V_{GS2} - V_t)^2$$

Substituting $I_D = V_2 + 2.5$ and $V_{GS2} = -V_2$,

$$V_2 + 2.5 = \frac{1}{2} \times 1.5(-V_2 - 0.9)^2$$

$$\frac{2}{1.5}(V_2 + 2.5) = V_2^2 + 1.8\ V_2 + 0.81$$

$$V_2^2 + 0.467\ V_2 - 2.523 = 0$$

$$\Rightarrow V_2 = -1.84 \text{ V}$$

Thus,

$$I_D = V_2 + 2.5 = -1.84 + 2.5 = 0.66 \text{ mA}$$

and

$$V_{GS2} = 1.84 \text{ V}$$

Since Q_1 is identical to Q_2 and is conducting the same I_D, then

$$V_{GS1} = 1.84 \text{ V}$$

$$\Rightarrow V_1 = 2.5 - 1.84 = 0.66 \text{ V}$$

which confirms that Q_1 is operating in saturation, as assumed.

(b) Refer to the circuit in Fig. P5.57(b). From symmetry, we see that

$$V_4 = 2.5 \text{ V}$$

Now, compare the part of the circuit consisting of Q_2 and the 1-kΩ resistor. We observe the similarity of this part with the circuit between the gate of Q_2 and ground in Fig. P5.57(a). It follows that for the circuit in Fig. P5.57(b), we can use the solution of part (a) above to write

$$I_{D2} = 0.66 \text{ mA} \quad \text{and} \quad V_{GS2} = 1.84 \text{ V}$$

Thus,

$$V_5 = V_4 - V_{GS2} = 2.5 - 1.84 = 0.66 \text{ V}$$

Since Q_1 is conducting an equal I_D and has the same V_{GS},

$$I_{D1} = 0.66 \text{ mA} \quad \text{and} \quad V_{GS1} = 1.84 \text{ V}$$

$$\Rightarrow V_3 = V_4 + V_{GS1} = 2.5 + 1.84 = 3.34 \text{ V}$$

We could, of course, have used the circuit symmetry, observed earlier, to write this final result.

5.58

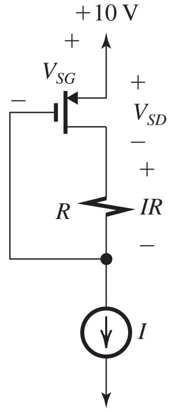


Fig. 1

(a) From Fig. 1 we see that

$V_{DG} = IR$

Since for the PMOS transistor to operate in saturation,

$V_{DG} \leq |V_{tp}|$

It follows the

$IR \leq |V_{tp}|$ Q.E.D

(b) (i) $R = 0$, the condition above is satisfied and

$I_D = I = \frac{1}{2} k_p |V_{OV}|^2$

$0.1 = \frac{1}{2} \times 0.2 \times |V_{OV}|^2$

$\Rightarrow |V_{OV}| = 1$ V

$V_{SG} = |V_{tp}| + |V_{OV}| = 1 + 1 = 2$ V

$V_G = 10 - 2 = 8$ V

$V_D = V_G = 8$ V

$V_{SD} = 2$ V

(ii) $R = 10$ kΩ

$IR = 0.1 \times 10 = 1$ V

which just satisfies the condition for saturation-mode operation in (a) above. Obviously I_D and $|V_{OV}|$ will be the same as in (i) above.

$V_{SG} = 2$ V

$V_G = 8$ V

$V_D = V_G + IR = 8 + 1 = 9$ V

$V_{SD} = 1$ V

(iii) $R = 30$ kΩ

$IR = 0.1 \times 30 = 3$ V

which is greater than $|V_{tp}|$. Thus the condition in (a) above is not satisfied and the MOSFET is operating in the triode region. From Fig. 2,

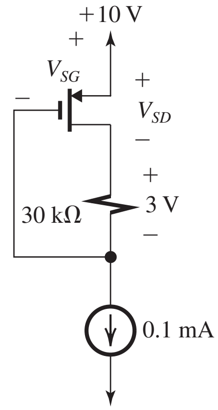


Fig. 2

From Fig. 2, we see that

$V_{SD} = V_{SG} - 3$

Now, for triode-mode operation,

$$I_D = k_p\left[(V_{SG} - |V_{tp}|)V_{SD} - \frac{1}{2}V_{SD}^2\right]$$

$$0.1 = 0.2\left[(V_{SG} - 1)(V_{SG} - 3) - \frac{1}{2}(V_{SG} - 3)^2\right]$$

$\Rightarrow V_{SG}^2 - 2V_{SG} - 4 = 0$

$\Rightarrow V_{SG} = 3.24$ V

$V_{SD} = V_{SG} - 3 = 0.24$ V

(iv) $R = 100$ kΩ

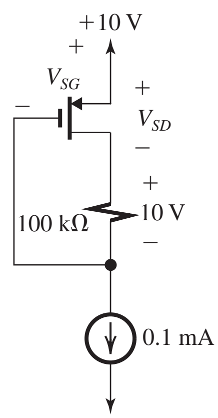


Fig. 3

Here also (see Fig. 3) the MOSFET will be operating in the triode region, and

$V_{SD} = V_{SG} - 10$ V

Since we expect V_{SD} to be very small, we can neglect the V_{SD}^2 term in the expression for I_D and write

$I_D \simeq k_p(V_{SG} - |V_t|)V_{SD}$

$0.1 = 0.2(V_{SG} - 1)(V_{SG} - 10)$

$\Rightarrow V_{SG}^2 - 11V_{SG} + 9.5 = 0$

$\Rightarrow V_{SG} = 10.055$ V

$V_{SD} = V_{SG} - 10 = 0.055$ V

5.59 (a) Refer to the circuit in Fig. P5.59(a). Since the two NMOS transistors are identical and have the same I_D, their V_{GS} values will be equal. Thus

$$V_{GS} = \frac{3}{2} = 1.5 \text{ V}$$

$V_2 = 1.5$ V

$V_{OV} = V_{GS} - V_t = 1.0$ V

$$I_1 = I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{OV}^2$$

$$= \frac{1}{2} \times 270 \times \frac{3}{1} \times 1$$

$= 405$ μA

(b) Refer to the circuit in Fig. P5.59(b). Here Q_N and Q_P have the same $I_D = I_3$. Thus

$$I_3 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{OVN}^2 \qquad (1)$$

$$I_3 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)V_{OVP}^2 \qquad (2)$$

Equating Eqs. (1) and (2) and using $\mu_n C_{ox} = 3\mu_p C_{ox}$ gives $3V_{OVN}^2 = V_{OVP}^2$:

$|V_{OVP}| = \sqrt{3}\, V_{OVN}$

Now,

$V_{GSN} = V_{OVN} + V_t = V_{OVN} + 0.5$

$V_{SGP} = |V_{OVP}| + |V_t| = \sqrt{3}\, V_{OVN} + 0.5$

But

$V_{SGP} + V_{GSN} = 3$

$(\sqrt{3} + 1)V_{OVN} + 1 = 3$

$\Rightarrow V_{OVN} = 0.732$ V

$V_{OVP} = 1.268$ V

$V_{GSN} = 1.232$ V

$V_{SGP} = 1.768$ V

$V_4 = V_{GSN} = 1.232$ V

$$I_3 = \frac{1}{2} \times 270 \times \frac{3}{1} \times 0.732^2 = 217 \text{ μA}$$

(c) Refer to Fig. P5.59(c). Here the width of the PMOS transistor is made 3 times larger than that of the NMOS transistor. This compensates for the factor 3 in the process transconductance parameter, resulting in $k_p = k_n$, and the two transistors are matched. The solution will be identical to that for (a) above with

$$V_5 = \frac{3}{2} = 1.5 \text{ V}$$

$I_6 = 405$ μA

5.60 Refer to the circuit in Fig. P5.60. First consider Q_1 and Q_2. Both are operating in saturation and since they are identical, they have equal V_{GS}:

$$V_{GS1} = V_{GS2} = \frac{5}{2} = 2.5 \text{ V}$$

Thus,

$$I_{D2} = I_{D1} = \frac{1}{2}\,\mu_n C_{ox}\frac{W}{L}(V_{GS1} - V_t)^2$$

$$= \frac{1}{2} \times 50 \times \frac{10}{1}(2.5 - 1)^2$$

$= 562.5$ μA

Now, Q_3 has the same V_{GS} at Q_1 and is matched to Q_1. Thus if we assume that Q_3 is operating in saturation, we have

$I_{D3} = I_{D1} = 562.5$ μA

Thus,

$I_2 = 562.5$ μA

This is the same current that flows through Q_4, which is operating in saturation and is matched to Q_3. Thus

$V_{GS4} = V_{GS3} = V_{GS1} = 2.5$ V

Thus,

$V_2 = 5 - V_{GS4} = 2.5$ V

This is equal to the voltage at the gate of Q_3; thus Q_3 is indeed operating in saturation, as assumed.

If Q_3 and Q_4 have $W = 100$ μm, nothing changes for Q_1 and Q_2. However, Q_3, which has the same V_{GS} as Q_1 but has 10 times the width, will have a drain current 10 times larger than Q_1.
Thus

$I_{D2} = I_{D3} = 10\, I_{D1} = 10 \times 562.5$ μA

$= 5.625$ mA

Transistor Q_4 will carry I_2 but will retain the same V_{GS} as before, thus V_2 remains unchanged at 2.5 V.

5.61 Refer to the circuit in Fig. P5.61.

(a) Q_1 and Q_2 are matched. Thus, from symmetry, we see that the 200-μA current will split equally between Q_1 and Q_2:

$I_{D1} = I_{D2} = 100\ \mu\text{A}$

$V_1 = V_2 = 2.5 - 0.1 \times 20 = 0.5\ \text{V}$

To find V_3, we determine V_{GS} of either Q_1 and Q_2 (which, of course, are equal),

$$I_{D1} = \frac{1}{2}\,\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_t)^2$$

$$100 = \frac{1}{2} \times 125 \times 20 \times (V_{GS} - 0.7)^2$$

$\Rightarrow V_{GS} = 0.983\ \text{V}$

Thus,

$V_3 = -0.983\ \text{V}$

(b) With $V_{GS1} = V_{GS2}$, but $(W/L)_1 = 1.5(W/L)_2$, transistor Q_1 will carry a current 1.5 times that in Q_2, that is,

$I_{D1} = 1.5 I_{D2}$

But,

$I_{D1} + I_{D2} = 200\ \mu\text{A}$

Thus

$I_{D1} = 120\ \mu\text{A}$

$I_{D2} = 80\ \mu\text{A}$

$V_1 = 2.5 - 0.12 \times 20 = 0.1\ \text{V}$

$V_2 = 2.5 - 0.08 \times 20 = 0.9\ \text{V}$

To find V_3, we find V_{GS} from the I_D equation for either Q_1 or Q_2,

$$I_{D1} = \frac{1}{2}\,\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_t)^2$$

$$120 = \frac{1}{2} \times 125 \times 20 \times (V_{GS} - 0.7)^2$$

$\Rightarrow V_{GS} = 1.01\ \text{V}$

$V_3 = -1.01\ \text{V}$

5.62 Using Eq. (5.30), we can write

$$V_t = V_{t0} + \gamma\,[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\,]$$

where

$V_{t0} = 1.0\ \text{V}$

$\gamma = 0.5\ \text{V}^{1/2}$

$2\phi_f = 0.6\ \text{V}$

and

$V_{SB} = 0$ to $4\ \text{V}$

At

$V_{SB} = 0, \quad V_t = V_{t0} = 1.0\ \text{V}$

At

$V_{SB} = 4\ \text{V}$,

$V_t = 1 + 0.5[\sqrt{0.6 + 4} - \sqrt{0.6}\,]$

$= 1.69\ \text{V}$

If the gate oxide thickness is increased by a factor of 4, C_{ox} will decrease by a factor of 4 and Eq. (5.31) indicates that γ will increase by a factor of 4, becoming 2. Thus at $V_{SB} = 4\ \text{V}$,

$V_t = 1 + 2[\sqrt{0.6 + 4} - \sqrt{0.6}\,]$

$= 3.74\ \text{V}$

5.63 $|V_t| = |V_{t0}| + \gamma\left[\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f}\right]$

$= 0.7 + 0.5[\sqrt{0.75 + 3} - \sqrt{0.75}\,]$

$= 1.24\ \text{V}$

Thus,

$V_t = -1.24\ \text{V}$

5.64 (a) $i_D = \dfrac{1}{2} k_n'\left(\dfrac{W}{L}\right)(v_{GS} - V_t)^2$

$$\frac{\partial i_D}{\partial T} = \frac{1}{2}\,\frac{\partial k_n'}{\partial T}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2$$

$$-k_n'\left(\frac{W}{L}\right)(v_{GS} - V_t)\frac{\partial V_t}{\partial T}$$

$$\frac{\partial i_D/i_D}{\partial T} = \frac{\partial k_n'/k_n'}{\partial T} - \frac{2}{V_{GS} - V_t}\ \frac{\partial V_t}{\partial T}$$

For

$$\frac{\partial V_t}{\partial T} = -2\ \text{mV/°C} = -0.002\ \text{V/°C}$$

and

$$\frac{\partial i_D/i_D}{\partial T} = -0.002/\text{°C},\ V_{GS} = 5\ \text{V}$$

and

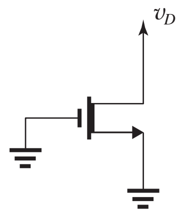
$V_t = 1\ \text{V}$

$$-0.002 = \frac{\partial k_n'/k_n'}{\partial T} - \frac{2 \times -0.002}{5 - 1}$$

$$\Rightarrow \frac{\partial k_n'/k_n'}{\partial T} = -0.003/\text{°C}$$

or $-0.3\%/\text{°C}$

5.65



The NMOS depletion-type MOSFET has the same $i-v$ characteristics as the enhancement-type NMOS except that V_{tn} is negative, for the depletion device:

$$i_D = k_n\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right], \quad \text{for } v_{DS} \leq v_{GS} - V_{tn}$$

$$i_D = \frac{1}{2}k_n(v_{GS} - V_{tn})^2,$$

for $v_{DS} \geq v_{GS} - V_{tn}$

For our case, $v_{GS} = 0$, $V_{tn} = -3$ V, and $k_n = 2$ mA/V^2. Thus

$$i_D = 2\left(3v_D - \frac{1}{2}v_D^2\right), \quad \text{for } v_D \leq 3 \text{ V}$$

$$i_D = \frac{1}{2} \times 2 \times 9 = 9 \text{ mA}, \quad \text{for } v_D \geq 3 \text{ V}$$

For

$$v_D = 0.1 \text{ V}, \quad i_D = 2\left(3 \times 0.1 - \frac{1}{2} \times 0.1^2\right)$$
$= 0.59$ mA (triode)

For

$$v_D = 1 \text{ V}, \quad i_D = 2\left(3 \times 1 - \frac{1}{2} \times 1\right)$$
$=5$ mA (triode)

For

$v_D = 3$ V, $\quad i_D = 9$ mA (saturation)

For

$v_D = 5$ V, $\quad i_D = 9$ mA (saturation)

5.66 $i_D = k_n\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$,
for $v_{DS} \leq v_{GS} - V_{tn}$

$$i_D = \frac{1}{2}k_n(v_{GS} - V_{tn})^2(1 + \lambda\, v_{DS}),$$
for $v_{DS} \geq v_{GS} - V_{tn}$

For our case,

$V_{tn} = -2$ V, $k_n = 0.2$ mA/V^2, $\lambda = 0.02$ V^{-1}

and $v_{GS} = 0$. Thus

$$i_D = 0.2\left(2\, v_{DS} - \frac{1}{2}v_{DS}^2\right), \quad \text{for } v_{DS} \leq 2 \text{ V}$$

$$i_D = 0.4(1 + 0.02\, v_{DS}), \quad \text{for } v_{DS} \geq 2 \text{ V}$$

For $v_{DS} = 1$ V,

$$i_D = 0.2\left(2 - \frac{1}{2}\right) = 0.3 \text{ mA}$$

For $v_{DS} = 2$ V,

$$i_D = 0.4(1 + 0.02 \times 2) = 0.416 \text{ mA}$$

For $v_{DS} = 3$ V,

$$i_D = 0.4(1 + 0.02 \times 3) = 0.424 \text{ mA}$$

For $v_{DS} = 10$ V,

$$i_D = 0.4(1 + 0.02 \times 10) = 0.48 \text{ mA}$$

If the device width W is doubled, k_n is doubled, and each of the currents above will be doubled. If both W and L are doubled, k_n remains unchanged. However, λ is divided in half; thus for $v_{DS} = 2$ V, i_D becomes 0.408 mA; for $v_{DS} = 3$ V, i_D becomes 0.412 mA; and for $v_{DS} = 10$ V, i_D becomes 0.44 mA.

5.67

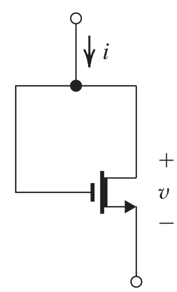


Fig. 1

The depletion-type MOSFET operates in the triode region when $v_{DS} \leq v_{GS} - V_t$: that is, $v_{DG} \leq -V_t$, where V_t is negative. In the case shown in Fig. 1, $v_{DG} = 0$. Thus the condition for triode-mode operation is satisfied, and

$$i_D = k_n\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

which applies when the channel is not depleted, that is, when $v_{GS} \geq V_t$. For our case,

$$i = k_n\left[(v - V_t)v - \frac{1}{2}v^2\right], \quad \text{for } v \geq V_t$$

Thus,

$$i = \frac{1}{2}k_n(v^2 - 2V_t v), \quad \text{for } v \geq V_t$$

For $v \leq V_t$, the source and the drain exchange roles, as indicated in Fig. 2.

Here $v_{GS} = 0$ and $v_{DS} = -v$; thus $v_{DS} \geq -V_t$. Thus the device is operating in saturation, and

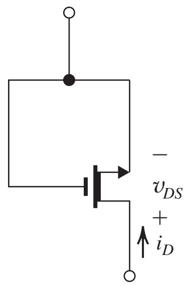


Fig. 2

$$i_D = \frac{1}{2}k_n(0 - V_t)^2$$

$$i_D = \frac{1}{2}k_n V_t^2$$

But $i = i_D$; thus

$$i = \frac{1}{2}k_n V_t^2, \quad \text{for} \quad v \leq V_t$$

Figure 3 is a sketch of the $i-v$ relationship for the case $V_t = -2$ V and $k_n = 2$ mA/V^2.

Here

$$i = v(v+4), \quad \text{for } v \geq -2 \text{ V}$$

and

$$i = -4 \text{ mA}, \quad \text{for } v \leq -2 \text{ V}$$

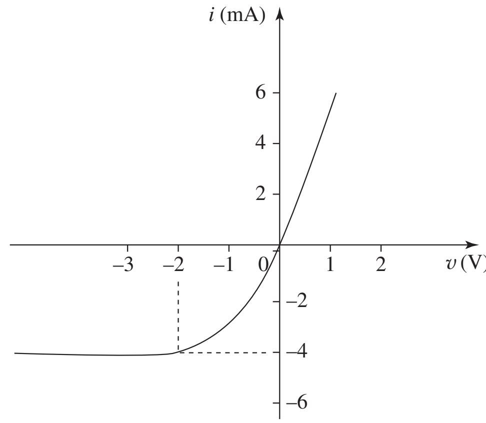


Fig. 3