

بِسْمِ اللّٰهِ الرَّحْمٰنِ الرَّحِيْمِ

# Electronics Theory

Trimester: Fall-2018

Faculty: Most Handsome, smart  
and Serious faculty  
(Abir Hasan)

[Lecturer, EEE dept.]

Prepared & Submitted by :

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9/10/11

\* electrical circuit deal w/ only conductor mat.

\* electronics circuit deal w/ only semiconductor mat.

④ Semiconductors (Advantages):

\* Property can be changed easily.

\* Resistivity decreases with increasing temperature.

Semiconductor: ~~more e- areas~~  $\rightarrow$  ~~more e-~~  $\rightarrow$  ~~more e-~~  $\rightarrow$  ~~more e-~~

$\hookrightarrow$  If more e- areas normally,

temp. fluct bond (e<sup>-</sup>) e<sup>-</sup> create e<sup>-</sup> e<sup>-</sup> nmb  
factors  $\rightarrow$   $\downarrow$  resistance or  $\downarrow$  resistance or  $\downarrow$

④ Semiconductors (Types):

{ Intrinsic sc (pure sc)

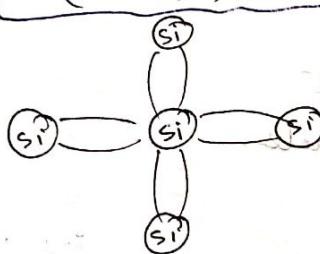
Extrinsic sc (from dopants), not 100% pure

{ P-type sc

n-type sc

Intrinsic sc:

[Si (former), Ge, Ga, GaAs (semiconductor)]

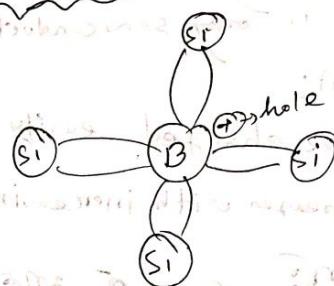


Last outer shell  $\rightarrow$  4 val. e<sup>-</sup> each  
of bonding e<sup>-</sup> share  
one oxygen, one oxygen, 8x  
one e<sup>-</sup> outer shell for

### Extrinsic:

P-type

B, As, At (boron, arsenic, antimony)



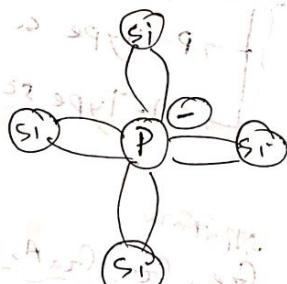
hole created  
last shell & 3rd  
like Boron, arsenic, antimony  
add dots  
P-type sc 22°.

nLLP

majority carriers  $\rightarrow$  hole  
minority carriers  $\rightarrow$   $e^-$

### n-type:

P  $\rightarrow$  n-inverter



$n \gg p$

majority carriers  $\rightarrow e^-$

minority carriers  $\rightarrow$  hole.

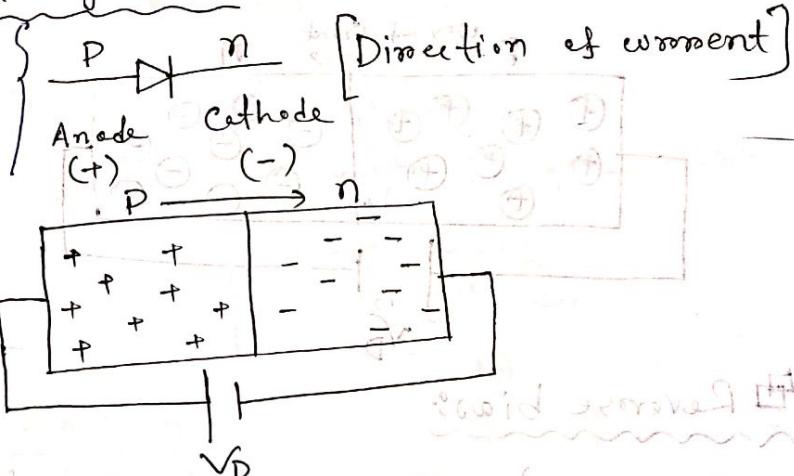
13/10/18

## \* P-n Junction

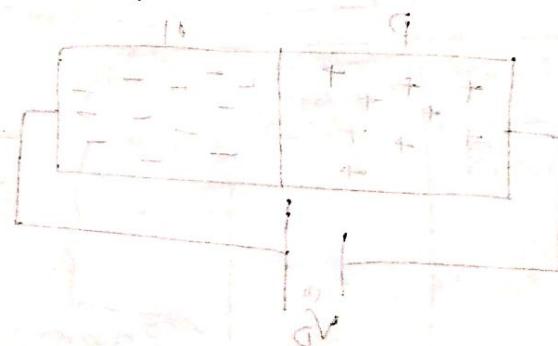


\* Current = flow of charge

\* Circuit symbol :-



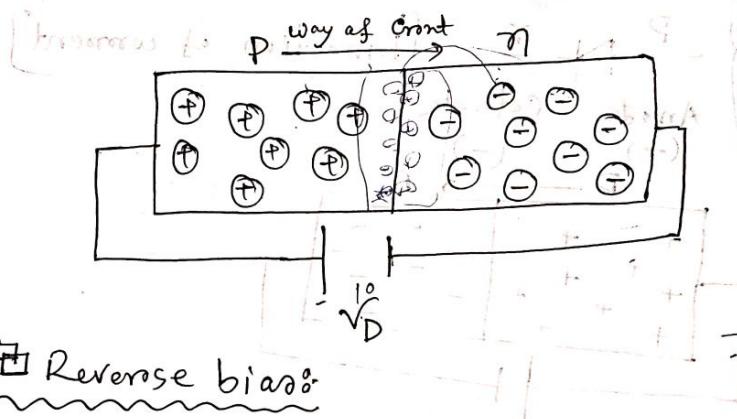
## \* Diode



P.T.O.

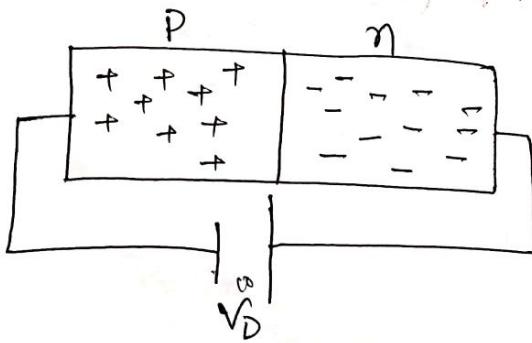
Forward bias

Forward bias  
+ charge दूषित संरचना परिवर्तन करते हुए current flow हो।  
अर्थात्, '+' ओर '-' ओर इनमें बीच में एक बिल्डिंग ड्रोप होता है।  
- ' ओर '-' ओर इनमें बीच में एक बिल्डिंग ड्रोप होता है।  
"forward bias."



Reverse bias

P sight  $t_1$  - R  $m_2$  zero in sight  $t_1 + t_2$   
smile zero in  $t_1$  -  $t_2$  reverse bias.



## Diode current:

$$I_S = I_D \text{ at } V_D = 0$$

$$I_D = I_S e^{\frac{V_D}{nV_T}}$$

$$V_T = \frac{kT_K}{q}$$

\* \* \* Forward bias  $\Rightarrow I_D = I_S e^{\frac{V_D}{nV_T}} = I_F$ .

\* \* \* Reverse bias,  $I_D = I_R = -I_S$

Hence,

\*  $V_T = \text{Thermal Voltage} = \frac{kT_K}{q}$

\*  $n = \text{ideality factor}$

\*  $I_S = \text{reverse saturation current.}$

$T \rightarrow \text{Temperature}$   
 $k \rightarrow \text{Boltzmann constant}$

$$= 1.38 \times 10^{-23} \text{ J K}^{-1}$$

$\downarrow$  Kelvin  
 $\downarrow$  Joule

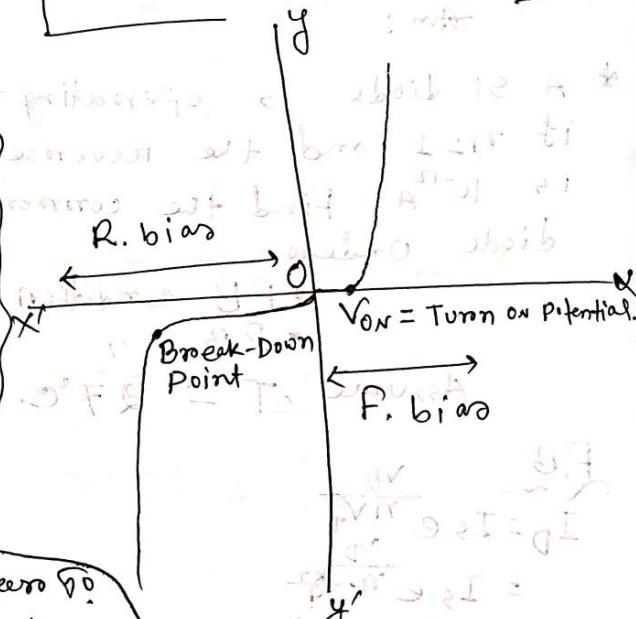
$q \rightarrow \text{charge of one } e^-$   
 $= 1.6 \times 10^{-19} \text{ C}$

## Forward bias:

if  $(V_D \geq 0)$

$$I_F = I_D = I_S e^{\frac{V_D}{nV_T}}$$

Condition  $(V_D \geq V_{ON})$



## Reverse bias:

if  $(V_D < 0)$

$$I_D = -I_S$$

R. bias & minority carrier flow  $\Rightarrow$  Current flow  $\approx 0$ .

Flow  $\approx 10^{-9} - 10^{-5} \text{ A}$  Current flow  $\approx 0$ .

N.B. earth  $\oplus$  centers Positive charge  
 earth  $\ominus$  surface negative "  
 whole earth neutral"

\* Calculate the thermal voltage of a Si-diode at  $27^\circ\text{C}$ .

$$V_T = \frac{kT}{q} = \frac{1.38 \times 10^{-3} \text{ J/K} \times 27 + 273}{1.6 \times 10^{-19} \text{ C}}$$

$$= 0.025 \text{ V}$$

$T = \text{Temperature}$

$k = \text{Boltzmann constant}$

$$= 1.38 \times 10^{-3} \text{ J/K} \quad \text{at } 27^\circ\text{C}$$

$$q = e^{-\text{e.s.d. charge}} = 1.6 \times 10^{-19} \text{ C}$$

\* A Si diode is operating at ~~reverse bias~~  $0.7 \text{ V}$ . If  $n=1$  and the reverse saturation current is  $10^{-12} \text{ A}$ , find the current through the diode under -

• F.B. condition

• R.B. "

Assume,  $T = 27^\circ\text{C}$ .

F.B.

$$I_D = I_s e^{\frac{V_D}{nV_T}}$$

$$= I_s e^{\frac{0.7}{1.6 \times 10^{-19}}}$$

$$= 10^{-12} \cdot e^{\frac{0.7}{1.6 \times 10^{-19}}}$$

$$=$$

R.B.

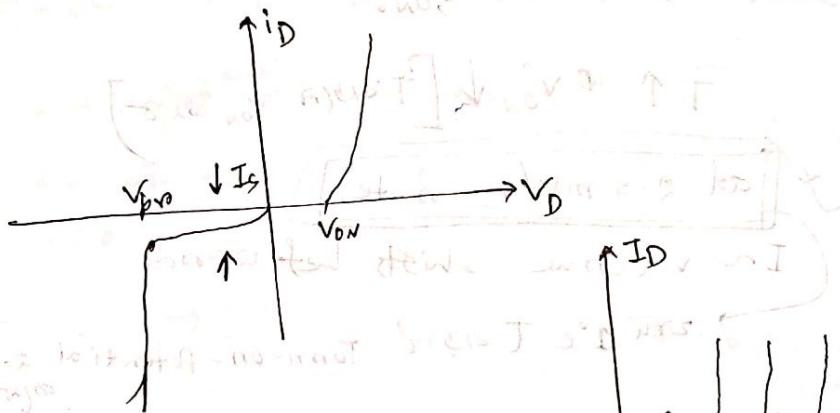
$$I_D = -I_s$$

$$= -10^{-12} \text{ A}$$

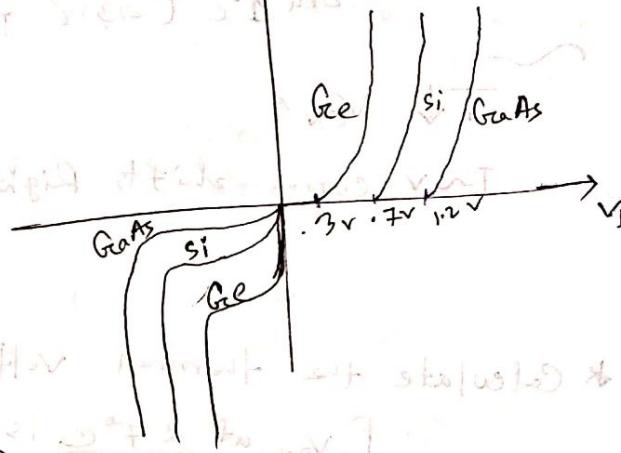
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3rd class

Q1 I-v curve of diode:



Q2 Si, Ge, GaAs:



$V_{ON}$

$$\begin{cases} \text{Ge} \rightarrow 0.3 \text{ V} \\ \text{Si} \rightarrow 0.7 \text{ V} \\ \text{GaAs} \rightarrow 1.2 \text{ V} \end{cases}$$

Turn-on potential  $\text{GaAs} > \text{Si} > \text{Ge}$

Turn-on-potential:  $\text{GaAs} > \text{Si} > \text{Ge}$ .

\* Reverse saturation current,  $I_s$ :  $\text{Ge} > \text{Si} > \text{GaAs}$

\*  $\approx$  2nd turn-on potential (error, or? reverse saturation current error)

- \* Impact of Temperature is at  $I \sim V$  curve.
- \* For Forward bias:

Effect of  $T$  on  $V_{ON}$ :

$$T \uparrow \propto V_{ON} \downarrow [T \text{ increases } V_{ON} \text{ decreases}]$$

at  $2.5 \text{ mV/}^{\circ}\text{C}$  rate,

$I \sim V$  curve shifts Leftward.

$\rightarrow$   $1^{\circ}\text{C} T \text{ increase} \rightarrow$  Turn-on-potential  $2.5 \text{ mV}$

$T \downarrow V_{ON} \uparrow$

$I \sim V$  curve shifts Rightward.

- \* Calculate the thermal voltage of  $\text{Ge}$  at  $30^{\circ}\text{C}$ .

$[V_{ON} \text{ at } 27^{\circ}\text{C} \text{ is } 0.3\text{V}]$

Ans:  $3 \times 2.5 \times 10^{-3} \text{ V}$

$0.3 - 3 \times 2.5 \times 10^{-3} \text{ V}$ ,

$\hookrightarrow$  Change of  $T$ . On Potential.

$2.5 \times 10^{-3}$

\*  $T = 10^\circ\text{C}$  2nd part 2nd QD Si Ge  
Tunnel potential  $\approx 7\text{V}$ ?

$$\begin{aligned} & \cdot 7 + \left( \cancel{\frac{2.5 \times 10 \times 10^{-3}}{10}} \right) (2.5 \times 10 \times 10^{-3}) \\ & = \cdot 7 + \cancel{0.25} \quad 2.5 \times 10^{-2} \\ & = \cdot 7.25 \text{ V.} \end{aligned}$$

$$\frac{2.5}{1000} = 0.025$$

$$\begin{aligned} & \xrightarrow{\text{on}} \quad 10^\circ\text{C} \longrightarrow 2.5 \times 10^{-3} \times 10 \\ & \qquad \qquad \qquad = 2.5 \times 10^{-2} \\ & \cdot 7 + 0.025 \\ & = 7.25 \text{ V.} \end{aligned}$$

\* effect of temp on  $I_s$  (reverse saturation)

$I_s$  doubles per  $10^\circ\text{C}$  rise in temp.  
 mean: temp  $10^\circ\text{C}$  more QD  $I_s$  double  $26^\circ\text{C}$ .

Ex: at  $10^\circ\text{C} \rightarrow I_s = 1 \text{ PA}$ .

at  $40^\circ\text{C} \rightarrow I_s = ?$

An:

$10^\circ\text{C} \rightarrow 1 \text{ PA}$

$20^\circ\text{C} \rightarrow 2 \text{ PA}$

$30^\circ\text{C} \rightarrow 4 \text{ PA}$

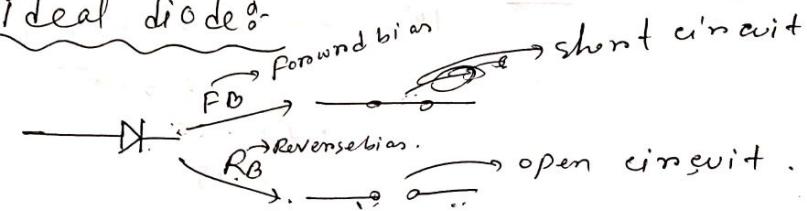
$40^\circ\text{C} \rightarrow 8 \text{ PA}$ .

Chptrn - 1

1.2, 1.5, 1.6, article अस्ति प्रमाण वर्गी

## Chptrn - 2

Ideal diode :-

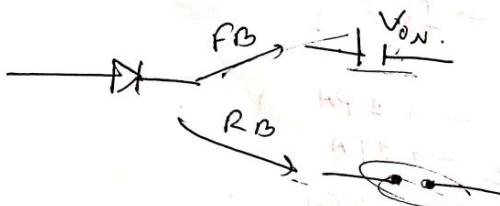


\* ideal diod F.B & short circuit फॉर्मोर्मेन

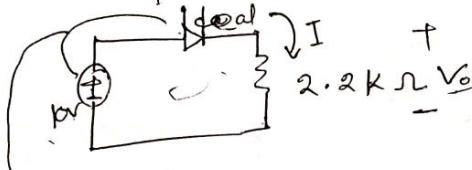
\* " " " R.B ", open "

Semi conductor diode:

F.B & ~~V<sub>on</sub>~~ V<sub>on</sub>.



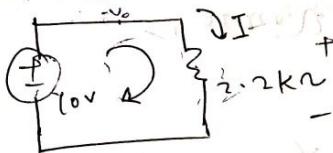
\* Find  $V_o$  &  $I$



$\rightarrow +, +$  terminal.

$\therefore$  get F. bias.

$\therefore$  get ideal diode,  $\therefore$  short circuit  $V_D$ .



$$V_o - 10 = 0$$

$$\Rightarrow V_o = 10V.$$

error:  $\checkmark$  Parallel & same

$$\therefore V_o = 10V$$

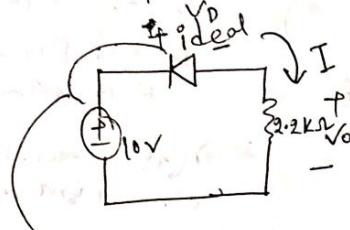
$$I = \frac{V_o}{R} = \frac{10}{2.2} = 4.5 \text{ mA.}$$

$$V_D = i R$$

$$= 4.5 \text{ mA} \times 0$$

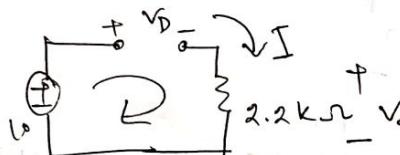
$$= 0V.$$

\* Find the  $V_o$  &  $I$



As +, - Gmnr connected!  
∴ get reverse bias.

∴ GTR open circuit  $\text{v}_o = 0$ ,



$$I = 0$$

$$V_o = IR$$

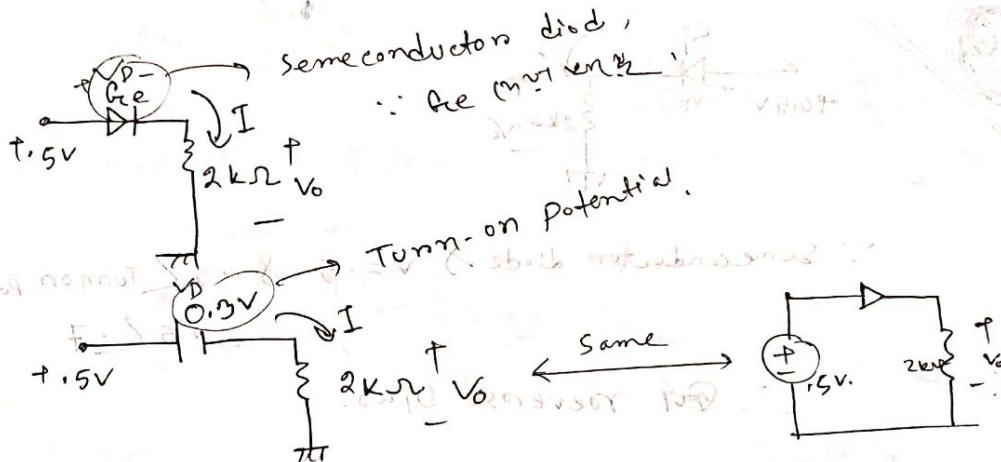
$$\therefore V_o = 0 \text{ V}$$

KVL

$$V_D + V_o = -10$$

$$\Rightarrow V_D = -10$$

\* Find  $V_o$  &  $I, V_D$



Apply kvl:  $-0.5 + 0.3 + V_o = 0$

$$\Rightarrow V_o = 0.2 \text{ V.}$$

$$I = \frac{V_o}{R} = \frac{0.2}{2k\Omega} = 0.1 \text{ mA.}$$

$$V_D = 0.3 \text{ V.}$$

$$V_D = 0.3 \text{ V.}$$

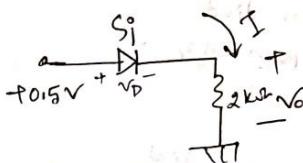
Now calculate  $V_o$ .

Method of solution:

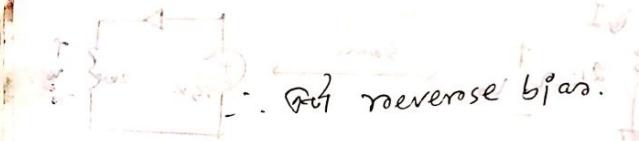
1. Calculate  $V_o$  at  $I = 0$

2. Calculate  $V_o$  at  $I = I_{max}$

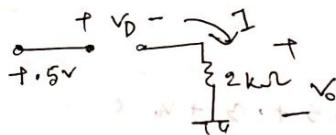
\* Find  $V_o$ ,  $I$ ,  $v_d$



$\therefore$  Semiconductor diode  $\delta v = .5 \text{ } \delta .5 \angle \text{Turn on Potential}$



$\therefore$  But reverse bias.



$$I = 0,$$

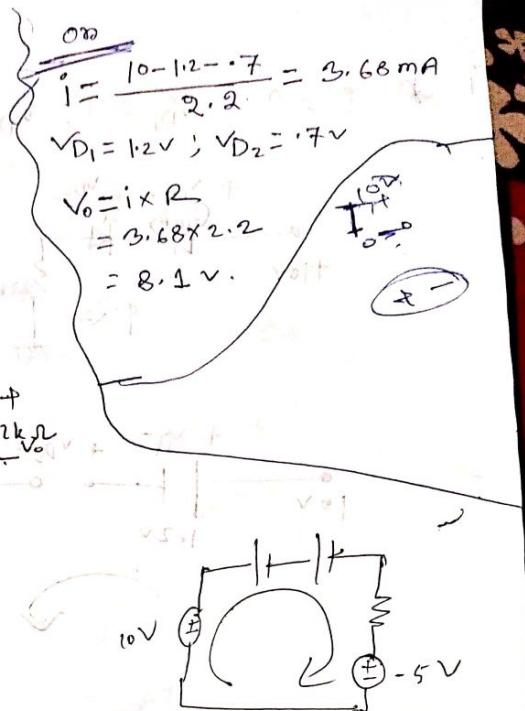
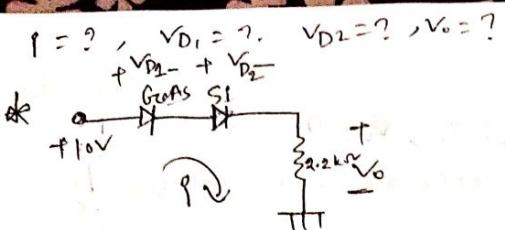
$$V_o = IR = 0.$$

kVL:

$$-.5 + V_D + V_o = 0$$

$$\Rightarrow V_D = 0.5\text{V.}$$

An.



$$\therefore V_{D_1} = 1.2V$$

$$I_{D_2} = 0.7V$$

KVL:  $-10 + 1.2 + 0.7 + V_o = 0 \Rightarrow -10 + V_{D_1} + V_{D_2} + (-5) = 0$

$$\Rightarrow V_o = 8.1V$$

$$I = \frac{V_o}{R} = \frac{8.1}{2.2} \text{ mA} = 3.68 \text{ mA}$$

Jewayriyya Sahab suha

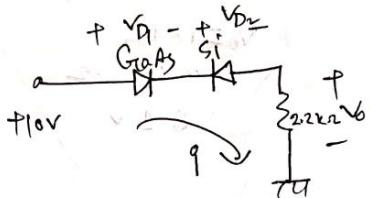
Dob: 06-06-2018

Mohammad sahabuddin

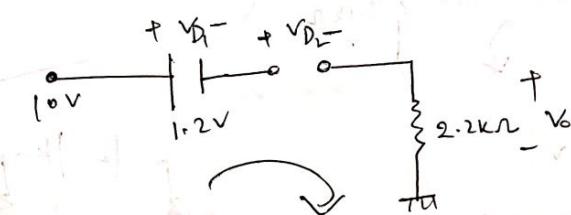
Nishat minira Zia

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$$i \neq 0 = ?, V_{D_1} = ?, V_{D_2} = ?, V_o = ?$$



$$x - (-5) = 7 \\ n = 7 - 5$$



$$V_{D_1} = 1.2V$$

$$i = 0 \text{ [As open circuit]} \quad V_{D_1} = 1.2V$$

$$V_o = i \times R \quad \frac{10}{2.2k\Omega} = \frac{10}{2.2} = 5V$$

KVL:

$$-10 + 1.2 + V_{D_2} + 0 = 0$$

$$\Rightarrow V_{D_2} = 8.8V$$

Ans:

22/10/18 (Shojeet Sin)

## Shojeet Sin

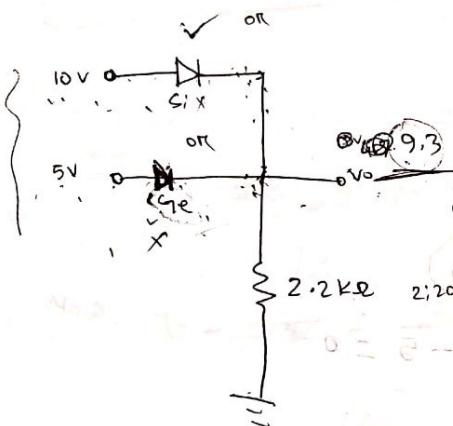
① Diode - on-off chk.

② diod के दो अन्य वितर फैसला.

③ P और n अंगू

\* ideal diod <sup>model</sup> analysis. - ?

(virtual & actual,  
voltage = ?)



$$i = 4.279 \times 10^3 A$$

$$\frac{9.3 - 0}{2200}$$

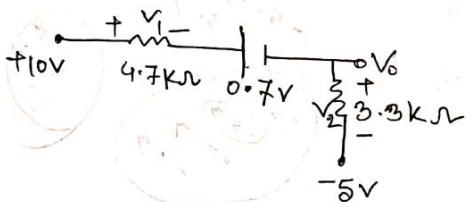
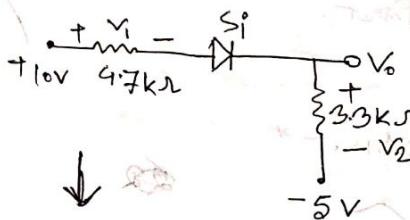
$$8 = 5.0 \times 8.71 = 41.5 V$$

$$8.2 = 5.0 \times 8.4 = 41.5 V$$

ID vs D

20/10/18

Find  $V_1, V_2, V_o$  &  $I$



$$-10 + V_1 + 6.7 + V_2 + (-5) = 0$$

$$\Rightarrow -10 + 4.7I + 0.7 + 3.3I - 5 = 0$$

$$\Rightarrow I = 1.78 \text{ mA}$$

$$V_1 = IR = 1.78 \times 4.7 = 8.36 \text{ V}$$

$$V_2 = IR = 3.3 \times 1.78 = 5.87 \text{ V}$$

Now,

$$V_2 = V_o - (-5)$$

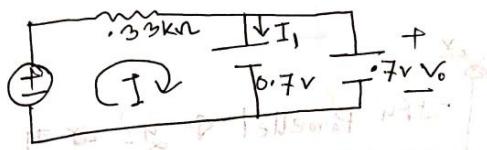
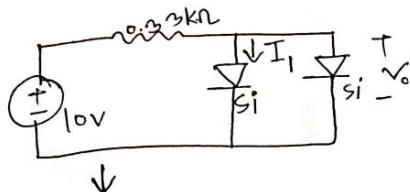
$$V_o = V_2 - 5$$

$$= 0.87 \text{ V.}$$

$\therefore V = V_a - V_b$

-on:

$$V_o = ? , I_1 = ?$$



$$-10 + 0.33 \times I + 0.7 = 0$$

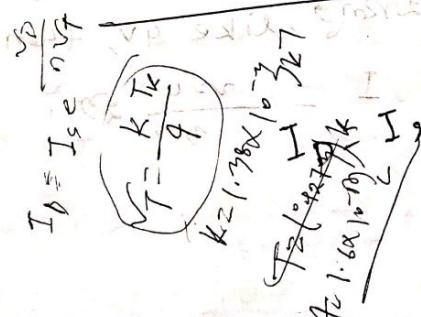
$$\Rightarrow I = 28.18 \text{ mA}$$

$$V_o = 0.7V$$

$$\text{Now, } I_F = \frac{I}{2} = \frac{28.18}{2}$$

Ans:

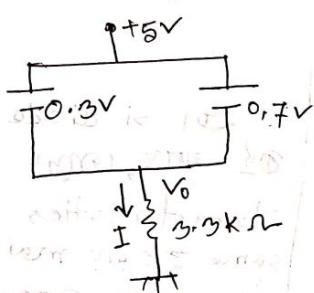
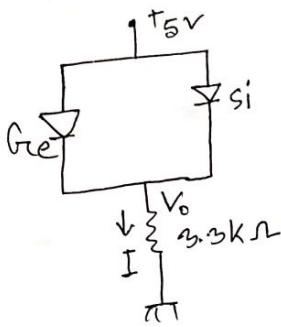
বি. ২/১ si diode Parallel  
কু আরে, গোলু উভয়ের  
characteristics ও সমান  
same ক্ষেত্রে main current  
কু একেই ক্ষেত্রে  
প্রত্যেক-প্রত্যেক ২ side দ- ঘূর্ব



$$V_T = \frac{kT}{q} = \frac{1.38 \times 10^{-23} \times 290}{1.6 \times 10^{-19}}$$

$$I_D = I_S e^{\frac{V_D}{V_T}} = 1.6 \times 10^{-19}$$

at  $V_o = ?$ ,  $I = ?$



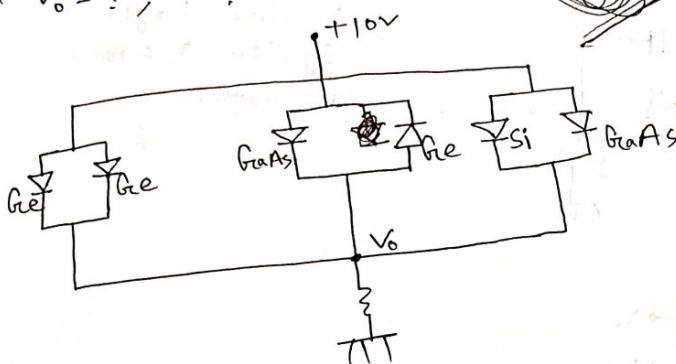
$$[ \text{Given } V = 5V ] \quad V_o = 4.7V \quad [ \because 5 - 0.3 = 4.7 ]$$

$$\begin{aligned} I &= \frac{V_o - 0}{3.3k\Omega} \\ &= \frac{4.7}{3.3k\Omega} \end{aligned}$$

An.  $\approx 1.4mA$

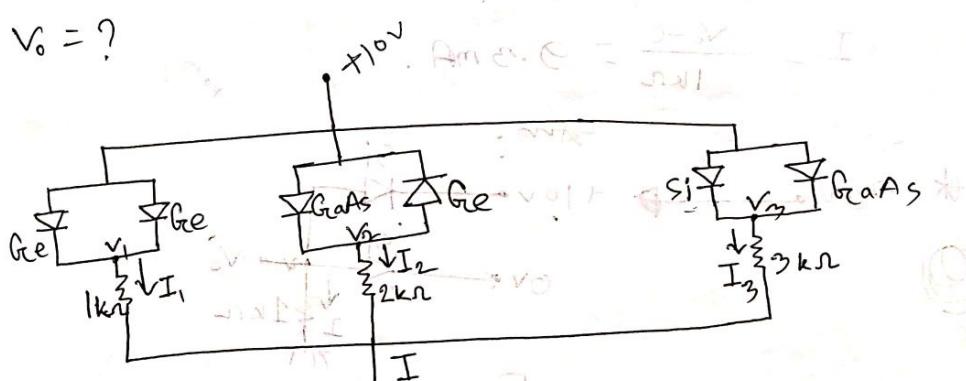
~~Transistor 2N3904  
at 2V300mV  
like 4V, then  
 $I = \frac{4V}{3.3k\Omega}$~~

\*  $V_o = ?$ ,  $I = ?$



$$V_o = 10 - 0.7 = 9.7 \text{ V}$$

\*  $V_o = ?$



$$V_1 = 10 - 0.3 = 9.7 \text{ V}$$

$$V_2 = 10 - 1.2 = 8.8 \text{ V}$$

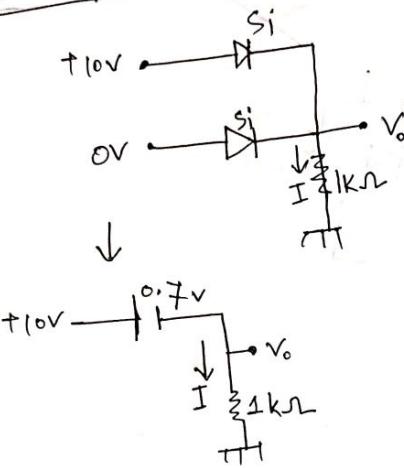
$$V_3 = 10 - 0.7 = 9.3 \text{ V}$$

$$I_1 = \frac{V_1 - 0}{1 \text{ k}\Omega}; I_2 = \frac{V_2 - 0}{2 \text{ k}\Omega} \Rightarrow I_2 = \frac{8.8 \text{ V}}{2 \text{ k}\Omega} = 4.4 \text{ mA}$$

$$I_3 = \frac{V_3 - 0}{3 \text{ k}\Omega} = \frac{9.3 \text{ V}}{3 \text{ k}\Omega} = 3.1 \text{ mA}$$

$$\therefore I = I_1 + I_2 + I_3$$

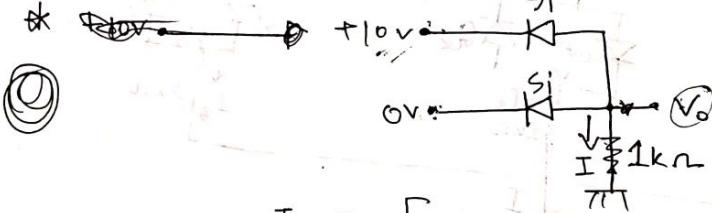
\* AND / OR Gate:



⇒ Positive logic  
System is OR  
Gate.

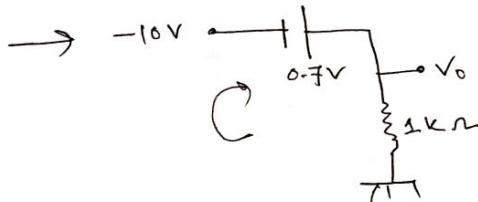
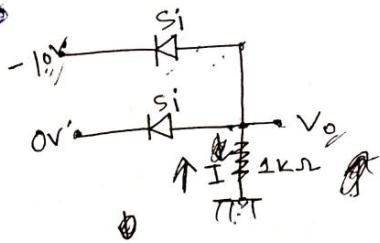
$$V_o = 10 - 0.7 = 9.3\text{V}$$

$$I = \frac{V_o - 0}{1\text{k}\Omega} = 9.3\text{mA}$$



$I = 0$   
 $V_o = 0$  [since negative side connected,  
+10V goes to ground, so current zero]

+10V current input ଯେଣ୍ଟିରୁଥିଲୁଛି, ତେଣୁ କାହାର  
Positive logic system. ଏହା ଏହା ଏହା ଏହା  
ଏହା ଏହା ଏହା ଏହା ଏହା ଏହା ଏହା  
ଏହା ଏହା ଏହା ଏହା ଏହା ଏହା ଏହା  
AND Gate.



$$0.7 = V_O - (-10)$$

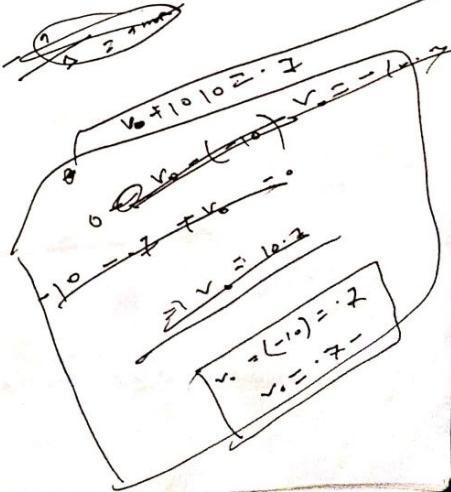
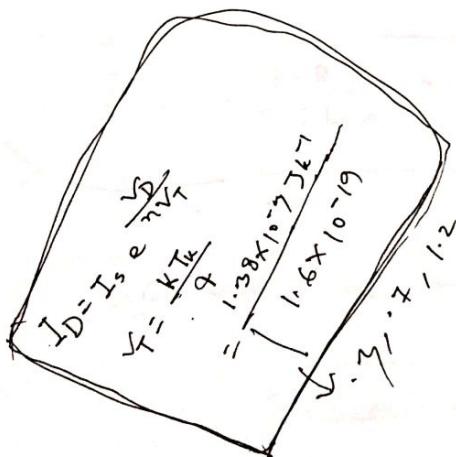
$$\Rightarrow V_O = -9.3V$$

$$\textcircled{2} \quad I = \frac{V_O}{R}$$

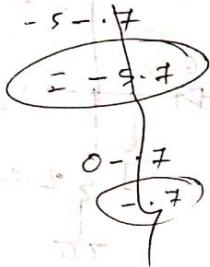
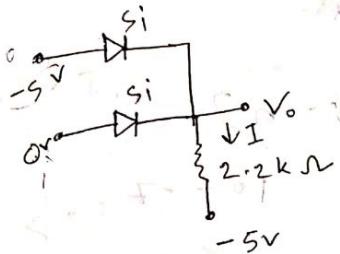
$$= 0.3 \text{ mA}$$

it's negative logic system.

It's OR gate.



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$$V_0 = 0 - 5 + = -4.5V \quad /0V$$

$$I = 0 \frac{V_0 - 0}{2.2} = 0A$$

~~OR Gate AND gate.~~

negative logic system

$$V_0 = -1.7V$$

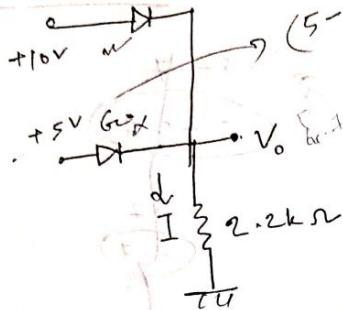
$$I = \frac{-1.7 - 0}{2.2 \text{ k}\Omega} \text{ mA}$$

~~OR Gate AND Gate. OR Gate.~~

AND Gate.

~~positive negative logic system.~~

~~sk~~ ~~skipped~~



$(5 - 0.7) \text{ no + possible}$   
 $\text{on given cond.}$   
 $\text{G.e., off.}$

$$10 - 0.7 = 9.3$$

~~$V_o = 9.3 \text{ V} \cdot (10 - 0.7) \text{ V}$~~

~~$I_o = \frac{9.3 - 0}{2.2} \text{ mA}$~~

~~$V_F = 0 \text{ V}$~~

~~$I_o = \frac{20 - F - 0}{2 \times 3.5} \text{ mA}$~~

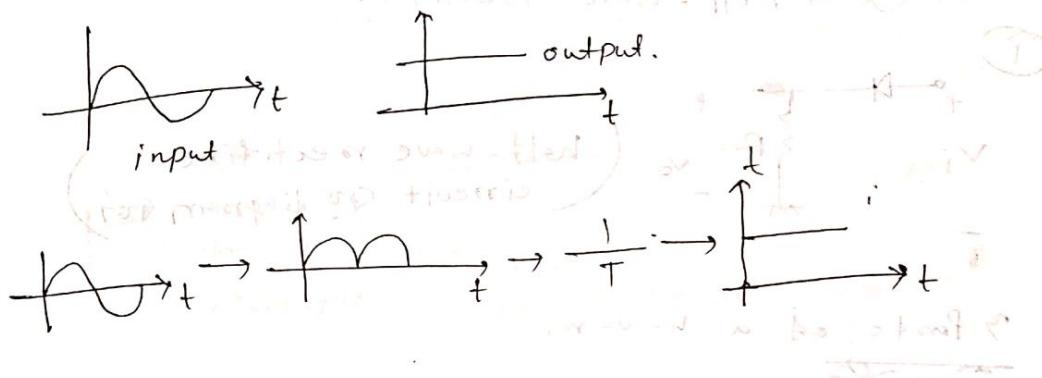
~~- check Q.A~~

~~control signal with open fitting~~

Qct (1st class - 20.10.18 m/s)

## Converters

- \* Converters / charger / adaptor  $\Rightarrow$  2nd class AC (or) DC to convert voltage. Qno star converter.



7806  $\rightarrow$  & output always 6 V m/s

temp 30

7805  $\rightarrow$  " " " 5 V "

- \* input 10V negative o/p point (or) o/p out one output m/s  
not functioning circuit.

~ input 10V (or) circuit rectifying m/s circuit.  
functioning circuit

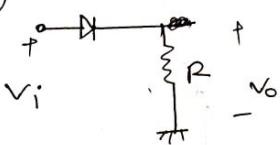
~ input 10V (or) (+, -), output 10V  $\Rightarrow$  only positive voltage or negative voltage m/s.  
when (or) a 10V  $\Rightarrow$  10V m/s

(functioning (or) not functioning)

## Q Rectifying circuit:

- ① Half-wave rectifier.
- ② Full-wave rectifier.

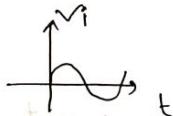
①



(half-wave rectifier  
circuit Q diagram Q2)

Parts of a h-w-r.

R.F. circuit  $\Rightarrow$  input AC signal, output  $\text{G}$  and DC signal.



ideal diod

Half.W.R. with ideal diod

1st: +ve half cycle,

At forward bias.

short circuit  $\Rightarrow$ ,

$$\therefore V_o = V_i \text{ (input = output)}$$



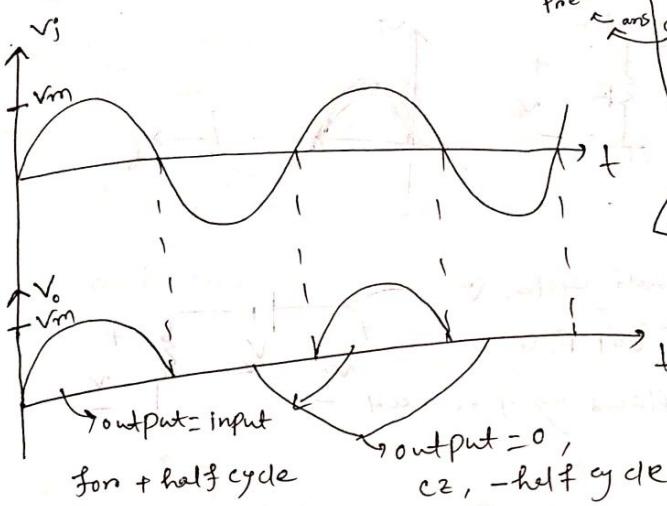
2nd negative half cycle: (-ve),

reverse bias At

$\therefore$  Open circuit

$$i = 0$$

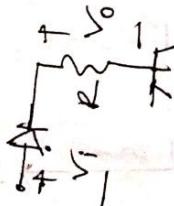
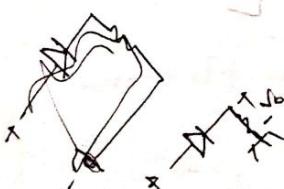
$$V_o = iR = 0 \text{ (output)}$$



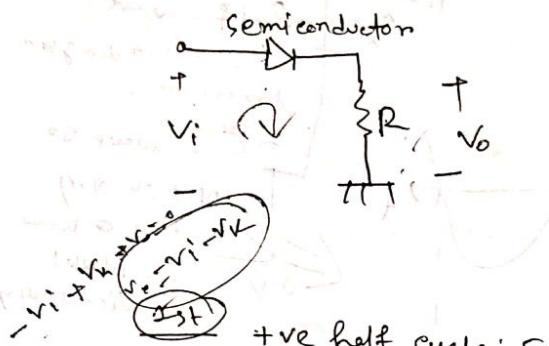
Previous Pg.  
Ans  
① ideal & - wave-  
circuit diagram  
drawn.  
ideal  
② Sine wave  $90^\circ$   
input  $v_i$   $90^\circ$   
output  $v_o$  draw  
ans zero ideal  
diode  $90^\circ$

Output of half cycle  $90^\circ$  and  $90^\circ$   
for half positive half-wave cycle.

Self Practice:



## \* Half Wave Rectifiers with Semiconductors diode



+ve half cycle:  $\therefore$

~~so, if F.b.~~

- replaced by open circuit.

$$V_o = V_i - V_k \quad [V_{\text{output}}]$$

②

- ve half cycle,  $\therefore$  ~~got r.b.~~

$$\therefore i = 0$$

$$V_o = iR = 0.$$



\* pure sign graph  $G$ : avg value = 0.

?  $\therefore$  ideal rectifier  $G$ : diod rectifies  $\Rightarrow$  avg value = 0.

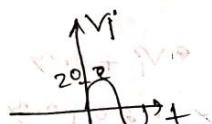
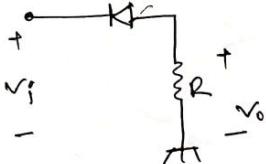
$$V_{avg} = V_{de} = \frac{1}{\pi} V_{max}$$

\* if  $|I|_{sat} \leftarrow V_{avg} = V_{de} = \frac{1}{\pi} V_{max} \rightarrow$  max output  $V_{Th}$

\* semiconductor  $\leftarrow V_{avg} = V_{de} = \frac{1}{\pi} (V_{max} - V_k)$

$$V_{avg} = V_{de} = \frac{1}{\pi} (V_{max} - V_k)$$

Example-2.16



Sketch the output & determine the DC level.

i) for ideal diode

ii) for semiconductor diode.

iii) for half cycle, i.e. diod to R.L.

$$\begin{cases} \text{for ideal,} \\ V_{de} = \frac{1}{\pi} V_{max} \\ \text{for se,} \\ V_{de} = \frac{1}{\pi} (V_{max} - V_k) \end{cases}$$

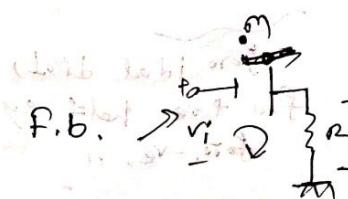
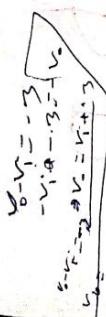
reverse bias  $\Rightarrow$  diod o.c.  $\Rightarrow$   $i = 0$ ,  $V_o = 0$ .

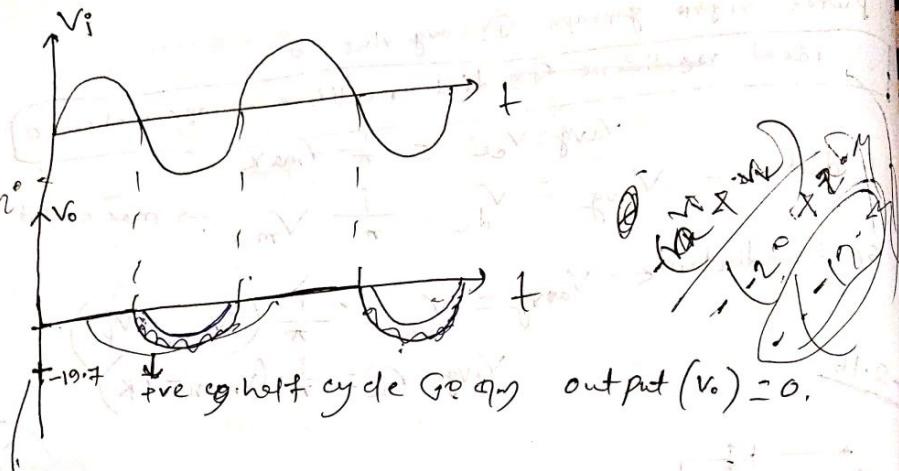
$$V_o = iR = 0,$$

-ve half cycle  $\Rightarrow$  diod to f.b.

$$-V_p - 0.7 + V_o = 0$$

$$\Rightarrow V_o = V_p + 0.7$$





$$\begin{aligned} \text{Output} &= +V_i + 0 \cdot \gamma \\ &= +20 + 0 \cdot \gamma \\ &= -19.7 \end{aligned}$$

~~Diode~~

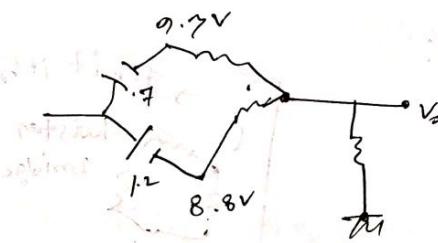
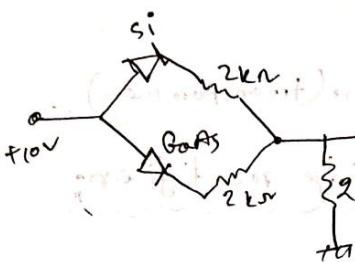
$$\begin{aligned} V_{dc} &= \frac{1}{\pi} (V_{max} - V_k) \\ &= \frac{1}{\pi} \times 20 (-19.7) \\ &= -6.27 \text{ V} \end{aligned}$$

for ideal diod,

For pre half cycles,  $V_o = 0$   $\therefore V_o = V_{in}$

$$\begin{aligned} \therefore V_{dc} &= V_{avg} = \frac{1}{\pi} \times V_{max} = \frac{1}{\pi} \times 20 \\ &= 6.27 \text{ V} \end{aligned}$$

# C7-1 (solution)



$$\frac{V_o - 0}{2} = \frac{9.7 - V_o}{2} + \frac{8.8 - V_o}{2}$$

$$9.7 - V_o = 8.8 - 2V_o$$

$$V_o = 6.03 \text{ V}$$

$$I_{Si} = \frac{9.7 - V_o}{2} = 1.635 \text{ mA}$$

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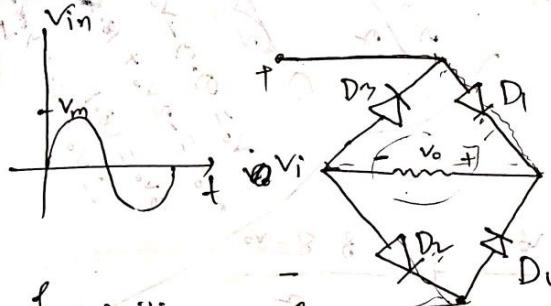
full wave rectifiers

→ Diode-bridge

→ Centre tapped xen (transformer)

\* Diode-bridge rectifier/bridge rectifier

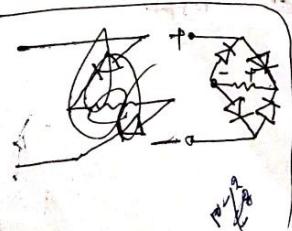
Circuit diagram:



for positive half cycle

$$V_o = V_i \rightarrow (\text{ideal diod})$$

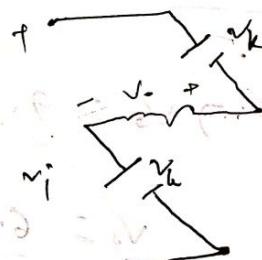
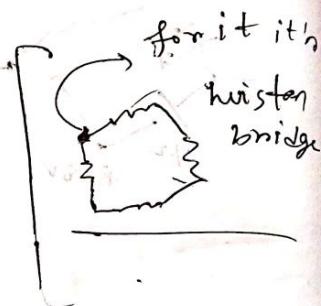
$$V_o = V_i - 2V_k \rightarrow (\text{semi con-dioid})$$



on applying KVL,

$$-V_i + V_k + V_o + V_k = 0$$

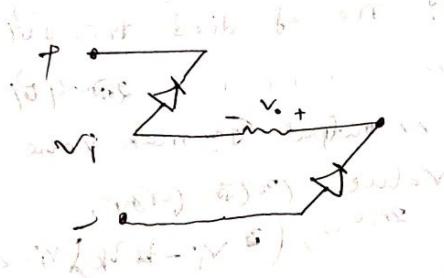
$$\Rightarrow V_o = V_i - 2V_k$$



$$\begin{aligned} & V_o = V_i - V_k \\ & -V_i + V_k + V_o + V_k = 0 \\ & V_o = V_i - 2V_k \end{aligned}$$

negative half cycle:

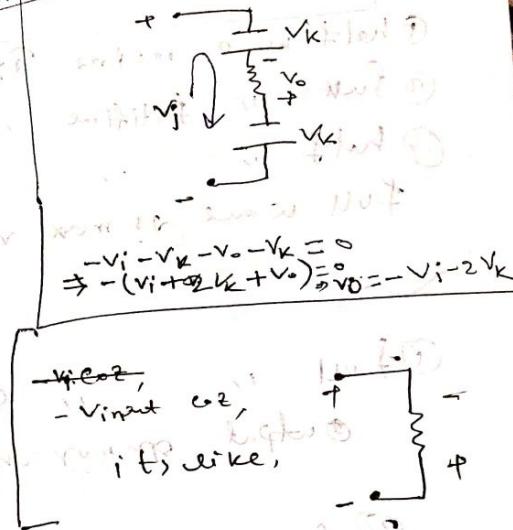
$$\begin{aligned}
 -V_i - V_K - V_o - V_K &= 0 & V_i + V_K + V_o + V_K &= 0 \\
 \Rightarrow -V_o &= V_i + 2V_K & \text{(cancel } V_K\text{)} \\
 \Rightarrow V_o &= -V_i - 2V_K
 \end{aligned}$$



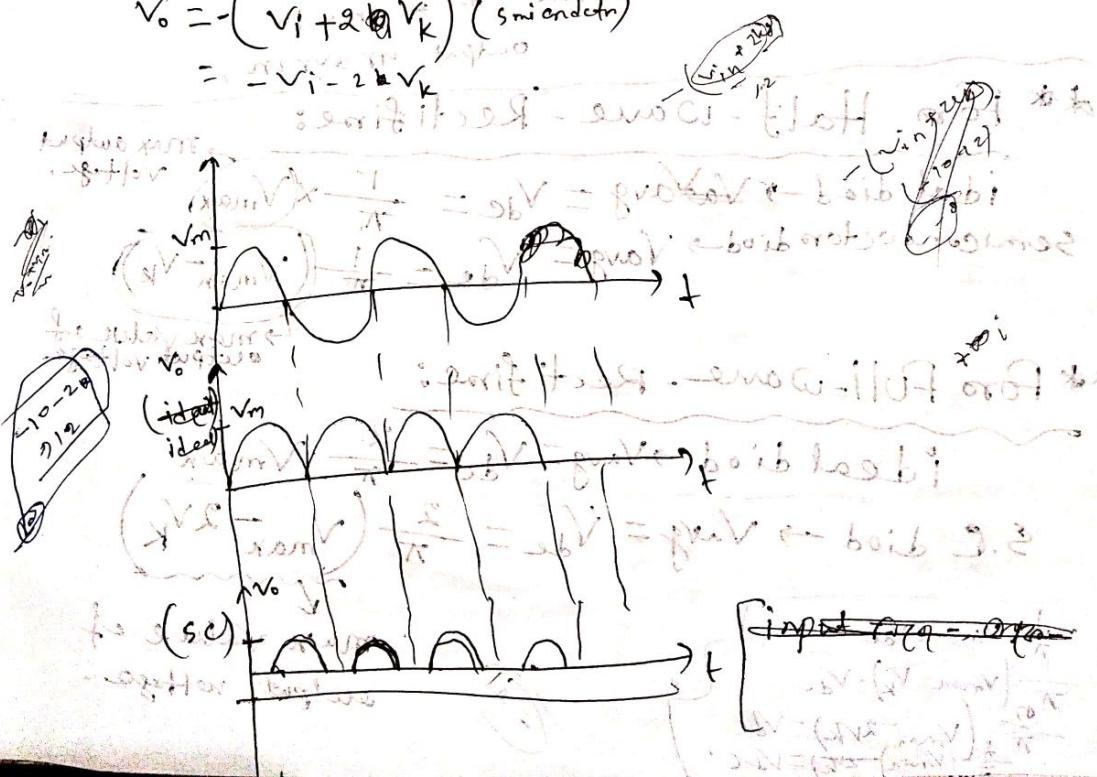
V<sub>output</sub>:

$$V_o = -V_{\text{input}} \text{ (ideal)}$$

(diode)



$$\begin{aligned}
 V_o &= -(V_i + 2V_K) \quad (\text{since } V_o < 0) \\
 &= -V_i - 2V_K
 \end{aligned}$$



① Half Wave Rectification, ideal diod  $\rightarrow V_{avg}$

\* half wave rectifier  $\Rightarrow$  no. of diod  $\frac{1}{2}$  out  
full wave rectifier  $\Rightarrow$  no. of diod 4 out

② full wave rectifier " " max value

③ half " " " output  $\Rightarrow$  max value  
full wave  $\Rightarrow$  max value.  $\approx \sqrt{2}$  (error)  
 $\text{max} = (\sqrt{V_i - 2V_K}) \sqrt{V_i - 2V_K}$

④ full " " " complete cycle  $\Rightarrow$   $\frac{1}{2} V_{max}$

Output  $\Rightarrow$  suryam

⑤ full wave rectifier.  $\Rightarrow$  (so smooth)  $= V$   
output  $\Rightarrow$  suryam

\* For Half-Wave-Rectifier:

ideal diod  $\rightarrow V_{avg} = V_{dc} = \frac{1}{\pi} \times V_{max}$   $\Rightarrow$  max output voltage.

Semiconductor diod  $\rightarrow V_{avg} = V_{dc} = \frac{1}{\pi} (V_{max} - V_K)$   $\Rightarrow$  max value of output voltage

\* For Full-Wave-Rectifier:

ideal diod  $\rightarrow V_{avg} = V_{dc} = \frac{2}{\pi} V_{max}$

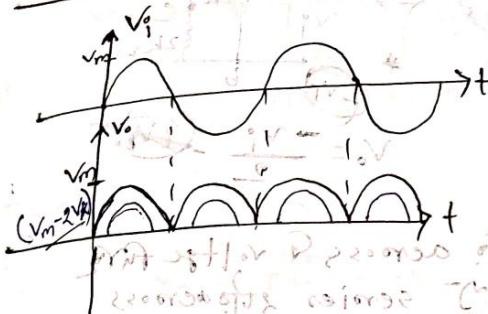
S.C. diod  $\rightarrow V_{avg} = V_{dc} = \frac{2}{\pi} (V_{max} - 2V_K)$

$$\begin{aligned} \frac{1}{\pi} (V_{max} - V_K) &= V_{dc} \\ \frac{1}{\pi} (V_{max} - 2V_K) &= V_{dc} \\ \frac{2}{\pi} (V_{max} - 2V_K) &= V_{dc} \end{aligned}$$

max value of output voltage

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## Diode bridge:



half wave  $\Rightarrow$

$$\text{formula: } \frac{1}{\pi} (V_{max} - V_k)$$

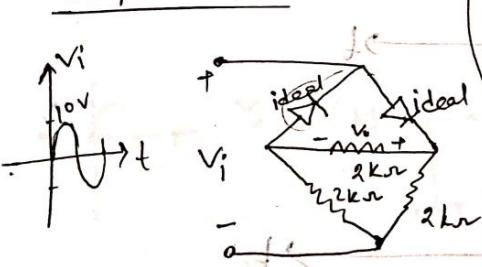
full wave  $\Rightarrow$

$$\frac{2}{\pi} (V_{max} - 2V_k)$$

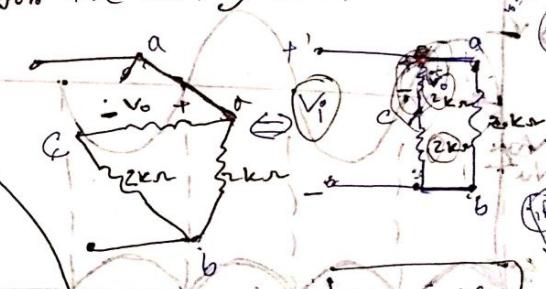
$$V_{dc} = V_{avg} = \frac{1}{\pi} (V_{max} - 2V_k)$$

maximum value of output voltage

Example - 2.17



for +ve half cycle input:

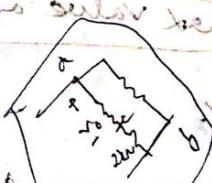


Sketch  $V_o$ :

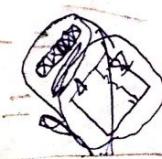
What is the DC value of  $V_o$ ,

to get to series here

Series 0  $\rightarrow$   
 $V$  divide  $0V$   
 $= n$  same or



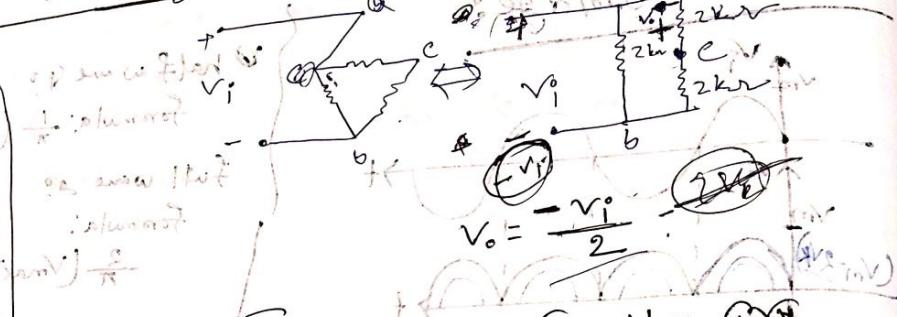
$$V_o = \frac{8}{\pi}$$



as given voltage dividers  
will apply to P260?

for -ve half cycle:

full wave rectifying circuit  
will give full wave rectified  
voltage across load.

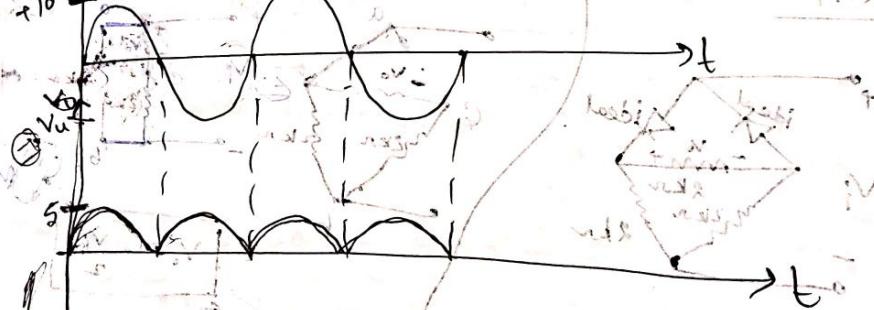


$V_o$  is across G voltage filter  
G = series ztfo across  
 $(V_i - V_o)$  divide  $2C_0 G_{\text{filter}}$   
as so same  $\therefore V_o = \frac{V_i}{2}$

filter voltage to obtain  $V_o$

negative half cycle

F.I.S =  $\frac{V_o}{V_i}$



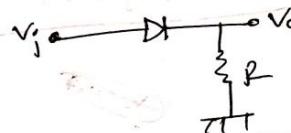
$$V_{dc} = \frac{2}{\pi} V_{max} = \frac{2}{\pi} V_k$$

$$\frac{2}{\pi} \times 5 = \frac{10}{\pi} = 3.183 \text{ V}$$

Max value of output.

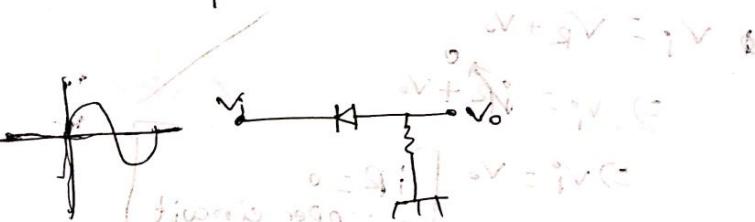
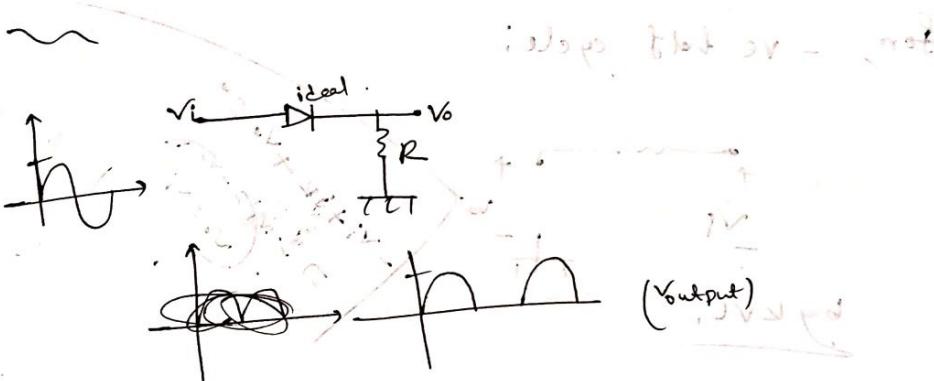
2nd half voltage amb.

### Clippers Circuit:



[simple example of clipper circuit]

it's a half w.r.t.  $V_{DSS}$

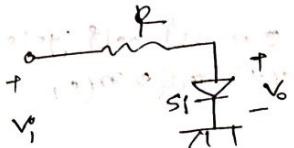


for -ve half cycle;

$$V_o = V_D$$

for +ve "

$$V_o = V_D + V_p$$



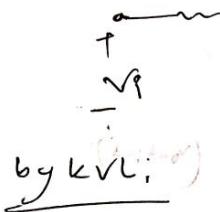
short circuit  $\Rightarrow$  on?  
across  $V_o$  always  $0.7V$

open circuit  $\Rightarrow$   $V_o$   
zero  $\Rightarrow$  zero  $\Rightarrow$   $V_o$   
open circuit  $\Rightarrow$   $0.7V$   
KVL apply  $\Rightarrow$   $V_o = 0.7V$

for, +ve

$$\therefore V_o = (V_i - 0.7V) = 0.7V.$$

( for, -ve half cycle:



by KVL

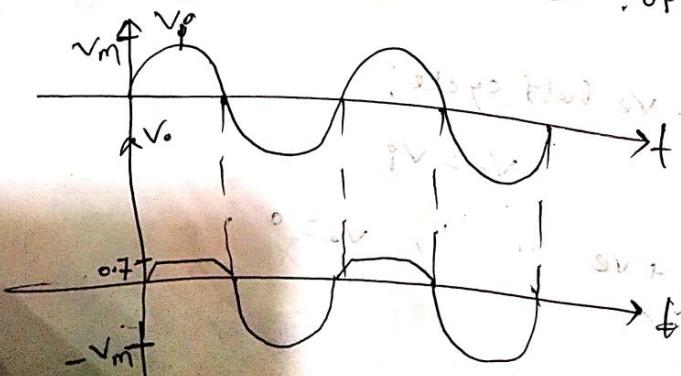
$$V_i = V_R + V_o$$

$$\Rightarrow V_o = V_R + 0.7V$$

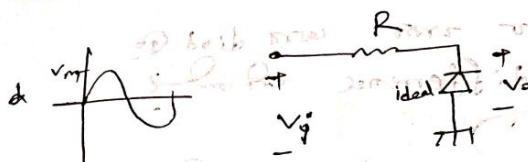
$$\Rightarrow V_o = 0.7V$$

$$iR = 0$$

$\therefore$  open circuit



∴ input freq  
output freq  
same, so, output  
is also constant  
DC input is  
followed  
zero current,



$\$ \text{ in short circuit}$

$$V = iR$$

$$= ix_0$$

$$= 0$$

$$\therefore i = 0$$

for, +ve half cycle:

$\therefore$  open circuit  $22^\circ$ .

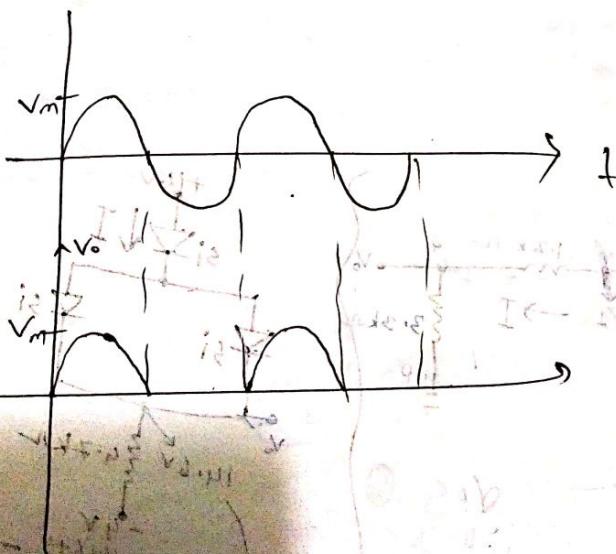
$$\therefore V_o = -x_1$$



for, -ve half cycle:  $R = \infty$   $I = 0$

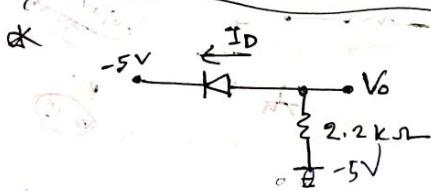
$\therefore$  diod  $\text{at F.B.} \therefore$  shunt circuit  $22^\circ$ .

$$V_o = ir = ix_0 = 0.$$

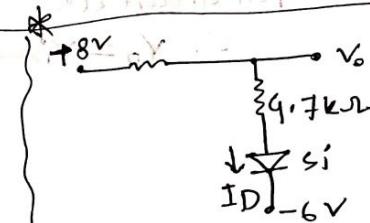


~~Q~~ No resistance  $G_0$  and zero error was diod  $G_0$   
 emg error very difference

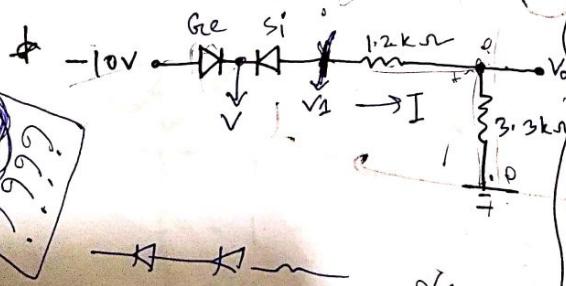
difference?



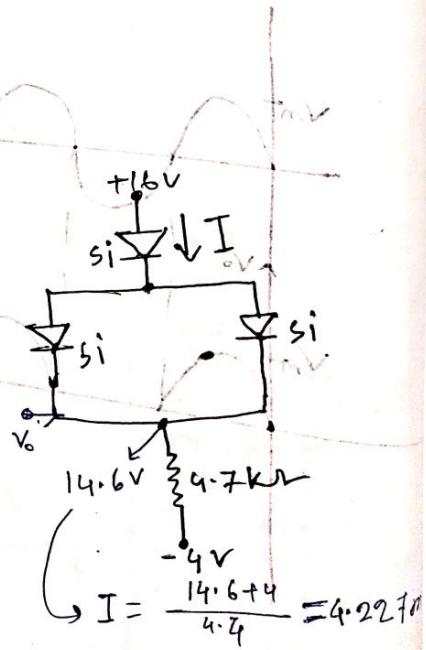
$$I_D = ? \quad v_o = ?$$

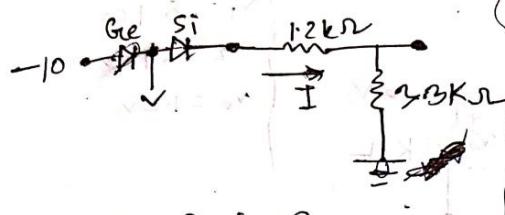


$$V_0 = ? \text{, } I_D = ?$$

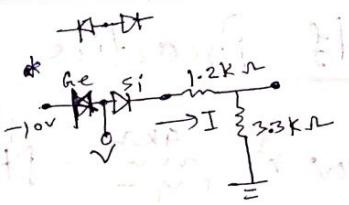


88  
11

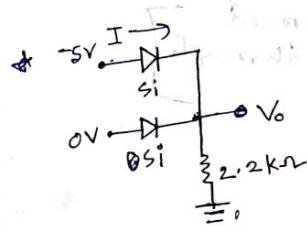




$$V = ? \quad i = ?$$

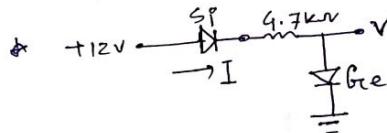


$$\text{find } I \text{ } 8V$$



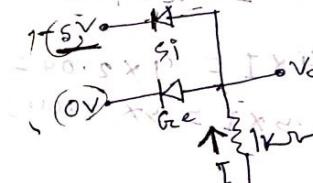
$$V_o, I = ?$$

$$V_o = 0V, I = 0mA$$



$$I = ?, V = ?$$

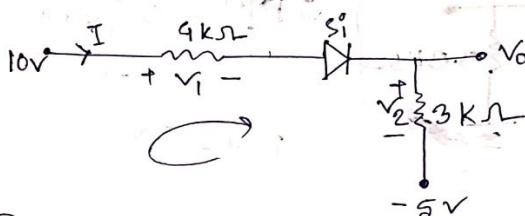
$$\begin{aligned} & V_o = 0V \\ & I = 0mA \\ & V_o = 0V, I = 0mA \end{aligned}$$



$$\begin{aligned} & \text{only } si \text{ on } R^2 \\ & -5 + 7 = -4.3V = V \\ & I = -6 + 4.17 \\ & -1.7mA \end{aligned}$$



## Self Practice



$$\left. \begin{array}{l} V_1 = 8.16V \\ V_2 = 6.12V \\ V_0 = 1.12V \end{array} \right\}$$

Find  $V_1$ ,  $V_2$ ,  $V_0$  & Current.

$$\underline{\frac{V_T = 10}{\text{by KVL}}}$$

$$-10 + V_1 + 7 + V_2 - 5 = 0$$

$$V_1 + V_2 = 14.3$$

$$\Rightarrow 4I + 3I = 14.3$$

$$7I = 14.3$$

$$\therefore I = 2.04 \text{ mA}$$

This is the current  
which will flow through  
the circuit

$$V_1 = 4 \times I = 4 \times 2.04 = 8.16 \text{ V}$$

$$V_2 = 3 \times I = 3 \times 2.04 = 6.12 \text{ V}$$

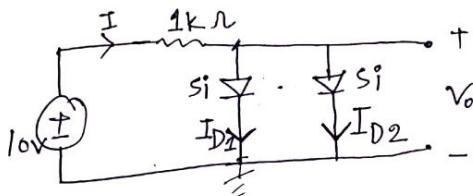
$$V_0 - (-5) = 6.12$$

$$\Rightarrow V_0 = 6.12 - 5$$

$$= 1.12 \text{ V}$$

Ans:

\* Find  $V_o$ , current I,  $I_{D1}$ ,  $I_{D2}$  for the circuit:



$$I = \frac{V}{R} = \frac{10}{1} = 10 \text{ mA}$$

~~$I_{D1} = 5 \text{ mA}, I_{D2} = 5 \text{ mA.}$~~

$$I = \frac{10 - .7}{1} = 9.3 \text{ mA.}$$

$$\therefore I_{D1} = I_{D2} = 4.65 \text{ mA.}$$

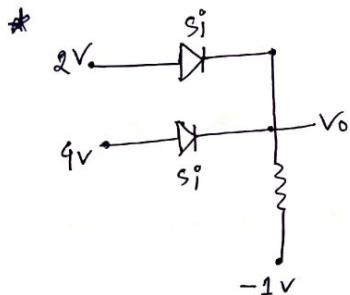
on,

by  $kV^2$

$$-10 + 1I + .7 = 0$$

$$\Rightarrow I = 10 - .7$$

$$= 9.3 \text{ mA.}$$



$$V_o = ?$$

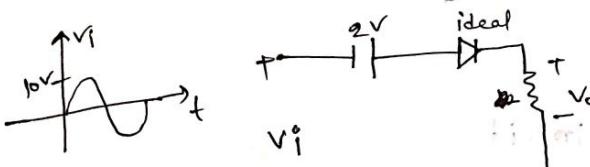
$$2 - .7 = 1.3 \text{ V}, \quad 4 - .7 = 3.3 \text{ V.}$$

$\therefore$  1st diod will remain off and  
only 2nd diod will remain on.

$$\therefore V_o = 4 - .7 = 3.3 \text{ V.}$$

3/u/18

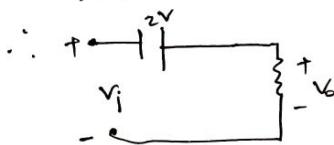
## Clipper Circuit:



Ref-book  
chpt n-2  
Clipper circuit

for, +ve half cycle of i/p,

F. b.

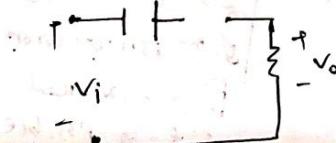


Diode - 1st half cycle  $\rightarrow$  F. b. off  
2nd half cycle  $\rightarrow$  on  
R. b. 270°  
 $2m-f \rightarrow$  opposite 0°,

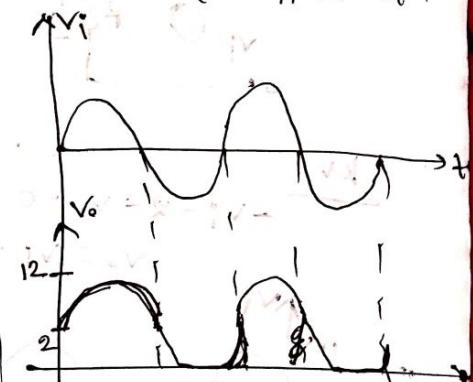
by kvl:  $-v_i - 2 + v_o = 0$

$\Rightarrow v_o = v_i + 2$

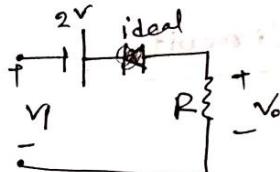
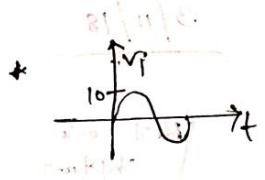
for, -ve half cycle of i/p:



$i = 0$   
 $\therefore v_o = iR = 0$



negative half cycle  
(To cut 450° off)  
. Gt clipper circuit.

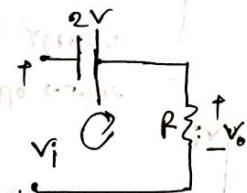


For, +ve half cycle,

R.B.  $\therefore$  open circuit

$$\text{Block for } \leftarrow. i=0; V_o = i \times R = 0$$

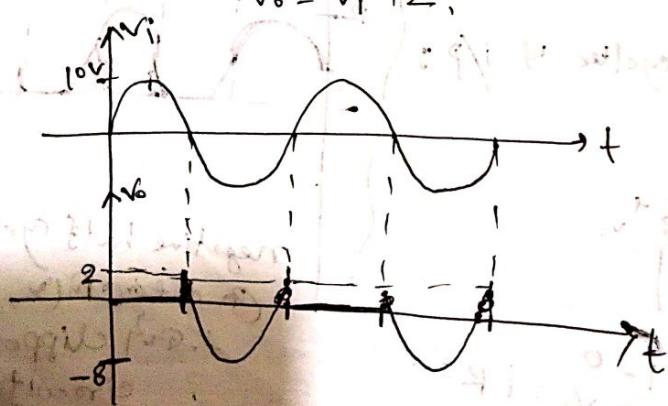
for, -ve half cycle of i/p,



kVZ

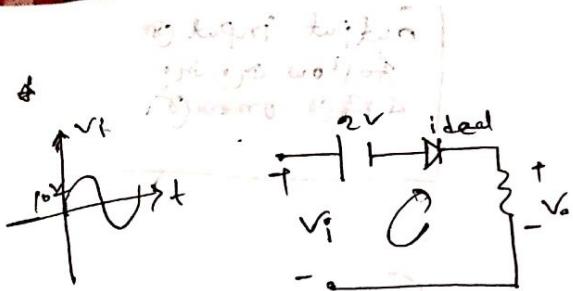
$$-V_i - 2 + V_o = 0$$

$$V_o = V_i + 2,$$



Output  $0(2V)$   
 $\Rightarrow 0 + 2(2V)$   
 To find minimum  
 find max real  
 life is possible  
 $\therefore$   $0(2V)$   
 is the answer

draw  $0(2V)$   
 $0(2V)$  min  
 amper.



for +ve half cycle,

$$-Vi + 2V + Vo = 0$$

F.B.

$$-Vi + 2V + Vo = 0$$

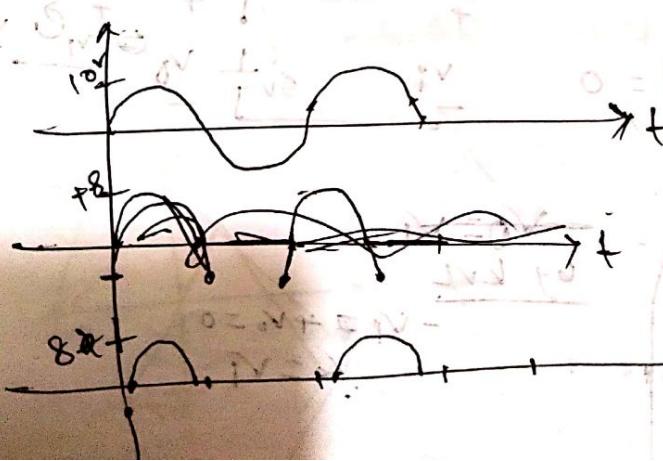
$$Vo = Vi - 2V$$

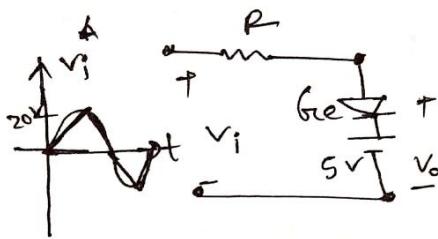
for -ve,

R.B.

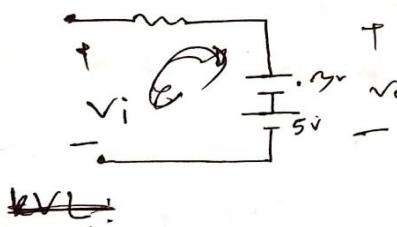
$$-Vi + 2V + Vo = 0$$

$$i = 0$$





for +ve feedback  
F.B.



Output voltage  
follows input  
in B.C. on care

Amplifier circuit  
G = output / input R  
G = across  $R_f$   
G =  $\beta$ ,  $R_f$  across  
G = output / input  
 $R_f$  across G = out  
Put  $\beta = \infty$ ,  $V_o = \infty$ ,

Rectifiers & Q.T. Look at example / exercise  
on 27.7.20.

et-2

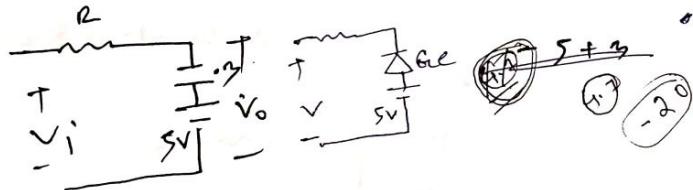
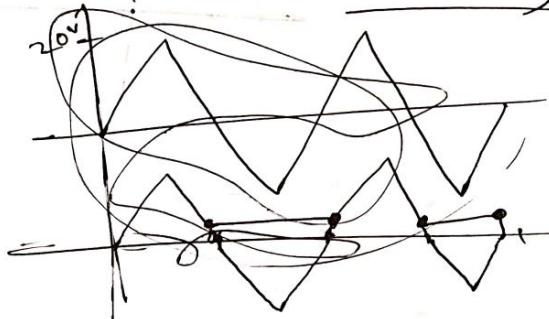
Rectifier circuit  
clippers etc  
next Saturday

for, +ve,

R.B.

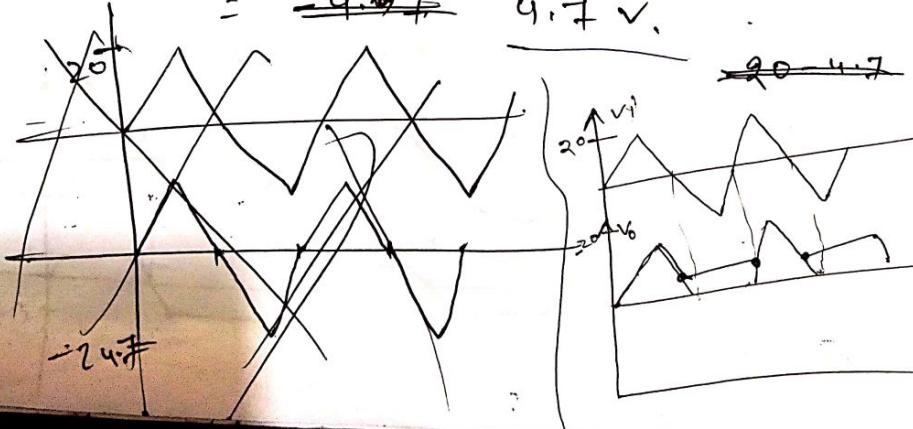
$$\therefore V_o = V_i$$

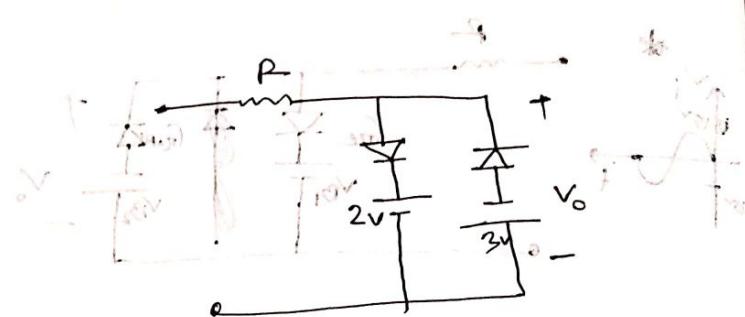
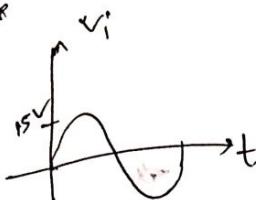
for, -ve,



$$V_o = 5 \text{ V}$$

$$= -4.7 \text{ V} \quad 4.7 \text{ V.}$$

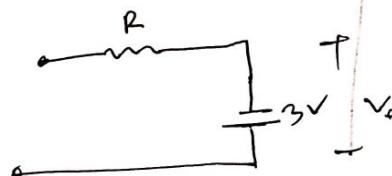




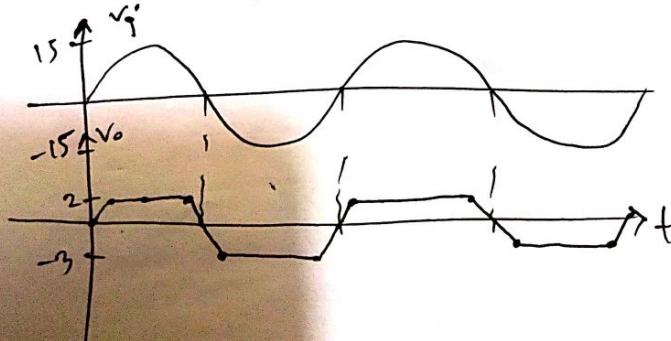
for, +ve half cycle,  $V_o = 10V$

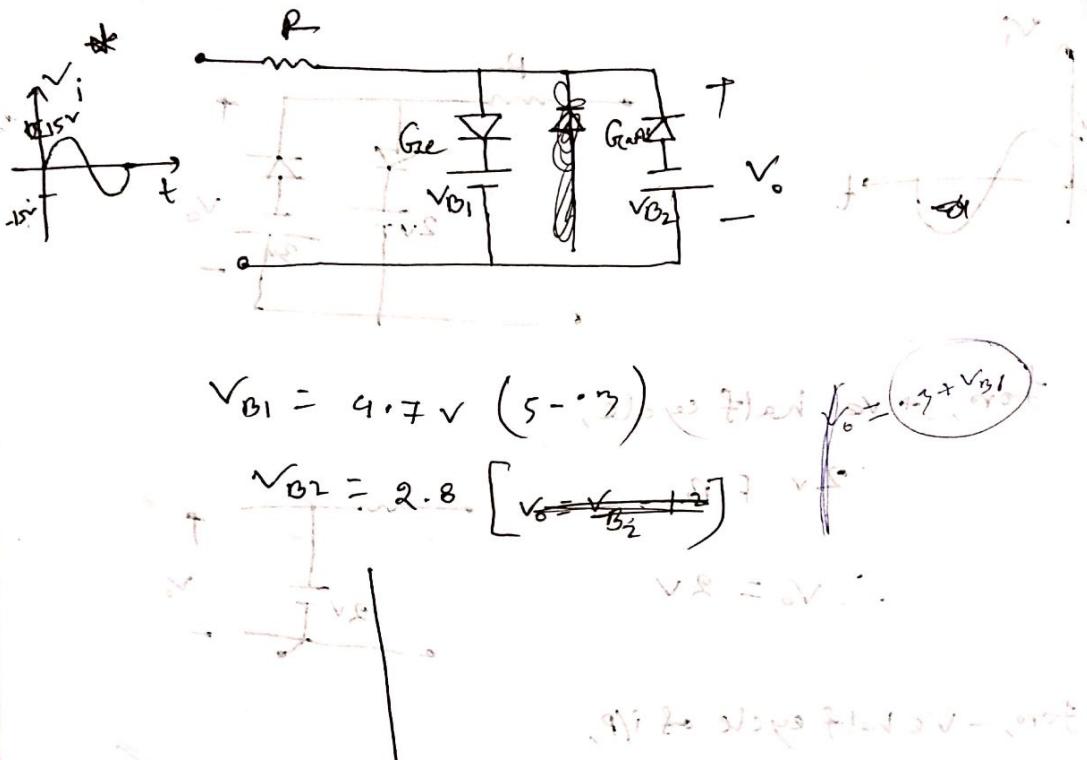


for, -ve half cycle of i/p,



$$\therefore V_o = -3V.$$

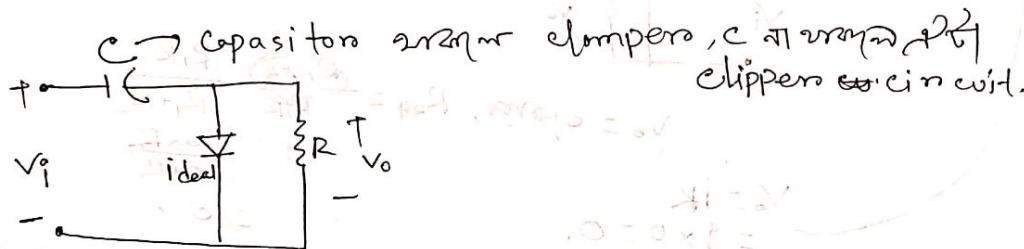




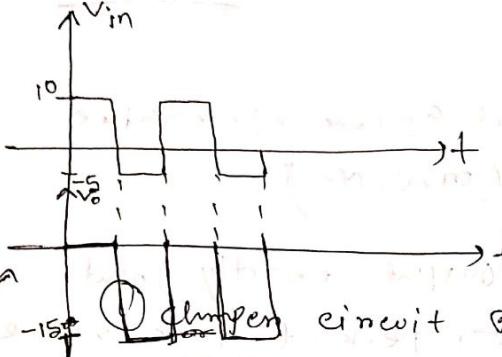
6/11/18

## clamper circuit:

- \* Clipper circuit input  $V_i$ : peak-to-peak value  
( $\approx$  change in  $V_o$  (current  $i_v$ ))
- \* Clamper circuit & output exactly input  
 $V_i$  shape &  $\frac{1}{2}$  range, peak-to-peak & same  
range,  
either ~~will have~~  $\text{for } V_o$   $\text{will have}$   $\text{either } V_o$   
on  $V_o$ ,  $\text{for } V_o$   $\text{will have}$ ,  
 $\text{and, either upward shift } V_o$ ,  
neither downward  $V_o$



simple clamper circuit diagram.



clamper C. 50°  
voltage Peak to Peak  
value some 10V  
from first 50° 50V & 0V  
AC part.

বাস্তু এই 1st ক্লেমে +,-ve (অ-হেফ)

cycle দ্বিতীয় পর্যন্ত আবারো করা হচ্ছে

P.P.G. circuit টি P+ve half cycle diod এ F.B. 6265.



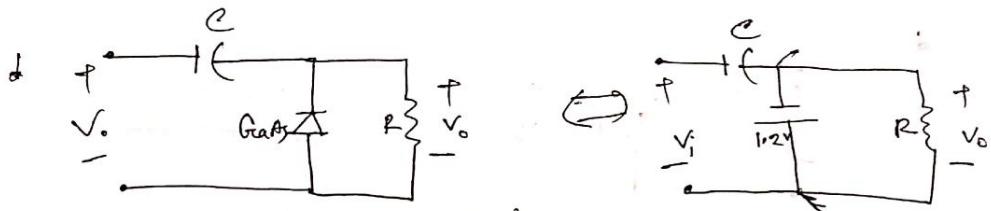
$$V_o = 0 \text{ VDC}, R_{eq} = \frac{R_1 R_2}{R_1 + R_2}$$

$$\begin{aligned} V_o &= iR \\ &= 9 \times 0 = 0. \end{aligned}$$

$$\begin{aligned} &= \frac{0 \times R}{0 + R} \\ &= 0. \end{aligned}$$

+ve half cycle থেকে 10 VDC আবারো  
means peak

-ve 10 VDC থেকে আবারো আবারো

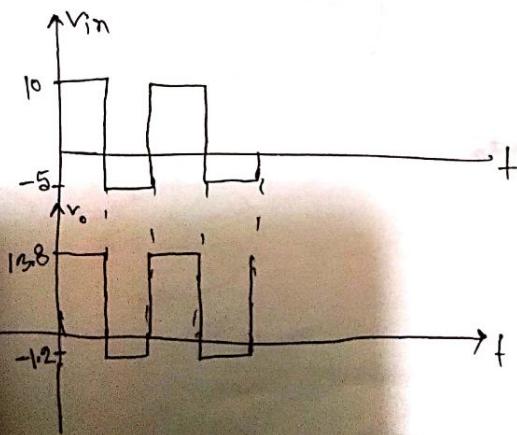


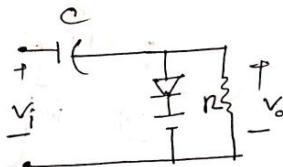
As Capacitor charges get clamps circuit.

∴ Diod ପାଇଁ F.T ଏକାର୍ଥ ହଣେ input ଦେଇବେ half cycle ନିମ୍ନରୀତି ।

Output filter  $R^G$  across  $G$ ,  $\therefore 1.2V^G + V^G$   
 direction  $R^G$  direction opposite.

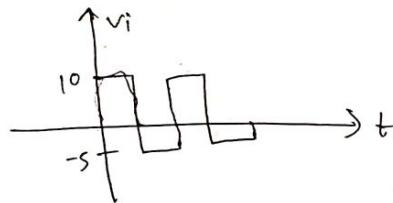
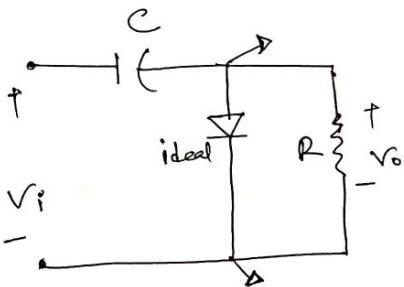
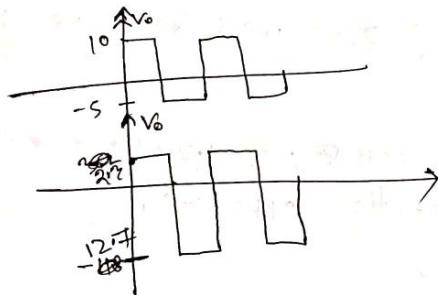
$$\therefore V_0 = -1.2 \text{ V}$$



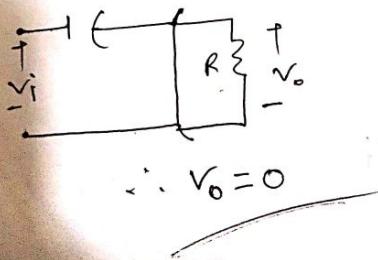


$$+3 + 2 = 2 \cdot 3$$

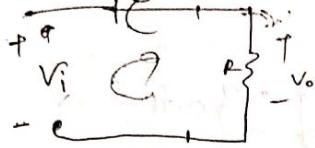
(3.2)



for +ve half cycle of input,



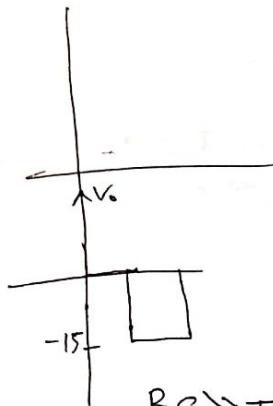
for, -ve half cycle,



$$V_o = \underline{V_i - V_C} \rightarrow \text{capacitor},$$

$$\Rightarrow V_o = \underline{-5 - 10}$$

$$= \underline{-15V}$$



$R_C \gg T_{\text{trans}}$ , ~~Capacitors~~:  
+ve, -ve going same output  $V_{\text{out}}$  /

$$V_i - V_o = V_C$$

for + ve

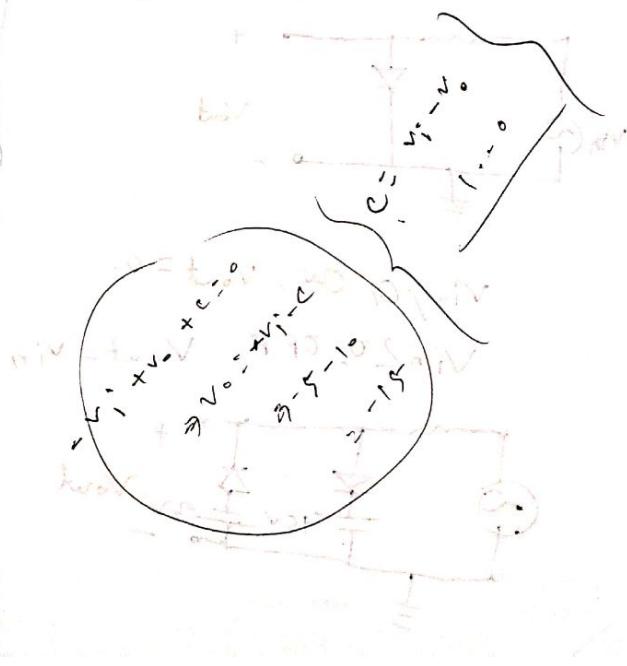
$$V_B = 0$$

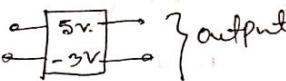
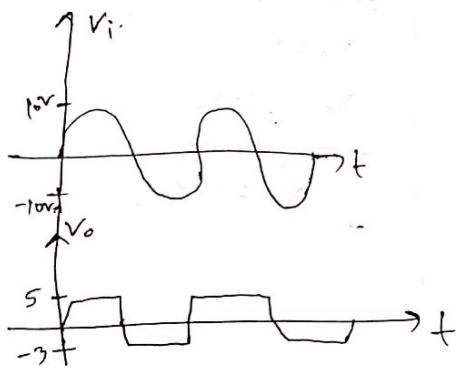
$$V_o = V_i - V_c$$

$$\Rightarrow \theta = 10 - v_C$$

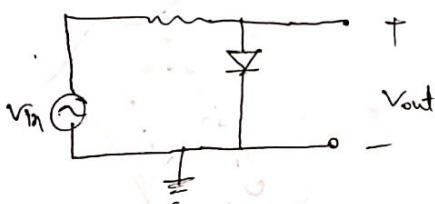
$$\sqrt{c} = 10^{\nu}.$$

Capacitor द्वारा बना विद्युतीय वर्तमान का विभिन्न संकेतों का अध्ययन करते हैं।





shunt clippers / parallel clipper:



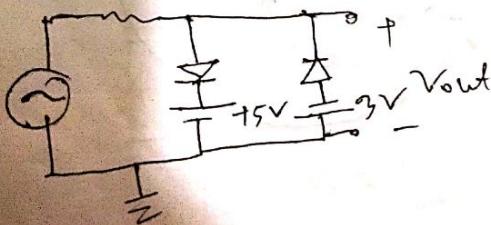
$V_{in} > 0$ , ON;  $V_{out} = 0$ .

$V_{in} \leq 0$ , OFF,  $V_{out} = V_{in}$

diode forward  
forward bias

diode reverse  
reverse bias

diode forward  
forward bias



$$V_{rms} = \frac{\text{Peak}}{\sqrt{2}} \quad (\text{Peak} \leftrightarrow \text{rms (transformation)})$$

Graph to time, peak, frequency and voltage  
from meter तरीके,

Q level तरीके बताये, फॉर्म बनाये रखें,

### Champer

diode तिर्यक फॉर्म बनाये तिर्यक shift रखें.

diode क्लिप तरीके बनाये तिर्यक फॉर्म बनाये.

$$\text{Current} = \frac{\text{Voltage}}{\text{Resistance}} = \frac{V}{R} = 10^{-3}$$

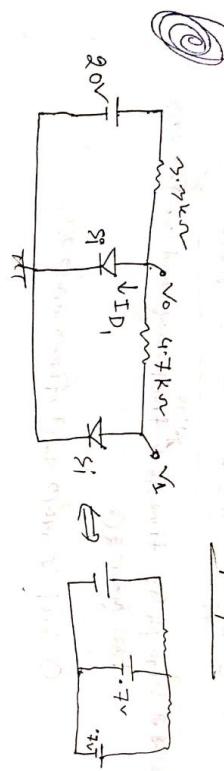
Amper

Amper

Amper जो किए जाना चाहिए तो इसका विस्तृत वर्णन करें।

## Theory

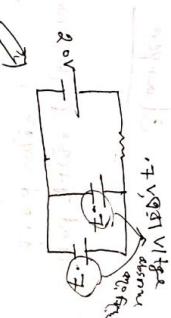
6/11/18



$$V_0 - 0 = 4.7 \text{ V}$$

$$\therefore V_0 = 4.7 \text{ V}$$

$$V_A = 0.7 \text{ V}$$

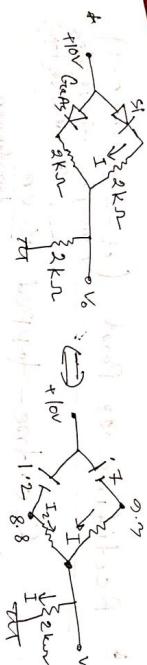


$\left. \begin{array}{l} \text{From first analysis (R), } \therefore 4.7 \text{ k} \Omega \text{ Resistor} \\ \text{In perfectly short circuit current } I_D, \end{array} \right\}$

$$\therefore I_{D1} = I_{D2} = I/2 = \frac{20 - 0.7}{2 \cdot 4.7} = 2.02 \text{ mA.}$$

Ans:

\* \* Normal battery always connect supply to Mr. 1 and potential always take absolute val. (+7.07, +2.02)



$$I = I_1 + I_{DZ} \quad \text{at } 8.8^\circ$$

$$\frac{V_o}{2} = \frac{9.17 - 6}{2} + \frac{8.8}{2}$$

$$\frac{V_o}{2} = -V_o + 9.17 - 8.8$$

$$\Rightarrow V_o + V_o = +9.17 - 8.8$$

$$\therefore V_o = 0.37 \text{ V}$$

$$18.1 - 18.1 = 4.4 \text{ mA}$$

turn on Potential  
ultimately short circuit  
at voltage absorption  
(Zener diode) main (supply)  
voltage (पूर्ण वोल्टेज  
ताप स्थिति तरीके सिर्फ  
जटिल सर्वानुसार करना  
एवं 20V, 1

current  
(पूर्ण वोल्टेज  
on  
high  
low voltage on)  
can't high voltage (पूर्ण  
low voltage on. Right  
now!

Chapter 4

Half wave rectifier  
with Zener diode

2 diodes, 2 resistors  
full wave rectifiers.

Rectifying Point (at -2° <sup>innermost</sup>)  
may be mid <sup>go</sup> syllables  
or topic

Centre-tapped  $\frac{X\text{-em}}{\text{transformer}}$ .

full wave rectifier

pair

$$V_1 = \{x \in \mathbb{R}^n : x_i > 0, i = 1, \dots, n\}$$

卷之三

100

卷之三

100

Conclusions

off

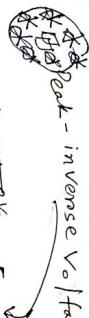
— 1 —

卷之三

50

Secondary fit  
Secondary contact

Peak - inverse voltage



reverse bias condition &

$$V_L = -V_i$$

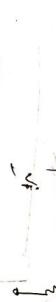
diode reverse bias & anti  
parallel diode to  $V_L$ ,  $-V_i$  direction

Peak inverse voltage

Tank  $\Rightarrow$  diode  $R_L$  and  $V_L$



Peak -  
diode  $R_L$  and  $V_L$  no effect  
 $-PIV \rightarrow [$  diode to  $V_L$ ,  $-V_i$  direction  
reverse bias!  $] + PIV$



$$\begin{aligned} & \text{reverse bias condition } \Rightarrow \text{ diode } R_L \text{ and } V_L \\ & -PIV + V_o = 0 \\ & -PIV = -V_i + V_o \\ & = -V_i + i_R R_o \\ & = -V_i \times R_o \end{aligned}$$



$$= -V_i$$

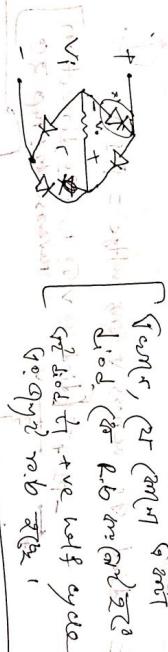
R.L condition  $\Rightarrow$   $G_o$  with diode  
max current  $i_R$   $\Rightarrow$   $V_o = -V_i$

$\text{PIV} \leftarrow \text{Yield stress} - \frac{\text{Sign } \sigma_i \text{ val in } \tau_{\text{max}}}{\text{val in } \tau_{\text{min}}}$

$\text{PIV} \leftarrow \text{Yield stress} - \frac{\text{Sign } \sigma_i \text{ val in } \tau_{\text{max}}}{\text{val in } \tau_{\text{min}}} \times \frac{\text{val in } \tau_{\text{max}} - \text{val in } \tau_{\text{min}}}{\text{val in } \tau_{\text{max}} + \text{val in } \tau_{\text{min}}}$

$$\text{half w.r.t PIV} = \sigma_i$$

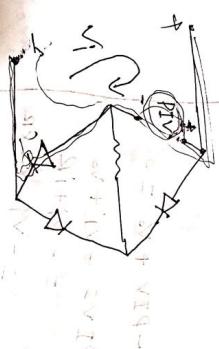
\* Full w.r. circuit



General case  
Point P lies  
inside the polygon

Half cycle  
one half cycle

PIV is zero  
at the center  
of the circle



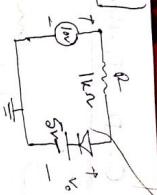
$$\text{PIV} = \sigma_i - \sigma_e = 0$$

$$\text{for finding } \text{PIV} = \sigma_i - \sigma_e = \frac{\sigma_i + \sigma_e}{2}$$

$\text{PIV} = \sigma_i - \sigma_e$

③ set A

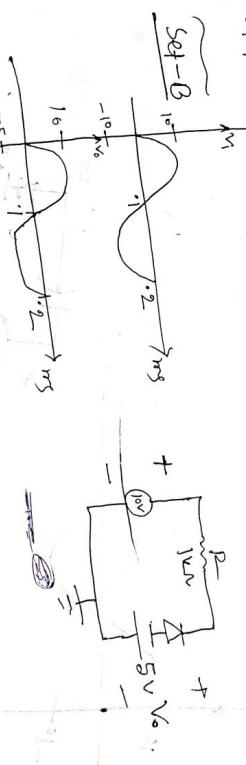
$$R_{ms} = \frac{\text{Peak}}{\sqrt{2}}$$



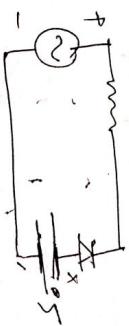
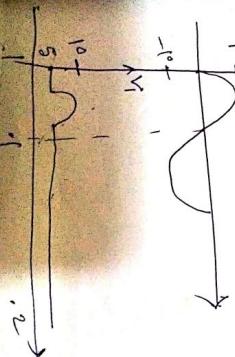
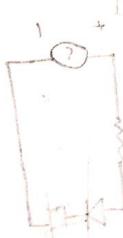
(1)

$$f = \frac{1}{T} = \frac{1}{0.2\pi} = 15.9\text{Hz}$$

Diode  
1N4007GP

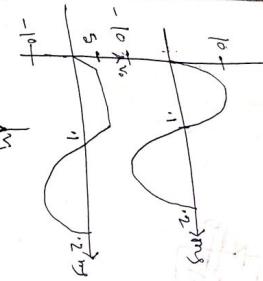
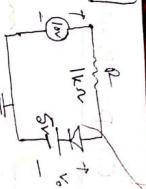


Set-C



④ set A

$$\text{Rms} = \frac{\text{Peak}}{\sqrt{2}}$$

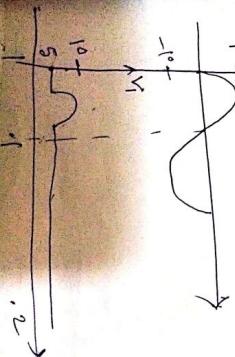
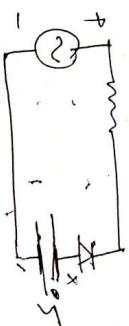
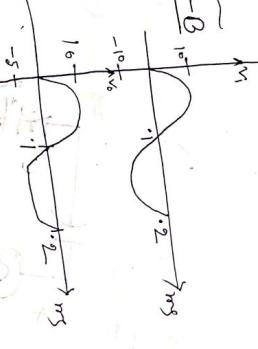
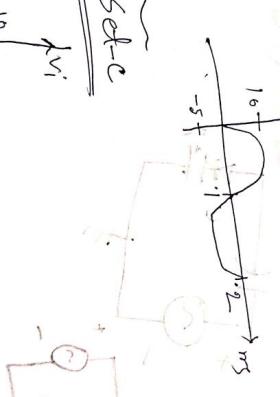


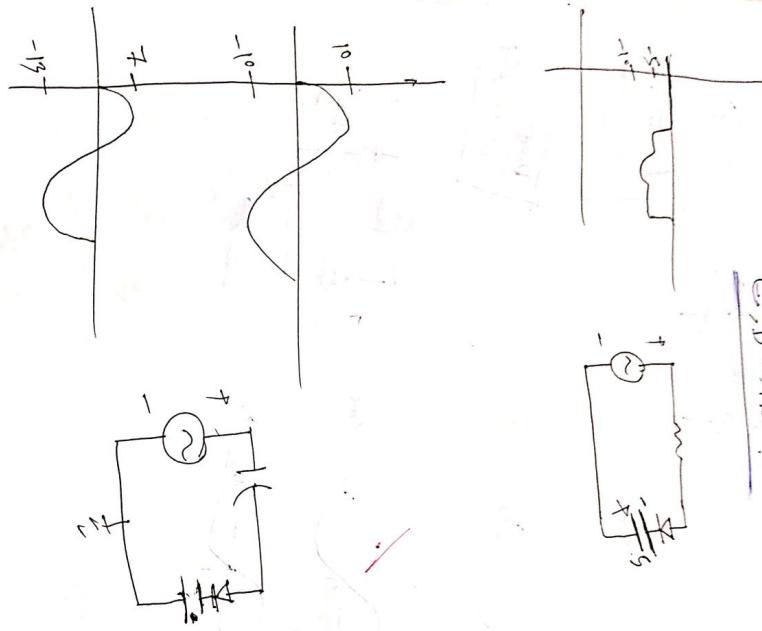
(1)

$$f = \frac{1}{\pi} \cdot \frac{1}{2\pi} \cdot \frac{1}{500 \cdot 10^{-6}}$$

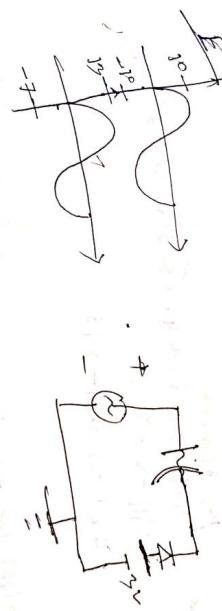
Diode  
1N4007GAP

Set C





C → D → Problem



\* Clip (रुपरेखा लेने का बारिले) ।  
\* Clamp (तापी, तापी को लेने का बारिले) ।



4 terminals:

- Drain (D) (Highly doped)
- Gate (G)
- Source (S) (highly doped)
- Body (B) (moderately doped)

→  $100^{\circ}\text{C}$   $2\text{V}$   $5^{\circ}\text{C}$  2 doped

→  $100^{\circ}\text{C}$   $5\text{V}$  1 doped

\* metal  $G: 2\text{V}$  or only Gate directly connected  $2\text{V}$ , body

Metal

oxide (insulator)

Semiconductor

of 3rd part for MOSFET (Body-Gate)- $\rightarrow$ (2nd MOS)

\* Transfer of Resistors (Transistor)

→  $\infty$  (R infinity)

→ 0 (R zero)

R of transfer  $\rightarrow$  1

Field effect transistor, of transformation  $\rightarrow$  R of transformation  $\rightarrow$

Mos

As M...G<sub>S</sub> input voltage, output current.

i/p  $\rightarrow$  Voltage  $\rightarrow V_{DS}$

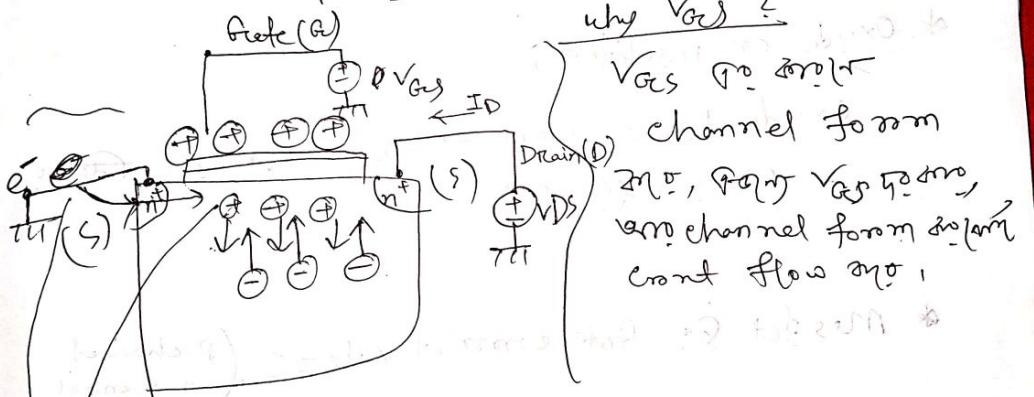
O/p  $\rightarrow$  Current  $\rightarrow I_{DS}$  or  $I_D$

D<sub>S</sub> has higher potential, S has lower potential  $\rightarrow$   $V_{DS}$  is supply voltage.

Drain & Source G<sub>S</sub>  $\rightarrow$  D<sub>S</sub> has current in it.

Current from D to S.

\* Qn. In channel MOSFET current goes from Drain to source & e<sup>-</sup> flows from Source to Drain.



why  $V_{GS}$ ?

$V_{GS} \geq 0$  for channel formation,  $V_{GS} < 0$  no channel formation so current flow zero.

At source e<sup>-</sup> to p-substrate So junction, p-substrate e<sup>-</sup> to absolve m<sup>+</sup> carrier charge or p<sup>+</sup> - positive carriers of So.

So, if D (or m<sup>+</sup>) charge is p<sup>+</sup> (or n<sup>-</sup> charge) then D<sup>+</sup> = 0.

## channel

The distance between ~~area D & S~~  
is called channel.

V<sub>GS</sub> apply on the channel form  
positive to negative, then it forms n-channel  
and p-channel to be used mosfet

\* Oxyde on insulator,

Oxyde layer form on silicon + film  
- तीव्रता द्वारा (V<sub>G</sub>)

\* Mosfet G: Gate current value = 0, (P-channel  
n-channel)

\* mosfet is a voltage control device.

Current - G - current flow in

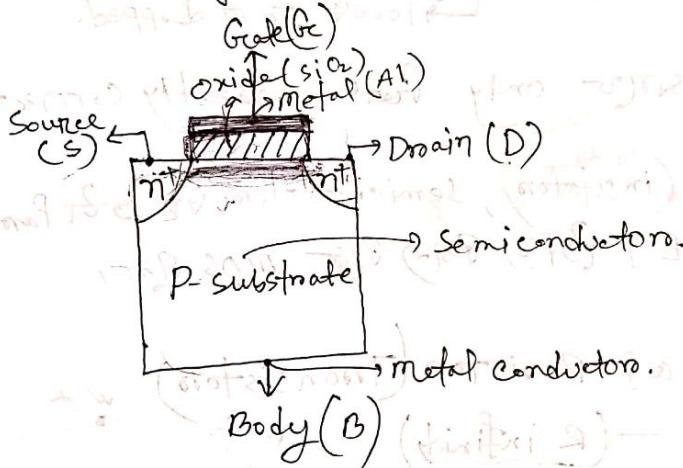
from gate control in  $V_{GS}$  (Gate voltage)

26/14/18

# MOSFET

M → metal, O → Oxide, S → Semiconductor,  
F → Field, E → Effect, T → Transistor.

- \* Block diagram of MOSFET :-



$n^+$  means highly doped.  
 $p^+$  means highly doped.

Q2: What is n-channel MOSFET.

\* Normally p-type substrate (p-substrate) तो  
इसके उपर n-type लोप्पिंग से n-channel MOSFET  
形成 है।

\* ideal MOSFET → 3 terminal device.

\* Practical MOSFET → 4 " "

\* In general MOSFET 4 terminal GTI.

+ MOSFET is a 4 terminal electronics device.

\* 4 terminals :-

→ 1000  $\Omega$  2N5500 doped.

① Drain (D) (Highly doped)

② Gate (G)

③ Source (S) (highly doped)

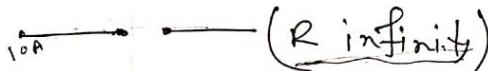
④ Body (B) (moderately doped)

→ 1000  $\Omega$  50 N doped.

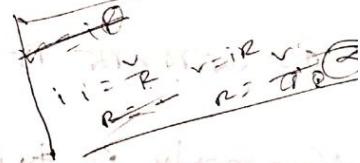
\* Metal gate will only gate directly connected.

\* Metal, oxide (insulator), semiconductor,  $\text{SiO}_2$  3-21 Pa<sub>o</sub>  
TFT - MOSFET (TFT, TFT, TFT, MOSistor,

\* Transfer of Resistor (Transistor)



∴ R, transfer  $\approx \infty$

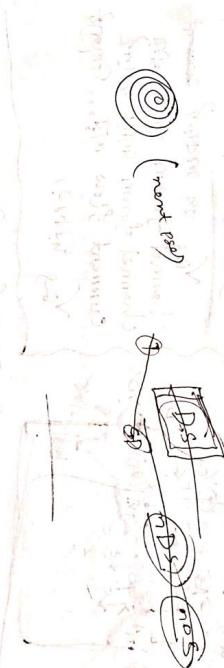


Field effect Transistor;

→ Fig. 2 R  $\Rightarrow$  transformation of

\* MOS Q: input voltage, output  $\omega$   $\rightarrow$  current.  
 $i/p \rightarrow V_{Huge} \rightarrow V_D$  (DS after higher, & source lower  
 $o/p \rightarrow$  current  $\rightarrow I_D$  On ID.

\* In channel mosFET q current flows  
from Drain to Source & e- flows from  
source to Drain.



\* Channel: The distance between D & S is called channel.

\* apply same concept of channel form 2nd test e- test, theory similar n-channel mosFET.

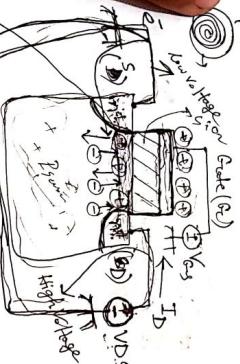
\* Oxide on insulation: Oxide layer form 2<sup>nd</sup> test  
oxide  $\rightarrow$   $\text{SiO}_2$ ,  $\text{SiO}_2 \rightarrow$   $\text{SiO}_2$ ,  $\text{SiO}_2 \rightarrow$   $\text{SiO}_2$ .

Scanned by CamScanner

MOSFET :- Gate current not  $I_G = 0$   
 $V_{GS} = 0$ . (P-channel, n-channel)

MOSFET is a voltage control device.

And, MOSFET  $\Rightarrow$  current flow  $\Rightarrow$  controlled by  $V_{GS}$  (gate voltage).



Why  $V_{GS} \neq 0$ ?  
 If  $V_{GS} = 0$ , then no current flows in the channel, so there is no current flow between drain and source.

Because P-substrate  $\Rightarrow$  N-type, & P-well after  
 P-substrate Positive charge  $\Rightarrow$  positive charge  
 So,  $V_{GS} = 0$   $\Rightarrow$  no current flow between drain and source.

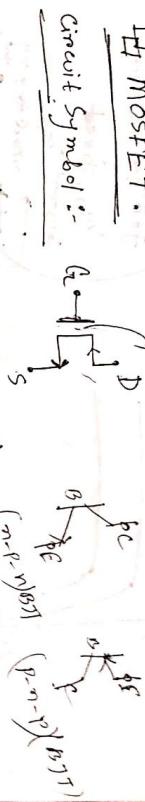
So,  $V_{GS} \neq 0$   $\Rightarrow$  current flow between drain and source.

Current  $\leftarrow$   $I_D$  (drain current)

outside part separated. 27/11/18

## MOSFET:

Circuit Symbol :-



(n-channel)

$I_D$

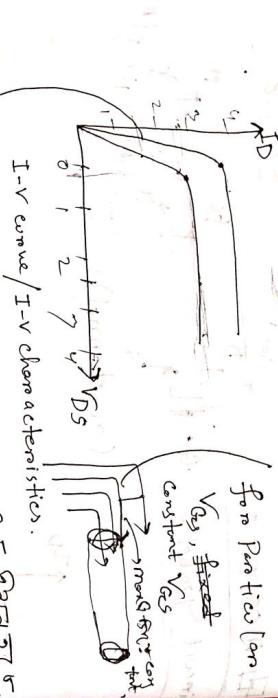
$V_t \rightarrow$  threshold voltage.

$\rightarrow V_{DS}$

- \* Body is internally connected with Source. i.e.
- \* Body - source internally shorted over an ideal MOSFET or,  $V_B = 0$ . Terminal set to zero.
- \* MOSFET is called voltage control device.
- \*  $V_{GS}$  channel sheet ( $\rightarrow$  carrier accumulate over).  
 $\rightarrow$  gate voltage.

$\approx V_t \rightarrow$  threshold voltage

- \* MOSFET on  $S_0$  condition  $\Rightarrow V_{GS} \geq V_t \rightarrow ON$
- \* 'OFF'  $\Rightarrow V_{GS} < V_t \rightarrow OFF$
- minimum amount of gate voltage for sufficient channel formation.  
channel form from  $V_{GS}$  minimum carrier velocity



I-V curve / I-V characteristics.

বেশি VGS থেকে বেশি VDS সমে তের VGS নামের চিহ্ন রয়ে।

৩ region of operation  $\Rightarrow$

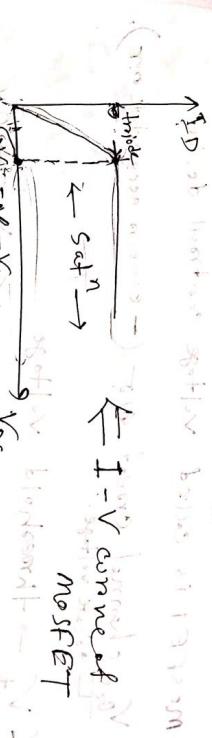
① cut-off ( $VGS < V_t$ )

② triode region

③ saturation region

② P.B  
③ R.B

③ Break down reg.



$V_{ov}$  = Overdrive voltage

- 1) cut-off ( $V_{GS} < V_t$ ) /  $V_{DS} < V_{GS} - V_t$
- 2) triode region ( $V_{DS} < V_{OV}$ ) /  $V_{DS} \geq V_{GS} - V_t$
- 3) saturation region ( $V_{DS} \geq V_{OV}$ ) /  $V_{DS} \geq V_{GS} - V_t$

note  
① MOSFET on/off identity,

② condition curve identify for region & wrt.

$$I_D = \mu n C_{ox} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \rightarrow \text{triode.}$$

$$I_D = \frac{1}{2} \mu n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_t)^2 \rightarrow \text{satn.}$$

where  
W → drain current & carrier moving from source

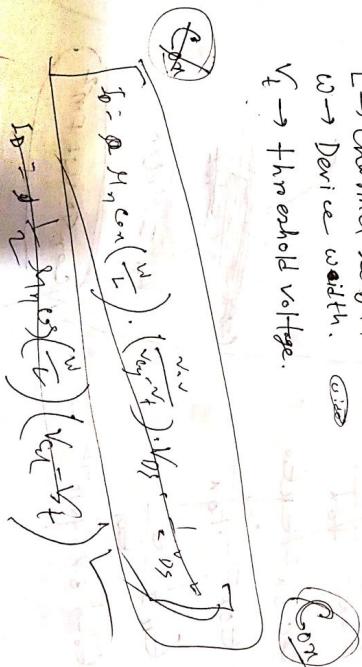
$\mu n$  → Mobility of  $e^-$ . current more move more cur.

$C_{ox}$  → oxide capacitance.

$L$  → channel length.

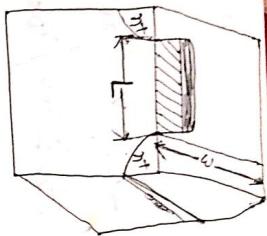
$w$  → Device width.

$V_t$  → threshold voltage.



$$I_D = \mu n C_{ox} \left( \frac{W}{L} \right) \cdot (V_{GS} - V_t) \cdot V_{DS} \cdot \left( 1 + \frac{V_{DS}}{V_{OV}} \right)$$

$$I = \frac{dQ}{dt}$$



$\propto$  Mobility  $\propto I$  (current)

$\propto$  Capacitance,  $C = \frac{Q}{V}$

$\propto$  MOSFET saturation region or constant current source (IDS) condition.

$$C_{ox} = \frac{\epsilon_0 \epsilon_r}{t_{ox}}$$

$$\epsilon_{ox} = \epsilon_r \epsilon_0$$

$$\therefore \epsilon_{ox} = \frac{C_{ox}}{t_{ox}}$$

$$\epsilon_0 \rightarrow 8.854 \times 10^{-12}$$

$$\mu_{n,ox}$$

$$C_{ox} \text{ unit } F/m^2$$

\* Consider a process technology for which  $t_{\text{min}} = 0.4 \mu\text{m}$ ,  $t_{\text{ox}} = 8 \mu\text{m}$ ,  $A_{\text{min}} = 450 \mu\text{m}^2$ ,  $V_t = 0.7 \text{ V}$ ,  $\epsilon_{\text{ox}} = 5$ .

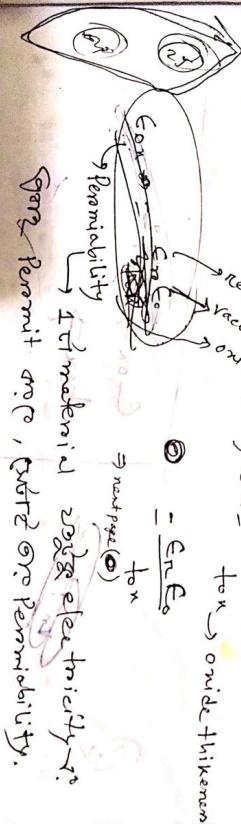
① find  $C_{\text{ox}}$  &  $k_t^*$ .

- ② For a MOSFET with  $w/l = 3.4 \mu\text{m}/0.8 \mu\text{m}$   
calculate the value of  $V_{\text{DS, min}}$  needed to  
operate the transistor in saturation region with  
 $I_D = 100 \mu\text{A}$ .

$$\textcircled{1} \quad C = \frac{\epsilon A}{d} \quad \Rightarrow \quad \frac{C}{A} = \frac{\epsilon}{d} \quad \Rightarrow \quad C_{\text{ox}} = \frac{\epsilon}{d}$$

$$\textcircled{2} \quad C_{\text{ox}} = \frac{C}{A} = \frac{\epsilon}{d} \quad \Rightarrow \quad C_{\text{ox}} = \frac{\epsilon}{d}$$

$$C_{\text{ox}} = \frac{\epsilon}{d_{\text{ox}}}$$



Relative permittivity  
vacuum  $\rightarrow$   $\epsilon_0$   
oxide thickness  $\rightarrow$   $t_{\text{ox}}$

$$\Rightarrow C_{\text{ox}} = \frac{\epsilon_0 \epsilon}{t_{\text{ox}}} \rightarrow \text{oxide thickness}$$

$$\Rightarrow C_{\text{ox}} = \frac{\epsilon_0 \epsilon}{t_{\text{ox}}}$$

Relative permittivity

1st material  $\rightarrow$  electricity  $\rightarrow$   
permittivity,  $\epsilon$ ,  $\epsilon_0$ ,  $\epsilon_r$ ,  $\epsilon_{\text{r}}$ ,  $\epsilon_{\text{r}}$ ,  $\epsilon_{\text{r}}$ ,  $\epsilon_{\text{r}}$

Relative Permittivity,  $\epsilon_r = \frac{\epsilon}{\epsilon_0}$  → Relative permittivity,  $\epsilon_0$  → vacuum Gr. Permi.

$$\epsilon_r = \frac{\epsilon}{\epsilon_0} = \frac{8.854 \times 10^{-12}}{8.85 \times 10^{-12}}$$

$$\Rightarrow \text{Conc} = \frac{\epsilon_{\text{ext}}}{\text{Torr}} = \frac{\epsilon_{\text{real}}}{\text{Torr}}$$

$$= \frac{8.854 \times 10^{-12}}{8.85 \times 10^{-12}}$$

$f_{\text{real}}$

$$= 5.53 \times 10^{-4} \text{ F m}^{-2}$$

$$= 0.00553 \text{ pF m}^{-2}$$

$\text{D} = 0.01 = \text{C}$

$$k_m' = \text{mobility of } e^-$$

$$= 4 \times 450 \times 10^{-4} \times 5.53 \times 10^{-2}$$

$$\approx 2.5 \times 10^{-4} \left( \frac{\text{m}^2}{\text{Vs}} \cdot \frac{\text{F}}{\text{m}^2} \right) \rightarrow \text{Unit of } k_m'$$

$$= 2.5 \times 10^{-4} \text{ F m}^{-2} \text{ Vs}^{-1}$$

$$\text{Ans: } 0.0024886 \frac{\text{F}}{\text{Vs}}$$

Ans.  $k_m' = 0.0024886 \text{ F m}^{-2} \text{ Vs}^{-1}$

Ans.  $k_m' = 0.0024886 \text{ F m}^{-2} \text{ Vs}^{-1}$

$$\text{Conc} \Rightarrow \text{F m}^{-2}$$

$$\text{Conc} \Rightarrow \frac{1}{\text{Torr}}$$

$$\text{Conc} \Rightarrow \text{F m}^{-2}$$

$$\text{Conc} \Rightarrow \text{F m}^{-2}$$

$$⑥ V_{DS} \geq V_{DS} - V_t$$

$$\Rightarrow V_{DS} \geq V_{DS} - 0.7$$

$$\Rightarrow V_{DS\min} = V_{DS} - 0.7$$

so in region G,

$$I_D = \frac{1}{2} k_n \frac{w}{L} (V_{GS} - V_t)^2$$

$$I_D = \frac{1}{2} \times 2.5 \times 10^{-4} \times \frac{8}{0.8} \times (t_0 - 0.89)^2$$

$$(t_0 - 0.89)$$



$$V_{GS} = \sqrt{0.8 \times 10^{-4}}$$

$$= 2.828 + 0.7$$

$$= 3.528$$

$$V_{GS} = t_0 - 0.89$$

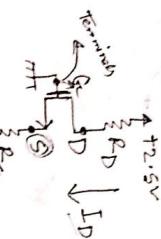
$$t_0 - 0.89 = \sqrt{0.8 \times 10^{-4}}$$

$$= 2.828$$

$$t_0 - 0.89 = \sqrt{0.8 \times 10^{-4}} = 2.828$$

$$V_{DS} = 2.828 - 0.7$$

Ex. Example - 4.21



$$I_D = 0.4 \text{ mA}$$

$$V_D = 0.5 \text{ V}$$

$$V_t = 0.7 \text{ V}$$

$$\text{or } \ln \alpha = 100 \text{ mV/V}$$

$$L = 1 \text{ nm}$$

$$w = 2.5 \text{ nm}$$

*for some  
more  
info.*

- 0.5V

(a)  $R_D = ?$

$$R_D = \frac{2.5 - 0.5}{0.4}$$

$$= 5 \text{ k}\Omega$$

for finding Mosfet's region:

①. 0.7V - FF char.

(b)  $R_s = ?$

$$R_s = \frac{V_s - (-2.5)}{I_D}$$

$$= \frac{-1.5 + 2.5}{0.4}$$

$$= 5 \text{ k}\Omega$$

$$I_D = \frac{1}{2} \cdot n \cdot C_{ox} \left( \frac{\omega}{L} \right) (V_{xy} - V_t)$$

$$\Rightarrow 0.4 \times 10^{-3} = \frac{1}{2} \times 10^0 \times 10^{-6} \times \frac{32}{1} (V_{xy} - 0.7)$$

$$\Rightarrow V_{xy} = 1.2 \text{ V}$$

$$\Rightarrow V_G - V_S = 1.2$$

$$\Rightarrow 0 - V_S = 1.2$$

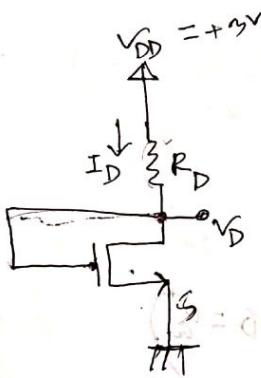
$$\Rightarrow V_S = -1.2 \text{ V}$$

$V, R, I$

$$V = IR$$

$$I = \frac{V}{R}$$

$$R = \frac{V}{I}$$



$$(I_D) = 80 \text{ mA}$$

$$V_T = 0.6 \text{ V}$$

$$r_{\pi} \text{ con } = 200 \text{ mV/A}$$

$$L = 0.8 \text{ m}$$

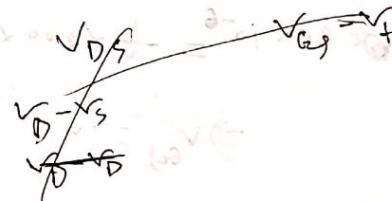
$$w = 4 \text{ m}$$

(a)  $V_D = ?$

(b)  $R_D = ?$

$$R_D = \frac{V_D - V_S}{I_D}$$

$$= \frac{3 - 1}{80}$$



$$V_D = V_{DD} - V_{DS}$$

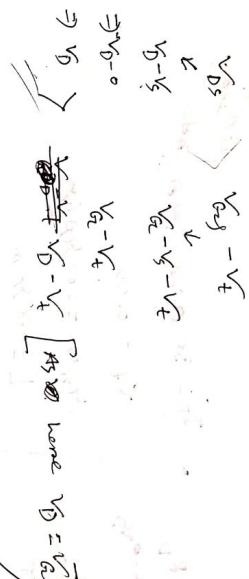
$$V_D = 2 - 0.6$$

$$V_D = 1.4 \text{ V}$$

② In circuit & Drain  $\rightarrow$  Gate short circuit,

$$\therefore V_D = V_{DG}$$

Finding mosfet's region:



$$\therefore I_D = \frac{1}{2} g_m \cos\left(\frac{\omega}{L}\right) (V_{GS} - V_t)^2$$

$$\Rightarrow I_D = 80 \times 10^{-6} = \frac{1}{2} \times 200 \times 10^{-6} \times \frac{9}{0.8} \times (V_{GS} - 0.6)$$

$$\Rightarrow V_{GS} = 1V$$

$$\Rightarrow V_{DS} = 1V$$

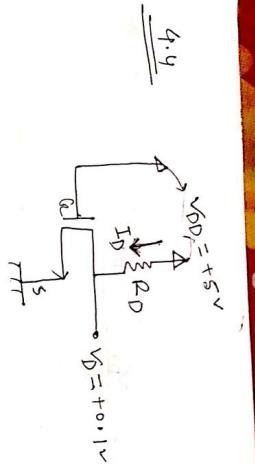
$$\Rightarrow V_{DG} = 1V$$

$$\therefore V_D = 1V.$$

4.4

$$V_{DD} = +5 \text{ V}$$

Tuesday  
MOSFET Q: forward,  
Magnet theory.



~~$R_D = ? \quad R_{DS} = ?$~~

$$R_D = \frac{V_{DD} - V_D}{I_D}$$

$$\left| \begin{array}{l} V_t = 1 \text{ V} \\ k_n' \left( \frac{w}{L} \right) = 1 \text{ mA/V}^2 \end{array} \right.$$

$$V_{DS}$$

$$V_{GS} - V_t$$

$$V_D - V_S$$

$$V_G - V_S - V_T$$

$$V_D - V_t$$

$$V_G - V_t$$

: third region

$$\begin{aligned} \therefore I_D &= k_n' \left( \frac{w}{L} \right) \left[ (V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \\ &= 1 \times 10^{-2} \left[ 5 - 0 - 1 \right] \times (0.1 - 0) - \frac{1}{2} \times (0.1)^2 \end{aligned}$$

$$= 4.995 \text{ mA}$$

$$\therefore R_D = \frac{V_{DD} - V_D}{I_D} = \frac{5 - 0.1}{0.001} = 4995 \Omega$$

$$= 12.4 \text{ k}\Omega$$

4/12/18

## BJT (Bipolar Junction Transistor)

Transistor  
is a three terminal device.



E = emitter.

B = base. (A + R)

C = collector.

- \* BJT is a  $\pm 3$  terminal device.
- \* BJT is a  $\pm 3$  terminal device.

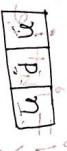
Symbol of emitter (E)

Symbol of base (B)  
or  
Symbol of collector (C)

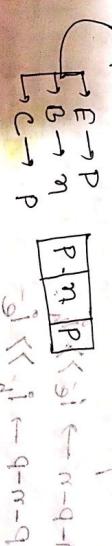
Two Junctions  
- EBJ (Emitter base junction)  
- CBJ (Collector base junction)

- \* BJT has two Junctions.  
- EBJ (Emitter base junction)  
- CBJ (Collector base junction)

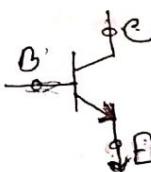
Types of BJT:



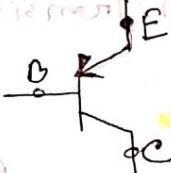
① n-p-n  
    p-n-p.



## \* Circuit Symbol:



(carries majority carriers)



$$(n-p-n) \text{ and } (p-n-p)$$

both have = 3

{ \* MOSFET is a Unipolar device.  
\* BJT is a bipolar device.

\* BJT, why bipolar?

negative terminal

} Unipolar  $\rightarrow$   
single polarity  
either only + carriers or - carriers  
so major current flow  
exists,

\* n-channel MOSFET

G only e<sup>-</sup>  $\rightarrow$  ?  
Current flow  $\rightarrow$  ?

p-channel  $\rightarrow$  ?  
MOSFET G only hole  
(+) carriers  $\rightarrow$  ?  
current flow  $\rightarrow$  ?  
so, MOSFET  $\rightarrow$

Unipolar device

other circuit

positive type G

Polarity concern

so for TGT

current flow  $\rightarrow$

\* BJT, why bipolar:

BJT ( $\rightarrow$  current flow

because, current flows due

to both type of carriers (+ e<sup>-</sup>) and (holes)

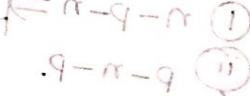
$$i = i_h + i_e = i_{hole} + i_e$$

for TGT to connect

n-p-n / p-n-p

$$n-p-n \rightarrow i_e >> i_h$$

$$p-n-p \rightarrow i_h >> i_e$$



## Bipolar Junction Transistor (BJT)

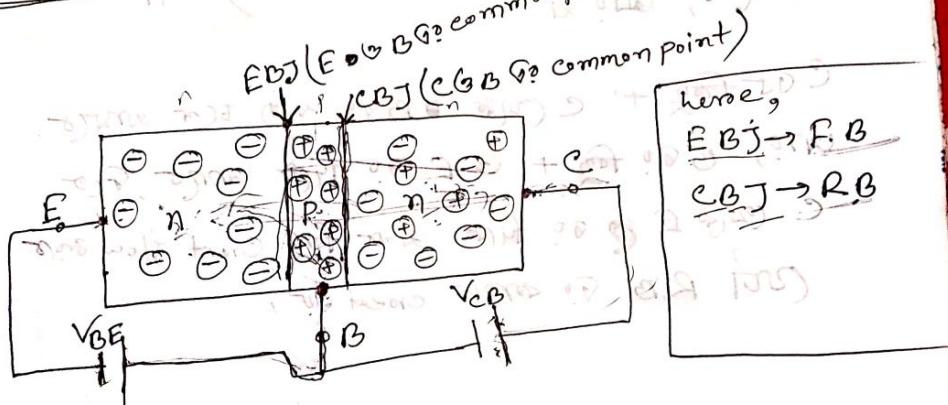
### \* Construction

E → highly doped

B → lightly doped (carrier  $2 \times 10^{14} \text{ cm}^{-3}$ ) ( $10^6 \text{ or } 5 \times 10^5 \text{ cm}^{-3}$ )

C → moderately " (carrier  $10^7 \text{ to } 10^8 \text{ cm}^{-3}$ ) ( $10^7 \text{ to } 100-200 \text{ cm}^{-3}$ )

### \* Working Mechanism of BJT :-



here,  $e^-$  flow  $\rightarrow E \rightarrow C$  }  $n-p-n$  BJT  
current " "  $\rightarrow C \rightarrow E$

\* base is lightly doped and  $2\mu$ , so that it can't absorb much  $e^-$  / To ensure lower absorption rate. on base, that's why base is lightly doped and ??

\* Why emitted highly damped?

Ans: base far  $e^-$  absorb more and less  
near far  $e^-$  C (O) reach zero magnet.

\* C do  $e^-$  current flow & C do (current)  
more & magnet, so, C do highly damped.  
more (cm<sup>2</sup>), ~~area~~

C do -> + C (magnet) & B do.  $\propto$  C do current.

so, B do + C E do  $\propto$  C do current, C do

C do & E do  $\propto$  C do current flow & C do  
but R.B do more current.

Tension =  $\frac{1}{2} \cdot B^2 \cdot A$   $\propto$  B<sup>2</sup>  $\propto$  current<sup>2</sup>

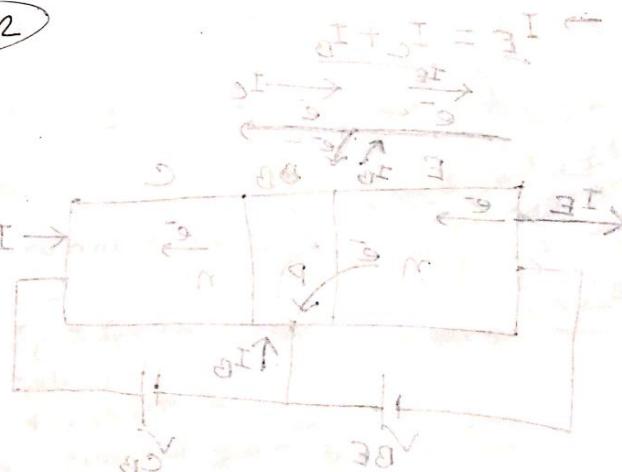
time constant  $\propto$  mass  $\propto$  magnetic field  $\propto$  area  $\propto$   
mass  $\propto$  current  $\propto$  current  $\propto$  time  $\propto$  time

## Mode of operations:

- ① cut-off  $\rightarrow$  RB  $\rightarrow$  RB
- ② Active  $\rightarrow$  FB  $\rightarrow$  FB
- ③ Saturation  $\rightarrow$  FB  $\rightarrow$  FB
- ④ Reverse active  $\rightarrow$  RB  $\rightarrow$  FB

Transistor biasing:

CS AR



with biasing  $\rightarrow$  Horizontal OT

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BJT eqns:

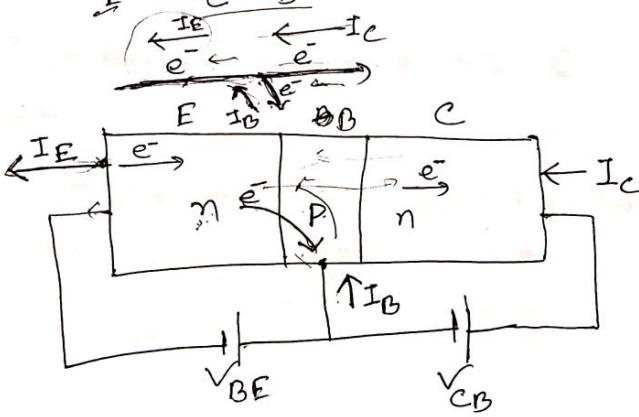
→ common base current gain  $\alpha = \frac{I_C}{I_E}$

→ common emitter current gain  $B = \frac{I_C}{I_B}$

$$\rightarrow \alpha = \frac{\beta}{1+\beta}$$

$$\rightarrow \beta = \frac{\alpha}{1-\alpha}$$

$$\rightarrow I_E = I_C + I_B$$



BJT  $\Rightarrow$  3 terminal  $\Rightarrow$  3 terminal current flow

qn?

①  $I_E \rightarrow$  Emitter current

②  $I_B \rightarrow$  Base "

③  $I_C \rightarrow$  collector "

\* n-p-n BJT Q<sub>1</sub> (positive outgoing current at collector terminal, incoming current at base terminal & incoming current at base terminal & incoming current at base terminal)

at C.R.B G.O. current incoming  
at E " " outgoing

$$\text{Current (Q1)} \quad I_E = I_C + I_{EB} \quad [\text{Total incoming} = \text{total outgoing}]$$

\* gain = output & input G.O. ratio.

& must be > 0. Saturation region (at & amplifier for G.O. & we get 20).

& J.T. Active

& use over 20% current gain,  $\alpha = \frac{I_C}{I_E}$  (more than 20%)

& → common

→ as  $I_E = I_C + I_B$  (at 20%)

always  $I_E > I_C$  or  $I_E > I_B$

& common emitter current gain,  $B = \frac{I_C}{I_B}$

& → Common emitter here,  $B \gg 1$  (already)

$$C_2, I_C \gg I_B$$

\* At E G.O.  $100 e^{-\beta \cdot 20 \text{ mV}}$  0.8-0.9999  $e^{-2}$  & diodes are only 1-2 & B.C.  $\beta_1 \approx 20$  mV  
 $I_C, I_E \approx I_E$  ( $I_E$  almost  $I_E$  G.O. zero, but not exact zero)  
 $I_E > I_C$ ,

\* Base current,  $I_B \approx 0, 0.00$  amperes, but present

in  $\text{BJT}$

because of parasitic resistance in the circuit

\* High power application (e.g.  $\text{BJT}$  use over 100W)

\* Low power application (e.g. "MOSFET" or FET)

Explain

$$\alpha = \frac{I_C}{I_E}$$

$$\beta = \frac{I_C}{\alpha I_E}$$

$$\Rightarrow 1 + \beta = \frac{I_C}{I_E} + 1$$

$$1 + \beta = \frac{I_C + I_B}{I_E}$$

$$\Rightarrow 1 + \beta = \frac{I_C + I_B}{I_E}$$

$$(N.B.) \quad 1 + \beta = \frac{I_C + I_B}{I_E}$$

$$\frac{I_C}{I_E} = \frac{B}{1 + \beta}$$

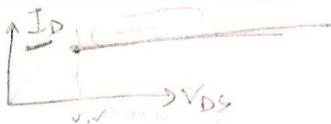
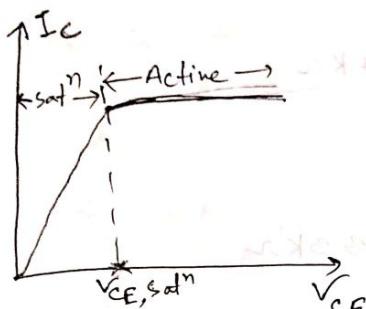
$$\frac{I_C}{I_E} = \frac{B}{1 + \beta}$$

$$\frac{I_C}{I_E} = 1 + \beta$$

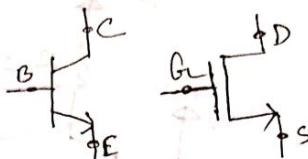
$$\frac{I_C}{I_E} = 1 + \beta$$

$$x_2 =$$

\* Inv curve:



$(I_D - V_{DS})_{\text{curve}}$   
MOSFET  
 $G = mV$   
Compare w/ graph  
in draw  
and?



(n-p-n) BJT

\*  $V_{BE} = 0.7$  for  $Sat^n$  & active

$V_{CE}, Sat^n = 0.2$  v only for  $V_{CE}$ .

\* BJT as amplifiers

\* BJT works as an amplifier in the active region.

\* ... .. , a switch in the saturation &

cut-off region.

\* BJT is a current control device. ( $I_B$   $\rightarrow$  control)

\* MOSFET is a voltage controlled device ( $V_G$   $\rightarrow$  control)

\* In BJT,  $i_c = \beta i_b$

(So, if,  $i_b = 0, i_c = 0$ )

$$V_o = \frac{i_e}{I_o} \cdot I_o$$

$$I_c = I_o \times \alpha$$

$$A_v = \frac{V_o}{V_i} = \frac{i_e}{I_o} = \alpha$$

\*  $V_{TF}$  or photo, light, heat  $\rightarrow$  current flow

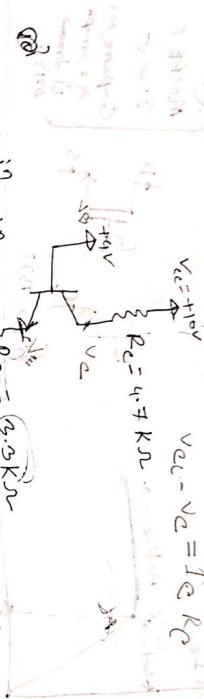
$$\Delta I_{CE} = 1 \times \frac{\alpha}{\alpha+1} = \frac{\alpha}{\alpha+1} = \frac{x}{1+x}$$

## Meth

Transistor  
Diagram

$$V_{CE} = +10V$$

$$V_{CE} - V_E = I_C R_C \quad \downarrow$$



Q2

on activation of input voltage  $V_E$  and  $R_E = 1M\Omega$

Q. Find all node voltages & all branch currents

$$I_B = 100 \cdot (I_E, I_{BE} = ?, V_E, V_B, V_C = ?)$$

Solve AT ON

$$V_{BE} = 0.7V.$$

$$\Rightarrow V_B - V_E = 0.7$$

$$\Rightarrow V_B = 4.7V$$

$$V_E = 0.7V$$

$$V_C = 9.3V$$

$$I_E = 1mA$$

$$I_E = \frac{V_E}{R_E}$$

$$I_E = 1mA$$

We know,

$$\beta = \frac{I_E}{I_B}, \alpha = \frac{I_E}{I_B}$$

Given  $\beta = 100, \alpha = 0.99$

$$\alpha = \frac{I_E}{I_E + I_B}$$

$$\frac{I_E}{I_E} = \frac{0.99}{0.99 + 1}$$

$$\Rightarrow I_E = 0.99mA$$

$$I_E = 0.99mA$$

$$I_E = 0.99mA$$

$$I_E = 0.99mA$$

$$I_E = \frac{V_E}{R_E}$$

$$I_E = 0.99mA$$

$$I_E = 0.99mA$$

$$I_E = 0.99mA$$

$$I_E = 0.99mA$$

$$I_E = I_C + I_B$$

$$\Rightarrow I_B = I_E - I_C$$

$$= 0.01 \text{ mA}$$

$$V_{CC} - V_C = I_C R_C$$

$$\Rightarrow V_C = V_{CC} - I_C R_C$$

$$= 10 - 4.7 \times 0.01$$

$$= 5.3 \text{ V}$$

Ans:

Process:

BJT is active region:

Step-1: Apply  $V_{BE} = 0.7$ , we will get  $V_B$  or  $V_E$ ,

Step-2: Calculate either  $I_E$  or  $I_B$  (Step 1  $V_B$  or  $V_E$  and  $\alpha$  or  $B$  are given present  $R$ )

Step-3: Calculate  $I_{C,0}$  using the value of  $\alpha$ ,  $B$  conversion

- To find  $I_{C,0}$  refer to the  $IE$  vs  $T$  graph

Step-4: Calculate another current using,  $I_E = I_C + I_B$ ,

Step-5: Calculate  $V_C$  using  $V_C = V_{CC} - I_C R_C$ ,

$$V_C = IR$$



$$V_E = 0$$

$$V_E = I_E R_E$$

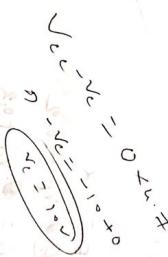
$$\Rightarrow V_E = 0V$$

$$V_B = 0V$$

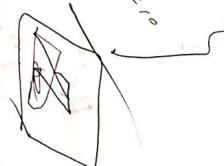
$$V_C = V_{CE} - I_C R_C$$

$$\Rightarrow V_C = 10V$$

Ans:



$$\begin{aligned} V_{CE} - V_C &= 10V \\ V_C &= -10V \\ V_E &= 10V \end{aligned}$$



Sol Practice  
Ans.  $V_{BE} = 0.7V$ ;  $\text{satn} \Rightarrow V_{CE} = 0.2V$ .

$$\alpha = \frac{I_C}{I_E}$$

$$\alpha b = \frac{I_C}{I_B}$$

$$1 + b = \frac{I_C}{I_B} + 1$$

$$\boxed{1 + b = \frac{\alpha}{\alpha b} + 1}$$

$$\alpha = \frac{\alpha}{1 + b} \rightarrow \boxed{\alpha}$$

$$\frac{I_C}{I_E} = \frac{\alpha}{1 + b}$$

$$A_{Hh} = 0.9$$

$$= 0.9 \cdot 0.96 = 0.864$$

$$I_E = I_C + I_B$$

$$= 1.6mA$$

$$I_E = \frac{V_E - V_{BE}}{R_E}$$

$$= 0.96mA$$

$$I_C = \frac{V_E - V_{CE}}{R_C}$$

$$= 0.47mA$$

(2)

$$\begin{aligned} I_E &= \frac{V_E - V_{BE}}{R_E} \\ &= \frac{5.5V - 0.7V}{2k\Omega} \\ &= 1.8mA \\ V_E &= 5.5V \\ V_{BE} &= 0.7V \\ V_{CE} &= 0.2V \end{aligned}$$

(3)

$$\begin{aligned} I_E &= \frac{V_E - V_{BE}}{R_E} \\ &= \frac{5.5V - 0.7V}{2k\Omega} \\ &= 1.8mA \end{aligned}$$

$$I_C = \frac{V_E - V_{CE}}{R_C}$$

$$= 0.47mA$$

$$\begin{aligned} V_E &= 5.5V \\ V_{BE} &= 0.7V \\ V_{CE} &= 0.2V \end{aligned}$$

(4)

$V_E = 10V$

$I_E = \sqrt{2 \cdot 10 \cdot 2k\Omega}$

$I_E = 4.7mA$

$I_C = 4.7mA$

$V_{BE} = 0.7V$

$V_{CE} = 10V$

saturation region of transistor

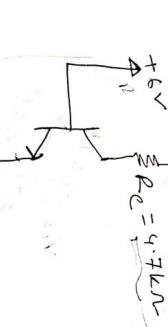
$$I_E = \frac{V_E - V_{BE}}{R_E}$$

$$= 10V - 0.7V$$

$$= 9.3V$$

$$= \frac{9.3V}{2k\Omega}$$

$$= 4.7mA$$



$$I_E = 4.7mA$$

$$I_C = 4.7mA$$

$$V_E = 10V$$

$$V_{BE} = 0.7V$$

$$V_{CE} = 10V$$

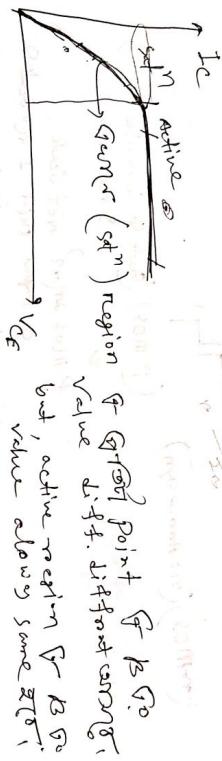
$$I_E = 4.7mA$$

$$I_C = 4.7mA$$

$$V_E = 10V$$

and why  $\beta$  was max in saturation region.

$$\beta = \frac{I_c}{I_B} = \frac{0.96}{0.64} = 1.5$$



\* B active &  $\beta$  (value) fixed, so  $I_c$  always same.

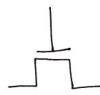
①BJT & MOSFET characteristics.

- ② Most BJT & BJT characteristics are similar.  
MOSFET has more drain current flow rate,  
so, MOSFET can handle more power, but  
TGT is better if it is used in high frequency.

## Cmos

### Implementation of Logic gate:-

cmos implementation



(n-MOS) (<sup>no arrow sign</sup>)



(p-MOS) (gate & bubble exist) <sup>g no arrow</sup>

p-MOS (<sup>not</sup> gate)

Not Gate, input 1 & 0, Gate 0

1 1 0 0 0 0 0 0

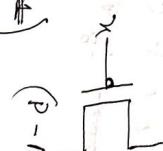
n-MOS or n-channel MOSFET

input  $n = 0 \Rightarrow$  OFF  
 $n = 1 \Rightarrow$  ON

OR gate logic 1 (~~OR~~  
off in logic 0. (~~1.5~~)



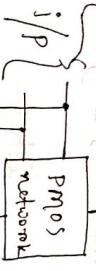
~~n-MOS~~,  
~~input, n = 0~~  $\Rightarrow$  ON (~~1.5~~)



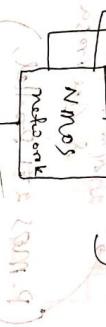
(p-MOS)

bubble

switch (on/off) with voltage applied to them  
current flow through voltage applied to them



N-MOS network



N-MOS

$V_t = 1.5 \text{ V}$  (always +)

$v_s \geq 1.5 \rightarrow 1$  (logic 1)  
 $v_s < 1.5 \rightarrow 0$  (logic 0)

P-MOS

$V_t = -1.5 \text{ V}$  (always -)

$v_s = -2.5 \rightarrow 0$  (logic 1)  
 $v_s > -2.5 \rightarrow 1$  (logic 0)

→ logic 1

→ logic 0

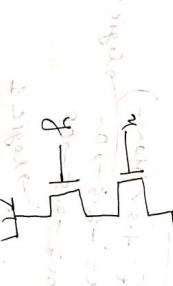
Logic 1 / Logic 0 → Represent numerically (by resistor value (smallest logic 1 → zero value))  
or logic 0.

complementary MOSFET/complementary Mos  
CMOS implementation of NAND gate.  $f = \overline{xy}$



two PMOS series or NMOS series  
and vice versa.

(PMOS & NMOS parallel)  
CMOS, i.e. Series

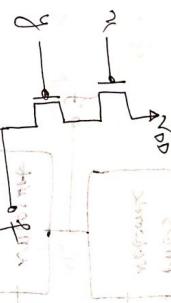
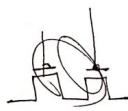


Truth Table:

x	y	f
0	0	1
0	1	1
1	0	1
1	1	0

$\overline{xy} \rightarrow D_{nwo}$  the CMOS circuit with dynamic  
of NAND gate (from astm)  
Any input diode.

~~to design~~  
de CMOS implementation of NOR gate;  $f = \overline{x+y}$



\* 2nd input  
inverter  
and  
PMOS  
and NMOS  
not

inverter  
buffer  
PMOS  
not

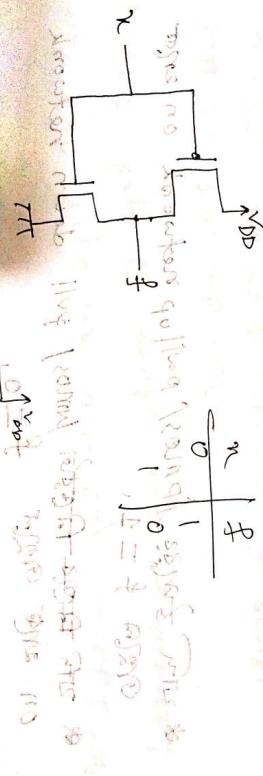
PMOS  
not

x	y	f = $\overline{x+y}$
0	0	1
0	1	0
1	0	0
1	1	0

\* If you want to implement NOR gate using NMOS only then  
you have to invert the inputs and then feed them to the NOR gate.

inverter

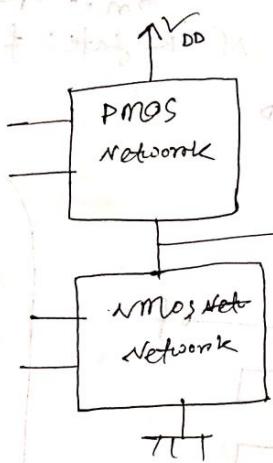
$$f = \overline{x+y}$$



using NMOS only  
inverters  
and  
NMOS  
not

inverter

29/22/28



\* Why PMOS/NMOS are not used rather than CMOS:-

→ CMOS ensures non floating output.

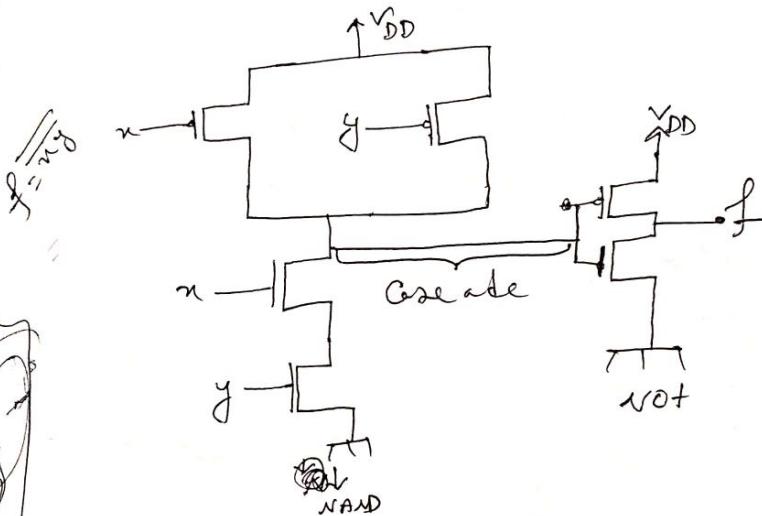
→ We always get an output in CMOS whether it's '0' or '1'.

→ CMOS also ensures minimum cost, cause it

\* With PMOS pull up network on one OR gate f = 1.

\* With NMOS pull down network on one OR gate f = 0.

\* CMOS implementation of AND Gate :-



Cascade → 1st stage तो output (⇒ 2nd stage  
तो input रिमूट कर दें।

\* AND & OR gate (⇒ design करना क्या है)  
Step 1: NAND, NOR, NOT (⇒ design करना क्या है)  
Step 2: 1st step NAND.

\* NAND gate (⇒ design करना क्या है) mosFET  
but, AND gate क्या करना 6 टो mosFET करना

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## CMOS implementation of Boolean fn:

$$f = ( )$$

- OR  $\rightarrow$  PMOS series
- AND  $\rightarrow$  PMOS Parallel
- no inverting i/p

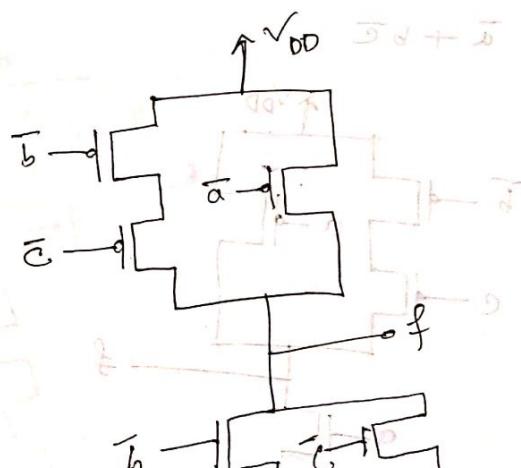
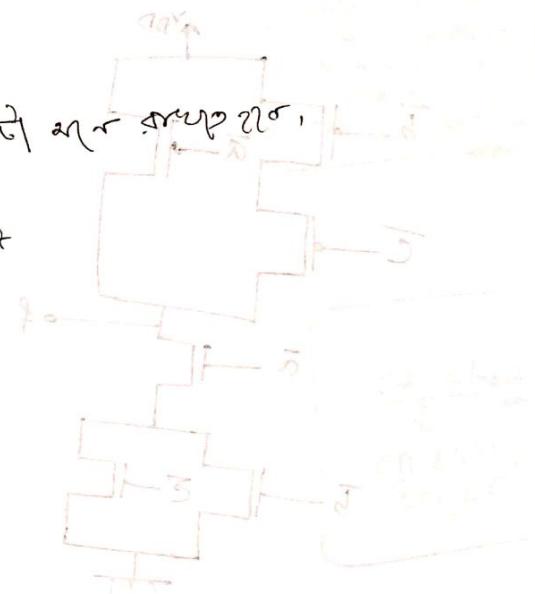
original input

~~f~~

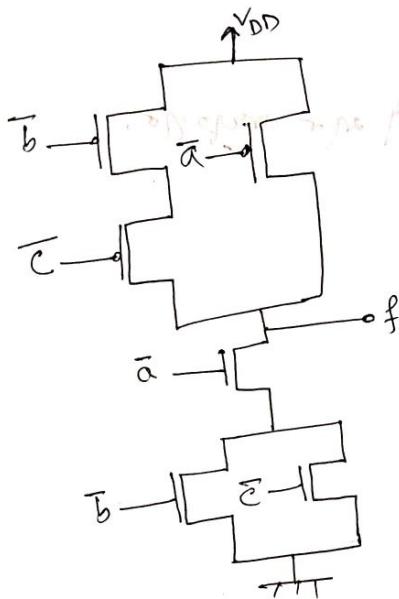
$$\tilde{f} = ( )$$

- OR  $\rightarrow$  PMOS Parallel
- AND  $\rightarrow$  PMOS Series
- inverting i/p.

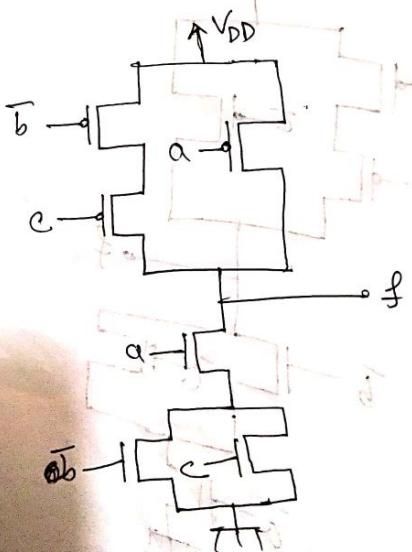
$$\begin{aligned}
 f &= \frac{a+bc}{a+b+c} \\
 &= \frac{a+bc}{\overline{a} \cdot bc} \\
 &= \frac{a}{\overline{a}} \cdot \frac{b+c}{b+c} \\
 &= \overline{a} \cdot (b+c)
 \end{aligned}$$



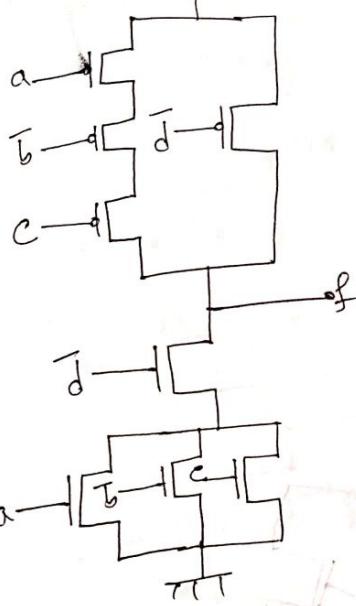
$$* f = a + bc$$



$$* f = \bar{a} + b\bar{c}$$



$$* f = \bar{a}b\bar{c} + d$$

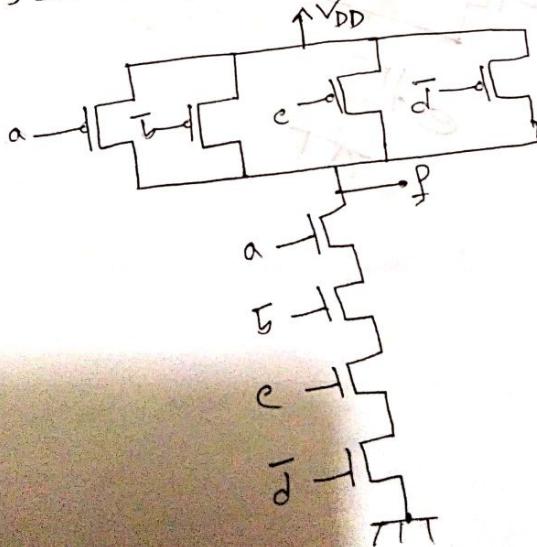


$$\bar{a} + b (\bar{a} + \bar{b})$$

~~common  
source, common  
drain, common  
drain~~

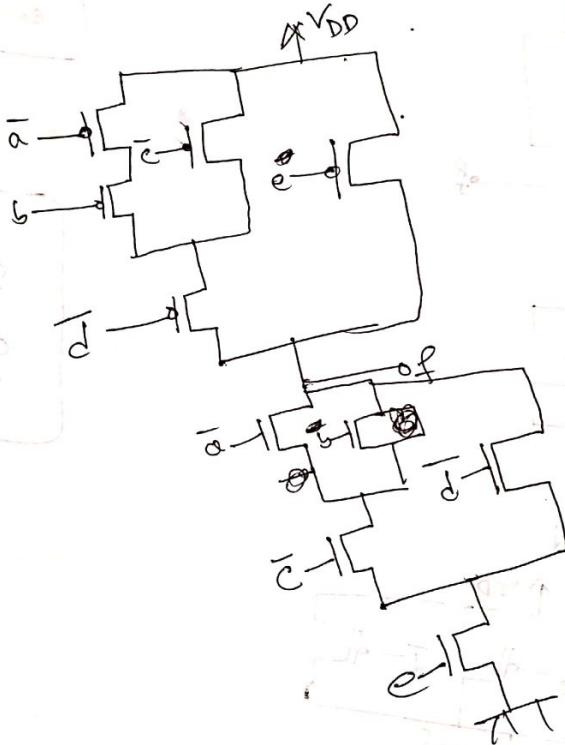
BJT abin sin  
BJT & abin  
sin & lee (N)  
BJT common  
transistor, common  
abn sin & lee  
common & common  
common opo inde  
details

$$* f = \bar{a} + b + \bar{c} + d$$



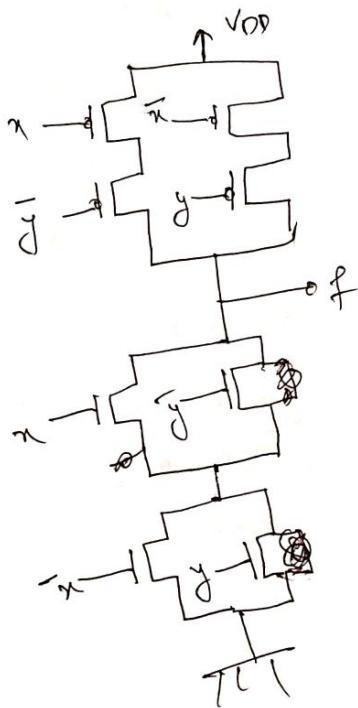
ct-6 (next day)  
cmos Q.  
forget,

( ) (or2  $\rightarrow$  pull)  $\rightarrow$  And  $\rightarrow$  series (invert input)

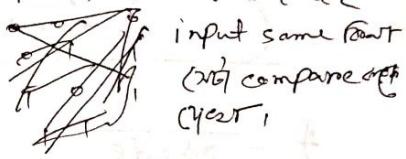


$$x * f = x \oplus y$$

$$= \bar{x}y + x\bar{y}$$

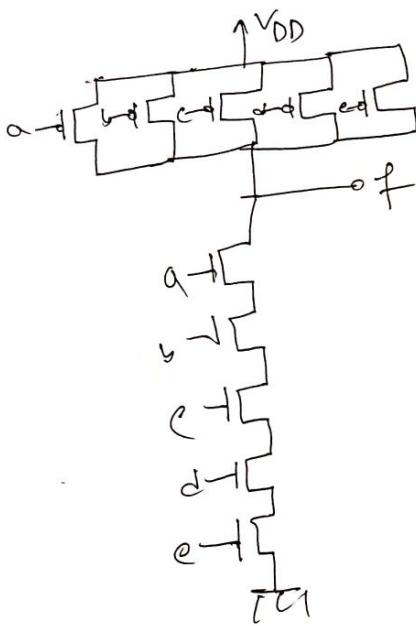


input same 2<sup>nd</sup> output 0, x or y gives 1<sup>st</sup>  
input same point  
(not compare diff  
point)



$A + B$  or  $\rightarrow$  Smaller,  $A \cdot B$  and  $\rightarrow$  Parallel

$$f = \overline{abcde}$$

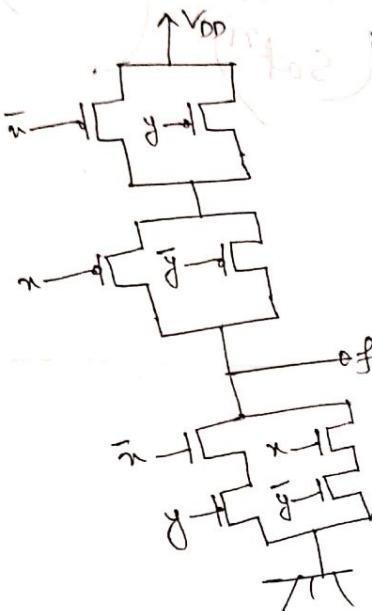


\* Triode Region So cont  $\Rightarrow$  two trip  $\Rightarrow$  inspect  
emc only.

X-NOR Gate:

$$f = \overline{\bar{x}\bar{y} + \bar{y}\bar{x}}$$

(at)



010 43 80 15 12

$$f = \bar{x}\bar{y} + \bar{y}\bar{x}$$