



Assignment (2)

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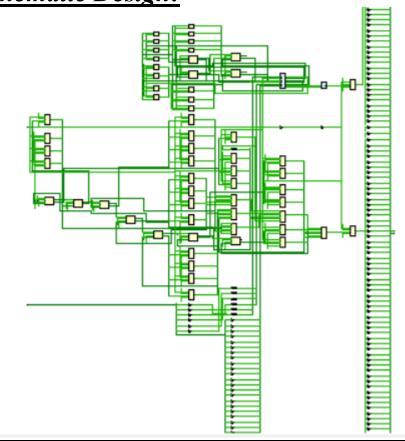
Submission Date: 14.4.2020

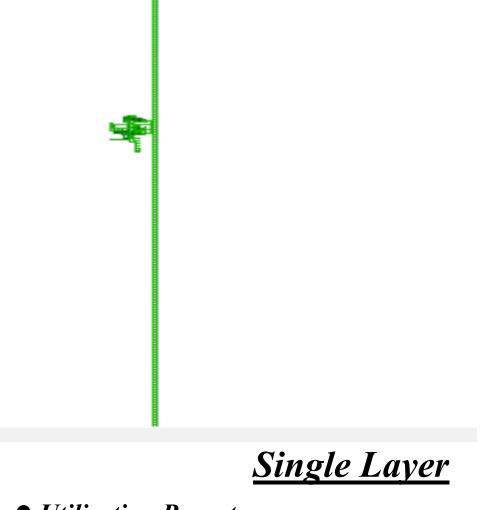
Single Layer

• **Utilization Report:**

+	+-		+		+		+-		+
Site Type	İ	Used				Available			İ
Slice LUTs*		7590	i	0	Ċ	53200			i
LUT as Logic	I	7590	I	0	I	53200	I	14.27	I
LUT as Memory	I	0	I	0	I	17400	I	0.00	I
Slice Registers	I	1019	I	0	I	106400	I	0.96	I
Register as Flip Flop	I	1019	I	0	I	106400	I	0.96	I
Register as Latch	I	0	I	0	I	106400	I	0.00	I
F7 Muxes	I	0	I	0	I	26600	I	0.00	I
F8 Muxes	I	0	I	0	I	13300	I	0.00	I
+	+-		+		+		+-		+

• Schematic Design:

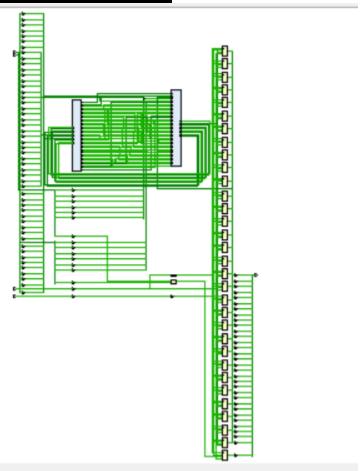




• <u>Utilization Report:</u>

D +	+	+		+		+-	+
1 Site Type	Use	ed	Fixed	I	Available	I	Util%
2 +	+	+		+		+-	+
3 Slice LUTs*	24	14	0	I	53200	I	0.46
4 LUT as Logic	1 24	14	0	I	53200	I	0.46
5 LUT as Memory	I	0	0	I	17400	I	0.00
6 Slice Registers	1 3	32	0	I	106400	I	0.03
7 Register as Flip Flop	3	32	0	I	106400	I	0.03
B Register as Latch	I	0 [0	I	106400	I	0.00
9 F7 Muxes	1	0 [0	I	26600	I	0.00
0 F8 Muxes	1	0	0	I	13300	I	0.00
1 +	+	+		+		+-	+

• Schematic Design:

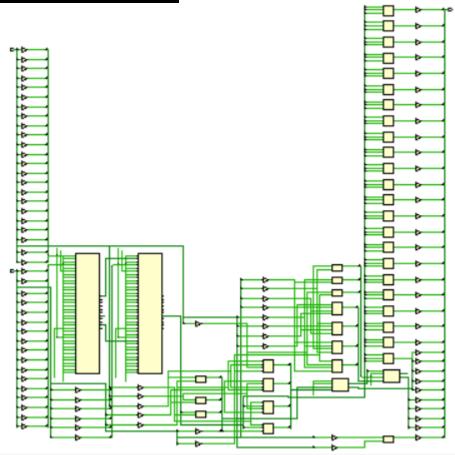


Multiplier

• <u>Utilization report:</u>

Site Type	i	Used	į	Fixed	į	Available	į	Util%
Slice LUTs*	i	21	i	0	i	53200	i	0.04
LUT as Logic	1	21	I	0	I	53200	I	0.04
LUT as Memory	1	0	I	0	I	17400	I	0.00
Slice Registers	1	0	I	0	I	106400	I	0.00
Register as Flip Flop	1	0	I	0	I	106400	I	0.00
Register as Latch	1	0	Ī	0	I	106400	I	0.00
F7 Muxes	1	0	I	0	I	26600	I	0.00
F8 Muxes	1	0	I	0	I	13300	I	0.00
+	+-		+		+		+	+

• Schematic Design:

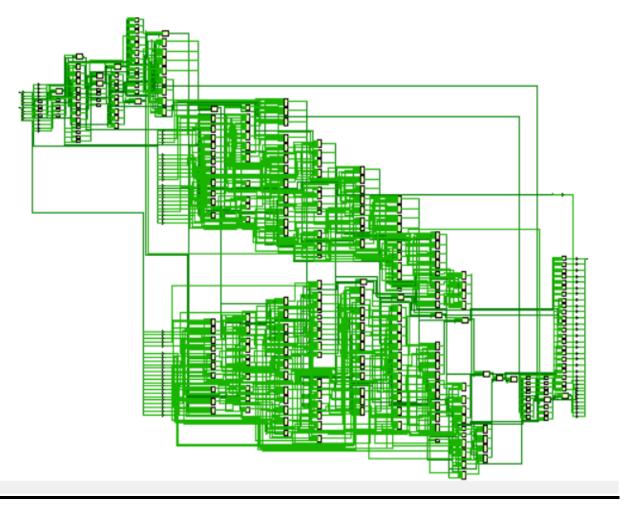


<u>Adder</u>

• **Utilization Report:**

	-+-		-+		-+		+-	+
Site Type	Ì	Used	İ	Fixed	I	Available	İ	Util%
Slice LUTs*	ı	204	ī	0		53200	ı	0.38
LUT as Logic	1	204	I	0	I	53200	I	0.38
LUT as Memory	1	0	I	0	I	17400	I	0.00
Slice Registers	1	0	I	0	I	106400	I	0.00
Register as Flip Flop	1	0	I	0	I	106400	I	0.00
Register as Latch	1	0	I	0	I	106400	I	0.00
F7 Muxes	1	0	I	0	I	26600	I	0.00
F8 Muxes	1	0	I	0	I	13300	I	0.00
+	-+-		+		+		+-	+

Schematic Design:



<u>Pipeline</u>

PipeLined 3-stage

