Assignment (2)

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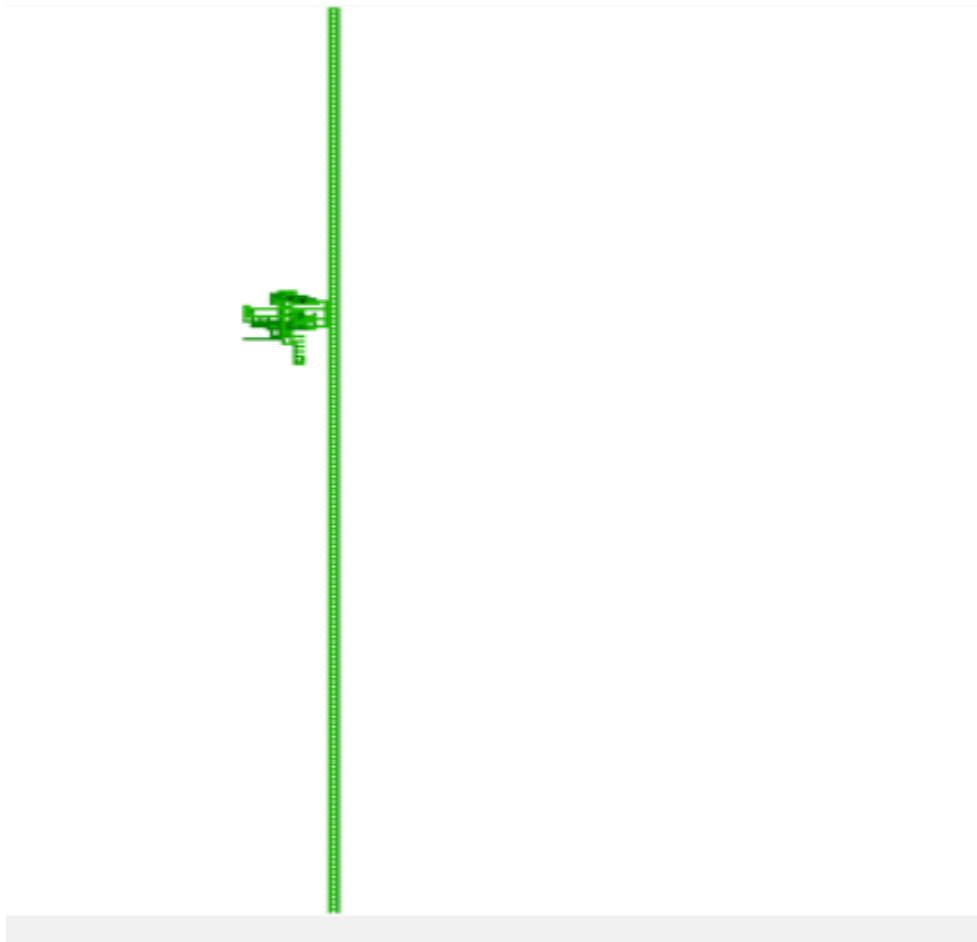Mohamed ELSayed   1170239

Submission Date: 14.4.2020

Single Layer

- ## *Utilization Report:*

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+---------------------------+------+-------+-----------+-------+
|        Site Type          | Used | Fixed | Available | Util% |
+---------------------------+------+-------+-----------+-------+
| Slice LUTs*               | 7590 |    0  |     53200 | 14.27 |
|   LUT as Logic            | 7590 |    0  |     53200 | 14.27 |
|   LUT as Memory           |    0 |    0  |     17400 |  0.00 |
| Slice Registers           | 1019 |    0  |    106400 |  0.96 |
|   Register as Flip Flop   | 1019 |    0  |    106400 |  0.96 |
|   Register as Latch       |    0 |    0  |    106400 |  0.00 |
| F7 Muxes                  |    0 |    0  |     26600 |  0.00 |
| F8 Muxes                  |    0 |    0  |     13300 |  0.00 |
+---------------------------+------+-------+-----------+-------+
```
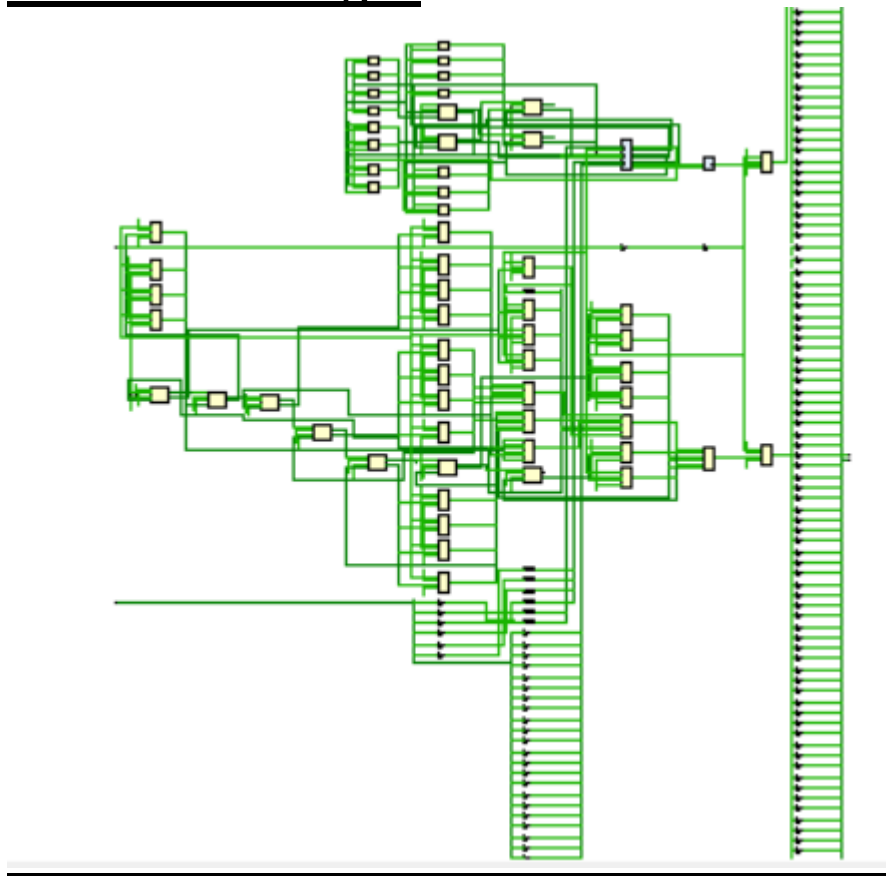
- ## *Schematic Design:*

Single Layer

- ## Utilization Report:

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	244	0	53200	0.46
LUT as Logic	244	0	53200	0.46
LUT as Memory	0	0	17400	0.00
Slice Registers	32	0	106400	0.03
Register as Flip Flop	32	0	106400	0.03
Register as Latch	0	0	106400	0.00
F7 Muxes	0	0	26600	0.00
F8 Muxes	0	0	13300	0.00

• _Schematic Design:_
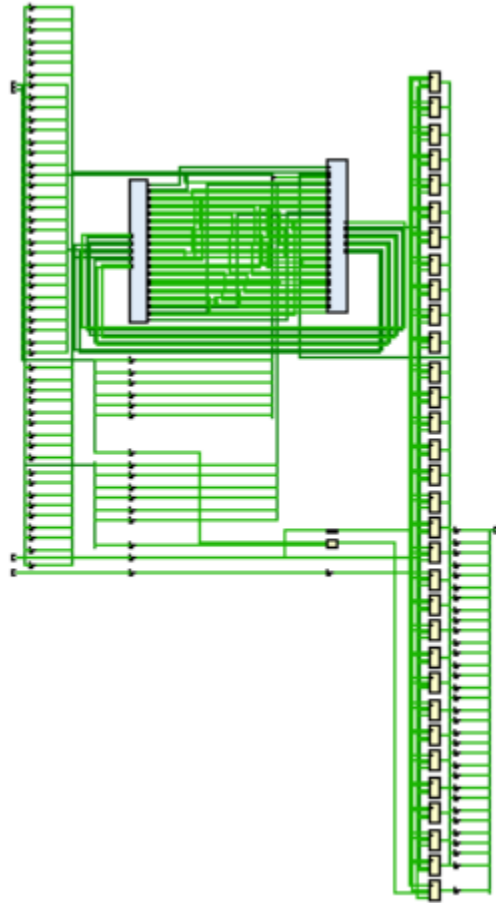
Multiplier

• _Utilization report:_

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	21	0	53200	0.04
LUT as Logic	21	0	53200	0.04
LUT as Memory	0	0	17400	0.00
Slice Registers	0	0	106400	0.00
Register as Flip Flop	0	0	106400	0.00
Register as Latch	0	0	106400	0.00
F7 Muxes	0	0	26600	0.00
F8 Muxes	0	0	13300	0.00

- ## *Schematic Design:*
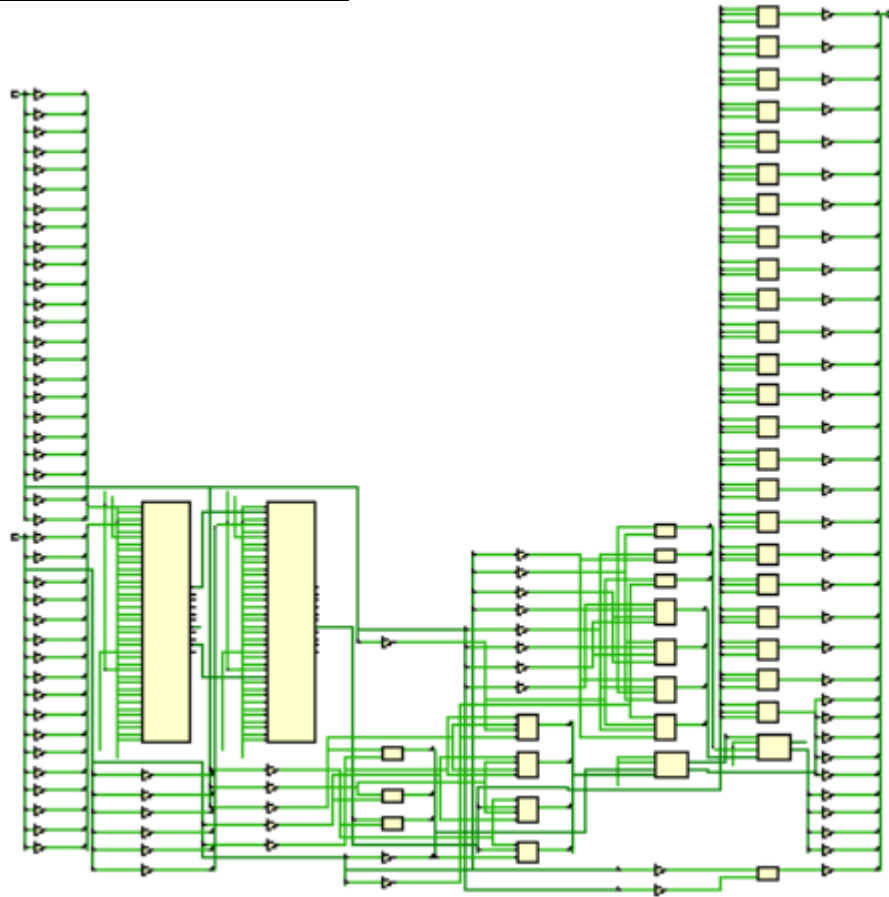
Adder

- ## *Utilization Report:*

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	204	0	53200	0.38
LUT as Logic	204	0	53200	0.38
LUT as Memory	0	0	17400	0.00
Slice Registers	0	0	106400	0.00
Register as Flip Flop	0	0	106400	0.00
Register as Latch	0	0	106400	0.00
F7 Muxes	0	0	26600	0.00
F8 Muxes	0	0	13300	0.00

- ## *Schematic Design:*
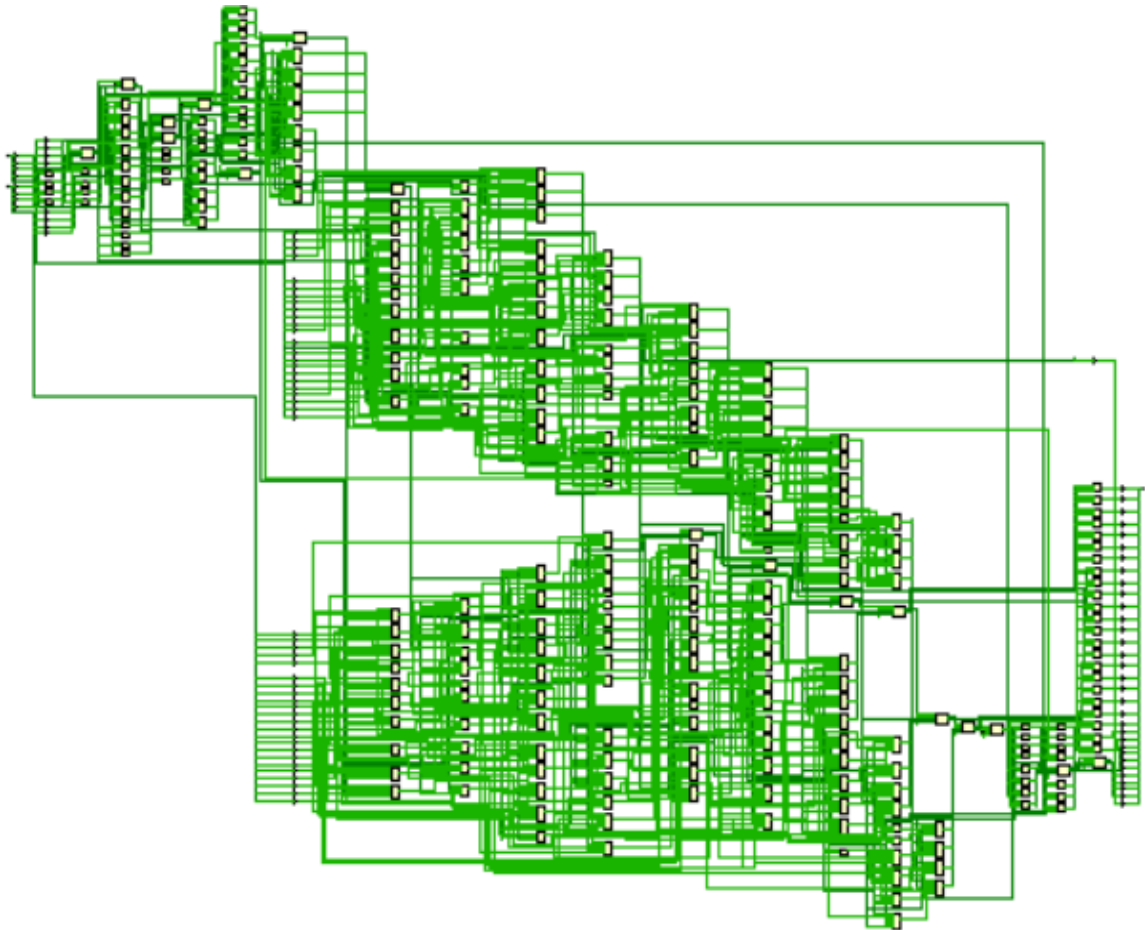
Pipeline

PipeLined 3-stage