Chittagong University of University of Engineering & Technology

Department of Electrical and Electronic Engineering

Project Name:

Designing and Testing Schematics, Symbol and Layout of 8 to 3 Bit Encoder

Course No: EEE490

Course Title: VLSI Technology Sessional

Level-4, Term-2

Submitted by

Name : Md Sayedul

ID : 1702079

Name : Jakaria Khan Sakib

ID : 1702092

Submitted to

Md Mahmudul Hasan Tareq

Assistant Professor

Dept. of EEE, CUET

Objectives:

The objectives of this experiment are

1. To design a 8 to 3 binary encoder (Schematic and Layout) using CMOS Technology and create symbol.
2. To observe DRC simulation and verify it with schematics diagram.
3. To observe LVS simulation and verify it with schematics diagram.

Abstract:

This experiment introduces **Cadence Virtuoso Software** which provides an environment to simulate our Verilog codes and test whether it works as it has to. Using this we designed the schematic of a 8 to 3 binary encoder.

Theory:

The combinational circuits that change the binary information into N output lines are known as **Encoders**. The binary information is passed in the form of 2^N input lines. The output lines define the N-bit code for the binary information. In simple words, the **Encoder** performs the reverse operation of the **Decoder**. At a time, only one input line is activated for simplicity. The produced N-bit output code is equivalent to the binary information.

The 8 to 3 line Encoder is also known as **Octal to Binary Encoder**. In 8 to 3 line encoder, there is a total of eight inputs, i.e., Y_0, Y_1, Y_2, Y_3, Y_4, Y_5, Y_6, and Y_7 and three outputs are A_0, A1, and A_2. In 8-input lines, one input-line is set to true at a time to get the respective binary code in the output side. Below are the block diagram and the truth table of the 8 to 3 line encoder.

Required Software:

1. CADENCE-VMware Workstation Software
2. MS word 2016

Truth Table:

INPUTS								OUTPUTS		
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	A2	A1	A0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

A2=Y4+Y5+Y6+Y7
A1=Y2+Y3+Y6+Y7
A0=Y1+Y3+Y5+Y7

4 Input OR Gate

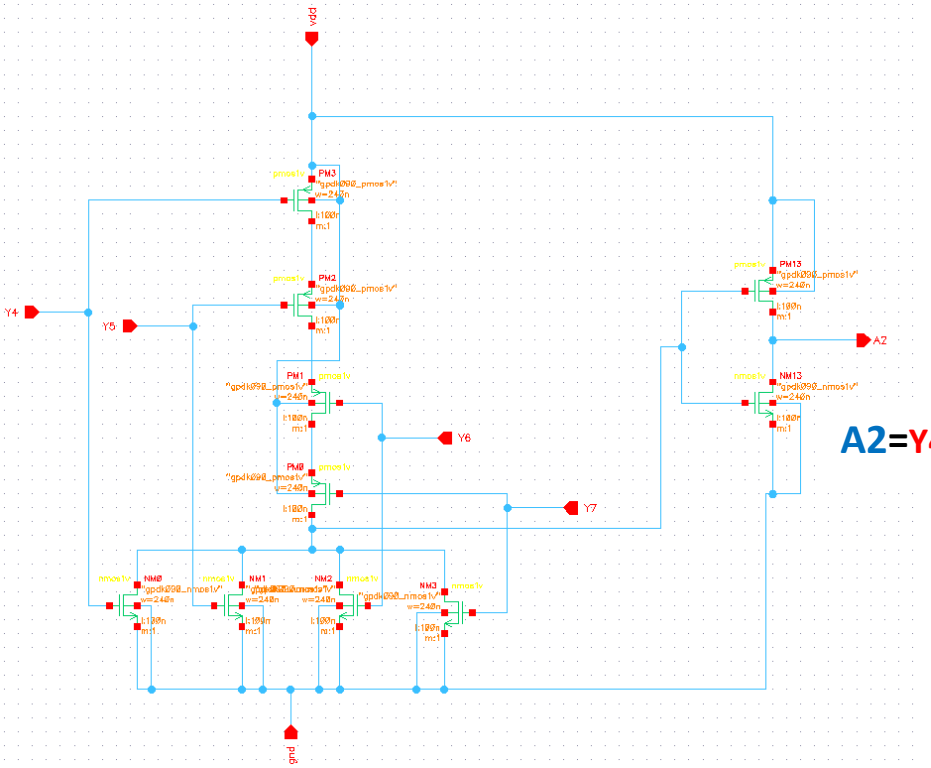


Fig.1. 4 input OR gate Schematic.

4 Input OR Gate Symbol

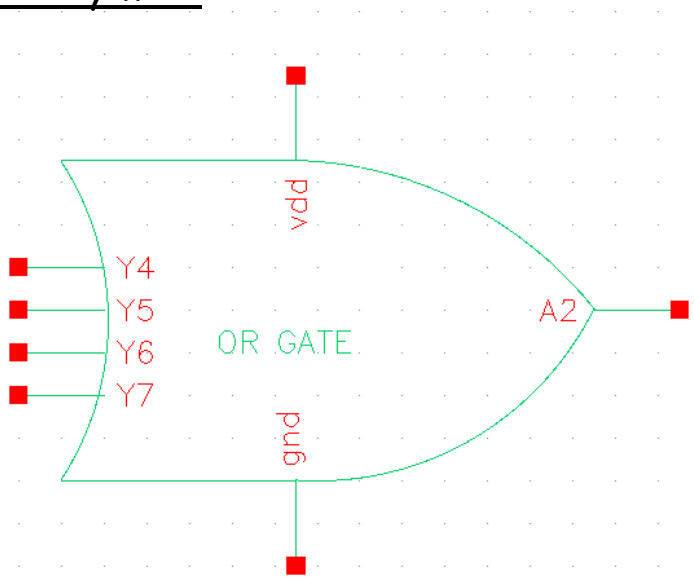


Fig.2. 4 input OR gate symbol

8 to 3 Encoder Implementation Using OR Gate

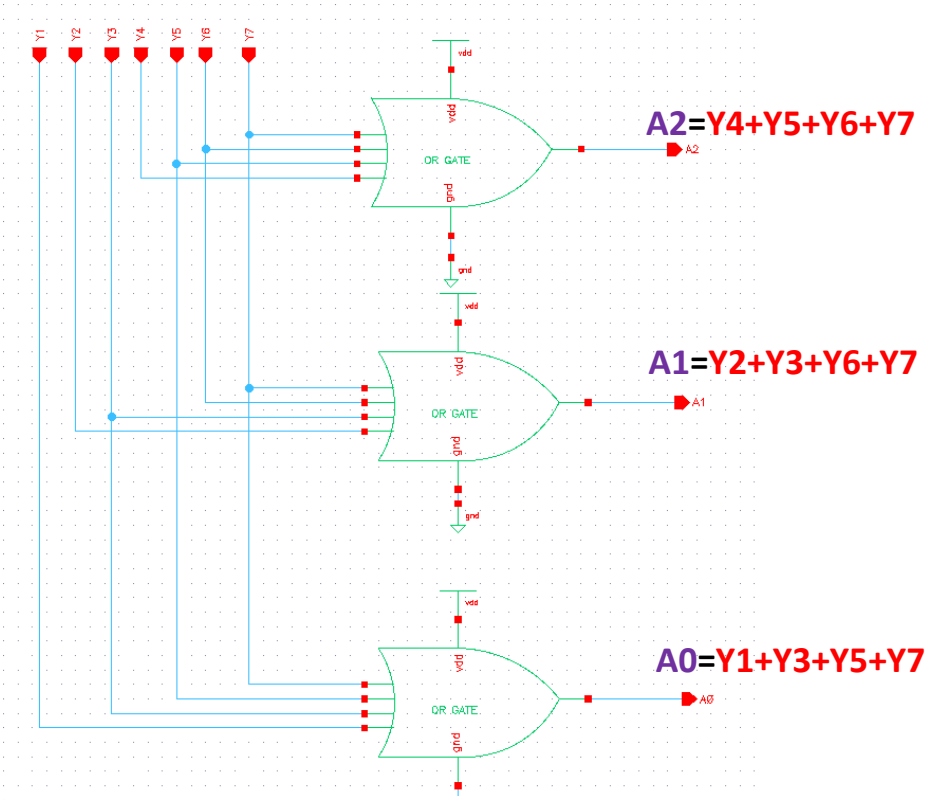


Fig.3. 8 to 3 encoder implementing using OR gate

8:3 Encoder Schematic Design

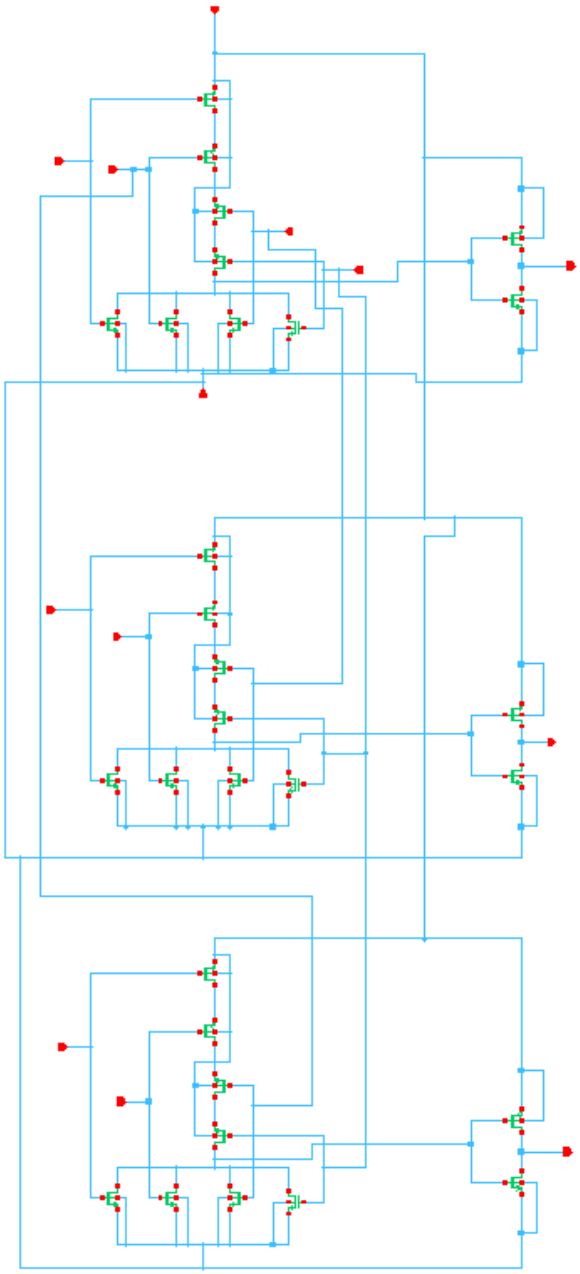


Fig.4. 8 to 3 encoder schematic design using CMOS

Symbol of 8:3 Encoder

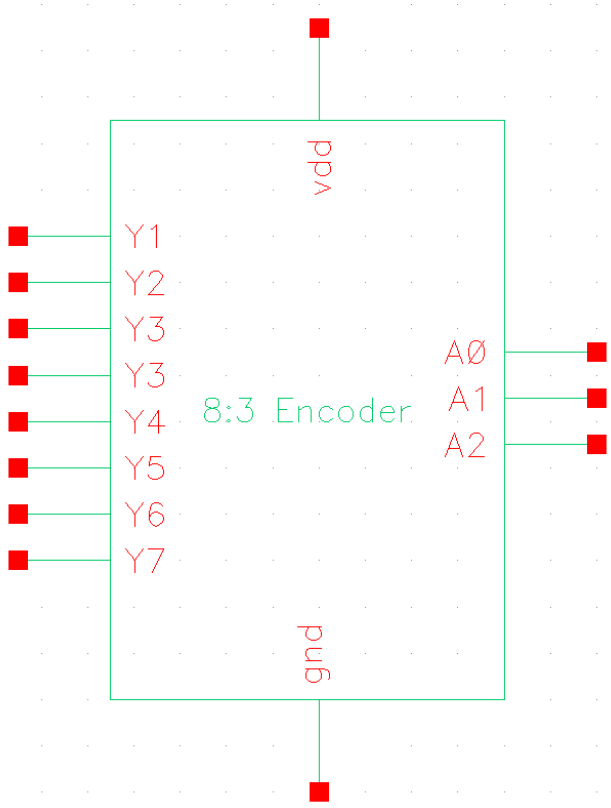


Fig.5. 8 to 3 encoder symbol

Output

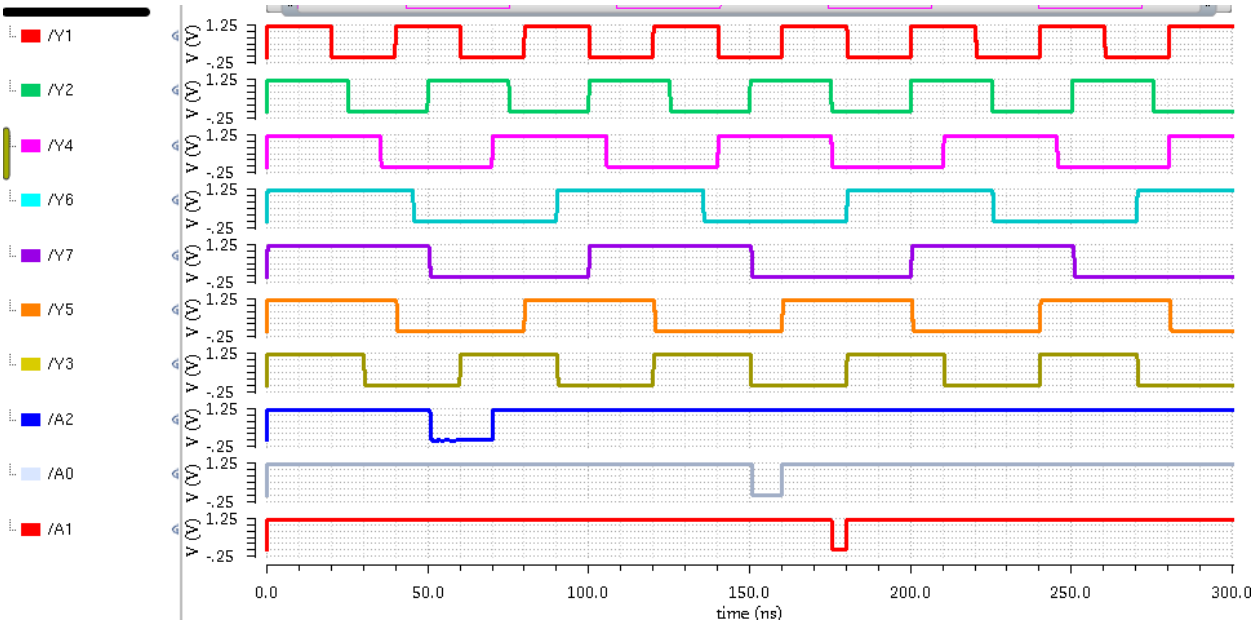


Fig.6. Input output waveform of 8 to 3 encoder.

4 Input OR Gate layout

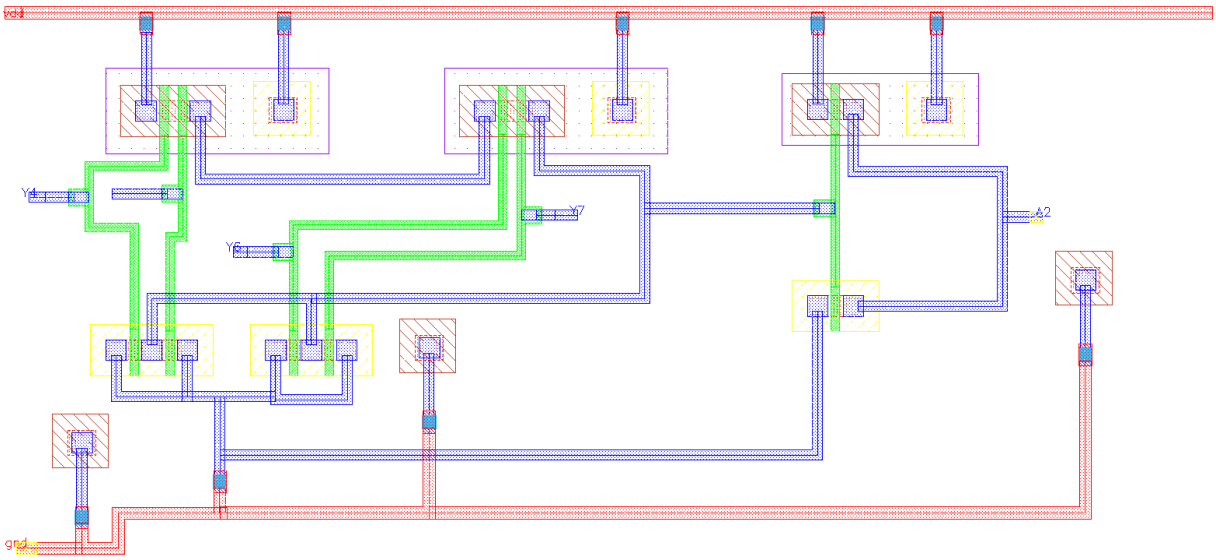
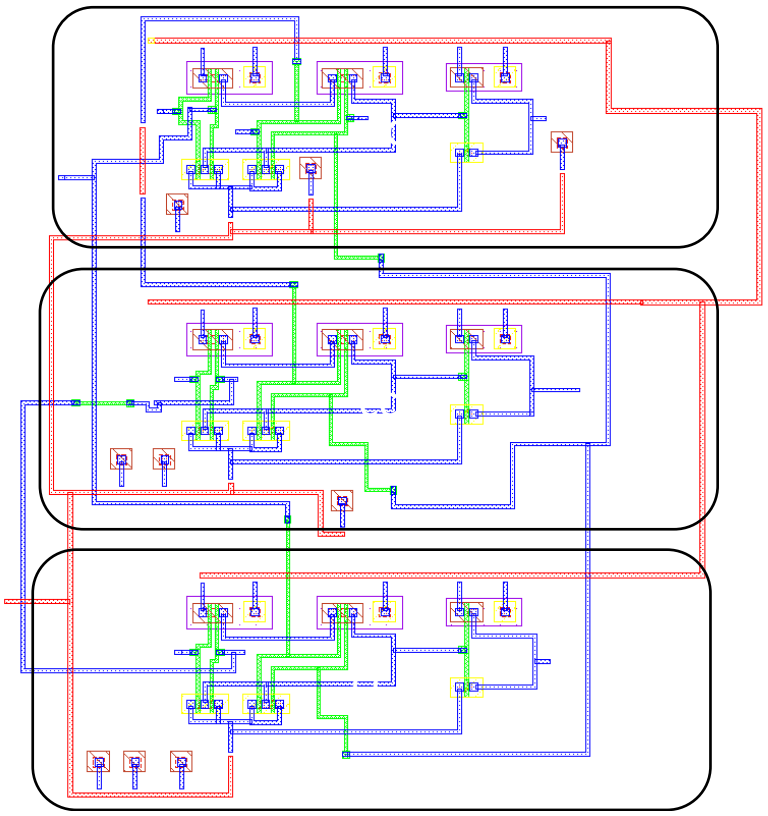


Fig.7. 4 input OR gate layout design using cadence virtuso.

8:3 Encoder Layout Design



A2=Y4+Y5+Y6+Y7

A1=Y2+Y3+Y6+Y7

A0=Y1+Y3+Y5+Y7

Fig.8. 8:3 encoder layout design using cadence virtuoso.

DRC Check

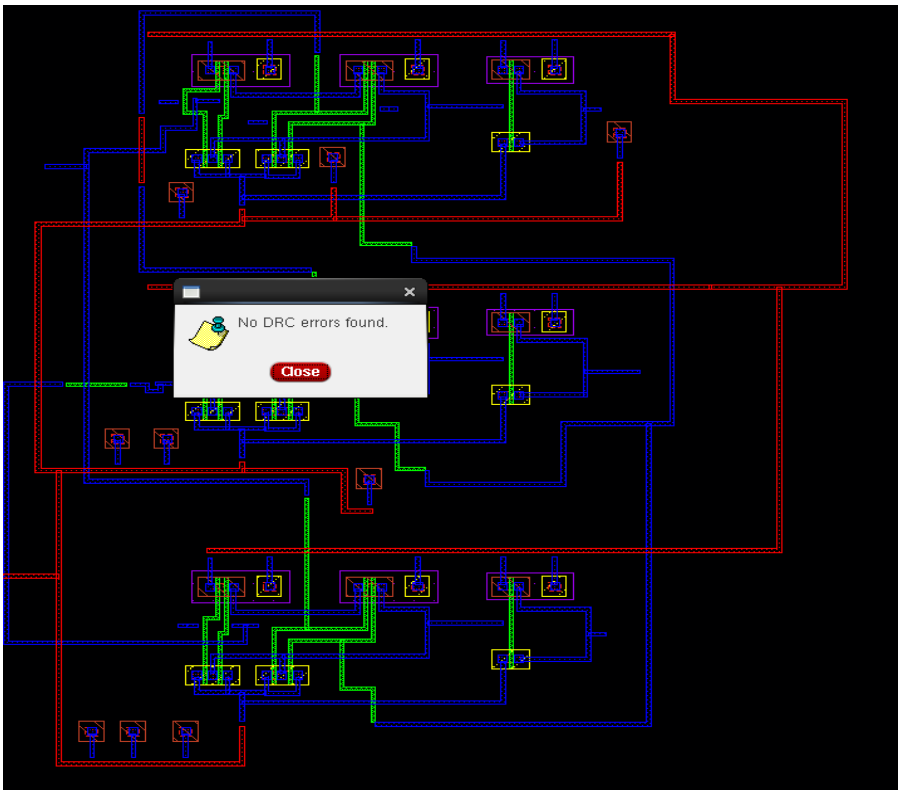


Fig.9. No DRC error found in 8:3 encoder design.

LVS Check

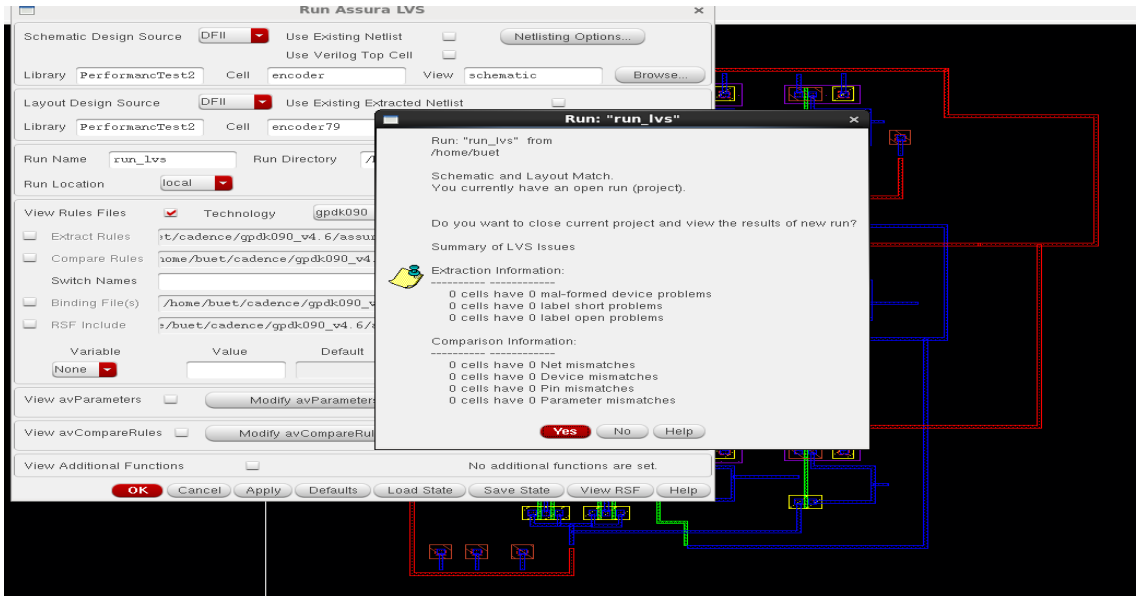


Fig.10. No mismatch found between schematic and layout design.

Discussion

The objective of the experiment was to design Gated 8 to 3 bit encoder design and then create it's symbol. We'll check the DRC and LVS from ASSURA. We've had to maintain the given criterion. However, we've successfully designed the desired circuit by maintaining the criteria. At first there was some DRC error, which we've fixed successfully and finally the LVS tab showed no mismatch between schematic and layout.