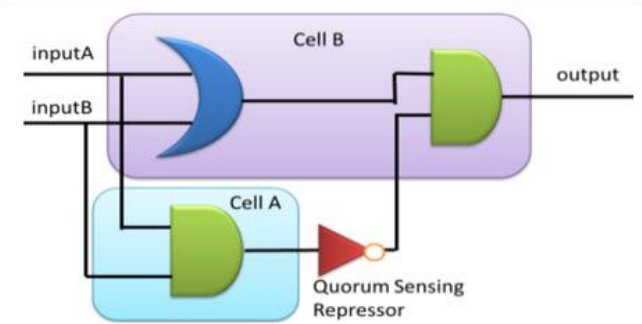
Birlesik Mantık Tasarımı



Suhap SAHIN

Birlesik Mantık Tasarımı (Combinational Logic Design)

ayrık degiskenler:

giris ve cıkıslar

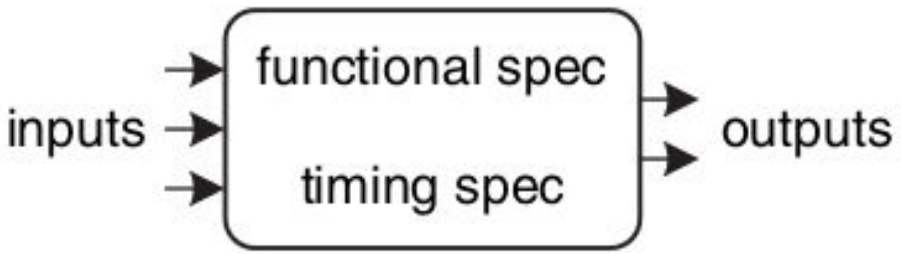
fonksiyonel tanımlamalar:

giris çıkıs arasındaki iliski

zamansal tanımlamalar:

girislerdeki degisiklige cıkısların tepki süresi

Blackbox



Birlesimsel Mantık Tasarımı (Combinational Logic Design)

Element:

Giris, çıkıs ve belirli tanımlamalara sahip devre

Node:

Ayrık degiskenleri ileten bir tel

Element:

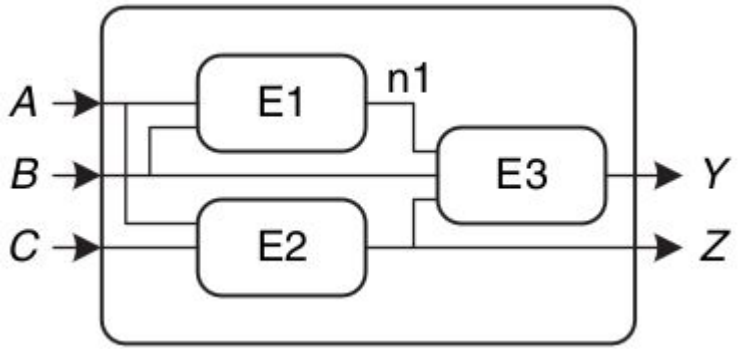
E1, E2, E3

Node:

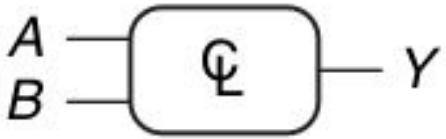
A,B,C (giris)

Y,Z (çıkıs)

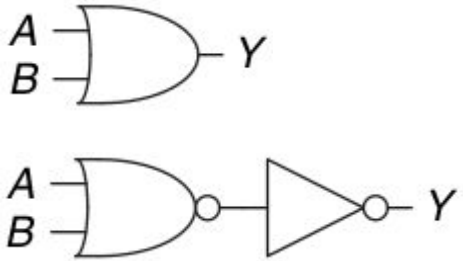
n1 (ara)



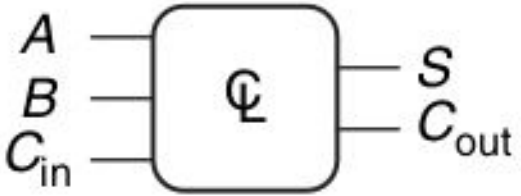
Birlesimsel Mantik Devre (Combinational Logic Circuit)



$$Y = F(A, B) = A + B$$

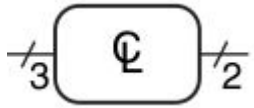


Birlesimsel Mantik Devre (Combinational Logic Circuit)



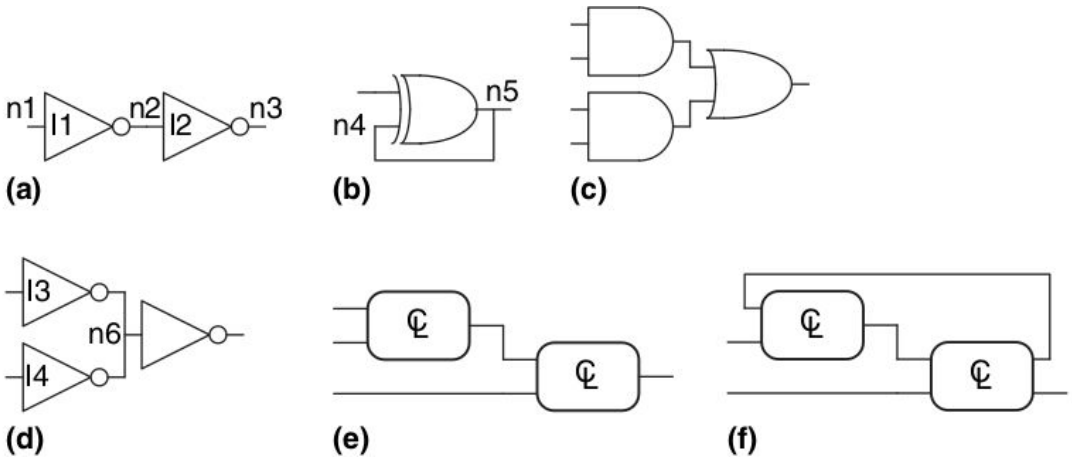
$$S = A \oplus B \oplus C_{in}$$

$$C_{out} = AB + AC_{in} + BC_{in}$$



Birlesimsel Mantık Devre (Combinational Logic Circuit) Özellikleri

- Devrenin herbir elemanı bir birlesimsel mantık devresidir.
- Bir giris, çıkıs ve iç baglantı dügümlerinden olusmustur.
- Devredeki herbir yol, devreki her dügümü bir kez ziyaret eder ve döngüsel yol içermez.



Birlesimsel Mantık Devre (Combinational Logic Circuit) Özellikleri

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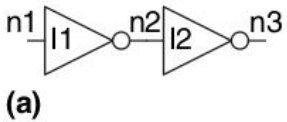
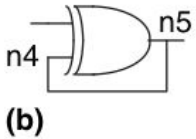


(a)

- I1 ve I2 tersleyiciler: Devrenin herbir elemanı bilesimsel mantık devresidir.
- Devre n1,n2 ve n3 dügümlerine sahiptir.
- Devre döngüsel yol içermiyor
- Devre bilesimsel bir mantık devresidir.

Birlesimsel Mantık Devre (Combinational Logic Circuit) Özellikleri

- Devrenin herbir elemanı bir bilesimsel mantık devresidir.
- Bir giris, çıkıs ve iç baglantı dügümlerinden olusmustur.
- Devredeki herbir yol, devreki her dügümü bir kez ziyaret eder ve döngüsel yol içermez.

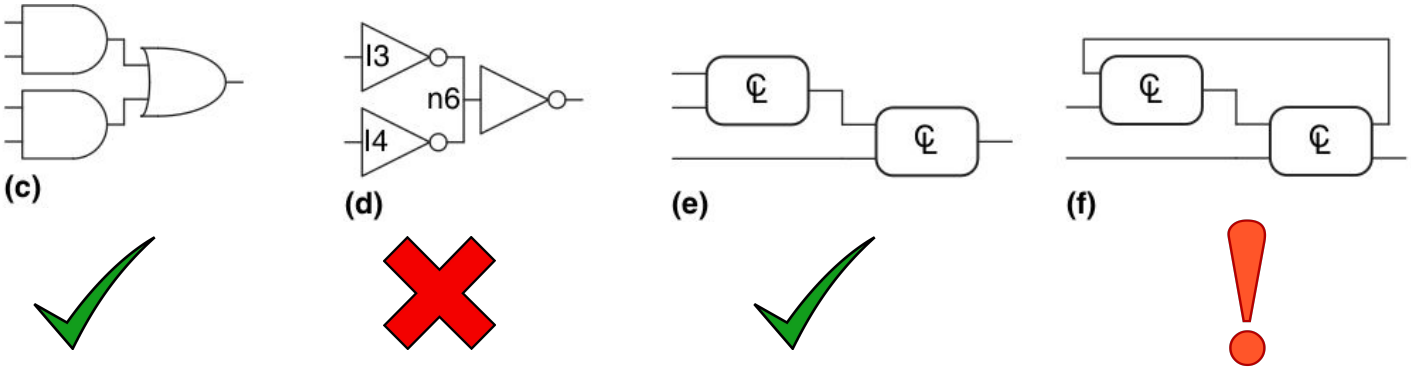


(b)

- Devre döngüsel yol içeriyor
- Devre bilesimsel bir mantık devresi DEGiLDiR.

Birlesimsel Mantık Devre (Combinational Logic Circuit) Özellikleri

- Devrenin herbir elemanı bir bilesimsel mantık devresidir.
- Bir giris, çıkıs ve iç baglantı dügümlerinden olusmustur.
- Devredeki herbir yol, devreki her dügümü bir kez ziyaret eder ve döngüsel yol içermez.



Boolean Denklemleri

A : true form

A' : complementary form

AND: product, implicant

OR: sum

islem Önceligi

NOT

AND

OR

AND Lojik Fonksiyon

Degiskenler: A, B ve C

Minterm: $A\bar{B}\bar{C}$

OR Lojik Fonksiyon

Degiskenler: A, B ve C

Maxterm: $A+\bar{B}+C$

Y = A + BC

Y = A OR (B AND C)

Sum of Product Form & Sigma Notation

A	B	Y	minterm	minterm name
0	0	0	$\bar{A}\ \bar{B}$	m_0
0	1	1	$\bar{A}\ B$	m_1
1	0	0	$A\ \bar{B}$	m_2
1	1	0	$A\ B$	m_3

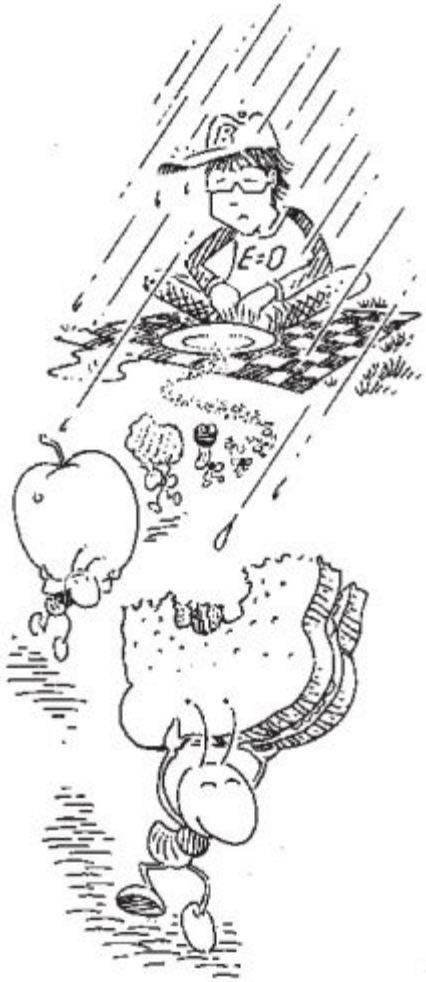
$Y = \bar{A}B$

A	B	Y	minterm	minterm name
0	0	0	$\bar{A}\ \bar{B}$	m_0
0	1	1	$\bar{A}\ B$	m_1
1	0	0	$A\ \bar{B}$	m_2
1	1	1	$A\ B$	m_3

$Y = \bar{A}B + AB$

$$F(A,B) = \Sigma(m_1, m_3)$$

$$F(A,B) = \Sigma(1,3)$$



PiCNiC

- Karınca çok olması
- Yagmurun yagması

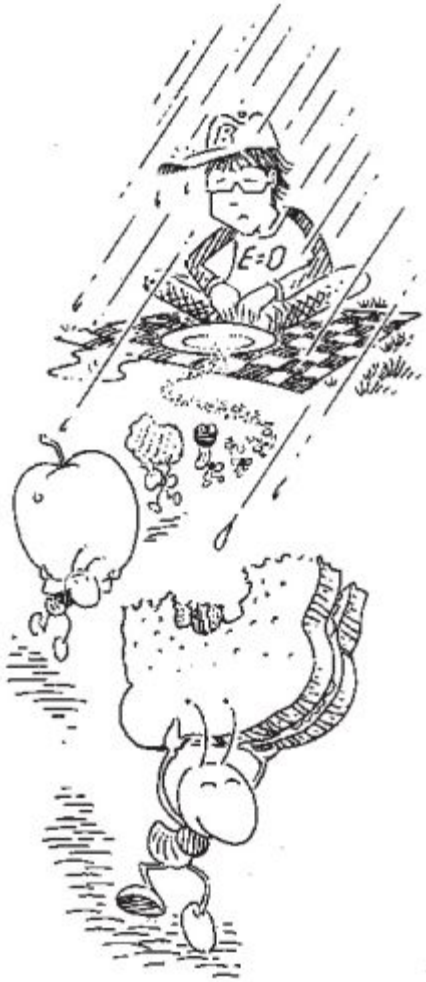
PiCNiC yapmak TRUE

A	R	E
0	0	1
0	1	0
1	0	0
1	1	0

$$E = \overline{A}\,\overline{R}$$

$$E = \Sigma(0)$$

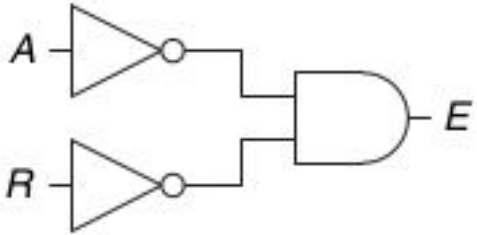
PiCNiC



A	R	E
0	0	1
0	1	0
1	0	0
1	1	0

$$E = \overline{A}\,\overline{R}$$

$$E = \Sigma(0)$$



Sum of Product Form

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

$$Y = \overline{A}\,\overline{B}\,\overline{C} + A\overline{B}\,\overline{C} + A\overline{B}C$$

$$Y = \Sigma(0, 4, 5)$$

Product of Sum Form & Pi Notation

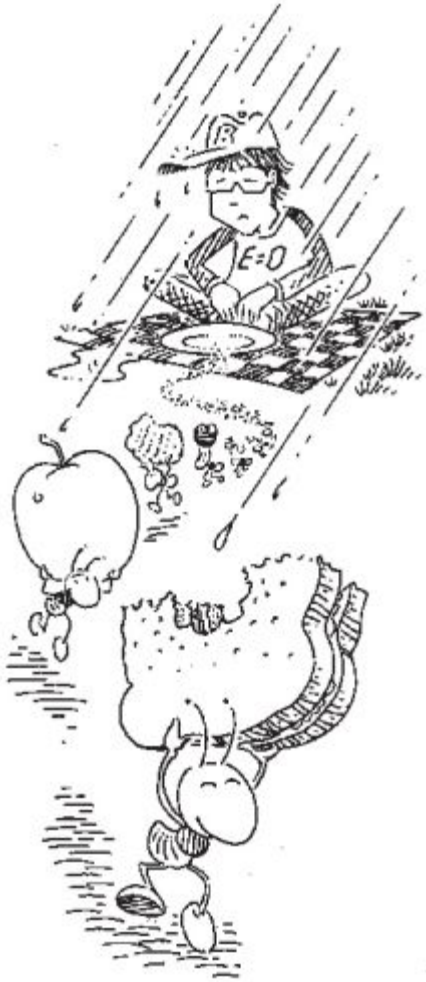
A	B	Y	maxterm	maxterm name
0	0	0	$A + B$	M_0
0	1	1	$A + \overline{B}$	M_1
1	0	0	$\overline{A} + B$	M_2
1	1	1	$\overline{A} + \overline{B}$	M_3

$$Y = (A + B)(\overline{A} + B)$$

$$Y = \Pi(M_0, M_2)$$

$$Y = \Pi(0, 2)$$

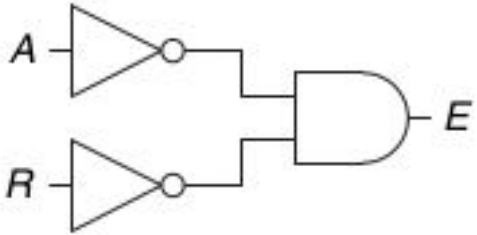
PiCNiC



A	R	E
0	0	1
0	1	0
1	0	0
1	1	0

$$E = (A + \overline{R})(\overline{A} + R)(\overline{A} + \overline{R})$$

$$E = \Pi(1, 2, 3)$$

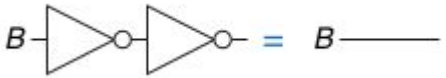


BOOLE CEBRİ

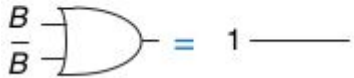
	Axiom		Dual	Name
A1	$B = 0$ if $B \neq 1$	A1′	$B = 1$ if $B \neq 0$	Binary field
A2	$\overline{0} = 1$	A2′	$\overline{1} = 0$	NOT
A3	$0 \bullet 0 = 0$	A3′	$1 + 1 = 1$	AND/OR
A4	$1 \bullet 1 = 1$	A4′	$0 + 0 = 0$	AND/OR
A5	$0 \bullet 1 = 1 \bullet 0 = 0$	A5′	$1 + 0 = 0 + 1 = 1$	AND/OR

Bir Degiskene ait Teoremler

	Theorem		Dual	Name
T1	$B \bullet 1 = B$	T1′	$B + 0 = B$	Identity
T2	$B \bullet 0 = 0$	T2′	$B + 1 = 1$	Null Element
T3	$B \bullet B = B$	T3′	$B + B = B$	Idempotency
T4		T4′	$\overline{\overline{B}} = B$	Involution
T5	$B \bullet \overline{B} = 0$	T5′	$B + \overline{B} = 1$	Complements

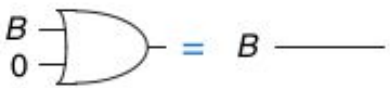


(a)



(b)

(a)



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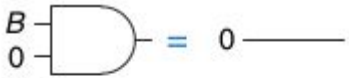
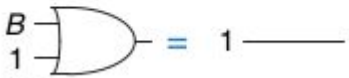


(a)



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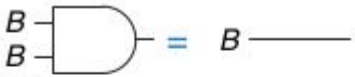


(a)

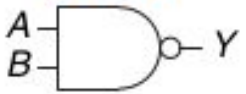
(b)

Birden çok Degiskene ait Teoremler

	Theorem		Dual	Name
T6	$B \bullet C = C \bullet B$	T6′	$B + C = C + B$	Commutativity
T7	$(B \bullet C) \bullet D = B \bullet (C \bullet D)$	T7′	$(B + C) + D = B + (C + D)$	Associativity
T8	$(B \bullet C) + (B \bullet D) = B \bullet (C + D)$	T8′	$(B + C) \bullet (B + D) = B + (C \bullet D)$	Distributivity
T9	$B \bullet (B + C) = B$	T9′	$B + (B \bullet C) = B$	Covering
T10	$(B \bullet C) + (B \bullet \overline{C}) = B$	T10′	$(B + C) \bullet (B + \overline{C}) = B$	Combining
T11	$(B \bullet C) + (\overline{B} \bullet D) + (C \bullet D)$ $= B \bullet C + \overline{B} \bullet D$	T11′	$(B + C) \bullet (\overline{B} + D) \bullet (C + D)$ $= (B + C) \bullet (\overline{B} + D)$	Consensus
T12	$\overline{B_0 \bullet B_1 \bullet B_2 \ldots}$ $= (\overline{B}_0 + \overline{B}_1 + \overline{B}_2 \ldots)$	T12′	$\overline{B_0 + B_1 + B_2 \ldots}$ $= (\overline{B}_0 \bullet \overline{B}_1 \bullet \overline{B}_2 \ldots)$	De Morgan's Theorem

De Morgan Kuralı

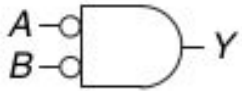
NAND



$$Y = \overline{AB} = \overline{A} + \overline{B}$$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR



$$Y = \overline{A + B} = \overline{A}\,\overline{B}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Örnek

A	B	Y	$\overline{Y}$
0	0	0	1
0	1	0	1
1	0	1	0
1	1	1	0

A	B	Y	$\overline{Y}$	minterm
0	0	0	1	$\overline{A}\,\overline{B}$
0	1	0	1	$\overline{A}\,B$
1	0	1	0	$A\,\overline{B}$
1	1	1	0	$A\,B$

$\overline{Y}$ ye ait sum of product formundan; De Morgan kullanılarak Y product of sum formunu çıkarınız

$$\overline{Y} = \overline{A}\,\overline{B} + \overline{A}B$$

$$\overline{\overline{Y}} = Y = \overline{\overline{A}\,\overline{B} + \overline{A}B} = (\overline{\overline{A}\,\overline{B}})(\overline{\overline{A}B}) = (A+B)(A+\overline{B})$$

Denklem indirgeme

$\overline{A}\,\overline{B}\,\overline{C}+A\overline{B}\,\overline{C}+A\overline{B}C$ Denklemini indirgeyiniz

Step	Equation	Justification
	$\overline{A}\,\overline{B}\,\overline{C}+A\overline{B}\,\overline{C}+A\overline{B}C$	
1	$\overline{B}\,\overline{C}(\overline{A}+A)+A\overline{B}C$	T8: Distributivity
2	$\overline{B}\,\overline{C}(1)+A\overline{B}C$	T5: Complements
3	$\overline{B}\,\overline{C}+A\overline{B}C$	T1: Identity

Denklem indirgeme

$\overline{A}\,\overline{B}\,\overline{C}+A\overline{B}\,\overline{C}+A\overline{B}C$ Denklemini indirgeyiniz

Step	Equation	Justification
	$\overline{A}\,\overline{B}\,\overline{C}+A\overline{B}\,\overline{C}+A\overline{B}C$	
1	$\overline{B}\,\overline{C}(\overline{A}+A)+A\overline{B}C$	T8: Distributivity
2	$\overline{B}\,\overline{C}(1)+A\overline{B}C$	T5: Complements
3	$\overline{B}\,\overline{C}+A\overline{B}C$	T1: Identity

$\overline{B}\,\overline{C}$ $A\overline{B}$

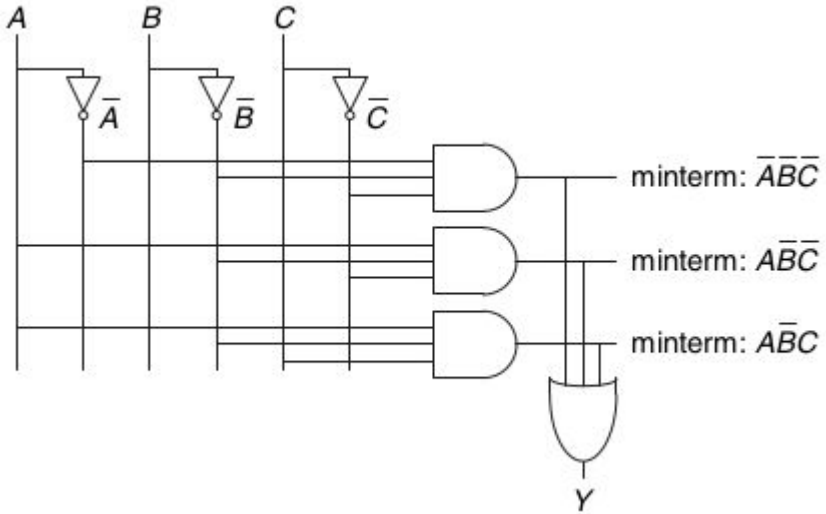
Denklem indirgeme

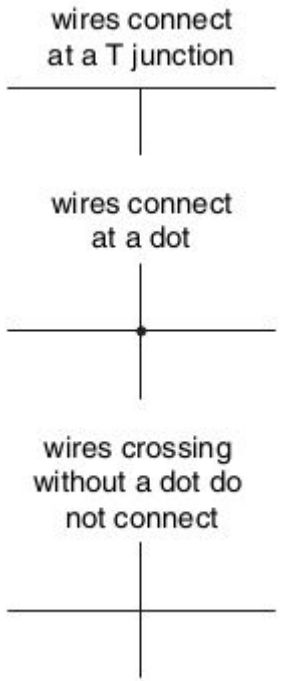
$\overline{A}\,\overline{B}\,\overline{C}+A\overline{B}\,\overline{C}+A\overline{B}C$ Denklemini indirgeyiniz $B=B+B+B+B\ldots.$

Step	Equation	Justification
	$\overline{A}\,\overline{B}\,\overline{C}+A\overline{B}\,\overline{C}+A\overline{B}C$	
1	$\overline{A}\,\overline{B}\,\overline{C}+A\overline{B}\,\overline{C}+A\overline{B}\,\overline{C}+A\overline{B}C$	T3: Idempotency
2	$\overline{B}\,\overline{C}(\overline{A}+A)+A\overline{B}(\overline{C}+C)$	T8: Distributivity
3	$\overline{B}\,\overline{C}(1)+A\overline{B}(1)$	T5: Complements
4	$\overline{B}\,\overline{C}+A\overline{B}$	T1: Identity

Lojik ifadelerden Lojik Kapılara (sematik)

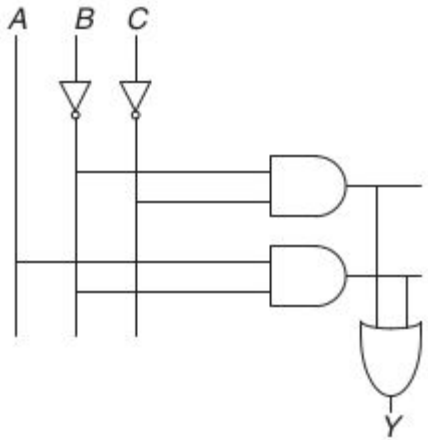
$$Y = \overline{A}\,\overline{B}\,\overline{C} + A\overline{B}\,\overline{C} + A\overline{B}\,C$$

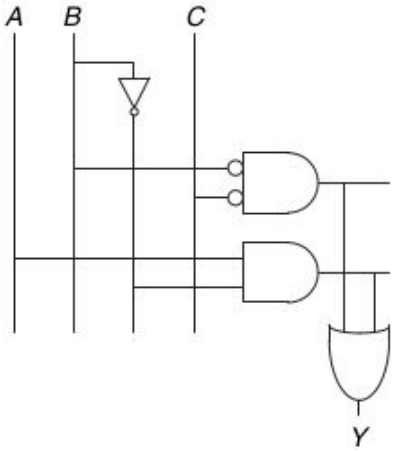




Lojik ifadelerden Lojik Kapılara (sematik)

$$Y = \overline{B}\,\overline{C} + A\overline{B}$$





Konferans Salonu Kullanım Problemi

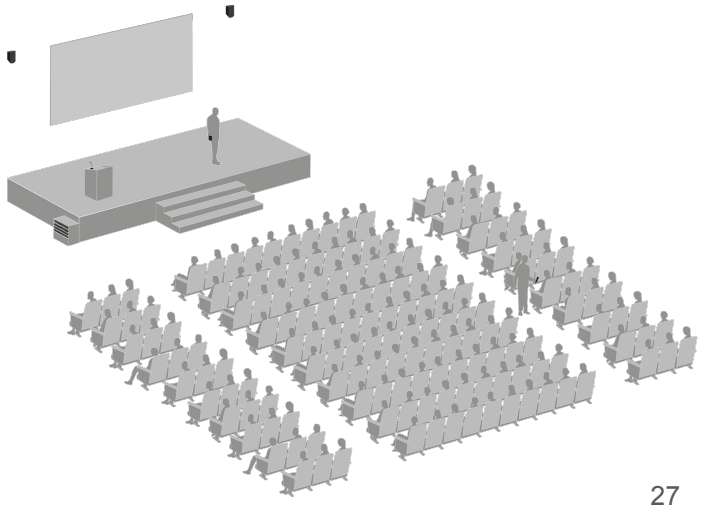
Konferans Salonunu Kullananlar:

0: Yurt Müdürü
1: Ögretim Üyesi
2: Bölüm Baskanı
3: Dekan

Çakısma meydana gelmemesi için gerekli islemleri gereçeklestiren lojik devreyi ciziniz.
Cizilen devreye ait dogruluk tablosunu ve Boolean denklemlerini yazınız.

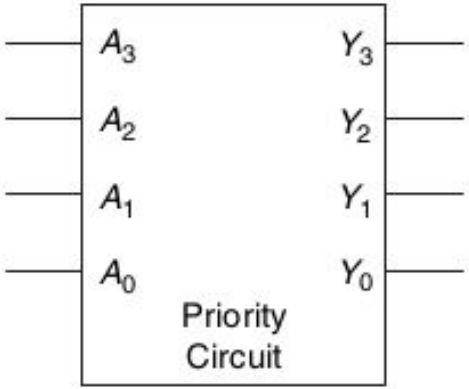
Sistem girisleri: A0, A1, A2, A3
Sistem çıkısları: Y0, Y1, Y2, Y3
Kullanıcı önceligi:

A0⟶ Y0: Yurt Müdürü
A1 ⟶ Y1 : Ögretim Üyesi
A2⟶ Y2: Bölüm Baskanı
A3-->Y3: Dekan



Dört Girisli Öncelik Devresi

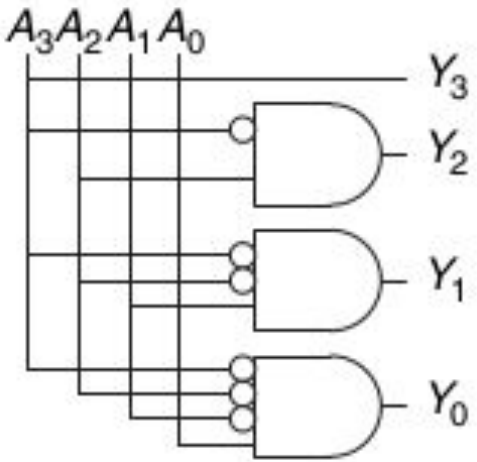
A0→ Y0: Yurt Müdürü
A1 → Y1 : Ögretim Üyesi
A2→ Y2: Bölüm Baskanı
A3-->Y3: Dekan



A_3	A_2	A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	0
1	0	1	0	1	0	0	0
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	0
1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	0

Dört Girisli Öncelik Devresi

A0→ Y0: Yurt Müdürü
A1 → Y1 : Ögretim Üyesi
A2→ Y2: Bölüm Baskanı
A3-->Y3: Dekan



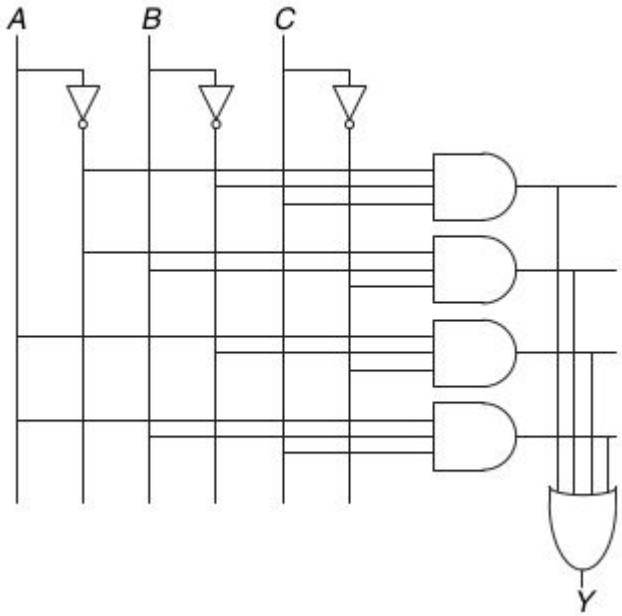
A_3	A_2	A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	X	0	0	1	0
0	1	X	X	0	1	0	0
1	X	X	X	1	0	0	0

ÇOK SEVİYELİ BİRLEŞİK MANTIK

Sum of products formunda girisler AND lojik sevyelerinden ve çıkıslar OR lojik sevyelerinden olustugu için iki sevyeli lojik seklinde adlandırılır.

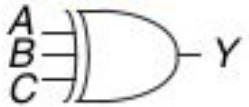
$$Y = \overline{A}\,\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\,\overline{C} + ABC$$

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



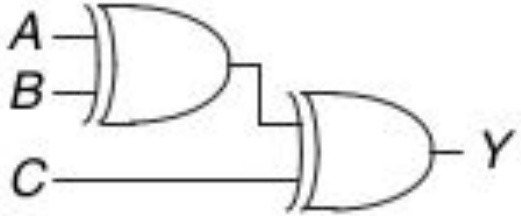
ÇOK SEVİYELİ BİRLEŞİK MANTIK

XOR3

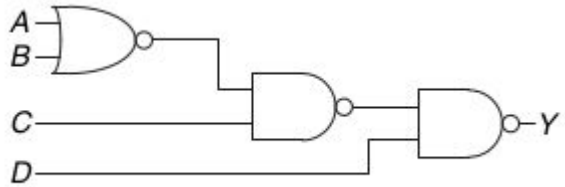


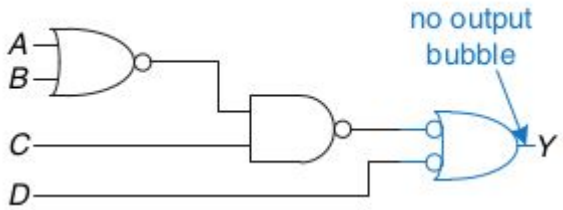
$$Y = A \oplus B \oplus C$$

$$A \oplus B \oplus C = (A \oplus B) \oplus C$$

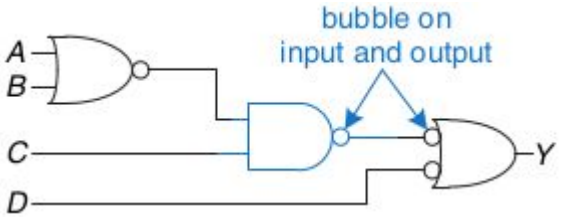


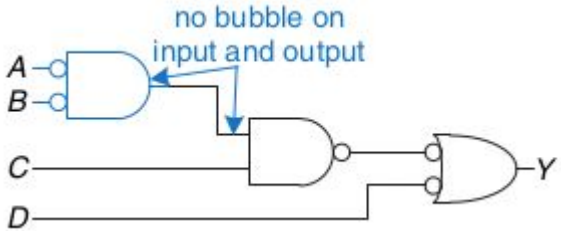
Tersleyici itme



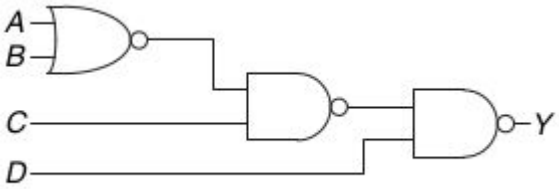


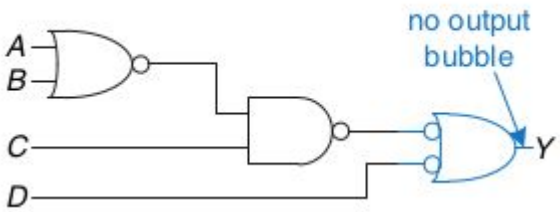
$$Y = \overline{A}\,\overline{B}C + \overline{D}$$

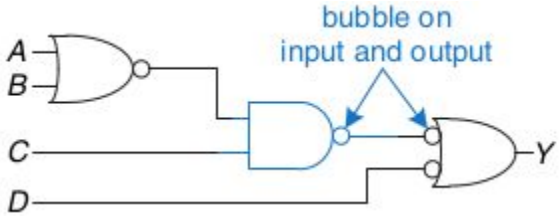


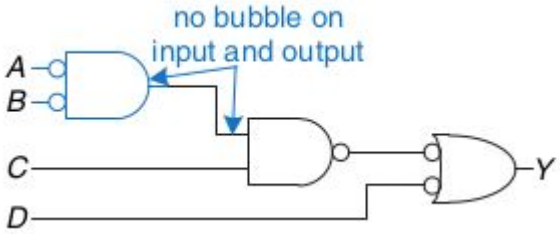


Tersleyici itme

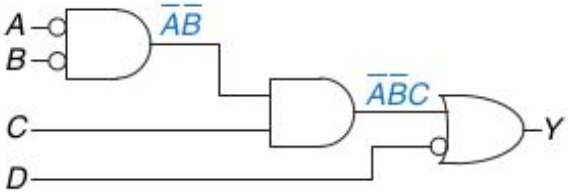






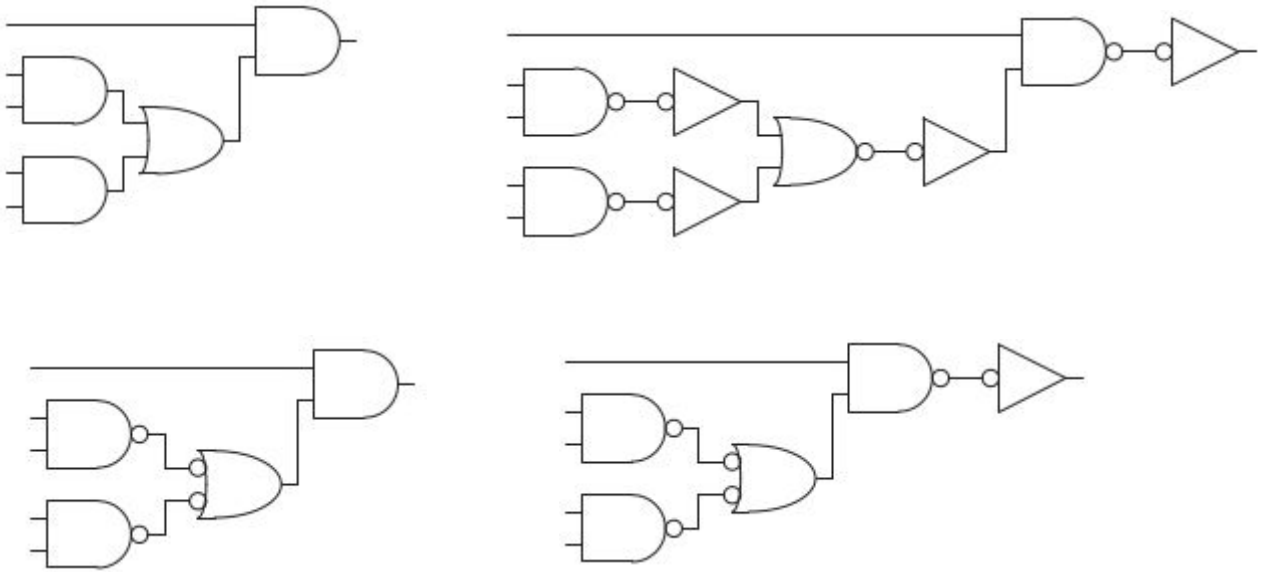


$$Y = \overline{A}\,\overline{B}C + \overline{D}$$



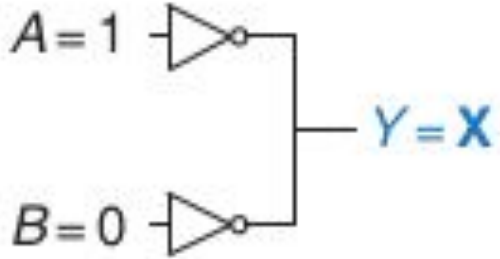
$$Y = \overline{A}\,\overline{B}C + \overline{D}$$

Tersleyici itme CMOS Lojik



illegal X Degeri

X⟶ HIGH/LOW degeri
(forbidden zone)



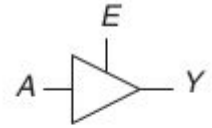
X degeri ile sürülen devreler, devre elemanlarının özelliklerine göre bazen LOW bazende HIGH degeri olarak islem yapabilirler.

X degeri, simülatorlerde baslangıç degeri ile sürülmemis devre elemanlarını sürmek için kullanılır.

X degeri dogruluk tablolarında "don't care" durumları için kullanılır

Kayan Z Degeri

Z⟶ HIGH/LOW DEGiL degeri
floating, high impedance, high Z



E	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1

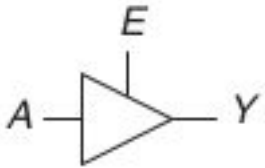
Z degeri ile sürülen devreler, devre elemanlarının özelliklerine göre bazen LOW bazende HIGH degeri olarak islem yapabilirler.

Lojik islemler sürerken görülen Z degeri hata anlamına gelmez.

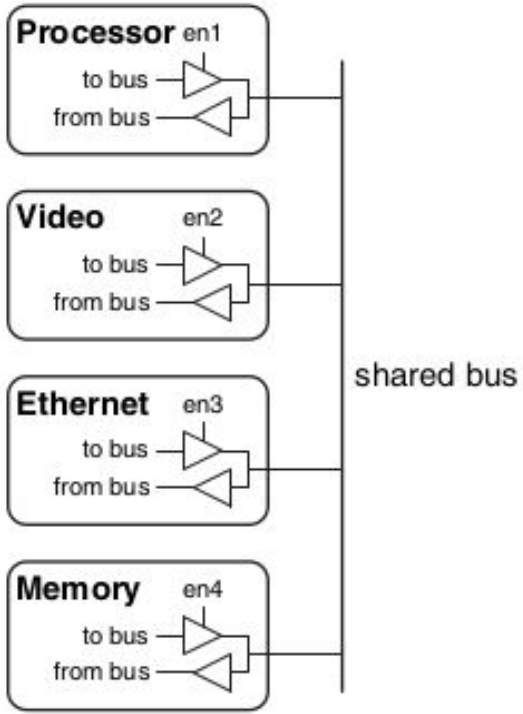
Devre girisine voltaj baglamamak veya baglanmamıs bir girisin 0 degerine sahip oldugunu varsaymak Z degerine sebep olur.

Devreye dokunmak, statik elektrik sebebiyle devrenin Z ile sürülmesine yeterli olabilir.

Ortak Yol Kullanımı

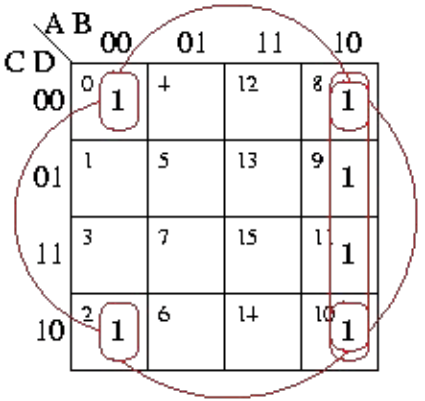


E	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1

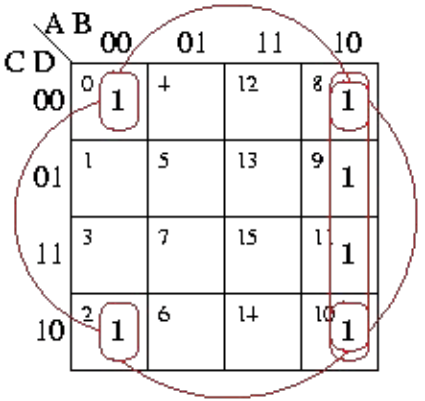


Harita Yöntemi ile Sadelestirme(Karnaugh Map Minimization)

- Görsel bir sadelestirme yöntemidir.
  - Yakınlık özelligini kullanır.
  - En küçük deyimi bulur.
  - Kullanımı kolay ve hızlıdır.
- Problemler:
  - Belirli sayıda degiskene uygulanabilir. (4 ~ 8)
  - Dogruluk tablosundan haritaya geçirirken yanlıslar yapılabilir.
  - Haritadaki hücreler dogru bir sekilde gruplanmayabilir.
  - Son deyim yanlıs okunabilir.



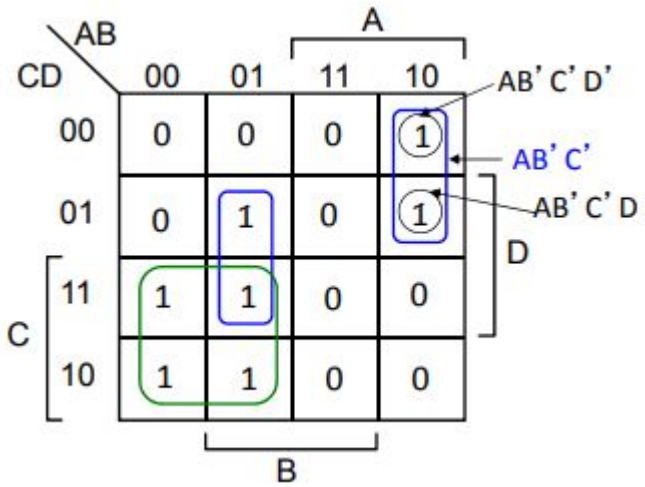
Harita Yöntemi ile Sadelestirme(Karnaugh Map Minimization)



- Harita belli sayıda hücreden olusan bir 2 boyutlu dizgedir.
  - Her kare dogruluk tablosundaki bir satıra karsılık gelir
  - ilgili satır için Y çıktısının degerini içerir.
- Hücrelerin yerlesimi
  - Bitisik terimlerde sadece 1 degisken degeri farklıdır. örn. m6 (110) and m7 (111)

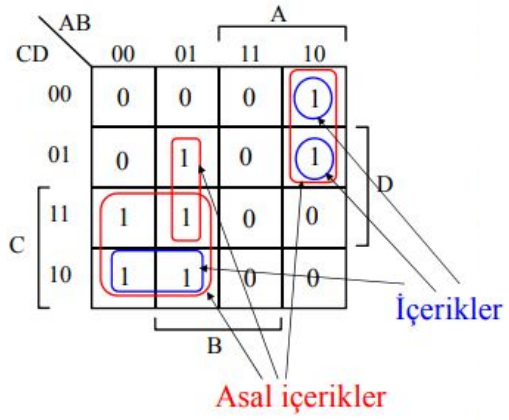
Gruplama - Bitisiklik ilkesinin uygulanması

- iki hücre aynı degere sahip (1) ve birbirlerine komsu ise, deyimler bitisiktir.
- Gruplar üst üste gelebilir
- Grup sayısı 2 nin kuvveti. (1, 2, 4, 8)
- 1 ler ve 0 lar gruplandırılabilir.

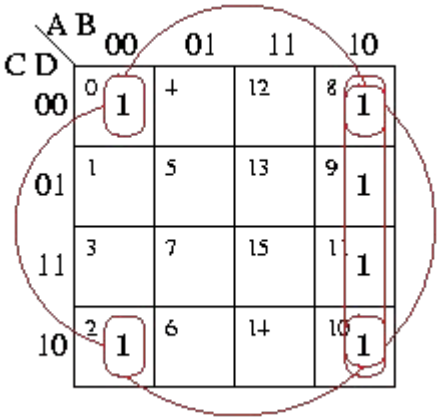


içerikler(Implicants) ve Asal içerikler (Prime Implicants)

- Daha büyük bir grubun parçası olan tek bir hücre ya da bir grup hücreye içerik denir.
- En büyük gruba asal içerik denir.
- Tek bir hücre de asal içerik olabilir.
- Tüm degerleri (1 leri) içeren içeriklerin herhangi istenilen islevi gösterir.
- Tüm degerleri (1 leri) içeren asal içeriklerin en küçük kümesi, islevin en küçük deyim ile gösterimini verir.
    - Birden fazla en küçük küme olabilir.



K Haritaları Kuralları



Tüm 1 leri kapsayacak en az çemberi kullanılmalıdır.

Çemberin içindeki tüm kareler 1 içermelidir.

Gruplamalarda seçilen kutu sayısı 1,2,4,8,16,...olmalıdır.

Herbir çember olabildigince büyük olmalıdır.

Karsılıklı köse ve kenarlardaki kareler birbirlerine komsu kare sayılırlar.

Harita içindeki 1 degeri en az çemberi saglamak için birden fazla çember içinde olabilir.

Bitisik terimlerde sadece 1 degisken degeri farklıdır. örn. m6 (110) and m7 (111)

Gray Kod

GEMi kelimesinin iNEK kelimesine dönüsümü;
Kural her bir adımda sadece bir harf degisebilir.

GEMi,
iEMi,
iEMK,
iNMK,
iNEK

ABCD	
0000	
0001	
0011	
0010	
0110	
0111	
0101	
0100	
1100	
1101	
1111	
1110	
1010	
1011	
1001	
1000	

Dogruluk Çizelgesi ve Bitisiklik (adjacency)

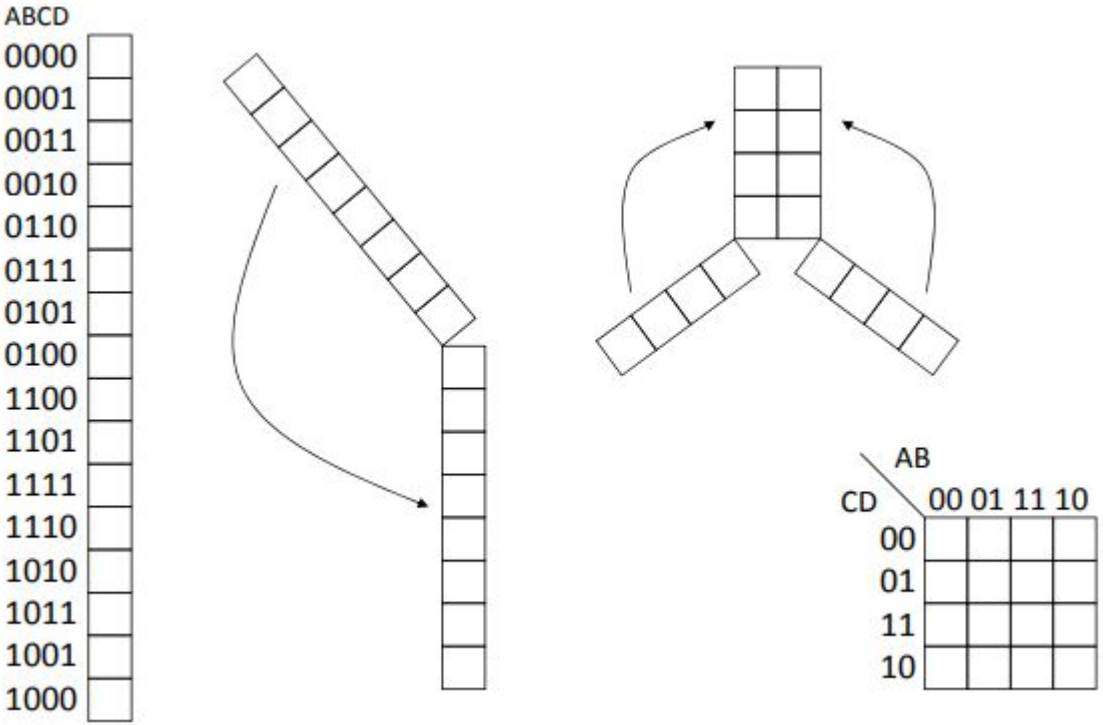
Standart dogruluk çizelgesi

A	B	C	D	minterm
0	0	0	0	m0
0	0	0	1	m1
0	0	1	0	m2
0	0	1	1	m3
0	1	0	0	m4
0	1	0	1	m5
0	1	1	0	m6
0	1	1	1	m7
1	0	0	0	m8
1	0	0	1	m9
1	0	1	0	m10
1	0	1	1	m11
1	1	0	0	m12
1	1	0	1	m13
1	1	1	0	m14
1	1	1	1	m15

Gray kodları

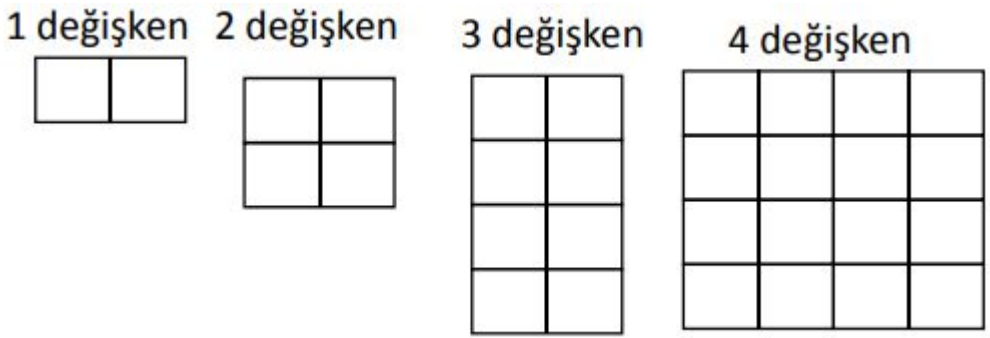
A	B	C	D	minterm
0	0	0	0	m0
0	0	0	1	m1
0	0	1	1	m3
0	0	1	0	m2
0	1	1	0	m6
0	1	1	1	m7
0	1	0	1	m5
0	1	0	0	m4
1	1	0	0	m12
1	1	0	1	m13
1	1	1	1	m15
1	1	1	0	m14
1	0	1	0	m10
1	0	1	1	m11
1	0	0	1	m9
1	0	0	0	m8

Gray Kodlarından Haritaya

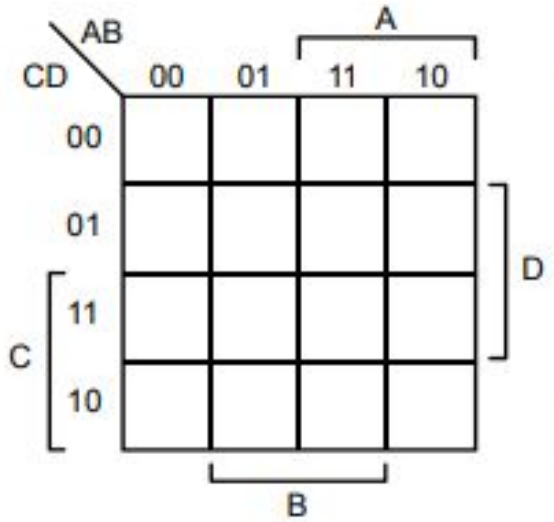


Harita (K-Maps)

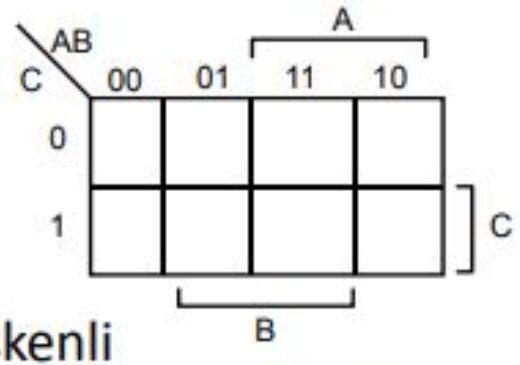
1 degiskenli harita $2^1 = 2$
2 degiskenli harita $2^2 = 4$
3 degiskenli harita $2^3 = 8$
4 degiskenli harita $2^4 = 16$
hücreye sahiptir



Harita (K-Maps)



4 değişkenli



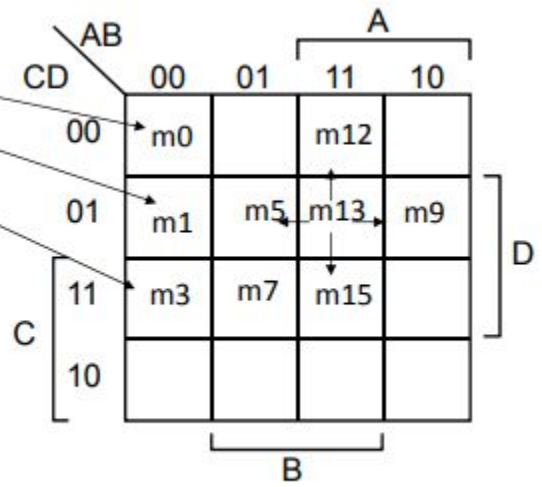
3 değişkenli

En üst ve en alttaki hücreler, en sağ ve en sol hücreler de bitişiktir.

Dogruluk Tablosundan Haritaya

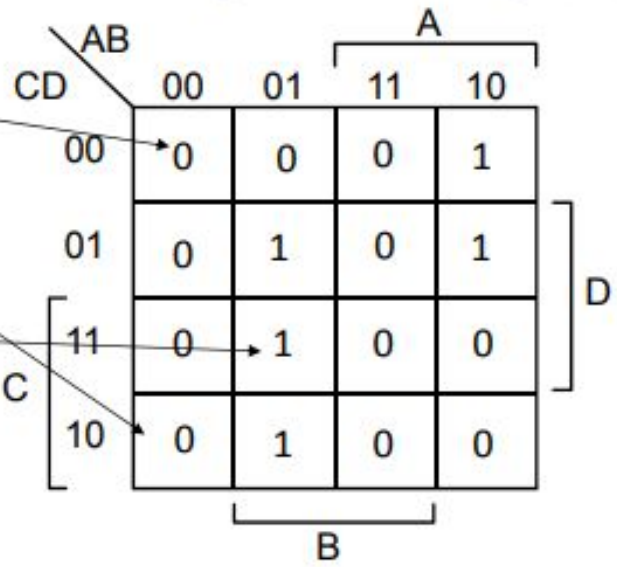
Dogruluk tablosundaki satırların sayısı ile haritanın hücrelerinin sayısı aynı olmalıdır.!

A	B	C	D	F
0	0	0	0	x
0	0	0	1	x
0	0	1	0	x
0	0	1	1	x
0	1	0	0	x
0	1	0	1	x
0	1	1	0	x
0	1	1	1	x
1	0	0	0	x
1	0	0	1	x
1	0	1	0	x
1	0	1	1	x
1	1	0	0	x
1	1	0	1	x
1	1	1	0	x
1	1	1	1	x



Harita ile Sadelestirme

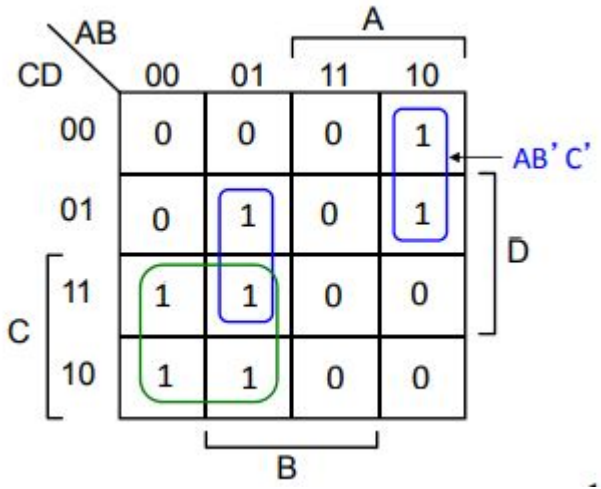
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0



10 ve 11 sütunlarının yerine dikkat!

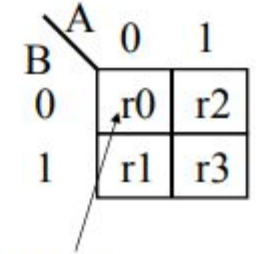
Grupların okunması

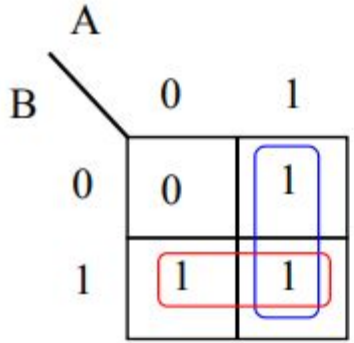
	1leri gruplama	0ları gruplama
Değişken değişiyor	*Dahil etme*	*Dahil etme*
Değişken sabit 0	tümleri	kendisi
Değişken sabit 1	kendisi	tümleri



2-Degiskenli Harita

Satır	A	B	F(A,B)
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	1

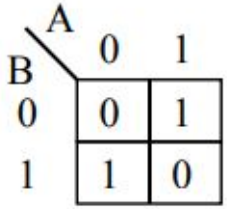




$F(A,B) = A + B$

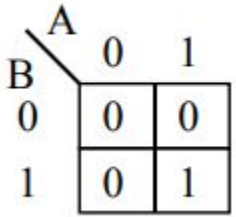
2-Degiskenli Harita

Satır	A	B	F1(A,B)
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	0



$F1(A,B) = A'B + AB'$

Satır	A	B	F2(A,B)
0	0	0	0
1	0	1	0
2	1	0	0
3	1	1	1



$F2(A,B) = AB$

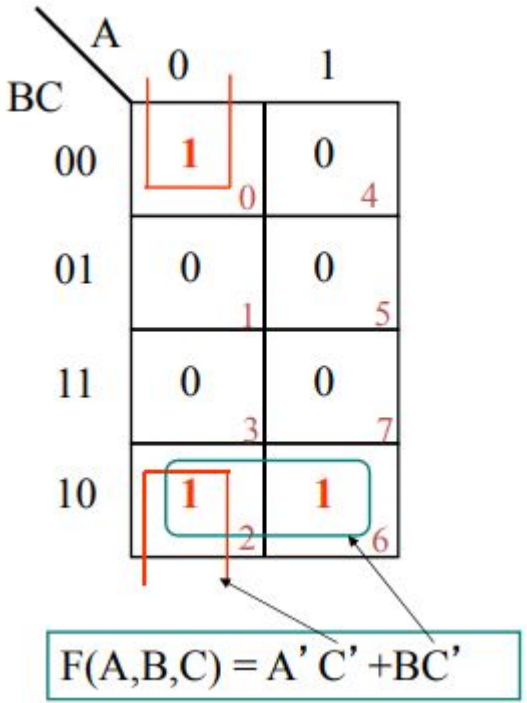
3 Degiskenli Harita

Satır	A B C	F(A,B,C)
0	0 0 0	1
1	0 0 1	0
2	0 1 0	1
3	0 1 1	0
4	1 0 0	0
5	1 0 1	0
6	1 1 0	1
7	1 1 1	0

$F(A,B,C) = \Sigma m(0,2,6)$

$F'(A,B,C) = \Sigma m(1,3,4,5,7)$

$F(A,B,C) = \pi M(1,3,4,5,7)$



K Haritaları

Sum of Product

$$Y = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C = \overline{A}\,\overline{B}(\overline{C} + C) = \overline{A}\,\overline{B}$$

A	B	C	Y
0	0	0	**1**
0	0	1	**1**
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Y \ AB / C	00	01	11	10
0	$\overline{A}\,\overline{B}\,\overline{C}$	$\overline{A}B\overline{C}$	$A\overline{B}\overline{C}$	$AB\overline{C}$
1	$\overline{A}\,\overline{B}C$	$\overline{A}BC$	ABC	$A\overline{B}C$

$$\overline{A}\,\overline{B}$$

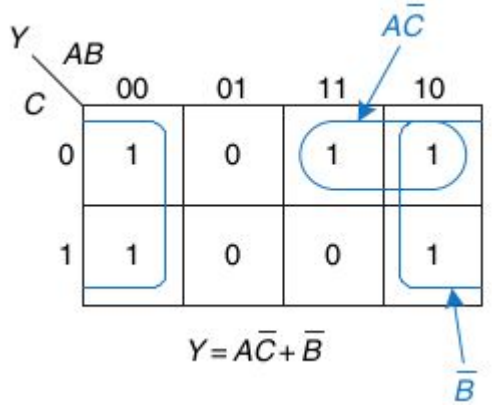
Y \ AB / C	00	01	11	10
0	1	0	0	0
1	1	0	0	0

Y \ AB / C	00	01	11	10
0	1	0	0	0
1	1	0	0	0

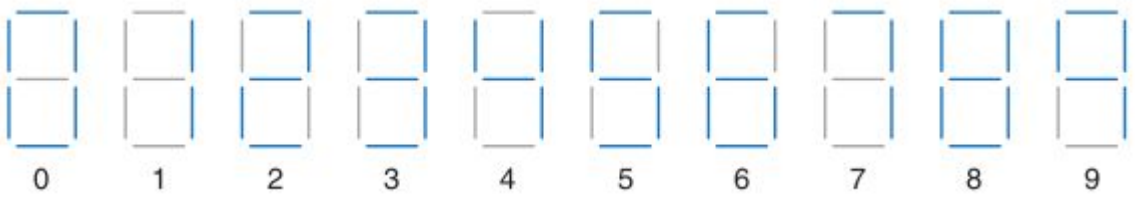
Örnek: K Haritaları

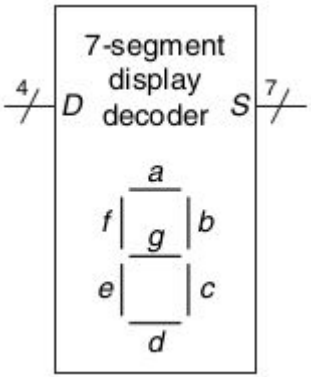
$Y = F(A, B, C)$

Y \ AB	00	01	11	10
C = 0	1	0	1	1
C = 1	1	0	0	1



Yedi Parçalı Display Decoder

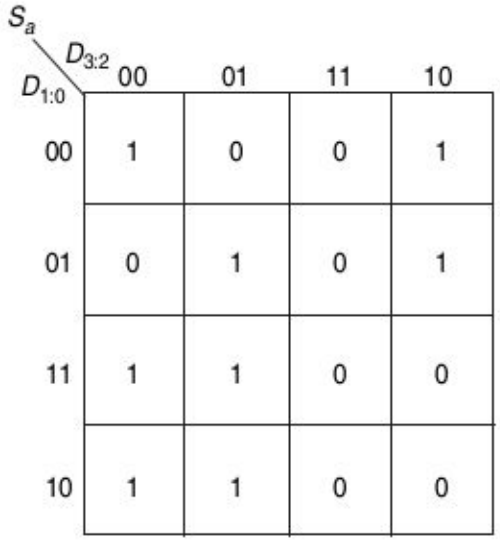


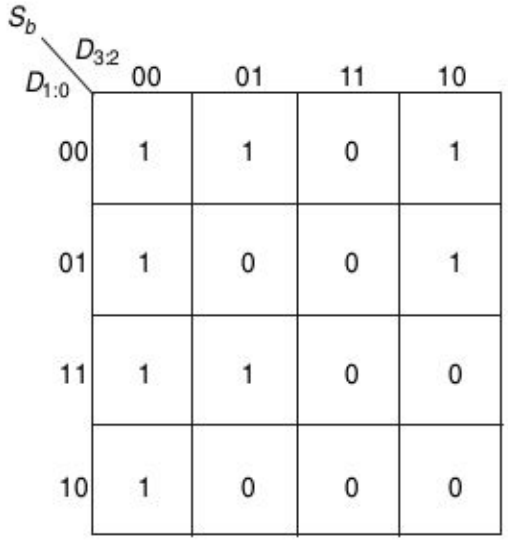


$D_{3:0}$	S_a	S_b	S_c	S_d	S_e	S_f	S_g
0000	1	1	1	1	1	1	0
0001	0	1	1	0	0	0	0
0010	1	1	0	1	1	0	1
0011	1	1	1	1	0	0	1
0100	0	1	1	0	0	1	1
0101	1	0	1	1	0	1	1
0110	1	0	1	1	1	1	1
0111	1	1	1	0	0	0	0
1000	1	1	1	1	1	1	1
1001	1	1	1	0	0	1	1
others	0	0	0	0	0	0	0

Sa ve Sb için K Haritası

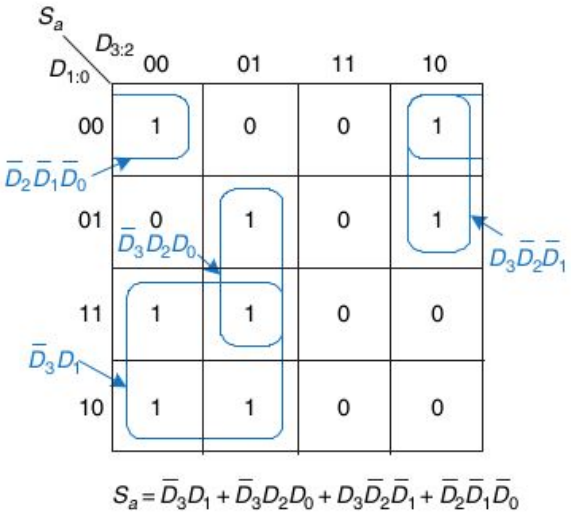
$D_{3:0}$	S_a	S_b	S_c	S_d	S_e	S_f	S_g
0000	1	1	1	1	1	1	0
0001	0	1	1	0	0	0	0
0010	1	1	0	1	1	0	1
0011	1	1	1	1	0	0	1
0100	0	1	1	0	0	1	1
0101	1	0	1	1	0	1	1
0110	1	0	1	1	1	1	1
0111	1	1	1	0	0	0	0
1000	1	1	1	1	1	1	1
1001	1	1	1	0	0	1	1
others	0	0	0	0	0	0	0

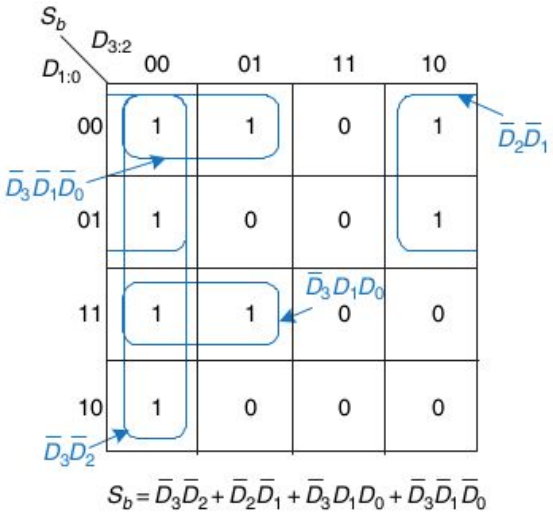




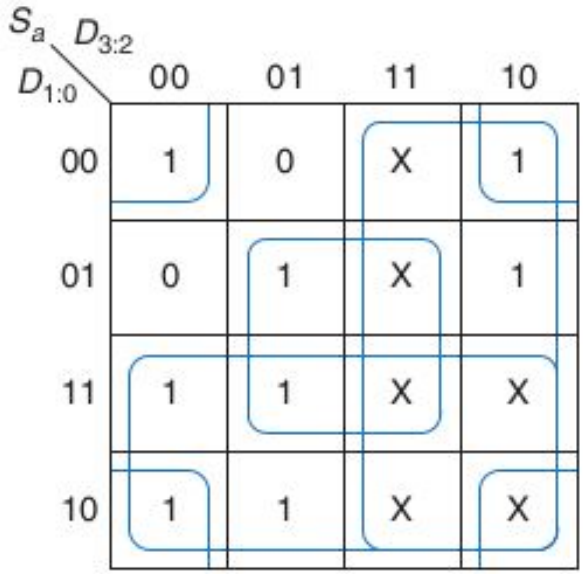
Sa ve Sb için K Haritası

$D_{3:0}$	S_a	S_b	S_c	S_d	S_e	S_f	S_g
0000	1	1	1	1	1	1	0
0001	0	1	1	0	0	0	0
0010	1	1	0	1	1	0	1
0011	1	1	1	1	0	0	1
0100	0	1	1	0	0	1	1
0101	1	0	1	1	0	1	1
0110	1	0	1	1	1	1	1
0111	1	1	1	0	0	0	0
1000	1	1	1	1	1	1	1
1001	1	1	1	0	0	1	1
others	0	0	0	0	0	0	0

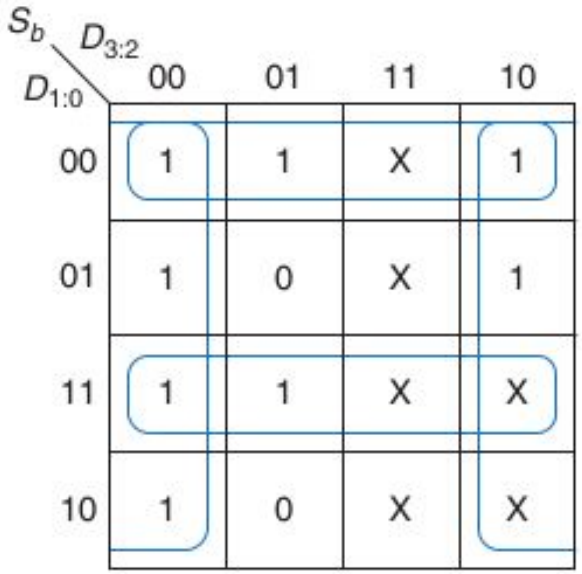




Önemsenmeyen Durumlar



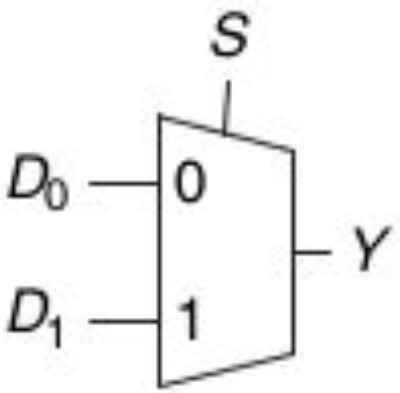
$$S_a = D_3 + D_2 D_0 + \bar{D}_2 \bar{D}_0 + D_1$$



$$S_b = \bar{D}_2 + D_1 D_0 + \bar{D}_1 \bar{D}_0$$

Birlesik Lojik Blokları - Multiplexer (Çoklayıcılar)

2:1 MUX

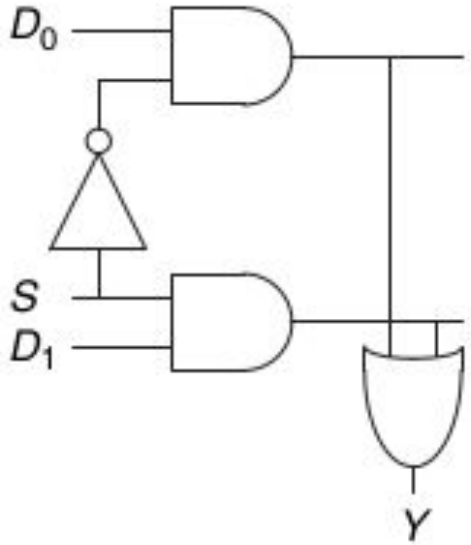


S	D_1	D_0	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Birlesik Lojik Blokları - Multiplexer (Çoklayıcılar)

Y / S \ $D_{1:0}$	00	01	11	10
0	0	1	1	0
1	0	0	1	1

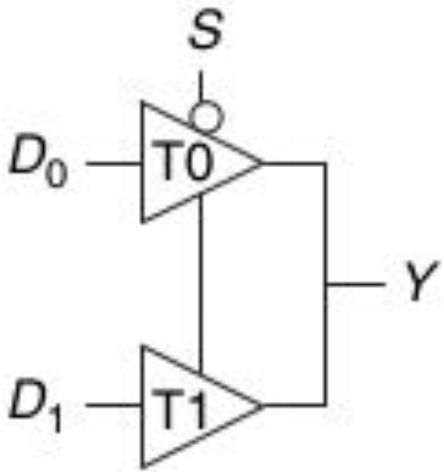
$$Y = D_0\bar{S} + D_1S$$



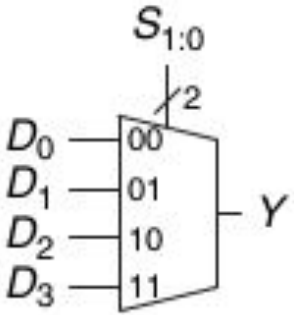
Birlesik Lojik Blokları - Multiplexer (Çoklayıcılar)

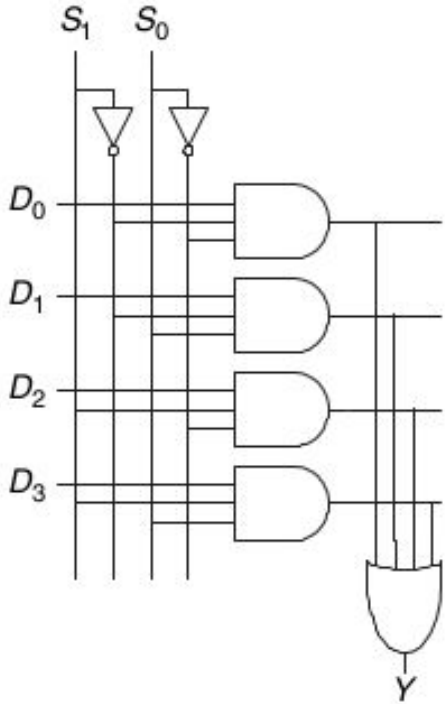
Y / S \ $D_{1:0}$	00	01	11	10
0	0	1	1	0
1	0	0	1	1

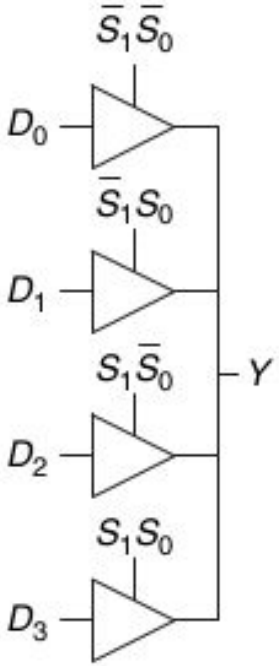
$$Y = D_0\bar{S} + D_1 S$$

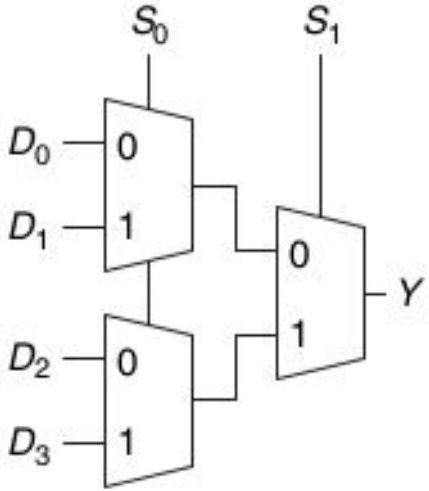


Birlesik Lojik Blokları - Multiplexer (Çoklayıcılar)





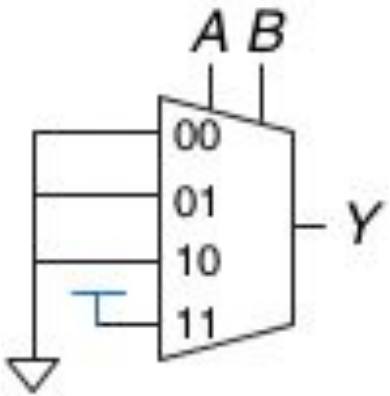




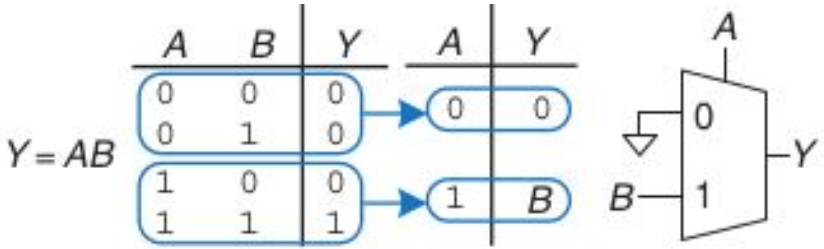
Multiplexer Lojik (Çoklayıcılar)

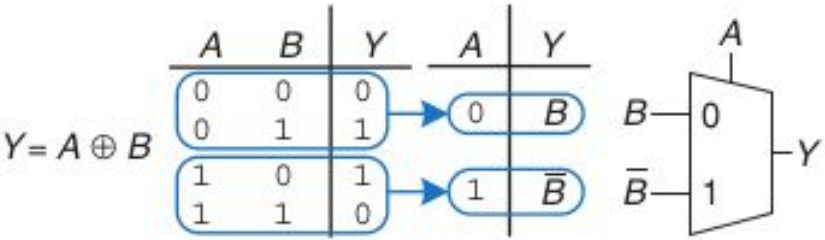
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

$Y = AB$



Multiplexer Lojik (Çoklayıcılar)



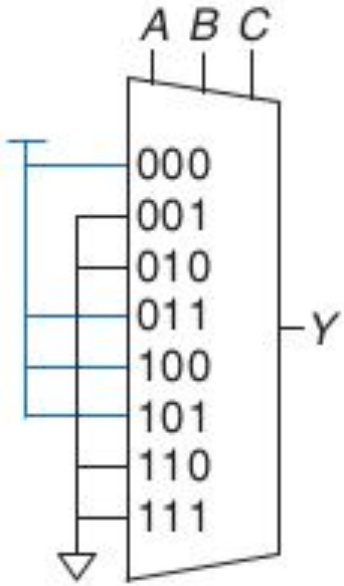


Multiplexer Lojik Örnek-1

Ayse dönem ödevini bitirmek için asagıdaki fonksiyonu gerçeklestirmek istiyor. Ancak laboratuvarda sadece 8:1 multiplexer vardır.

$$Y = A\overline{B} + \overline{B}\,\overline{C} + \overline{A}BC$$

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0



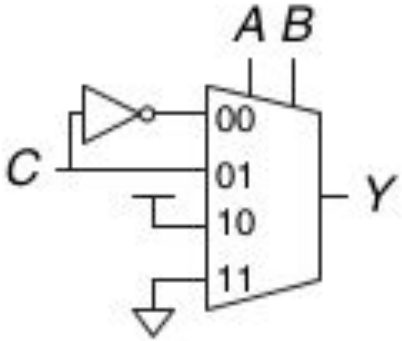
Multiplexer Lojik Örnek -2

Ayse ödev sunumundan önce devresine yanlıslıkla 20V vererek yaktı. Panikle arkadasından 4:1 mux ve bir tersleyici aldı ve devreyi gerçekleme istiyor.

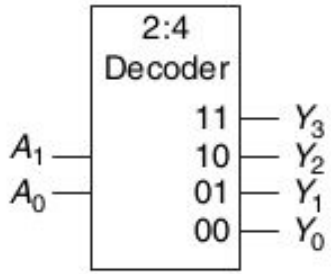
$$Y = A\overline{B} + \overline{B}\,\overline{C} + \overline{A}BC$$

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

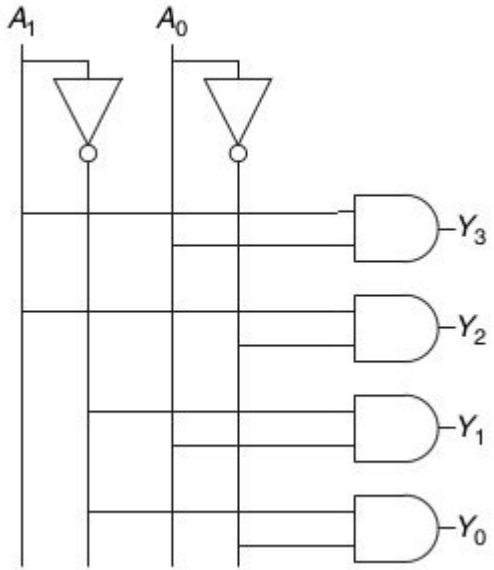
A	B	Y
0	0	$\overline{C}$
0	1	C
1	0	1
1	1	0



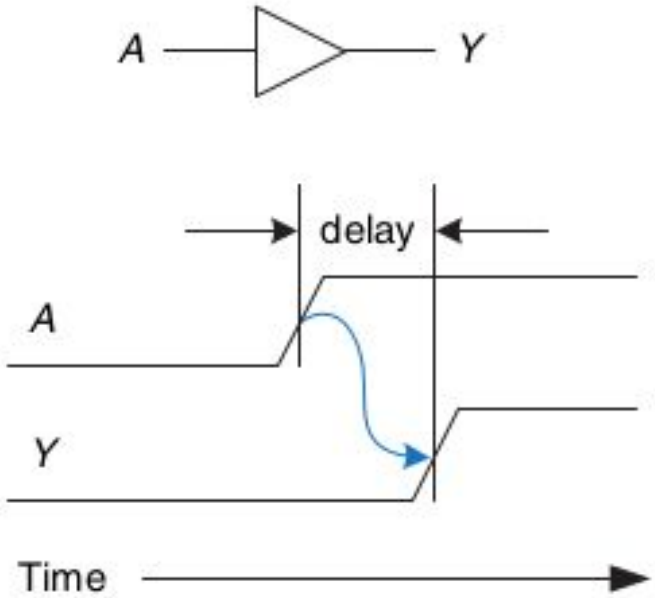
Decoder lojik



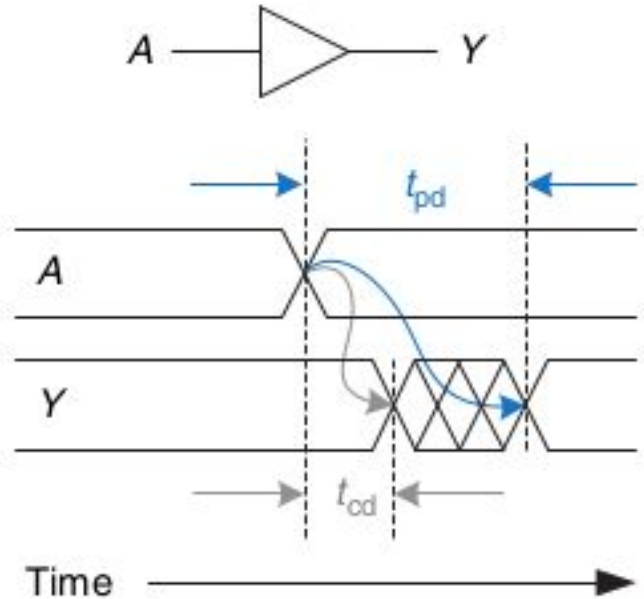
A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0



Zamanlama



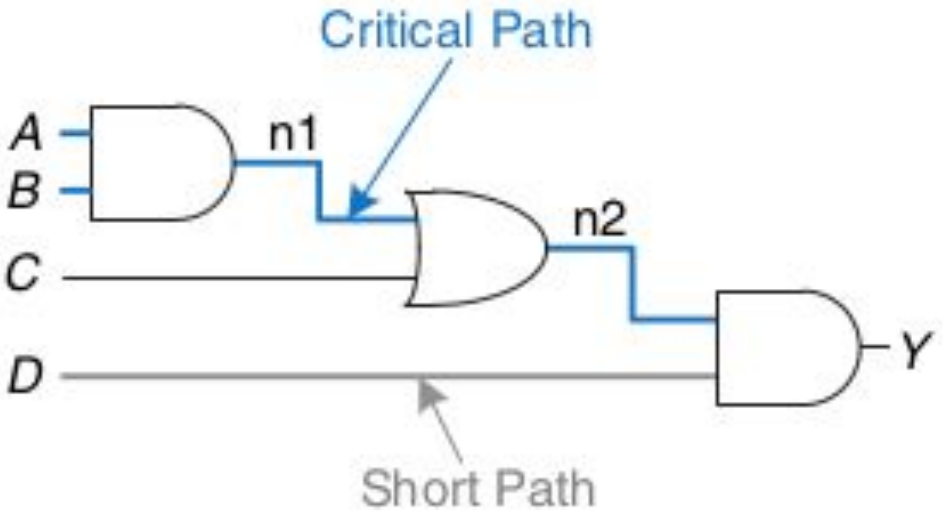
Yayılma ve Kirlenme Gecikmesi



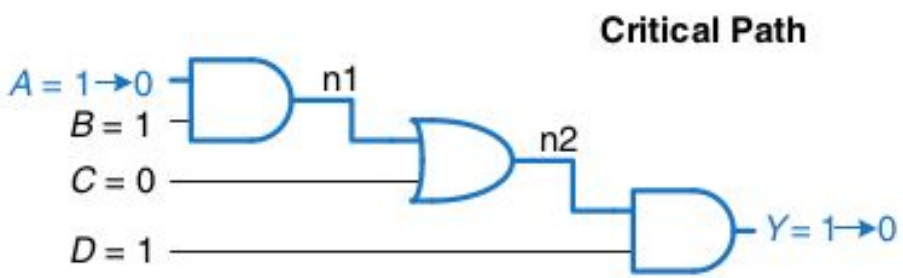
t_{pd}: Yayılma gecikmesi

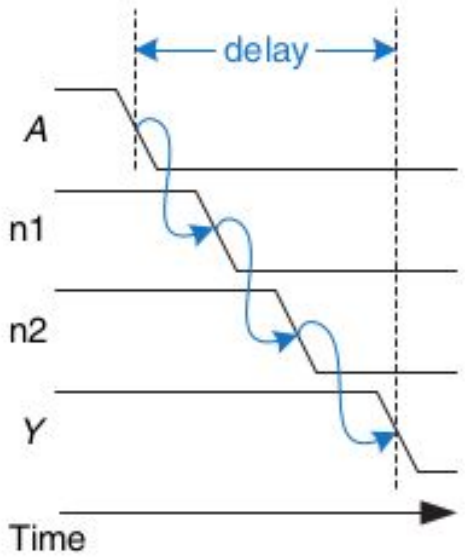
t_{cd}: Kirlenme gecikmesi

Yayılma Gecikmesi



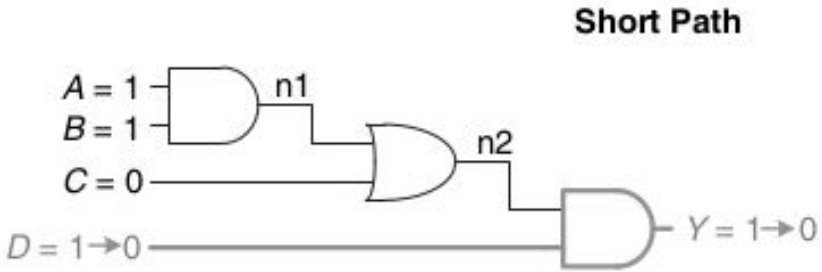
Yayılma Gecikmesi

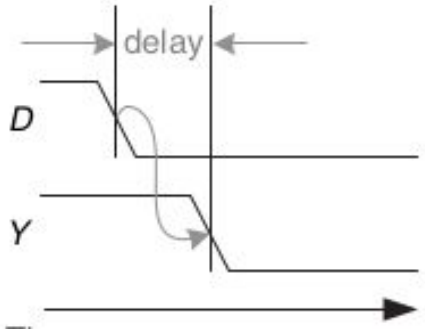




$$t_{pd} = 2t_{pd\_\mathrm{AND}} + t_{pd\_\mathrm{OR}}$$

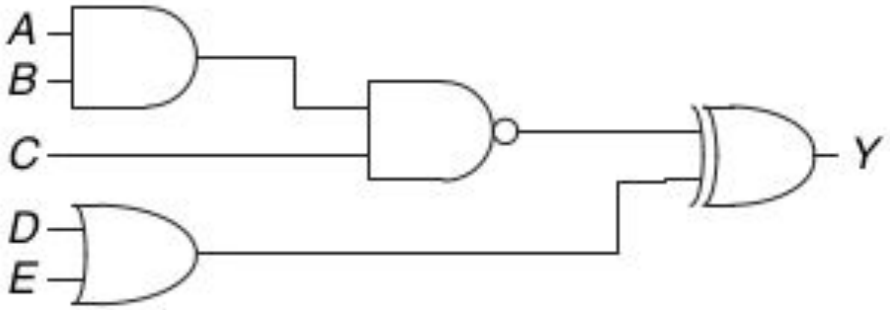
Kirlenme Gecikmesi





$$t_{cd} = t_{cd\_\mathrm{AND}}$$

Gecikmelerin Tespiti Örnek

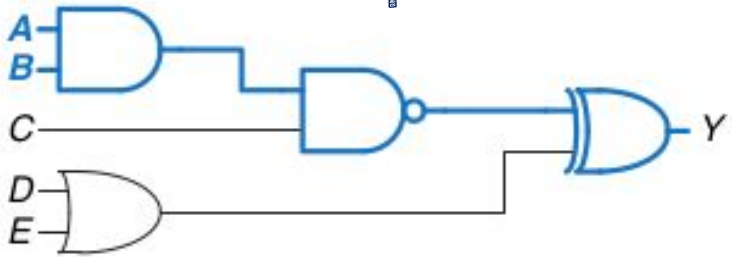


t_{pd}: 100 ps

t_{cd}: 60 ps

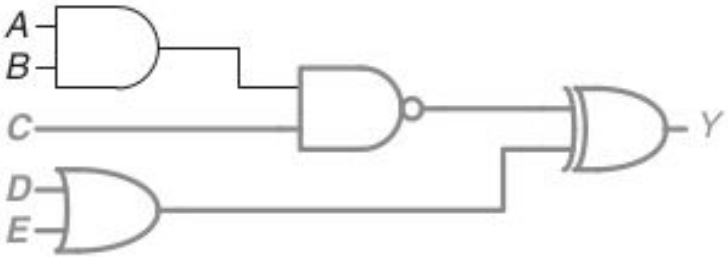
Gecikmelerin Tespiti Örnek

critical path



t_{pd}: 3 x 100 ps = 300 ps

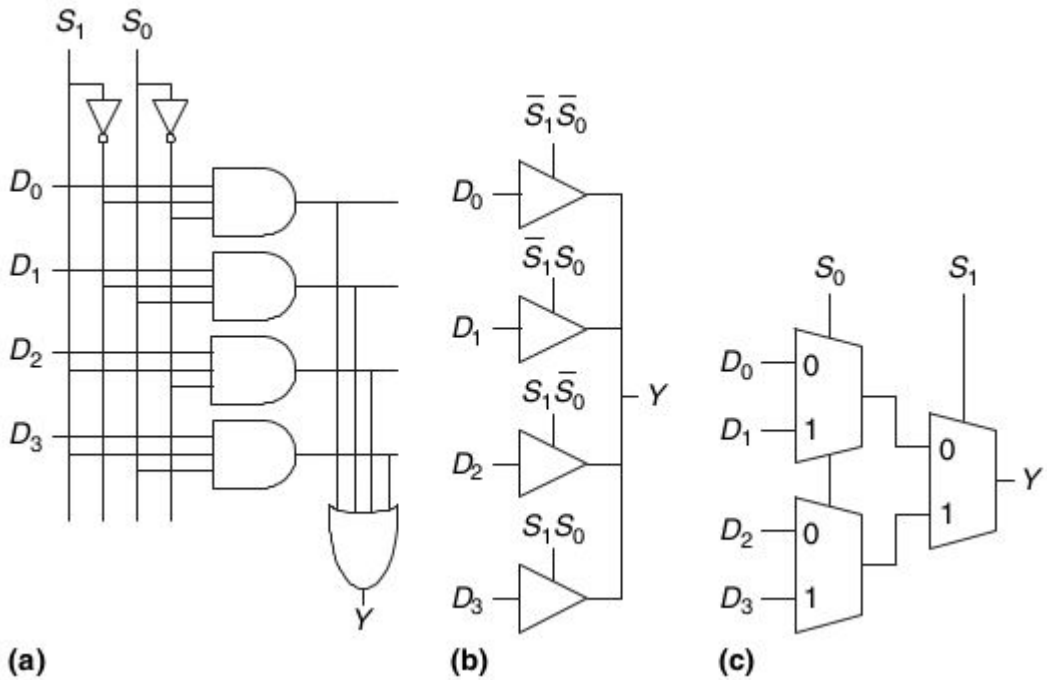
shortest path



t_{cd}: 2 x 60 ps = 120 ps

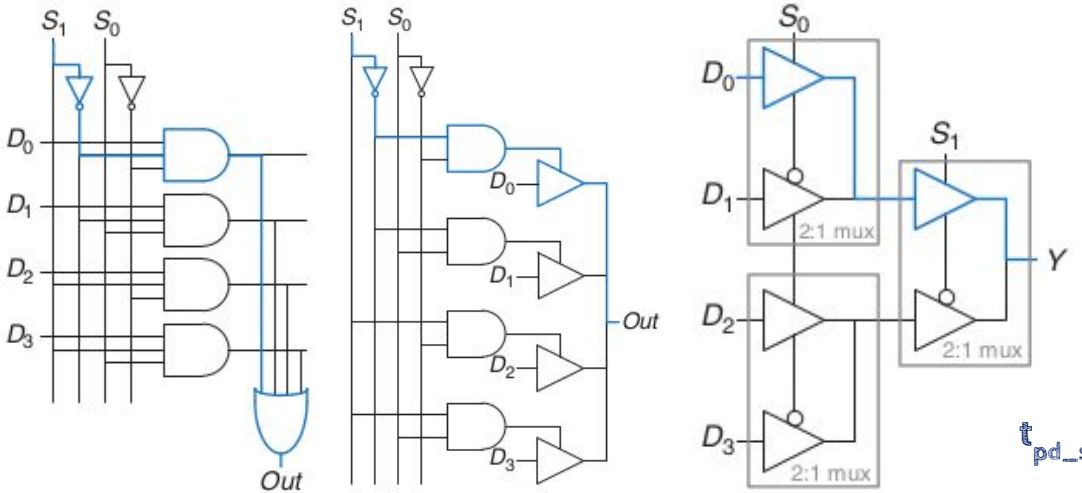
Çoklayıcı (Mux) Zamanlama

Asagıdaki Mux devrelerinin zamanlamalarını karsılastırın



Gate	t_{pd} (ps)
NOT	30
2-input AND	60
3-input AND	80
4-input OR	90
tristate (A to Y)	50
tristate (enable to Y)	35

Çoklayıcı (Mux) Zamanlama



Gate	t_{pd} (ps)
NOT	30
2-input AND	60
3-input AND	80
4-input OR	90
tristate (A to Y)	50
tristate (enable to Y)	35

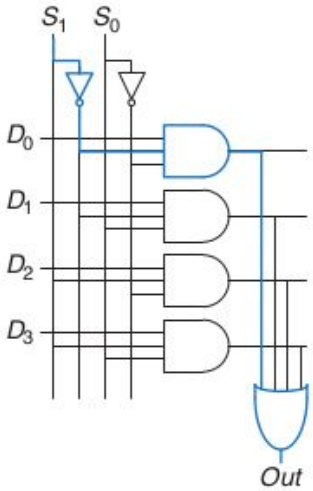
t_{pd_sy}: S ile Y arasındaki yayılma gecikmesi

t_{pd_dy}: D ile Y arasındaki yayılma gecikmesi

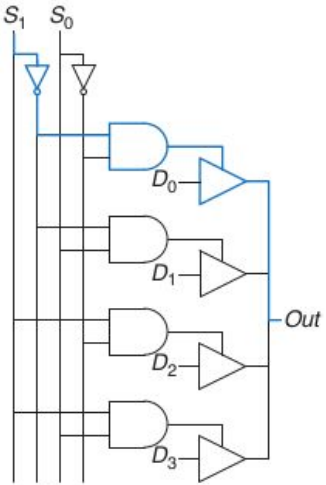
t_{pd}: $\max(t_{pd\_sy}, t_{pd\_dy})$

Çoklayıcı (Mux) Zamanlama

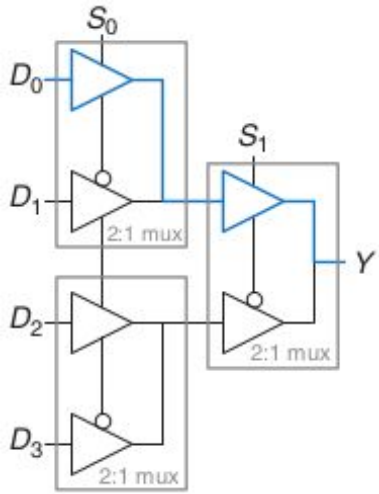
Gate	t_{pd} (ps)
NOT	30
2-input AND	60
3-input AND	80
4-input OR	90
tristate (*A* to *Y*)	50
tristate (enable to *Y*)	35



$$t_{pd\_sy} = t_{pd\_INV} + t_{pd\_AND3} + t_{pd\_OR4}$$
$$= 30\text{ ps} + 80\text{ ps} + 90\text{ ps}$$
$$= \mathbf{200\text{ ps}}$$
$$t_{pd\_dy} = t_{pd\_AND3} + t_{pd\_OR4}$$
$$= \mathbf{170\text{ ps}}$$

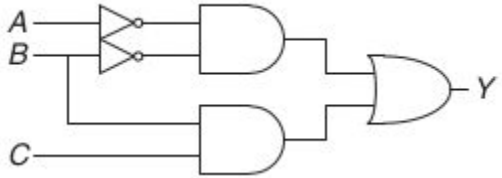


$$t_{pd\_sy} = t_{pd\_INV} + t_{pd\_AND2} + t_{pd\_TRI\_sy}$$
$$= 30\text{ ps} + 60\text{ ps} + 35\text{ ps}$$
$$= \mathbf{125\text{ ps}}$$
$$t_{pd\_dy} = t_{pd\_TRI\_ay}$$
$$= \mathbf{50\text{ ps}}$$



$$t_{pd\_s0y} = t_{pd\_TRLSY} + t_{pd\_TRI\_AY} = \mathbf{85\text{ ns}}$$
$$t_{pd\_dy} = 2\,t_{pd\_TRI\_AY} = \mathbf{100\text{ ns}}$$

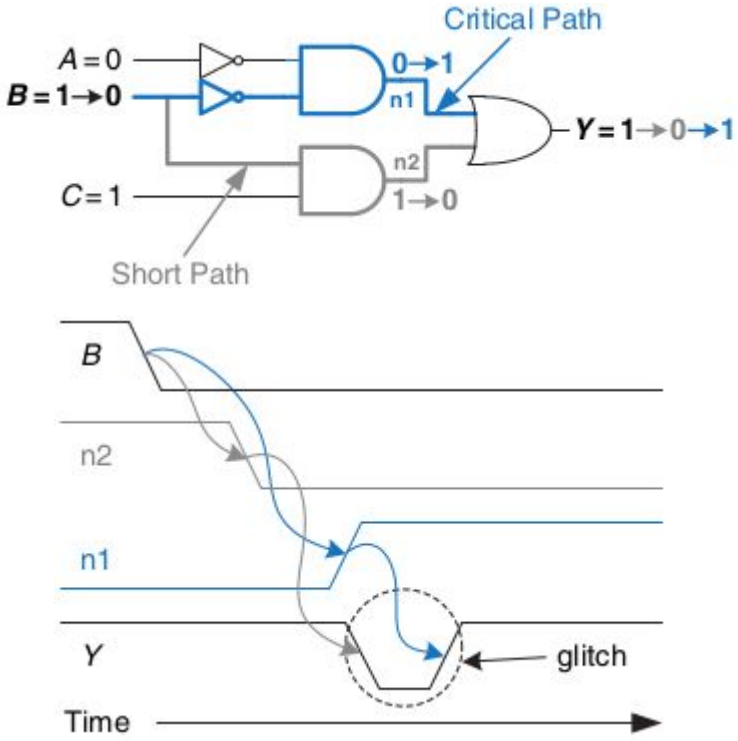
Tek girisin çoklu çıkısı tetiklemesi



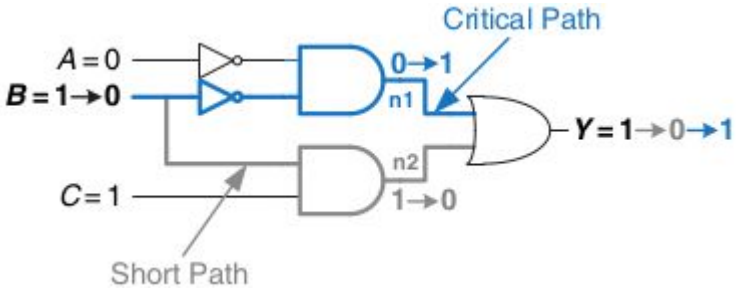
Y \ AB	00	01	11	10
C = 0	1	0	0	0
C = 1	1	1	1	0

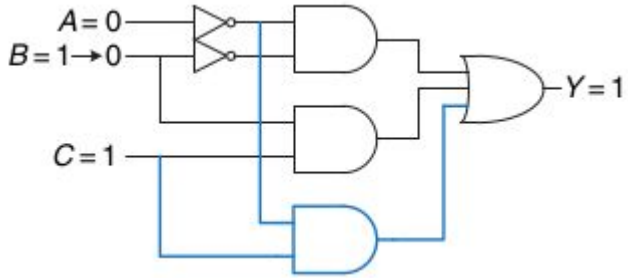
$Y = \overline{A}\overline{B} + BC$

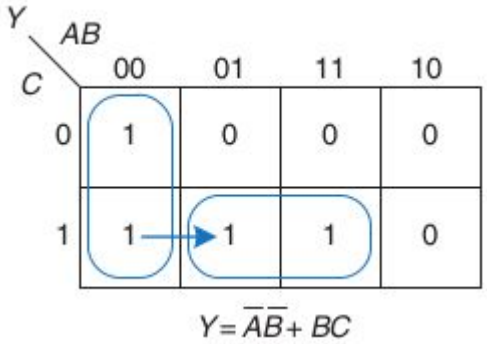
Tek girisin çoklu çıkısı tetiklemesi

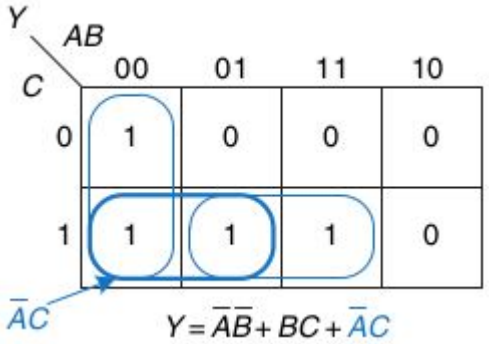


Tek girisin çoklu çıkısı tetiklemesi









Sorular

https://web.cs.hacettepe.edu.tr/~aykut/classes/fall2012/bbm231/sunumlar/lecture3_4.pdf