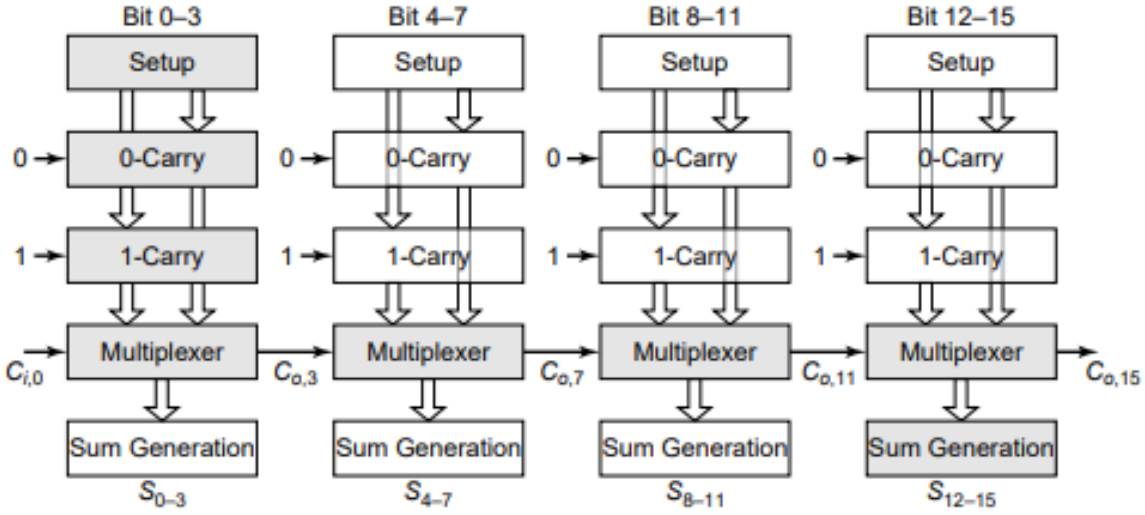
CARRY SELECT ADDER

Carry select adder is implemented in Verilog with 4 stages and each stage consisting of a 4-bit ripple carry adder

The Ripple carry adder modules are defined and instantiated in the Carry select adder



$$t_{add} = t_{setup} + Mt_{carry} + \left(\frac{N}{M}\right)t_{mux} + t_{sum}$$