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ASSIGNMENT CO1

1. Explain the MOS change in MOS band structure with respect to accumulation, depletion and inversion region of operation.

A. The MOS structure exhibits different band bending behavior depending on the applied gate voltage. The three main regions of operation are:-

1. Accumulation region:-

- Occurs when $V_G < 0$ for n-type or $V_G > 0$ for p-type semiconductor.
- The applied gate voltage attracts majority carriers to the oxide-semiconductor interface.
- Band bends upward at the surface.
- No depletion region forms.
- No conduction channel is created.

2. Depletion region:-

- Occurs at small $V_G > 0$ for n-type or $V_G < 0$ for p-type.
- Majority carriers are repelled, forming a depletion region.
- Bands bend downward at the surface.
- Depletion width increases with V_G.
- No conducting channel forms yet.

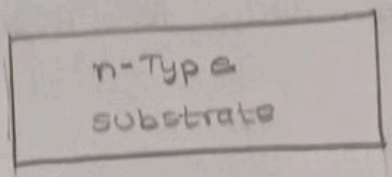
3, Inversion region:-

- Occurs when $V_G > V_T$ for n-type or $V_G < V_T$ for p-type.
- The surface inverts to the opposite type.
- Minority carriers form a inversion layer.
- Bands bend further downward, crossing E_F.
- A conductive channel forms, enabling MOSFET operation.

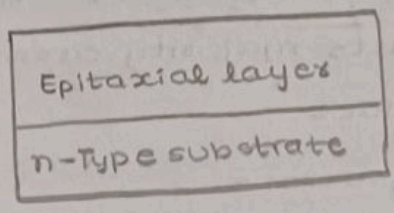
2. Explain the hierachy of steps involved in cmos fabrication using Twin-Tubeprocess.

A. Twin-Tubeprocess:

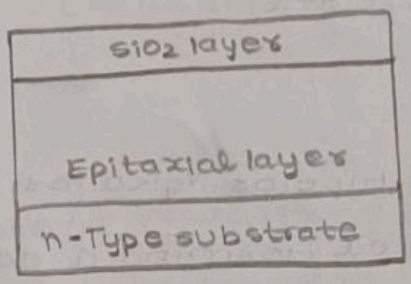
→ Let us use n Type substrate. The resistivity of substrate should be higher.



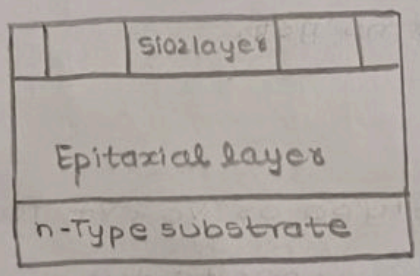
→ Then we should grow n+ layer epitaxially.



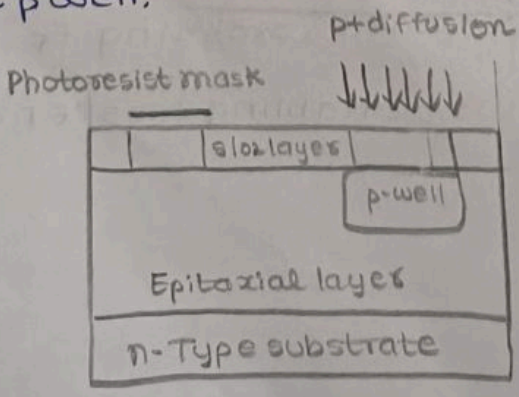
→ After that, substrate is subjected to oxidation & we grow SiO_2 layer.



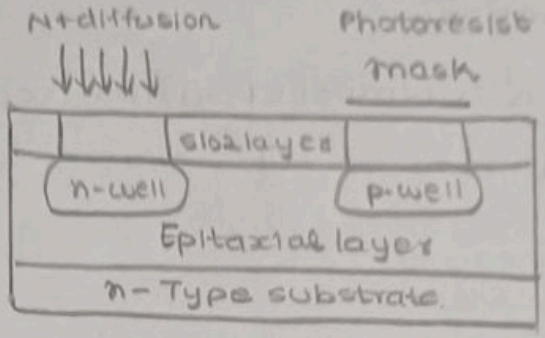
→ SiO_2 layer is etched using masking. Two windows are formed, one for n-well and another for p-well.



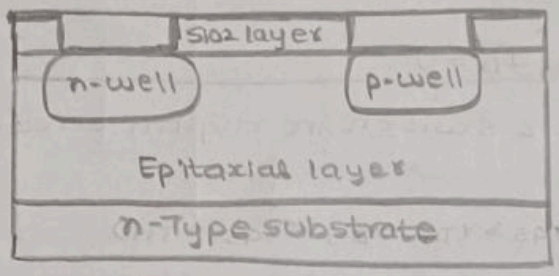
→ 1st window is covered by photoresist mask. Then p-type impurities diffused to form p well.



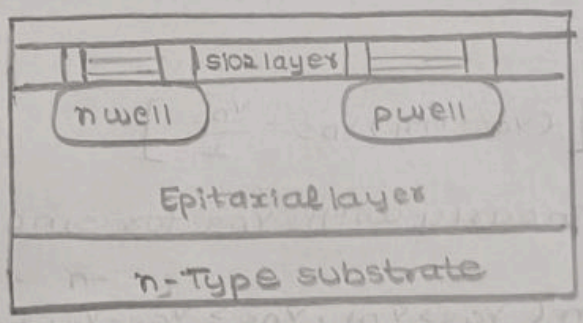
→ 2nd window is covered by photoresist mask. Then n type impurities diffused to form n well.



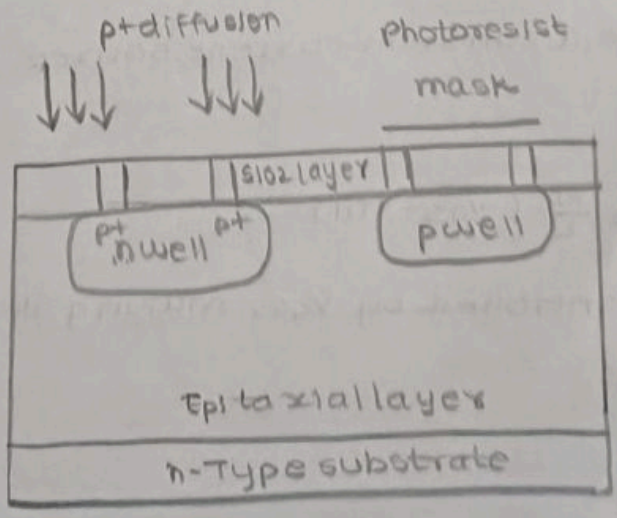
→ Grow Thin SiO2 layer by thermal oxidation for Gate terminal. Grow polysilicon layer for photolithography & pattern making.



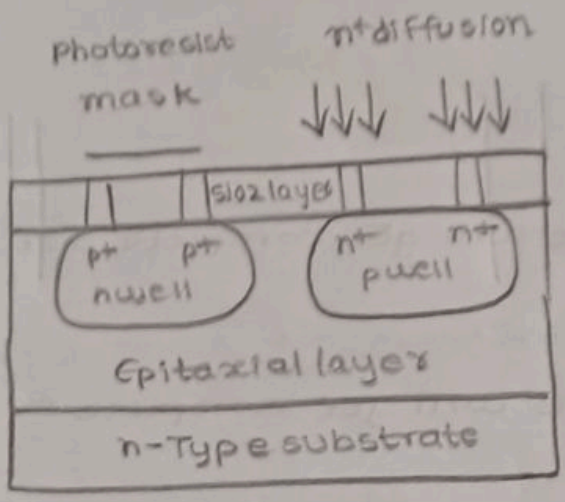
→ Each SiO2 & polysilicon to implant Drain and source.



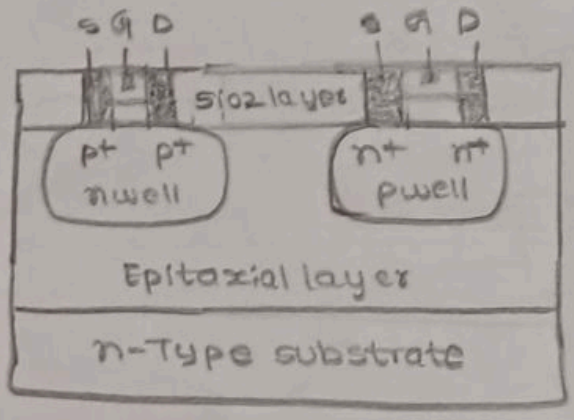
→ p well covered with photoresist mask and p+ diffusion is done to form source and drain region.



→ n well covered with photoresist mask and n^+ diffusion is done to form source and drain region.



→ Metal diffusion is done for contact formation.



Atlast, metal etching is done. contact formation for source S, Drain D and Gate G is done.

3. Describe the drain current equation of a NMOS FET at different modes of operation.

A. The drain current (I_D) in a NMOSFET varies depending on its operating region:

1. Cutoff Region ($V_{GS} < V_{TH}$)

- The NMOS FET is OFF (no conduction).
- The inversion layer does not form because V_{GS} is below the threshold voltage V_{TH}.
- Drain current equation: $I_D = 0$
- The FET acts as an open switch in digital circuits.

2. Linear (Triode) Region ($V_{GS} > V_{TH}$, $V_{DS} < V_{GS} - V_{TH}$)

- The MOSFET behaves like a variable resistor.
- A conductive channel forms, and current flows between drain and source.
- Drain current equation:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

- The current increases linearly with V_{DS} for small values.

3. Saturation (Active) Region ($V_{GS} > V_{TH}$, $V_{DS} \geq V_{GS} - V_{TH}$)

- The channel is pinched off near the drain, & current becomes independent of V_{DS}.
- The mosfet behaves like a constant current source.
- Drain current equation:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

- The current is mainly controlled by V_{GS}, making it useful for amplifier applications.

4. Describe how the gate voltage affects the formation of the inversion layer in an n-channel MOSFET parameters.

A. Formation of N-channel Inversion layer:

The inversion layer forms in an n-channel MOSFET when the gate voltage exceeds a certain threshold (V_{TH}), which is the minimum voltage required to create a conductive channel between the source and drain.

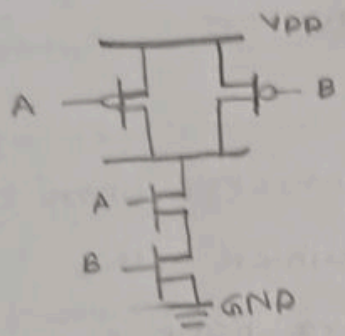
Effect of Gate voltage on Inversion layer formation:

- Gate voltage $V_G \geq V_{TH}$:
  - When the gate voltage exceeds the threshold voltage ($V_G > V_{TH}$), it attracts electrons at the oxide-silicon interface.
  - The concentration of electrons becomes high enough to form a n-type inversion layer, even though the underlying semiconductor is p-type.
  - This inversion layer creates a conductive channel between the source and drain.
- This inversion layer allows current to flow through the MOSFET when a voltage is applied across the drain and source terminals.

5. Explain the CMOS NAND gate using stick diagram.

A. A stick diagram is a simplified graphical representation of the layout of CMOS logic gates. A 2-input CMOS NAND gate consists two PMOS transistors connected in parallel and two NMOS transistors connected in series.

1) CMOS logic style $F = \overline{A \cdot B}$

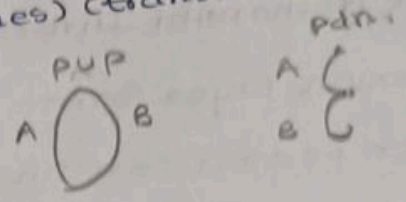


2) Graph

^

vertices edges

(nodes) (transistors)

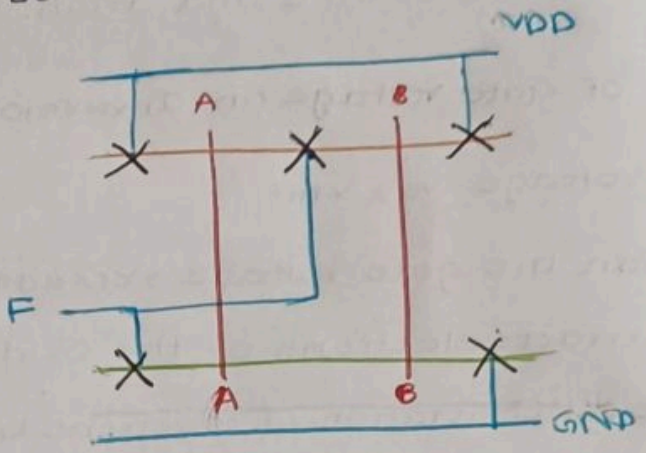


3) Euler's path

Covers all the nodes such that each edge is visited only once

"AB"

4) stick diagram



6. Explain the working operation of CMOS Ex-OR gate and verifying its truth table.

A. A CMOS EX-OR gate combines the behavior of both PMOS & NMOS transistors. It consists of:

- 2 PMOS transistors in parallel, which turn on when their input is 0.
- 2 NMOS transistors in series, which turn on when their input is 1.

Truth Table:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Verification:

1. When A=0 and B=0:

- Both PMOS transistors are on.
- Both NMOS transistors are off.
- Output (Y)=1

2. When A=0 and B=1:

- PMOS for A is on, PMOS for B is off.
- NMOS for A is off, NMOS for B is on.
- Output (Y)=0

3. When A=1 and B=0:

- PMOS for A is off, PMOS for B is on
- NMOS for A is on, NMOS for B is off
- Output (Y)=0

4. When A=1 and B=1:

- Both PMOS transistors are off.
- Both NMOS transistors are on.
- Output(Y)=1.

7. Illustrate how channel-length modulation alters the I-V characteristics of a MOSFET in the saturation region.

A. Channel-length modulation in a MOSFET affects its I-V characteristics in the saturation region, making the drain current (I_D) increase slightly with increasing drain-to-source voltage (V_{DS}).

Illustration of the Effect on I-V characteristics:

1. Without channel Length modulation (Ideal case)

- The saturation region ($V_{DS} > V_{GS} - V_T$) has a flat I_D vs V_{DS} curve.
- The drain current remains almost constant with V_{DS}.

2. With channel-length modulation (Real case)

- The saturation region shows a slight increase in I_D as V_{DS} increases.
- The output characteristic curves (I_D vs V_{DS}) now have a small slope.

- The drain current is given by:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

where λ represents CLM.

5. Explain the operating regions of an MOSFET using the I-V characteristics.

A. A MOSFET operates in three key regions depending on the gate-to-source voltage and drain-to-source voltage.

1. Cutoff Region:

- Condition: $V_{GS} < V_T$
- Behaviour: The MOSFET is OFF.
- Drain current: $I_D \approx 0$
- I-V characteristics: The flat curve near $I_D = 0$, showing almost no drain current.

2. Linear (Triode) Region:

- condition: $V_{DS} < V_{GS} - V_T$
- Behaviour: The MOSFET acts as a variable resistor.
- Drain current:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

- I-V characteristics: The parabolic curve in the small V_{DS} region, showing increasing I_D with V_{DS}.

3. Saturation (Active) Region:

- Condition: $V_{DS} \geq V_{GS} - V_T$
- Behaviour: The MOSFET acts as a current source.
- Drain current:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

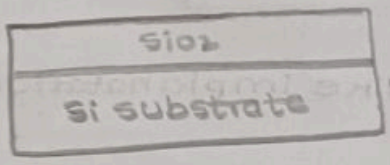
- I-V characteristics:

The flat region, but with a small positive slope due to channel-length modulation.

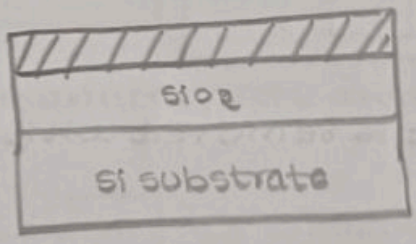
9. Describe the key steps involved in the philothography process during the fabrication of an mos transistor.

A. Photolithography is a process of fabricating integrated circuit layer by layer on silicon wafer.

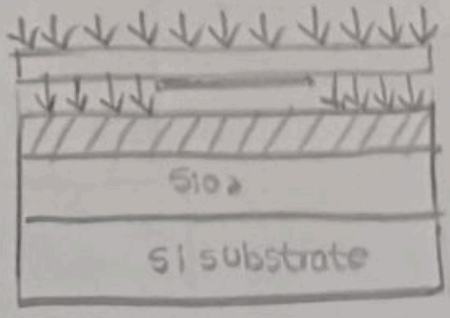
→ Oxidation: SiO_2 layer is deposited.



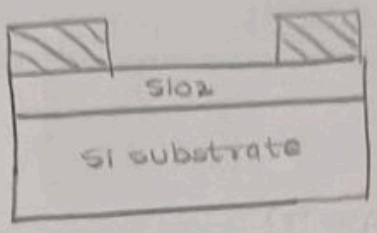
→ Photoresist coating: Light-sensitive polymer is applied.



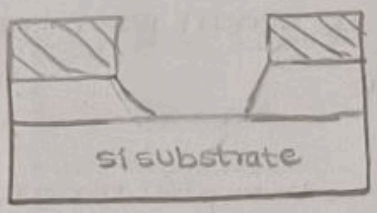
→ Exposure: UV light transfers the pattern using a mask.



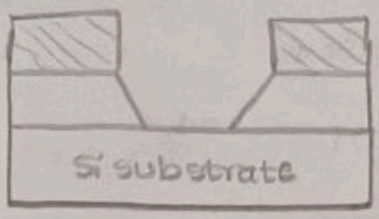
→ Soft Baking: Unexposed resist is removed and hardened.



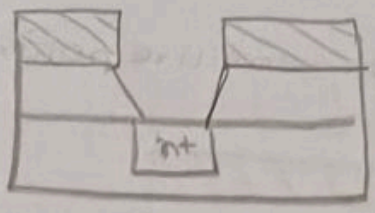
→ Etching: Exposed material is removed.



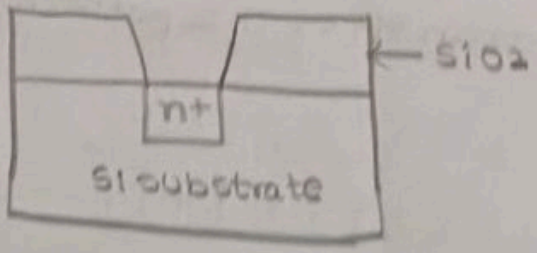
→ SRD: Wafer is cleaned and dried



→ Processing: Further steps like implanatation or deposition.

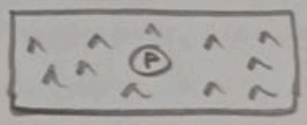


→ Ashing: Remaining resist is removed with plasma.

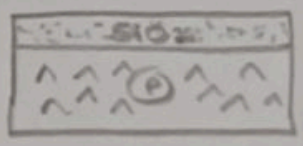


10. Illustrate the sequence of steps involved in fabricating nMOSFET.

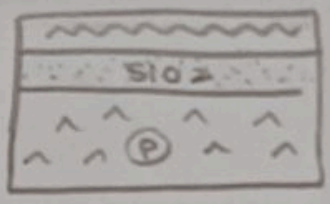
A. → consider p-substrate



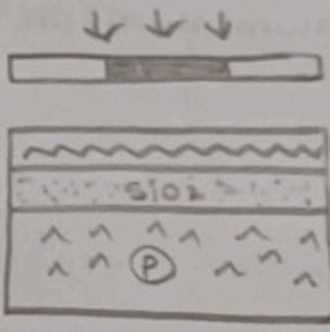
→ Deposite oxide layer using oxidation.



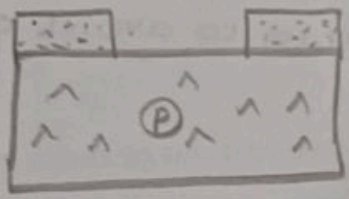
→ Apply photoresist layer.



→ Apply UV rays through mask

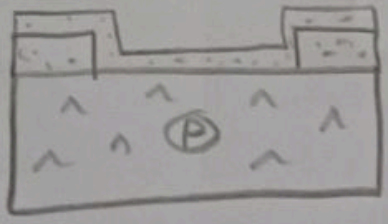


→ Etching: removing unwanted / soft area

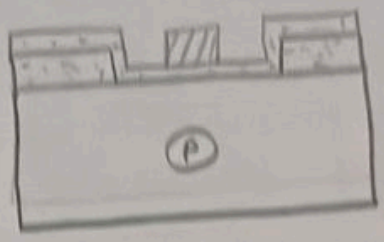


→ window structure

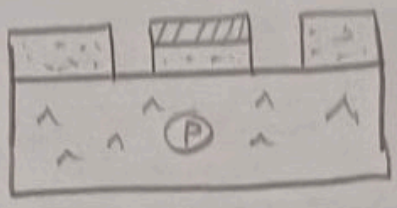
→ Using thin oxidation, create SiO_2 on the substrate.



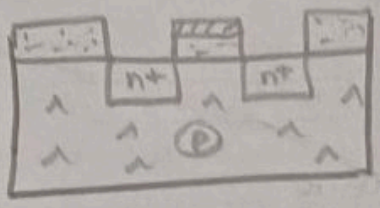
→ Using chemical vapour deposition, create polysilicon at centre.



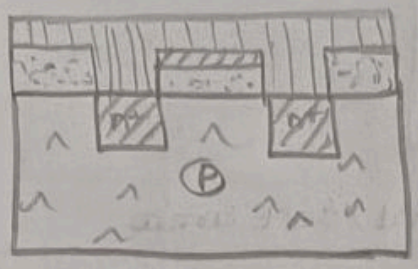
→ Using photolithography, create windows to diffuse n^+ regions.



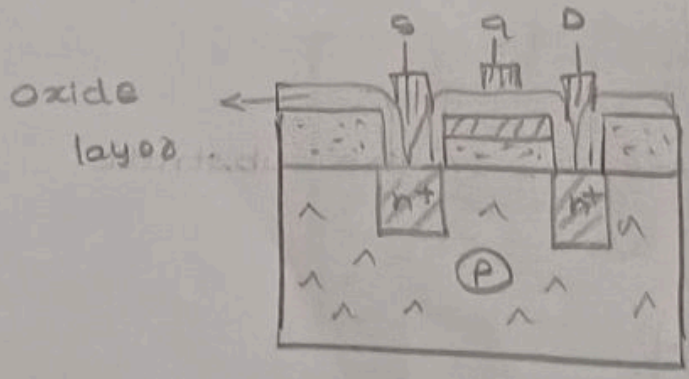
→ Diffuse two n^+ regions using diffusion.



→ Using metallisation, deposits metal (aluminium) on the entire substrate



→ Remove metal layer and deposit oxide to avoid contacts.



11. Describe the DC transfer characteristic having different gate voltages 0V, 1V, 2V and 4V.

A. DC transfer characteristics:

1. $V_{in} = 0V$

→ PMOS is fully ON

→ NMOS is OFF

→ $V_{out} \simeq V_{DD}$.

2. $V_{in} = 1V$

→ PMOS remain ON, keeping $V_{out} \simeq V_{DD}$.

→ Iff $V_{DD} = 5V$, the NMOS is still OFF.

→ No significant change in output.

3. $V_{in} = 2V$

→ PMOS starts turning OFF.

→ NMOS starts to turn ON partially

→ V_{out} starts decreasing.

4. $V_{in} = 4V$

→ PMOS is nearly OFF.

→ NMOS is strongly ON

→ $V_{out} \approx 0$

12. Tabulate the I-V expressions of NMOS and PMOS field effect transistors for different modes of operation.

A.

Mode	Condition	NMOS current	PMOS current
Cutoff (OFF)	$V_{GS} < V_T$	$I_D = 0$	$I_D = 0$
Linear (Triode)	$V_{GS} > V_T$ $V_{DS} < V_{GS} - V_T$	$I_D = \mu_n C_{OS} \frac{W}{L}$ $[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2}]$	$I_D = K_p * (V_{GS} - V_{th})$ $* V_{DS}$
Satura-tion (Active)	$V_{GS} > V_T$, $V_{DS} \geq V_{GS} - V_T$	$I_D = \frac{1}{2} \mu_n C_{OS} \frac{W}{L}$ $(V_{GS} - V_T)^2$	$I_D = \frac{1}{2} \times K_p *$ $(V_{GS} - V_{th})^2$