Department of Electronics and Communication Engineering

CO2 Assignment Questions

1. Explain briefly about the average power dissipated by a CMOS inverter over one entire time period.
2. Explain the advantages of linear load NMOS inverter over saturated load NMOS inverter.
3. A digital circuit has a known propagation delay of 10ns. Using the delay estimation formula, calculate the critical path delay for a combinational circuit with 5 logic gates connected in series.
4. Apply the concept of logical effort to size the transistors in a CMOS circuit for minimizing delay. Assume a specific fan-out.
5. For a CMOS circuit operating at a specific frequency 100MHz and supply voltage of 15V, calculate the dynamic power dissipation. Consider the gate capacitance as 10μF.
6. A scaled-down CMOS process reduces transistor area by a factor of 1/2. Calculate the resulting improvement in the transistor dimensions.
7. Explain the dynamic behavior of a CMOS inverter during switching.
8. Design a CMOS circuit to drive a capacitive load of 40 fF. The circuit consists of 4 stages with a combined logical effort of 2. Calculate the optimal stage effort and determine the size of each stage to minimize delay.
9. For a clock signal routed through an interconnect with R=50 Ω and C=200 fF, calculate the propagation delay using the lumped RC model.
10. A circuit has a setup time of 1.5 ns, hold time of 0.5 ns, and clock period of 4 ns. Calculate the timing margin for correct operation.
11. For a resistive-load inverter with RL=5 kΩ, calculate the propagation delay if the load capacitance is 20 fF.
12. For a technology scaling factor of 0.707, calculate the impact on transistor area, delay, and power dissipation for a CMOS inverter with initial dimensions of 1 μm.
13. Design a resistive-load inverter with RL=10 kΩ, VDD=5 V, and VT=1 V. Calculate the voltage transfer characteristic (VTC) and determine the noise margins.
14. Design a CMOS circuit to drive a capacitive load of 40 fF. The circuit consists of 4 stages with a combined logical effort of 2. Calculate the optimal stage effort and determine the size of each stage to minimize delay.