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ASSIGNMENT CO2

1. Explain briefly about the power / average power dissipated by a CMOS inverter over one entire time period.

A. The average power dissipated by a CMOS inverter over one entire time period consists of three components :-

→ static power dissipation (P_S)

→ Dynamic power dissipation (P_D)

→ short circuit power dissipation (P_{SC})

∴ Total power dissipation

$$P_T = P_S + P_D + P_{SC}$$

where,

$$P_D = C_L V_{DD}^2 f_p$$

$$P_S = I_{leakage} \times V_{DD}$$

$$P_{SC} = \frac{K}{2}(V_{DD} - 2V_t)^3 \frac{t_{rf}}{t_p}$$

$$\therefore P_T = C_L V_{DD}^2 f_p + I_{leakage} \times V_{DD} + \frac{K}{2}(V_{DD} - 2V_t)^3 \frac{t_{rf}}{t_p}$$

2. Explain the advantages of linear load NMOS inverter over saturated load NMOS inverter.

A. Advantages :-

→ Low power consumption :- Reduces static power dissipation compared to saturated load.

→ Better Noise margins : Provides improved noise immunity and stable operation.

→ Higher voltage swing : Allows output voltage to reach closer to V_{DD}.

→ Low static Power Dissipation: minimizes unnecessary power loss in steady state.

→ Faster switching speed: Avoids deep saturation, leading to quick transitions.

→ Simpler Fabrication: Uses depletion-mode NMOS, making circuit design easier.

3. A digital circuit has a known propogation delay of 10ns. Using the delay estimation formula, calculate the critical path delay for a combinational circuit with 5 logic gates connected in series.

A. Given,

Propogation delay per gate = 10 ns

Number of gates in series = 5

→ Critical path delay = Number of gates × Propogation delay per gate

= 5 × 10ns

= 50 ns.

4. Apply the concept of logical effort to size the transistors in a CMOS circuit for minimizing delay. Assume a specific fan-out.

A. Logical effort is a technique used to size transistors in CMOS circuit for minimum delay by balancing the drive strength of gates.

1. Fanout (H) → ratio of output load capacitance to input capacitance

- Logical effort (G) → A measure of how much harder a gate drives compared to an inverter.

Inverter = g = 1, NAND2 = g = 4/3, NOR2 = g = 5/3

Path Effort (F) → The product of logical effort and electrical effort.

2. Path Effort

$$F = G \times H$$

3. Optimal No. of stages (N):

$$N = \log_4(F)$$

4. Optimal Gate Effort:

$$f = F^{1/N}$$

5. Determine Transistor sizes

- Assign input capacitance c_{in} to each stage.

Example:

Let, consider circuit with three stages & $H = 4$

1. $G = (1) \times (4/3) \times (5/3) = 20/9$
2. $F = G \times H = 20/9 \times 4 = 80/9$
3. $N = \log_4(80/9) \approx 3$
4. $f = F^{1/N} = (80/9)^{1/3} \approx 2.3$
5. To maintain equal effort

   Inverter size $c_{in} = 1$

   NAND2 size $c_{in} = 2.3$

   NOR2 size $c_{in} = (2.3)^2 = 5.3$

5. For a CMOS circuit operating at a specific frequency 100MHz and supply voltage of 15V. Calculate the dynamic power dissipation. Consider the gate capacitance as 10μF.

A. Given,

$f_p = 100MHz = 100 \times 10^6 Hz$

$V_{DD} = 15V$

$C_L = 10\mu F = 10 \times 10^{-6} F$

$\Rightarrow$ Dynamic power dissipation $= C_L V_{DD}^2 f_p$

$= (10 \times 10^{-6})(15)^2 (100 \times 10^6)$

$= 1000 \times 225$

$= 225 kW$

6. A scaled-down CMOS reduces transistor area by a factor of 1/2. Calculate the resulting improvement in the transistor discussions.

A. Given

scaling factor $= 1/2$

In CMOS, transistor area is $\propto$ to square of the feature size

$$\boxed{A \propto L^2}$$

$$A_{new} = \frac{1}{2} A_{old}$$

$$L^2_{new} = \frac{1}{2} L^2_{old}$$

$$L_{new} = \frac{L_{old}}{\sqrt{2}}$$

$$L_{new} \approx 0.707 L_{old}$$

∴ Transistor length and width are reduced by a factor of 0.707 ($1/\sqrt{2}$). This results in smaller transistor dimensions, leading to improved switching speed, reduced capacitance and lower power consumption.

7. Explain the dynamic behavior of a CMOS inverter during switching.

A. The dynamic behaviour of a CMOS inverter refers to how the output voltage transitions between logic high and logic low when the input changes. The switching process involves:

1. charging phow (Low-to-High):

The process where the output voltage transitions from Low (0V) to High (V_{DD}) as the load capacitance charges through the PMOS transistor.

2. Discharging phase (High-to-Low):

The process where the output voltage transitions from HIGH (V_{DD}) to LOW (0V) as the load capacitance discharges through the NMOS transistor.

3. Propogation delay:

Time taken for output to respond to input.

$$t_p = \frac{t_{PLH} + t_{PHL}}{2}$$

4. Dynamic Power Dissipation:

The power consumed due to switching activity.

$$P_d = C_L V_{DD}^2 f_p.$$

8. Design a CMOS circuit to drive a capacitive load of 40ff. The circuit consists of 4 stages with a combined signal logical effort of 2. Calculate the optimal stage effort and determine the size of each stage to minimize delay.

A. Given,

$C_L = 40ff$, $N = 4$, $G = 2$

1. Path effort:

$$F = G \times H$$

Assume the initial gate has an input capacitance of C_{in}:

$$H = \frac{C_L}{C_{in}}$$

$$\therefore \quad F = 2 \times \frac{C_L}{C_{in}}$$

2. Optimal stage effort:-

$$f = F^{1/N}$$

$$f = \left(2 \times \frac{C_L}{C_{in}}\right)^{1/4} = \left(2 \times \frac{40}{C_{in}}\right)^{1/4}$$

Let, $C_{in} = 5fF$

$$f = \left(2 \times \frac{40}{5}\right)^{1/4}$$

$$f = (16)^{1/4}$$

$$f = (2^4)^{1/4}$$

$$f = 2$$

3. Gate size:

→ $C_1 = f \times C_{in} = 2 \times 5 = 10fF$

→ $C_2 = f \times C_1 = 2 \times 10 = 20fF$

→ $C_3 = f \times C_2 = 2 \times 20 = 40ff$

→ $C_4 = f \times C_3 = C_L = 40ff$

∴ C_4 matches with C_L

To minimize delay, the transistor sizes should be increase by a factor of 2 per stage.

9. For a clock signal routed through an interconnect with $R = 50\Omega$ and $C = 200fF$. calculate the propogation delay using the lumped RC model.

A. Given,

$R = 50\Omega$, $C = 200fF = 200 \times 10^{-15} F$

Propogation delay (RC model):

$$t_p = 0.69 \times R \times C$$

$$t_p = 0.69 \times 50 \times 200 \times 10^{-15}$$

$$t_p = 0.69 \times 10000 \times 10^{-15}$$

$$t_p = 6900 \times 10^{-15}$$

$$t_p = 6.9 \times 10^{-12}$$

$$t_p = 6.9\ ps$$

10. A circuit has a setup time of 1.5ns, hold time of 0.5ns, and clock period of 4ns. Calculate the timing margin for correct operation.

A. Given

$t_{setup} = 1.5ns$

$t_{hold} = 0.5ns$

$T = 4ns$

Margin for setup time:

The data must arrive at least tsetup before next clock edge.

$T - t_{setup}$

$= 4 - 1.5$

$= 2.5ns$

Margin for hold time:

The data must remain stable for at least thold after clock edge.

Data Arrival Time - thold

The circuit delay should be greater than thold for correct operation.

11. For a resistive-load inverter with $R_L = 5k\Omega$, Calculate the propogation delay if the load capacitance is 20fF.

A. Given,

$R_L = 5k\Omega$

$C_L = 20fF = 20 \times 10^{-15} F$

→ Propogation Delay for resistive-load inverter:

$$t_p = 0.69 \times R_L \times C_L$$

$$t_p = 0.69 \times 5 \times 10^3 \times 20 \times 10^{-15}$$

$$t_p = 0.69 \times 5000 \times 20 \times 10^{-15}$$

$$t_p = 0.69 \times 100000 \times 10^{-15}$$

$$t_p = 0.69 \times 10^{-10}$$

$$t_p = 69 \times 10^{-12}$$

$$t_p = 69 \text{ ps}$$

12. For a technology scaling factor of 0.707, calculate the impact on transistor area, delay, and power dissipation for a CMOS inverter with initial dimensions of 1 μm.

A. Given,

$$S = 0.707$$

Initial dimensions = 1 μm

⇒ Impact on transistor area:

we know that

$$A' = A \times S^2$$

$$A' = \frac{W}{L} \times (1 \times 1) \times (0.707)^2$$

$$A' = 1 \times 0.5$$

$$A' = 0.5 \mu m^2$$

Area reduces by 50%.

$t_p \propto R \propto C$

$t_p' = R' \times C'$

$t_p' = \left(R \times \frac{1}{s}\right)(C \times s)$

$t_p' = R \times C \times s$

$t_p' = t_p \times s$

⇒ Impact on Propogation Delay:-

$t_p' = t_p \times s$

$t_p' = t_p \times 0.707$

$t_p' \approx 0.707\, t_p$

Delay reduces by 29.3%

⇒ Impact on Power dissipation:-

Dynamic :-

$P_d = CV^2 f$

$C' = C \times s, \quad V' = V \times s, \quad f' = f \times \frac{1}{s}$

$P_d' = CV^2 f$

$= (C \times s)(V \times s)^2 (f \times \frac{1}{s})$

$= CV^2 f \times \cancel{s} \times s^2 \times \frac{1}{\cancel{s}}$

$P_d' = P_d \times s^2$

$P_d' = P_d \times (0.707)^2$

$P_d' = P_d \times 0.354$

reduces by 64.6%.

$\%\text{ Reduction} = \left(1 - \frac{P_d'}{P_d}\right) \times 100$

$= (1 - 0.354) \times 100$

$= 0.646 \times 100$

$= 64.6\%$

static :-

$P_S = V \times I_{leak}$

$V' = V \times S$, $I'_{leak} = I_{leak} \times S$

$P_S' = (V \times S) \times (I_{leak} \times S)$

$P_S' = V \times I_{leak} \times S^2$

$P_S' = P_S \times S^2$

$P_S' = P_S \times (0.707)^2$

$P_S' = P_S \times 0.5$

$\%$ Reduction $= \left(1 - \frac{P_S'}{P_S}\right) \times 100$

$= (1 - 0.5) \times 100$

$= 0.5 \times 100$

$= 50\%$

13. Design a resistive-load inverter with $R_L = 10K\Omega$, $V_{DD} = 5V$, $V_T = 1V$. Calculate the voltage transfer characteristic (VTC) and determine the noise margins.

A. Given

$R_L = 10K\Omega$, $V_{DD} = 5V$, $V_T = 1V$.

1. VTC :-

Case 1: Cutoff Region

When $V_{in} < V_T$, the NMOS is off, that means there is no current flows through R_L, the output remains at V_{DD}.

$V_{out} = V_{DD} = 5V$.

case 2: Linear region ($V_T \leq V_{in} \leq V_{out} + V_T$)

The NMOS turns ON, but the drain-source voltage is small.

$$I_D = K\left[2(V_{in} - V_T)V_{out} - V_{out}^2\right]$$

Current through load-resistor:

$$I_D = \frac{V_{DD} - V_{out}}{R_L}$$

case-3: Saturation region ($V_{in} > V_{out} + V_T$)

The NMOS is fully ON.

$$I_D = K(V_{in} - V_T)^2$$

Current through load-resistor:

$$I_D = \frac{V_{DD} - V_{out}}{R_L}$$

By equating, we get the output voltage for large V_{in}.

2. Noise margin:

It determines how much noise the inverter can tolerate while maintaining correct operation.

$$NM_L = V_{IL} - 0V$$

$$NM_H = 5V - V_{IH}$$

14. Design a cmos circuit to drive a capacitive load of 40fF. The circuit consists of 4 stages with a combined logical effort of 2. Calculate the optimal stage effort and determine the size of each stage to minimize delay.

A. Given,

$C_L = 40fF$, $N = 4$, $G = 2$

1. Path effort

$$F = G \times H$$

$$F = 2 \times \frac{C_L}{C_{in}}$$

$$F = 2 \times \frac{40}{1} \qquad (\because C_{in} = 1)$$

$$F = 80$$

2. Optimal stage effort

$$f = F^{1/N} = (80)^{1/4} = 3.17$$

3. Size

$$h = \frac{C_{out}}{C_{in}} = f$$

$C_4 = C_L = 40ff$

$$C_3 = \frac{C_4}{f} = \frac{40}{3.17} = 12.6\,fF$$

$$C_2 = \frac{C_3}{f} = \frac{12.6}{3.17} = 4.0\,fF$$

$$C_1 = \frac{C_2}{f} = \frac{4.0}{3.17} = 1.26\,fF$$

Each stage should have a size ratio of 3.17 relative to the previous stage.