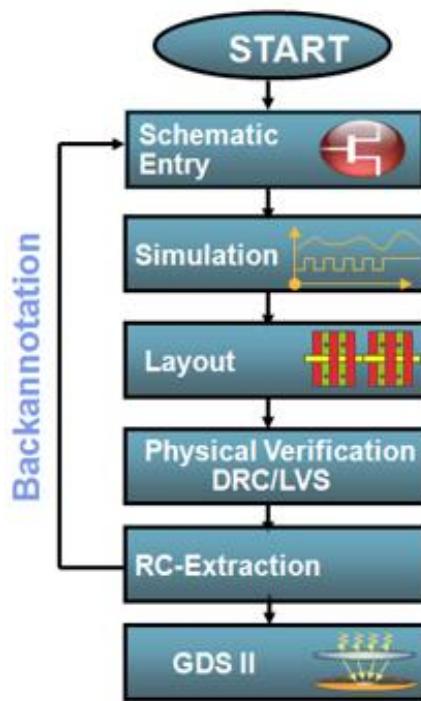


## FULL CUSTOM IC DESIGN FLOW

The flow chart for the Full Custom IC Design Flow is as follows:



**SCHEMATIC ENTRY:** The CMOS circuit will be designed based on the specification and the design will be captured **Virtuoso Schematic Editor**.

**SIMULATION:** Once the circuit is captured on the Virtuoso Schematic Editor, its functional behavior can be verified using **Spectre**.

**LAYOUT:** Layout is nothing but the physical representation of the components in the circuit based on the Length (L) and Width (W) of the components. It also gives an idea of how the components look like in a fabricated IC. The tool for layout capture is **Virtuoso Layout Editor**.

**PHYSICAL VERIFICATION:** Physical Verification is the process of checking out whether the design rules have been followed while designing the circuit. There are two steps involved in Physical Verification: (1) DRC (Design Rule Check) (2) LVS (Layout versus Schematic)

1. **DRC:** Each technology node will have certain set of rules that are to be followed while designing an analog layout. The process of verifying the design with design rules for the respective technology nodes is called DRC.
2. **LVS:** The layout that is created should be a copy of the schematic in terms of electrical connectivity. Comparison of schematic and layout in terms of netlist is called LVS.

Physical Verification in Cadence is carried out using a tool called **Assura (or) PVS**.

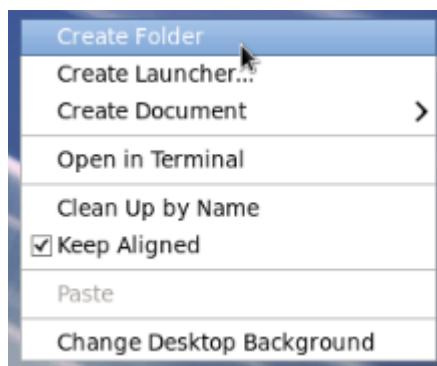
**RC-EXTRACTION:** Due to connectivity and layers used in the layouts, RC-Components are created in the design. These RC-Components are called Parasitics. **Quantus-QRC** is the tool to extract these parasitic components.

**BACKANNOTATION:** To check the impact of parasitic components, we import them to the schematic and resimulate the design. This process is called Backannotation.

**GDSII:** The Stream-Out file is generated through **Virtuoso**.

### WORK SPACE CREATION:

Make a right click on the Desktop and select the option “**Create Folder**” as given in Figure-1.



**Figure-1**

Name the folder, for example, we have named it as “inverter” as shown in Figure-2.



**Figure-2**

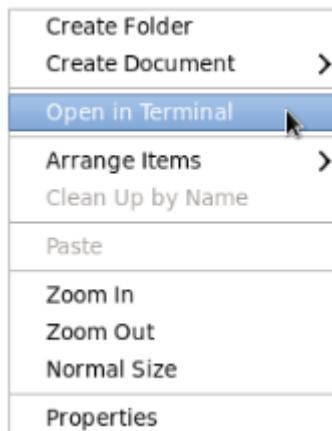
Open the created folder and you get the window as in Figure-3.



**Figure-3**

### INITIALISING csh & SOURCING cshrc:

Make a right click and select the option “**Open in Terminal**” as given in Figure-4.



**Figure-4**

Type the command “csh” to initialize shell and source the cshrc file with the command “source /home/cad/cshrc” or “source /cad/cshrc” (i.e) after “source” command, the exact path for the “cshrc” file should be given.

### INVOKING VIRTUOSO:

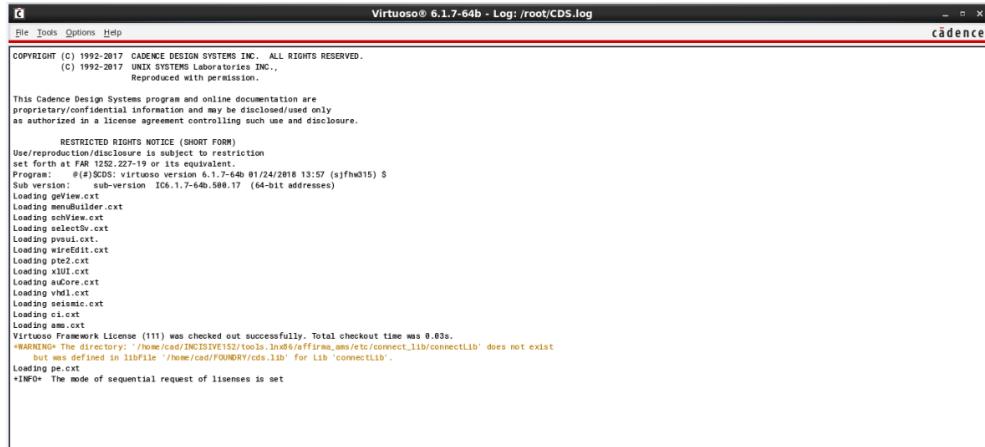
Soon after we source the “cshrc” file, we get a display “Welcome to Cadence Tools Suite”. Now invoke virtuoso using the command “virtuoso &” or “virtuoso” as given in Figure-5.

```
Welcome to Cadence Tools Suite

[root@navin iipvs_test]# virtuoso &
[1] 32165
[root@navin iipvs_test]#
```

**Figure-5**

We get a virtuoso window as given in Figure-6.



**Figure-6**

### CREATE A LIBRARY:

In virtuoso's top menu, select “Tools” and select “Library Manager”. The Cadence Library Manager appears as given in Figure-7(b).

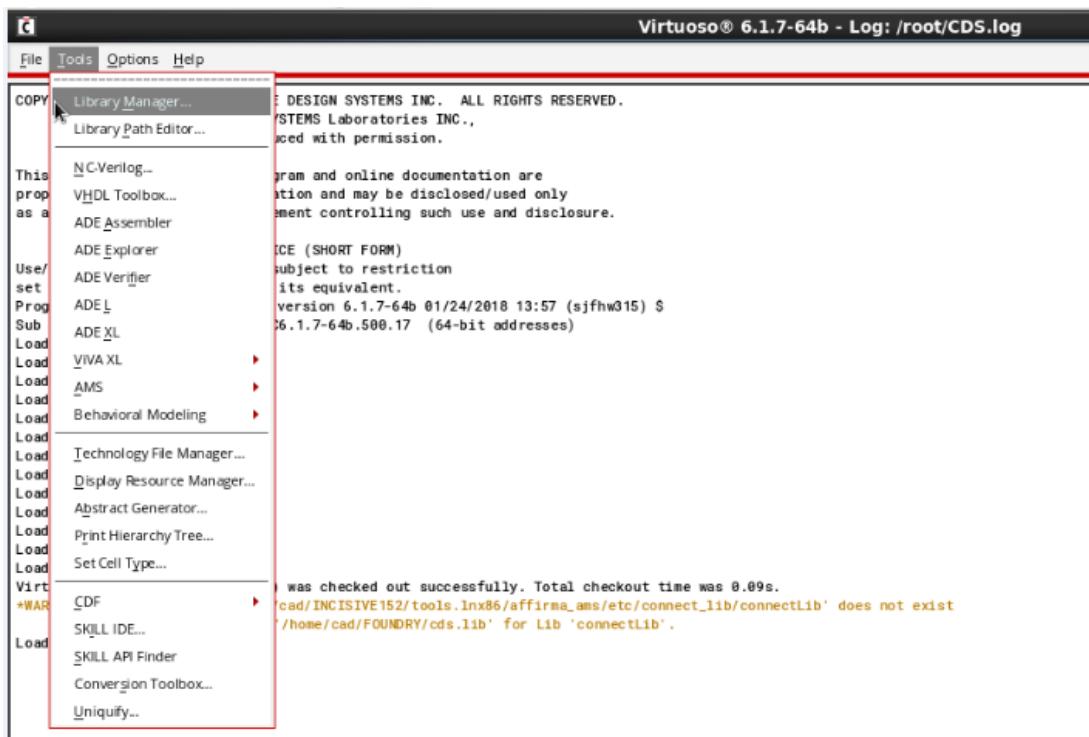


Figure-7(a)

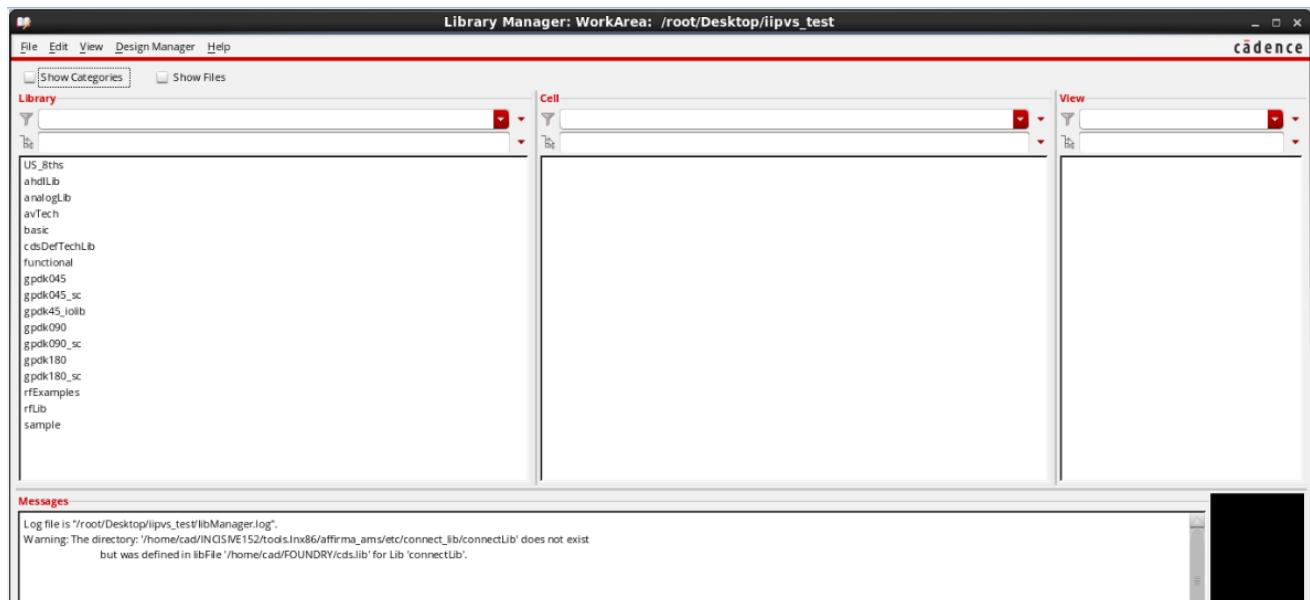
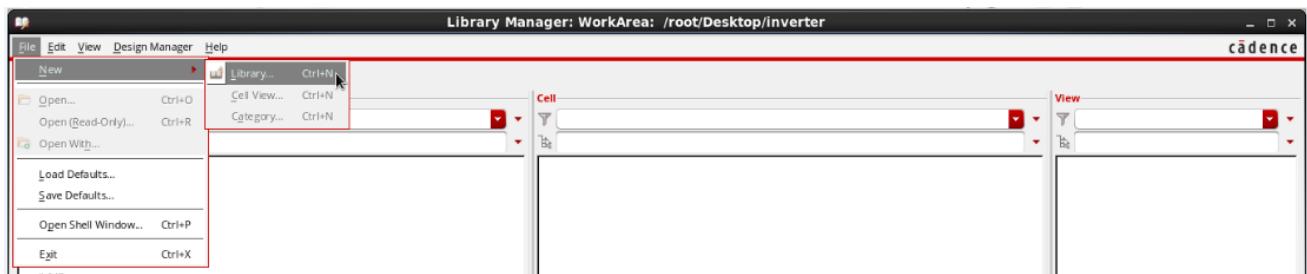


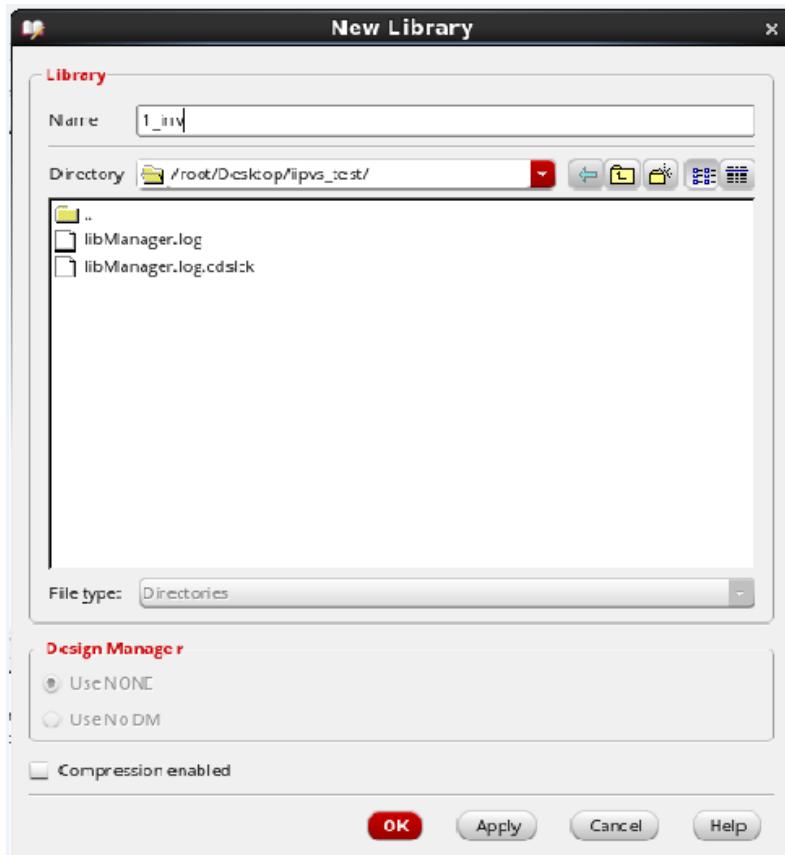
Figure-7(b)

From the top menu of the Library Manager, select “File -> New -> Library” to create a new library for a new design as given in Figure-8.



**Figure-8**

We'll get a “New Library” form where we can name the library that we create as given in Figure-9.



**Figure-9**

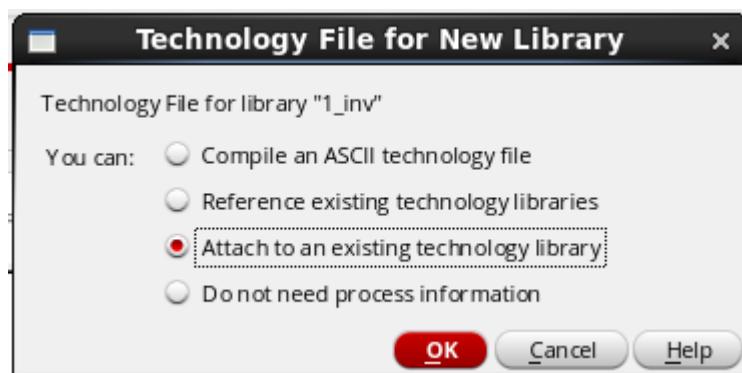
Select “OK” after the library is named.

Select “Technology File..” tab that keeps blinking at the bottom of the screen (Figure-10) to map the created library to a technology node based on the specification.



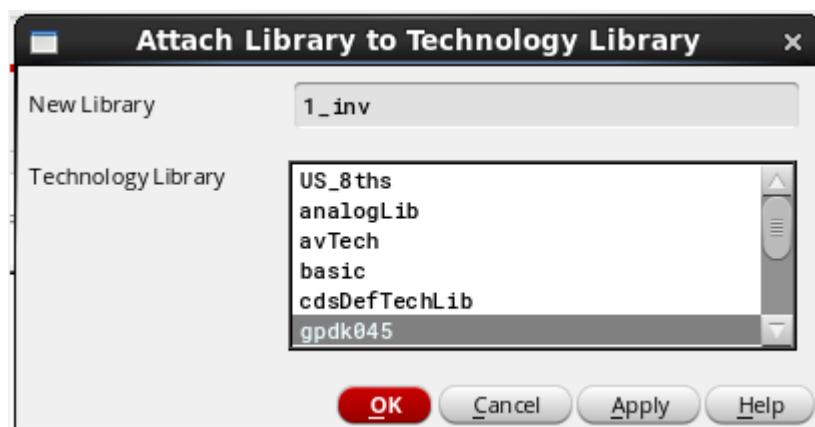
**Figure-10**

We get a form “**Technology File for New Library**”. Select the option “**Attach to an existing technology library**” as given in Figure-11.



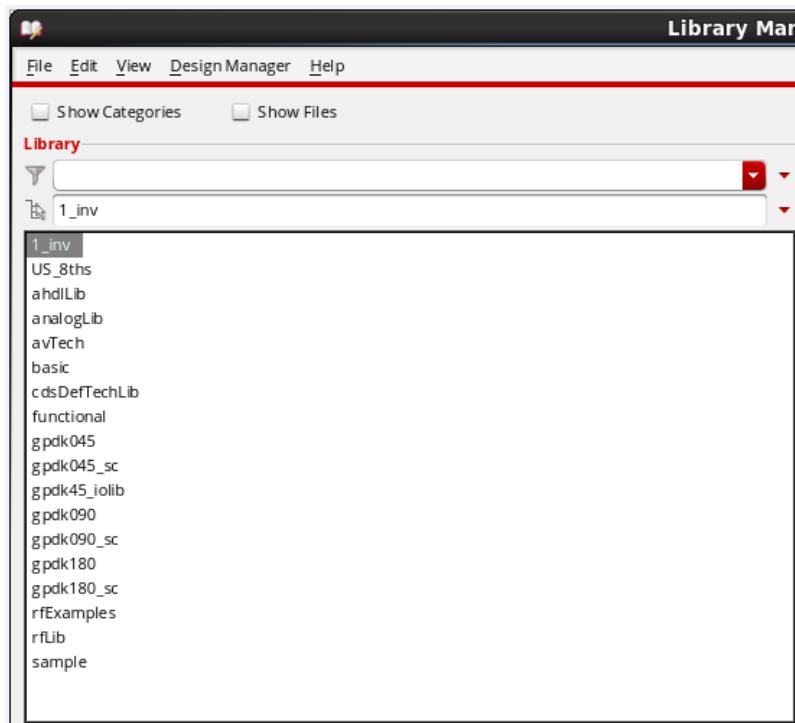
**Figure-11**

Select the respective Technology Node from the list of libraries as given in Figure-12. For example, we have selected “**gpdk045**”.



**Figure-12**

The created library is now available in the Library Manager under Library as given in Figure-13.

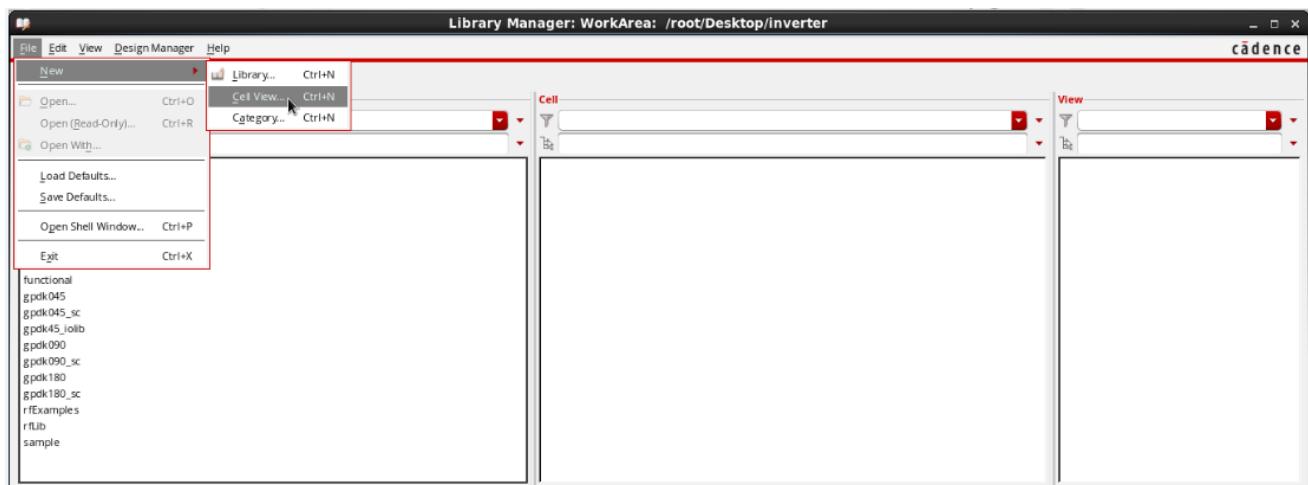


**Figure-13**

### CREATE A CELL:

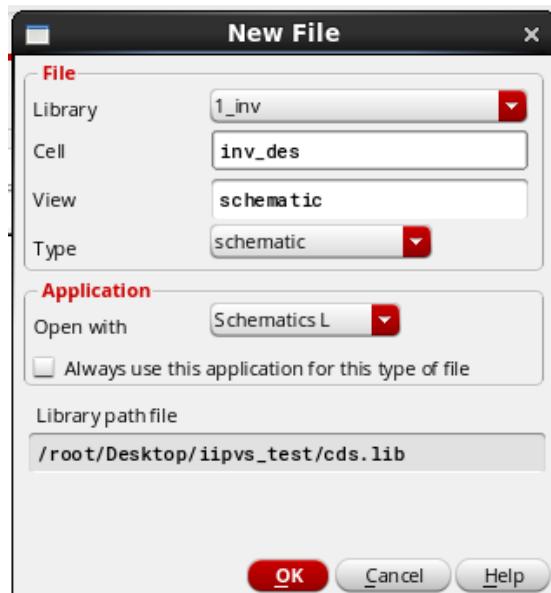
Before creating a cell, make sure that the created library is selected as given in Figure-13. Only then the created cell can be viewed under the respective library.

To create a Cell View, select **File -> New -> Cell View** as in Figure-14.



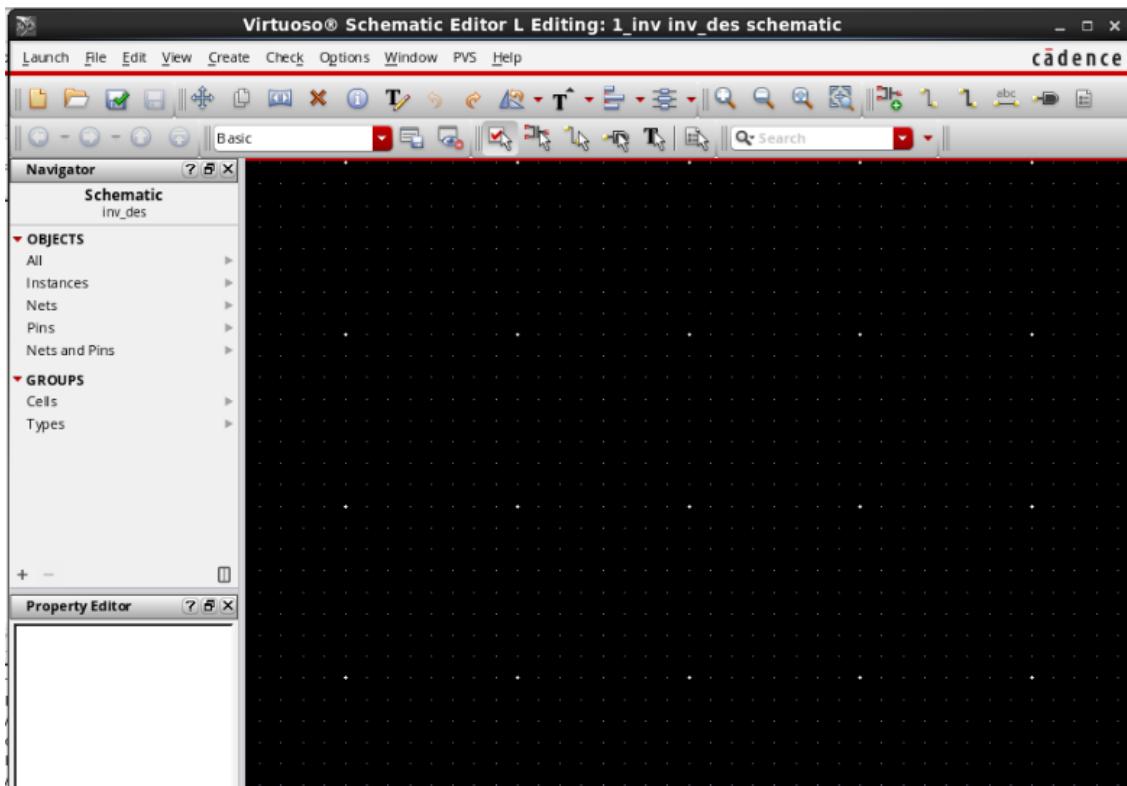
**Figure-14**

Now we get a “**New File**” from as given in Figure-15 and we can name the Cell and check the Library, View and Type of the respective Cell that is to be created.



**Figure-15**

We get the Virtuoso Schematic Editor as in Figure-16.



**Figure-16**

### ADD AN INSTANCE:

To add an instance to the circuit, select “**Create -> Instance**” as in Figure-17. We can also use the bin key ‘I’ or the icon as in Figure-17(a).

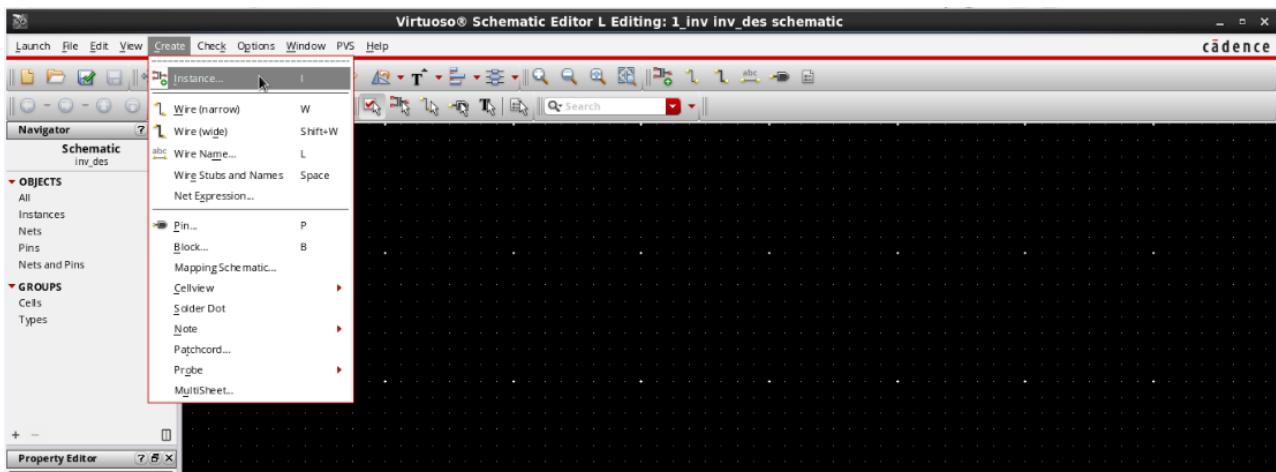


Figure-17



Figure-17(a)

We get the “**Add Instance**” form as given in Figure-18.

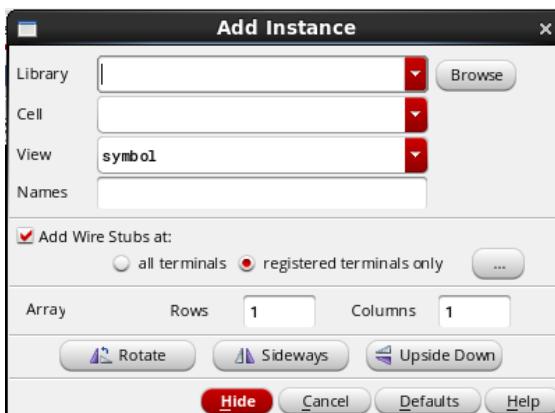
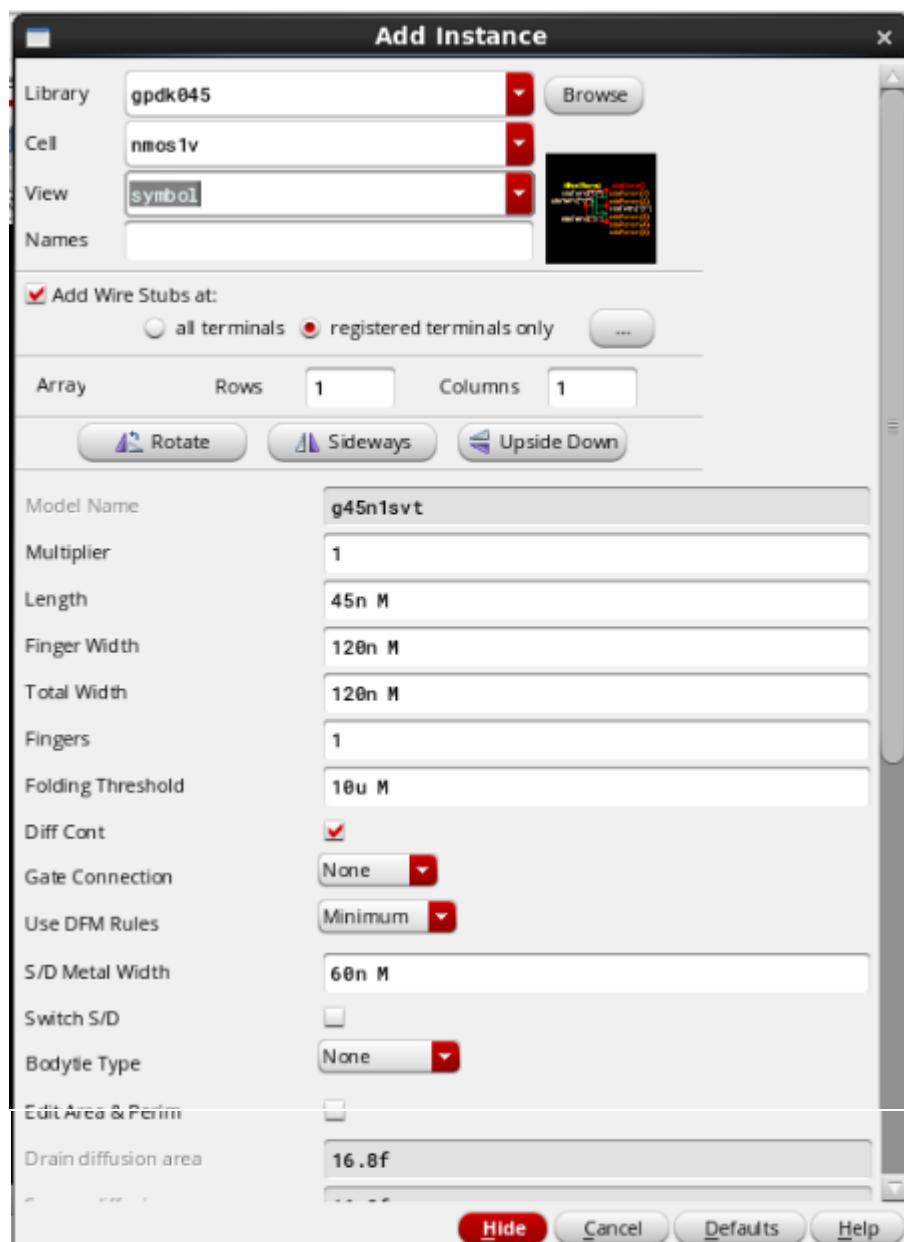


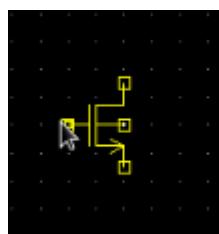
Figure-18

Select “**Browse**” option as seen in Figure-18, we get the “**Library Manager**” to choose the transistors required for the circuit and the type of view for the respective component from the respective Technology Library as selected in Figure-12.

After selecting the component, we get its properties like Length, Width, Multipliers, etc., as in Figure-19. Select “**Hide**” at the end of the form, we can have a view of the transistor in the Schematic Editor as in Figure-20.



**Figure-19**



**Figure-20**

### ADD PIN:

To include pins to the circuit, select “Create -> Pin” as in Figure-21. We get a form as in Figure-22. We can also use the bin key ‘P’ or the icon as in Figure-21(a).

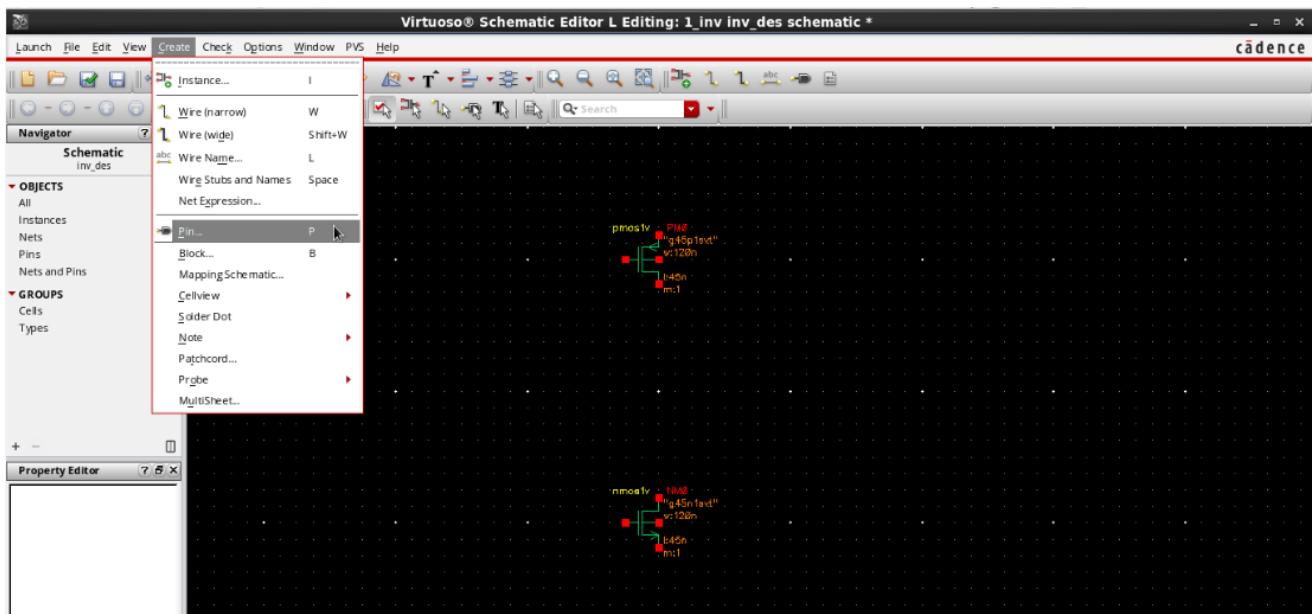


Figure-21



Figure-21(a)

We name the pins and select its direction as in Figure-22(a) and Figure-22(b).

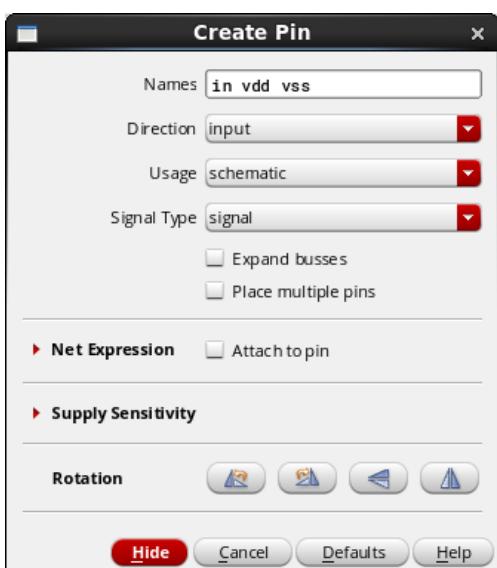


Figure-22(a)

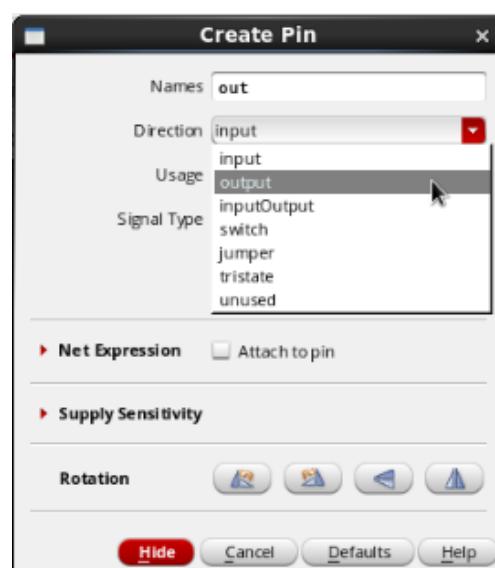


Figure-22(b)

Place the pins by a left click on the mouse and the circuit can be viewed as in Figure-23.

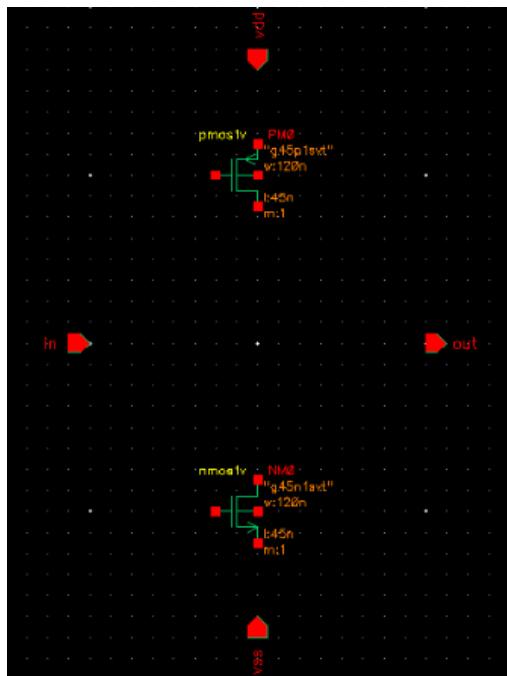


Figure-23

#### ADD WIRE:

Connect the pins and the components with the help of wire. Select “Create -> Wire” as in Figure-24. We can also use the bin key ‘W’ or the icon as in Figure-24(a).

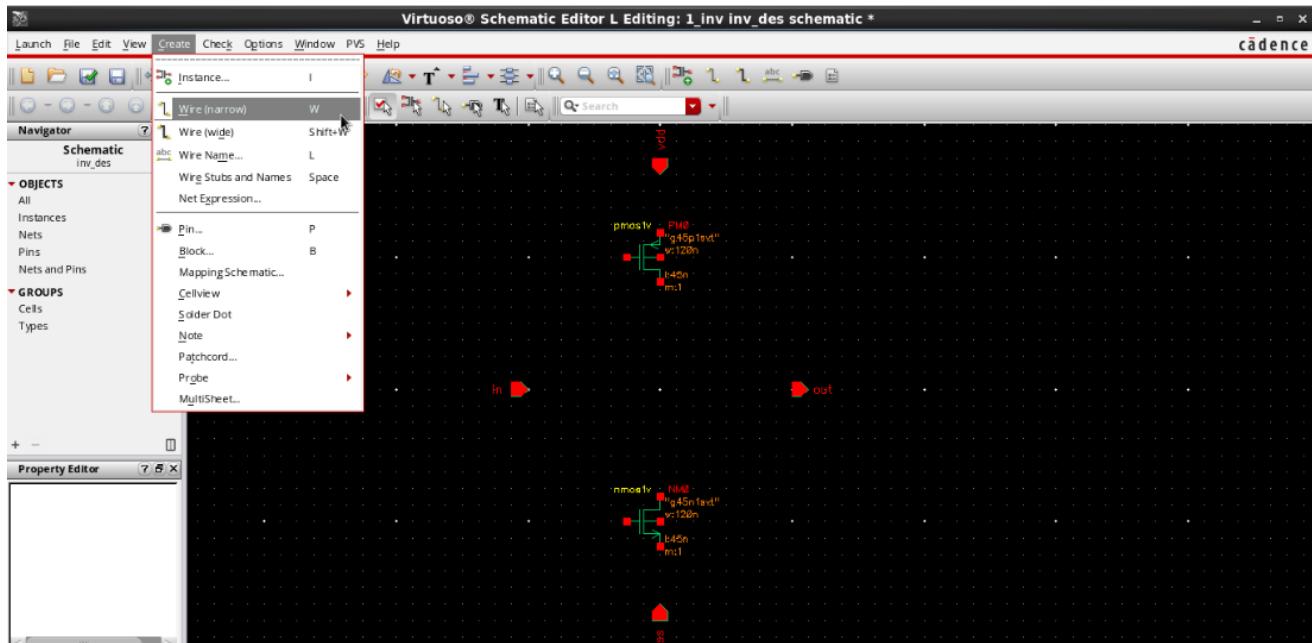


Figure-24



Figure-24(a)

Once wiring is completed, the circuit can be viewed as in Figure-25.

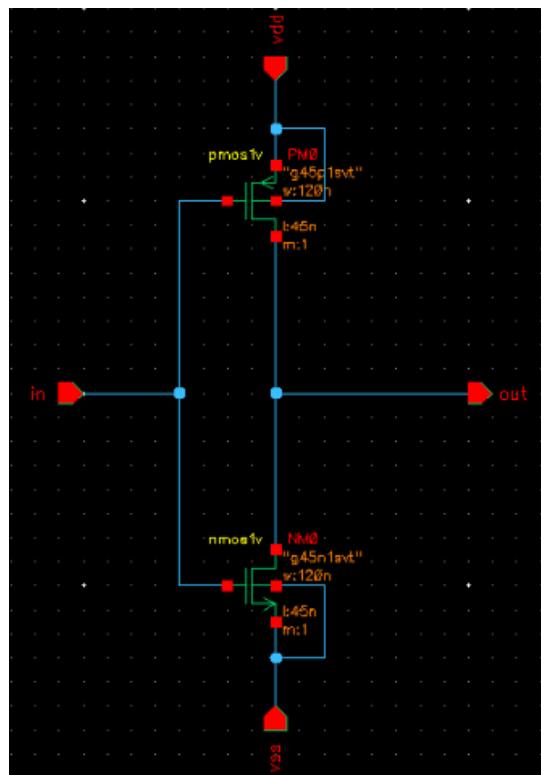


Figure-25

### SAVE THE DESIGN:

After completing the design, it is mandatory to save the design before we move ahead to Simulation. We have two options, “**Save**” and “**Check and Save**” as in Figure-26.



Figure-26

**Save** option saves your design as it is but **Check and Save** option checks for any discontinuities like floating net or terminal, provides the details of errors or warnings in the circuit and then saves the design. The results can be seen in the virtuoso tab as in Figure-27.

```

INFO (SCH-1170): Extracting "inv_des schematic"
INFO (SCH-1426): Schematic check completed with no errors.
INFO (SCH-1181): "1_inv inv_des schematic" saved.

```

Figure-27

### SYMBOL CREATION:

To create a symbol for the circuit, select “Create -> Cellview -> From Cellview” as in Figure-28.

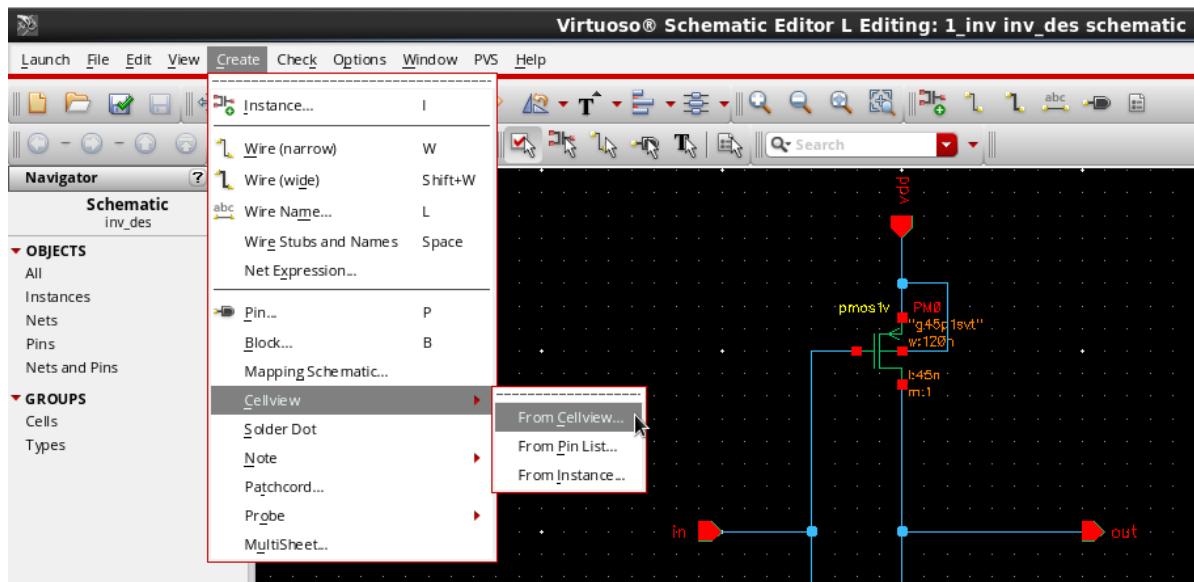


Figure-28

Check the Library Name, Cell Name, From View Name, To View Name, etc., as in Figure-29 and select OK.

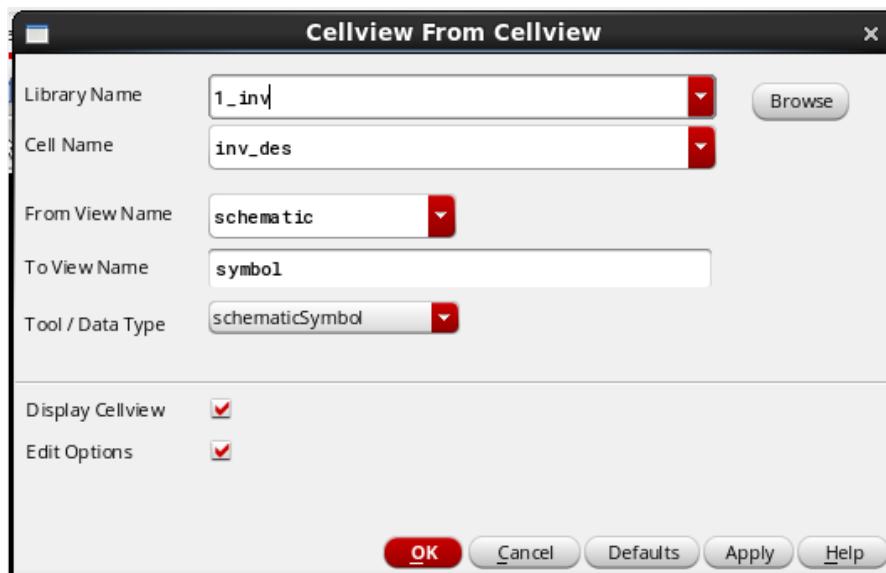
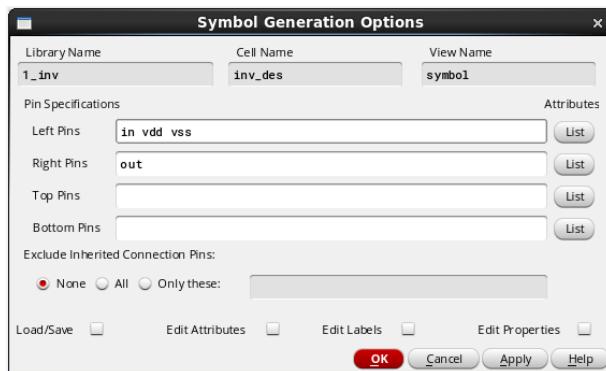


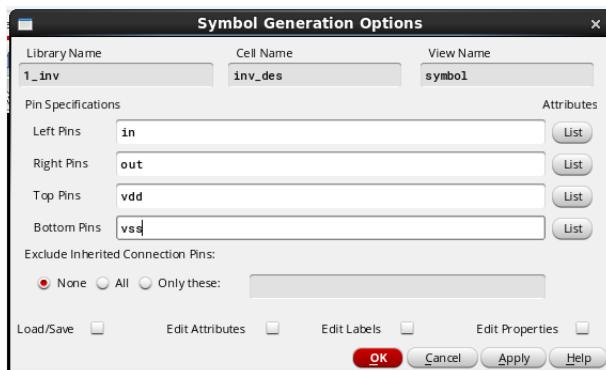
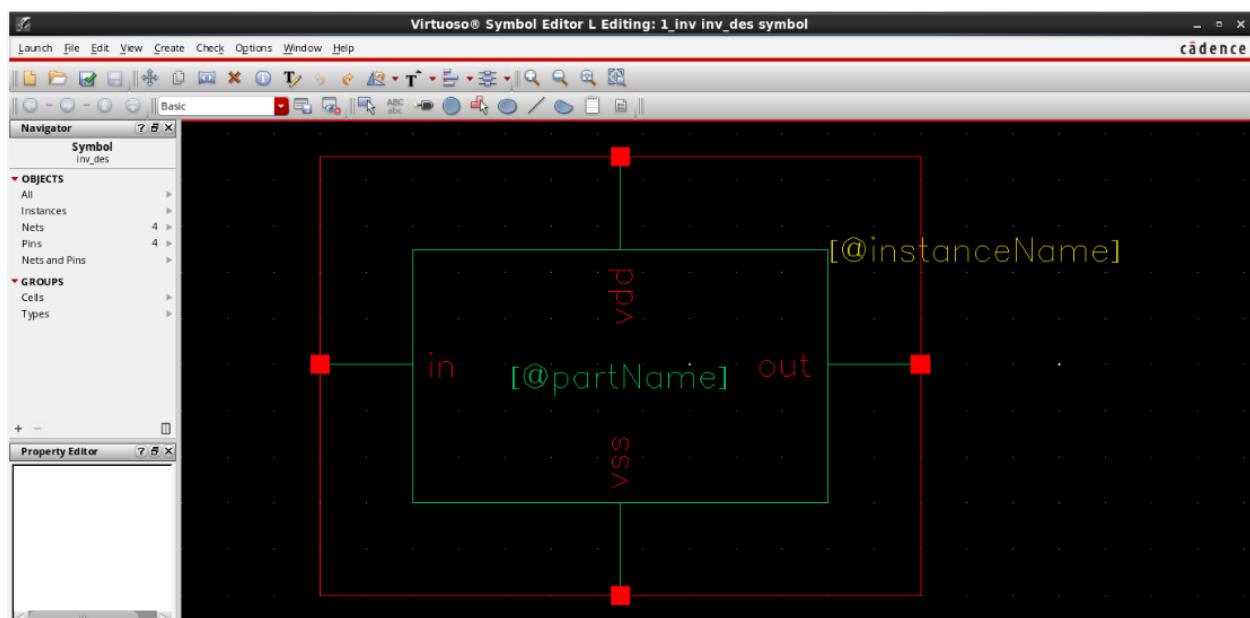
Figure-29

We get the “Symbol Generation Options” window as given in Figure-30. We are free to decide upon the pin locations with options like Left Pins, Right Pins, Top Pins and Bottom Pins.

**Note:** Pin Names are case sensitive.


**Figure-30**

After naming the Left, Right, Top and Bottom Pins as in example shown below (Figure-31), select OK. The tool opens a “**Virtuoso Symbol Editor**” window which shows a temporary view of the symbol based on the pins assigned as given in Figure-32.

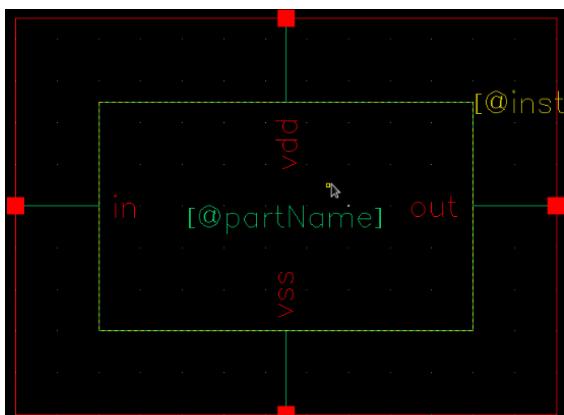

**Figure-31**

**Figure-32**

The symbol shown in Figure-32 can be customized with the help of drawing tools as given in Figure-33.

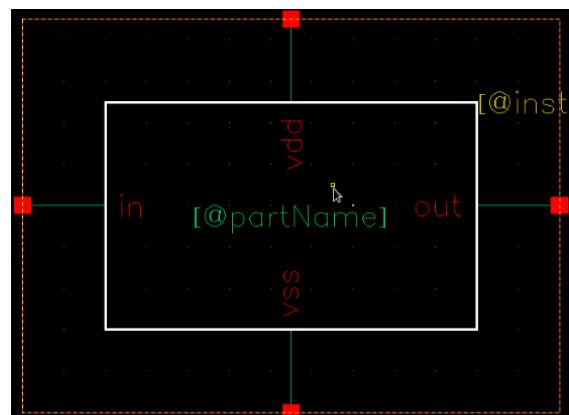


**Figure-33**

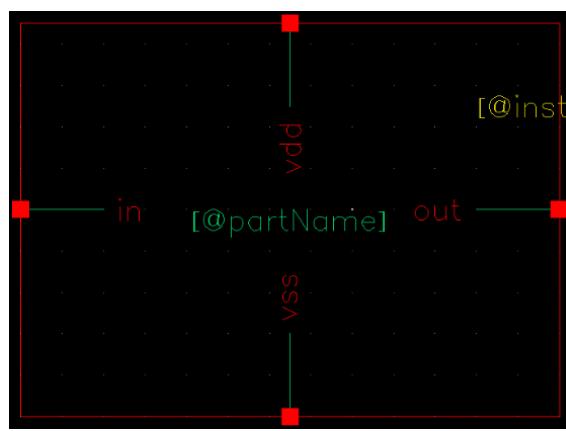
To create custom symbol, remove the inner rectangle (green) and then using drawing tools, custom symbol can be created. To remove the inner rectangle (green), place the mouse pointer within the rectangle so that the entire rectangle gets highlighted as in Figure-34(a), make a left click so that the entire rectangle gets selected as in Figure-34(b) and click on delete in the keyboard to remove the rectangle so that it is removed as in Figure-34(c).



**Figure-34(a)**



**Figure-34(b)**



**Figure-34(c)**

Since Inverter design is taken as an example in this manual, the focus is on creating its symbol. To create a triangle, use “**Create Line**” option as in Figure-35(a) among the drawing tools and the way triangle is created is as similar as how wiring is done in the schematic. To create a bubble, use “**Create Circle**” option as in Figure-35(b), decide a point, make a left click to expand the circle and again make a left click to fix its size as in Figure-35(c).



Figure-35(a)

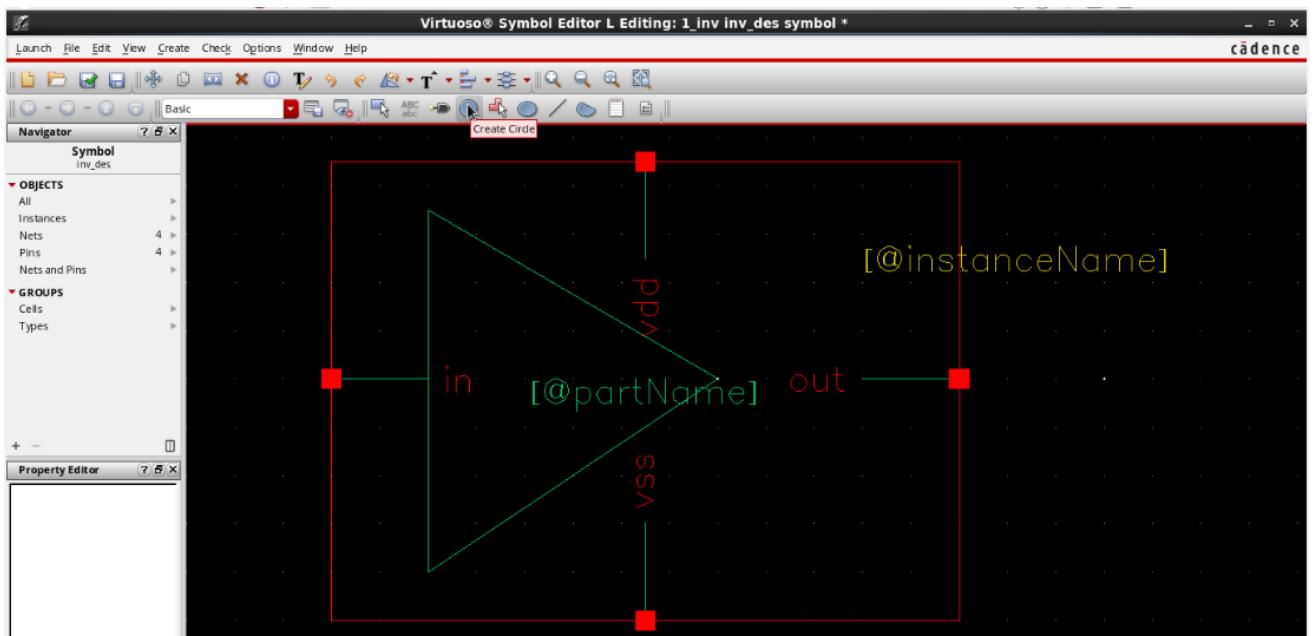


Figure-35(b)

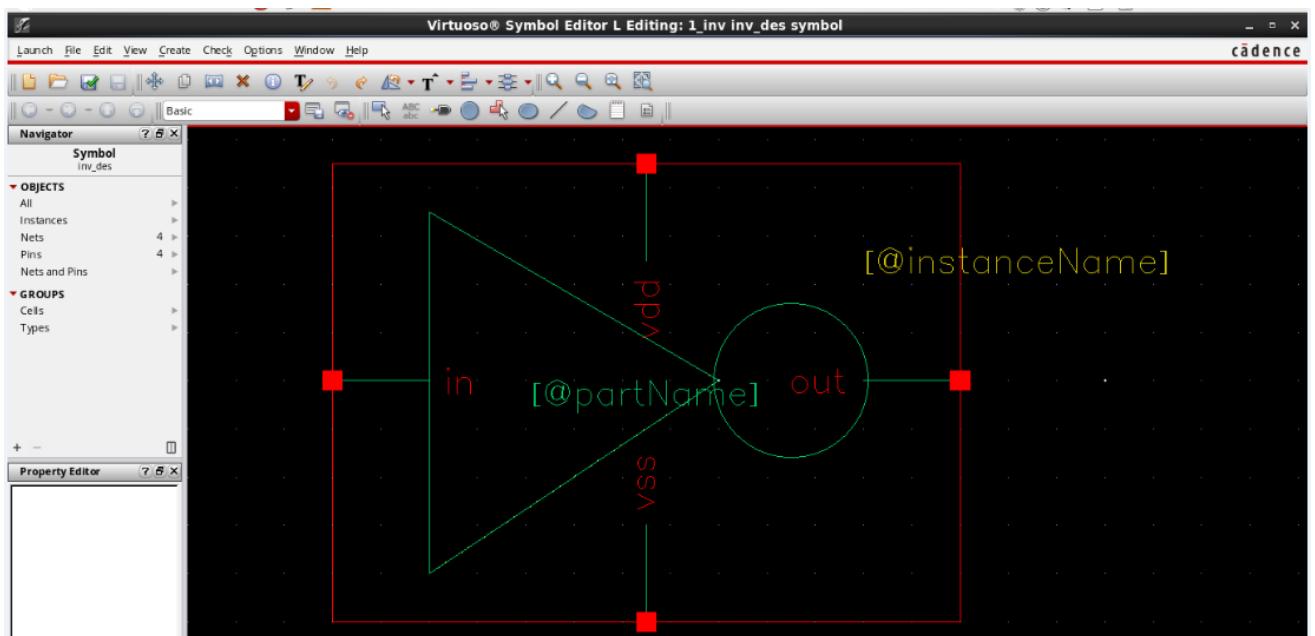


Figure-35(c)

After creating the symbol, save the symbol using the “Check & Save” option as in Figure-26.

### TESTBENCH CIRCUIT FOR SIMULATION:

Instead of using transistor level design, testbench circuit can be created using its symbolic representation. To create a testbench circuit, a new Cellview with a different Cell Name should be created as in Figure-36.



Figure-36

To include the created symbol, use the “Add Instance” option as in Figure-17 & 17(a) and select the respective library and cell as in Figure-37 using the browse option and then the symbol should appear in schematic editor with the mouse pointer.

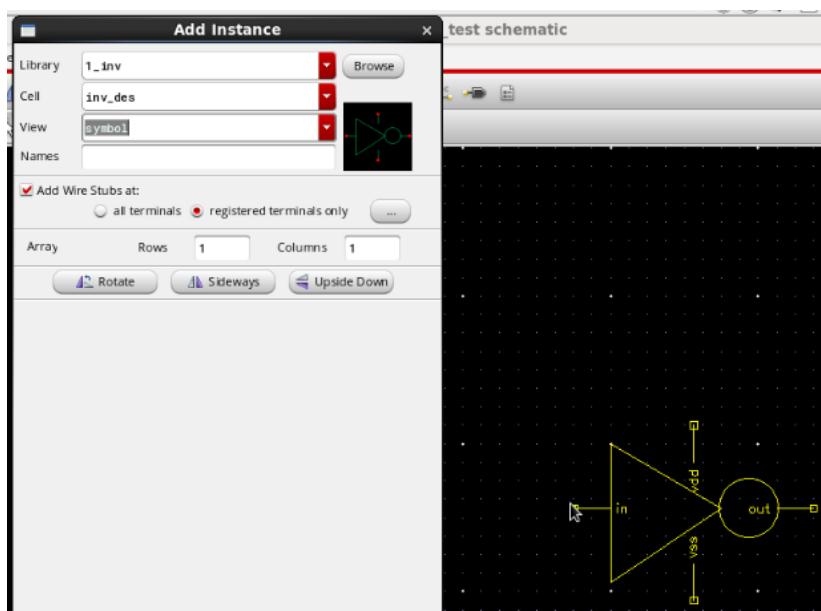
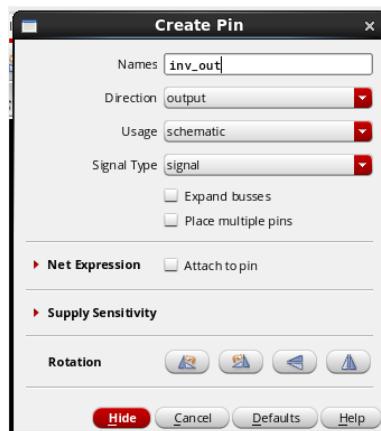
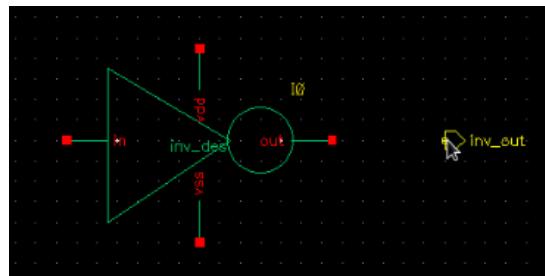


Figure-37

Create an output pin as in Figure-38(a) and 38(b).

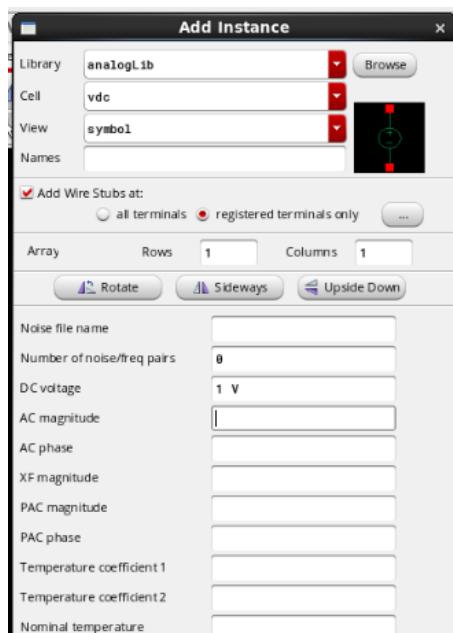


**Figure-38(a)**



**Figure-38(b)**

To include supply voltage and input signal sources, “**Add Instance**” option shall be used. Browse to the “**analogLib**” library, select the Cell as “**vdc**”, View as “**symbol**” and click on “**Tab**” key in the keyboard to get the device properties as in Figure-39.



**Figure-39**

Mention the appropriate “**DC voltage**” based on the specification or technology node. Similarly, for an input source, (for example) “**vpulse**” is considered and parameters like Voltage 1, Voltage 2, Period, Delay time, Rise time, Fall time and Pulse width are mentioned as in Figure-40.

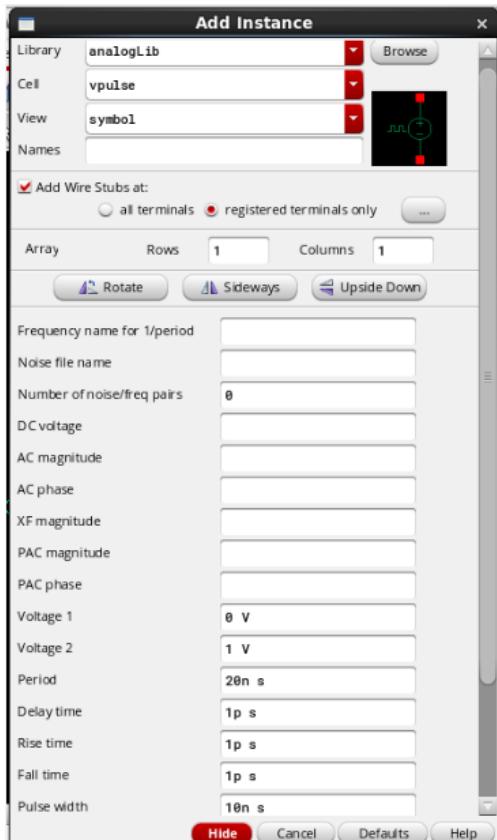


Figure-40

Similarly, “**gnd**” terminal shall be included to the circuit as in Figure-41 and the complete circuit is given in Figure-42.

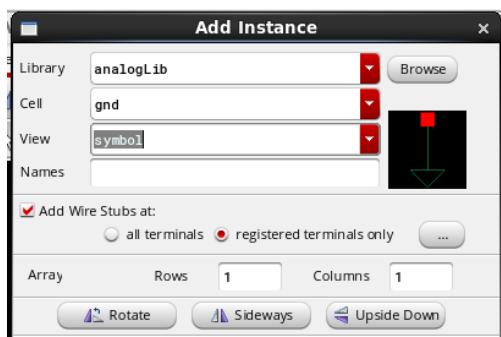


Figure-41

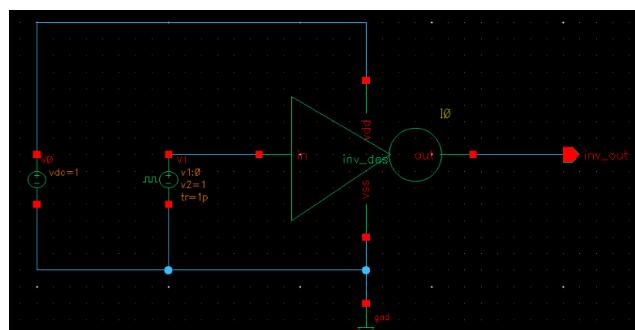


Figure-42

## FUNCTIONAL SIMULATION:

To simulate the design, Launch “ADE L” as in Figure-43(a).

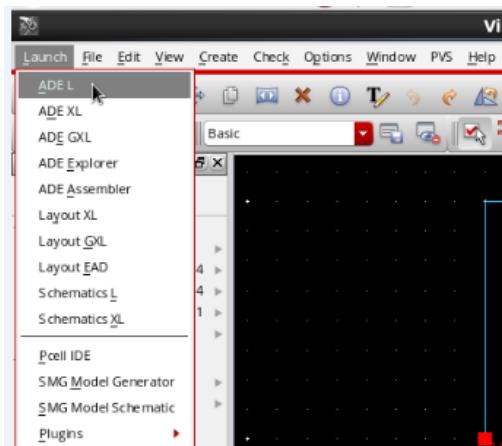


Figure-43(a)

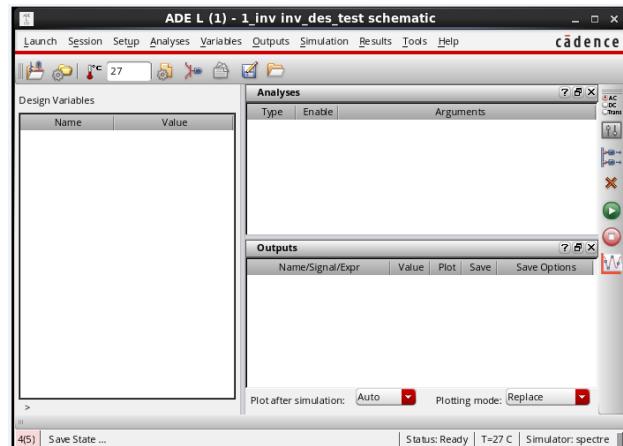


Figure-43(b)

We get a window as in Figure-43(b) and following options are to be verified:

- (1) **Simulator** – to make sure that **Spectre** is the simulator selected [Figure-44(a) & 44(b)]

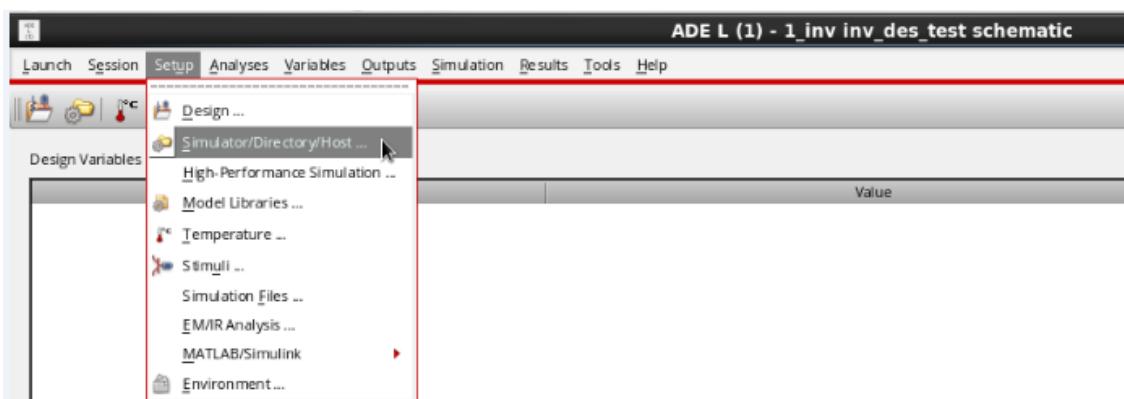


Figure-44(a)

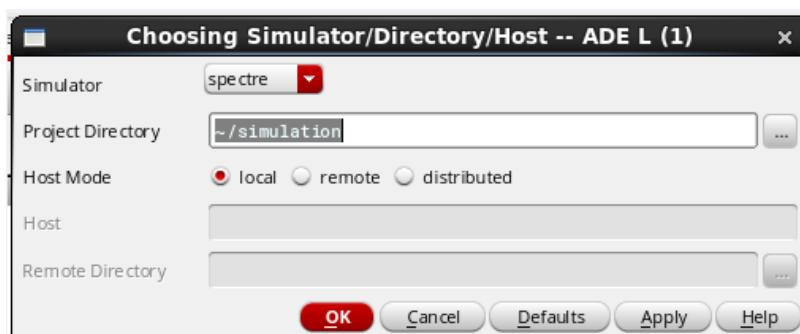
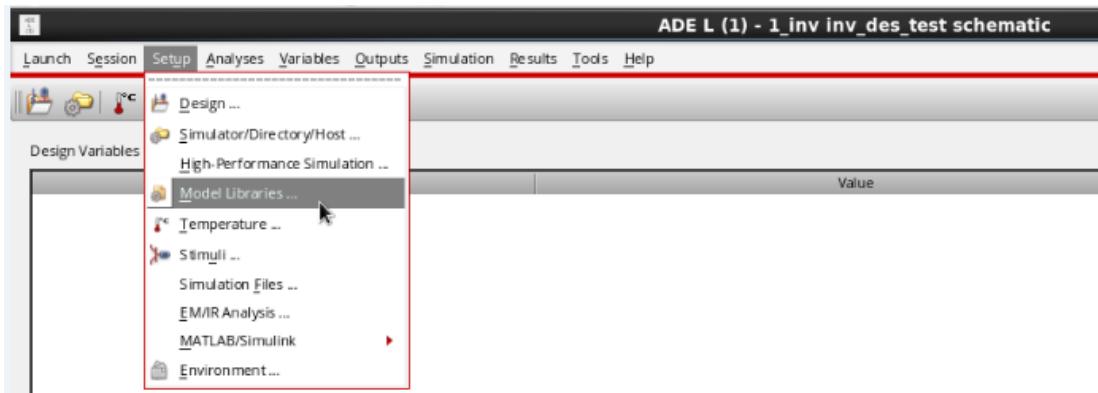
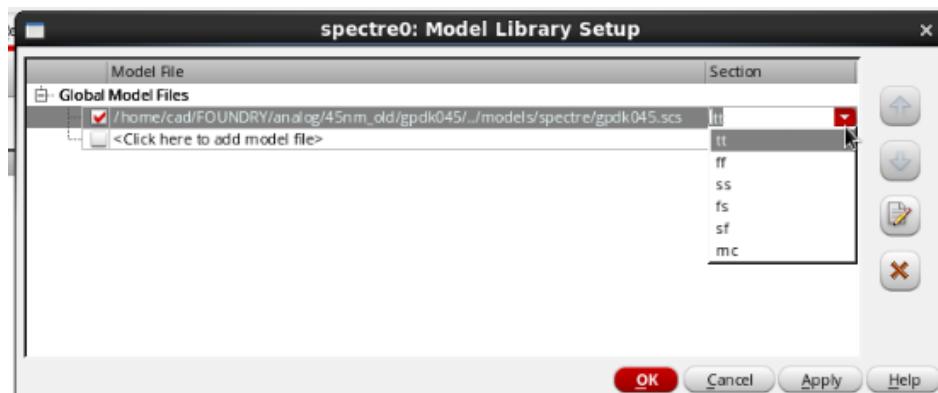


Figure-44(b)

(2) **Model Libraries & Process Corners** – to make sure that “.scs” file of the respective technology node has been selected [Figure-45(a) & 45(b)]

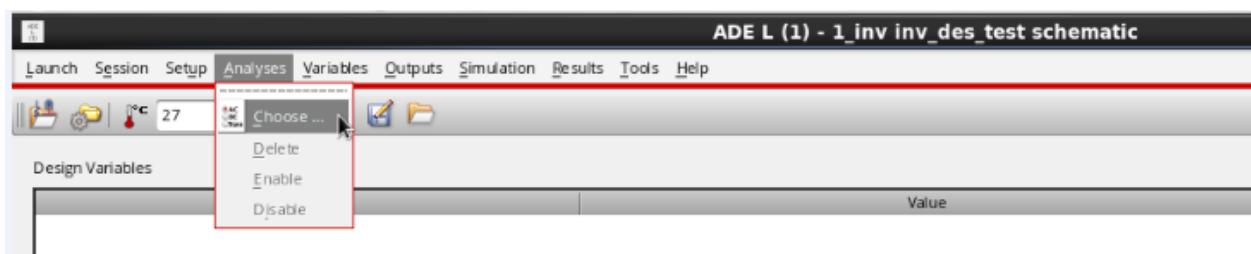


**Figure-45(a)**



**Figure-45(b)**

To analyze the circuit, select “**Analyses**” from the top menu in ADE L and under Analyses, select “**Choose**” as in Figure-46.



**Figure-46**

To set up a “**Transient Analysis**”, select “**tran**” under “**Analysis**” as in Figure-47(a), mention the “**Stop Time**” and “**Accuracy Defaults**” as in Figure-47(b) and select “**OK**”.

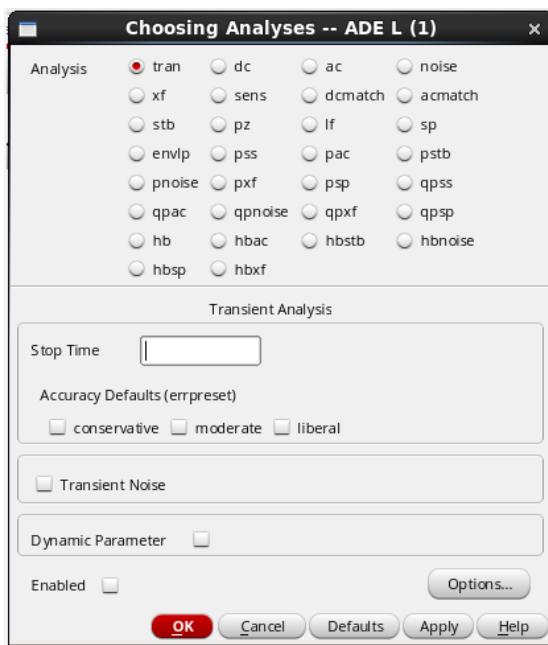


Figure-47(a)



Figure-47(b)

The analyses chosen and the arguments that had been set up can be seen under “Analyses” tab in the ADE L window as in Figure-47(c). Similarly, rest of the analyses can be performed based on designer’s demands.



Figure-47(c)

To setup the simulation, select “Outputs” from the ADE L window and select “Setup” under Outputs option as in Figure-48.

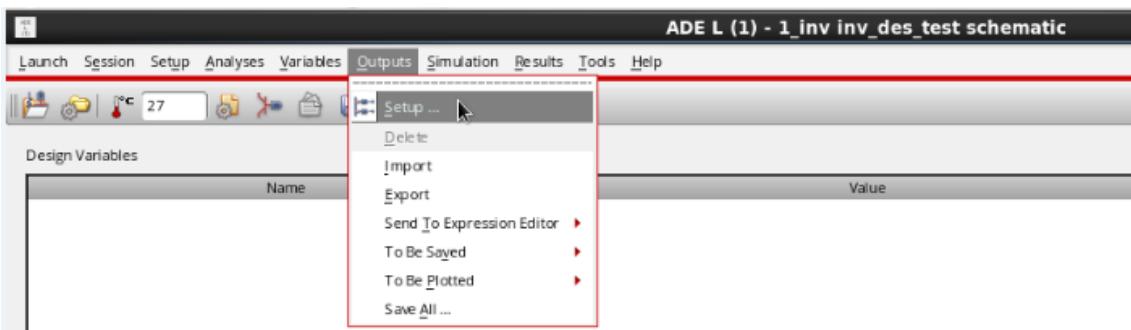
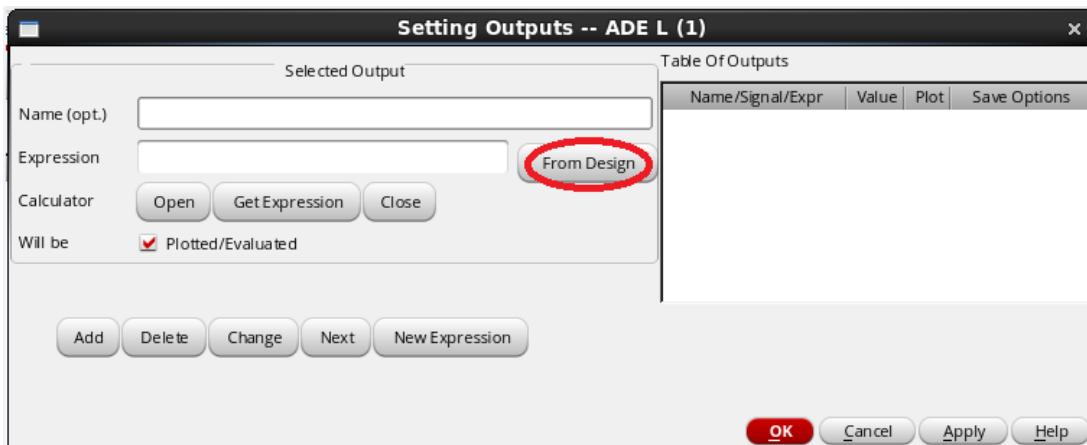


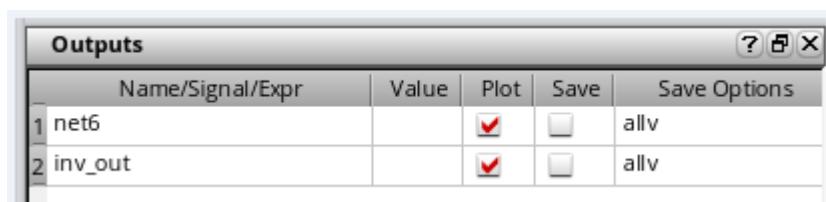
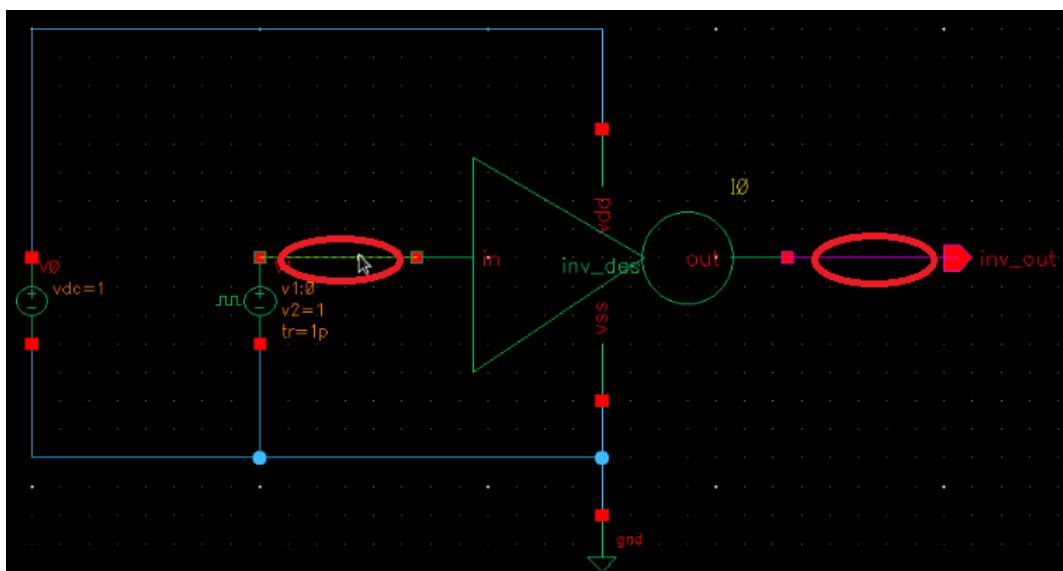
Figure-48

We get a “Setting Outputs” window as in Figure-49, select “From Design” which would bring back the testbench circuit created for the simulation process.



**Figure-49**

Select the input wire and output wire and in ADE L, they are supposed to be displayed under “Outputs” option as in Figure-50.



**Figure-50**

To run the simulation, select “**Simulation**” from ADE L and select the option “**Netlist and Run**” as in Figure-51. The design is simulated and waveforms are seen as in Figure-52.

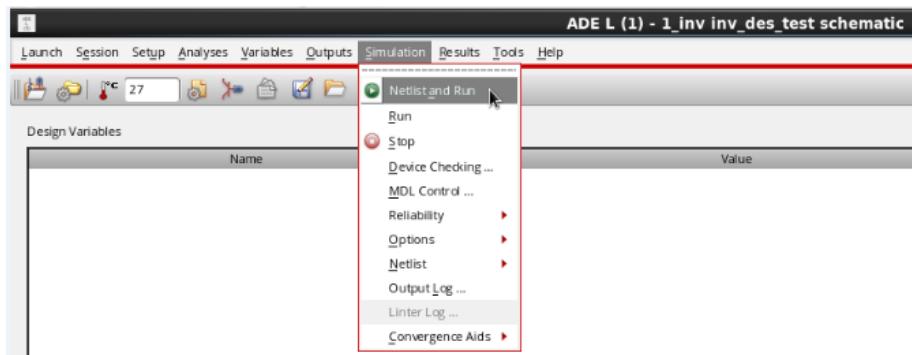


Figure-51

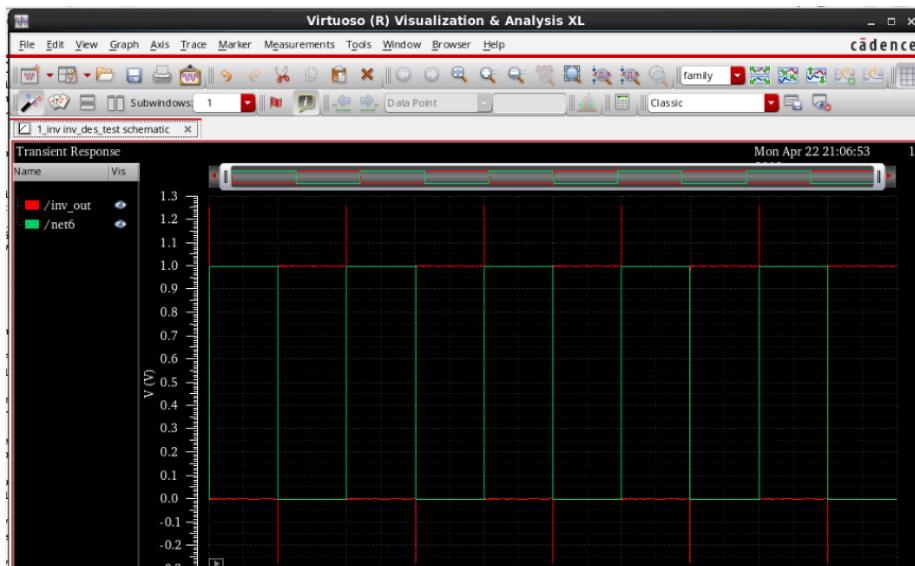


Figure-52

Input signals and Output signals can be seen separately by selecting “Graph -> Split All Strips” as in Figure-53.

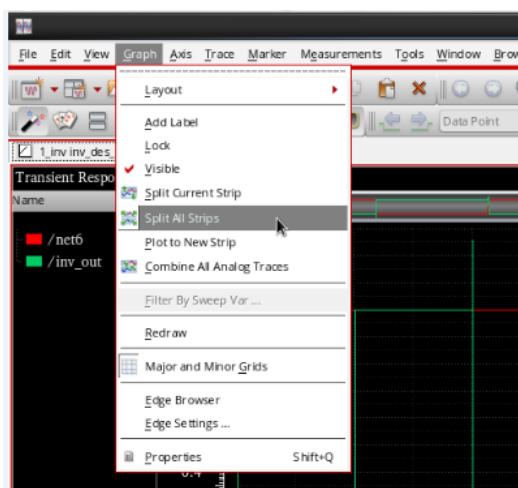


Figure-53

To save the simulation state, select “Session” under ADE L, select “Save State” as in Figure-54, we get a “Saving State” window as in Figure-55. Select “Cellview” and select “OK” to save the state.

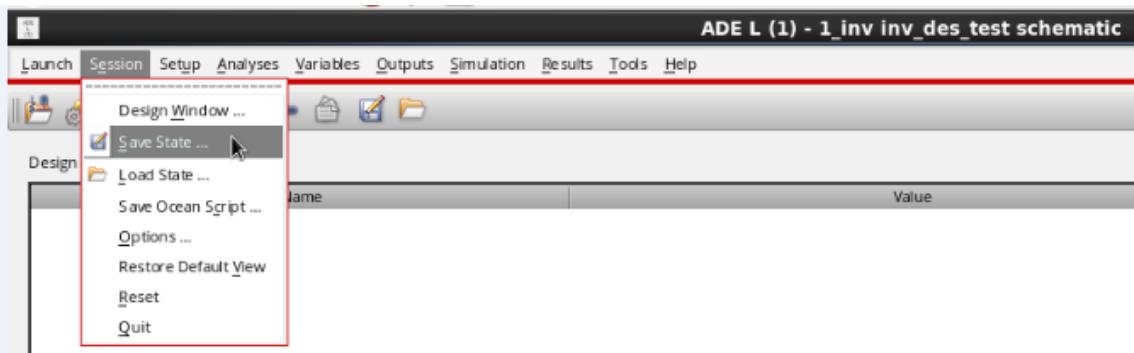


Figure-54

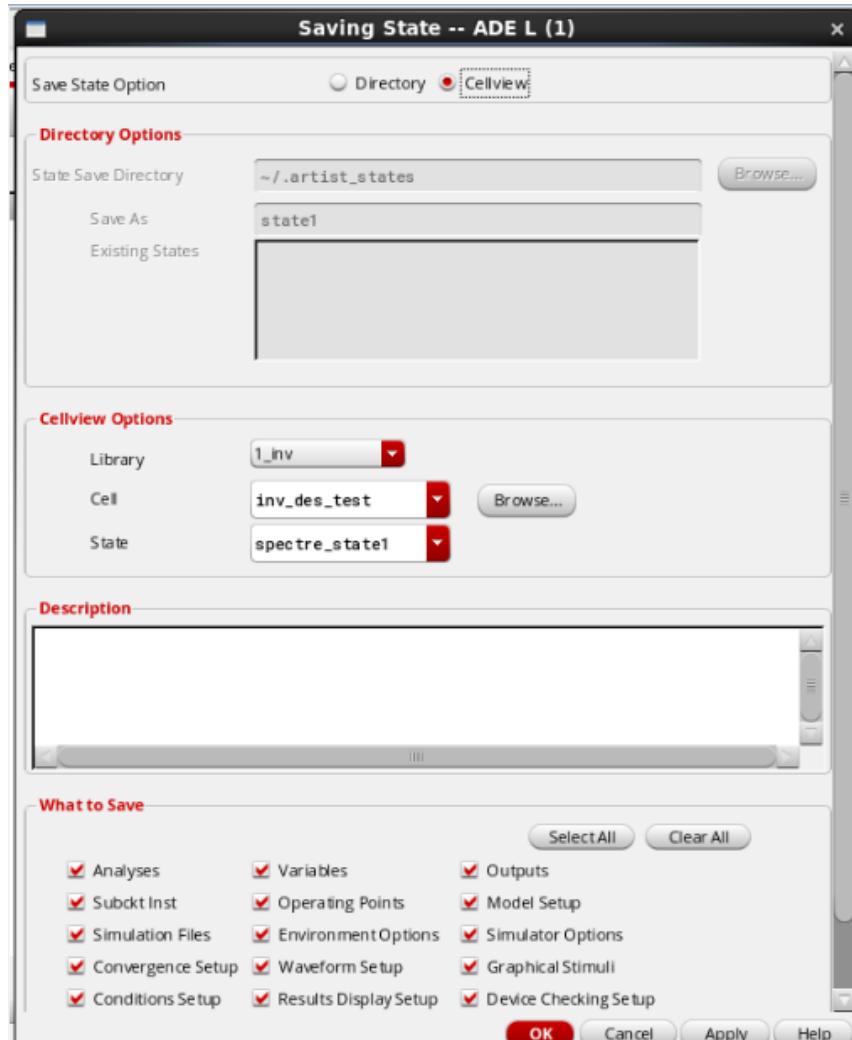


Figure-55

The simulation state and testbench circuit are viewed as in Figure-56.

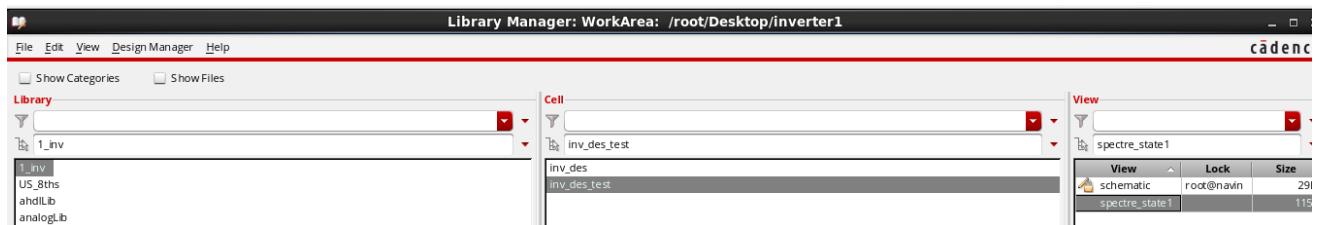


Figure-56

### LAYOUT:

Open the schematic as in Figure-25 through the Library Manager and select “Launch -> Layout XL” as in Figure-57.

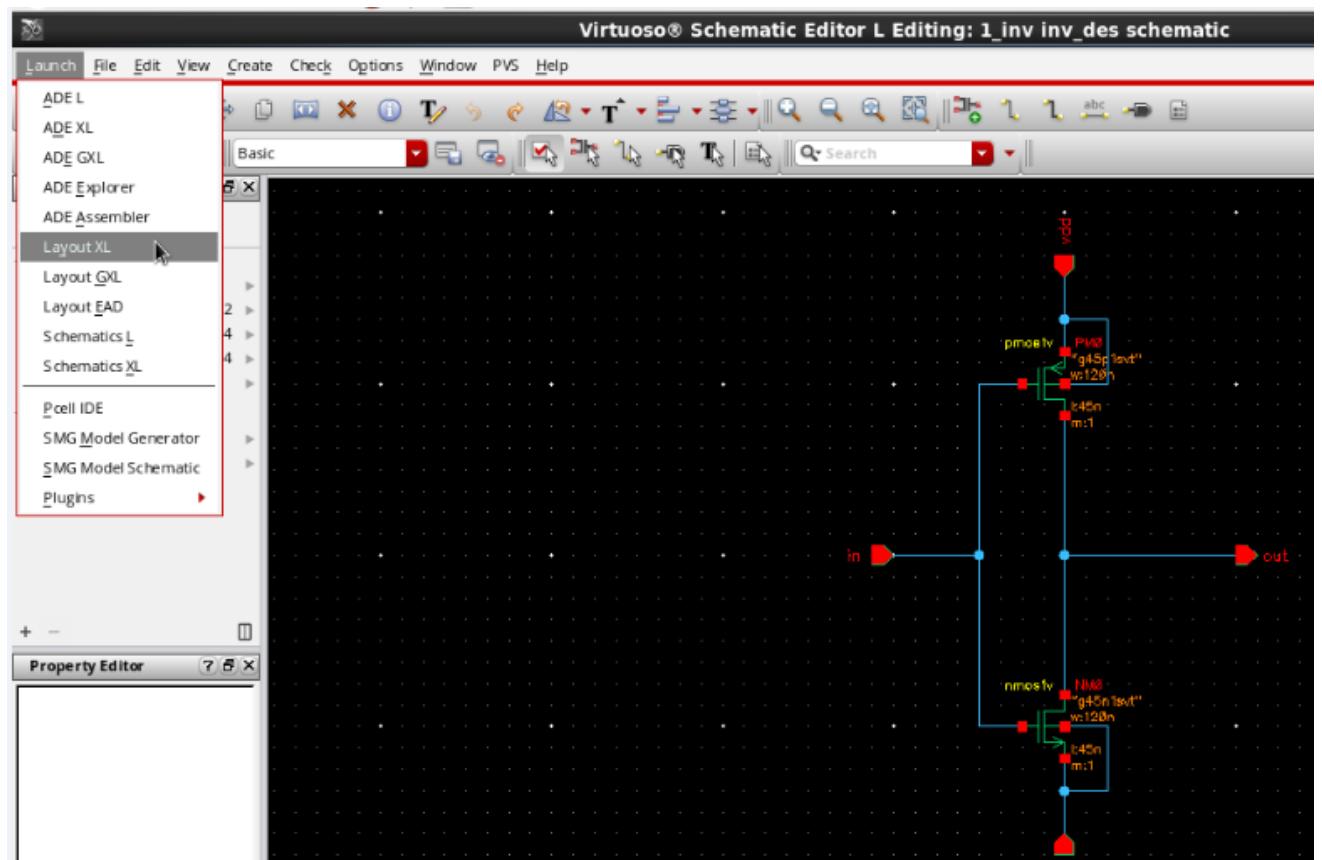


Figure-57

A “Startup Option” window pops up as in Figure-58. Select “Create New” under Layout tab, “Automatic” under Configuration tab and select OK.



Figure-58

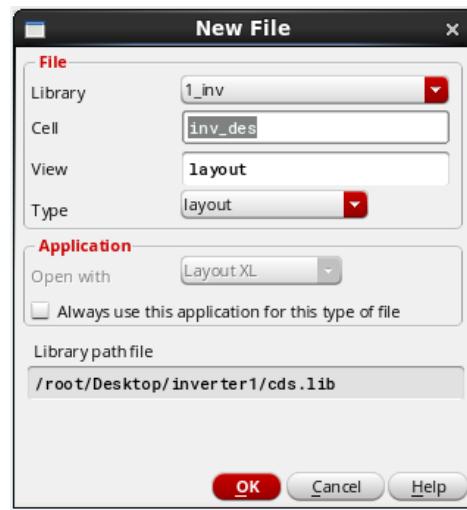


Figure-59

A “New File” window pops up as in Figure-59. No changes are to be made, so select OK. Virtuoso Layout Suite XL Editing window can be seen as in Figure-60.

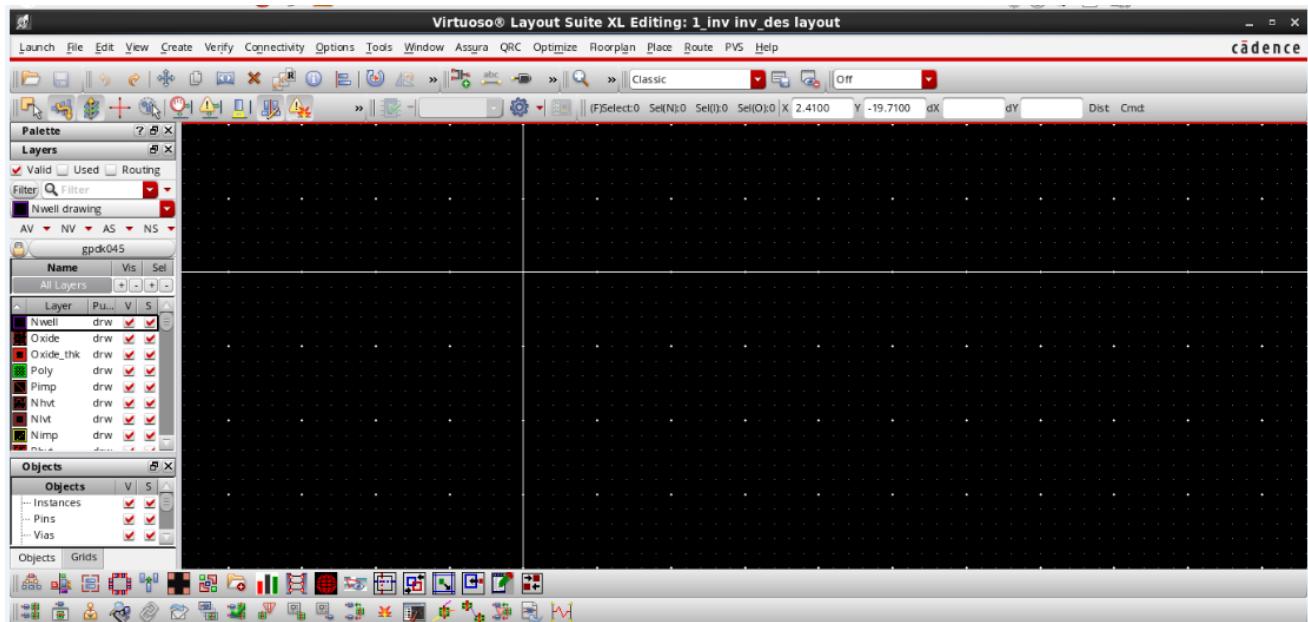
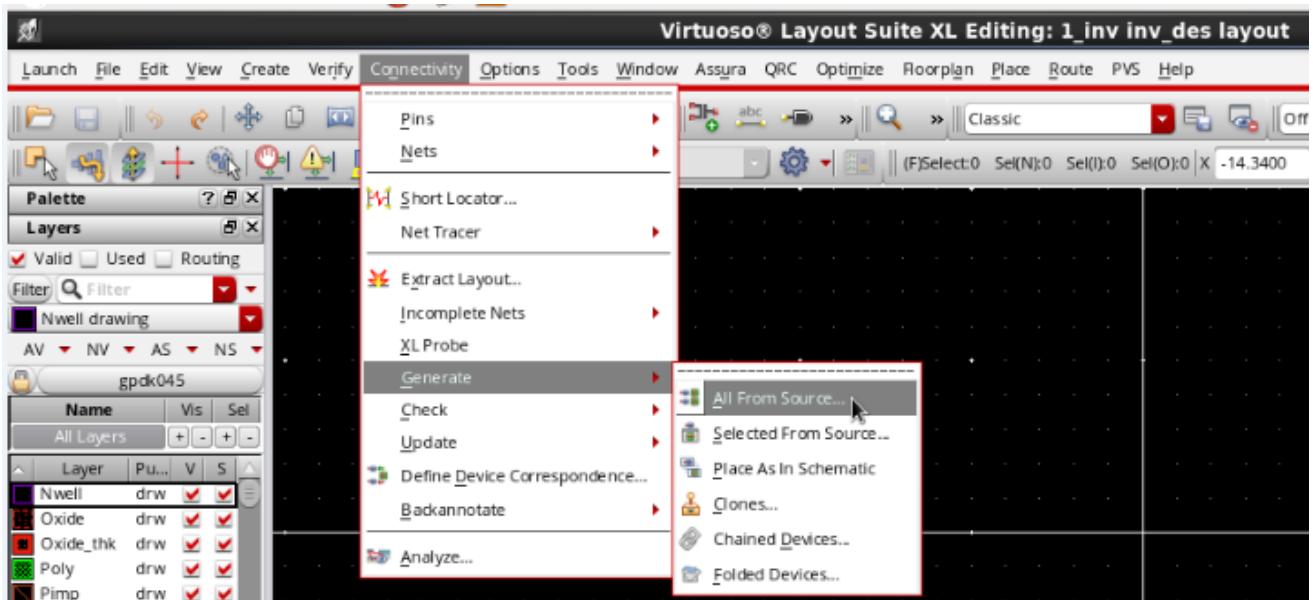


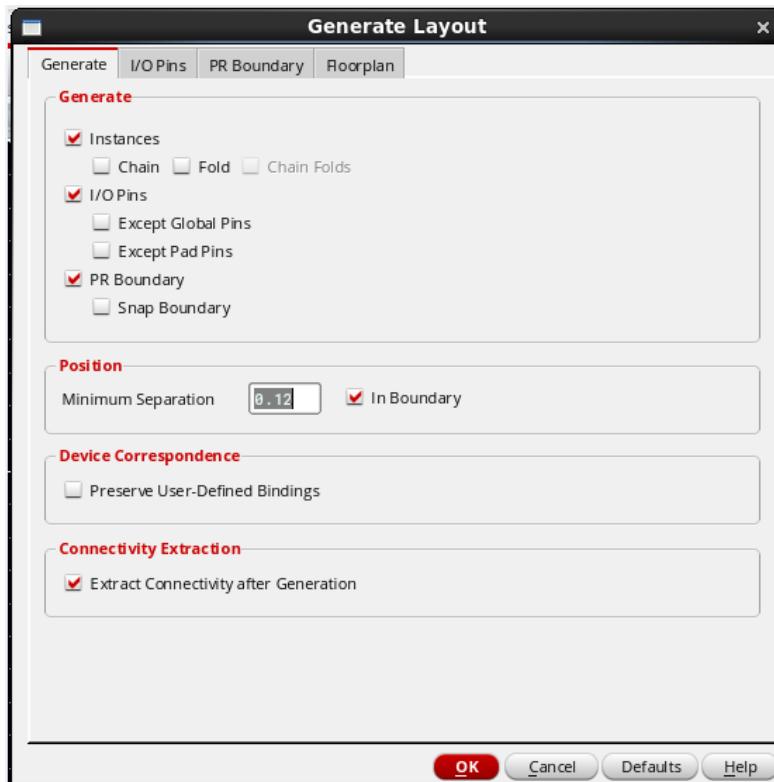
Figure-60

To import the circuit components, select “**Connectivity -> Generate -> All From Source**” as in Figure-61.



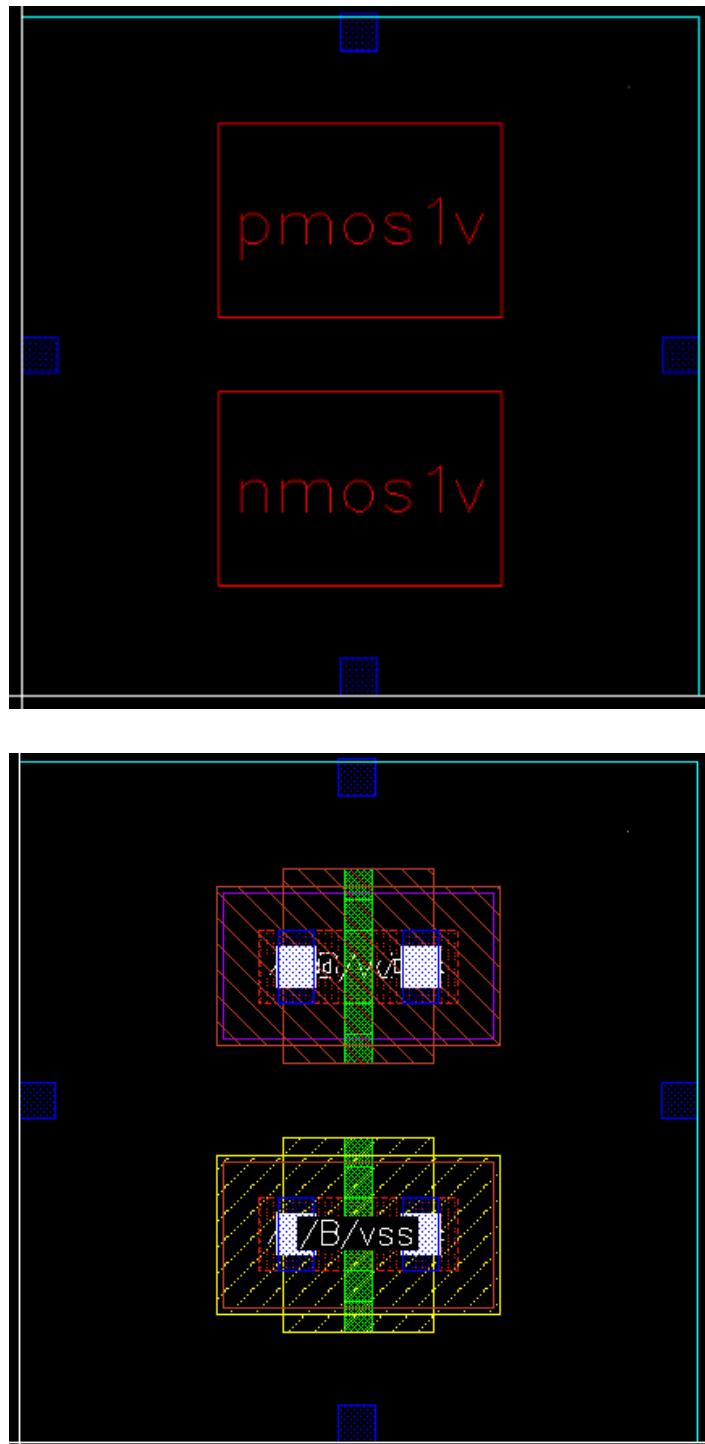
**Figure-61**

Select OK in the “Generate Layout” window as in Figure-62, and the components of the circuit can be seen as in Figure-63.



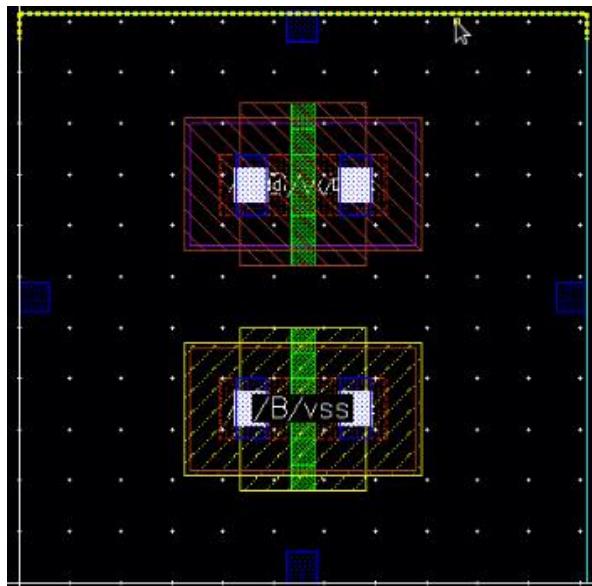
**Figure-63**

Select “Shift + F” to have a view of all the terminals of the transistors as in Figure-64.



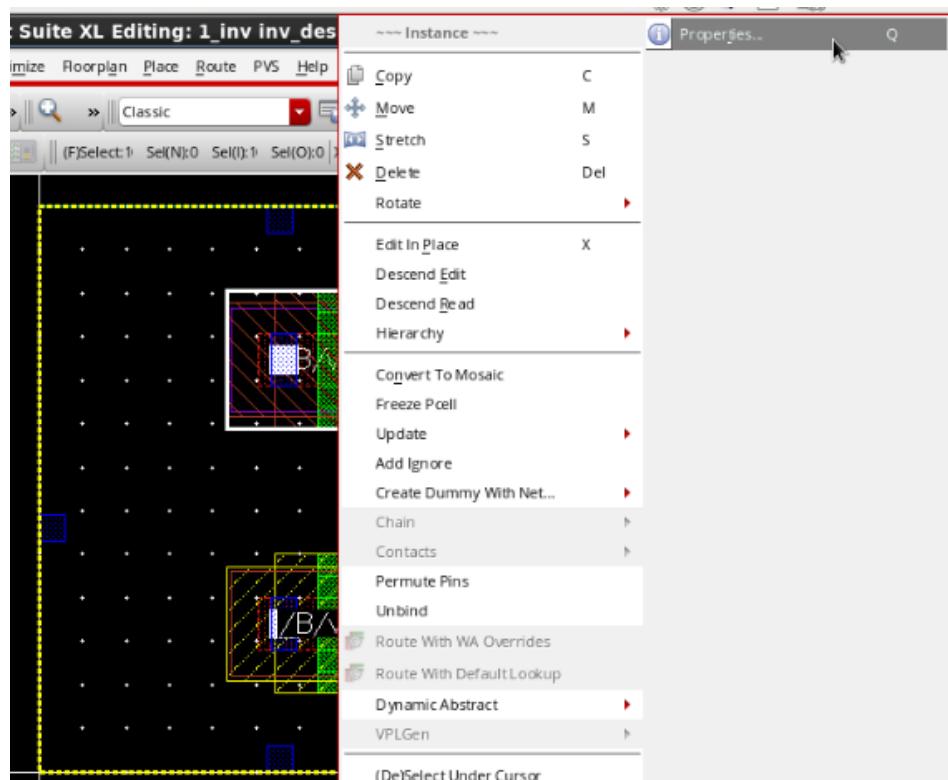
**Figure-64**

The blue colored box surrounding the circuit components is the **PR (Placement & Routing) Boundary**. PR-Boundary can be shifted using the shortcut “S”. To shift the PR-Boundary, place the mouse pointer close to the respective boundary so that it gets highlighted as in Figure-65, make a left mouse click to select the boundary, use the mouse or arrow (up, down, left or right) keys to shift the boundary.

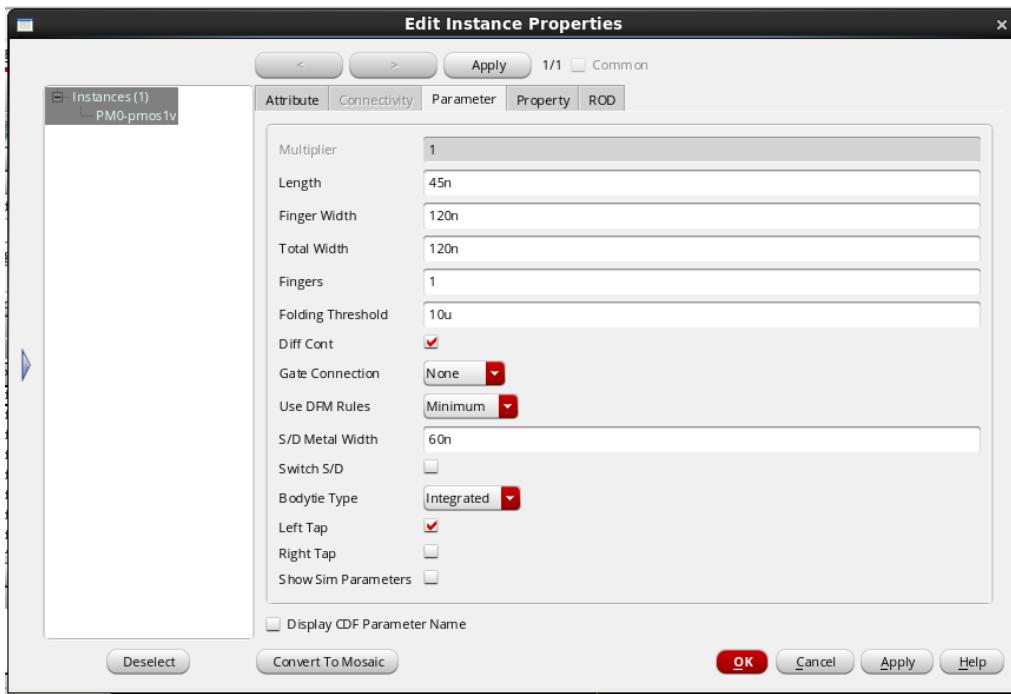


**Figure-65**

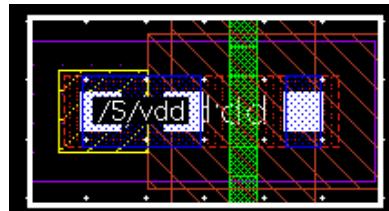
To attach “**Bulk**” terminal to the transistors, select the particular transistor by a left mouse click , make a right mouse click and select “**Properties**” as in Figure-66(a), select “**Parameter -> Bodytie Type -> Integrated (or) Detached -> Left Tap (or) Right Tap**” as in Figure-66(b) and select OK. Bulk terminal of that transistor can be seen as in Figure-66(c). Repeat the above steps for rest of the transistors to include the Bulk terminal.



**Figure-66(a)**

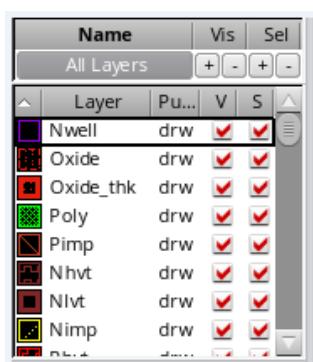


**Figure-66(b)**



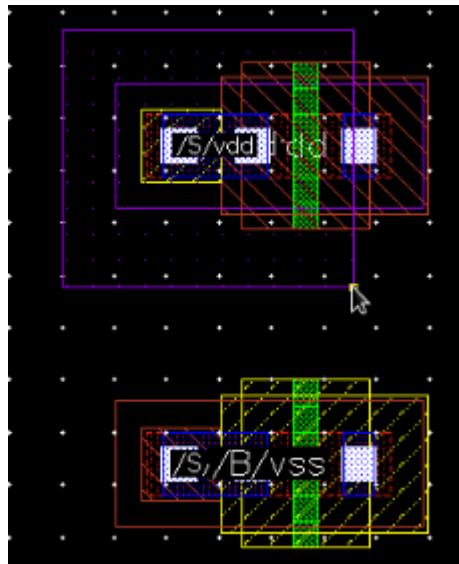
**Figure-66(c)**

By default, the background available in the Virtuoso Layout Editor is the P-Substrate. So, the PMOS transistors should be placed within an N-Well. This is mandatory for PMOS transistors in gdk090 and gdk045, but for PMOS transistors in gdk180, it has an N-Well by default. To create an N-Well, select the respective layer from the “**Layers**” tab on the left-hand side of the Virtuoso Layout Editor as in Figure-67.



**Figure-67**

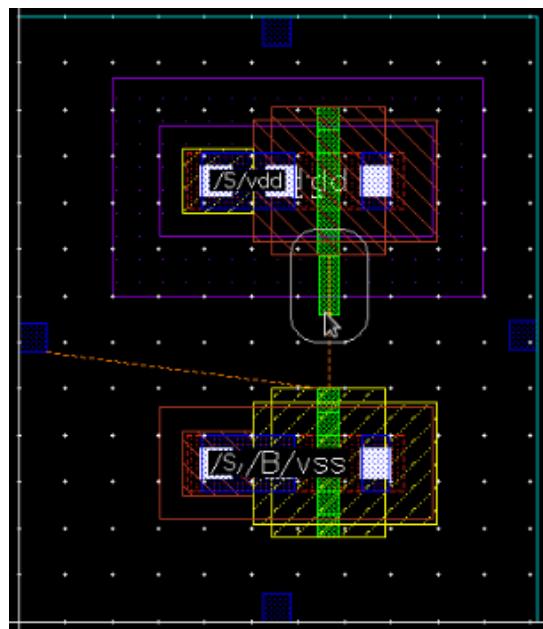
Select “R” to create N-Well in the shape of a rectangle surrounding the PMOS transistor as in Figure-68.



**Figure-68**

The PMOS transistor is placed within the N-Well as in Figure-69 and to complete routing between the components, we can use “P” which denotes “Path” in the layout and is meant for routing process.

When the mouse pointer is taken closer to any of the terminals of the components, the terminal gets highlighted with a yellow color bold line, make a left click to start the path segment from one terminal to another as in Figure-69.



**Figure-69**

For routing between two different layers, usage of “**Via**” is mandatory. There are two options to place a via. Start routing from the layer of interest, make a right-click, select “**Via Down To ..**” and select the layer of interest as in Figure-70(a) (or) select “**Create**” from the top menu, select “**Via**”, select the respective via under “**Via Definition**”, make a left mouse click to place the via as in Figure-70(b) & 70(c).

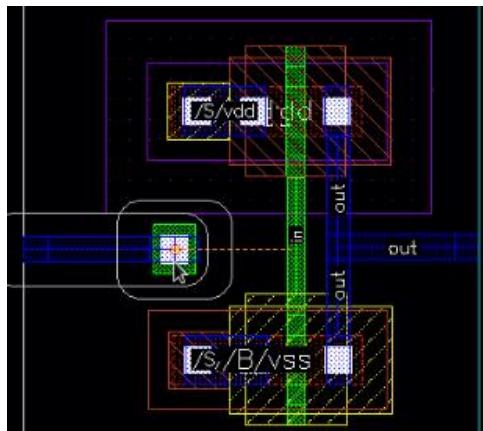
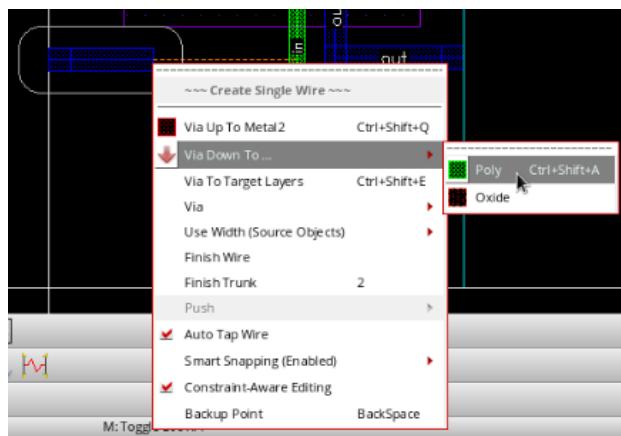


Figure-70(a)

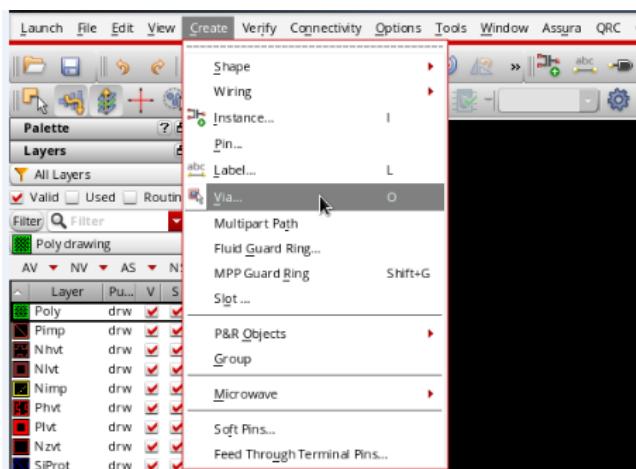


Figure-70(b)



Figure-70(c)

For the example used here, “**VDD**” is at the top and “**VSS**” is at the bottom. Source & Bulk of PMOS/NMOS can be routed to VDD/VSS respectively as earlier between other pins and terminals (or) the entire top layer can be used for VDD and bottom layer for VSS using “**Pin Placement**” option.

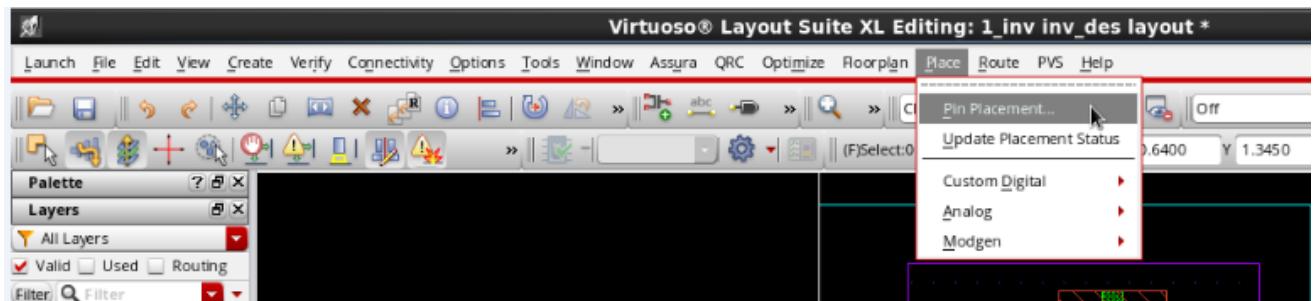


Figure-71

Select “**Place -> Pin Placement**” as in Figure-71, a window pops up as in Figure-72. Under “**Pin Planner**” tab, “**Pin Name, Attributes & Create**” options can be seen. Select “**VDD**” under “**Pin Name**”, select “**Top**” under “**Attributes -> Edge**”, select “**HRail**” under “**Create**” and select “**Apply**” under “**Attributes**” to place VDD at the top layer. Similarly, select “**VSS**” under “**Pin Name**”, select “**Bottom**” under “**Attributes -> Edge**”, select “**HRail**” under “**Create**” and select “**Apply**” under “**Attributes**” to place VSS at the bottom layer as in Figure-73. After routing the terminals of PMOS/NMOS terminals with VDD/VSS respectively, save the layout.



Figure-72

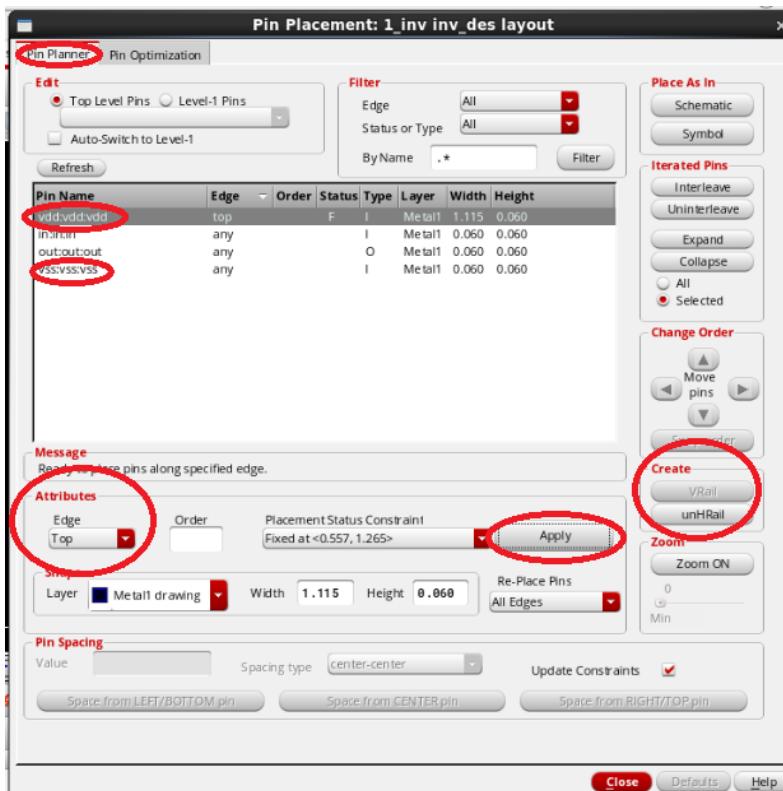


Figure-73

### PHYSICAL VERIFICATION:

The tool used for Physical Verification is Assura where DRC, LVS of a design are verified and Parasitics of the design are extracted using QRC for technology nodes like gpdk180, gpdk090 and gpdk045. PVS is another tool for Physical Verification on designs made using technology nodes like gpdk045 and below.

### PHYSICAL VERIFICATION WITH ASSURA:

The first step in Physical Verification is the Technology Library Mapping.

#### Technology Library Mapping:

Select “Assura -> Technology”, an “Assura Technology Lib Select” window can be seen as in Figure-74.

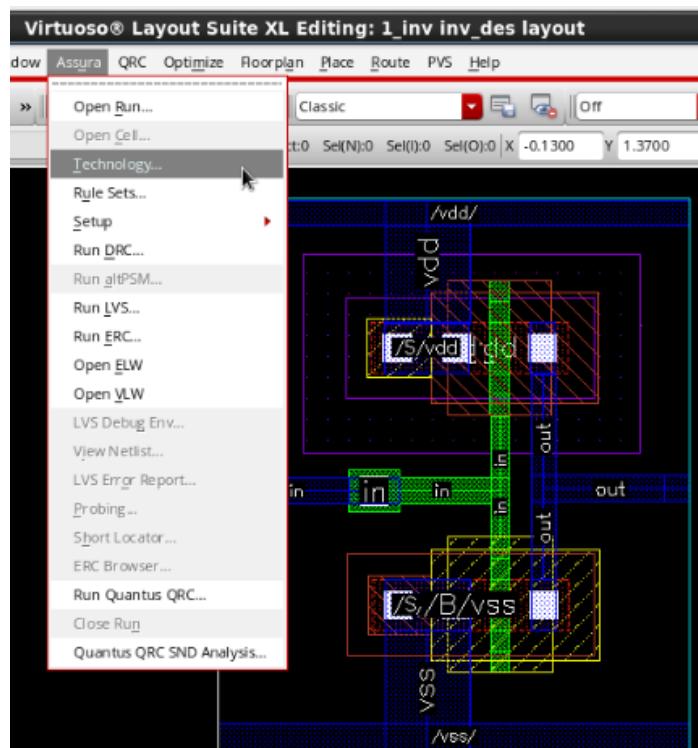


Figure-74

Select “Browse” so that the “File Selector” can be seen as in Figure-75.

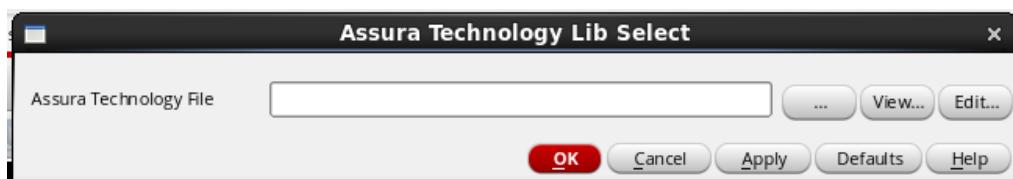
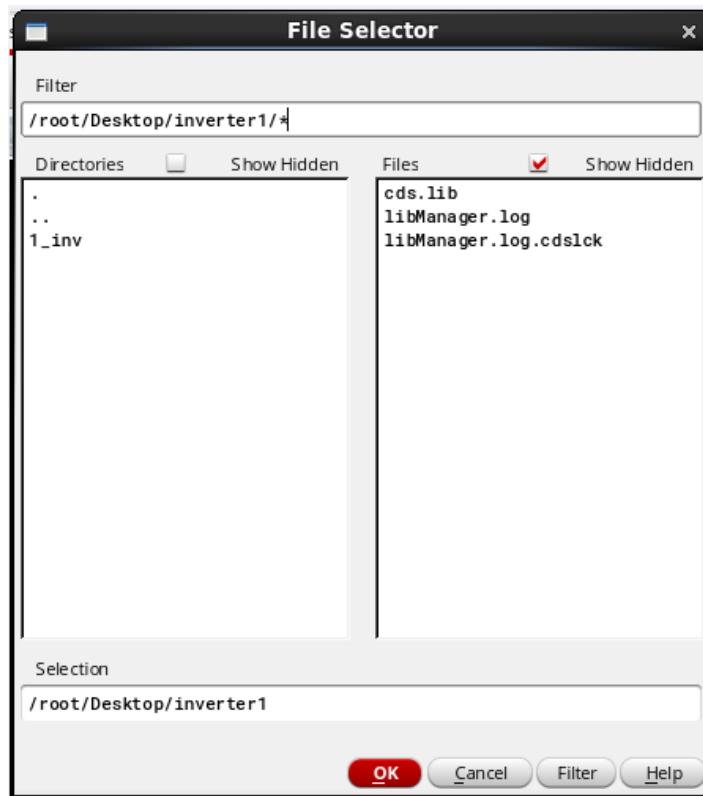


Figure-75

Two columns, “Directories” and “Files” can be seen. The “Single Dot” under “Directories” indicates the present working directory, “Double Dot” just below the “Single Dot” is used to

go back to the previous/next directories and “**1\_inv**” indicates the library under which the layout is saved. Use the “**Double Dot**” option to browse the library file “**assura\_tech.lib**” as in Figure-76, based on the technology node of interest and select OK.



**Figure-76**

### DRC:

To perform the DRC check, select “**Assura -> Run DRC**” as in Figure-77.

A “**Run Assura DRC**” window can be seen as in Figure-78. Verify the Library, Cell and View in the second row. Give any name under the “**Run Name**” option, click on the drop down next to “**Technology**” and select the “**Technology Node**” of interest.

The “**Run Assura DRC**” window after mentioning the options as given above can be seen as in Figure-79.

Select OK to run the DRC. A “**Progress**” tab can be seen at the right-side bottom corner of the screen as in Figure-80. To check the background process or log file, select “**Watch Log File**” option under the “**Progress**” tab. A run completion tab pops-up as in Figure-81(a). Select “**Yes**” and the DRC run result can be seen as in Figure-81(b).

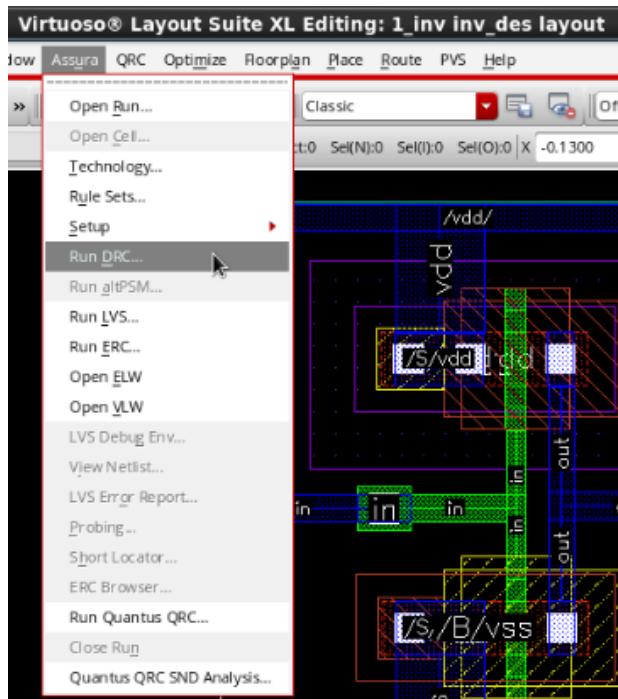


Figure-77

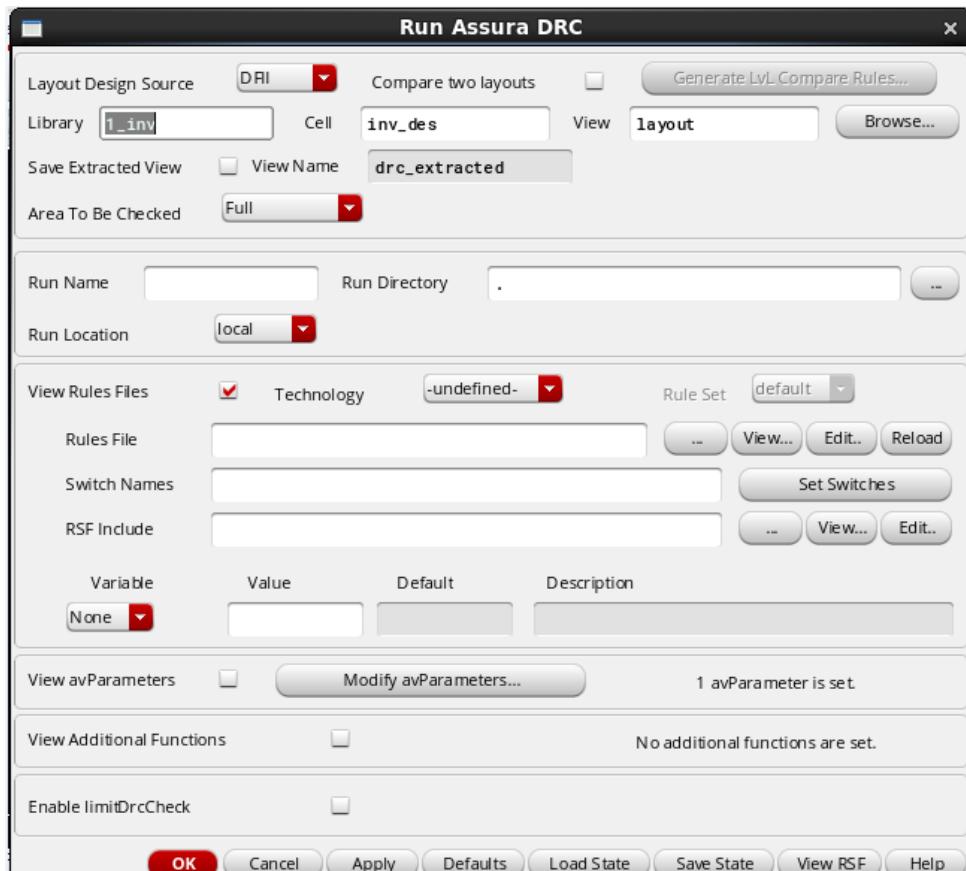
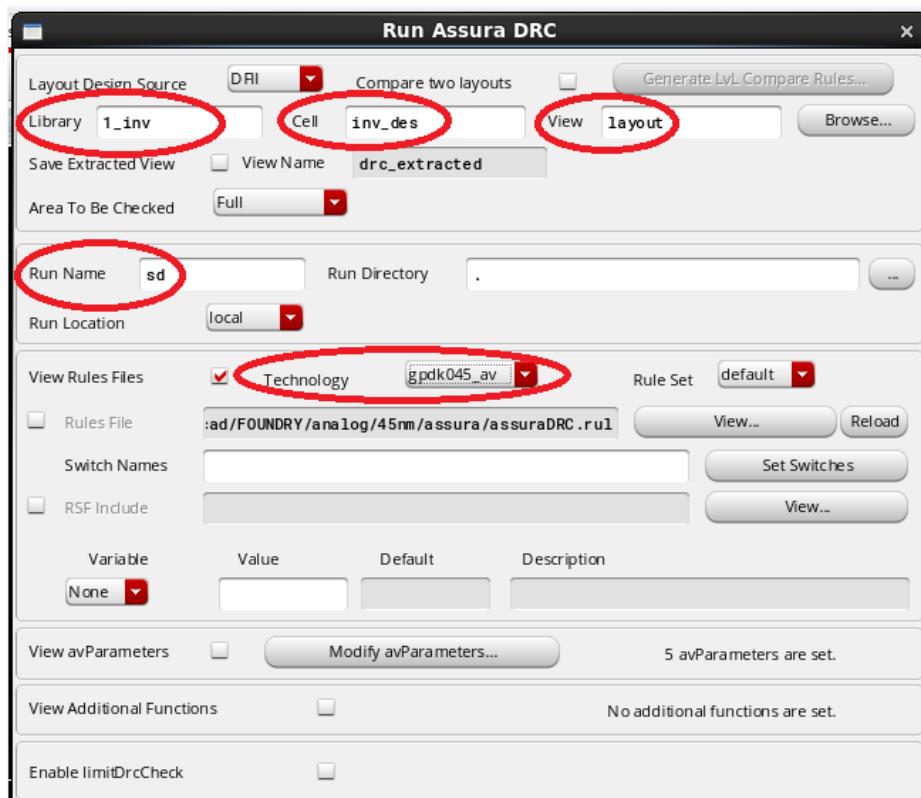
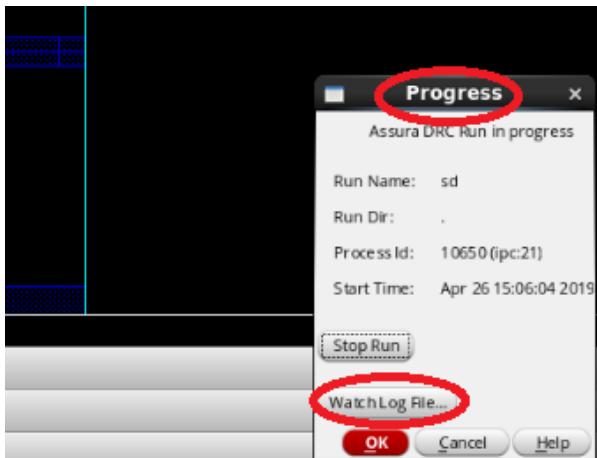
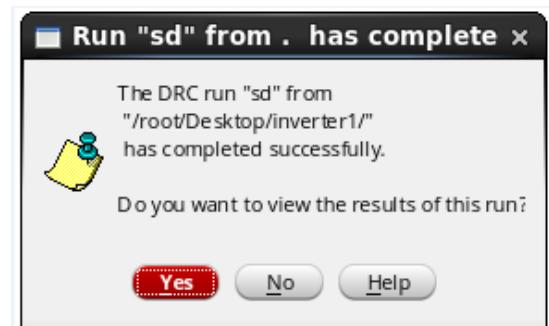
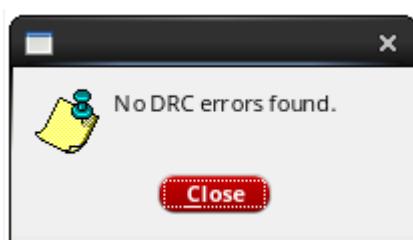


Figure-78


**Figure-79**

**Figure-80**

**Figure-81(a)**

**Figure-81(b)**

### LVS:

To perform the LVS check, select “Assura -> Run LVS” as in Figure-82.

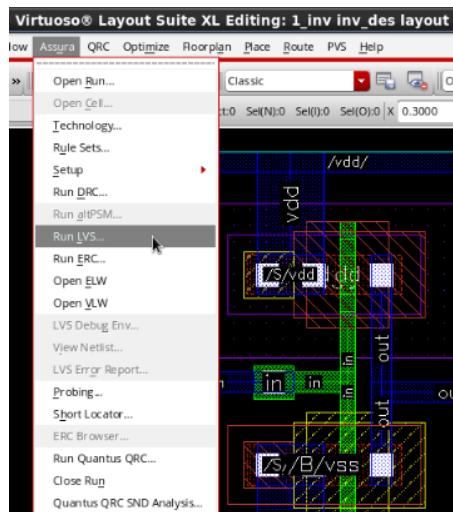


Figure-82

A “Run Assura LVS” window can be seen. Verify the Library, Cell and View for the Schematic Design Source and Layout Design Source. Give any name under the “Run Name” option, click on the drop down next to “Technology” and select the “Technology Node” of

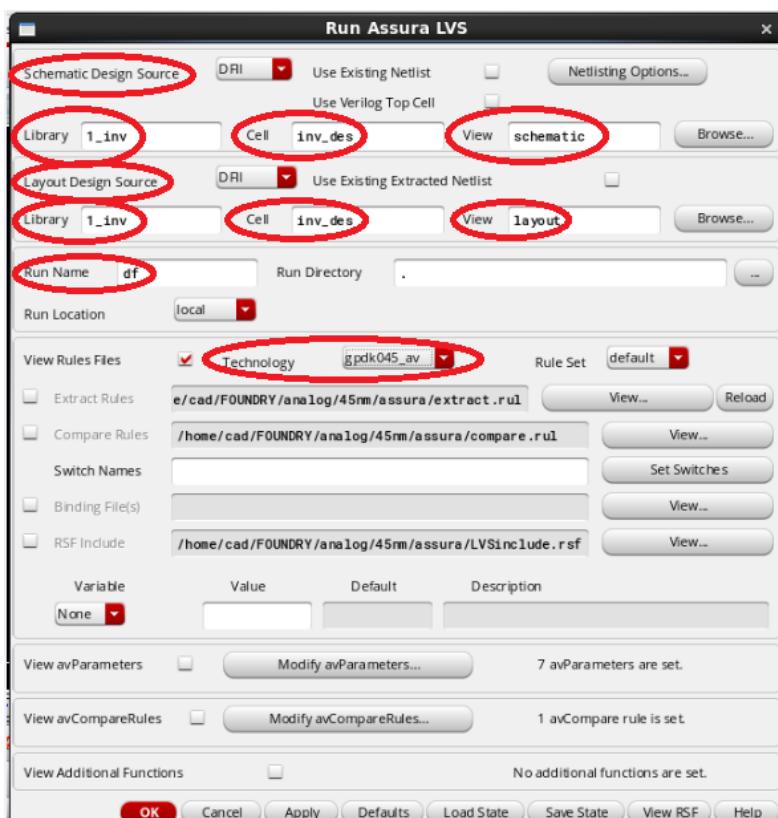


Figure-83

interest and the “**Run Assura LVS**” window after mentioning the options as given above can be seen as in Figure-83.

Select OK to run the LVS. A “**Progress**” tab can be seen at the right-side bottom corner of the screen similar to Figure-80. To check the background process or log file, select “**Watch Log File**” option under the “**Progress**” tab.

A run completion tab pops-up as in Figure-84(a). Select “**Yes**” and the DRC run result can be seen as in Figure-84(b).

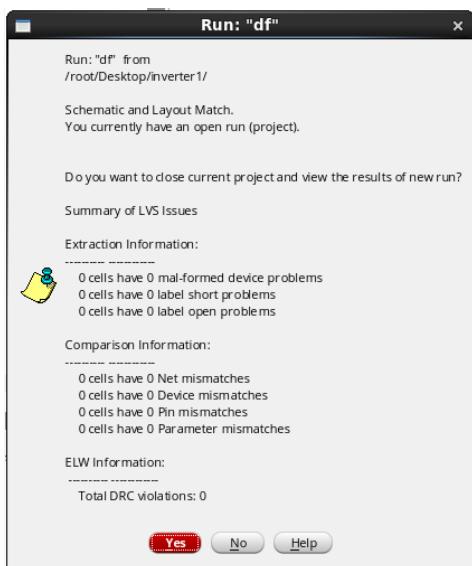


Figure-84(a)

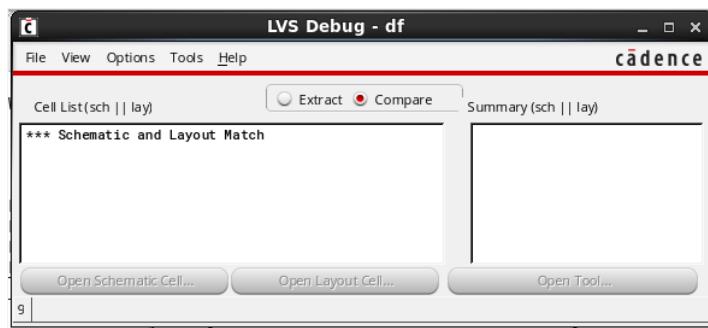


Figure-84(b)

### QRC:

To extract the Parasitics, select “**Assura -> Run Quantus QRC**” as in Figure-85.

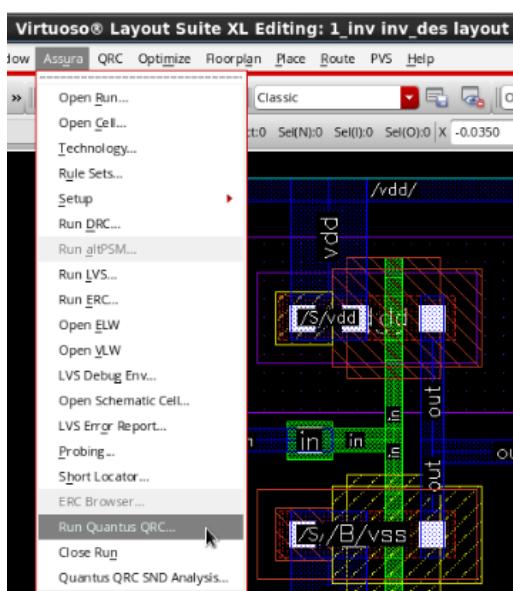
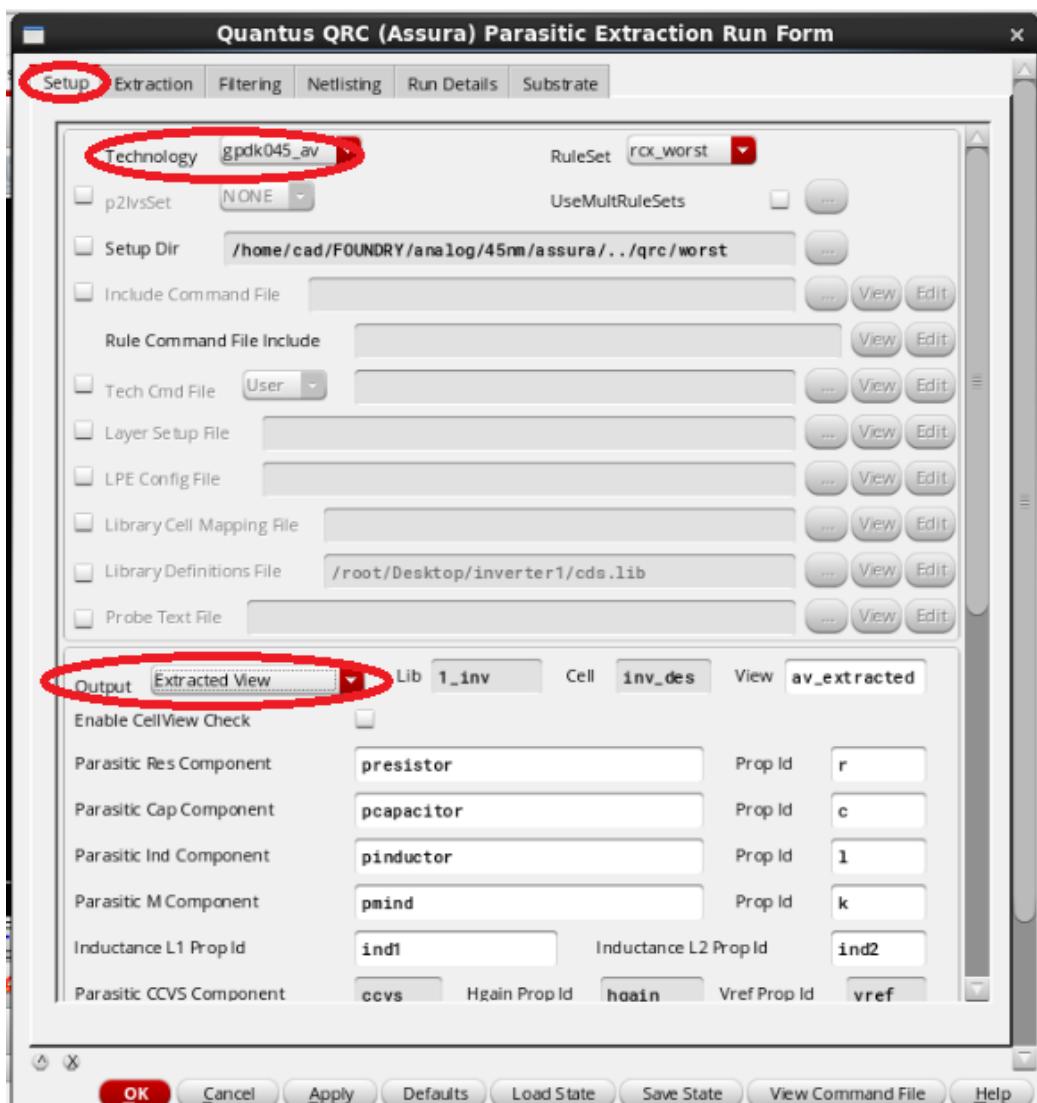


Figure-85

A “Quantus QRC (Assura) Parasitic Extraction Run Form” window can be seen as in Figure-86. Under the “Setup” tab, verify the “Technology”, “Output -> Extracted View” and under “Extraction” tab, verify “Extraction Type -> RC”, “Ref Node -> vdd! (or) gnd!” as in Figure-87(a) & 87(b). Select OK to extract the Parasitics.

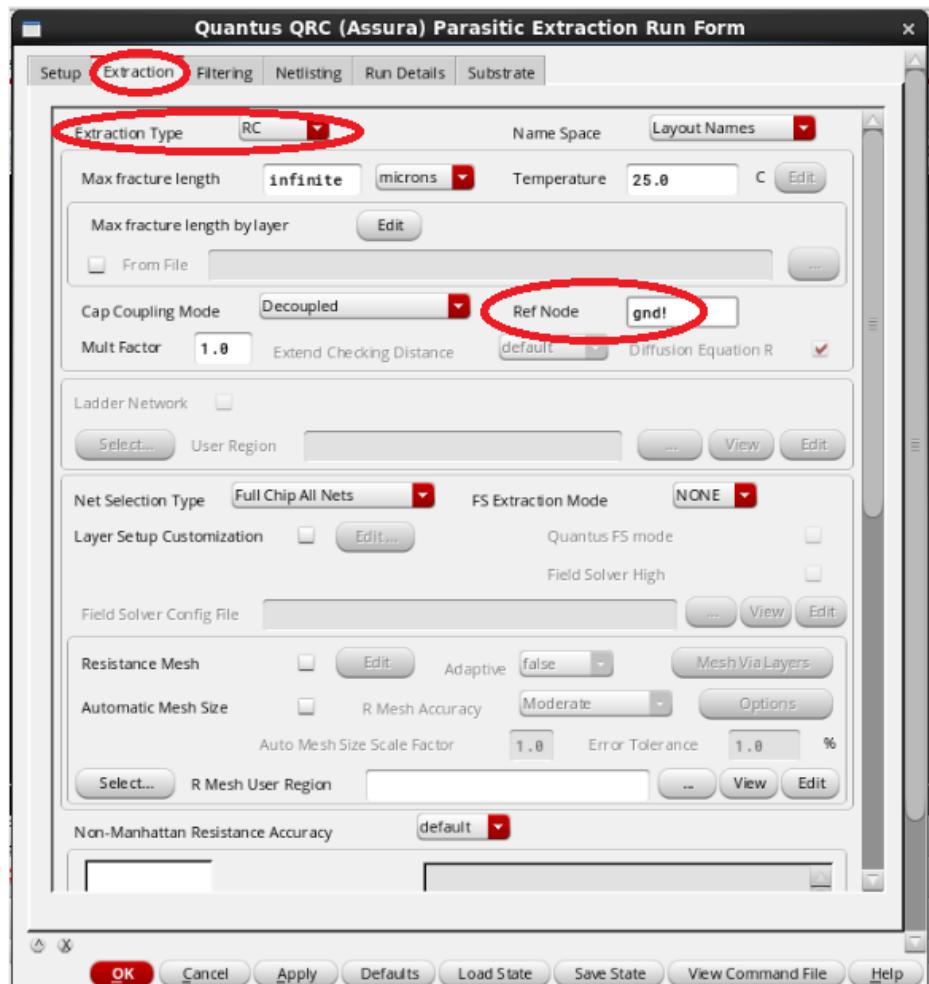


**Figure-87(a)**

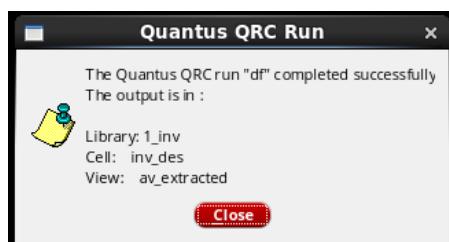
A “Progress” tab can be seen at the right-side bottom corner of the screen as in Figure-80. To check the background process or log file, select “Watch Log File” option under the “Progress” tab.

A run completion tab pops-up as in Figure-88. Select “Close” and the “av\_extracted” view can be seen in the Library Manager as in Figure-89.

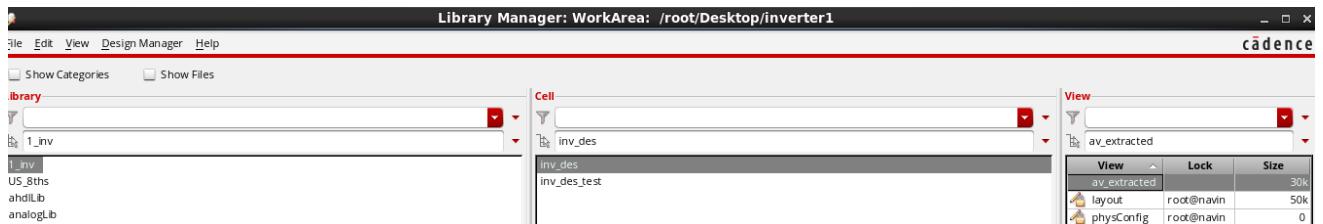
Make a double click on the “av\_extracted” view, a design can be seen as in Figure-90. Select “Shift+F” on the keyboard and if zoomed into the design with the help of mouse scroller, the parasitic resistor, its value and parasitic capacitor, its value can be seen as in Figure-91.



**Figure-87(b)**



**Figure-88**



**Figure-89**

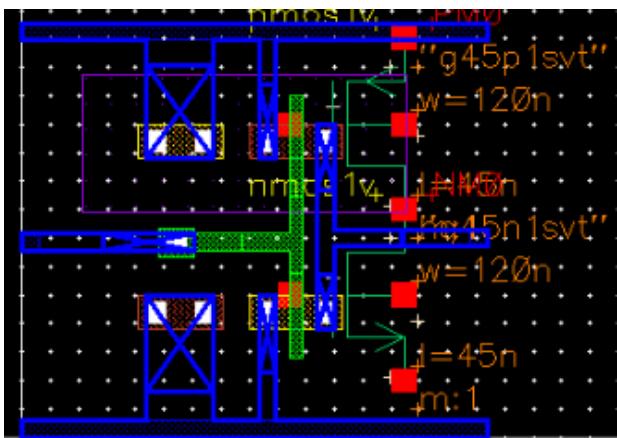


Figure-90

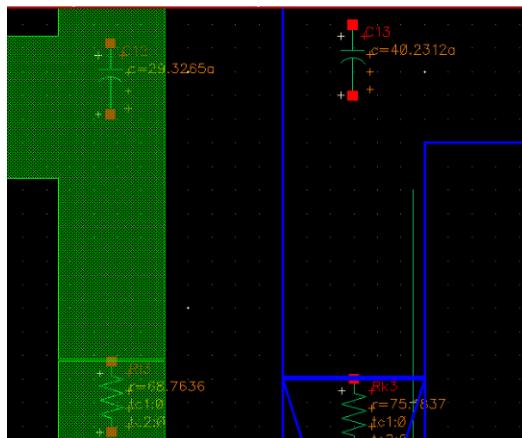


Figure-91

### PHYSICAL VERIFICATION WITH PVS:

PVS tool is for Physical Verification of circuits designed with Technology nodes of 45nm and below. The steps to perform DRC, LVS and QRC are as follows.

#### DRC:

To perform the DRC check, select “PVS -> Run DRC” as in Figure-92.

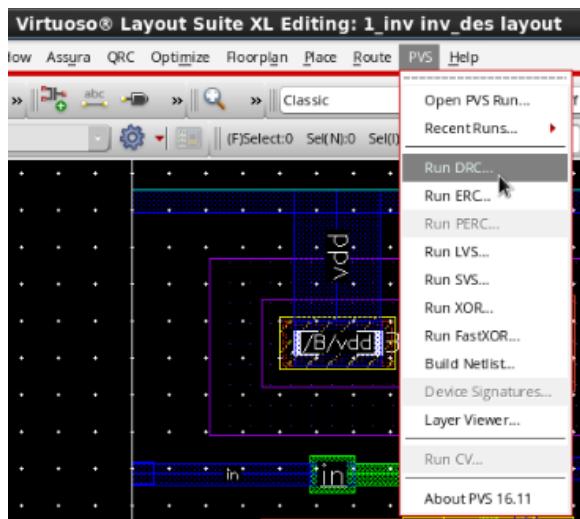


Figure-92

A “PVS DRC Run Submission Form” window can be seen as in Figure-93.

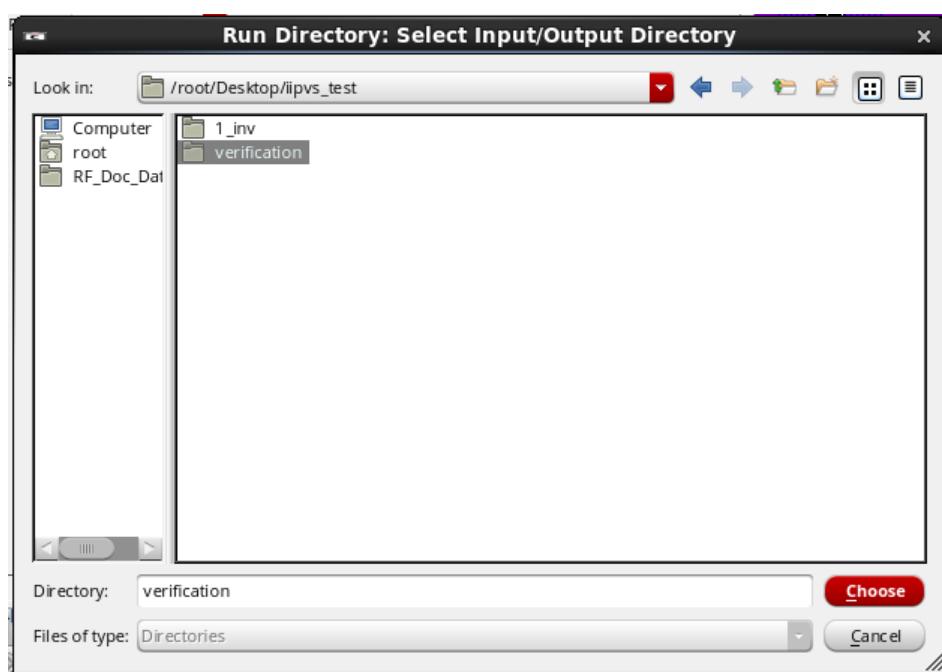
Select “Run Data” tab, browse a “Run Directory” as in Figure-94.

Select “Rules” tab, browse the “Technology Mapping File”, select the “Technology” after which the “DRC.rul” can be seen under “Rules” and select “Submit” as shown in Figure-95.

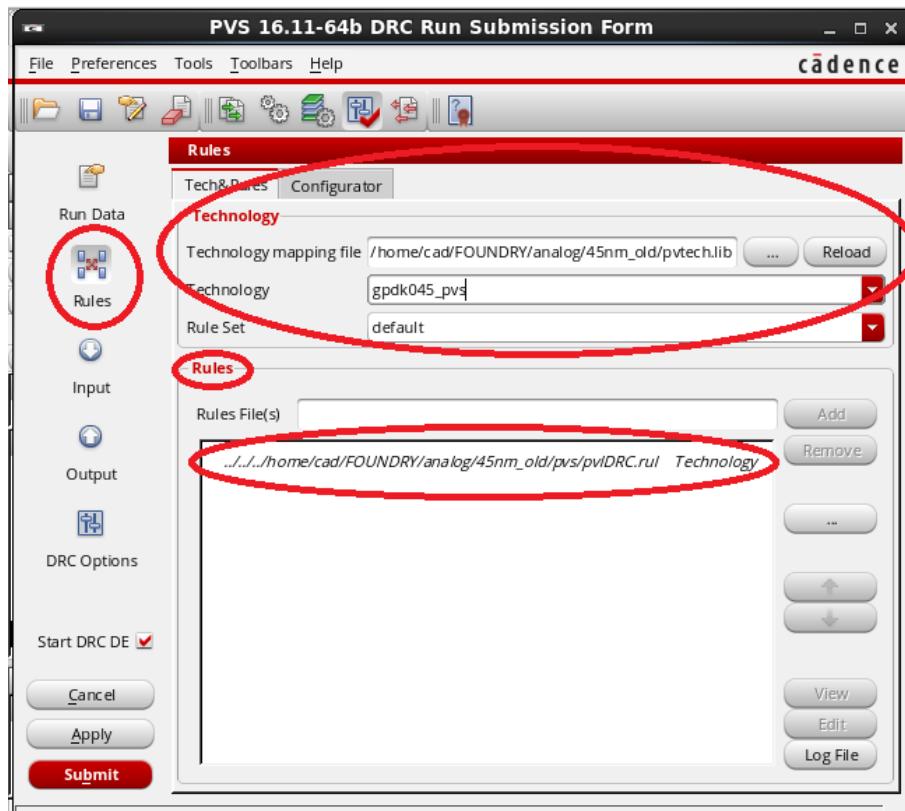
A run completion tab pops-up and the run results can be seen as in Figure-96.



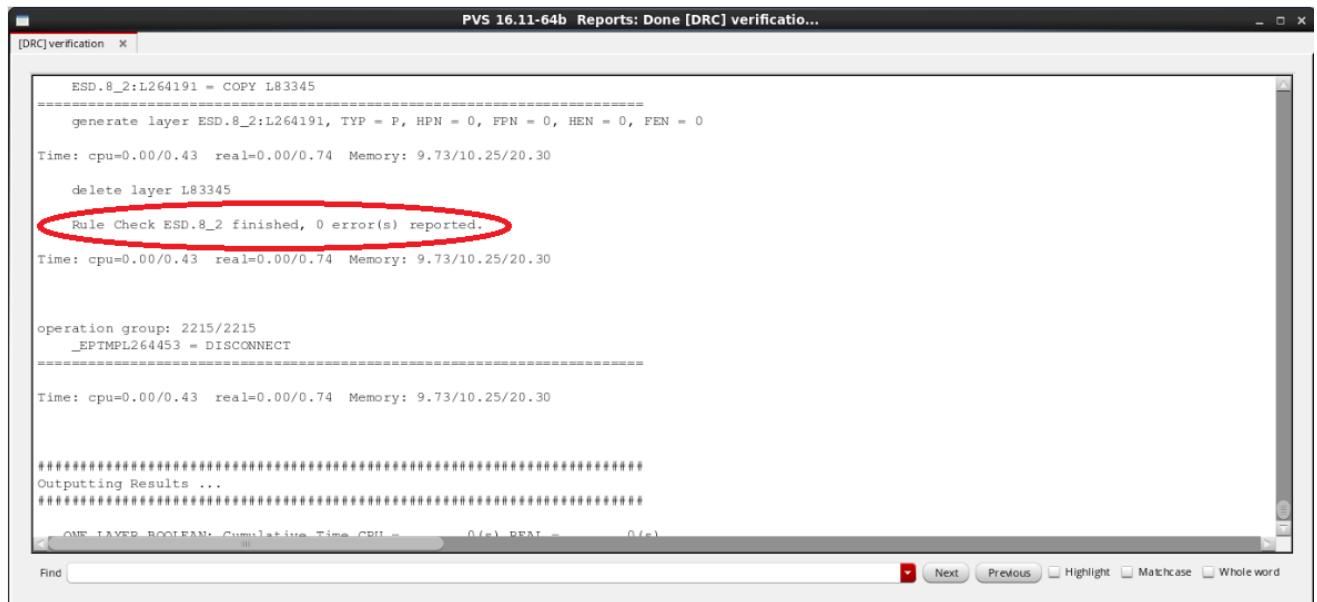
**Figure-93**



**Figure-94**



**Figure-95**



The screenshot shows the Cadence PVS 16.11-64b software interface with the title "PVS 16.11-64b Reports: Done [DRC] verification...". The window displays a command history and results for a DRC verification. The text output includes:

```

ESD.8_2:L264191 = COPY L83345
=====
generate layer ESD.8_2:L264191, TYP = P, HPN = 0, FPN = 0, HEN = 0, FEN = 0
Time: cpu=0.00/0.43 real=0.00/0.74 Memory: 9.73/10.25/20.30

delete layer L83345
Rule Check ESD.8_2 finished, 0 error(s) reported.
Time: cpu=0.00/0.43 real=0.00/0.74 Memory: 9.73/10.25/20.30

operation group: 2215/2215
_EPTMPL264453 = DISCONNECT
=====

Time: cpu=0.00/0.43 real=0.00/0.74 Memory: 9.73/10.25/20.30

#####
# Outputting Results ...
#####

ONE LAYER BOOLEAN Cumulative Time CPU= 0 (s) REAL= 0 (s)

```

At the bottom, there are "Find" and search/filter buttons: Find, Next, Previous, Highlight, Matchcase, Whole word.

**Figure-96**

### LVS:

To perform the LVS check, select “**PVS -> Run LVS**” as in Figure-97.

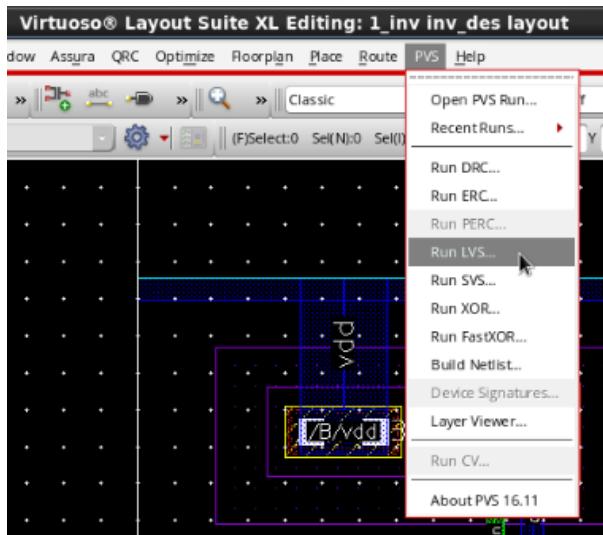


Figure-97

A “PVS LVS Run Submission Form” window can be seen as in Figure-98.

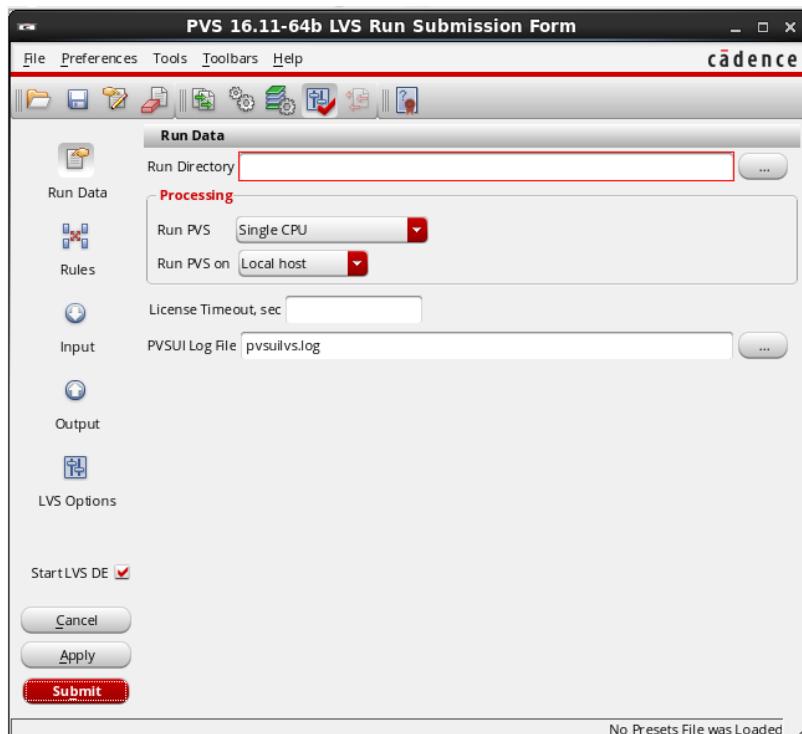
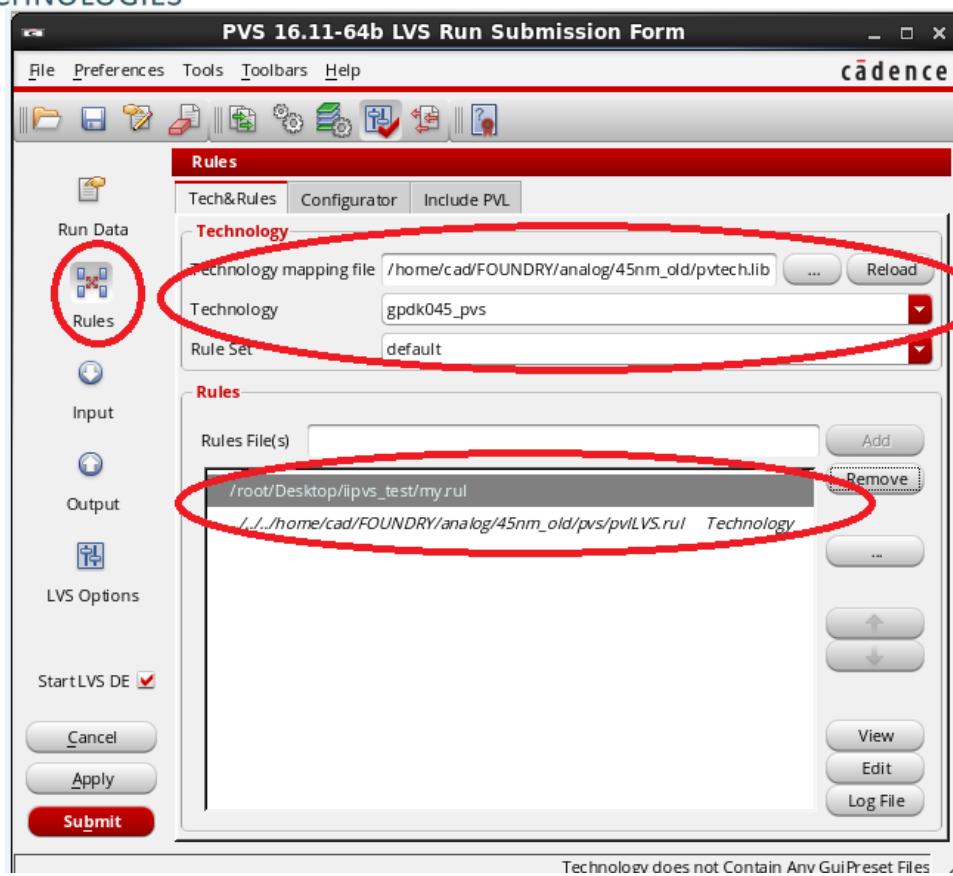
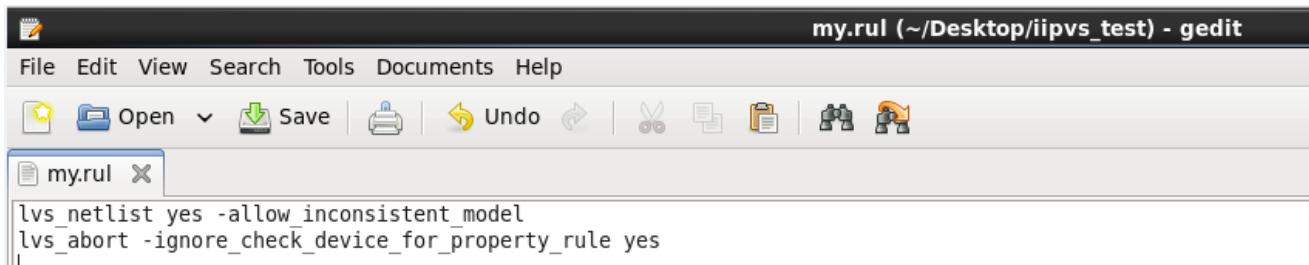
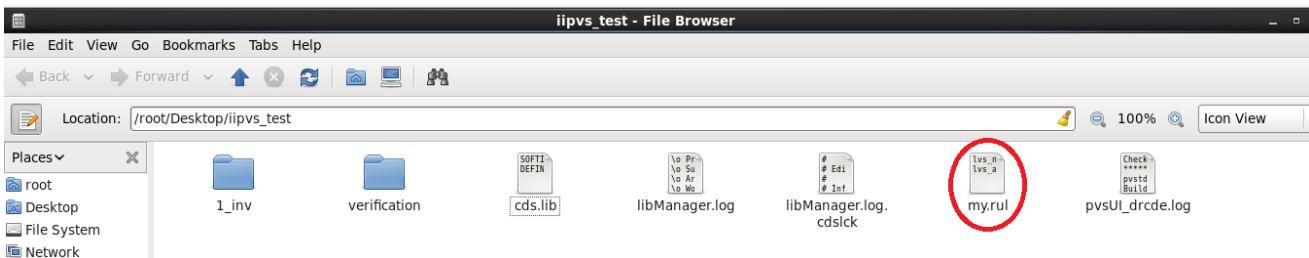


Figure-98

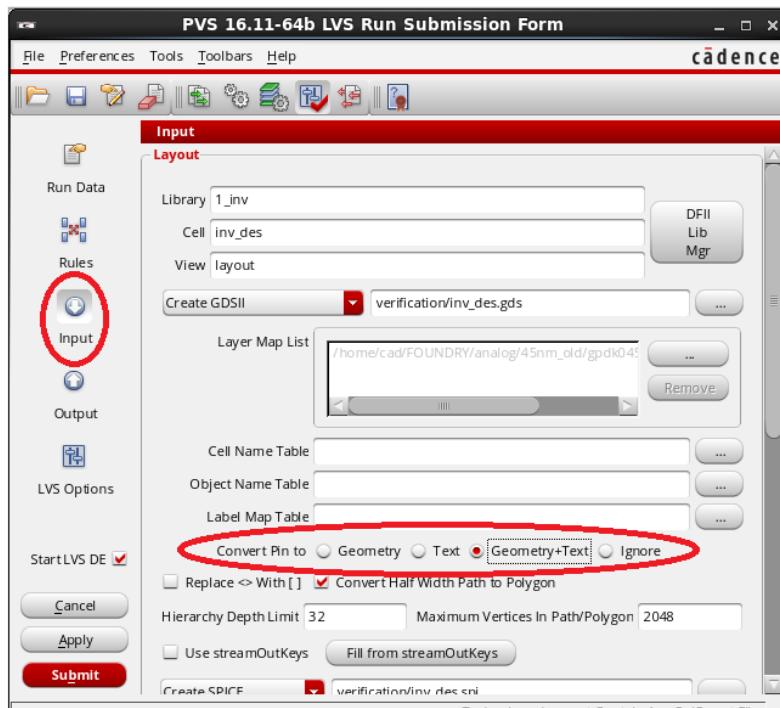
Select “Run Data” tab, browse a “Run Directory” similar to that in Figure-94. Select “Rules” tab, browse the “Technology Mapping File”, “my.rul” file and select the “Technology” after which the “LVS.rul” and “my.rul” can be seen under “Rules”. The “my.rul” file should be created manually as in Figure-99(a) and saved in the work directory as in Figure-99(b).


**Figure-98**


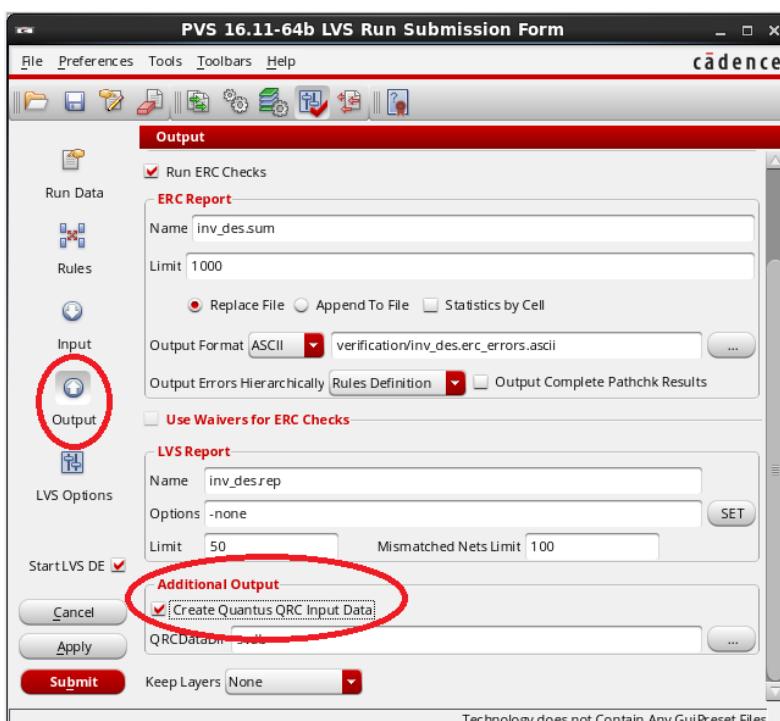
```
my.rul (~/_Desktop/iipvs_test) - gedit
File Edit View Search Tools Documents Help
File Open Save Undo Redo Cut Copy Paste Find Replace Print View
my.rul X
lvs_netlist yes -allow_inconsistent_model
lvs_abort -ignore_check_device_for_property_rule yes
```

**Figure-99(a)**

**Figure-99(b)**

Select “**Input**” tab and select “**Convert Pin to -> Geometry + Text**” as in Figure-100.  
Select “**Output**” tab and enable “**Create Quantus QRC Input Data**” under “**Additional Output**” as in Figure-101 to create the input for QRC run and select “**Submit**”.

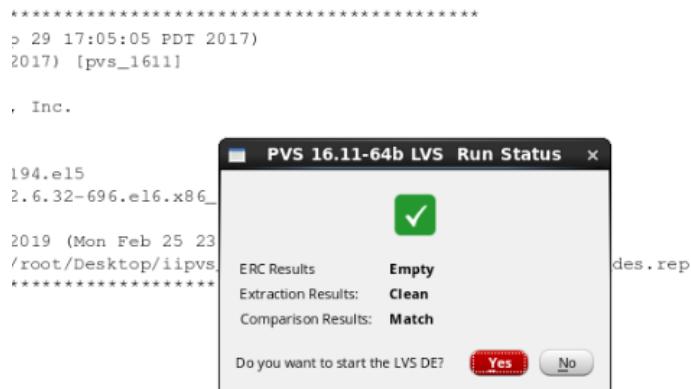


**Figure-100**

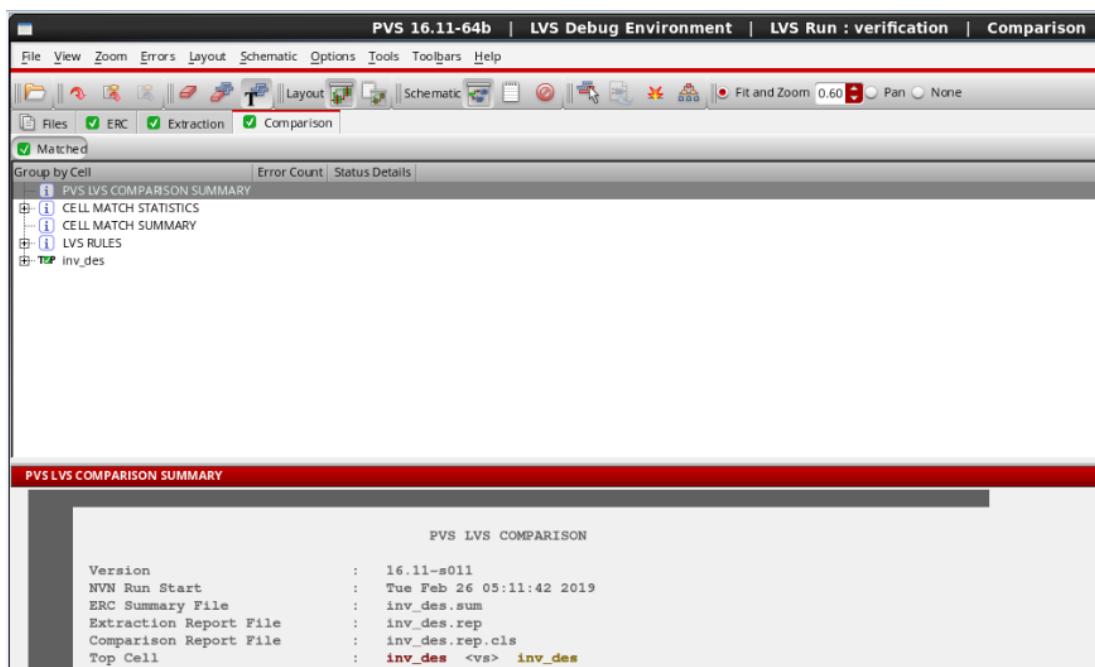


**Figure-101**

A run completion tab pops-up and the run results can be seen as in Figure-102(a) & (b).



**Figure-102(a)**



**Figure-102(b)**

### QRC:

To extract the Parasitics, select “**QRC -> Run PVS - Quantus QRC**” as in Figure-103.

A “**Quantus QRC (PVS) Parasitic Extraction Run Form**” window can be seen. Under the “**Setup**” tab, verify the “**Technology**”, “**RuleSet**”, “**Output -> Extracted View**”, “**Enable CellView Check**” option should be disabled and under “**Extraction**” tab, verify “**Extraction Type -> RC**”, “**Ref Node -> vdd! (or) gnd!**” as in Figure-104(a) & 104(b). Select OK to extract the Parasitics.

A “**Progress**” tab can be seen at the right-side bottom corner of the screen as in Figure-80. To check the background process or log file, select “**Watch Log File**” option under the “**Progress**” tab. A run completion tab pops-up as in Figure-88. Select “**Close**” and the “**av\_extracted**” view can be seen in the Library Manager as in Figure-89.

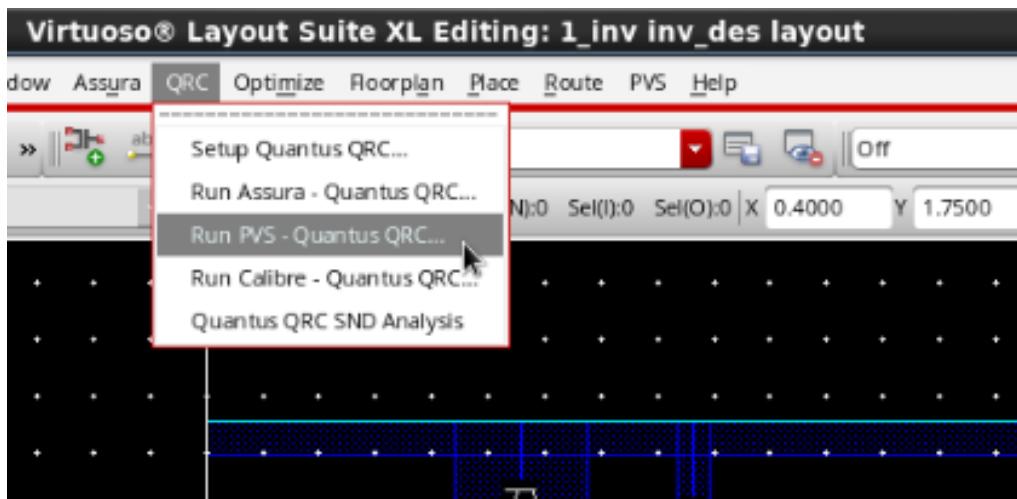


Figure-103

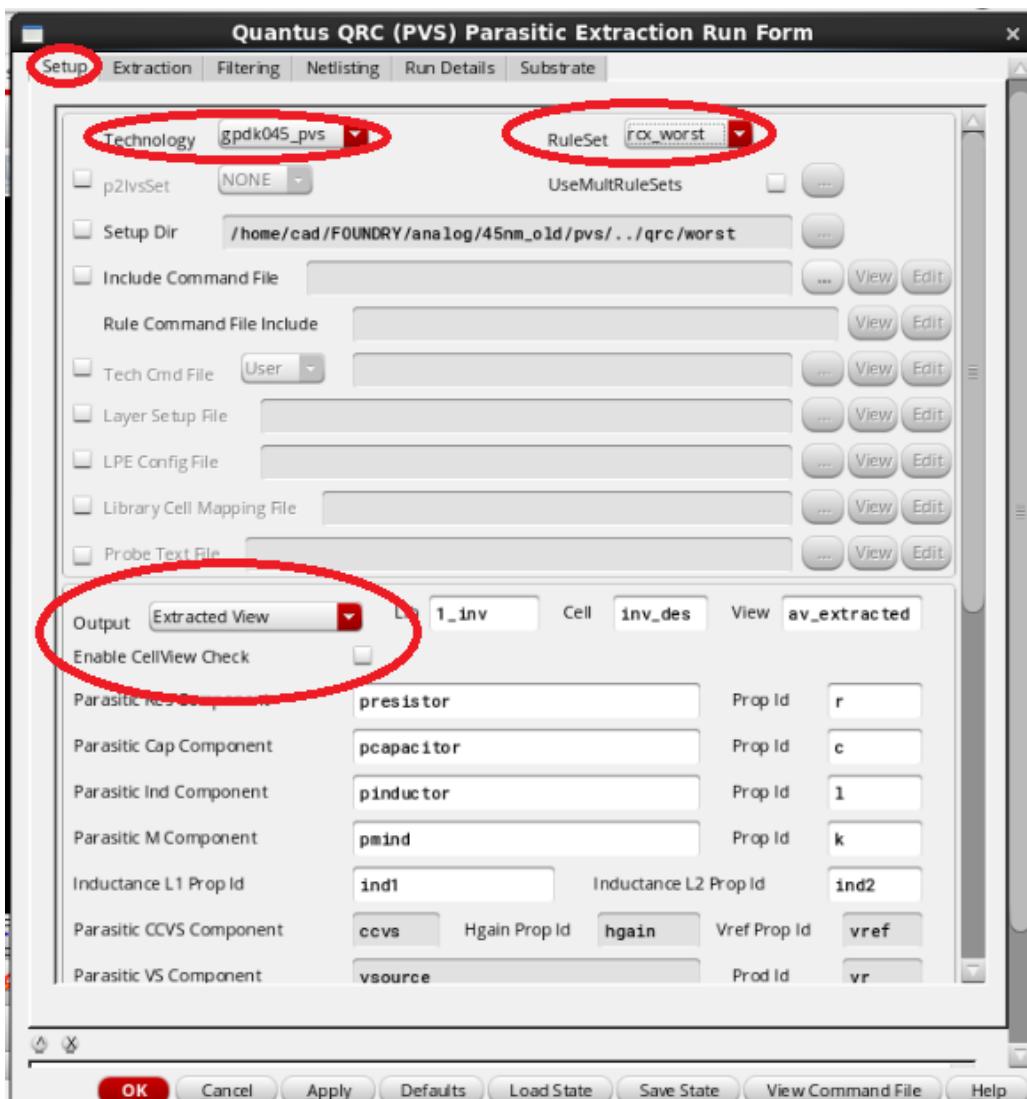
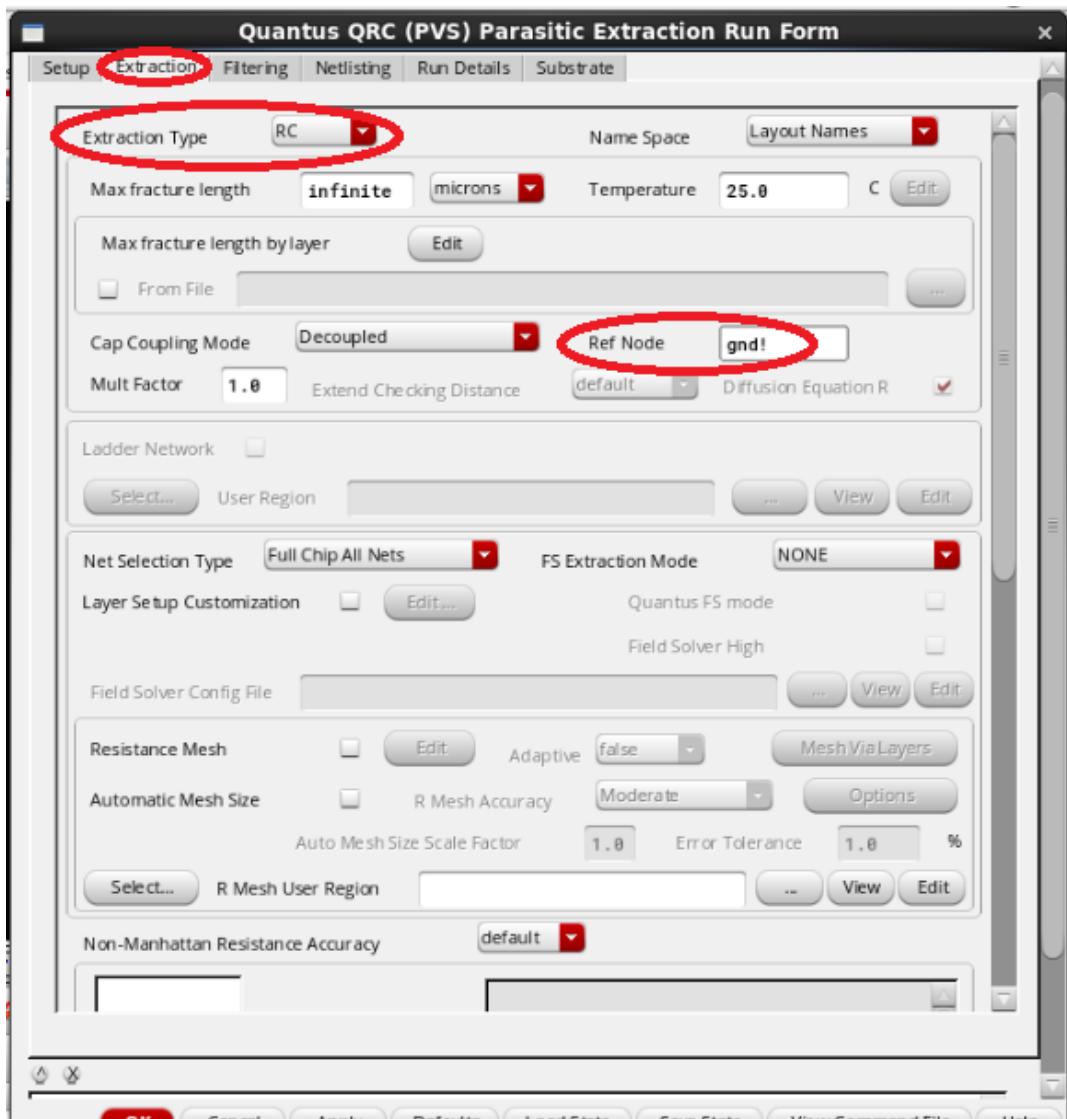


Figure-104(a)



**Figure-104(b)**

Make a double click on the “av\_extracted” view, a design can be seen as in Figure-90. Select “Shift+F” on the keyboard and if zoomed into the design with the help of mouse scroller, the parasitic resistor, its value and parasitic capacitor, its value can be seen as in Figure-91.

### BACKANNOTATION (or) POST LAYOUT SIMULATION:

To perform Backannotation, select the library that was created earlier, select the cell that has the testbench circuit and select schematic as view as in Figure-105.

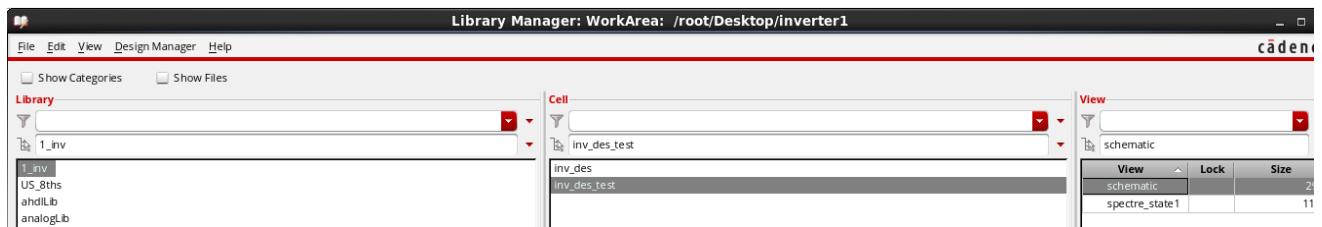


Figure-105

Select “File -> New -> Cell View”, select “Type -> Config” as in Figure-106 and select OK.

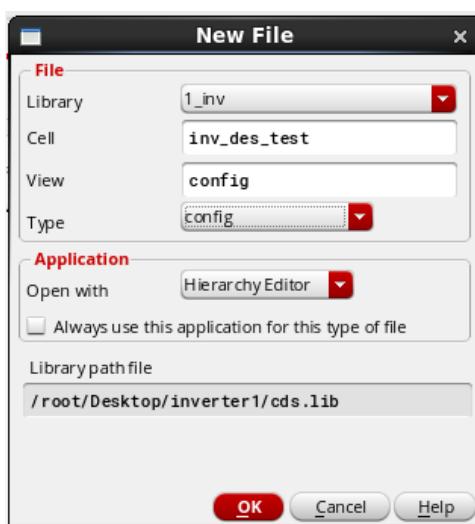
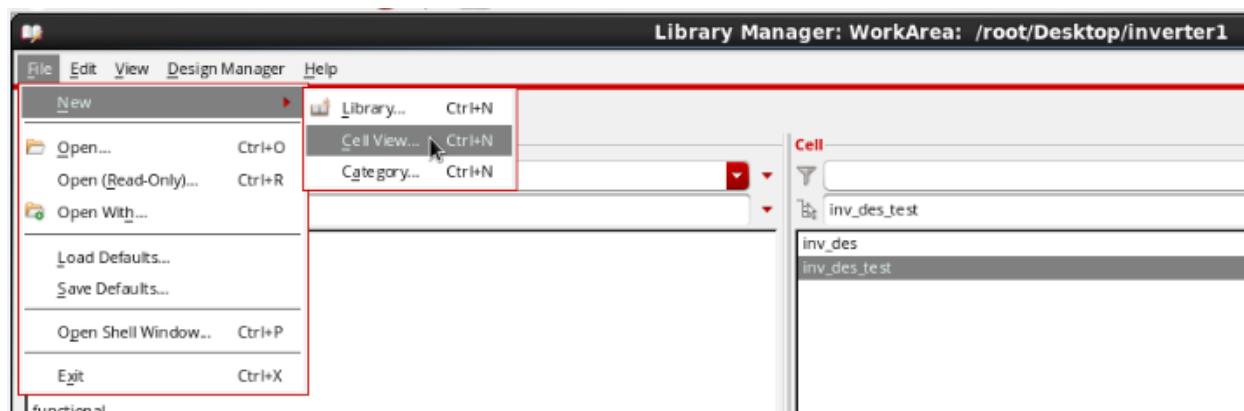


Figure-106

A “New Configuration” window pops-up as in Figure-107. Select “Use Template” option, a “Use Template” tab pops-up as in Figure-108(a), select “Name -> spectre” under “Template” and select OK as in Figure-108(b).

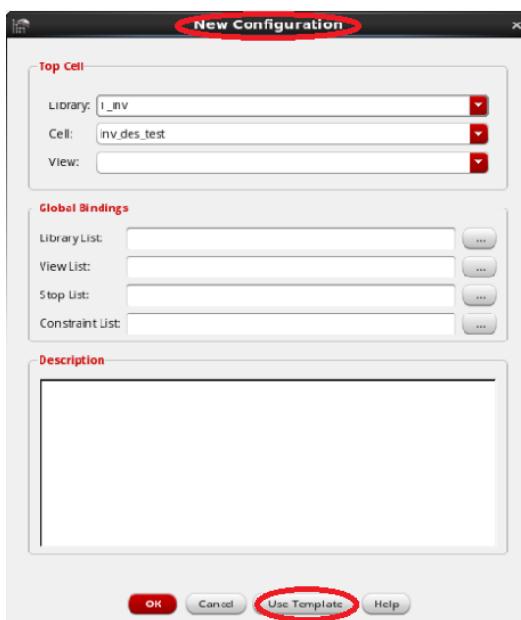


Figure-107



Figure-108(a)

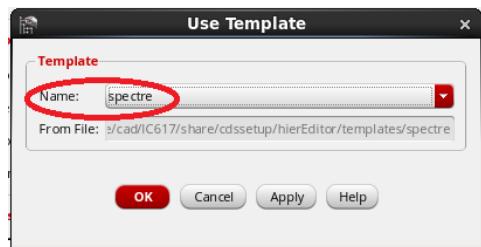


Figure-108(b)

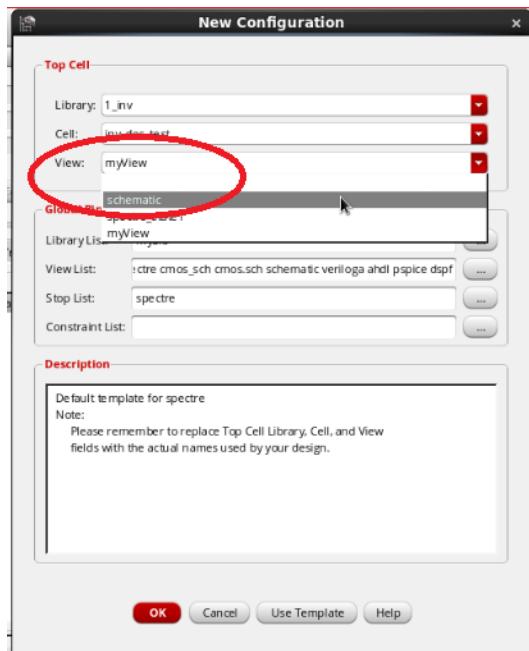
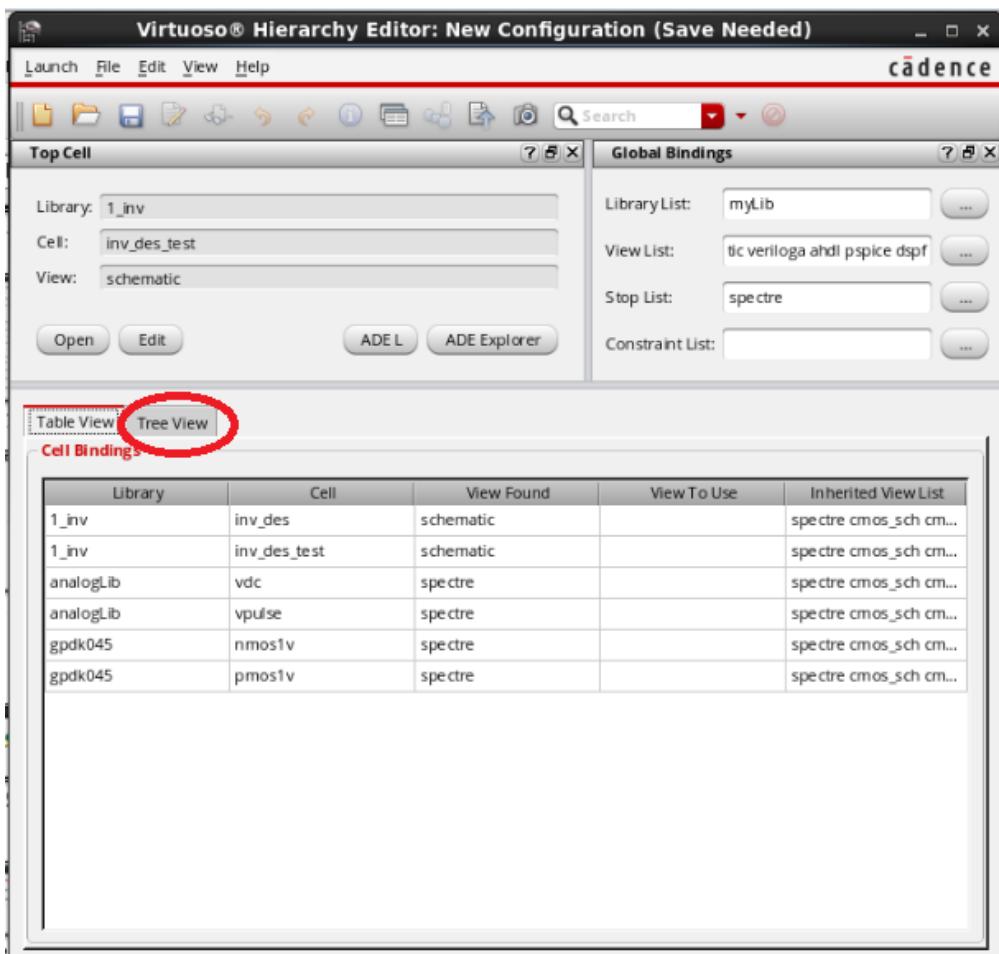


Figure-108(c)

This brings back the “**New Configuration**” window as in Figure-108(c), under “**Top Cell**”, select “**View -> Schematic**” and select OK.

A “**Virtuoso Hierarchy Editor: New Configuration**” window pops-up as in Figure-109(a). Select “**Tree View**”, now select “**I0**” folder, make a right click on mouse, select “**Set Instance View**” and select “**av\_extracted**” as in Figure-109(b).



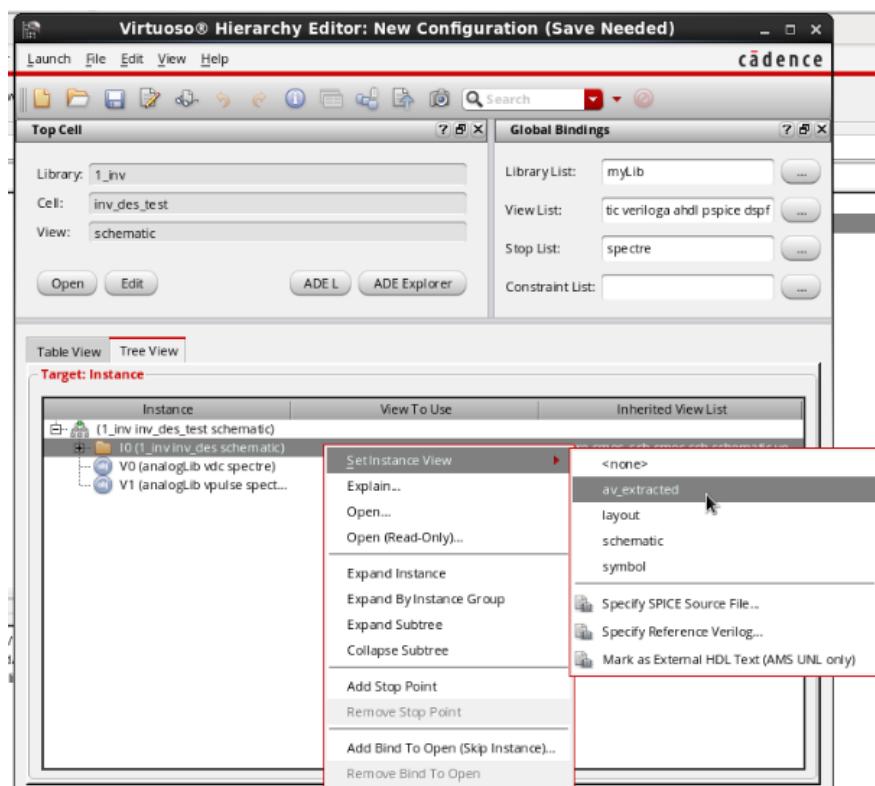
**Figure-109(a)**

When we select the “+” sign just before the “**I0**” folder, we can see the parasitic resistors and capacitors getting imported to the circuit as in Figure-110.

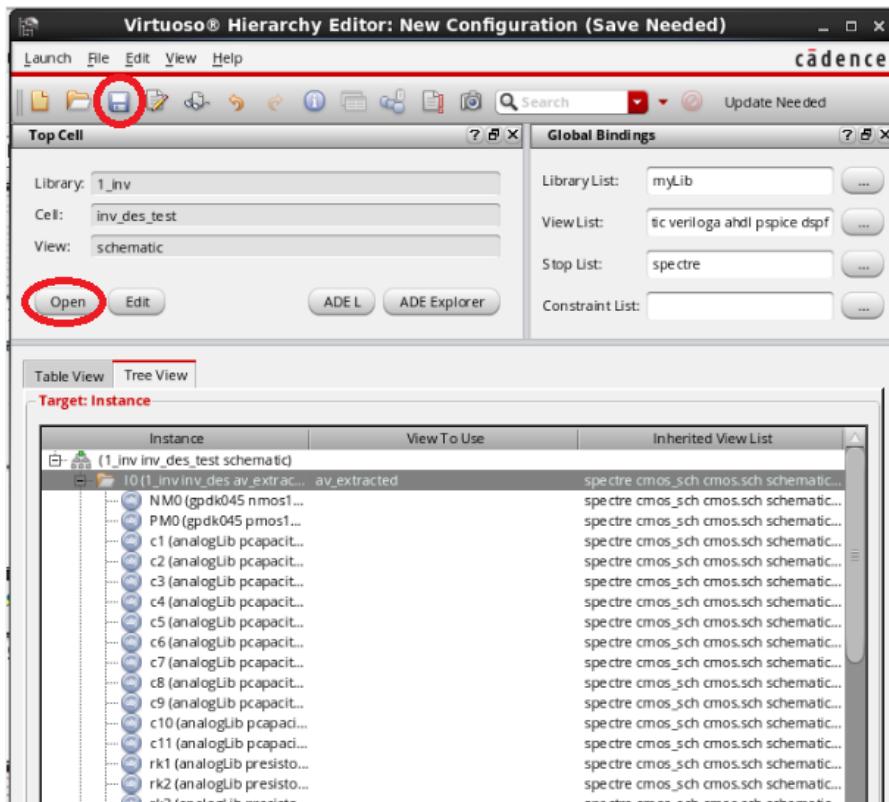
Save the configuration and select “**Open**”, this should bring back the testbench circuit as in Figure-111.

Open ADE L by selecting “**Launch -> ADE L**”, select “**Session -> Load State**”, load the simulation state with which we simulated the circuit earlier by selecting “**Load State Option -> Cellview**” and select OK. This brings back the “**Analyses**” and “**Input & Output Nets**” as in Figure-112.

Select “**Simulation -> Netlist & Run**” and re-run the simulation. Compare the results of Pre-Layout & Post-Layout Simulation to analyze the impact of parasitic resistors and capacitors.



**Figure-109(b)**



**Figure-110**

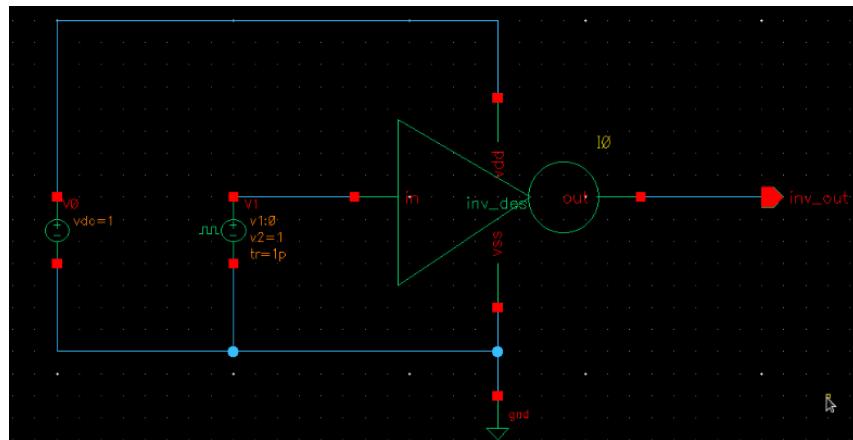


Figure-111

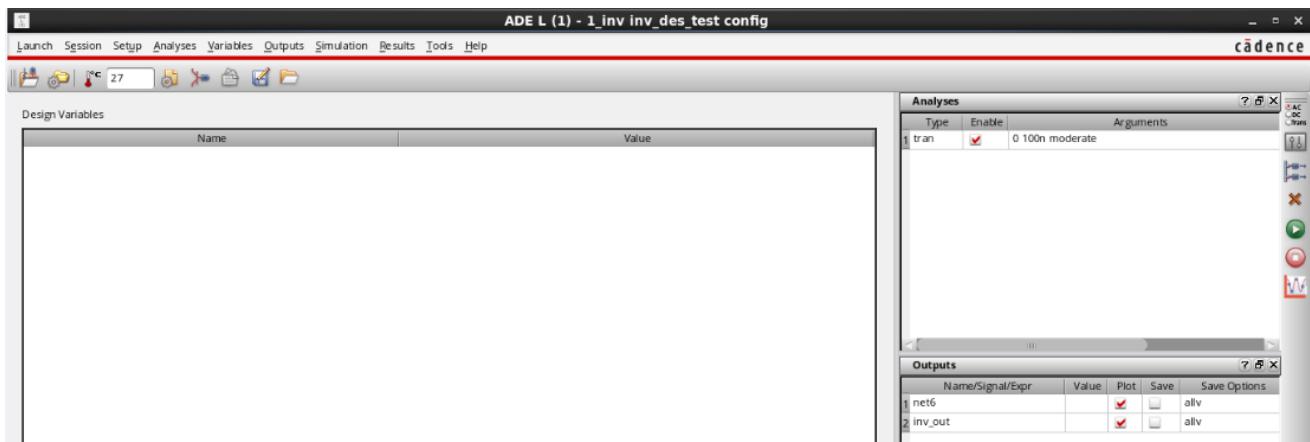


Figure-112

### GDSII:

The final step of the Full Custom IC Design flow is the generation of GDS file. To generate GDS file, open Virtuoso tab, select “File -> Export -> Stream”, this pops-up the “Virtuoso XStream Out” tab as in Figure-113(a) & (b) with “View(s) -> layout”.

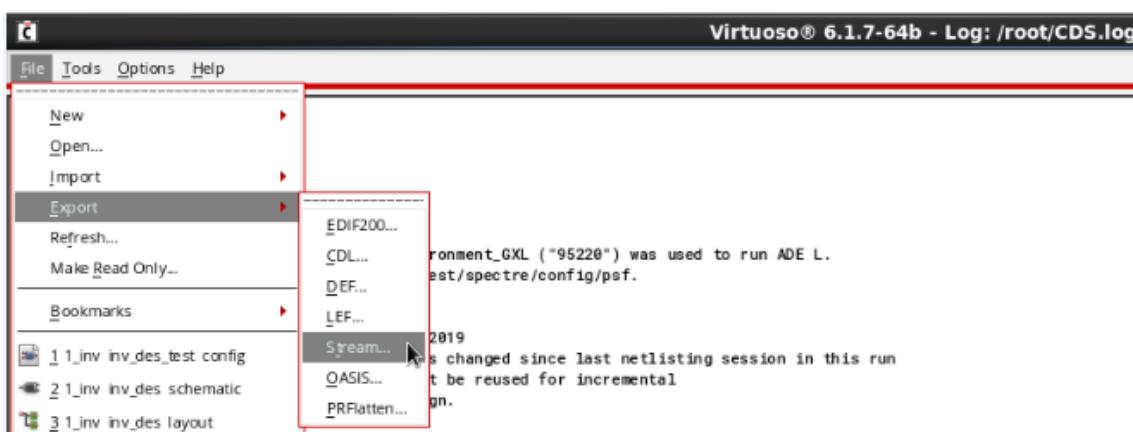


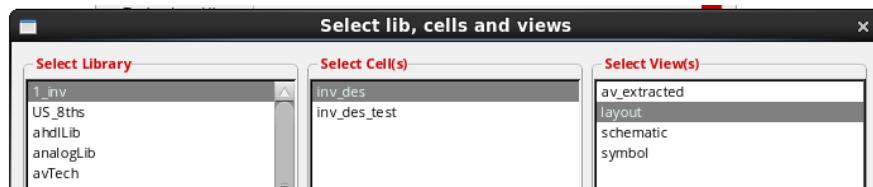
Figure-113(a)



**Figure-113(b)**

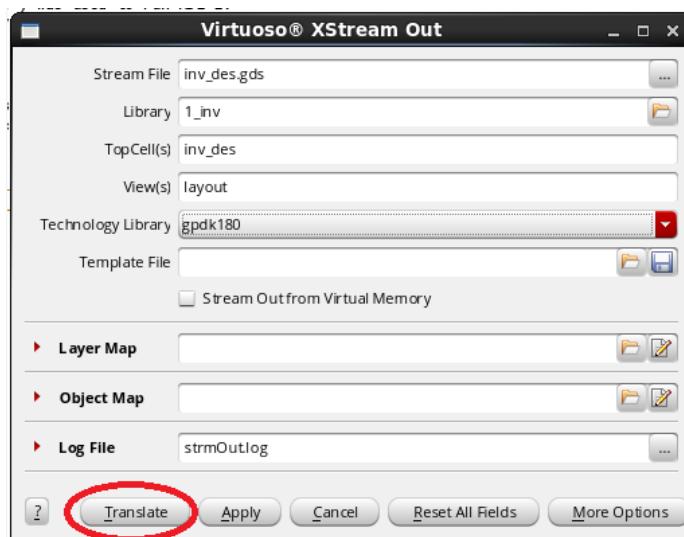
This means that the particulars related to layout of the design has to be browsed.

In “Virtuoso XStream Out” tab, select “Library” that was created earlier, select “TopCell(s)” which has the layout and the “Technology Library” with which the design was created as in Figure-113(c).



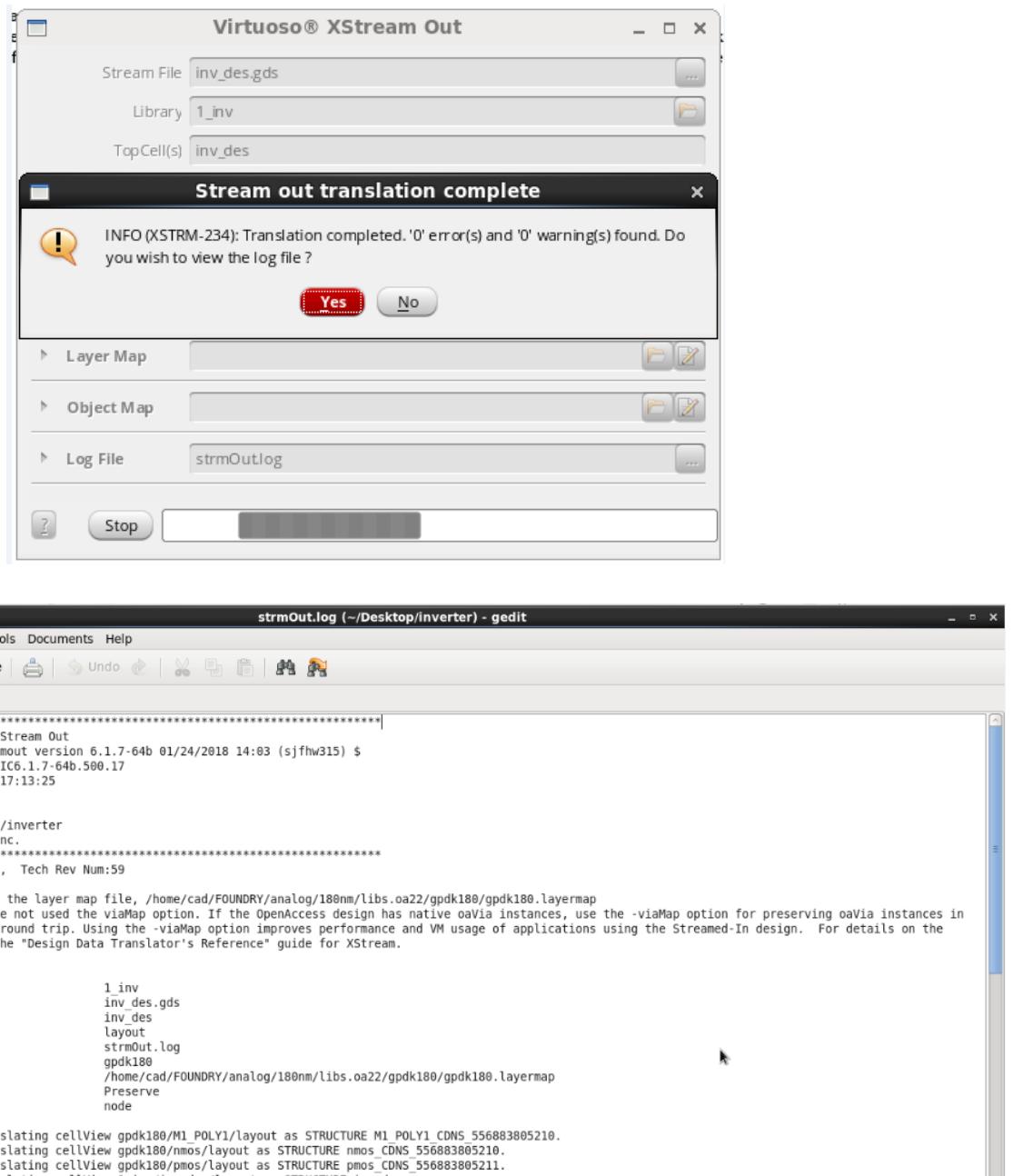
**Figure-113(c)**

Now select OK. The “Virtuoso XStream Out” tab can be seen as in Figure-113(d).



**Figure-113(d)**

Select “**Translate**” and the .gds file will be created and saved in the work directory. The log file can be seen as in Figure-114.



**Figure-114**