Koneru Lakshmaiah Education Foundation

(Category -1, Deemed to be University estd. u/s. 3 of the UGC Act, 1956)

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ACADEMIC YEAR 2023-24 - EVEN SEMESTER

22EC2222 - DIGITAL VLSI DESIGN

SEM – IN EXAM – 1 [QUESTION PAPER SET 1]

TIME: 90 MINUTES **MAX MARKS: 50 M**

Q.NO	QUESTION DESCRIPTION	CO	COI-BTL
SECTION – A [ANSWER ALL QUESTIONS]			
1	**Answer all Questions [6X 2 = 12 M]**		
1.A	Discuss different modelling styles in Verilog HDL.	CO1	BTL-2
1.B	Identify the keyword used in dataflow modelling in Verilog HDL.	CO1	BTL-2
1.C	Identify the type of modelling which uses basic primitives in Verilog.	CO1	BTL-2
1.D	Discuss different types of PLDs.	CO2	BTL-2
1.E	Infer key aspects of design methodology using Verilog HDL.	CO2	BTL-2
1.F	Describe some advantages of design using HDLs.	CO2	BTL-2
SECTION – B [ANSWER ALL QUESTIONS]			
2	**Answer all Questions [4 X 4 = 16M]**		
2.A	Examine the functionality of the bufif0 gate in Verilog and explain its use in digital circuit modelling.	CO1	BTL-2
2.B	Explore the application and significance of the ternary operator in Verilog.	CO1	BTL-2
2.C	Demonstrate the working principle of a Microcell in a CPLD.	CO2	BTL-2
2.D	Illustrate the components and arrangement of an FPGA using a block diagram.	CO2	BTL-2
SECTION – C [ANSWER Q3 OR Q4]			
3	**Answer all Questions [5M + 6M = 11M]**		
3.A	Apply gate level modelling to implement the Boolean function, Y = AB' + C in Verilog HDL. Write the code in a neat and readable manner.	CO1	BTL-3
3.B	Write a testbench using Verilog HDL for the design in the question above.	CO1	BTL-2
OR			
4	**Answer all Questions [5M + 6M = 11 M]**		
4.A	Imagine you are a digital system designer working on a security system for a smart building. The system involves two key sensors, P and Q, to detect motion and door status, respectively. The alarm should be triggered when either motion is detected, or door is open. Identify the logic of the circuit and write the Verilog HDL for the same.	CO1	BTL-3
4.B	Write a testbench using Verilog HDL for the design above.	CO1	BTL-2

SECTION – D [ANSWER Q5 OR Q6]			
5	**Answer all Questions [5M + 6M = 11M]**		
5.A	Illustrate the difference between a synchronous and asynchronous sequential circuit.	CO2	BTL-2
5.B	You are a digital circuit designer tasked with enhancing the robustness and reliability of a data storage unit in a critical aerospace control system. The data storage unit utilizes flip-flops to retain crucial information related to the system's state. The scenario involves the necessity for asynchronous inputs, particularly a reset functionality, in the flip-flop design. Illustrate the operation of such flip flop with asynchronous reset.	CO2	BTL-3
OR			
6	**Answer all Questions [5M + 6M = 11 M]**		
6.A	Compute the number of states and number of flip flops employed in a 3-bit counter.	CO2	BTL-2
6.B	You are tasked with designing a 3-bit circuit that is going through the following states: 000, 111, 010, 011, 100, 110, 101, 011 and back again. Identify the type of circuit.	CO2	BTL-3

*** END OF QUESTION PAPER ***