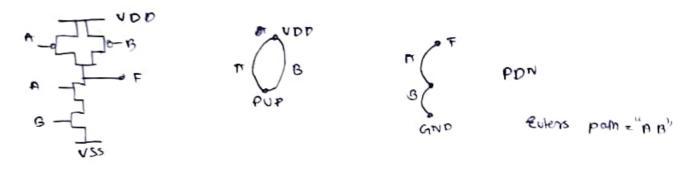
To make Shik diagram

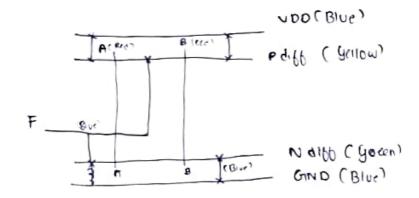
- (i) cmos logic gare > BE
- (Ti) Convert the error > graph
- citis EU140's path ( from the graph)
- (iv) Stick diagram

F = A .B



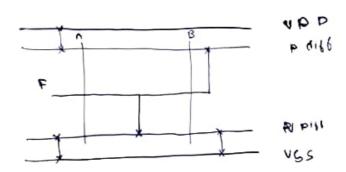
groph -> Verners > Node La Edga - Transistor

It should cover all nodes so mat it covers all nodes Eulias only once.



. NOR gate

F = A+B



## 

