Assignment 02

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1) The average power dissipated by a CMOS inverter can be attributed to three main sources:

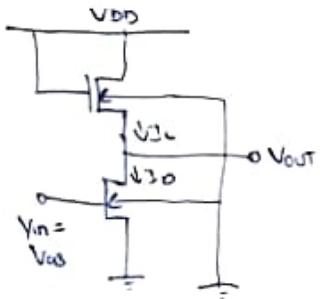
$P_T = P_S + P_D + P_{SC}$

P_S = Static power dissipation (due to leakage current)
P_D = Switching power dissipation
P_{SC} = Short circuit power dissipation

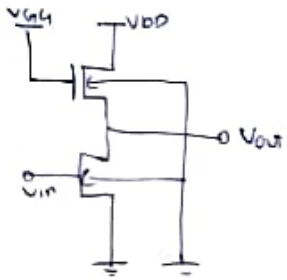
2) A linear load NMOS inverter offers advantages over a saturated load NMOS inverter with respect to noise margin and output voltage.

→ Higher output voltage →

In linear load NMOS V_{OH} (output) = V_{DD}
In saturated enhancement type NMOS O/P V = $V_{DD} - V_T$



Saturated enhancement type nmos load



Linear enhancement type load

3) $P_D = C_L V_{DD}^2 f$

$= 10 \times 10^{-6} \times 15 \times 15 \times 100 \times 10^6 = 225 \times 10^3$ W //

6) Assume scaling factor as S

$\frac{A}{2} = \frac{WL}{S^2}$

$S = \sqrt{2} = 1.414$

i.e transistor dimension improved (reduced) by 1.414

9) The dynamic behaviour of CMOS inverter during switching involves the charging and discharging of load capacitors. which leads to dynamic power dissipation

Factor affecting dynamic power dissipation
- Clock frequency
- Supply voltage
- Load capacitance

a) $t_{delay} = R \times C$

$= 50 \times 200 \times 10^{-5} = 100ps$

10) $t_{setup} = 1.5\,ns$

$t_{hold} = 0.5\,ns$

$t_{clk} = 4ns$

Timing margin $= T_{clk} - t_{setup}$

$= 4ns - 1.5\,ns = 2.5\,ns$

11) $t_{delay} = R_L C_L$

$= 500 \times 10^{-15} \times 70 = 100ps$

12) $Area_{new} = s^2 \times Area_{old} = (0.707)^2 = 0.5$

i.e Area reduced by 50%

$D_{new} = s \times D_{old}$

$= 0.707 \cdot D_{old}$

i.e Delay reduced 29.3%

13) $P_{new} = s^3 \times P_{old}$

$= (0.707)^3 = 0.354$

Power reduced by 0.354