Sense Amplifier Based High Speed Flip-Flop Design for Advanced Sub-Micron FinFET Standard Cell Library

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***Abstract*—A novel high-speed sense-amplifier based flip-flop is presented in this paper. The proposed flip-flop design has improved D2Q delay and a glitch-less output. An in-depth analysis of sense-amplifier stacking order is presented and the proposed sense-amplifier design exploit multiple stacking orders of the clocked devices, input and feedback transistor and show approximately 25% overall advantage in performance of the flop as compared to the conventional variant of a flip-flop. Simulation results were obtained for sub-micron FinFET technology using industry standard production characterization setup. Monte Carlo stress checks were performed on the proposed designs to ensure bug-free operation and high-yield at the time of fabrication.**

I. Introduction

High-performance flip-flop is an integral part of all the high-speed system-on-chip (SOC) designs which are heavily used in high-definition quantum-dot televisions, virtual/Augmented Reality consoles. In these high speed SOC's pipeline processing plays an vital role in determining the time taken from input to output. Because of large number of pipeline stages the flip-flop and its design has a significant impact on the performance and power of the chip. Hence a low-power and high-performance flip-flop design is required to improve the overall power, performance and area of an SOC. A Sense-Amplifier (SA) based flip-flop has nearly negative or zero setup time which helps in improving the overall D2Q delay of the design. Further, the True-Single Phase Clock (TSPC) nature of proposed flip-flop design has significant impact on SOC's clock power and CLK2Q delay.

A number of SA based flip-flop designs have been proposed and prior topologies are presented in [1] [2] [3] [4] have different types of output latches ranging from strong-ARM, NAND-based, hybrid combination of NAND-based and NC2-MOS etc. These output latches have been combined with the conventional NMOS based SA to obtain a flip-flop designs presented in the previous cases. In Fig.1, which uses the conventional design of SA, bridged transistor N6 connecting the two branches with N2 and N4 transistor makes the design vulnerable to failures at multiple iterations of vector checks which are necessary for standard cell usage. The prior designs shown in [1] [2] [3] [4] also fail for some of the effects of 6-sigma Monte-Carlo variation simulations and thus are not robust in nature. This robustness and vector check issue has been solved in [5] which uses a different feedback technique of using $\overline{S}$ and $\overline{R}$ signals instead of bridge transistor. This robust $\overline{S}$ and $\overline{R}$ based control logic strategy is used in all the further proposed designs.

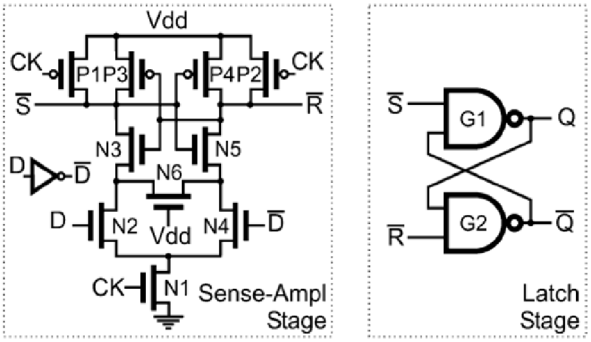

Fig. 1. NMOS Sense Amplifier based Flip-Flop

II. Analysis of Sense Amplifier Stacking Order

A. Existing Sense Amplifier based Flip-Flop Design

Fig.1 shows the existing design of a SA based flip-flop which uses an NMOS N6 transistor to make the design static in nature. SA feedback nodes $\overline{S}$ and $\overline{R}$ are pre-charged during the interval when clock signal is low. The high state of $\overline{S}$ and $\overline{R}$ keeps N3 and N5 on by charging their gates. When the CK signal is high depending on the input at N2 and N4 the state of $\overline{S}$ and $\overline{R}$ changes. The use of N6 is to prevent change of $\overline{S}$ and $\overline{R}$ signals if input changes when CK is high.

Two drawbacks of this prior art are that firstly, the slave latch used in the design is not suitable for standard cell libraries as it is area consuming in nature for higher drive cells. Secondly, technique to keep $\overline{S}$ and $\overline{R}$ stable for changes in data after the clock signal is high by using N6 NMOS device to make the flop static in nature is not a suitable for making this design usable for standard cell library.

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B. Lumped RC Modeling of the existing Sense Amplifier based Flip-Flop(SAFF) Design

RC modeling structure of the existing SAFF design shown in Fig.1 was analyzed. The analysis was performed to calculate the discharging time of $\overline{S}$ and $\overline{R}$ which plays a critical role in performance parameters such as CLK2Q delay. The lumped RC model of sense-amplifier master part is shown in Fig. 2. Now when CK goes high signals $\overline{S}$ and $\overline{R}$ discharges through N3,N2 and N1 or N5,N4 and N1 depending upon the input data condition.

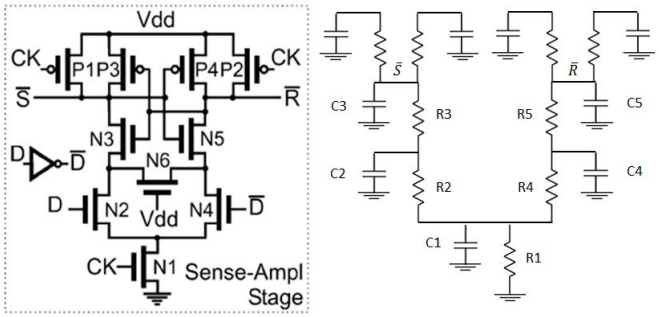

Fig. 2. Lumped RC model of sense-amplifier stage of flip-flop

According Elmore's delay model, discharging time of signals $\overline{S}$ and $\overline{R}$ is shown below:-

$$t_{f\overline{S}} = C1(R1) + C2(R1+R2) + C3(R1+R2+R3)$$
$$t_{f\overline{R}} = C1(R1) + C4(R1+R4) + C5(R1+R4+R5)$$

These $t_{f\overline{S}}$ and $t_{f\overline{R}}$ delays directly contribute to the overall delay of design. This discharging time has been optimized by changing the stacking order of clocked transistors, input data transistors and gating transistors. An in-depth study of SA stacking order is also discussed in next section to verify the results and access all other possible options.

C. Analysis of Sense Amplifier Stage Stacking Order

From the RC modeling of SA stage, it can be deduced that the stacking order of SA plays a very important role in overall performance of the design. Hence, a comparative analysis of SA stacking order was performed in which we have changed the stacking order of clock transistor (N1) abbreviated as C, data transistors (N2 and N4) abbreviated as D and gating feedback transistors (N3 and N5) abbreviated as N. Analysis of all the different stacking order variations have been compared according to their performance as shown in Table I.

TABLE I
POST-LAYOUT COMPARISON OF DIFFERENT SA STACKING ORDER WITH THE EXISTING DESIGN

Stacking Order	CLK2Q	Setup	D2Q
nMOS NDC	1x	1x	1x
nMOS NCD	0.951x	1.198x	0.989x
nMOS DCN	0.967x	0.895x	0.956x
nMOS CND	0.908x	1.213x	0.954x
nMOS DNC	0.995x	0.775x	0.953x
nMOS CDN	0.904x	1.107x	0.947x

It was observed that CDN was the most optimal stacking order for the SA stage due to the least discharging time due to least amount of parasitic capacitance that needs to be discharged after the clock signal CK goes high. This is due to the fact that all other capacitances in CDN have already discharged before the clock goes high as a discharging path is available during the CK low time interval for input and feedback transistors. For the optimal stacking order CDN, the discharging time $t_f\overline{S}$ and $t_f\overline{S}$ for the control signals $\overline{S}$ and $\overline{R}$ respectively is shown below:-

$$t_{f\overline{S}} = C3(R1+R2+R3)$$
$$t_{f\overline{R}} = C5(R1+R4+R5)$$

By changing the stacking order of SA stage CLK2Q delay, setup time and overall D2Q delay can be improved as compared to the existing design.

III. PROPOSED OPTIMAL STACKING SENSE AMPLIFIER BASED HIGH-SPEED FLIP-FLOP DESIGN

In the previous section, we have observed that the NAND-based latch is not suitable for standard cell libraries due to a significant high delay and its inability to be scaled to higher drive cells. Also, the stacking order of sense-amplifier stage plays a crucial role in total CLK2Q or D2Q delays which directly impacts the overall performance of the design.

A. Latch Design

The most optimal design for an output latch was decided based on a number of iterations which involved changing the feedback inverter position, stacking of forward path, choice of control signals based on sharing of devices in layout of the design etc. The final latch showed minimum delay, power, area amongst the options explored and also has the capability to be extended for higher drives by increasing the number of fingers of output inverter. Latch design which will be used with the proposed sense-amplifier stage is shown in Fig.3.

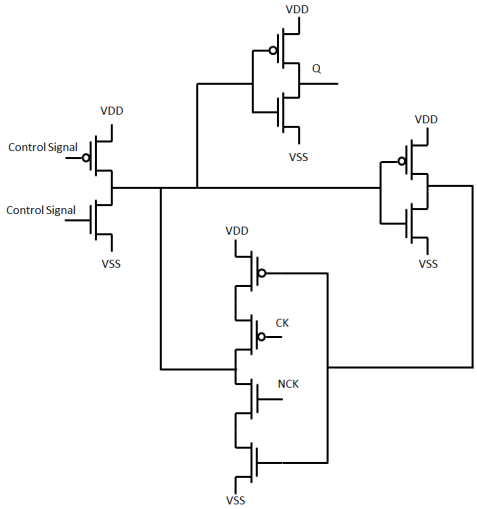

Fig. 3. Latch Design suitable for Standard Cell Library

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Fig.3 has single stack delay after the control signal $\overline{S}$ and $\overline{R}$ and has output inverter which provides glitch-free output signal and ability to extend to higher drive by increasing the output inverter fingers.

B. True-Single Phase NMOS Sense Amplifier based Flip-Flop

True single clock phase positive edge triggered NMOS sense amplifier based flip-flop is shown in fig.4 in which latch design is used according to the standard cell library specifications and the optimal stacking order of the sense amplifier stage has been used. Clock signal load is reduced by changing the clock signals in latch feedback by the control signal $\overline{S}$ and $\overline{R}$ so that block level clock signal is not degraded due to the standard cell clock load. Sizes of all the transistors have been optimized to achieve maximum performance in the minimal layout area. Sub-micron FinFET layout of the proposed design has been extracted and parasitics netlist has been used for all the simulations.

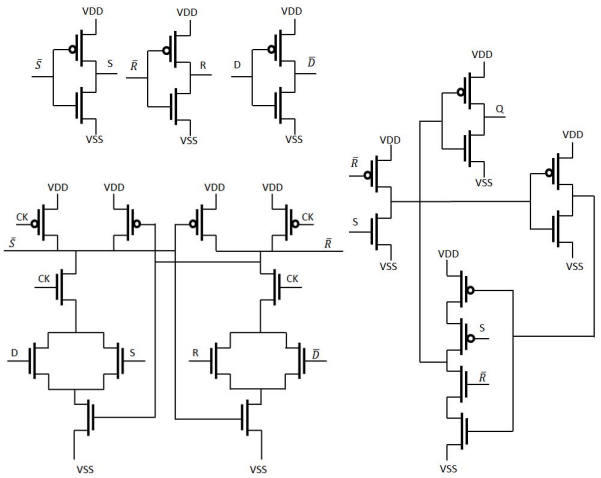

Fig. 4. Proposed optimal stacking NMOS Sense-Amplifier based Flip-Flop

C. PMOS Sense Amplifier based Flip-Flop

PMOS based stacking version of sense amplifier stage has been shown which uses the negative edge of clock and further reduces the clock load. The PMOS sense amplifier based flip-flop with optimal stacking and better latch design is shown in Fig.5. Sub-micron FinFET layout of the proposed PMOS design has been extracted and the parasitics netlist has been used for all the simulations.

IV. Low-Voltage Monte-Carlo Simulations

Monte-Carlo simulations were performed on the proposed designs to ensure robust performance at low voltages. Three major type of simulations i.e. Data-Write, Data-Hold, Data-Corruption with power glitches were performed on a number of combinations of process, voltage, temperature (PVT) and sigma-variations. All the three major types of simulations have been briefly discussed below:-

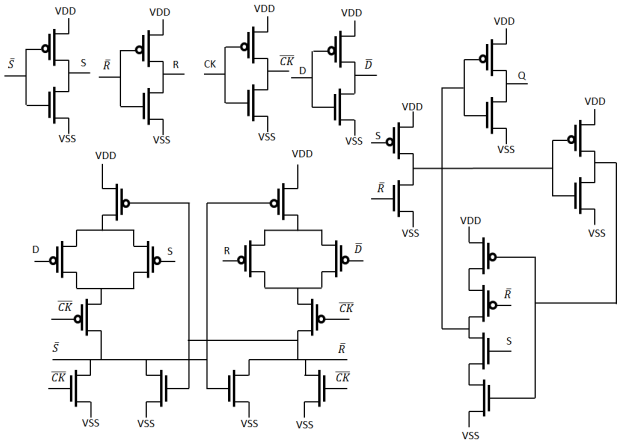

Fig. 5. Proposed optimal stacking reduced clock load PMOS Sense-Amplifier based Flip-Flop

A. Data-Write

Data-write is the ability to write the data to the output latch of the flip-flop with reliability at the intended clock edge. In Fig.6 the possible error cases with respect to positive edge triggered flip-flop have been presented, In the error case 1 and 2 data is written earlier than the intended clock edge and error cases 3 and 4 the data write ability failure where the correct data is not written in the output latch even at the proper clock edge.

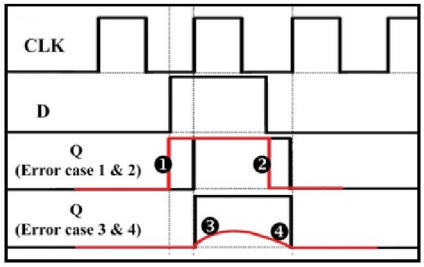

Fig. 6. Error Possibilities in Data Write

B. Data-Hold

Data-hold corresponds to data stability post intended clock edge. In Fig. 7, the error case 1 and 2 show output data change possibility because of change in input. Error case 3 depicts the possibilities of glitches at the output node (Q). Error case 4 shows the erroneous much delayed output beyond the acceptable transition time.

C. Data-Corrupt

In Fig. 8, few instances of stored data corrupt because of disruption in power supply i.e. glitches in power supply. Sometimes, in order to reduce power consumption, operating voltage is lowered in case of low activity in the circuits. In such cases, it is required to ensure the integrity of the stored data in the output latches. Error case 1 and 2 shows that the output

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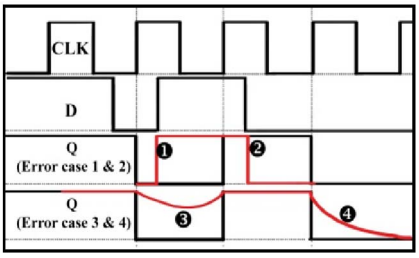

Fig. 7. Error Possibilities in Data Hold

data flips even at the negative clock edges when the output voltage is lowered or if there is an unwanted glitch observed in the power supply. The error case 3 and 4 show output data glitch beyond an acceptable range because of power supply disruption.

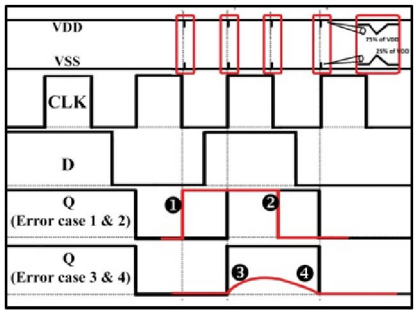

Fig. 8. Error Possibilities in Data Corrupt

The proposed designs were checked for a different Process, Voltage and Temperature conditions and the results are shown in Table II. Both the proposed designs show robustness up to the voltage of 0.5 which is typical voltage for most of the 10nm process across foundries.

TABLE II
NUMBER OF MONTE-CARLO SEEDS FAILED AT A PARTICULAR COMBINATION OF PROCESS, TEMPERATURE AND VOLTAGE

Monte Iterations = 5000	Low-Voltage Monte-Carlo Checks						
Process:- SSP, FFP, SF, FS Temperature:- m40c and 125c	Sigma	0.5	0.6	0.7	0.8	0.9	1.0
Proposed Optimal Stacking NMOS Sense Amplifier based Flip-Flop	3	0	0	0	0	0	0
	4.5	0	0	0	0	0	0
	6	0	0	0	0	0	0
Proposed Optimal Stacking PMOS Sense Amplifier based Flip-Flop	3	0	0	0	0	0	0
	4.5	0	0	0	0	0	0
	6	0	0	0	0	0	0

V. SIMULATION RESULTS

Post-layout simulation of all the proposed designs have been performed at the delay($SS\{Slow, Slow\}\_0.9V\_m40C$) and leakage($FF\{Fast, Fast\}\_1.1V\_125C$) PTV using siliconsmart tool and the results have been compared with the existing SA topology of the flip-flop is shown in Table III.

From the results in Table III, it is clearly evident that D2Q delay (CLK2Q delay + setup time) shown an improvement as compared to the existing SAFF design. D-to-Q delay of the proposed design has improved by 25% across different PVT conditions.

TABLE III
POST-LAYOUT SIMULATION RESULTS OF PROPOSED DESIGNS

CellName	Leakage	CLK2Q	Setup Time	D2Q	Area	Hold Time
Reference	1x	1x	1x	1x	1x	1x
NMOS Sense Amplifier based Flip-Flop	0.90x	0.904x	1.107x	0.95x	1x	0.99x
PMOS Sense Amplifier based Flip-Flop	1.02x	0.864x	0.084x	0.75x	1.05x	1.19x

VI. CONCLUSION

A new and improved variant of a SAFF has been developed and tested in different PVT conditions. The proposed design with its split clock and most optimal stacking in the SA stage shows significant performance benefit as compared to the existing reference topology being used in the industry. Another version of rising edge triggered SAFF has also been proposed which uses a PMOS based design to achieve similar results. The two designs proposed in this paper use differential input signal nature of design which makes it compatible with the logic utilizing reduced signal swing. The designs have been customized to fit for standard cell library usage with carefully placed inverters to make the design robust for all PVT conditions. Further, the performance of flip-flop improved by most optimal sizing for the design which is complaint with the layout requirements. Measurement results place proposed designs on the top in terms of speed as compared to other flip-flops used in high-end image processing SOC's and Application Processors (APs) for number of consumer electronics products.

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