Variability Analysis of Sense Amplifier for FinFET Subthreshold SRAM Applications

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***Abstract*—This paper investigates the impact of intrinsic random variability on the robustness of sense amplifier (SA) for fin-shaped field-effect transistor (FinFET) subthreshold static random access memory (SRAM) applications. We employ a model-assisted statistical approach to consider both fin line edge roughness (fin LER) and work function variation, which are regarded as the major variation sources in an advanced FinFET device. Our results indicate that fin LER dominates the overall variability of subthreshold SA robustness and sensing margin. In addition, it is observed that the offset voltage (V_{OS}) of current latch SA calculated solely from threshold voltage (V_T) mismatch underestimates the actual variation and is shown to be optimistic. For large-signal single-ended inverter sensing, we find that sense "0" hinders the allowable sensing margin and needs to be carefully designed. Compared with bulk CMOS, the superior electrostatic integrity and variability of FinFET enhance the feasibility of differential sensing in subthreshold SRAM applications.**

***Index Terms*—Fin-shaped field-effect transistor (FinFET), sense amplifier (SA), subthreshold circuit, variability.**

I. Introduction

DUE TO its superior gate control and variability immunity, fin-shaped field-effect transistor (FinFET) has demonstrated satisfactory scalability and feasibility for mass production beyond the 22-nm technology node [1]. The improved I_{ON}/I_{OFF} ratio and reduced leakage current of FinFET also facilitate subthreshold circuit design for ultra-low-power applications [2]. Due to ever-increasing capacity requirements, static random access memory (SRAM) cells are usually designed with minimum-size or sub-groundrule devices and suffer severe impact from variability, particularly in an ultra-low-power subthreshold operation. Several novel cell structures have been proposed to replace the conventional 6 T SRAM cell for subthreshold applications [3]–[5]. The adoption of a FinFET device for subthreshold SRAM applications has been shown in [5]–[7] to exhibit significant advantages in cell stability and variability compared with the planar bulk counterpart.

Fig. 1 illustrates the schematic of a simplified SRAM array in the READ operation. In addition to the robustness of SRAM cell, the functionality of the sense amplifier (SA) determines the correctness of the sensing action [8], [9] and merits detailed investigation. Compared with our previous work in [7] and [8], an improved variability analysis with a model-assisted statistical approach is carried out to efficiently consider multiple variation sources [fin line edge roughness (fin LER) and work function variation (WFV)] simultaneously for evaluating the robustness of subthreshold FinFET SA. For the variation sources considered in this work, fin LER is found to greatly influence the robustness of subthreshold SA. In addition, the use of multiple-fin design in subthreshold SRAMs to improve the cell stability [6] and sensing margin [8] is found to be marginal and increases the total area. Hence, in this study, our analysis is based on single-fin FinFET with $L_{eff} = 25$ nm, $W_{fin} = 7$ nm, $H_{fin} = 20$ nm, and EOT $= 0.65$ nm on the SOI substrate (relevant geometries are defined in the inset of Fig. 3). In addition, the values of mobility have been calibrated with the measured 25-nm gate-length FinFET transistor [10] and the threshold voltage for NMOS/PMOS is designed around ± 0.45 V for the subthreshold operation. The remainder of this paper is organized as follows. Section II describes the framework of the model-based approach used in this study. With the established framework, two commonly used SAs, the current latch SA (CLSA) and large-signal single-ended inverter, are investigated in the presence of random variations in Section III. Finally, the conclusion is drawn in Section IV.

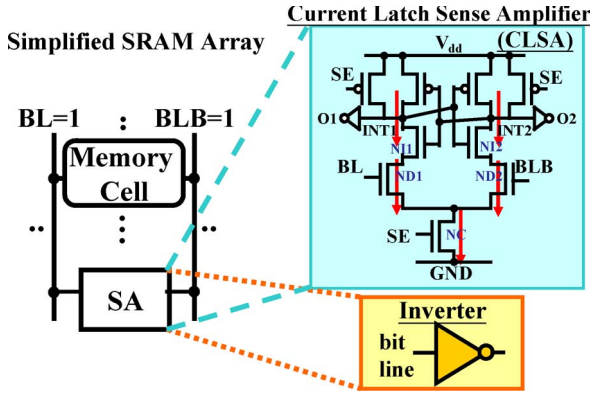

Fig. 1. Schematics of SRAM array in the READ operation and the sense amplifiers considered in this work.

II. Framework of the Model-Based Statistical Approach

Two SAs evaluated in this work are shown in Fig. 1: 1) small-signal differential sensing using CLSA [11] and 2) large-signal single-ended inverter sensing. For CLSA,

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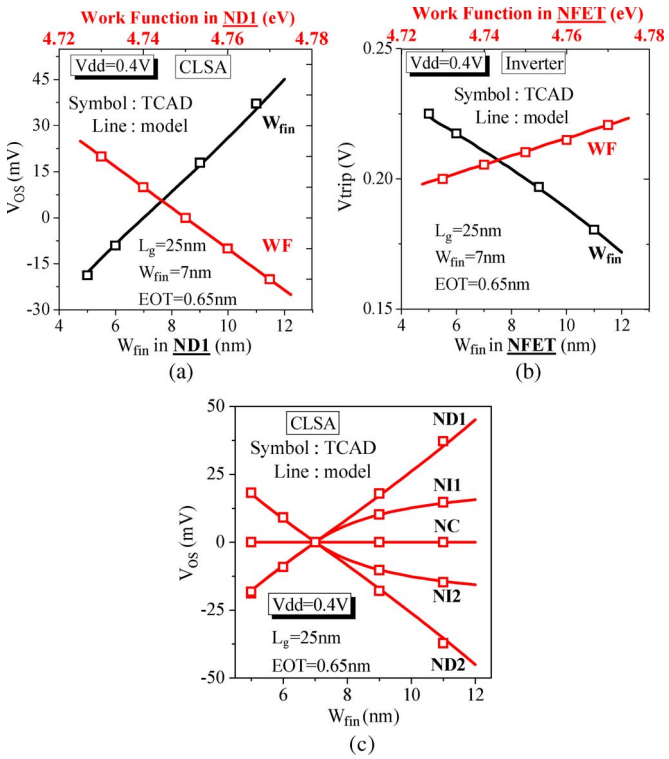

Fig. 2. Verifications of (a) V_{OS} and (b) V_{trip} model for CLSA and the inverter sense amplifier, respectively. The values of W_{fin} and work function are varied in ND1 (for CLSA) and pull-down NFET (for inverter) devices. (c) The impact of individual W_{fin} sensitivity on CLSA V_{OS}. Our models exhibit satisfactory accuracy with errors smaller than 3 mV for the cases studied.

the high-going sense enable (SE) signal activates CLSA as bit-line/bit-line bar (BL/BLB) differential voltage reaches the specified value that should be larger than the input offset voltage (V_{OS}, due to current mismatch between two branches) of CLSA [12]. For large-signal single-ended sensing, an inverter is employed to sense either the BL or BLB signal.

Using the subthreshold drain current model reported in [13], the V_{OS} can be calculated by solving Kirchhoff's current law at all possible nodes in CLSA while considering possible device variations. The value of BL (or BLB) is then iteratively solved to balance the currents between two branches. For the inverter SA, Kirchhoff's current law is applied in the output node with various input voltages to construct the voltage transfer curve [6] and find the corresponding trip voltage (V_{trip}). Fig. 2 shows the verification of the accuracy of our model in describing the W_{fin} and work function (WF) dependencies. As can be seen, our models exhibit excellent agreement with technology computer-aided design (TCAD) mixed-mode simulations for the cases studied. In this paper, we consider the impact of static current mismatch due to variability and ignore the contribution of parasitic capacitance fluctuations.

Fig. 3 shows the $I_d - V_g$ dispersion of FinFET MOSFET using TCAD atomistic Monte Carlo simulations [14] accounting for fin LER and WFV simultaneously. Due to the long computation time and computational resources required in 3-D TCAD atomistic simulations, the sample size used in this work is limited to 200, which has been shown to be adequate and is commonly used for TCAD statistical assessments [15]. Fin LER, resulting from the rough line edge pattern along the

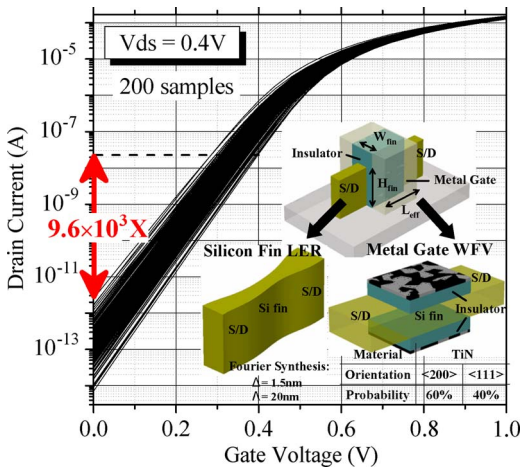

Fig. 3. The distribution of $I_d - V_g$ characteristics of FinFET considering fin LER and WFV simultaneously. The inset shows the geometry definitions of SOI FinFET and the variation sources considered in this work.

channel length, are considered by the Fourier synthesis approach with correlation length $(\Delta) = 20$ nm and RMS amplitude $(\Lambda) = 1.5$ nm [15]. In addition, due to the variation in grain size and grain orientation, the resulting WF differs from device to device, resulting in V_T variations [16], [17]. To assess WFV, the poly-grain pattern in the metal-gate stack (Fig. 3) is randomly generated with the assigned grain size and probability for different grain orientations [18]. It can be seen that at $V_{dd} = 0.4$ V, a satisfactory I_{ON}/I_{OFF} ratio (9.6×10^3) is observed under the worst-case condition. Based on the simulated fin LER and WFV dispersions, the approach in [7] is applied to build model libraries for the variability analysis of subthreshold FinFET SAs. In the subthreshold region, device subthreshold swing (S.S.) and OFF-state current (I_{OFF}) are used to calibrate individual FinFET characteristic from the distribution of fin LER and WFV. For fin LER with an irregular fin pattern (Fig. 3), the $I_d - V_g$ characteristics can be described by a set of effective fin width (W_{fin}) and effective WF that produce the same S.S. and I_{OFF} as that from TCAD atomistic simulations. Using a similar approach as in [7], Fig. 4 demonstrates the calibrations of the model library in terms of S.S. and I_{OFF} with excellent accuracy across the distribution caused by fin LER.

To create the model library for WFV, a planar single-gate device with a gate area identical to the area of FinFET sidewall gate is simulated, and the drain current dispersion is shown in Fig. 5. Because WFV does not impact device electrostatic integrity directly (while fin LER does), the observed S.S. variation is negligible and the V_T difference with respect to the nominal case alone can be used to build the model library. For FinFET with double sidewall gates, the value of WF for each gate is sampled independently from the library to emulate the actual case with both gates suffering WFV.

III. Analysis of Subthreshold FinFET SA

With the model libraries, the influences of device variability on SA robustness are analyzed in this section. As can be seen in Fig. 6(a), the proposed model-assisted statistical approach

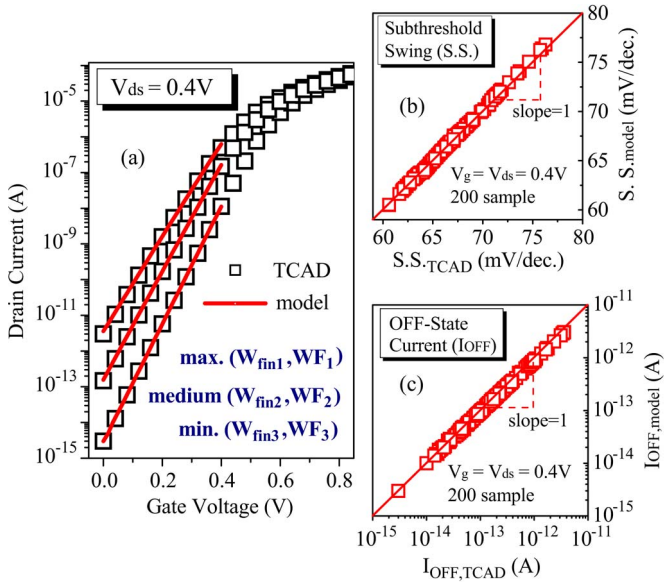

Fig. 4. Calibration of the model with TCAD atomistic simulations to build the library for fin LER at (a) three extreme cases, and the error analysis of (b) S.S. and (c) I_{OFF} for each device.

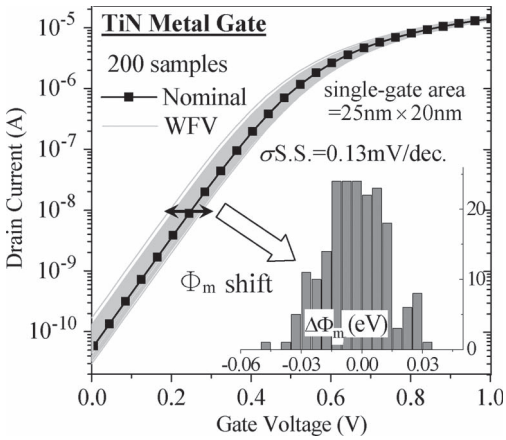

Fig. 5. Calibration of WFV-induced effective $\Phi_m(V_T)$ shifts for TiN metal gate with the optimized grain size (3 nm). The single-gate MOSFET with gate area identical to one of the FinFET sidewall gate is simulated in this work.

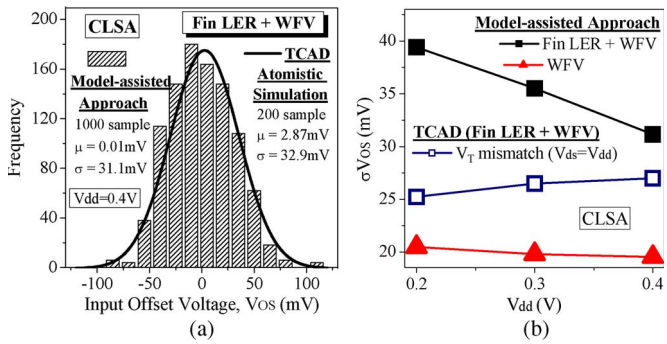

Fig. 6. (a) Comparison of V_{OS} variation between TCAD atomistic simulations and model-assisted approach considering fin LER and WFV and (b) the V_{OS} variation at various V_{dd}.

shows fairly good agreement with TCAD mixed-mode simulations in describing the V_{OS} dispersion at $V_{dd} = 0.4$ V. Fig. 6(b) compares the values of σV_{OS} between three different

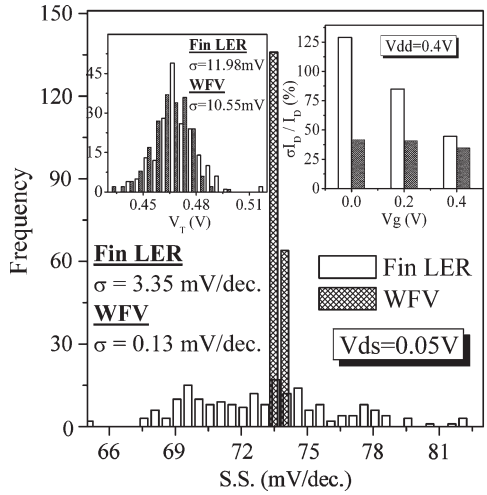

Fig. 7. Comparisons of V_T, I_D, and S.S. fluctuations. Fin LER dominates FinFET overall variations due to its larger S.S. variation in the subthreshold region.

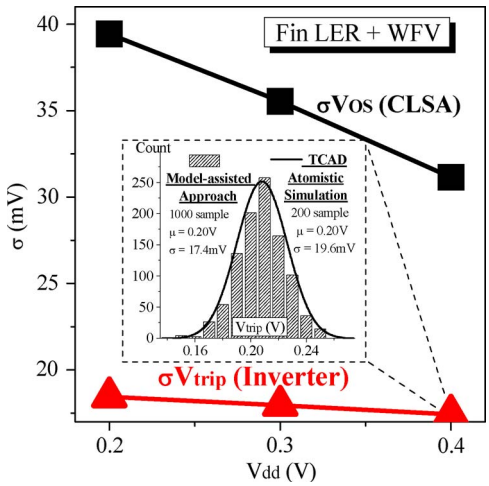

Fig. 8. Variability comparison of CLSA and inverter sense amplifier. The inset verifies the V_{trip} distribution between TCAD simulation and model-assisted approach at $V_{dd} = 0.4$ V.

approaches at various V_{dd}. In addition to the V_{OS} variations calculated from the model-assisted approach, the V_T mismatch between the ND1/ND2 transistors (see Fig. 1) is calculated and used to approximate the actual V_{OS} variations in the presence of fin LER and WFV. It is found that the model-assisted approach considering both fin LER and WFV exhibits larger V_{OS} variation and stronger V_{dd} dependence, whereas negligible V_{dd} dependence and less impact are observed for the case considering WFV only. Furthermore, opposite V_{dd} dependence is observed for the case using V_T mismatch alone, which also significantly underestimates σV_{OS}, particularly at lower V_{dd}. This can be explained in Fig. 7, which shows the device-level comparisons of S.S., V_T, and I_D variations induced by fin LER and WFV in the subthreshold region. It can be seen that the V_T variations from fin LER and WFV are comparable. However, the degraded S.S. fluctuation caused by fin LER results in larger drain current variation ($\sigma I_D/I_D$ in the inset of Fig. 7) and the variation becomes significantly worse with the decreasing gate voltage (deeper subthreshold), leading to the obvious increase

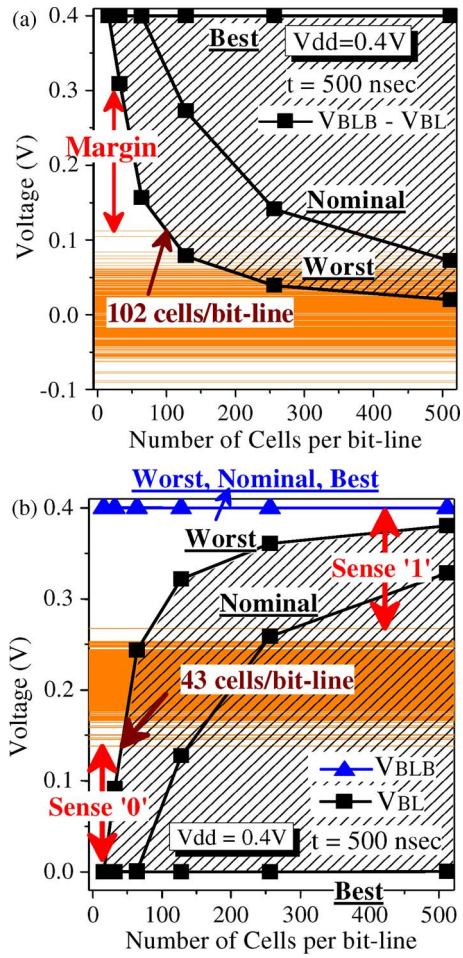

Fig. 9. The determinations of the sensing margin for (a) differential CLSA and (b) large-signal inverter sense amplifier. The horizontal orange lines represent the dispersions of (a) V_{OS} and (b) V_{trip}.

in σV_{OS} (using model-assisted approach) with decreasing V_{dd}. In Fig. 8, V_{trip} variations (for inverter) are assessed and compared with σV_{OS} (for CLSA). It can be seen that the inverter SA exhibits better variation immunity ($\sigma V_{trip} < \sigma V_{OS}$).

Similar to the methodology in [8] and [19], in this work, the extreme bit-line voltages during the READ operation are determined by the conventional 6T SRAM cells with least/nominal/most "cell" READ and Standby leakage currents for the analysis of the sensing margin and performance. To evaluate the possible bit-line voltages, the worst-case data pattern where all unselected cells have identical data opposite to that in the selected cell is investigated. The calculated bit-line voltages are shown in Fig. 9 for differential CLSA and large-signal inverter sensing schemes at $t = 500$ nsec. In addition, the calculated V_{OS} and V_{trip} dispersions are applied to determine the allowable sensing margins. For CLSA, in order to correctly sense the signal, the values of the BL/BLB differential voltage should be larger than the maximum of the V_{OS} dispersion. Thus, the differential sensing scheme can afford up to 102 (i.e., 64) cells per bit-line. For large-signal sensing in Fig. 9(b), sense "0" and "1" margins are defined as the voltage difference between the BL/BLB levels and inverter V_{trip}. To ensure the correct sense "0" operation, the low-going BL voltages must be lower than the minimum of V_{trip} dispersion, while the "high-held" BLB

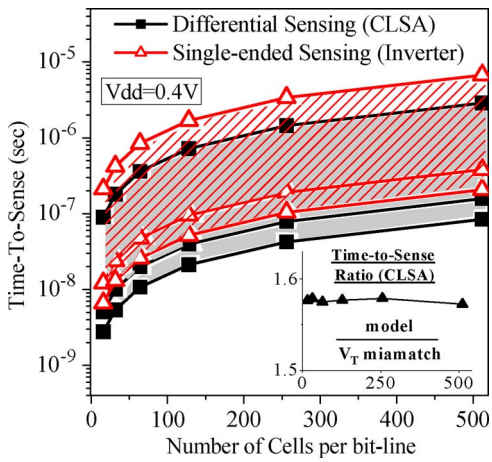

Fig. 10. Performance comparison of differential (CLSA) and large-signal (inverter) sensing schemes at $V_{dd} = 0.4$ V. The inset shows the ratio of Time-To-Sense using model approach and merely V_T mismatch method to determine V_{OS} for CLSA. The Time-To-Sense is defined as the time required to develop viable margin for a certain number of cells per bit-line.

voltage should stay above the maximum of the V_{trip} dispersion for correct sense "1" action.

The "high-held" BLB voltage is held by the pull-up PMOS (which holds the cell "1" storage node) and access NMOS of the selected cell. Due to the superior I_{ON}/I_{OFF} ratio in the FinFET device, the leakage through the "OFF" access transistors of unselected cells on the selected bit-line has limited impact on the sense "1" margin. On the other hand, as the "low-going" BL voltage is pulled down, the READ current from the selected cell decreases and eventually vanishes, whereas the leakage through the "OFF" access transistors of unselected cells on the selected bit-line increases due to larger V_{DS} across the "OFF" access transistors. As such, the sense "0" margin is significantly worse than the sense "1" margin, and the low-going BL voltage exhibits larger dispersion. This can be clearly seen in Fig. 9 where the worse sense "0" margin limits the allowable number of cells per bit-line (43, i.e., 32, cells in this case).

Fig. 10 compares the Time-To-Sense (defined as the time required to develop viable margin for a certain number of cells per bit-line) among two SAs for different number of cells per bit-line. As expected, the large-signal sensing scheme requires longer Time-To-Sense (poor performance) than the differential CLSA sensing. However, the difference between the CLSA and inverter SA is insignificant. The result validates the feasibility of small-signal differential sensing for the FinFET subthreshold SRAM applications. The inset of Fig. 10 also shows the ratio of Time-To-Sense using model and V_T mismatch approaches to determine the value of V_{OS} for various numbers of cells per bit-line. The larger V_{OS} variation predicted by the model-assisted approach reduces the sensing margin, thus requiring longer Time-To-Sense compared with the case using merely V_T mismatch. As such, the performance is overestimated by about 57% using V_T mismatch method, and longer SE time is necessary to ensure correct sensing operation.

IV. Conclusion

We have employed a model-based statistical framework to efficiently evaluate the robustness of FinFET SAs in the presence

of multiple variation sources. Our results indicate that fin LER dominates over WFV in the subthreshold region and the impact increases with decreasing V_{dd}. It is also observed that for CLSA, the offset voltage calculated solely from the threshold voltage mismatch underestimates the actual dispersion, and the error will increase with decreasing V_{dd}. For large-signal inverter sensing, a sense "0" margin limits the overall sensing margin and a flexible fin height design [20] to increase the trip voltage is a possible method to improve the margin. In summary, the superior electrostatic integrity and better immunity to device variability of FinFET render small-signal differential sensing scheme viable for FinFET subthreshold SRAM applications.

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