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Low Power, High Performance PMOS Biased Sense Amplifier

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***Abstract* - Sense amplifiers plays a significant role in terms of its recital, functionality and reliability of the memory circuits. In this paper two new circuits have been proposed. The proposed circuit is PMOS biased sense amplifier, which provides very high output impedance and has reduced sense delay and power dissipation. As such, the proposed circuit performs the identical operations as that of conventional circuits but with the reduced the sense delay and power consumption. The suggested sense amplifiers overall performance have been simulated and examined using Cadence virtuoso with gpdk 180 nm library parameters.**

Keywords*: *low power; high performance; sense delay; sense amplifier.

I. Introduction

In any digital logic design memories are the most important blocks in DSP, microprocessors, microcontrollers, and computers. Audio players, digital cameras stores the data in the form of images, audio, video, speech in a flash memory should have less power with the display of memory capacity performance on high side on a single chip. Low sensing delay and increased higher capacities are required for improved quality of stored data. In order to accomplish the towering rate of staging, sense amplifiers [1] are customarily applied to amplify the very small voltage difference on the bit lines at congruous sense timings [2-11]. If the sense amplifiers enable signal is asserted early, the SA cannot amplify the minuscule voltage difference accurately. The overhead of access time and power consumption is incremented if the SAE is asserted tardy. Consequently, the optimum timing for SAE is critical for a high-speed and low-power SRAM cell [12-21].

One of the most consequential parts is a sense amplifier in memories [22]. Access time of memory is mostly recognized by the sense amplifier. If any changes in the bit-lines noticed, the signals are amplified and delivers the stored memory data. It is a challenge for any designer to design the fast, low power sense amplifier [23-25] mainly in the area of submicron CMOS technologies. In the present days, memory bit lines are the main cause of extra signal delays in terms of capacitance. If the channel length is small, the signal voltage gain also reduces all these problems and are eliminated by sensing the current signal instead of voltage signals [26-30]. For low voltage, high speed and large memories the current sensing approach is the right choice [31-38]. Why because there will be no large voltage swing on the bit-lines which are needed.

II. PMOS Bias Type Sense Amplifiers

A. Sense Amplifier Circuit-1

The proposed circuit-1 provides high output impedance, no static error. In this proposed circuit (Fig. 1) the gate terminals of T_1, T_2 and T_{17} are short circuited and I_R is greater than I_C then there is a slight difference of current flowing through both bit lines. So the current I_1-I_d will flows through the bit-line BL_2 and current I_1 will flows through the bit-line BL_1.

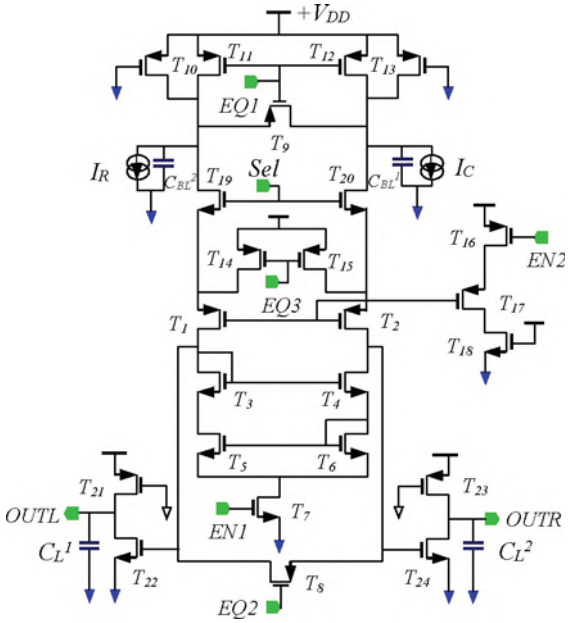

Fig. 1. Proposed sense amplifier circuit-1

Transistor pairs T_3-T_4 and T_5-T_6 are exactly coincided. So, input and output potentials are approximately the same, then in principle the input and output currents are equal. Number of transistors is reduced and compared to the conventional

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type of sense amplifiers. Therefore, sense delay and power dissipation gets reduced.

The conventional PMOS bias type sense amplifier has more number of transistors and power consumed is also higher side. The projected sense amplifier is shown in Fig. 1. *OUTL* is taken across T_1 and T_3 and *OUTR* across T_2 and T_4. The modified sense amplifier reduces the power consumption and sense delay.

B. Sense Amplifier Circuit-2

The second proposed sense amplifier is shown in Fig 2. *OUTL* is taken across T_1 and T_5 and *OUTR* across T_2 and T_6. The modified sense amplifier reduces the power consumed and sense delay [13], [17], [20].

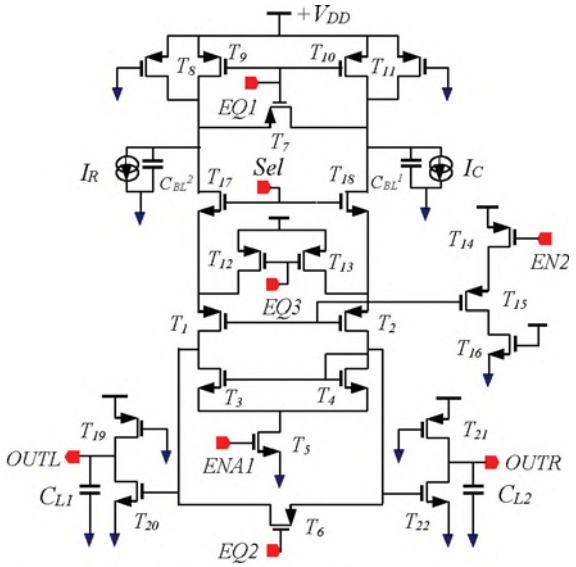

Fig. 2. Proposed sense amplifier circuit-2

III. Simulation Results

Simulation has been done by using 180 nm CMOS technology using the Cadence Virtuoso Tool. All the simulations were carried out keeping the same fan-in and fan-out. The transistors in current mirror included in Fig. 1 sense amplifiers are of equal size, W/L = 0.9 µm/0.18 µm. The current I_R indicates the memory and I_C indicates the current for the reference cell. The currents 10 µA and 1 µA were given to I_R and I_C. At the output nodes the load capacitance used was 50 fF and at bit-lines the capacitance used to be 1 pF.

The performance of the sense amplifier is mostly dependent on bit-line capacitances. The transient analysis for the proposed sense amplifier-1 is shown in Fig. 3. Sensing delay against different supply voltages ($+V_{DD}$) at 27^0 C and 125^0 C of Fig. 1 is shown in Fig. 3. When the supply voltage $+V_{DD}$, increases from +1 V to +3 V, the sensing delay is decreased, which is given in Fig. 4 graph.

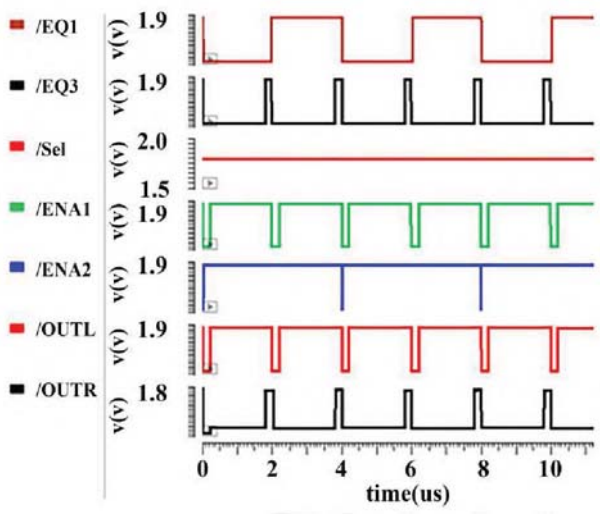

Fig. 3. Transient analysis of proposed circuit-1

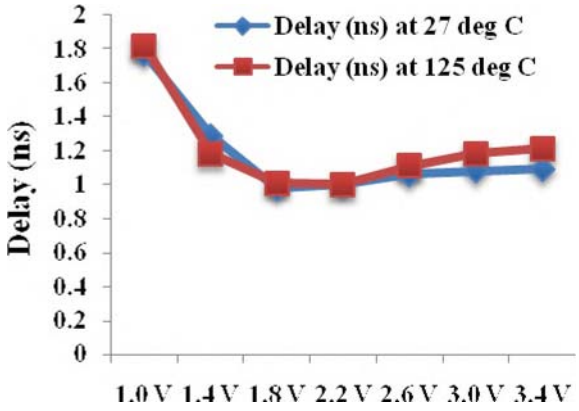

Fig. 4. Sensing delay time Vs different voltages ($+V_{DD}$)

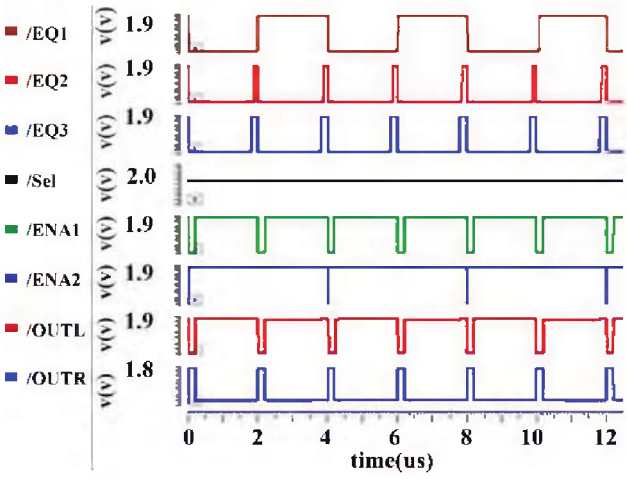

Fig 5. Transient analysis of proposed circuit-2

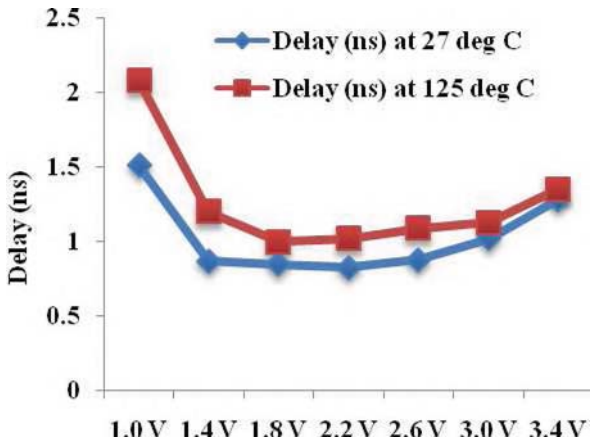

Fig. 6. Sensing delay time Vs different voltages ($+V_{DD}$)

The transient analysis for second sense amplifier-2 is shown in Fig. 5. Sensing delay against $+V_{dd}$ at 27^0 C and 125^0 C of Fig. 2 is shown in Fig. 6. When $+V_{dd}$ increases from +1 V to +3 V the sensing delay is decreased, which is given in graphs.

IV. Conclusion

Two new sense amplifiers were designed using Cadence 180 nm CMOS Technology and the transient results of the proposed sense amplifiers were congruent with the theoretical analysis. Also, the graph is drawn for a simulated sensing delay at different supply voltages. The proposed circuits have less number of transistors, so that sensing delay and power dissipation are also reduced. The simulated power dissipation of the proposed circuit-1, and proposed circuit-2 are 80.05 µW and 35.9 µW respectively.

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