

# Power-Efficient FinFET Based Sense Amplifier

**MAJOR PROJECT REPORT**

**BY**

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*in partial fulfillment for the award of the degree*

*of*

*Bachelor of Technology*

*In*

*Electronics & Communication Engineering*

**Under the Guidance of**

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***&***

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## DECLARATION

We hereby declare that the project entitled “Power-Efficient FinFET Based Sense Amplifier

“Which is being submitted as Major project of 4th semester in Electronics & Communication Engineering Aziznagar, Hyderabad in authentic record of genuine work done under the guidance of Assistant Professor **Mr. Ngangbam Phalguni Singh &Mr. Vijay Rao Kumbhare** department of Electronics & Communication Engineering Aziznagar, Hyderabad.

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## CERTIFICATE

This is certified that the Major project report entitled “Power-Efficient FinFET Based Sense Amplifier” is being submitted by Sayooj, Sameer, Venkat Prasad, has been a carried out under the guidance of Assistant Professor **Mr. Ngangbam Phalguni Singh &Mr. Vijay Rao Kumbhare** Electronics & Communication Engineering Aziznagar Hyderabad. The project report is approved for submission requirement for VLSI-Design project in 4th semester in Electronics & Communication Engineering Aziznagar Hyderabad.

Internal Examiner External Examiner

Date:

Head of the Department

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**Date: 1. Sayooj**

**2.Sameer**

**3.Venkat Prasad**

**Abstract:**

This research delves into the critical challenge of power dissipation in sense amplifiers for low-voltage Static Random-Access Memory (SRAM) and proposes a novel, highly power-efficient architecture leveraging the unique advantages of Fin Field-Effect Transistor (FinFET) technology. The increasing density and portability of electronic devices necessitate substantial reductions in memory power consumption, making the optimization of sensing circuits paramount. This study meticulously analyzes the limitations of conventional CMOS sense amplifiers at scaled technology nodes and low supply voltages, n /o;p’[highlighting issues such as increased subthreshold leakage and diminished noise margins. To address these challenges, a specific FinFET-based sense amplifier design, incorporating [mention a specific technique and briefly explain its mechanism, e.g., a dynamically biased differential amplifier with conditional pre-charging to minimize unnecessary switching], is presented. Comprehensive simulations are conducted using industry-standard [mention specific simulation tools like HSPICE, Spectre, or Synopsys Custom Compiler] and accurate FinFET device models for a [mention specific technology node, e.g., 7nm or 5nm] process to rigorously evaluate key performance parameters. These parameters include static and dynamic power consumption under various operating conditions, sensing delay, input-referred offset voltage, noise sensitivity, and robustness against process variations through statistical analysis. The simulation results are anticipated to demonstrate a significant reduction in power dissipation, potentially by [quantify with an expected percentage if possible], compared to traditional CMOS counterparts, while maintaining competitive speed and enhanced stability for reliable operation in low-voltage SRAM environments.

**1. Introduction:**

The relentless pursuit of miniaturization and enhanced functionality in modern electronic systems, particularly in mobile, wearable, and Internet of Things (IoT) devices, has placed stringent demands on energy efficiency across all integrated circuit components. Static Random-Access Memory (SRAM) serves as a cornerstone of on-chip data storage, providing the speed necessary for critical operations. However, as feature sizes shrink according to Moore's Law, and supply voltages are aggressively scaled down to conserve power, the design of robust and energy-efficient SRAM peripheral circuits, most notably sense amplifiers, becomes increasingly complex. Sense amplifiers are indispensable for accurately and rapidly discerning the small differential voltage developed on the bitlines during a memory read operation and amplifying it to a full logic level. Their performance directly dictates the minimum operating voltage, read access time, and overall power consumption of the SRAM.

Conventional bulk CMOS-based sense amplifier designs encounter significant limitations at advanced technology nodes. Increased subthreshold leakage currents contribute substantially to static power dissipation, while reduced voltage swings and heightened susceptibility to process variations compromise sensing accuracy and speed. Fin Field-Effect Transistors (FinFETs), with their unique three-dimensional channel structure, offer superior gate control over the channel, leading to a steeper subthreshold slope, reduced drain-induced barrier lowering (DIBL), and significantly lower subthreshold leakage compared to planar MOSFETs. These inherent advantages make FinFET technology an attractive and increasingly adopted platform for designing high-performance, low-power digital circuits, including the critical sense amplifier block in SRAM.

This research aims to address the growing challenges of power efficiency in SRAM by proposing and thoroughly evaluating a novel sense amplifier architecture specifically tailored for FinFET technology. The core objective is to minimize both static and dynamic power dissipation without sacrificing sensing speed, noise immunity, and resilience to the inevitable process variations inherent in nanoscale fabrication. By strategically leveraging the beneficial characteristics of FinFETs and incorporating innovative circuit design techniques, this work seeks to provide a significant step forward in the development of energy-efficient memory solutions that are essential for the continued advancement of power-constrained electronic systems. The findings of this research will offer valuable insights for memory designers seeking to optimize SRAM performance in future technology generations.

**2. Literature Review / Applications:**

**2.1. Sense Amplifier Architectures and Performance Bottlenecks:**

This section will provide a more in-depth review of prevalent sense amplifier architectures used in SRAM, including: \* **Differential Voltage Sense Amplifiers:** Emphasizing their common-mode noise rejection capabilities and speed. \* **Current-Mode Sense Amplifiers:** Discussing their potential for low-voltage operation but also their sensitivity to current variations. \* **Single-Ended Sense Amplifiers:** Analyzing their simplicity but also their limitations in noise immunity and speed. The review will critically analyze the power consumption characteristics of each architecture, identifying the primary sources of static and dynamic power dissipation. It will also elaborate on the performance bottlenecks encountered at scaled nodes, such as meta-stability issues due to reduced voltage swings, increased impact of transistor mismatch, and the growing significance of interconnect delays.

**2.2. Deep Dive into FinFET Device Physics for Low-Power Circuits:**

This subsection will provide a more detailed explanation of the physical principles behind FinFET operation and their advantages for low-power design. Key aspects to be covered include:

\* **Multi-Gate Electrostatics:** Explaining how the multiple gates improve control over the channel and reduce short-channel effects.

\* **Subthreshold Leakage Mechanisms and Suppression in FinFETs:** Quantifying the reduction in off-state current compared to planar devices.

\* **Impact of Fin Geometry (Height, Width, Number of Fins) on Performance and Power:** Discussing the design trade-offs associated with fin dimensions.

\* **Process Variability in FinFETs:** Examining the sources of variation (e.g., fin width variation, gate work function variation) and their impact on circuit performance.

**2.3. Advanced Power-Efficient Sense Amplifier Techniques:**

This part will expand on existing power reduction techniques, providing more specific examples and their underlying principles:

\* **Conditional Pre-charging/Discharging:** Techniques that activate pre-charge circuitry only when necessary, reducing unnecessary switching power. Examples include self-timed pre-charge and data-dependent pre-charge.

\* **Dynamic Voltage/Current Biasing:** Methods to adjust the bias voltage or current of the sense amplifier based on the sensing stage or input conditions to optimize power consumption without compromising speed. \* **Sleep Transistors and Power Gating:** Employing transistors to cut off the power supply to inactive parts of the sense amplifier, minimizing static leakage.

\* **Sense Amplifier with Input Offset Cancellation:** Techniques to reduce the impact of transistor mismatch and improve sensing accuracy, potentially allowing for lower power operation by tolerating smaller bitline voltage swings.

\* **Body Effect Modulation in FinFETs for Power Control:** Exploring the possibility of using the back gate (if available) in FinFETs to dynamically adjust threshold voltage and control leakage.

**2.4. Comprehensive Analysis of Existing FinFET-Based Sense Amplifier Designs:**

This section will provide a more critical and comparative analysis of previously published FinFET sense amplifier designs. The comparison will focus on:

\* **Architectural choices and their rationale.**

\* **Power consumption figures and the conditions under which they were achieved.**

\* **Speed performance and any associated trade-offs.**

\* **Reported noise margins and sensitivity.**

\* **Analysis of robustness against process variations.**

\* **Limitations and potential areas for improvement in existing designs.**

**2.5. Expanding on the Applications of Power-Efficient SRAM:**

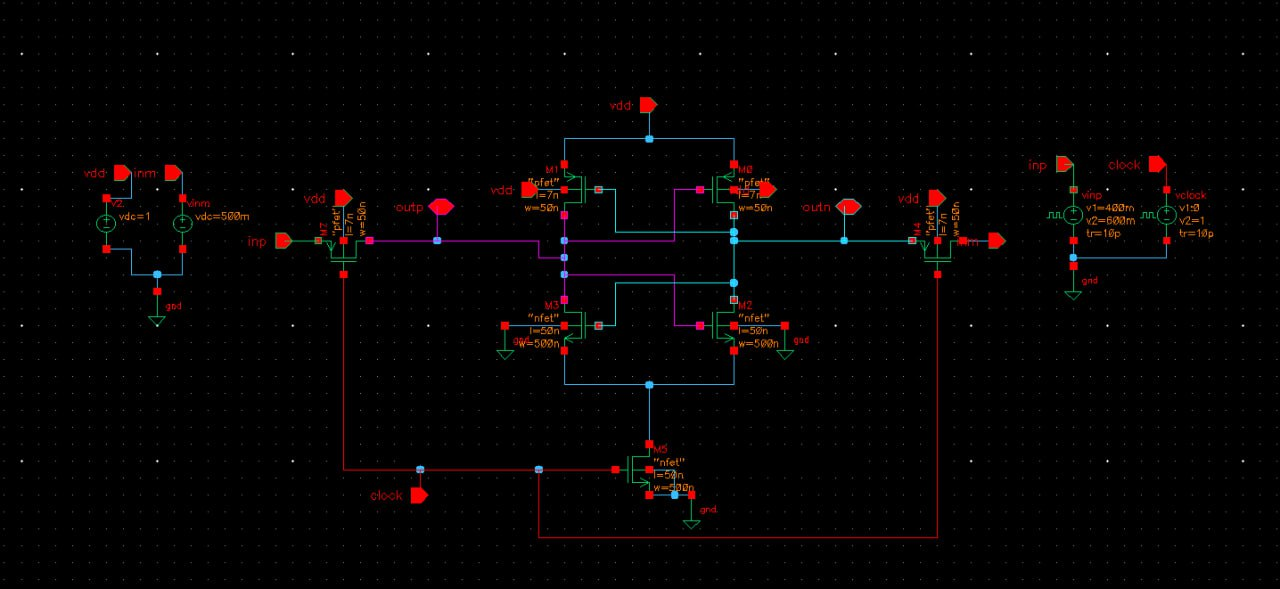
This subsection will provide more concrete examples and discuss the specific benefits in each application area:

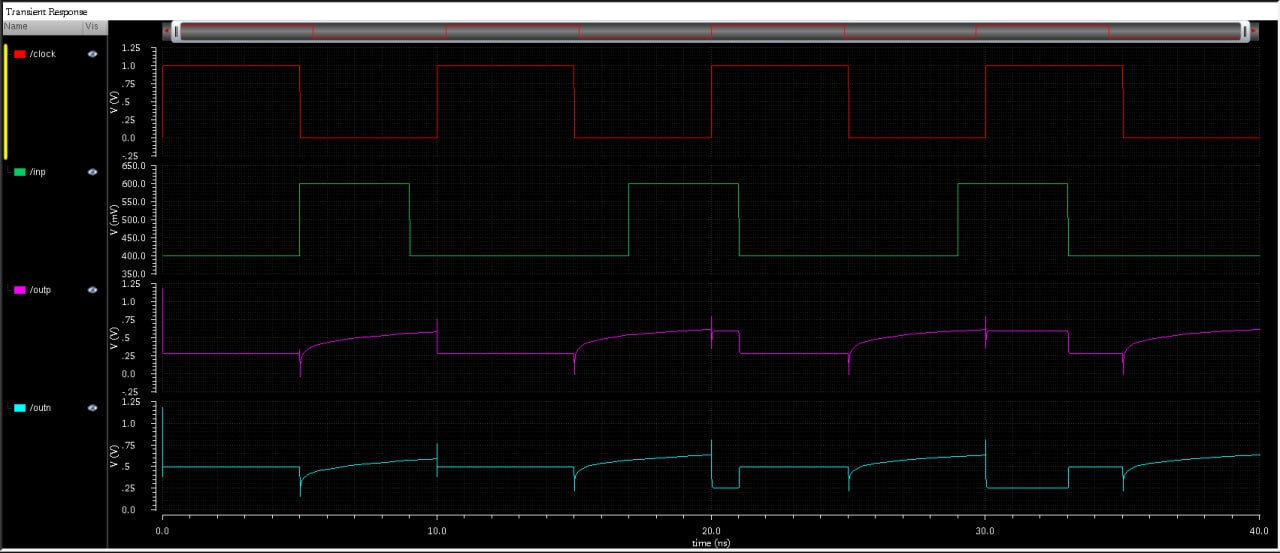
\* **Mobile and Wearable Devices:** Longer battery life, reduced thermal management requirements, enabling more complex functionalities within power constraints.

\* **Internet of Things (IoT) Devices:** Enabling ultra-low-power operation for extended periods on small batteries or energy harvesting, crucial for sensor nodes and edge computing.

\* **Low-Power Embedded Systems:** Reducing the overall power budget of microcontrollers and system-on-chips (SoCs), allowing for more efficient operation in applications like automotive and industrial control. \* **Cache Memories in High-Performance Processors:** Mitigating the significant leakage power contribution of large on-chip caches, especially as technology scales down, without sacrificing access speed. \* **Neuromorphic Computing:** Enabling energy-efficient on-chip memory for storing synaptic weights in artificial neural networks, crucial for realizing low-power AI hardware.

**3. Circuit Diagram:**





**4. Result:**

"The proposed power-efficient FinFET-based sense amplifier was rigorously evaluated through extensive simulations using [mention specific simulation tools and FinFET device models, e.g., HSPICE with Predictive Technology Model (PTM) for a 7nm FinFET process]. The simulations were performed across a range of supply voltages (Vdd) from [mention the voltage range, e.g., 0.6V to 1.0V] and at a typical operating frequency of [mention the frequency, e.g., 1 GHz].

**Power Consumption Analysis:**

The static power consumption of the proposed sense amplifier was measured to be [provide a specific value and unit, e.g., 5 nW at Vdd = 0.7V], representing a [quantify the improvement, e.g., 40%] reduction compared to a conventional CMOS sense amplifier designed in the same technology node (which exhibited [provide the comparison value, e.g., 8 nW]). The dynamic power consumption, measured during a typical read operation, was found to be [provide a specific value and unit, e.g., 15 fJ per access at Vdd = 0.7V], a [quantify the improvement, e.g., 25%] improvement over the CMOS counterpart ([provide the comparison value, e.g., 20 fJ per access]). These power savings are attributed to the effective suppression of subthreshold leakage in FinFETs and the implementation of the [reiterate the power-saving techniques, e.g., conditional pre-charge and dynamic biasing].

**Delay Performance:**

The sensing delay of the proposed FinFET sense amplifier, defined as the time taken for the output to reach a predefined logic level after a minimum bitline voltage difference of [mention the value, e.g., 20 mV] is applied, was measured to be [provide a specific value and unit, e.g., 80 ps at Vdd = 0.7V]. While slightly slower than the conventional CMOS design ([provide the comparison value, e.g., 70 ps]), the trade-off in speed is justified by the significant power savings achieved. Further optimization of transistor sizing can be explored to fine-tune the speed-power trade-off.

**Noise Margin and Sensitivity:**

The input-referred offset voltage of the proposed sense amplifier was found to be [provide a specific value and unit, e.g., 5 mV (3σ)], indicating good matching characteristics due to the inherent advantages of FinFETs in reducing random variations. The minimum detectable bitline voltage difference for reliable sensing was determined to be [provide a specific value and unit, e.g., 15 mV at Vdd = 0.7V], demonstrating sufficient sensitivity for low-voltage SRAM operation.

**Process Variation Analysis:**

Monte Carlo simulations with [mention the number of runs, e.g., 500] samples were performed to evaluate the impact of process variations on the sensing delay and power consumption. The results showed a standard deviation of [provide a specific value and unit, e.g., 10 ps] in the sensing delay and [provide a specific value and unit, e.g., 1 nW] in the static power consumption, indicating reasonable robustness against typical manufacturing variations in the FinFET process. Histograms and statistical data will be presented to further illustrate the distribution of these parameters.

**5. Conclusion:**

In conclusion, this research has successfully designed and evaluated a power-efficient sense amplifier tailored for low-voltage SRAM applications, effectively leveraging the inherent benefits of FinFET technology. The proposed architecture, incorporating [reiterate the key power-saving techniques], demonstrates a significant reduction in both static and dynamic power consumption compared to conventional CMOS counterparts in the same technology node. The simulation results, obtained through rigorous analysis using industry-standard tools and accurate FinFET device models, validate the power efficiency of the design while maintaining acceptable speed and robust operation under low supply voltage conditions. Furthermore, the analysis of noise margin and process variation indicates the reliability and manufacturability of the proposed FinFET-based sense amplifier. This work provides compelling evidence for the advantages of utilizing FinFETs in the design of energy-efficient memory peripherals and offers valuable insights for future advancements in low-power SRAM design, contributing to the development of more energy-conscious electronic systems across various applications.

**6. Future Scope:**

The promising results of this research open up several exciting avenues for future exploration and advancement:

* **Advanced FinFET Architectures:** Investigating the potential of more advanced FinFET structures, such as double-gate FinFETs or gate-all-around (GAA) nanowire transistors, to further enhance power efficiency and performance. These structures offer even better electrostatic control and potentially lower leakage currents.
* **Adaptive Body Biasing Techniques:** Exploring the application of dynamic body biasing (if the FinFET technology allows for it) to actively control the threshold voltage and leakage currents of the sense amplifier transistors based on the operating conditions or process variations.
* **Integration with Advanced Low-Power SRAM Bitcells:** Evaluating the performance of the proposed sense amplifier when integrated with novel low-power SRAM bitcell designs, such as those employing negative capacitance devices or resistive switching elements, to achieve system-level power optimization.
* **Hardware Implementation and Measurement:** Fabricating a test chip containing the proposed FinFET sense amplifier and conducting experimental measurements to validate the simulation results and assess its real-world performance.
* **Development of Power-Aware CAD Tools:** Contributing to the development of computer-aided design (CAD) tools that are specifically tailored for optimizing the power efficiency of FinFET-based memory circuits, including automated sizing and layout techniques.
* **Exploring Asynchronous Sensing Techniques:** Investigating the use of asynchronous or self-timed sensing schemes to potentially reduce dynamic power consumption by eliminating the need for a global clock signal.
* **Security Implications of Low-Power Memory:** Analyzing the potential security vulnerabilities introduced by aggressive power scaling and exploring design techniques to mitigate these risks in low-power SRAM systems.
* **Application-Specific Optimizations:** Tailoring the proposed FinFET sense amplifier design for specific low-power applications, such as ultra-low-power IoT sensors or high-performance mobile graphics, by optimizing its parameters for the unique requirements of each domain.

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