Low-Power, Fault-Tolerant Hybrid ADC for Edge IoT Devices

July 18, 2025

Alternative Titles

- Design and Simulation of a Hybrid 8-bit Flash-SAR ADC with Fault Detection for Edge Computing
- Energy-Efficient Hybrid ADC Architecture with Fault Resilience for IoT Applications

Project Overview (Plain Language Summary)

This project focuses on the design and simulation of an energy-efficient, fault-resilient 8-bit Analog-to-Digital Converter (ADC) intended for edge IoT applications. The hybrid ADC architecture merges the speed of Flash ADC with the power efficiency of SAR ADC, while integrating a fault detection mechanism to monitor reference voltage stability.

Architecture Breakdown

Component	Role
3-bit Flash ADC	Rapidly acquires the most significant bits (MSBs) of the analog signal. Optimized for speed.
5-bit SAR ADC	Efficiently resolves the least significant bits (LSBs). Designed for low power operation.
Fault Detection Block	Monitors reference voltage (V_{ref}) and flags errors when deviations may affect accuracy. Enhances system reliability.

Key Outcomes

1. Reduced Power Consumption

- Flash ADCs are inherently fast but power-hungry.
- SAR ADCs are slower but significantly more energy-efficient.
- **Our hybrid design uses Flash for 3 MSBs and SAR for 5 LSBs**—balancing performance and power.
- **Result:** Faster than pure SAR, but consumes less power than full Flash.

2. Fault-Tolerant Design

- IoT edge devices often face environmental disturbances: noise, temperature shifts, battery instability.
- The fault detection block checks V_{ref} continuously and raises an error flag if an anomaly is detected.
- **Result:** Improved robustness and reliability in harsh or noisy conditions.

3. Edge Device Readiness

- Edge devices demand lightweight, efficient, and resilient components.
- The hybrid ADC is tailored to meet these needs—low power, high reliability, and fault awareness.
- **Result:** Ideal for wearables, remote sensors, edge-AI modules, and real-time monitoring systems.

Research Significance

This project is not just another ADC design. It contributes to the research landscape through:

- **Architectural Innovation:** Combines Flash and SAR into a hybrid design.
- **Fault Resilience:** Integrates real-time fault detection logic for increased reliability.
- **IoT Relevance:** Specifically targets resource-constrained, real-world edge applications.

Conclusion: While typical undergraduate projects stop at simulating a basic ADC, this work explores design trade-offs and system robustness, adding real-world applicability and engineering depth.