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Approximate Computing Based Logic Design

Proposed Project Summary:

Approximate computing is a solution for energy efficient designs providing trade-off between accuracy and power. It can reduce the design complication with an increase in performance and power efficiency for error resilient applications. It is based on the observation that in many scenarios, although performing exact computation requires large number of resources, allowing bounded approximation can provide disproportionate gains in performance and energy, while still achieving acceptable result accuracy [3]. It has been used in a variety of domains where the applications are error-tolerant, such as multimedia processing, machine learning, signal processing, scientific computing. Therefore, approximate computing is mostly driven by applications that are related to human perception/cognition and have inherent error resilience [4].

An adder is a kind of calculator that is used to add two binary numbers. It is an elementary block of multiplier and speed limiting element of multiplier as well. Therefore, there is a huge need for careful optimization of adder design [2].

The purpose of the ongoing research works is to successfully implement energy efficient designs. Applications like data mining and multimedia signal processing does not require exact results in many cases. So, in such cases approximate computing is used [1].

Problem Statement:

There is a need to reduce the design complication which would result in increased performance and power efficiency in error resilient applications. Various computationally intensive applications like visual processing and multimedia signals do not require high precision to work correctly. Therefore, we do not need to produce accurate output due to reasons such as limitation of human sense organs which are unable to recognize very subtle variations also the input data gathered from an image sensor has a decreased quality. Hence, a novel approximate architecture, which improves output quality is required.

Expected Project Outcomes:

The usage of approximate computing permits performing multimedia processing in an energy and resource efficient way. To reduce the computational effort and bandwidth required for the execution of the discussed algorithm. A technique to accelerate systems or applications or increase their power efficiency by allowing appreciable loss of precision.

Project Tasks Description:

S.No	Task	Methodology	Resource Required	Start Date	Expected End Date
1	Implementation and simulation			01/12/2021	30/03/2022
2	Report Writing and evaluation			01/09/2021	30/11/2021
I.	**STUDENT 1- VEDANSHI SAINI & 07211502819**				
1	Research	Carry based approximate full	IEEE conference	01/09/2021	03/09/2021

	Paper	adder for low power approximate computing	paper		
2	Research Paper	Exploring the Use of Parallel Prefix Adder Topologies into Approximate Adder Circuits	IEEE conference paper	03/09/2021	06/09/2021
II.	**STUDENT 2- ANUSHKA GAGWARI & 08611502819**				
1	Research Paper	Adaptive Approximate Adder (A3) to Reduce Error Distance for Image Processor	IEEE conference paper	01/09/2021	03/09/2021
2	Research Paper	Design of Low Power, Area Efficient and High Speed Approximate Adders for Inexact Computing	IEEE conference paper	03/09/2021	06/09/2021
III.	**STUDENT 3 – SHREYAS GUPTA & 08911502819**				
1	Research Paper	A LUT-Based Approximate Adder	IEEE conference paper	01/09/2021	03/09/2021
2	Research Paper	Approximate Multipliers based on Inexact Adders for Energy Efficient Data Processing	IEEE conference paper	03/09/2021	06/09/2021
IV.	**STUDENT 4- ABIR MOITRA & 35111502817**				
1	Research Paper	Low-Power and Energy-Efficient Full Adders With Approximate Adiabatic Logic for Edge Computing	IEEE conference paper	01/09/2021	03/09/2021
2	Research Paper	Study of Approximate Multiplier with Different Adders	IEEE conference paper	03/09/2021	06/09/2021

References:

[1] M. Ramasamy, G. Narmadha and S. Deivasigamani, "Carry based approximate full adder for low power approximate computing," 2019 7th International Conference on Smart Computing & Communications (ICSCC), 2019, pp. 1-4, doi: 10.1109/ICSCC.2019.8843644.

[2] M. Macedo, L. Soares, B. Silveira, C. M. Diniz and E. A. C. da Costa, "Exploring the use of parallel prefix adder topologies into approximate adder circuits," 2017 24th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2017, pp. 298-301, doi: 10.1109/ICECS.2017.8292078.

[3] S. Kim and Y. Kim, "Adaptive approximate adder (A3) to reduce error distance for image processor," 2016 International SoC Design Conference (ISOCC), 2016, pp. 295-296, doi: 10.1109/ISOCC.2016.7799794.

[4] A. Becher, J. Echavarria, D. Ziener, S. Wildermann and J. Teich, "A LUT-Based Approximate Adder," 2016 IEEE 24th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2016, pp. 27-27, doi: 10.1109/FCCM.2016.16.

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