Full Adder using CMOS

SAYYAM VITALKAR

Department of Electronics Engineering
Yeshwantrao Chavhan College of Engineering, Nagpur
September 30,2025
sayyamvitalkar123@gmail.com

Abstract:

A full adder is one of the most important building blocks in digital systems, as it performs the basic arithmetic operation of adding three binary inputs to produce a sum and a carry output. In this work, a full adder circuit is designed using CMOS technology, which offers advantages such as low power consumption, high noise immunity, and compact layout. The design uses complementary MOS transistors to implement the logic functions required for sum and carry generation. The CMOS approach ensures reliable switching characteristics while reducing static power dissipation compared to other logic styles. Such a full adder circuit can be integrated into larger arithmetic units like adders, multipliers, and digital signal processors, making it essential for efficient VLSI design.

REFERENCE CIRCUIT DETAILS

In my complete full adder. I broke down the sum and carry equations utilising fundamental logic .To create sum we need xor consist of 8 transistor in which 4 are pmos and 4 nmos therefore we use 16 transistor and we have to use pmos is series and nmos is parallel

Therefore the transistor required is 16

Now to create carry we require

1.OR gate for (A+B)

Where nmos is in parallel and pmos is in series

2.AND gate with C =C*(A+B)

Nmos series with C and pmos parallel with C

3. OR gate With AB=AB+C(A+B)

here Nmos are in parallel and pmos is in series

Therefor the transistor requirement in carry is 18-20 subtractor logic with reduced gate usage while preserving correct logical functionality.

.

Reference Circuit

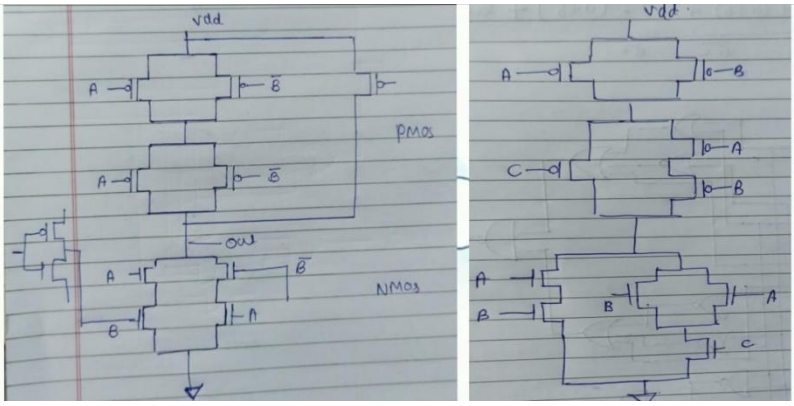
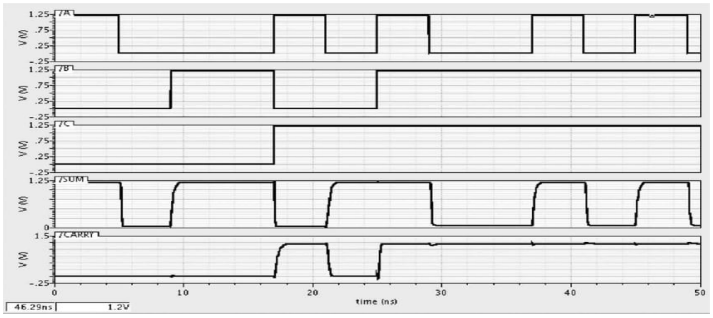


Figure 1: Reference circuit diagram.

Reference waveform

Figure 2: Reference waveform.



Reference

1. Beltran Jr., Angelo A., Kristina Nones, Reina Louise Salanguit, Jay Bhie Santos, Jose Maria Rei Santos & Keith Joseph Dizon, “Low Power NAND Gate–based Half and Full Adder / Subtractor Using CMOS Technique.”