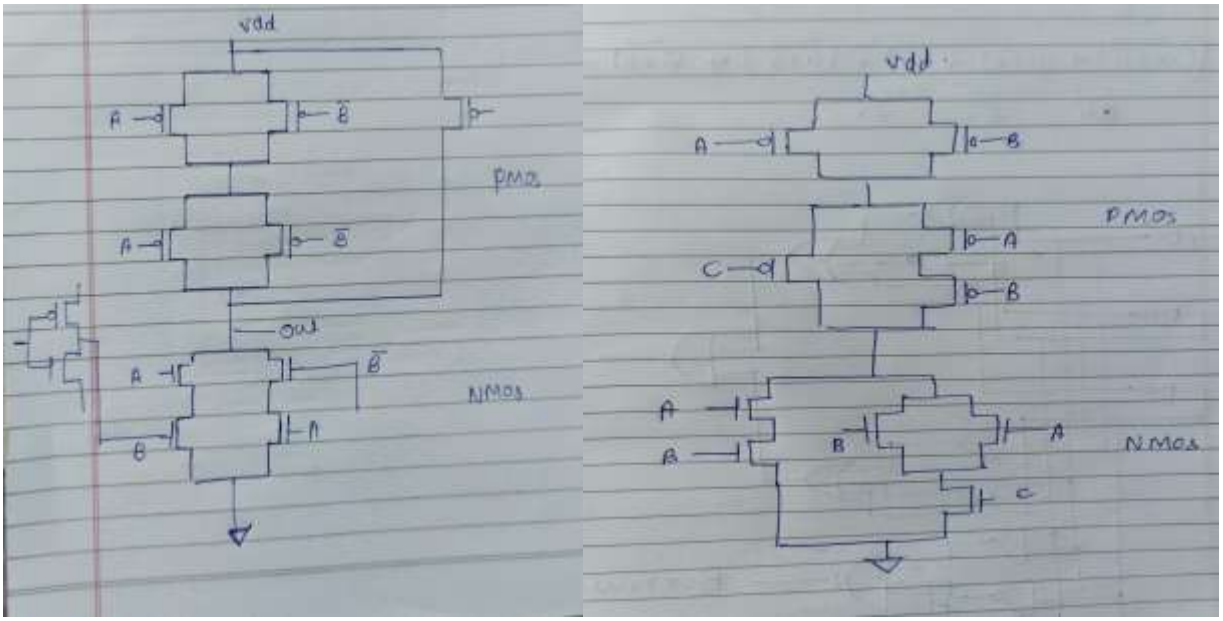
Project title: Full adder using CMOS

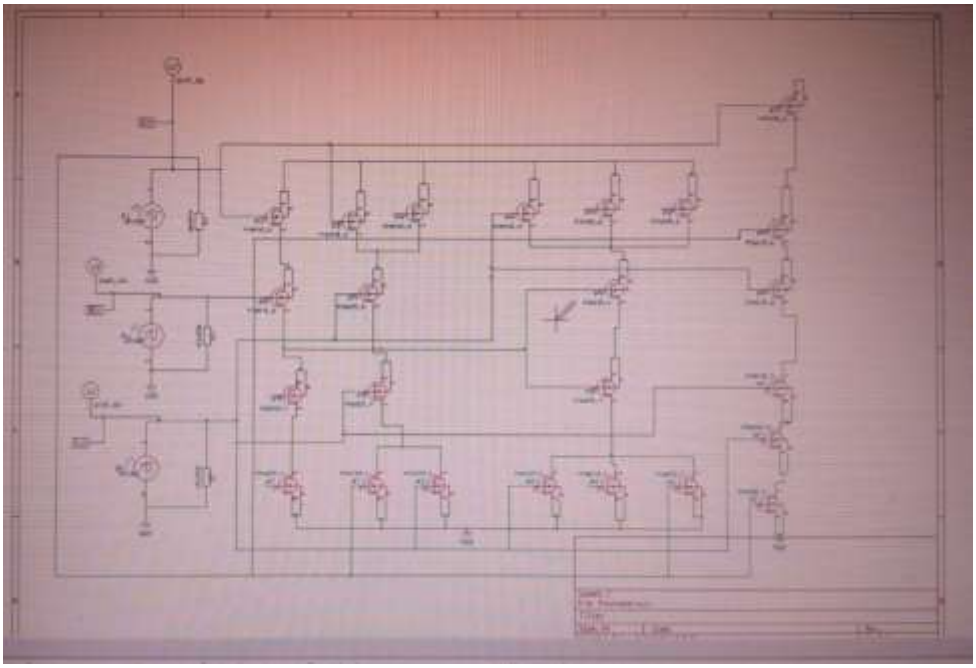
Objective:

This experiment's goal is to use CMOS technology to design and build a complete adder circuit. It seeks to comprehend how binary addition with low power consumption and high noise immunity can be accomplished using CMOS logic. Analyzing the sum and carry outputs for every possible combination of inputs is the main goal of the experiment. Through simulation or real-world application, it also aims to confirm the full adder's truth table. The overall goal is to investigate the functionality and effectiveness of CMOS-based arithmetic circuits.

Circuit:

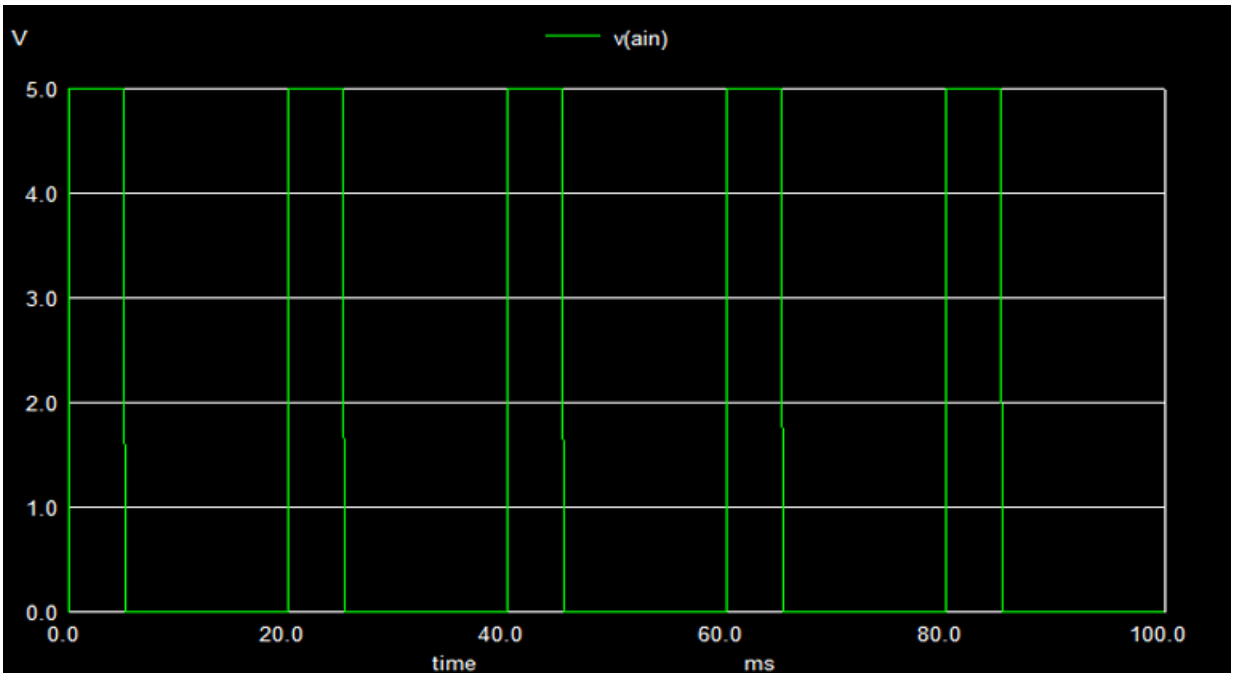


Schematic :

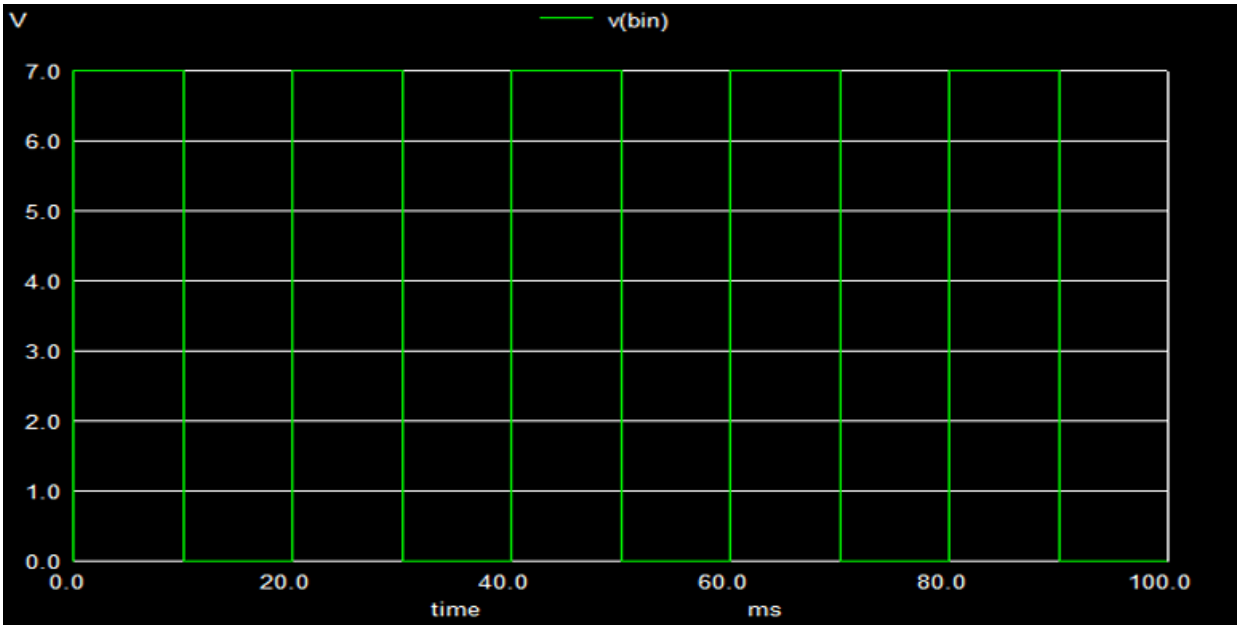


Simulation result:

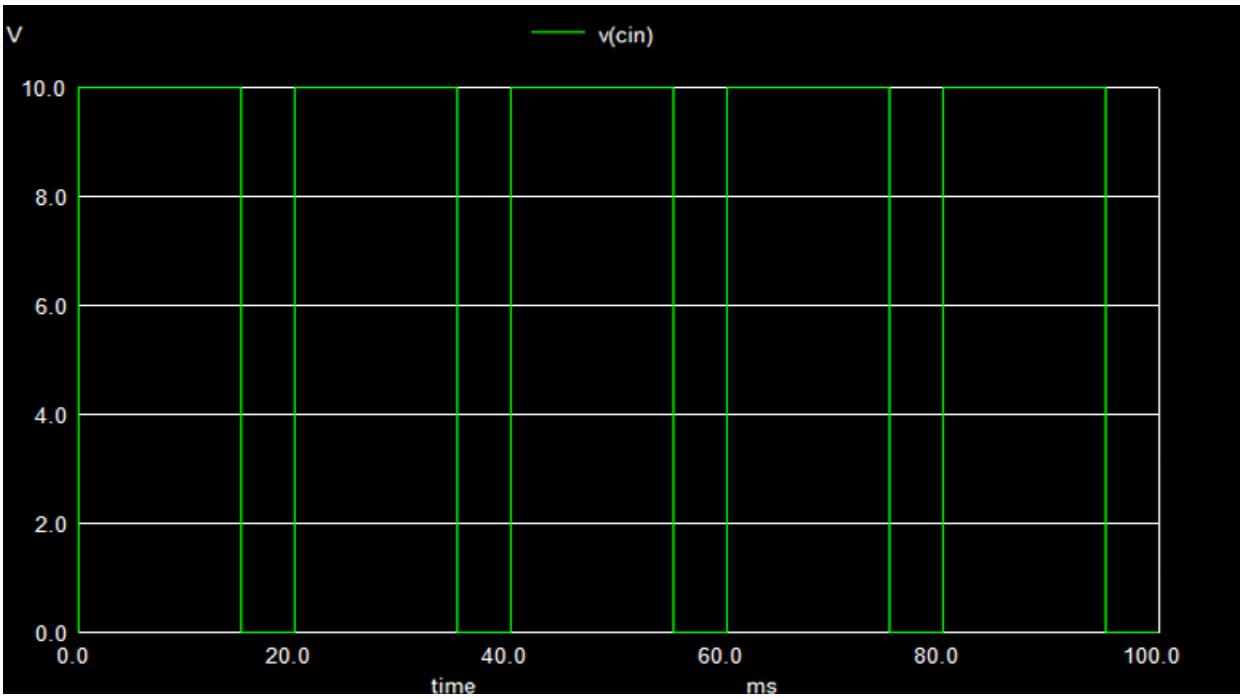
A



B

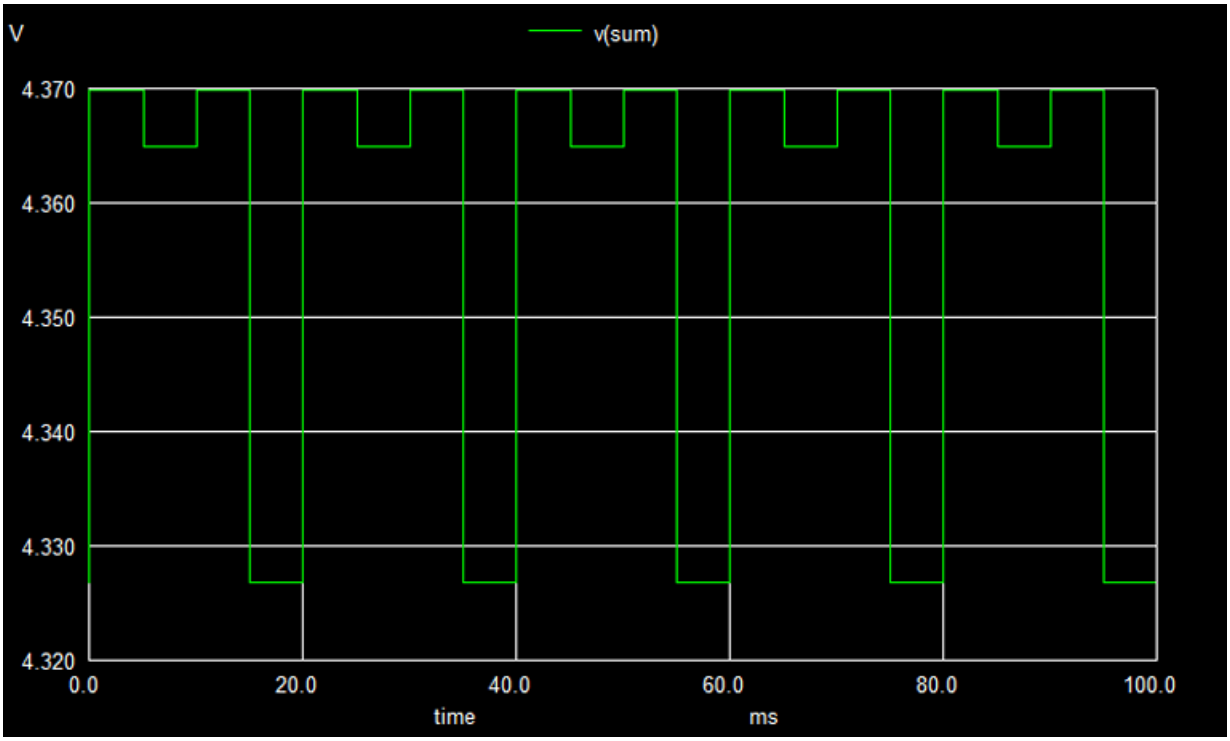

V
v(bin)
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

C

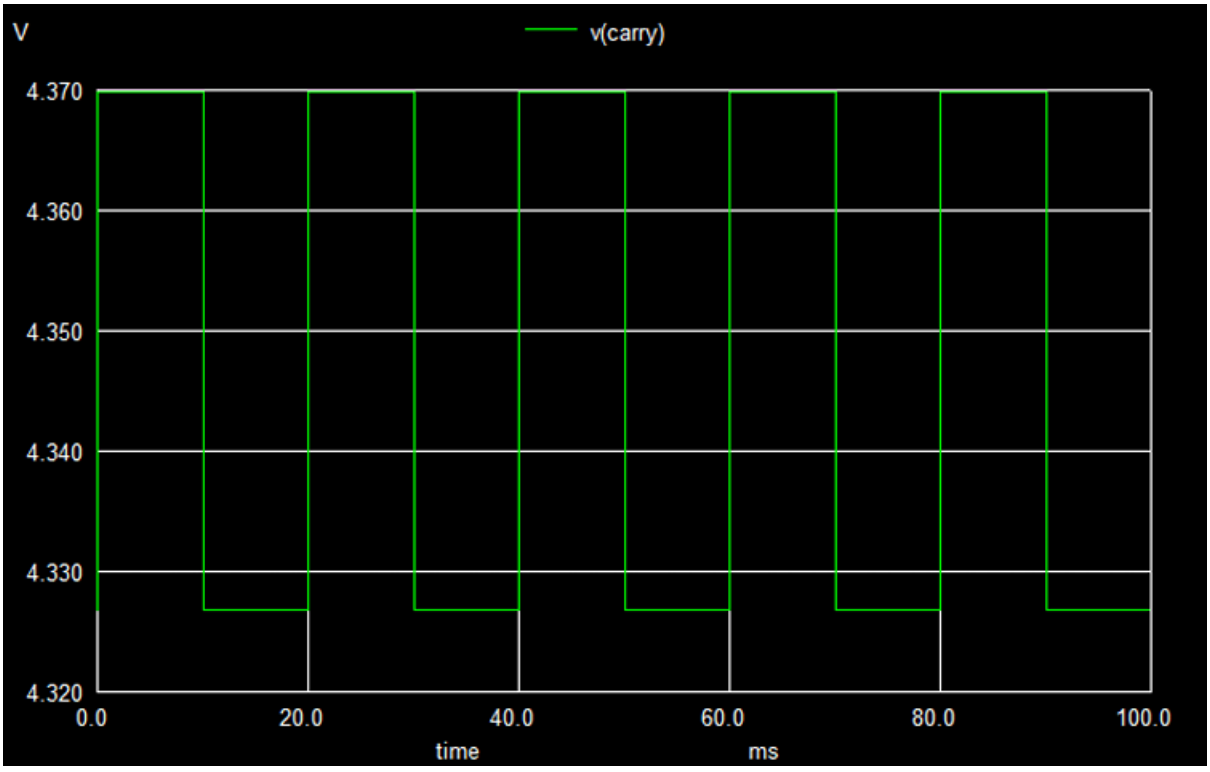

V
v(cin)
10.0
8.0
6.0
4.0
2.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

Ouput :

Sum


V
v(sum)
4.370
4.360
4.350
4.340
4.330
4.320
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

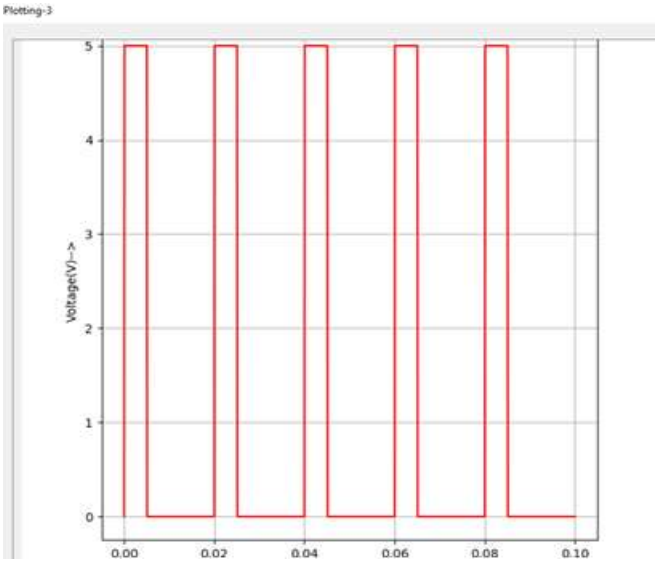
Carry :


V
v(carry)
4.370
4.360
4.350
4.340
4.330
4.320
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

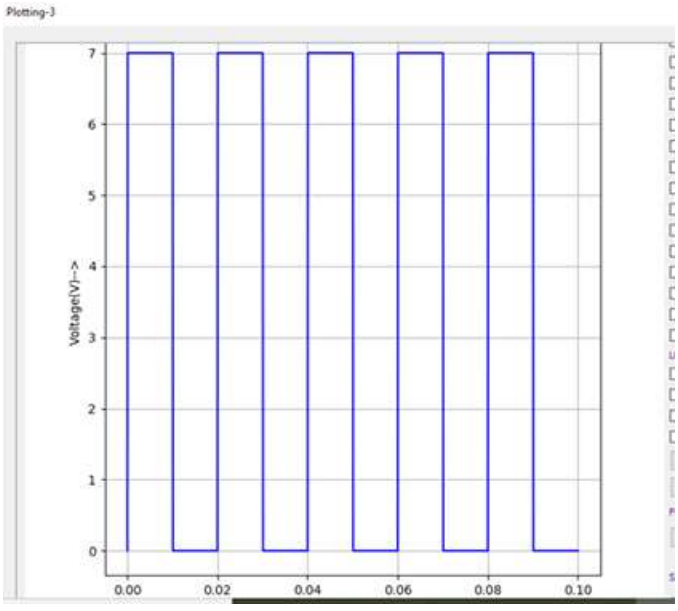
Python plot :

Input :

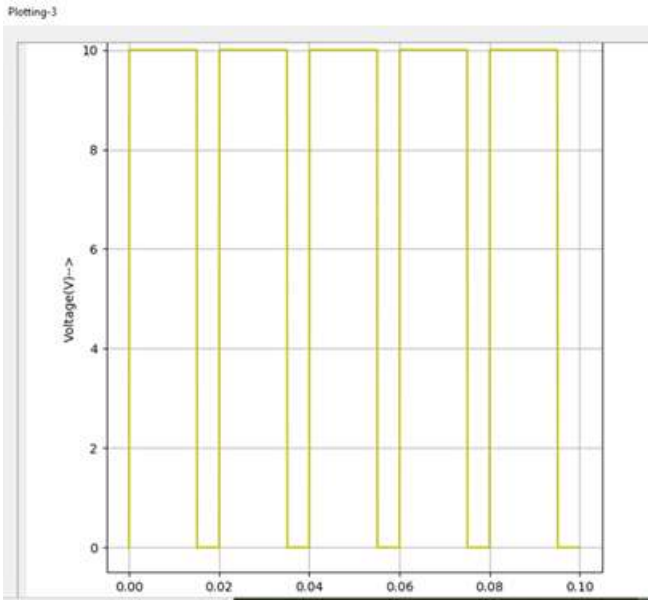
A



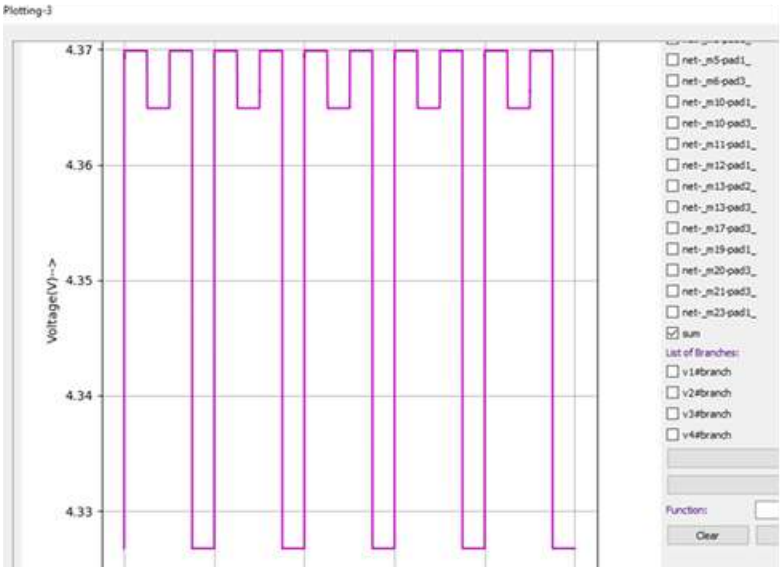
B



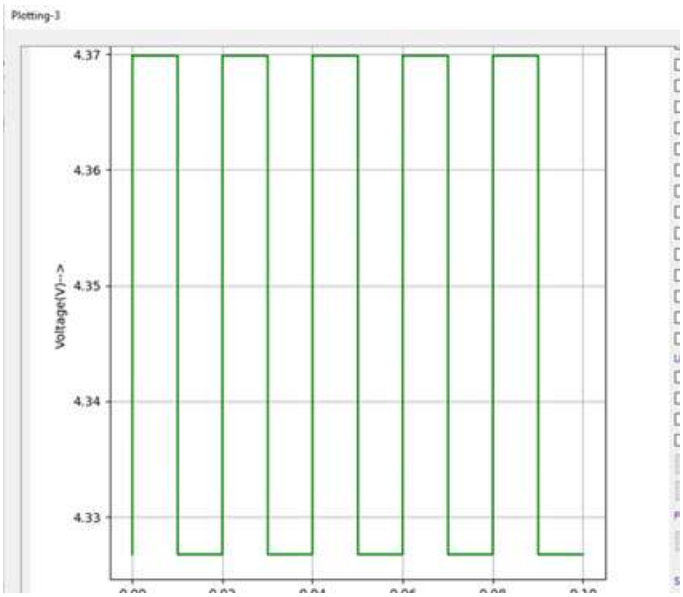
C


Plotting-3
Voltage(V)-->
10
8
6
4
2
0
0.00
0.02
0.04
0.06
0.08
0.10

Sum


Plotting-3
Voltage(V)-->
4.37
4.36
4.35
4.34
4.33
net-_m5-pad1_
net-_m6-pad3_
net-_m10-pad1_
net-_m10-pad3_
net-_m11-pad1_
net-_m12-pad1_
net-_m13-pad2_
net-_m13-pad3_
net-_m17-pad3_
net-_m19-pad1_
net-_m20-pad3_
net-_m21-pad3_
net-_m23-pad1_
sum
List of Branches:
v1#branch
v2#branch
v3#branch
v4#branch
Function:
Clear

Carry



Github repository :

https://github.com/sayyamvitalkar123-droid/eSimproject

Conclusion : Successfully simulation was done and thus we get appropriate waveforms.