EECE 2150: Quiz 3 Notesheet Sean Balbale October 2024

1 Logic Gates and Truth Tables

1.1 AND Gate

Boolean Expression: $A \cdot B$
Truth Table:

A	B	A AND B
0	0	0
0	1	0
1	0	0
1	1	1

1.2 OR Gate

Boolean Expression: $A + B$
Truth Table:

A	B	A OR B
0	0	0
0	1	1
1	0	1
1	1	1

1.3 XOR Gate

Boolean Expression: $A \oplus B = \overline{A}B + A\overline{B}$
Truth Table:

A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

1.4 NAND Gate

Boolean Expression: $\overline{A \cdot B}$
Truth Table:

A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

1.5 NOR Gate

Boolean Expression: $\overline{A + B}$
Truth Table:

A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

1.6 XNOR Gate

Boolean Expression: $A \odot B = AB + \overline{AB}$
Truth Table:

A	B	A XNOR B
0	0	1
0	1	0
1	0	0
1	1	1

1.7 NOT Gate

Boolean Expression: $\overline{A}$
Truth Table:

A	$NOT A$
0	1
1	0

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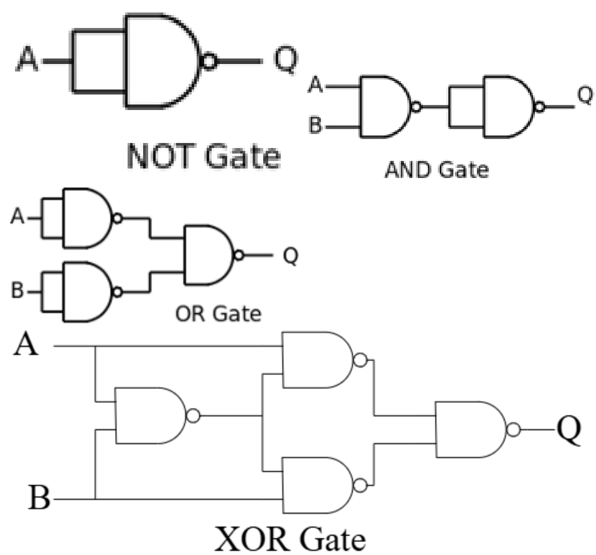
2 NAND Gate Equivilance



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3 Karnaugh Maps (K-Maps)

Used to simplify Boolean expressions:

- Group 1s in powers of 2 (1, 2, 4, 8...).
- Simplify terms by reducing variables.

3.1 Example 4-Variable K-Map

$AB \backslash CD$	00	01	11	10
00	X	0	1	1
01	1	1	X	0
11	1	1	X	0
10	0	0	X	1

This example shows a 4-variable K-Map with values for each combination of inputs (A, B, C, D). Group 1s in powers of 2 to simplify.
$Y = \overline{A}C + A\overline{C} = A \oplus C$
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4 Two's Complement

Two's Complement Conversion:

1. Invert all bits.
2. Add 1 to the least significant bit (LSB).

Example: Convert 5 to binary and find -5:

$$5_{10} \rightarrow 0101 \rightarrow \text{Invert: } 1010 \rightarrow \text{Add 1: } 1011 \rightarrow -5$$

Overflow Detection: This happens when a number larger than the maximum allowed number of bits occurs. When adding two numbers of the same sign, if the result's sign differs from the operands, an overflow occurred.
Caryout Detection: When the result has a one in the most significant bit + 1 position.
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5 Multiplexers, Shifters, and Steady State Machines

5.1 Multiplexer (MUX)

5.1.1 2:1 Multiplexer

- **Description**: A 2:1 multiplexer has two inputs (A and B), one output (Y), and one select line (S).

- **Functionality**: The select line S determines which input is connected to the output Y:

$$Y = S' \cdot A + S \cdot B$$

- **Application**: Basic signal selection in low-complexity circuits.

5.1.2 4:1 Multiplexer

- **Description**: A 4:1 multiplexer has four inputs (A, B, C, D), one output (Y), and two select lines (S_0 and S_1).

- **Functionality**: The select lines S_0 and S_1 determine which input is routed to the output Y:

$$Y = S_1'S_0' \cdot A + S_1'S_0 \cdot B + S_1S_0' \cdot C + S_1S_0 \cdot D$$

- **Application**: Used for selecting one of multiple signals in data routing and control systems.

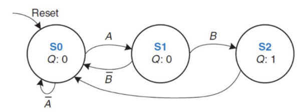
5.2 Shifters

Logical, Arithmetic, and Circular Shifters:

- Logical Shifter: Moves all bits left or right by adding zero.
- Arithmetic Shifter: Left, same as logical, Right, skips most significant bit.
- Circular Shifter: Rotates bits.

5.3 Steady State Machines

Moore Machine: Output depends on current state only.



State	Encoding	
	s_1	s_0
S0	0	0
S1	0	1
S2	1	0

Current State		Inputs		Next State	
s_1	s_0	A	B	s_1'	s_0'
0	0	0	X	0	0
0	0	1	X	0	1
0	1	X	0	0	0
0	1	X	1	1	0
1	0	X	X	0	0

State transition table with binary encodings

Current State		Output
s_1	s_0	Q
0	0	0
0	1	0
1	0	1

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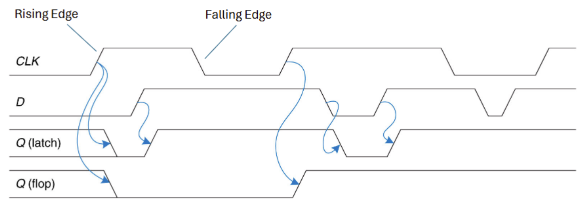
6 D Latch vs. D Flip-Flop



6.1 D Latch (Level-Triggered)

- **Functionality**: The D latch passes the input D to the output Q when the Enable signal (often denoted as E or EN) is active (high, or logic 1). When the enable is low (0), the output Q holds its previous value, effectively "latching" onto the last state.

- **Level-Triggered**: A D latch is **level-triggered**, meaning it responds to the level (high or low) of the enable signal. As long as the enable signal is high, changes at D will pass directly to Q.

6.2 D Flip-Flop (Edge-Triggered)

- **Functionality**: A D flip-flop captures the value at input D only at the moment of a clock edge (typically the rising or falling edge of the clock signal). The value of Q is updated only on the clock edge and then remains constant until the next clock edge.

- **Edge-Triggered**: Unlike the latch, the D flip-flop is **edge-triggered**, meaning it only updates Q on a specific transition of the clock signal (either rising or falling edge). This characteristic makes it useful in synchronous circuits.