- CPSC 275: Introduction to Computer Systems

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Fall 2025

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Homework 29

NOTE: You are not required to hand in the following exercises, but you are strongly encouraged to complete them to strengthen your understanding of the concepts covered in class.

1. In general, if the high-order *s* bits of an address are used as the set index, contiguous chunks of memory blocks are mapped to the same cache set.
   A. How many blocks are in each of these contiguous array chunks?
   B. Consider the following code that runs on a system with a cache of the form (*S*, *E*, *B*, *m*) = (512, 1, 32, 32):

```
int array[4096];

for (i = 0; i < 4096; i++)
   sum += array[i];
```

   What is the maximum number of array blocks that are stored in the cache at any point in time?

2. Complete the following table, filling in the missing entries and replacing each question mark with the appropriate integer. Use the following units: K = 2^{10} (Kilo), M= 2^{20} (Mega), G = 2^{30} (Giga), T = 2^{40} (Tera), P = 2^{50} (Peta), or E = 2^{60} (Exa).

No. virtual address bits (*n*)	No. virtual addresses (*N*)	Largest possible virtual address
8		
	$2^{?}$ = 64K	
		$2^{32} - 1$ = ?G − 1
	$2^{?}$ = 256T	
64		

3. Determine the number of page table entries (PTEs) that are needed for the following combinations of virtual address size (n) and page size (P):

n	$P = 2^p$	No. PTEs
16	4K	
16	8K	
32	4K	
32	8K	

- **Welcome: Sean**
  - LogOut