- [CPSC 275: Introduction to Computer Systems](#)

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Fall 2025

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Homework 26

NOTE: You are not required to hand in the following exercises, but you are strongly encouraged to complete them to strengthen your understanding of the concepts covered in class.

1. The following table gives the parameters for a number of different caches. For each cache, determine the number of cache sets (S), tag bits (t), set index bits (s), and block offset bits (b).

```
Cache   m     C     B    E    S    t    s    b
  1.    32  1024    4    1
  2.    32  1024    8    4
  3.    32  1024   32   32
```

where m is the number of memory address bits, and C is cache size in bytes not including overhead such as the valid and tag bits.

2. The following table gives the parameters for a number of different caches. For each cache, fill in the missing fields in the table.

```
Cache   m     C     B    E    S     t    s    b
  1.    32   ___    8    1   ___    21   8    3
  2.    32  2048   ___  ___  128    23   7    2
  3.    32  1024    2    8   64    ___  ___   1
  4.    32  1024   ___   2   16     23   4   ___
```

- **Welcome: Sean**

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