

Lab 9

NMOS Common-Source Amplifier

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1 Objective

The objective of this laboratory exercise is to study the NMOS common-source (CS) amplifier. This will be accomplished by:

- Completing a DC and small-signal analysis to design an amplifier that meets a specific gain requirement.
- Simulating the designed circuit to compare its performance against the paper analysis.
- Implementing the circuit in an experimental setting, taking measurements, and comparing its performance with both theoretical and simulated results.
- Measuring the output resistance of the prototyped amplifier.

2 Theory

A Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a three-terminal device (Gate, Drain, Source) that can be used for amplification. The common-source (CS) configuration is a fundamental amplifier topology.

DC Analysis To analyze an amplifier, the first step is to determine the DC operating point (Q-point) by eliminating AC signal sources. For the NMOS amplifier, this involves finding the DC drain current (I_D) and drain-to-source voltage (V_{DS}). Assuming the transistor is in the saturation region (the region for amplification) and neglecting channel-length modulation, the drain current is:

$$I_D = \frac{1}{2}k_n(V_{GS} - V_t)^2 = \frac{1}{2}k_nV_{OV}^2$$

where k_n is the process transconductance parameter, V_{GS} is the DC gate-to-source voltage, V_t is the threshold voltage, and V_{OV} is the overdrive voltage. The DC drain voltage is then found using Ohm's law on the drain resistor R_D :

$$V_D = V_{DD} - R_D I_D$$

To confirm the transistor is in saturation, the condition $V_{DS} > V_{OV}$ must be met.

AC Small-Signal Analysis Once the DC operating point is found, the small-signal parameters are calculated. The most important parameter is the transconductance, g_m :

$$g_m = \frac{2I_D}{V_{OV}} = \sqrt{2k_n I_D}$$

Another parameter is the transistor output resistance r_o , caused by channel-length modulation (λ), given by $r_o = 1/(\lambda I_D)$.

Next, all DC sources are set to zero (voltage sources become short circuits, current sources become open circuits) and the transistor is replaced with its small-signal model. For the CS amplifier, the voltage gain A_v is the ratio of the AC output voltage ($v_o = v_{ds}$) to the AC input voltage ($v_i = v_{gs}$). When including the load resistor R_L and the transistor's output resistance r_o , the gain is:

$$A_v = \frac{v_o}{v_i} = -g_m(R_D \parallel r_o \parallel R_L)$$

The negative sign indicates that the output signal is 180° out of phase with the input signal.

The amplifier's input resistance R_{in} is the resistance seen by the signal source. For the CS amplifier, this is dominated by the gate resistor R_G (as the MOSFET gate itself has infinite resistance). The output resistance R_o is the Thevenin equivalent resistance seen looking into the amplifier's output terminal (with R_L removed). For this circuit, $R_o = R_D \parallel r_o$.

3 Experimental Method and Reasoning

A common-source amplifier was designed using an enhancement-type NMOS transistor (2N7000) and dual voltage supplies of $V_+ = 15$ V and $V_- = -15$ V. The full circuit schematic is shown in Figure 1.

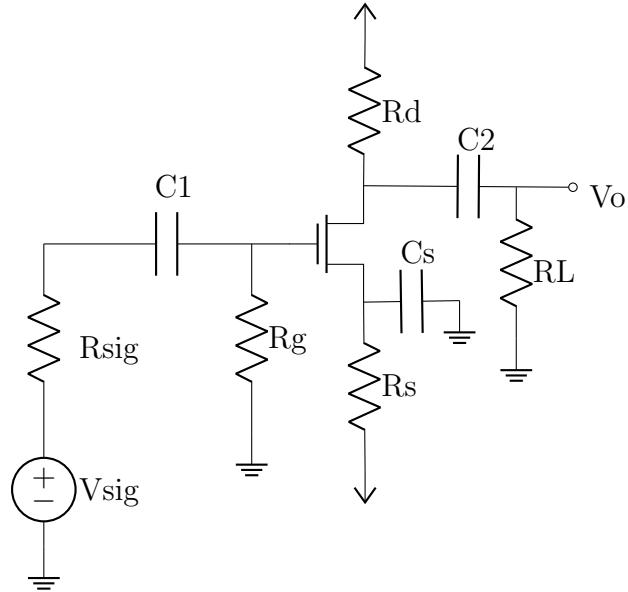


Figure 1: Full Schematic of the Common-Source Amplifier

Part 1: Design and Simulation First, a DC and AC analysis was performed by hand to design the amplifier. The design goals were $I_D = 1 \text{ mA}$ and $A_v \leq -5 \text{ V/V}$, using given transistor parameters (k_n , V_{tn} , λ). This analysis determined the required values for the source resistor R_S and drain resistor R_D .

The circuit was then simulated in LTspice using the calculated resistor values and the provided 2N7000 SPICE model. A $20 \text{ mV}_{\text{pk-pk}}$, 1 kHz sinusoidal input signal (v_{sig}) was applied. The simulation was used to measure the DC operating point (V_{GS} , V_{DS} , I_D) and the AC voltage gain A_v , which were then compared to the hand calculations.

Part 2: Prototyping The circuit was assembled on a breadboard using standard resistor values close to the calculated design values, as shown in Figure 2.

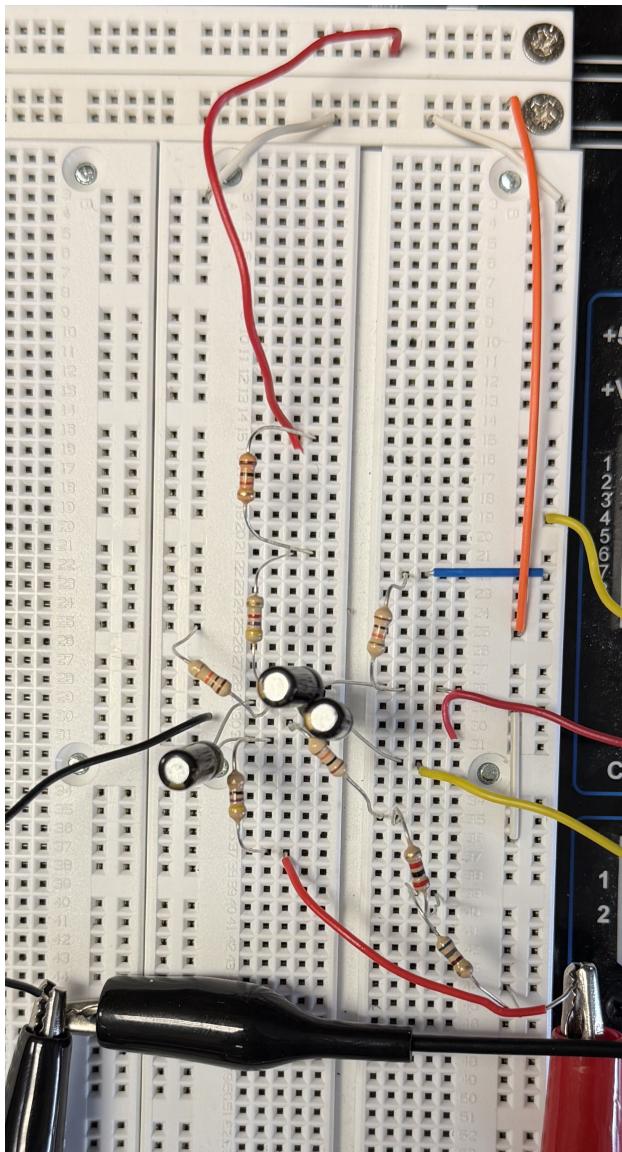


Figure 2: The prototyped NMOS CS amplifier circuit on the breadboard.

Part 3: Measurements Several measurements were taken from the prototyped circuit.

- **DC Bias Point:** A digital multimeter was used to measure the DC voltages at the gate (V_G), source (V_S), and drain (V_D). All resistor values were also measured.
- **AC Voltage Gain:** A function generator applied a $20 \text{ mV}_{\text{pk-pk}}$, 1 kHz sinusoid, and an oscilloscope was used to measure the AC output (v_o) and input (v_{sig}) waveforms to determine the gain A_v .
- **Output Resistance:** The load resistor R_L was replaced with a $1 \text{ M}\Omega$ resistor and the output amplitude was measured. R_L was then adjusted (using a $4.7 \text{ k}\Omega$ resistor) until

the output amplitude was approximately 50% of this "open-load" value. This value of R_L is equal to the output resistance R_o .

Finally, post-measurement calculations were performed to find the experimental I_D , A_v , and R_o , and all three sets of results (hand-calculated, simulated, and measured) were compared.

4 Results and Conclusions (Discussion)

4.1 Hand Calculations (Design)

4.1.1 DC Operating Point Analysis

Given Parameters

- **Voltage Supplies:** $V_+ = 15 \text{ V}$, $V_- = -15 \text{ V}$
- **Design Goals:** $I_D = 1 \text{ mA}$, $A_v \leq -5 \text{ V/V}$
- **Circuit Resistors:** $R_{sig} = 50 \Omega$, $R_L = 10 \text{ k}\Omega$, $R_G = 10 \text{ k}\Omega$
- **Transistor Parameters (2N7000):** $\lambda = 0.0146 \text{ V}^{-1}$, $k_n = 1.08 \text{ mA V}^{-2}$, $V_{tn} = 1.45 \text{ V}$

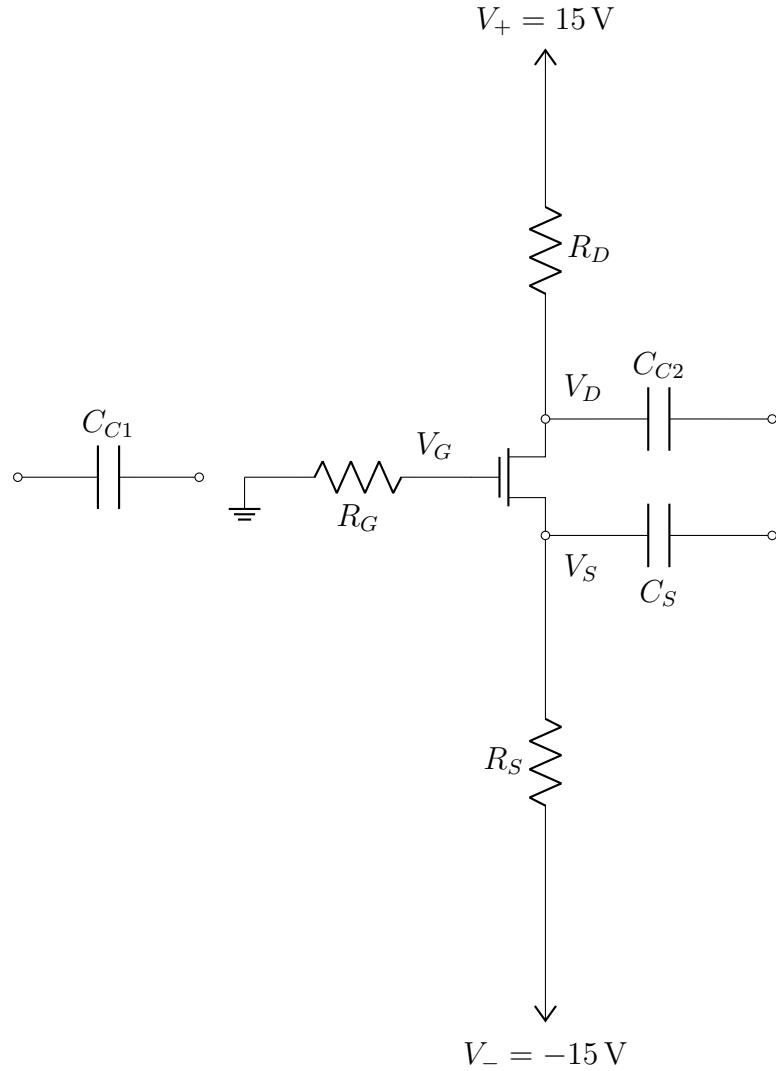


Figure 3: DC Model of the Common-Source Amplifier

1. DC Gate Current and Voltage (I_G, V_G) The DC gate current I_G for a MOSFET is effectively 0 A. Assuming R_G connects the gate to ground, the DC voltage drop is $I_G \cdot R_G = 0\text{ V}$. Therefore, the DC gate voltage is $V_G = 0\text{ V}$.

2. Overdrive Voltage (V_{OV}) Using the saturation current equation for the design goal $I_D = 1\text{ mA}$:

$$I_D = \frac{1}{2}k_n(V_{OV})^2$$

$$1\text{ mA} = \frac{1}{2}(1.08\text{ mA V}^{-2})(V_{OV})^2$$

$$V_{OV}^2 = \frac{2\text{ mA}}{1.08\text{ mA V}^{-2}} \approx 1.8519\text{ V}^2$$

$$V_{OV} = \sqrt{1.8519 \text{ V}^2} \approx 1.361 \text{ V}$$

3. Transconductance (g_m) and Gate-Source Voltage (V_{GS})

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2 \cdot 1 \text{ mA}}{1.361 \text{ V}} \approx 1.4695 \text{ mA V}^{-1} \text{ (or } 1.47 \text{ mS)}$$

$$V_{GS} = V_{OV} + V_{tn} = 1.361 \text{ V} + 1.45 \text{ V} = 2.811 \text{ V}$$

4. Early Effect Resistance (r_o)

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{(0.0146 \text{ V}^{-1})(1 \text{ mA})} \approx 68.5 \text{ k}\Omega$$

5. Source Resistor (R_S)

First, find the DC source voltage V_S using $V_G = 0 \text{ V}$:

$$V_{GS} = V_G - V_S \implies 2.811 \text{ V} = 0 \text{ V} - V_S \implies V_S = -2.811 \text{ V}$$

R_S connects the source terminal (V_S) to the negative supply ($V_- = -15 \text{ V}$). The DC current through it is $I_S = I_D = 1 \text{ mA}$.

$$R_S = \frac{V_S - V_-}{I_D} = \frac{-2.811 \text{ V} - (-15 \text{ V})}{1 \text{ mA}} = \frac{12.189 \text{ V}}{1 \text{ mA}} = 12.19 \text{ k}\Omega$$

A standard $12.1 \text{ k}\Omega$ resistor will be used.

4.1.2 AC Analysis

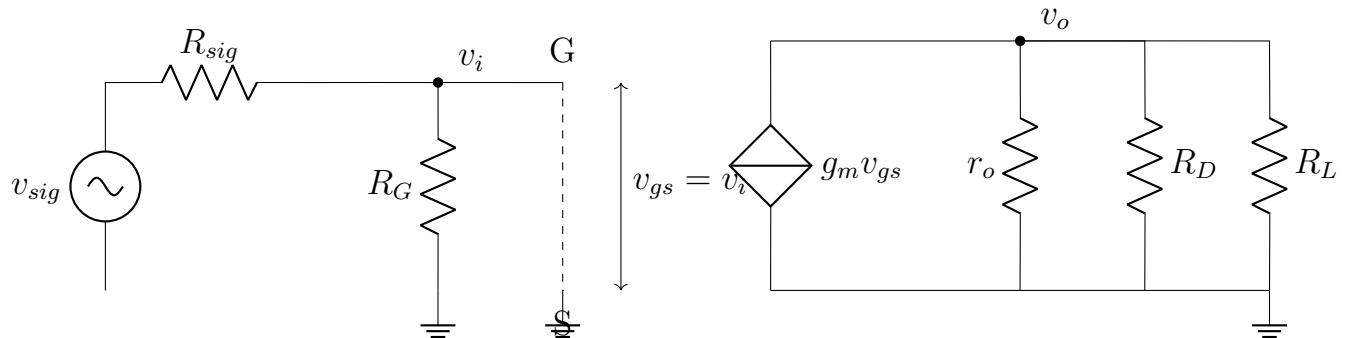


Figure 4: AC Small-Signal Model of the Common-Source Amplifier

1. Input Voltage Ratio (v_i/v_{sig})

The AC input resistance is $R_{in} = R_G = 10 \text{ k}\Omega$.

$$\frac{v_i}{v_{sig}} = \frac{R_G}{R_{sig} + R_G} = \frac{10\,000 \Omega}{50 \Omega + 10\,000 \Omega} \approx 0.995$$

(We will approximate $v_i \approx v_{sig}$).

2. Drain Resistor (R_D) for Gain $A_v = -5 \text{ V/V}$ The AC bypass capacitor C_S shorts R_S to ground. The gain is:

$$A_v = -g_m(r_o \parallel R_D \parallel R_L)$$

Solving for R_D to get $A_v = -5 \text{ V/V}$:

$$-5 \text{ V/V} = -(1.4695 \text{ mS})(68.5 \text{ k}\Omega \parallel R_D \parallel 10 \text{ k}\Omega)$$

Let $R'_L = r_o \parallel R_L = 68.5 \text{ k}\Omega \parallel 10 \text{ k}\Omega \approx 8.726 \text{ k}\Omega$.

$$5 = (1.4695 \text{ mS})(R_D \parallel 8.726 \text{ k}\Omega)$$

Let $R_{eq} = R_D \parallel 8.726 \text{ k}\Omega$.

$$R_{eq} = \frac{5}{1.4695 \text{ mS}} \approx 3.4025 \text{ k}\Omega$$

Now, solve for R_D :

$$\frac{1}{R_D} = \frac{1}{R_{eq}} - \frac{1}{R'_L} = \frac{1}{3.4025 \text{ k}\Omega} - \frac{1}{8.726 \text{ k}\Omega} \approx 0.1793 \text{ mS}$$

$$R_D = \frac{1}{0.1793 \text{ mS}} \approx 5.577 \text{ k}\Omega$$

A standard 5.6 kΩ resistor will be used.

3. DC Drain Voltage (V_D) and Saturation Check Using $R_D = 5.577 \text{ k}\Omega$:

$$V_D = V_+ - I_D R_D = 15 \text{ V} - (1 \text{ mA})(5.577 \text{ k}\Omega) = 9.423 \text{ V}$$

Check saturation condition: $V_{DS} \geq V_{OV}$.

$$V_{DS} = V_D - V_S = 9.423 \text{ V} - (-2.811 \text{ V}) = 12.234 \text{ V}$$

Since $V_{DS}(12.234 \text{ V}) \geq V_{OV}(1.361 \text{ V})$, the transistor is in saturation.

4. Amplifier Output Resistance (R_o) The output resistance R_o is R_D in parallel with r_o .

$$R_o = R_D \parallel r_o = 5.577 \text{ k}\Omega \parallel 68.5 \text{ k}\Omega \approx 5.157 \text{ k}\Omega$$

4.2 Simulation Results

Table 1: Simulation Results

Parameter	Simulated Value
V_G	0.000 V
V_D	9.314 V
V_S	-2.715 V
V_{GS}	2.715 V
V_{DS}	12.029 V
I_D	1.015 mA
$A_v = v_o/v_i$	-5.487 V/V

4.3 Measurement Data

Table 2: Measured Component Values

Component	Measured Value
R_D (5.600 k Ω nominal)	5.650 k Ω
R_S (12.100 k Ω nominal)	12.110 k Ω
R_G (10.000 k Ω nominal)	9.670 k Ω
R_L (10.000 k Ω nominal)	9.400 k Ω
R_{sig} (50.000 Ω nominal)	46.100 Ω

Table 3: Measured DC and AC Values

Parameter	Measured Value
V_G	0.000 V
V_D	7.540 V
V_S	-2.256 V
v_{sig} (pk-pk)	20.800 mV
v_o (pk-pk, $R_L = 9.400$ k Ω)	68.000 mV
R_o (from 50% amplitude)	≈ 4.700 k Ω

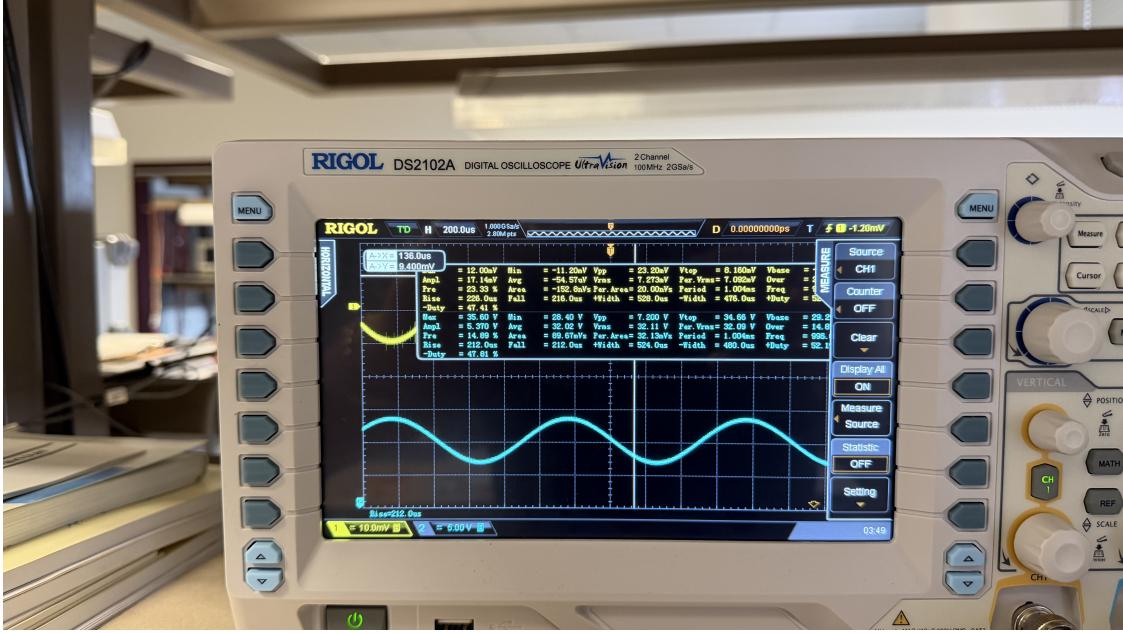
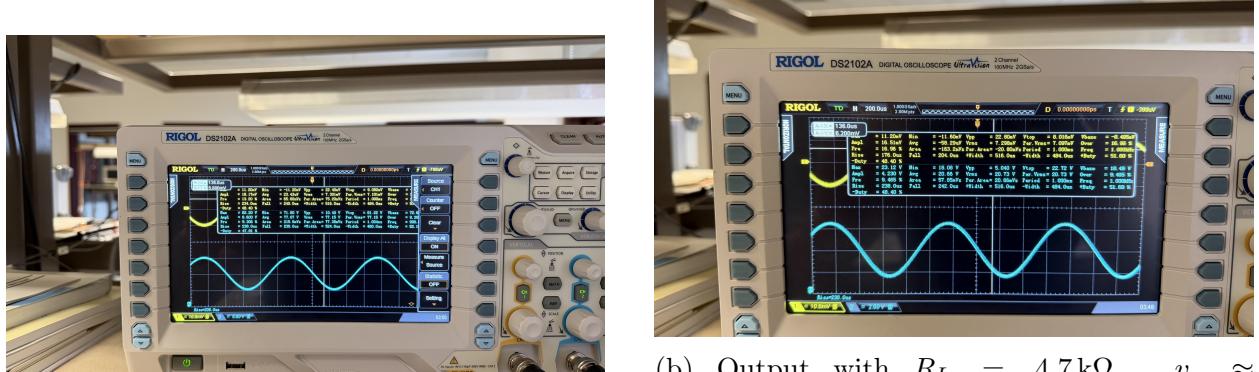


Figure 5: Oscilloscope reading for AC gain (A_v) with $R_L = 9.4 \text{ k}\Omega$. Ch1 (Yellow): $v_{sig} = 20.8 \text{ mV}_{\text{pk-pk}}$. Ch2 (Blue): $v_o = 68 \text{ mV}_{\text{pk-pk}}$.



(a) "Open-load" ($R_L \approx 1 \text{ M}\Omega$) output $v_o \approx 104 \text{ mV}_{\text{pk-pk}}$.

(b) Output with $R_L = 4.7 \text{ k}\Omega$. $v_o \approx 52 \text{ mV}_{\text{pk-pk}}$, which is 50% of the open-load voltage.

Figure 6: Oscilloscope measurements for determining the output resistance R_o .

Post-Measurement Calculations Using measured values from Tables 2 and 3, and measured $V_+ = 15.036 \text{ V}$ and $V_- = -15.079 \text{ V}$:

$$V_{GS} = V_G - V_S = 0 \text{ V} - (-2.256 \text{ V}) = 2.256 \text{ V}$$

$$V_{DS} = V_D - V_S = 7.54 \text{ V} - (-2.256 \text{ V}) = 9.796 \text{ V}$$

$$I_D = \frac{V_S - V_-}{R_S} = \frac{-2.256 \text{ V} - (-15.079 \text{ V})}{12.11 \text{ k}\Omega} = \frac{12.823 \text{ V}}{12.110 \Omega} = 1.059 \text{ mA}$$

Calculate v_i from measured v_{sig} :

$$v_i = v_{sig} \frac{R_G}{R_{sig} + R_G} = 20.8 \text{ mV} \frac{9.67 \text{ k}\Omega}{46.1 \Omega + 9.67 \text{ k}\Omega} = 20.70 \text{ mV}$$

$$A_v = v_o/v_i = \frac{-68 \text{ mV}}{20.70 \text{ mV}} = -3.285 \text{ V/V}$$

R_o = Value from Table 3 $\approx 4.7 \text{ k}\Omega$

4.4 Comparison of Results

Table 4: Comparison of Calculated, Simulated, and Measured Values

Parameter	Hand Calc (Goal)	Simulation	Measured
V_{GS}	2.811 V	2.715 V	2.256 V
V_{DS}	12.234 V	12.029 V	9.796 V
I_D	1.000 mA	1.015 mA	1.059 mA
A_v	-5.000 V/V	-5.487 V/V	-3.285 V/V
R_o	5.157 k Ω	(N/A)	4.700 k Ω

4.5 Discussion

The results from the hand calculations and the LTspice simulation show excellent agreement. The simulated I_D of 1.015 mA was within 1.5% of the 1.0 mA design goal, and the simulated gain $A_v = -5.487 \text{ V/V}$ was very close to the target of -5.0 V/V . This validates the design equations and the simulation model.

Comparing the measured results to the calculated and simulated values reveals several discrepancies, which can be explained by variations in the physical transistor parameters.

- **DC Operating Point:** The measured I_D (1.059 mA) was very close to the design goal (1.0 mA). However, the measured V_{GS} (2.256 V) was significantly *lower* than the calculated (2.811 V) and simulated (2.715 V) values. As noted in the lab manual, the most likely cause is that the threshold voltage (V_{tn}) of the specific 2N7000 transistor used was lower than the 1.45 V value from the datasheet used in the calculations. A lower V_{tn} would require a smaller V_{GS} to achieve the same I_D .
- **Voltage Gain (A_v):** The measured gain $A_v = -3.285 \text{ V/V}$, supported by the data in Figure 5, was substantially lower than the calculated goal (-5.0 V/V) and the simulation (-5.487 V/V). The gain is given by $A_v = -g_m(R_{eq})$, where $R_{eq} = R_D \parallel$

$r_o \parallel R_L$. The measured R_{eq} (using measured component values) is $\approx 3.42 \text{ k}\Omega$, which is very close to the design value. This implies that the discrepancy must come from the transconductance, g_m .

The measured g_m can be estimated as $|A_v|/R_{eq} = 3.285/3.42 \text{ k}\Omega \approx 0.96 \text{ mS}$. This is much lower than the calculated $g_m = 1.47 \text{ mS}$. Since $g_m = \sqrt{2k_n I_D}$ and the measured I_D was accurate, this strongly suggests that the actual process transconductance parameter (k_n) of the transistor was significantly lower than the 1.08 mA/V^2 value used in the design.

- **Output Resistance (R_o):** The measured output resistance was $R_o \approx 4.7 \text{ k}\Omega$. This was determined by finding the load R_L that caused the output amplitude to drop to 50% of its "open-load" value, as shown in Figure 6. This result is in good agreement with the calculated value of $R_o = R_D \parallel r_o = 5.157 \text{ k}\Omega$. A theoretical R_o based on measured component values ($R_D = 5.65 \text{ k}\Omega$ and $r_o \approx 64.7 \text{ k}\Omega$) would be $5.19 \text{ k}\Omega$. The measured value is close to this and correctly follows the hint $R_o \leq R_D$ ($4.7 \text{ k}\Omega \leq 5.65 \text{ k}\Omega$).
- **Further Exploration:** When the input signal amplitude was increased to $1 \text{ V}_{\text{pk-pk}}$, the output waveform began to show significant distortion (clipping), as seen in Figure 7. This occurs because the large-signal v_{gs} violates the small-signal condition ($v_{gs} \ll 2V_{OV}$) and pushes the transistor out of the saturation region (into cutoff or triode), which is required for linear amplification.



Figure 7: Output signal distortion (clipping) when the input signal v_{sig} was increased to $\approx 1 \text{ V}_{\text{pk-pk}}$.

4.6 Conclusion

This lab successfully demonstrated the design, simulation, and implementation of an NMOS common-source amplifier. The design goals were closely met in simulation, but the physical prototype showed deviations in performance. The measured gain ($A_v = -3.285 \text{ V/V}$) was lower than the -5.0 V/V target, while the DC bias current ($I_D = 1.059 \text{ mA}$) was very accurate.

The discrepancies between theory and measurement are primarily attributed to the inherent variations in the 2N7000 transistor's physical parameters, specifically a lower-than-assumed V_{tn} and k_n . The measured output resistance $R_o \approx 4.7 \text{ k}\Omega$ showed good agreement with the theoretical value. This exercise successfully highlighted the core principles of CS amplifier operation and the significant impact of real-world component tolerances on circuit performance.

5 Bibliography

- [1] Fixel, Debora. "ENGR 305 - Lab 9: NMOS Common-Source Amplifier." Trinity College, Hartford, CT, October 2025.
- [2] Microchip Technology Inc. "2N7000 N-Channel Enhancement-Mode Vertical DMOS FET." Datasheet, DS20005695A, 2021.