Engineering Midterm Notesheet
Chapters 3-5

ENGR 305

Key Constants & Values

- **Elementary Charge (q):** 1.602×10^{-19} C
- **Thermal Voltage (V_T) at 300K (Room Temp):** $V_T = kT/q = 25.9$ mV
- **Intrinsic Silicon (n_i) at 300K:** $\approx 1.5 \times 10^{10}$ carriers/cm^3
- **Permittivity of Silicon (ϵ_s):** 1.04×10^{-12} F/cm
- **Constant Voltage Drop (CVD) Model:** Assume $V_D \approx 0.7$ V for a conducting silicon diode unless specified otherwise.

Chapter 3: Semiconductors

- **Intrinsic Semiconductors:** Pure silicon (Si). Covalent bonds. At 0K, it's an insulator. At room temp, thermal generation creates free electrons and holes.
  - $n = p = n_i$ (electron and hole concentrations are equal)
  - **Mass Action Law:** $np = n_i^2$ (holds for intrinsic and doped silicon in thermal equilibrium)
- **Doped Semiconductors:**
  - **n-type:** Doped with a pentavalent element (e.g., Phosphorus). These are **donors** (N_D).
    - Majority carriers: electrons ($n_n \approx N_D$)
    - Minority carriers: holes ($p_n = n_i^2/N_D$)
  - **p-type:** Doped with a trivalent element (e.g., Boron). These are **acceptors** (N_A).
    - Majority carriers: holes ($p_p \approx N_A$)
    - Minority carriers: electrons ($n_p = n_i^2/N_A$)

- **Current Flow Mechanisms:**
  - **Drift Current:** Movement of carriers due to an electric field (E).
    - Electron drift velocity: $v_{n-drift} = -\mu_n E$
    - Hole drift velocity: $v_{p-drift} = \mu_p E$
    - Total Drift Current Density (J_{drift}): $J_{drift} = q(n\mu_n + p\mu_p)E$
    - (μ_n and μ_p are electron and hole mobilities)
  - **Diffusion Current:** Movement of carriers from a high-concentration area to a low-concentration area (due to a concentration gradient).
    - Hole Diffusion: $J_p = -qD_p \frac{dp}{dx}$
    - Electron Diffusion: $J_n = qD_n \frac{dn}{dx}$
    - (D_n and D_p are the diffusion constants)
- **Einstein Relation:** Relates mobility (μ) and diffusion constant (D).
  - $D_n = V_T \mu_n$
  - $D_p = V_T \mu_p$

Chapter 4: Diodes

- **The pn Junction (Open Circuit):**
  - A **depletion region** (or space-charge region) forms at the junction, clear of free carriers.
  - Contains uncovered bound charges: positive donors (N_D) on the n-side, negative acceptors (N_A) on the p-side.
  - This charge creates a built-in voltage (V_0): $V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$.
  - Two currents balance at equilibrium: **diffusion current** (I_D) and **drift current** (I_S). I_S is the saturation current.
- **Diode I-V Models:**
  1. **Exponential Model (Shockley Equation):** Most accurate.
     - $i_D = I_S(e^{v_D/(nV_T)} - 1)$
     - I_S is the saturation current (typically 10^{-15} A).
     - n is the ideality factor (usually 1 to 2).
     - At room temp, $V_T \approx 25$ mV.
     - For $v_D \gg V_T$, $i_D \approx I_S e^{v_D/(nV_T)}$.
     - A 60mV increase in v_D (for $n = 1$) increases i_D by $\approx 10\times$.

2. **Constant-Voltage-Drop (CVD) Model:** Most common for hand analysis.
   - If conducting: $v_D = 0.7$ V (acts as a 0.7V battery).
   - If off: $i_D = 0$ (acts as an open circuit).
   - Turn-on threshold is $v_D \approx 0.5$ V (cut-in voltage).
3. **Ideal Diode Model:** A simple switch.
   - If conducting (forward-biased): $v_D = 0$ V (short circuit).
   - If off (reverse-biased): $i_D = 0$ (open circuit).

- **Small-Signal Model (for DC bias point Q):**
  - First, solve for DC values (I_D, V_D) using the CVD or exponential model.
  - Then, for small ac signals, replace the diode with its **small-signal resistance** (r_d):
  - $r_d = \frac{nV_T}{I_D}$
- **Zener Diode (Breakdown Region):**
  - Used for voltage regulation. Operates in reverse breakdown.
  - Model: $V_Z = V_{Z0} + r_z I_Z$
    * V_{Z0}: Zener voltage at $I_Z \approx 0$.
    * r_z: Zener incremental resistance.
- **Diode Capacitance:**
  - **Junction/Depletion Capacitance (C_j):** Dominant in reverse bias.
    * $C_j = \frac{C_{j0}}{(1+V_R/V_0)^m}$ (where $m \approx 0.5$ for abrupt junction)
  - **Diffusion Capacitance (C_d):** Dominant in forward bias. Proportional to current.
    * $C_d = \left(\frac{\tau_T}{V_T}\right) I_D$ (where τ_T is transit time)
- **Rectifier Circuits:**
  - **Half-Wave (HW):** One diode. PIV $= V_s$(peak). V_O(peak) $= V_s$(peak) $- V_D$.
  - **Full-Wave (FW) - Center-Tapped:** Two diodes. PIV $= 2V_s$(config) $- V_D$. V_O(peak) $= V_s$(peak) $- V_D$.
  - **Full-Wave (FW) - Bridge:** Four diodes. PIV $= V_s$(peak) $- V_D$. V_O(peak) $= V_s$(peak) $- 2V_D$.
- **Peak Rectifier (HW with Filter Capacitor C):**
  - Output V_O is approximately the peak input, V_p, minus a small **ripple voltage** (V_r).
  - Capacitor discharges through R_L when diode is off.

- For $CR_L \gg T$ (period of input): $V_r \approx \frac{V_p}{fCR_L} = \frac{I_L}{fC}$
- For FW Rectifier: $V_r \approx \frac{V_p}{2fCR_L} = \frac{I_L}{2fC}$
- Diode conducts for a short interval (Δt) near the peak to replenish capacitor charge.
- Diode current is large and pulsed: $i_{D,avg} \approx I_L(1 + \pi\sqrt{2V_p/V_r})$.

Chapter 5: MOSFETs

- **Structure:** n-channel (NMOS) and p-channel (PMOS). Terminals are Gate (G), Drain (D), Source (S), Body (B).
- **Parameters:**
  - **Threshold Voltage (V_t):** V_{tn} for NMOS (positive), V_{tp} for PMOS (negative).
  - **Oxide Capacitance (C_{ox}):** $C_{ox} = \epsilon_{ox}/t_{ox}$.
  - **Process Transconductance (k'):** $k'_n = \mu_n C_{ox}$, $k'_p = \mu_p C_{ox}$.
  - **Transistor Transconductance (k):** $k_n = k'_n(W/L)$, $k_p = k'_p(W/L)$.
- **Overdrive Voltage (V_{OV}):** The key control voltage.
  - NMOS: $V_{OV} = V_{GS} - V_{tn}$
  - PMOS: $|V_{OV}| = V_{SG} - |V_{tp}|$
- **Channel-Length Modulation (λ):**
  - Models the slight increase in i_D with v_{DS} in saturation.
  - $i'_D = i_D(1 + \lambda v_{DS})$
  - **Output Resistance (r_o):** $r_o = \frac{V_A}{I_D} \approx \frac{1}{\lambda I_D}$ (where $V_A = 1/\lambda$ is the Early Voltage).

Regions of Operation (Tables 5.1 & 5.2 are provided on exam)

NMOS Transistor

1. **Cutoff:**
   - **Condition:** $V_{GS} < V_{tn}$
   - **Current:** $i_D = 0$
2. **Triode (Linear) Region:**
   - **Conditions:** $V_{GS} \geq V_{tn}$ AND $V_{DS} < V_{OV}$ (or $V_{GD} > V_{tn}$)
   - **Current:** $i_D = k_n\left[(V_{GS} - V_{tn})V_{DS} - \frac{1}{2}V_{DS}^2\right]$

- Acts like a voltage-controlled resistor. For small V_{DS}: $r_{DS} = \frac{1}{k_n V_{OV}}$.

3. **Saturation Region:** (Used for amplifiers)
   - **Conditions:** $V_{GS} \geq V_{tn}$ AND $V_{DS} \geq V_{OV}$ (or $V_{GD} \leq V_{tn}$)
   - **Current:** $i_D = \frac{1}{2}k_n(V_{GS} - V_{tn})^2 = \frac{1}{2}k_n V_{OV}^2$
   - Acts like a voltage-controlled current source.

PMOS Transistor

(Use V_{SG}, V_{SD}, $|V_{tp}|$, k_p)

1. **Cutoff:**
   - **Condition:** $V_{SG} < |V_{tp}|$
   - **Current:** $i_D = 0$
2. **Triode (Linear) Region:**
   - **Conditions:** $V_{SG} \geq |V_{tp}|$ AND $V_{SD} < |V_{OV}|$
   - **Current:** $i_D = k_p\left[(V_{SG} - |V_{tp}|)V_{SD} - \frac{1}{2}V_{SD}^2\right]$
3. **Saturation Region:**
   - **Conditions:** $V_{SG} \geq |V_{tp}|$ AND $V_{SD} \geq |V_{OV}|$
   - **Current:** $i_D = \frac{1}{2}k_p(V_{SG} - |V_{tp}|)^2 = \frac{1}{2}k_p|V_{OV}|^2$

Homeworks 1-4: Problem-Solving Steps

- **DC Analysis of Diode Circuits:**
  1. Assume a state for each diode (ON or OFF) based on inspection.
  2. Model ON diodes as 0.7V sources (CVD model) and OFF diodes as open circuits.
  3. Solve the resulting linear circuit for all currents and voltages.
  4. **Check assumptions:**
     - If a diode was assumed ON, check if $i_D > 0$.
     - If a diode was assumed OFF, check if $v_D < 0.7$ V.
  5. If any assumption is wrong, change the state of that diode and re-solve.
- **DC Analysis of MOSFET Circuits (from Slides, e.g., Ex. 5.3, 5.6):**
  1. **Assume** a region of operation for the MOSFET (usually **Saturation** for amplifiers).

2. Write the i_D equation for that region (e.g., $i_D = \frac{1}{2}k_n V_{OV}^2$).
3. Write KVL/KCL equations for the rest of the circuit (e.g., $V_G = ...$, $V_S = ...$, $V_D = ...$).
4. Substitute known relationships (e.g., $V_{OV} = V_{GS} - V_{tn}$, $V_{GS} = V_G - V_S$, $i_D = i_S$).
5. Solve the system of equations for the unknown currents and node voltages (e.g., i_D, V_S, V_D).
6. **Check assumptions:**
   - If Saturation was assumed: Verify that $V_{DS} \geq V_{OV}$ (for NMOS) or $V_{SD} \geq |V_{OV}|$ (for PMOS).
   - If Triode was assumed: Verify that $V_{DS} < V_{OV}$ (for NMOS) or $V_{SD} < |V_{OV}|$ (for PMOS).
7. If the assumption is wrong, re-assume the correct region and re-solve from Step 2.

- **Small-Signal Diode Problems:**
  1. First, solve the DC circuit (using CVD model) to find the DC bias current I_D.
  2. Calculate the small-signal resistance: $r_d = nV_T/I_D$.
  3. Create the small-signal equivalent circuit: Replace the diode with r_d, turn off DC voltage sources (short to ground), and turn off DC current sources (open circuit).
  4. Solve the small-signal circuit for the required ac quantity (e.g., v_o/v_i).