

# ENGR 305 Midterm Notesheet

Chapters 3-5, Homeworks 1-4

## Content Summary & Key Formulas

### Chapter 3: Semiconductors

#### Intrinsic Carrier Concentration ( $n_i$ )

The concentration of free electrons and holes in pure (intrinsic) silicon, dependent on temperature ( $T$  in Kelvin).

$$n_i = B \cdot T^{3/2} \cdot e^{-E_g/(2kT)}$$

- **For Silicon (Si):**  $E_g \approx 1.12$  eV;  $B = 7.3 \times 10^{15} \text{ cm}^{-3} K^{-3/2}$
  - **At 300K:**  $n_i \approx 1.5 \times 10^{10} \text{ cm}^{-3}$
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#### Carrier Concentrations (Doped)

- **Mass-Action Law:**  $p \cdot n = n_i^2$
  - **n-type ( $N_D$ ):** Majority  $n_n \approx N_D$ ; Minority  $p_n \approx n_i^2/N_D$
  - **p-type ( $N_A$ ):** Majority  $p_p \approx N_A$ ; Minority  $n_p \approx n_i^2/N_A$
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#### Conductivity ( $\sigma$ ) & Resistivity ( $\rho$ )

- **Drift Current:**  $J_{\text{drift}} = q(n\mu_n + p\mu_p)\mathcal{E}$
  - **Conductivity:**  $\sigma = q(n\mu_n + p\mu_p)$
  - **Resistivity:**  $\rho = 1/\sigma$
  - **Diffusion Current:**  $J_p = -qD_p \frac{dp}{dx}$ ;  $J_n = qD_n \frac{dn}{dx}$
  - **Einstein Relation:**  $D/\mu = V_T$
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#### pn Junction Built-in Potential ( $V_0$ )

The voltage across the depletion region in thermal equilibrium.

$$V_0 = V_T \ln \left( \frac{N_A N_D}{n_i^2} \right)$$

- **Thermal Voltage ( $V_T$ ):**  $V_T = kT/q \approx 25.9$  mV at 300K.
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#### pn Junction Depletion Region ( $W$ )

- **Total Width (with  $V_R$ ):**  $W = \sqrt{\frac{2\epsilon_s}{q} \left( \frac{1}{N_A} + \frac{1}{N_D} \right) (V_0 + V_R)}$
- **Individual Widths:**  $x_n = W \frac{N_A}{N_A + N_D}$ ;  $x_p = W \frac{N_D}{N_A + N_D}$

## Chapter 4: Diodes

### Exponential Model (Shockley Eq)

$$i_D = I_S(e^{v_D/V_T} - 1)$$

- $I_S$  is the saturation current.
  - **Finding new V/I:**  $V_2 - V_1 = V_T \ln(I_2/I_1)$
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### Diode Circuit Models

1. **Ideal Diode:** 0V short circuit (forward), open circuit (reverse).
  2. **Constant Voltage Drop (CVD):** 0.7V battery (forward), open circuit (reverse).
  3. **Small-Signal Model:** A resistor  $r_d = V_T/I_D$  for AC analysis.
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### Rectifier Circuits

- **Half-Wave:** Uses one diode. Output  $v_O = v_S - V_D$  (on positive cycle).  $PIV = V_{\text{peak}}$ .
  - **Full-Wave (Center-Tap):** Uses two diodes. Output  $v_O = V_S - V_D$ .  $PIV = 2V_S - V_D$ .
  - **Full-Wave (Bridge):** Uses four diodes. Output  $v_O = V_S - 2V_D$ .  $PIV = V_S - V_D$ .
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### Peak Rectifier (Filter Capacitor)

A capacitor (C) in parallel with the load (R).

- Diode conducts for a short time ( $\Delta t$ ) to charge C to  $V_p$ .
  - C discharges through R, creating a small ripple  $V_r$ .
  - **Ripple Voltage:**  $V_r \approx \frac{V_p}{fCR} \approx \frac{I_L}{fC}$
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### Voltage Regulation

- **Line Regulation:**  $\Delta v_O = \Delta V_{\text{supply}} \cdot \frac{r}{r+R}$
- **Load Regulation:**  $\Delta v_O = -(\Delta I_{\text{diodes}}) \cdot r$
- **Zener Model:**  $V_Z = V_{Z0} + r_z I_Z$

## Chapter 5: MOSFETs

### Key Parameters

- **Overdrive Voltage ( $v_{OV}$ ):**  $v_{OV} = v_{GS} - V_{tn}$  (NMOS);  $|v_{OV}| = v_{SG} - |V_{tp}|$  (PMOS).
  - **Process Transconductance:**  $k'_n = \mu_n C_{ox}$ ;  $k'_p = \mu_p C_{ox}$ .
  - **MOSFET Transconductance:**  $k_n = k'_n (W/L)$ ;  $k_p = k'_p (W/L)$ .
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### NMOS Regions of Operation

#### 1. Cutoff:

- **Condition:**  $v_{GS} < V_{tn}$
- **Current:**  $i_D = 0$

#### 2. Triode (Linear):

- **Condition:**  $v_{GS} \geq V_{tn}$  AND  $v_{DS} < v_{OV}$
- **Current:**  $i_D = k_n [(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2]$
- **Resistor (small  $v_{DS}$ ):**  $r_{DS} = 1/(k_n v_{OV})$

#### 3. Saturation (Active):

- **Condition:**  $v_{GS} \geq V_{tn}$  AND  $v_{DS} \geq v_{OV}$
  - **Current (ideal):**  $i_D = \frac{1}{2}k_n v_{OV}^2 = \frac{1}{2}k_n (v_{GS} - V_{tn})^2$
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### PMOS Regions of Operation

(Uses positive  $v_{SG}$ ,  $v_{SD}$ , and  $|V_{tp}|$ )

#### 1. Cutoff:

- **Condition:**  $v_{SG} < |V_{tp}|$
- **Current:**  $i_D = 0$

#### 2. Triode (Linear):

- **Condition:**  $v_{SG} \geq |V_{tp}|$  AND  $v_{SD} < |v_{OV}|$
- **Current:**  $i_D = k_p [(v_{SG} - |V_{tp}|)v_{SD} - \frac{1}{2}v_{SD}^2]$

#### 3. Saturation (Active):

- **Condition:**  $v_{SG} \geq |V_{tp}|$  AND  $v_{SD} \geq |v_{OV}|$
  - **Current (ideal):**  $i_D = \frac{1}{2}k_p |v_{OV}|^2 = \frac{1}{2}k_p (v_{SG} - |V_{tp}|)^2$
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### Channel-Length Modulation (Saturation Effect)

As  $v_{DS}$  increases past  $v_{OV}$ , the channel pinch-off point moves, shortening the effective channel length  $L_{\text{eff}}$ . This causes  $i_D$  to **increase** slightly with  $v_{DS}$ .

- **Updated Current (NMOS):**  $i_D = \frac{1}{2}k_n v_{OV}^2 (1 + \lambda v_{DS})$
  - **Early Voltage:**  $V_A = 1/\lambda$
  - **Output Resistance:**  $r_o = \frac{V_A}{I_D}$  (where  $I_D$  is the ideal current).
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## MOSFET DC Circuit Analysis

1. **Assumptions:**  $I_G = 0$ . For amplifiers, **assume SATURATION**.
2. **Find  $V_G$ :** Use KVL at the gate (e.g., voltage divider).
3. **Write  $V_{GS}$  and  $I_D$  Equations:**
  - KVL at G-S loop:  $V_{GS} = V_G - V_S = V_G - I_D R_S$
  - Saturation Current:  $I_D = \frac{1}{2} k_n (V_{GS} - V_{tn})^2$
4. **Solve** for  $I_D$  and  $V_{GS}$ .
5. **Find Voltages:**  $V_D = V_{DD} - I_D R_D$ ;  $V_S = I_D R_S$  (or  $V_S = V_{SS} + I_D R_S$ ).
6. **VERIFY:** Check if  $V_{DS} \geq V_{OV}$  (where  $V_{DS} = V_D - V_S$ ).
7. **If False:** Assumption was wrong. Re-solve using the **Triode** equation.
8. **Diode-Connected:** If  $V_G = V_D$ , the transistor is *always in saturation* (if on).

## Midterm Learning Objectives

1. Calculate the intrinsic carrier concentration in a semiconductor.
2. Determine minority and majority carrier concentrations (electron and hole concentrations) in a semiconductor.
3. Calculate the built-in potential of a pn junction.
4. Calculate the depletion region width of a pn junction.
5. Given the voltage and current for a forward-biased diode, be able to calculate the current at a different value of voltage (or the voltage at a different value of current).
6. Be able to determine voltages and currents at points in a diode circuit, using either the ideal diode model or the constant voltage drop (0.7V) model.
7. Understand the operation of half-wave rectifiers.
8. Be able to calculate resistivity and conductivity in a semiconductor.
9. Perform drain current calculations for NMOS and PMOS transistors. Know the difference between the triode region and the saturation region of operation.
10. Discuss/explain the effect in a MOSFET when the channel pinches off and moves away from the drain (Finite Output Resistance in Saturation).
11. Be able to design an NMOS circuit with DC voltages. This may require determining resistor values needed or voltages and currents in the circuit.