ENGR 305 Lab 5

Sean Balbale

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Part 1: NMOS in Saturation Mode

This part requires designing the circuit to meet specific operating conditions. The goal is to find the values of the drain resistor (R_D) and the source resistor (R_S).

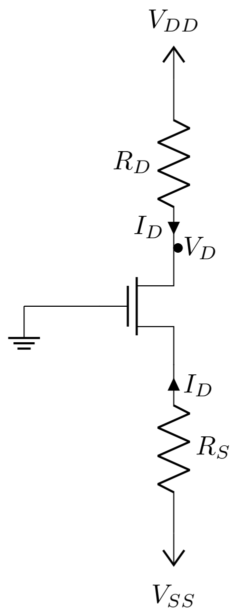
Given Parameters

- Drain Current: $I_D = 1.0$ mA
- Drain Voltage: $V_D = 5.0$ V
- Supply Voltages: $V_{DD} = +15$ V, $V_{SS} = -15$ V
- Threshold Voltage: $V_T = 2.0$ V
- Process Parameter: $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$
- Transistor Dimensions: $W = 32\ \mu$m, $L = 1\ \mu$m

1. Circuit Sketch

The circuit is a common-source NMOS amplifier with source degeneration. The gate is connected to ground ($V_G = 0$ V), the drain is connected to V_{DD} through R_D, and the source is connected to V_{SS} through R_S.

Part 1: NMOS in Saturation Mode



2. Calculation of R_D

The value of the drain resistor, R_D, can be found using Ohm's law. The voltage drop across R_D is the difference between the positive supply rail (V_{DD}) and the desired drain voltage (V_D). The current flowing through it is the drain current, I_D.

$$V_{RD} = V_{DD} - V_D$$
$$R_D = \frac{V_{DD} - V_D}{I_D}$$

Plugging in the given values:

$$R_D = \frac{15 \text{ V} - 5.0 \text{ V}}{1.0 \text{ mA}} = \frac{10 \text{ V}}{1.0 \times 10^{-3} \text{ A}} = 10,000\ \Omega$$

So, the required drain resistor is $R_D = 10\ \mathbf{k\Omega}$.

3. Calculation of Overdrive Voltage (V_{OV})

Since the transistor is operating in saturation, we use the saturation current equation to find the overdrive voltage ($V_{OV} = V_{GS} - V_T$).

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2 = \frac{1}{2}k_n'\left(\frac{W}{L}\right)V_{OV}^2$$

First, let's calculate the aspect ratio, W/L:

$$\frac{W}{L} = \frac{32\ \mu\text{m}}{1\ \mu\text{m}} = 32$$

Now, rearrange the equation to solve for V_{OV}:

$$V_{OV} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)}}$$

Plugging in the values:

$$V_{OV} = \sqrt{\frac{2 \times (1.0 \times 10^{-3} \text{ A})}{(100 \times 10^{-6} \text{ A/V}^2) \times 32}} = \sqrt{\frac{2 \times 10^{-3}}{3.2 \times 10^{-3}}} = \sqrt{0.625} \approx 0.791 \text{ V}$$

The required overdrive voltage is $V_{OV} \approx 0.791$ **V**.

4. Calculation of V_{GS} and V_S

With V_{OV} and V_T known, we can find the gate-source voltage, V_{GS}.

$$V_{GS} = V_{OV} + V_T = 0.791 \text{ V} + 2.0 \text{ V} = 2.791 \text{ V}$$

The gate of the transistor is connected to ground, so $V_G = 0$ V. We can use this to find the source voltage, V_S.

$$V_{GS} = V_G - V_S \implies V_S = V_G - V_{GS}$$
$$V_S = 0 \text{ V} - 2.791 \text{ V} = -2.791 \text{ V}$$

The calculated voltages are $V_{GS} \approx 2.791$ **V** and $V_S \approx -2.791$ **V**.

5. Calculation of R_S

Finally, we can find the source resistor, R_S, using Ohm's law. The voltage drop across R_S is the difference between the source voltage (V_S) and the negative supply rail (V_{SS}). The current is the source current, I_S, which equals I_D.

$$V_{RS} = V_S - V_{SS}$$
$$R_S = \frac{V_S - V_{SS}}{I_D}$$

Plugging in the values:

$$R_S = \frac{-2.791 \text{ V} - (-15 \text{ V})}{1.0 \text{ mA}} = \frac{12.209 \text{ V}}{1.0 \times 10^{-3} \text{ A}} \approx 12,209\ \Omega$$

The required source resistor is $R_S \approx 12.2\ \mathbf{k\Omega}$.

6. Post-Measurement Exercise

This section addresses the post-measurement questions for the NMOS circuit biased in the saturation region.

Measured Voltages: V_{GS} and V_{DS}

Based on the measurement data, the measured gate-to-source voltage is $V_{GS} = 1.3994$ **V**.
The drain-to-source voltage, V_{DS}, is calculated from the measured drain and source voltages:

- $V_D = 3.909$ V
- $V_S = -1.3994$ V

$$V_{DS} = V_D - V_S = 3.909 \text{ V} - (-1.3994 \text{ V}) = 5.3084 \text{ V}$$

Comparison and Discrepancies

Here's a comparison of the measured and calculated values:

- V_{GS}: Measured was 1.3994 **V**, while the calculated value was 2.791 **V**.
- V_{DS}: Measured was 5.3084 **V**, while the calculated value was $V_D - V_S = 5.0 \text{ V} - (-2.791 \text{ V}) =$ **7.791 V**.

The significant discrepancies are primarily due to the difference between the **assumed threshold voltage ($V_T = 2.0$ V)** used in the calculations and the actual V_T of the 2N7000 transistor used in the experiment. The actual V_T is much lower, meaning the transistor requires a smaller V_{GS} to turn on and conduct the target current. This lower required V_{GS} directly leads to a less negative V_S and a lower overall V_{DS}. Minor differences in resistor values and power supply voltages also contribute to the deviation.

Measured Drain Current (I_D)

The measured drain current, I_D, can be calculated using the measured voltages and resistor values.

1. Using the drain resistor (R_D)

- $V_+ = 15.027$ V
- $V_D = 3.909$ V
- $R_D = 9776.7\,\Omega$

$$I_D = \frac{V_+ - V_D}{R_D} = \frac{15.027 \text{ V} - 3.909 \text{ V}}{9776.7\,\Omega} \approx 1.137 \text{ mA}$$

2. Using the source resistor (R_S)

- $V_S = -1.3994$ V
- $V_- = -15.03$ V
- $R_S = 12022.325\,\Omega$

$$I_D = \frac{V_S - V_-}{R_S} = \frac{-1.3994 \text{ V} - (-15.03 \text{ V})}{12022.325\,\Omega} \approx 1.134 \text{ mA}$$

Both calculations yield a consistent result. The measured drain current is approximately 1.14 **mA**, which is reasonably close to the design target of 1.0 mA.

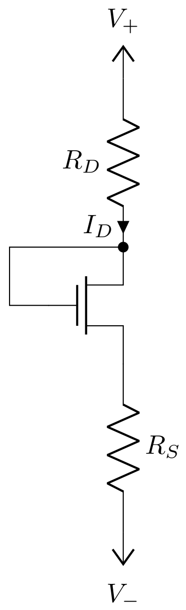
Part 2: Diode-Connected NMOS

In this configuration, the gate is connected directly to the drain ($V_G = V_D$). The goal is to find the values of V_S, V_D, and R_D.

Given Parameters

- Drain Current: $I_D = 1.0$ mA
- Source Resistor: $R_S = 15$ kΩ
- Supply Voltages: $V_+ = +15$ V, $V_- = -15$ V
- Transistor parameters are the same as in Part 1.

Part 2: Diode-Connected NMOS



1. Operating Region of the Transistor

For a diode-connected NMOS, the drain and gate are at the same potential, meaning $V_{DS} = V_{GS}$. The condition for an NMOS to be in the saturation region is $V_{DS} \geq V_{GS} - V_T$. Substituting V_{GS} for V_{DS}, the condition becomes:

$$V_{GS} \geq V_{GS} - V_T \implies 0 \geq -V_T \implies V_T \geq 0$$

Since this is an enhancement-type NMOS, V_T is positive (+2.0 V), so this condition is always met when the transistor is on. Therefore, the diode-connected transistor operates in the **saturation region**.

2. Calculation of Overdrive Voltage (V_{OV})

The calculation for V_{OV} is identical to Part 1 because the drain current ($I_D = 1.0$ mA) and the transistor parameters are the same.

$$V_{OV} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)}} \approx 0.791 \text{ V}$$

The overdrive voltage is $V_{OV} \approx 0.791$ **V**.

3. Calculation of V_S and V_D

First, let's find the source voltage, V_S.

$$V_S = V_- + (I_D \times R_S)$$

$$V_S = -15 \text{ V} + (1.0 \text{ mA} \times 15 \text{ k}\Omega) = -15 \text{ V} + 15 \text{ V} = 0 \text{ V}$$

Next, we find the drain voltage, V_D. We first need V_{GS}:

$$V_{GS} = V_{OV} + V_T = 0.791 \text{ V} + 2.0 \text{ V} = 2.791 \text{ V}$$

Since the gate is connected to the drain, $V_G = V_D$. Therefore:

$$V_{GS} = V_G - V_S = V_D - V_S$$

$$V_D = V_{GS} + V_S = 2.791 \text{ V} + 0 \text{ V} = 2.791 \text{ V}$$

The calculated voltages are $V_S = 0$ **V** and $V_D \approx 2.791$ **V**.

4. Calculation of R_D

Finally, we calculate the drain resistor, R_D, using Ohm's law.

$$R_D = \frac{V_+ - V_D}{I_D}$$

$$R_D = \frac{15 \text{ V} - 2.791 \text{ V}}{1.0 \text{ mA}} = \frac{12.209 \text{ V}}{1.0 \times 10^{-3} \text{ A}} \approx 12,209 \ \Omega$$

The required drain resistor is $R_D \approx 12.2$ **kΩ**.

5. Post-Measurement Exercise

This section addresses the post-measurement questions for the diode-connected NMOS circuit.

Comparison and Discrepancies

Here's a comparison of the key measured and calculated values for the circuit:

- V_D: Measured was 2.098 **V**, while the calculated value was 2.791 **V**.
- V_S: Measured was 0.7488 **V**, while the calculated value was 0 **V**.

The discrepancies can be explained as follows:

- The difference in V_D is, again, primarily caused by the **assumed V_T of** 2.0 **V** being much higher than the actual V_T of the physical transistor. A lower actual V_T results in a smaller required V_{GS} (and therefore V_D) to achieve the target current.
- The difference in V_S is not an error but a result of using a real resistor. The pre-lab calculation of $V_S = 0$ V was based on the negative supply ($V_- = -15$ V) being perfectly balanced by the voltage drop across an ideal $R_S = 15$ kΩ with exactly $I_D = 1.0$ mA flowing through it. The actual measured resistance was $R_S = 14.791$ kΩ and the actual current was slightly over 1.0 mA, resulting in a measured V_S of 0.7488 V instead of exactly 0 V.

Measured Drain Current (I_D)

The measured drain current, I_D, is calculated using the measured component values.

1. Using the drain resistor (R_D)

- $V_+ = 15.027$ V
- $V_D = 2.098$ V
- $R_D = 12022.325\,\Omega$

$$I_D = \frac{V_+ - V_D}{R_D} = \frac{15.027 \text{ V} - 2.098 \text{ V}}{12022.325\,\Omega} \approx 1.075 \text{ mA}$$

2. Using the source resistor (R_S)

- $V_S = 0.7488$ V

- $V_{-} = -15.03$ V
- $R_S = 14791\,\Omega$

$$I_D = \frac{V_S - V_{-}}{R_S} = \frac{0.7488 \text{ V} - (-15.03 \text{ V})}{14791\,\Omega} \approx 1.067 \text{ mA}$$

The results from both methods are consistent. The measured drain current is approximately 1.07 **mA**, very close to the design specification of 1.0 mA.