ENGR 305 Lab 8: Hand Calculations

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1 Part 1: PNP in Active Mode

1.1 Given Parameters

- **Voltage Supplies:** $V_+ = 15\,\text{V}$, $V_- = -15\,\text{V}$
- **Design Goals:** $I_C = 1\,\text{mA}$, $V_B = 0\,\text{V}$, $V_C = -5\,\text{V}$
- **Transistor Model:** $\beta = 100$
- **Assumption:** Active region $V_{EB(\text{on})} = 0.7\,\text{V}$

1.2 Circuit Analysis

The circuit is a standard four-resistor voltage divider bias for a PNP transistor.

- R_E is connected from V_+ to the Emitter.
- R_C is connected from the Collector to V_-.
- R_1 is connected from V_+ to the Base.
- R_2 is connected from the Base to V_-.

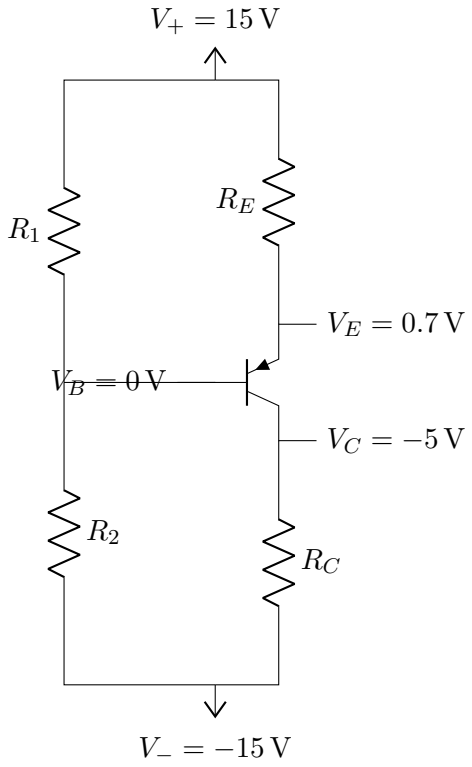

Figure 1: Part 1: PNP in Active Mode Circuit

1.3 Calculations

1. Calculate Base and Emitter Currents (I_B, I_E)
The base current is calculated from the collector current and β:

$$I_B = \frac{I_C}{\beta} = \frac{1\,\mathrm{mA}}{100} = 0.01\,\mathrm{mA} = 10\,\mu\mathrm{A}$$

The emitter current is the sum of the collector and base currents:

$$I_E = I_C + I_B = 1\,\mathrm{mA} + 0.01\,\mathrm{mA} = 1.01\,\mathrm{mA}$$

2. Calculate Emitter Voltage (V_E)
The emitter voltage is found relative to the base voltage, using the $V_{EB(\mathrm{on})}$ assumption:

$$V_E = V_B + V_{EB(\mathrm{on})} = 0\,\mathrm{V} + 0.7\,\mathrm{V} = 0.7\,\mathrm{V}$$

3. Calculate Emitter and Collector Resistors (R_E, R_C)
R_E is calculated using Ohm's law with the voltage drop across it ($V_+ - V_E$) and the current through it (I_E):

$$R_E = \frac{V_+ - V_E}{I_E} = \frac{15\,\mathrm{V} - 0.7\,\mathrm{V}}{1.01\,\mathrm{mA}} = \frac{14.3\,\mathrm{V}}{1.01\,\mathrm{mA}} \approx 14.16\,\mathrm{k\Omega}$$

R_C is calculated using the voltage drop across it ($V_C - V_-$) and the current through it (I_C):

$$R_C = \frac{V_C - V_-}{I_C} = \frac{-5\,\mathrm{V} - (-15\,\mathrm{V})}{1\,\mathrm{mA}} = \frac{10\,\mathrm{V}}{1\,\mathrm{mA}} = 10\,\mathrm{k\Omega}$$

4. Calculate Base Biasing Resistors (R_1, R_2)
This problem is not fully specified, as there is one KCL equation at the base with two unknown resistors. We must make a design choice for the stiffness of the voltage divider. A common rule of thumb is to set the divider current (I_{divider}) to be at least 10 times the base current.

- $I_B = 10\,\mu\text{A}$ (note: this current flows *out* of the PNP base).
- Let's set the current through R_2 as $I_{R2} = 10 \times I_B = 10 \times 10\,\mu\text{A} = 100\,\mu\text{A}$.

Now, we can find R_2:

$$R_2 = \frac{V_B - V_-}{I_{R2}} = \frac{0\,\text{V} - (-15\,\text{V})}{100\,\mu\text{A}} = \frac{15\,\text{V}}{0.1\,\text{mA}} = 150\,\text{k}\Omega$$

The current through R_1 is found by KCL at the base node ($I_{R1} = I_{R2} + I_B$):

$$I_{R1} = 100\,\mu\text{A} + 10\,\mu\text{A} = 110\,\mu\text{A}$$

Now, we can find R_1:

$$R_1 = \frac{V_+ - V_B}{I_{R1}} = \frac{15\,\text{V} - 0\,\text{V}}{110\,\mu\text{A}} = \frac{15\,\text{V}}{0.11\,\text{mA}} \approx 136.36\,\text{k}\Omega$$

2 Part 2: PNP in Saturation Mode

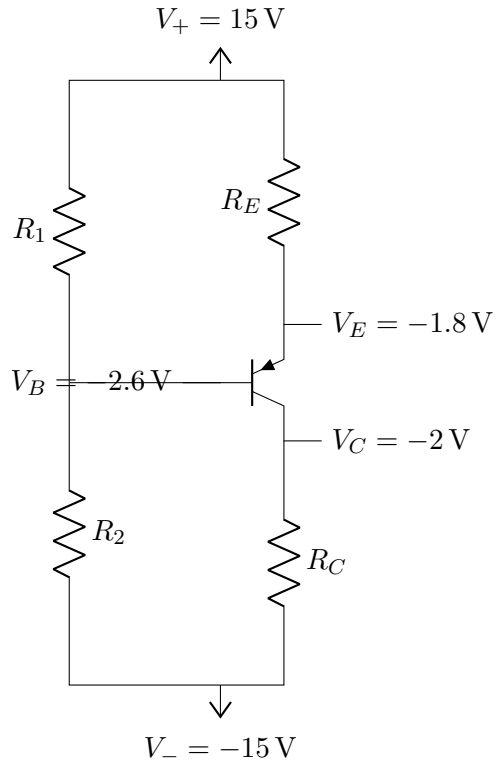

Figure 2: Part 2: PNP in Saturation Mode Circuit (Same topology as Part 1)

2.1 Given Parameters

- **Voltage Supplies:** $V_+ = 15\,\mathrm{V}$, $V_- = -15\,\mathrm{V}$
- **Design Goals:** $I_C = 1\,\mathrm{mA}$, $I_E = 1.2\,\mathrm{mA}$, $V_C = -2\,\mathrm{V}$, $V_{EC} = 0.2\,\mathrm{V}$
- **Assumption:** Saturation model $V_{EB(\mathrm{sat})} = 0.8\,\mathrm{V}$

2.2 Calculations

1. Calculate Emitter and Base Voltages (V_E, V_B)
The emitter voltage is found from the given collector voltage and V_{EC}:

$$V_E = V_C + V_{EC} = -2\,\mathrm{V} + 0.2\,\mathrm{V} = -1.8\,\mathrm{V}$$

The base voltage is found using the $V_{EB(\mathrm{sat})}$ assumption:

$$V_B = V_E - V_{EB(\mathrm{sat})} = -1.8\,\mathrm{V} - 0.8\,\mathrm{V} = -2.6\,\mathrm{V}$$

2. Calculate Emitter and Collector Resistors (R_E, R_C)
R_E is calculated using the voltage drop $(V_+ - V_E)$ and current I_E:

$$R_E = \frac{V_+ - V_E}{I_E} = \frac{15\,\mathrm{V} - (-1.8\,\mathrm{V})}{1.2\,\mathrm{mA}} = \frac{16.8\,\mathrm{V}}{1.2\,\mathrm{mA}} = 14\,\mathrm{k\Omega}$$

R_C is calculated using the voltage drop $(V_C - V_-)$ and current I_C:

$$R_C = \frac{V_C - V_-}{I_C} = \frac{-2\,\text{V} - (-15\,\text{V})}{1\,\text{mA}} = \frac{13\,\text{V}}{1\,\text{mA}} = 13\,\text{k}\Omega$$

3. Calculate β_{forced}
First, find the base current I_B:

$$I_B = I_E - I_C = 1.2\,\text{mA} - 1.0\,\text{mA} = 0.2\,\text{mA}$$

Now, calculate the forced β:

$$\beta_{\text{forced}} = \frac{I_C}{I_B} = \frac{1\,\text{mA}}{0.2\,\text{mA}} = 5$$

4. Calculate Base Biasing Resistors (R_1, R_2)
We must again choose a divider current. We will use the $10 \times I_B$ rule for the current through R_2.

- $I_B = 0.2\,\text{mA}$ (flowing out of the base).
- $I_{R2} = 10 \times I_B = 10 \times 0.2\,\text{mA} = 2.0\,\text{mA}$.

Now, find R_2:

$$R_2 = \frac{V_B - V_-}{I_{R2}} = \frac{-2.6\,\text{V} - (-15\,\text{V})}{2.0\,\text{mA}} = \frac{12.4\,\text{V}}{2.0\,\text{mA}} = 6.2\,\text{k}\Omega$$

Find I_{R1} using KCL at the base ($I_{R1} = I_{R2} + I_B$):

$$I_{R1} = 2.0\,\text{mA} + 0.2\,\text{mA} = 2.2\,\text{mA}$$

Now, find R_1:

$$R_1 = \frac{V_+ - V_B}{I_{R1}} = \frac{15\,\text{V} - (-2.6\,\text{V})}{2.2\,\text{mA}} = \frac{17.6\,\text{V}}{2.2\,\text{mA}} = 8\,\text{k}\Omega$$

3 Part 3: Diode-Connected PNP

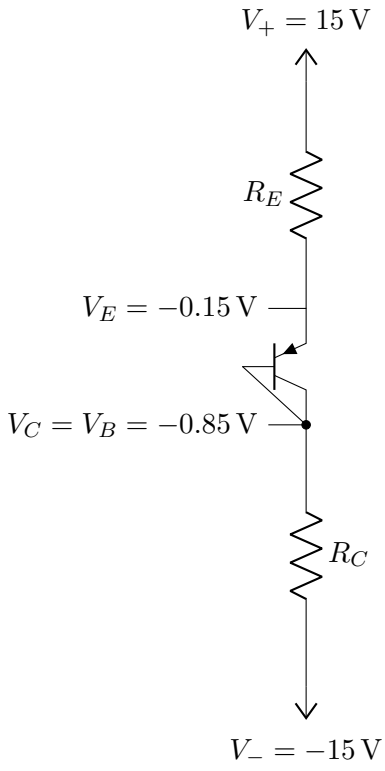

Figure 3: Part 3: Diode-Connected PNP Circuit

3.1 Given Parameters

- **Voltage Supplies:** $V_+ = 15\,\mathrm{V}$, $V_- = -15\,\mathrm{V}$
- **Design Goals:** $I_C = 1\,\mathrm{mA}$
- **Given Component:** $R_E = 15\,\mathrm{k\Omega}$
- **Transistor Model:** $\beta = 100$
- **Circuit:** Diode-connected ($V_B = V_C$)
- **Assumption:** Active region $V_{EB(\mathrm{on})} = 0.7\,\mathrm{V}$

3.2 Calculations

1. Operating Region
In a diode-connected BJT, the base and collector are shorted, so $V_{BC} = V_B - V_C = 0\,\mathrm{V}$. This places the transistor at the boundary between the active and saturation regions. It will operate in the **Active Region**, as it cannot enter saturation (V_{BC} cannot become positive for a PNP).

2. Calculate Currents (I_B, I_E)

$$I_B = \frac{I_C}{\beta} = \frac{1\,\text{mA}}{100} = 0.01\,\text{mA}$$

$$I_E = I_C + I_B = 1\,\text{mA} + 0.01\,\text{mA} = 1.01\,\text{mA}$$

3. Calculate Voltages (V_E, V_C)
The emitter voltage is determined by the V_+ supply, R_E, and I_E:

$$V_E = V_+ - (I_E \cdot R_E) = 15\,\text{V} - (1.01\,\text{mA} \cdot 15\,\text{k}\Omega) = 15\,\text{V} - 15.15\,\text{V} = -0.15\,\text{V}$$

The collector (and base) voltage is found relative to the emitter:

$$V_C = V_B = V_E - V_{EB(\text{on})} = -0.15\,\text{V} - 0.7\,\text{V} = -0.85\,\text{V}$$

4. Calculate Collector Resistor (R_C)
The circuit configuration is $V_+ \to R_E \to$ Emitter; Base $\to$ Collector $\to R_C \to V_-$. The current flowing out of the shared Base-Collector node and through R_C is the sum of I_B and I_C, which equals I_E.

$$I_{R_C} = I_B + I_C = I_E = 1.01\,\text{mA}$$

R_C is calculated using the voltage drop ($V_C - V_-$) and current I_E:

$$R_C = \frac{V_C - V_-}{I_E} = \frac{-0.85\,\text{V} - (-15\,\text{V})}{1.01\,\text{mA}} = \frac{14.15\,\text{V}}{1.01\,\text{mA}} \approx 14.01\,\text{k}\Omega$$