Lab 8

PNP at DC

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Lab 8: PNP at DC

1 Objective

The objective of this laboratory exercise is to study the DC biasing of a PNP bipolar transistor (2N3906). This will be accomplished by first completing a DC analysis for three distinct circuits: (1) a PNP transistor biased in the active region, (2) a PNP transistor biased in the saturation region, and (3) a diode-connected PNP transistor. The calculated results from this analysis will be compared against circuit simulations and device datasheets. Finally, the circuits will be implemented in an experimental setting to compare measured performance with both the theoretical and simulated results.

2 Theory

A Bipolar Junction Transistor (BJT) is a three-terminal semiconductor device (emitter, base, collector) that can be used for amplification or switching applications. This lab focuses on the PNP BJT, where the majority charge carriers are "holes." For a PNP transistor to operate, the base must be at a lower potential than the emitter ($V_{EB} > 0$), and the collector must be at a lower potential than the base ($V_{BC} < 0$).

The transistor's behavior is defined by its region of operation:

- **Active Region:** The emitter-base junction is forward-biased and the collector-base junction is reverse-biased. This region is used for signal amplification. The currents are related by the fundamental equations:

$$I_C = \beta I_B$$

$$I_E = I_C + I_B = (\beta + 1) I_B$$

  where β is the DC current gain (h_{FE}). A typical assumption for a forward-biased emitter-base junction is $V_{EB(\text{on})} \approx 0.7\,\text{V}$. The datasheet for the 2N3906 specifies h_{FE} ranges depending on the collector current; for example, at $I_C = 1.0\,\text{mA}$, h_{FE} is specified as being at least 80. Graphs suggest typical values around 150-160 at this current.

- **Saturation Region:** Both the emitter-base and collector-base junctions are forward-biased. The transistor acts like a closed switch. The collector current is no longer controlled by β and is instead limited by the external circuit. The collector-emitter voltage (V_{EC}) is small, and the relationship $I_C < \beta I_B$ holds. This is quantified by the β_{forced}:

$$\beta_{\text{forced}} = \frac{I_C}{I_B} < \beta$$

The datasheet specifies maximum saturation voltages, such as $V_{CE(sat)} \leq 0.25\,\text{V}$ at $I_C = 10\,\text{mA}$ (note $V_{EC(sat)}$ for PNP is positive) and $V_{BE(sat)}$ between $0.65\,\text{V}$ to $0.85\,\text{V}$ at $I_C = 10\,\text{mA}$ ($V_{EB(sat)}$ for PNP is positive).

- **Cutoff Region:** Both junctions are reverse-biased. The transistor acts like an open switch, and ideally, $I_C = I_E = I_B = 0$.

A diode-connected BJT, where the base and collector are shorted ($V_{BC} = 0$), operates at the boundary of the active and saturation regions.

3 Experimental method and reasoning

Three circuit configurations were analyzed, simulated, and built. All circuits used a 2N3906 PNP transistor and dual voltage supplies of $V_+ = 15\,\text{V}$ and $V_- = -15\,\text{V}$. For each part, hand calculations were performed first to determine the required resistor values (R_E, R_C, R_1, R_2) to meet the specified design goals.

Next, the circuits were simulated using a "dc op pnt" analysis to find the theoretical node voltages and branch currents, using the 2N3906 model. Finally, the circuits were prototyped on a breadboard. A digital multimeter was used to measure all resistor values and the DC node voltages (V_E, V_C, V_B). These measurements were then used to calculate the experimental currents (I_E, I_C, I_B) as part of the post-measurement exercise.

3.1 Part 1: PNP in Active Mode

Design Goals: $I_C = 1\,\text{mA}$, $V_B = 0\,\text{V}$, $V_C = -5\,\text{V}$. **Assumptions:** $\beta = 100$, $V_{EB(\text{on})} = 0.7\,\text{V}$.

Calculations were performed to find I_B, I_E, V_E, R_E, R_C, R_1, and R_2.

3.2 Part 2: PNP in Saturation Mode

Design Goals: $I_C = 1\,\text{mA}$, $I_E = 1.2\,\text{mA}$, $V_C = -2\,\text{V}$, $V_{EC} = 0.2\,\text{V}$. **Assumptions:** Saturation model (e.g., $V_{EB(\text{sat})} = 0.8\,\text{V}$).

Calculations were performed to find V_E, V_B, R_E, R_C, β_{forced}, R_1, and R_2.

3.3 Part 3: Diode-Connected PNP

Design Goals: $I_C = 1\,\text{mA}$. **Given:** $R_E = 15\,\text{k}\Omega$. **Assumptions:** $\beta = 100$, $V_{EB(\text{on})} = 0.7\,\text{V}$.

Calculations were performed to determine the operating region, V_C, and R_C.

4 Results and Conclusions (Discussion)

4.1 Part 1: Active Mode Results

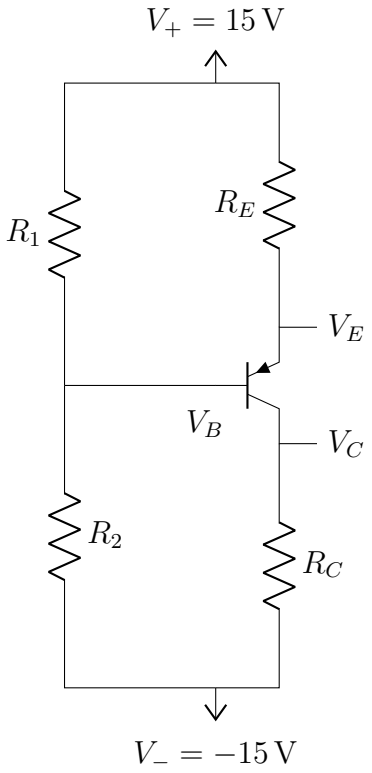

Figure 1: Part 1: PNP in Active Mode Circuit

4.1.1 Hand Calculations

Given Parameters

- **Voltage Supplies:** $V_+ = 15\,\text{V}$, $V_- = -15\,\text{V}$

- **Design Goals:** $I_C = 1\,\text{mA}$, $V_B = 0\,\text{V}$, $V_C = -5\,\text{V}$
- **Transistor Model:** $\beta = 100$
- **Assumption:** Active region $V_{EB(\text{on})} = 0.7\,\text{V}$

Calculations Calculated currents:

$$I_B = \frac{I_C}{\beta} = \frac{1\,\text{mA}}{100} = 10\,\mu\text{A}$$

$$I_E = I_C + I_B = 1\,\text{mA} + 0.01\,\text{mA} = 1.01\,\text{mA}$$

Calculated voltages and resistors:

$$V_E = V_B + V_{EB(\text{on})} = 0\,\text{V} + 0.7\,\text{V} = 0.7\,\text{V}$$

$$R_E = \frac{V_+ - V_E}{I_E} = \frac{15\,\text{V} - 0.7\,\text{V}}{1.01\,\text{mA}} \approx 14.16\,\text{k}\Omega$$

$$R_C = \frac{V_C - V_-}{I_C} = \frac{-5\,\text{V} - (-15\,\text{V})}{1\,\text{mA}} = 10\,\text{k}\Omega$$

$$I_{R2} = 10 \times I_B = 100\,\mu\text{A}$$

$$R_2 = \frac{V_B - V_-}{I_{R2}} = \frac{0\,\text{V} - (-15\,\text{V})}{100\,\mu\text{A}} = 150\,\text{k}\Omega$$

$$I_{R1} = I_{R2} + I_B = 100\,\mu\text{A} + 10\,\mu\text{A} = 110\,\mu\text{A}$$

$$R_1 = \frac{V_+ - V_B}{I_{R1}} = \frac{15\,\text{V} - 0\,\text{V}}{110\,\mu\text{A}} \approx 136.36\,\text{k}\Omega$$

4.1.2 Simulation Results

The circuit was simulated in LTspice using the calculated resistor values and a 2N3906 transistor.

- $V_E = 1.68\,\text{V}$
- $V_B = 1.03\,\text{V}$
- $V_C = -5.64\,\text{V}$
- $I_C = 0.936\,\text{mA}$
- $I_B = 4.40\,\mu\text{A}$
- $I_E = 0.941\,\text{mA}$

4.1.3 Measurement Data

The circuit was constructed and the following DC values were measured with a digital multimeter.

- $V_+ = 15.01\,\text{V}$, $V_- = -15.02\,\text{V}$
- $R_1 = 136.265\,\text{k}\Omega$, $R_2 = 151.03\,\text{k}\Omega$, $R_C = 10.02\,\text{k}\Omega$, $R_E = 14.7\,\text{k}\Omega$
- $V_E = 1.755\,\text{V}$, $V_B = 1.09\,\text{V}$, $V_C = -6.027\,\text{V}$

Post-Measurement Calculations Based on the measured values above:

$$V_{EB} = V_E - V_B = 1.755\,\text{V} - 1.09\,\text{V} = 0.665\,\text{V}$$

$$I_E = \frac{V_+ - V_E}{R_E} = \frac{15.01\,\text{V} - 1.755\,\text{V}}{14.7\,\text{k}\Omega} = 0.902\,\text{mA}$$

$$I_C = \frac{V_C - V_-}{R_C} = \frac{-6.027\,\text{V} - (-15.02\,\text{V})}{10.02\,\text{k}\Omega} = 0.898\,\text{mA}$$

$$I_B = I_E - I_C = 0.902\,\text{mA} - 0.898\,\text{mA} = 0.004\,\text{mA (or } 4\,\mu\text{A)}$$

$$\beta = \frac{I_C}{I_B} = \frac{0.898\,\text{mA}}{0.004\,\text{mA}} \approx 225$$

4.1.4 Comparison of Results (Part 1)

Table 1: Part 1: Comparison of Calculated, Simulated, and Measured Values

Parameter	Hand Calc (Goal)	Simulation	Measured
V_B	0.000 V	1.030 V	1.090 V
V_E	0.700 V	1.680 V	1.755 V
V_C	−5.000 V	−5.640 V	−6.027 V
V_{EB}	0.700 V (Assumed)	0.650 V	0.665 V
I_C	1.000 mA	0.936×10^{-3} A	0.898×10^{-3} A
I_B	10.000 µA	4.400×10^{-6} A	4.000×10^{-6} A
I_E	1.010 mA	0.941×10^{-3} A	0.902×10^{-3} A
β (h_{FE})	100 (Assumed)	≈ 213	≈ 225

4.2 Part 2: Saturation Mode Results

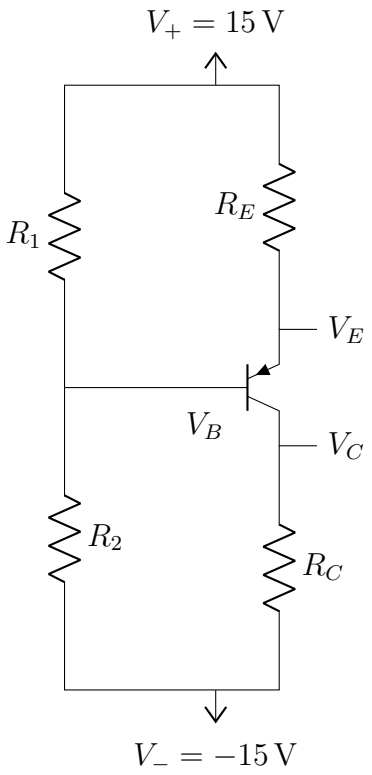

Figure 2: Part 2: PNP in Saturation Mode Circuit (Same topology as Part 1)

4.2.1 Hand Calculations

Given Parameters

- **Voltage Supplies:** $V_+ = 15\,\text{V}$, $V_- = -15\,\text{V}$
- **Design Goals:** $I_C = 1\,\text{mA}$, $I_E = 1.2\,\text{mA}$, $V_C = -2\,\text{V}$, $V_{EC} = 0.2\,\text{V}$
- **Assumption:** Saturation model $V_{EB(\text{sat})} = 0.8\,\text{V}$

Calculations

$$V_E = V_C + V_{EC} = -2\,\text{V} + 0.2\,\text{V} = -1.8\,\text{V}$$

$$V_B = V_E - V_{EB(\text{sat})} = -1.8\,\text{V} - 0.8\,\text{V} = -2.6\,\text{V}$$

$$R_E = \frac{V_+ - V_E}{I_E} = \frac{15\,\text{V} - (-1.8\,\text{V})}{1.2\,\text{mA}} = 14\,\text{k}\Omega$$

$$R_C = \frac{V_C - V_-}{I_C} = \frac{-2\,\mathrm{V} - (-15\,\mathrm{V})}{1\,\mathrm{mA}} = 13\,\mathrm{k\Omega}$$
$$I_B = I_E - I_C = 1.2\,\mathrm{mA} - 1.0\,\mathrm{mA} = 0.2\,\mathrm{mA}$$
$$\beta_{\text{forced}} = \frac{I_C}{I_B} = \frac{1\,\mathrm{mA}}{0.2\,\mathrm{mA}} = 5$$
$$I_{R2} = 10 \times I_B = 2.0\,\mathrm{mA}$$
$$R_2 = \frac{V_B - V_-}{I_{R2}} = \frac{-2.6\,\mathrm{V} - (-15\,\mathrm{V})}{2.0\,\mathrm{mA}} = 6.2\,\mathrm{k\Omega}$$
$$I_{R1} = I_{R2} + I_B = 2.0\,\mathrm{mA} + 0.2\,\mathrm{mA} = 2.2\,\mathrm{mA}$$
$$R_1 = \frac{V_+ - V_B}{I_{R1}} = \frac{15\,\mathrm{V} - (-2.6\,\mathrm{V})}{2.2\,\mathrm{mA}} = 8\,\mathrm{k\Omega}$$

4.2.2 Simulation Results

The circuit was simulated in LTspice using the calculated resistor values.

- $V_E = -0.996\,\mathrm{V}$
- $V_B = -1.66\,\mathrm{V}$
- $V_C = -1.04\,\mathrm{V}$
- $I_C = 1.074\,\mathrm{mA}$
- $I_B = 68.79\,\mu\mathrm{A}$
- $I_E = 1.143\,\mathrm{mA}$

4.2.3 Measurement Data

The circuit was constructed and the following DC values were measured.

- $V_+ = 15.01\,\mathrm{V}$, $V_- = -15.02\,\mathrm{V}$
- $R_1 = 8.6356\,\mathrm{k\Omega}$, $R_2 = 6.652\,\mathrm{k\Omega}$, $R_C = 12.945\,\mathrm{k\Omega}$, $R_E = 14.7\,\mathrm{k\Omega}$
- $V_E = -1.255\,\mathrm{V}$, $V_B = -1.91\,\mathrm{V}$, $V_C = -1.842\,\mathrm{V}$

Post-Measurement Calculations Based on the measured values above:

$$V_{EB} = V_E - V_B = -1.255\,\text{V} - (-1.91\,\text{V}) = 0.655\,\text{V}$$

$$V_{EC} = V_E - V_C = -1.255\,\text{V} - (-1.842\,\text{V}) = 0.587\,\text{V}$$

$$I_E = \frac{V_+ - V_E}{R_E} = \frac{15.01\,\text{V} - (-1.255\,\text{V})}{14.7\,\text{k}\Omega} = 1.106\,\text{mA}$$

$$I_C = \frac{V_C - V_-}{R_C} = \frac{-1.842\,\text{V} - (-15.02\,\text{V})}{12.945\,\text{k}\Omega} = 1.018\,\text{mA}$$

$$I_B = I_E - I_C = 1.106\,\text{mA} - 1.018\,\text{mA} = 0.088\,\text{mA (or } 88\,\mu\text{A)}$$

$$\beta_{\text{forced}} = \frac{I_C}{I_B} = \frac{1.018\,\text{mA}}{0.088\,\text{mA}} \approx 11.57$$

4.2.4 Comparison of Results (Part 2)

Table 2: Part 2: Comparison of Calculated, Simulated, and Measured Values

Parameter	**Hand Calc (Goal)**	**Simulation**	**Measured**
V_B	$-2.600\,\text{V}$	$-1.660\,\text{V}$	$-1.910\,\text{V}$
V_E	$-1.800\,\text{V}$	$-0.996\,\text{V}$	$-1.255\,\text{V}$
V_C	$-2.000\,\text{V}$	$-1.040\,\text{V}$	$-1.842\,\text{V}$
$V_{EC(sat)}$	$0.200\,\text{V}$ (Goal)	0.045 V	0.587 V
$V_{EB(sat)}$	$0.800\,\text{V}$ (Assumed)	$0.660\,\text{V}$	$0.655\,\text{V}$
I_C	$1.000\,\text{mA}$	1.074×10^{-3} A	1.018×10^{-3} A
I_B	$0.200\,\text{mA}$	68.790×10^{-6} A	88.000×10^{-6} A
I_E	$1.200\,\text{mA}$	1.143×10^{-3} A	1.106×10^{-3} A
β_{forced}	5 (Goal)	≈ 15.6	≈ 11.57

4.3 Part 3: Diode-Connected Results

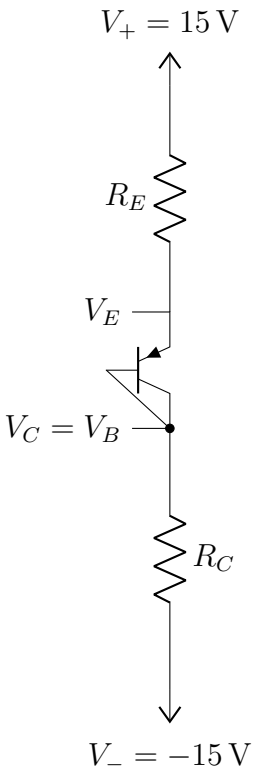

Figure 3: Part 3: Diode-Connected PNP Circuit

4.3.1 Hand Calculations

Given Parameters

- **Voltage Supplies:** $V_+ = 15\,\mathrm{V}$, $V_- = -15\,\mathrm{V}$
- **Design Goals:** $I_C = 1\,\mathrm{mA}$
- **Given Component:** $R_E = 15\,\mathrm{k\Omega}$
- **Transistor Model:** $\beta = 100$
- **Circuit:** Diode-connected ($V_B = V_C$)
- **Assumption:** Active region $V_{EB(\mathrm{on})} = 0.7\,\mathrm{V}$

Calculations

$$I_B = \frac{I_C}{\beta} = \frac{1\,\text{mA}}{100} = 0.01\,\text{mA}$$

$$I_E = I_C + I_B = 1\,\text{mA} + 0.01\,\text{mA} = 1.01\,\text{mA}$$

$$V_E = V_+ - (I_E \cdot R_E) = 15\,\text{V} - (1.01\,\text{mA} \cdot 15\,\text{k}\Omega) = -0.15\,\text{V}$$

$$V_C = V_B = V_E - V_{EB(\text{on})} = -0.15\,\text{V} - 0.7\,\text{V} = -0.85\,\text{V}$$

$$I_{R_C} = I_E = 1.01\,\text{mA}$$

$$R_C = \frac{V_C - V_-}{I_E} = \frac{-0.85\,\text{V} - (-15\,\text{V})}{1.01\,\text{mA}} \approx 14.01\,\text{k}\Omega$$

4.3.2 Simulation Results

The circuit was simulated in LTspice using the calculated resistor values.

- $V_E = -0.173\,\text{V}$
- $V_C = V_B = -0.828\,\text{V}$
- $I_C = 1.006\,\text{mA}$
- $I_B = 5.05\,\mu\text{A}$
- $I_E = 1.012\,\text{mA}$

4.3.3 Measurement Data

The circuit was constructed and the following DC values were measured.

- $V_+ = 15.01\,\text{V}$, $V_- = -15.02\,\text{V}$
- $R_C = 14.04\,\text{k}\Omega$, $R_E = 14.7\,\text{k}\Omega$
- $V_E = -0.0556\,\text{V}$, $V_C = -0.71\,\text{V}$, $V_B = -0.716\,\text{V}$

Post-Measurement Calculations Based on the measured values above:

$$V_{EB} = V_E - V_B = -0.0556\,\text{V} - (-0.716\,\text{V}) = 0.66\,\text{V}$$

$$I_E \text{ (from Emitter)} = \frac{V_+ - V_E}{R_E} = \frac{15.01\,\text{V} - (-0.0556\,\text{V})}{14.7\,\text{k}\Omega} = 1.025\,\text{mA}$$

$$I_E \text{ (from Collector)} = \frac{V_C - V_-}{R_C} = \frac{-0.71\,\text{V} - (-15.02\,\text{V})}{14.04\,\text{k}\Omega} = 1.019\,\text{mA}$$

We use the average of these two consistent current measurements: $I_E \approx 1.022\,\text{mA}$. Assuming the β measured in Part 1 is representative:

$$\beta \approx 225$$

$$I_C = I_E \left(\frac{\beta}{\beta + 1}\right) = 1.022\,\text{mA} \left(\frac{225}{226}\right) \approx 1.017\,\text{mA}$$

$$I_B = I_E - I_C = 1.022\,\text{mA} - 1.017\,\text{mA} = 0.005\,\text{mA (or } 5\,\mu\text{A)}$$

4.3.4 Comparison of Results (Part 3)

Table 3: Part 3: Comparison of Calculated, Simulated, and Measured Values

Parameter	**Hand Calc (Goal)**	**Simulation**	**Measured**
V_E	$-0.150\,\text{V}$	$-0.173\,\text{V}$	$-0.056\,\text{V}$
$V_C = V_B$	$-0.850\,\text{V}$	$-0.828\,\text{V}$	$\approx -0.713\,\text{V}$
V_{EB}	$0.700\,\text{V}$ (Assumed)	$0.655\,\text{V}$	$0.660\,\text{V}$
I_C	$1.000\,\text{mA}$	1.006×10^{-3} A	$\approx 1.017 \times 10^{-3}$ A
I_B	$10.000\,\mu\text{A}$	5.050×10^{-6} A	$\approx 5.000 \times 10^{-6}$ A
I_E	$1.010\,\text{mA}$	1.012×10^{-3} A	$\approx 1.022 \times 10^{-3}$ A
β (h_{FE})	100 (Assumed)	≈ 199	≈ 225

4.4 Discussion

This experiment successfully demonstrated the DC biasing of a PNP transistor (2N3906) in three different configurations: active mode, saturation mode, and diode-connected. The results highlight the differences between idealized hand calculations, more realistic simulations, actual circuit measurements, and datasheet specifications.

Comparison: Hand Calculations vs. Simulation vs. Datasheet Across all three parts, the simulation results deviated from the initial hand calculations. This was primarily due to the simplified assumptions used in the hand calculations, namely a fixed V_{EB} (0.7 V or 0.8 V) and a fixed β (100 or 5 for forced beta). The LTspice simulation employed a more sophisticated model for the 2N3906, resulting in different operating points. Datasheet values often provide ranges or typical values, which further adds context.

For instance, in Part 1, the hand calculation assumed $\beta = 100$. The simulation yielded $\beta \approx 213$. The datasheet minimum h_{FE} at $I_C = 1\,\text{mA}$ is 80, with typical graphical values suggesting 150-160. The higher actual β required less base current ($I_B = 4.4\,\mu\text{A}$ simulated vs. $10\,\mu\text{A}$ goal). This reduced loading on the base voltage divider caused V_B to rise (1.03 V simulated vs. 0 V goal), shifting other voltages. The assumed V_{EB} of 0.7 V was close to the simulated 0.65 V and the typical datasheet graph value around 0.7 V.

In Part 2 (Saturation), the hand calculation assumed $V_{EC(sat)} = 0.2\,\text{V}$. The simulation showed much deeper saturation ($V_{EC} = 0.045\,\text{V}$). The datasheet specifies $V_{CE(sat)} \leq 0.25\,\text{V}$ at a higher current of 10 mA, suggesting that smaller values are expected at 1 mA. The hand-calculated $V_{EB(sat)}$ of 0.8 V was higher than the simulated 0.66 V; the datasheet suggests $V_{BE(sat)}$ is typically around 0.7 V at 1 mA but gives a range of 0.65 V to 0.85 V only at 10 mA. Despite these voltage shifts, the simulated currents remained close to the design goals.

Comparison: Simulation vs. Measurement vs. Datasheet The measured results generally agreed well with the simulations. Component tolerances in resistors affected the measured operating points compared to simulations using ideal values. The measured V_{EB} was consistently around 0.66 V (0.665 V, 0.655 V, 0.66 V), aligning well with both simulation and typical datasheet values.

The measured active-mode β in Part 1 (≈ 225) was higher than both the simulation (≈ 213) and the typical datasheet value ($\approx$ 150-160), but well above the minimum specification of 80. This highlights the significant variability in β even for transistors of the same part number.

In Part 2, the measured $V_{EC(sat)}$ (0.587 V) was higher than both the simulation (0.045 V) and the datasheet maximum at 10 mA (0.25 V). While the calculated $\beta_{\text{forced}} \approx 11.6$ confirms saturation, the measured V_{EC} is unexpectedly high and warrants further investigation (po-

tential measurement error or component issue). The measured $V_{EB(sat)}$ (0.655 V) agreed well with simulation (0.66 V) and the lower end of the datasheet range for higher currents.

Part 3 showed excellent agreement for currents between simulation (1.006 mA) and measurement (≈ 1.017 mA). The measured voltages were also reasonably close.

Overall Performance The experiment successfully demonstrated BJT biasing principles. Active mode (Part 1) achieved $I_C = 0.898$ mA (vs. 1.0 mA goal). Saturation mode (Part 2) met current goals ($I_C = 1.018$ mA, $I_E = 1.106$ mA) and confirmed saturation ($\beta_{\text{forced}} \approx 11.6$). Diode-connected (Part 3) achieved $I_C \approx 1.017$ mA accurately. Post-measurement calculations using measured voltages/resistors were crucial. The results emphasize the discrepancies between simple assumptions, detailed simulations, datasheet ranges/typical values, and specific component measurements, particularly for β and saturation voltages.

4.5 Conclusion

This laboratory exercise successfully investigated the DC biasing of a 2N3906 PNP BJT in active, saturation, and diode-connected configurations. Hand calculations provided effective initial designs, while LTspice simulations offered more accurate predictions by using a detailed transistor model. Experimental measurements, combined with post-measurement calculations, validated the theoretical principles and generally aligned with simulations and datasheet typical values, highlighting the practical impact of component tolerances and transistor parameter variability. Key findings include:

- Target currents were closely achieved in all three configurations. Measured I_C values were 0.898 mA (Part 1), 1.018 mA (Part 2), and ≈ 1.017 mA (Part 3).
- Measured V_{EB} values were consistently around 0.66 V, aligning well with datasheet typical values and simulations, but differing slightly from the 0.7 V hand calculation assumption.
- The measured active-mode β (≈ 225) was significantly higher than the assumed 100 and the typical datasheet value, demonstrating expected device variance but falling within plausible limits (above the minimum 80).
- Saturation was confirmed in Part 2 ($\beta_{\text{forced}} \approx 11.6$), although the measured $V_{EC(sat)}$ (0.587 V) was higher than expected from simulation and datasheet values.

Overall, the experiment provided practical experience in BJT circuit analysis, simulation, and measurement, reinforcing the understanding of operating regions and the differences between idealized models, simulations, datasheet specifications, and real-world hardware performance.

5 Bibliography

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[2] ON Semiconductor. "2N3906 General Purpose Transistors PNP Silicon." Datasheet, 2N3906/D, Rev. 4, February 2010. Accessed October 24, 2025. http://onsemi.com.