ENGR 305

MOSFET Circuits at DC

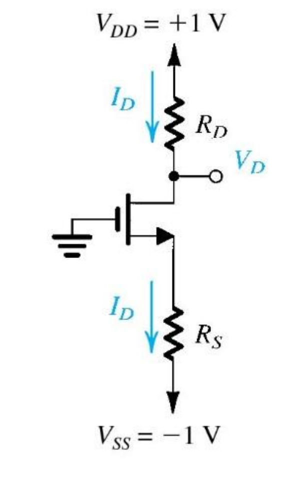
September 30, 2025

MOSFET Circuits at DC

- We now look at some examples involving only dc voltages and currents.
- To keep matters simple we will generally neglect channel-length modulation in the examples.
- Will work in terms of the overdrive voltage
  - $V_{OV} = V_{GS} - V_{tn}$ for NMOS
  - $|V_{OV}| = V_{SG} - |V_{tp}|$ for PMOS
- Since we are dealing with dc quantities, we will use uppercase symbols with uppercase subscripts for all currents and voltages.

Example 5.3

- Design the circuit shown; determine the values of R_D and R_S so that the transistor operates at $I_D = 0.2\ mA$ and $V_D = +0.2\ V$. The NMOS transistor has $V_t = 0.5\ V, \mu_n C_{ox} = 400\mu A/V^2$, $L = 0.5\mu m$, and $W = 15\mu m$. Neglect the channel length modulation effect (i.e., assume that $\lambda = 0$).



Example 5.3

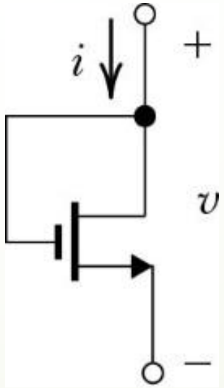
- In order for V_D to equal +0.2 V at the drain, we must select R_D as follows:
  - $R_D = \frac{V_{DD} - V_D}{I_D} = \frac{1-0.2}{0.2\ mA} = 4\ k\Omega$
- In order to determine the value for R_S, we need to know the voltage at the source. This can be found if we know V_{GS}.
- We note that since V_D is greater than V_G = 0, the NMOS transistor is operating in the saturation region.
- We use the saturation-region expression of i_D to find the required value of V_{OV}
  - $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{OV}^2$

Example 5.3

- Substituting $I_D = 0.2\ mA = 200\mu A$, $\mu_n C_{ox} = 400\mu A/V^2$ and ${}^W/_L = 15/0.5$,
  - $200 = \frac{1}{2} \times 400 \times \frac{15}{0.5} V_{OV}^2$
  - This gives $V_{OV} = 0.18\ V$
- Then, $V_{GS} = V_t + V_{OV} = 0.5 + 0.18 = 0.68\ V$
- We see that the gate is grounded and the source must be at -0.68 V.
- The required value of R_S can be determined from
  - $R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-0.68-(-1)}{0.2\ mA} = 1.6\ k\Omega$

Example 5.4

- The figure shows an NMOS transistor with its drain and gate terminals connected together. Find the $i - v$ relationship of the resulting two-terminal device in terms of the MOSFET parameters $k_n = k_n'(W/L)$ and V_{tn}. Neglect channel-length modulation. Note that this two-terminal device is known as a **diode-connected transistor.**

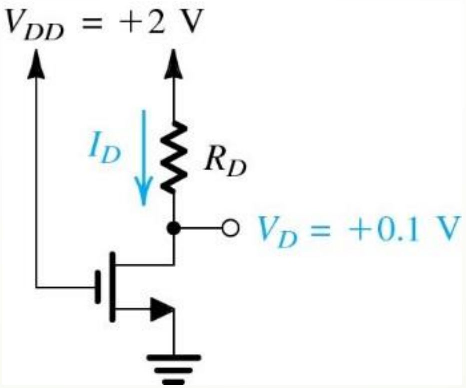


Example 5.4

- We first determine in which region the MOSFET is operating. Since $v_D = v_G$, operation is in the saturation mode.
  - $i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (v_{GS} - V_{tn})^2$
- Now $i = i_D \; and \; v = v_{GS}$ and
  - $i = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (v - V_{tn})^2$
- Replacing $k_n' \left(\frac{W}{L}\right)$ by k_n results in
  - $i = \frac{1}{2} k_n (v - V_{tn})^2$

Example 5.5

- Design the circuit to establish a dc drain voltage of 0.1 V. What is the effective resistance between drain and source at this operating point? Let $V_{tn} = 0.5V\ and\ k_n'(W/L) = 2mA/V^2$



Example 5.5

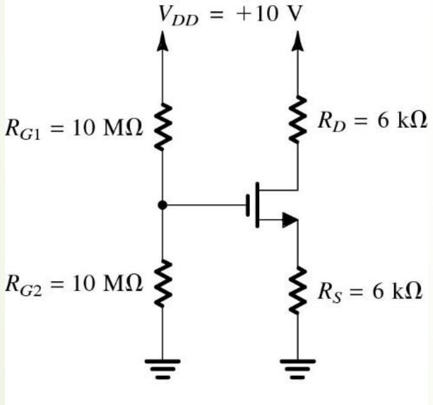
- Since the drain voltage is lower than the gate voltage by 1.9 V and $V_{tn} = 0.5\ V$, the MOSFET is operating in the triode region.
- The drain current is given by
  - $I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_{tn})V_{DS} - \frac{1}{2}V_{DS}^2\right]$
  - $I_D = 2 \times \left[(2 - 0.5) \times 0.1 - \frac{1}{2} \times 0.01\right] = 0.29\ mA$
- The required value for R_D can be found as
  - $R_D = \frac{V_{DD} - V_D}{I_D} = \frac{2 - 0.1}{0.29} = 6.55\ k\Omega$
- In a practical discrete-circuit design problem, one selects the closest standard value available for, say, 5% resistors – in this case, $6.8\ k\Omega$.

Example 5.5

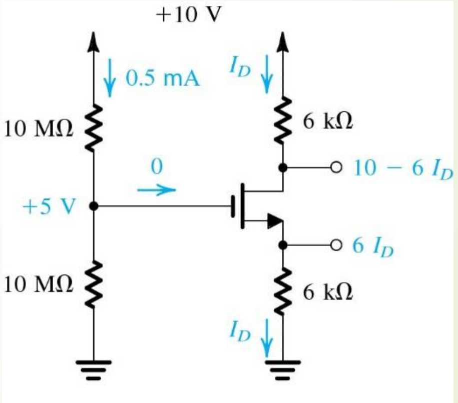
- Since the transistor is operating in the triode region with a small V_{DS}, the effective drain-to-source resistance can be determined as follows:
  - $r_{DS} = \frac{V_{DS}}{I_D} = \frac{0.1\ V}{0.29\ mA} = 345\ \Omega$
- Alternately, we can determine r_{DS} by using the formula
  - $r_{DS} = \frac{1}{k_n V_{OV}}$ to obtain
  - $r_{DS} = \frac{1}{2 \times (2 - 0.5)} = 0.333\ k\Omega = 333\ \Omega$
- This is close to the value found above.

Example 5.6

- Analyze the circuit shown to determine the voltages at all nodes and the currents through all branches. Let $V_{tn} = 1\,V$ and $k_n'(W/L) = 1mA/V^2$. Neglect the channel-length modulation effect ($\lambda = 0$).



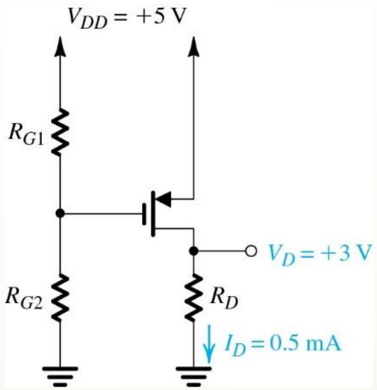
(a)



(b)

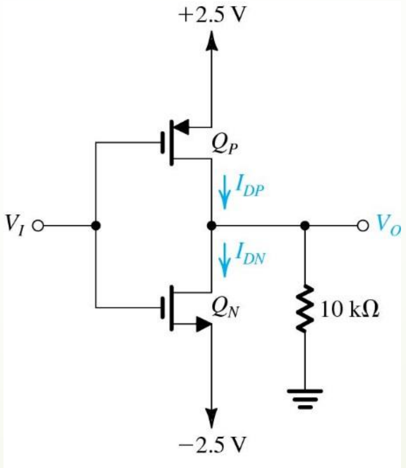
Example 5.7

- Design the circuit shown so that the transistor operates in saturation with $I_D = 0.5\ mA$ and $V_D = +3\ V$. Let the PMOS transistor have $V_{tp} = -1\ V$ and $k_p'(W/L) = 1\ mA/V^2$. Assume $\lambda = 0$. What is the largest value that R_D can have while maintaining saturation-region operation?



Example 5.8

- The NMOS and PMOS transistors in the circuit shown are matched, with $k_n'\left({}^{W_n}/_{L_n}\right) = k_p'\left({}^{W_p}/_{L_p}\right) = 1\ mA/V^2$ and $V_{tn} = -V_{tp} = 1\ V$. Assuming $\lambda = 0$ for both devices, find the drain currents $I_{DN}\ and\ I_{DP}$, as well as the voltage V_O, for $V_I = 0\ V, +2.5\ V, and\ -2.5\ V$.



(a)