ENGR 305 Lab 10: Hand Calculations

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1 Part 1: Design and DC Analysis

1.1 Given Parameters

- **Supplies:** $V_+ = 15\,\mathrm{V}$, $V_- = -15\,\mathrm{V}$
- **Design Goals:** $I_C = 1\,\mathrm{mA}$, Gain $A_v = -200$ V/V
- **Components:** $R_{sig} = 50\,\Omega$, $R_L = 10\,\mathrm{k}\Omega$, $R_B = 10\,\mathrm{k}\Omega$
- **Transistor Model:** 2N3904 NPN, assume $\beta = 100$, $V_{BE} = 0.7\,\mathrm{V}$, $V_T \approx 26\,\mathrm{mV}$

1.2 DC Operating Point Analysis

For the DC analysis, all coupling capacitors (C_{c1}, C_{c2}) and bypass capacitors (C_E) are treated as open circuits. The base is connected to ground through R_B.

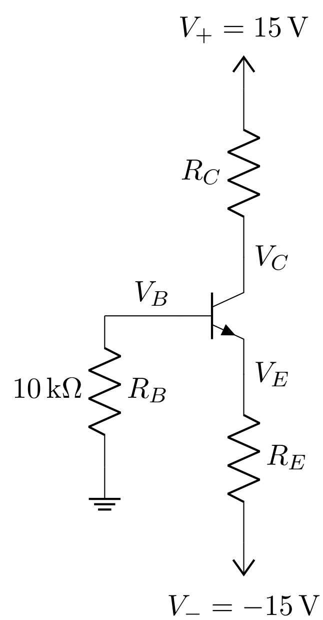

Figure 1: DC Equivalent Circuit

1. Calculate Base and Emitter Currents (I_B, I_E)
Using the target collector current $I_C = 1\,\text{mA}$ and $\beta = 100$:

$$I_B = \frac{I_C}{\beta} = \frac{1\,\text{mA}}{100} = 10\,\mu\text{A}$$

$$I_E = I_C + I_B = 1\,\text{mA} + 0.01\,\text{mA} = 1.01\,\text{mA}$$

2. Calculate Base and Emitter Voltages (V_B, V_E)
The base current flows from ground, through R_B, into the base.

$$V_B = 0 - I_B R_B = 0 - (10\,\mu\text{A})(10\,\text{k}\Omega) = -0.1\,\text{V}$$

Using the standard assumption of a $0.7\,\text{V}$ drop across the base-emitter junction:

$$V_E = V_B - V_{BE} = -0.1\,\text{V} - 0.7\,\text{V} = -0.8\,\text{V}$$

3. Design Emitter Resistor (R_E)
R_E sets the bias current. It is calculated from the voltage drop across it ($V_E - V_-$) and I_E.

$$R_E = \frac{V_E - V_-}{I_E} = \frac{-0.8\,\text{V} - (-15\,\text{V})}{1.01\,\text{mA}} = \frac{14.2\,\text{V}}{1.01\,\text{mA}} \approx 14.06\,\text{k}\Omega$$

Practical Note: $14.06\,\text{k}\Omega$ is not a standard E12/E24 value. It can be approximated using a decade box or a series combination (e.g., $10\,\text{k}\Omega + 3.9\,\text{k}\Omega + 160\,\Omega$).

2 Part 2: AC Small-Signal Analysis

2.1 Small-Signal Parameters

First, we calculate the transconductance (g_m) and input resistance (r_π) using the thermal voltage $V_T \approx 26\,\text{mV}$:

$$g_m = \frac{I_C}{V_T} = \frac{1\,\text{mA}}{26\,\text{mV}} \approx 38.46\,\text{mS}$$
$$r_\pi = \frac{\beta}{g_m} = \frac{100}{38.46\,\text{mS}} \approx 2.6\,\text{k}\Omega$$

2.2 Circuit Model

In the small-signal analysis, DC supplies become AC grounds, and large capacitors act as short circuits. The emitter resistor R_E is bypassed by C_E, connecting the emitter directly to ground.

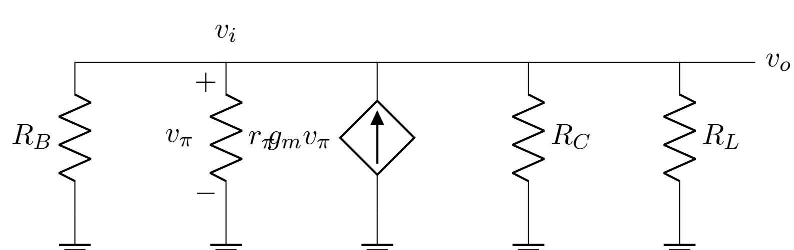

Figure 2: Small-Signal Model (Hybrid-π)

2.3 Gain Derivation and Design

1. Voltage Gain Expression (A_v)
The output voltage is generated by the dependent current source pulling current through the parallel combination of R_C and R_L:

$$v_o = -(g_m v_\pi)(R_C||R_L)$$

Since $v_\pi = v_i$ (emitter is grounded), the gain A_v is:

$$A_v = \frac{v_o}{v_i} = -g_m(R_C||R_L)$$

2. Design Collector Resistor (R_C)
We require a gain of $A_v = -200$.

$$|-200| = g_m(R_C||R_L) \implies 200 = (38.46\,\text{mS})\left(\frac{R_C R_L}{R_C + R_L}\right)$$

Solving for the equivalent resistance $R_{eq} = R_C||R_L$:

$$R_{eq} = \frac{200}{38.46\,\text{mS}} \approx 5.2\,\text{k}\Omega$$

Now solve for R_C knowing $R_L = 10\,\text{k}\Omega$:

$$\frac{1}{R_{eq}} = \frac{1}{R_C} + \frac{1}{R_L} \implies \frac{1}{R_C} = \frac{1}{5.2\,\text{k}\Omega} - \frac{1}{10\,\text{k}\Omega}$$

$$\frac{1}{R_C} \approx 1.923 \times 10^{-4} - 1 \times 10^{-4} = 0.923 \times 10^{-4}\ \text{S}$$

$$R_C \approx 10.83\,\text{k}\Omega$$

Practical Note: This can be implemented with a $10\,\text{k}\Omega$ and an $820\,\Omega$ resistor in series, or using a decade box.

2.4 Verification and Analysis

1. DC Collector Voltage (V_C)
We must verify the transistor remains in the active region ($V_C > V_B$).

$$V_C = V_+ - I_C R_C = 15\,\text{V} - (1\,\text{mA})(10.83\,\text{k}\Omega) = 15\,\text{V} - 10.83\,\text{V} = 4.17\,\text{V}$$

Since $V_C(4.17\,\text{V}) > V_B(-0.1\,\text{V})$, the transistor is in the Active Region.

2. Output Resistance (R_o)
The output resistance looking into the collector is approximately R_C (ignoring the transistor's early voltage V_A).

$$R_o \approx R_C = 10.83\,\text{k}\Omega$$

3. Input Attenuation (v_i/v_{sig})
The input impedance Z_{in} looking into the base is $R_B||r_\pi$:

$$Z_{in} = \frac{R_B r_\pi}{R_B + r_\pi} = \frac{10 \cdot 2.6}{10 + 2.6}\text{k}\Omega \approx 2.06\,\text{k}\Omega$$

The signal reaching the base v_i is a voltage divider with $R_{sig} = 50\,\Omega$:

$$\frac{v_i}{v_{sig}} = \frac{Z_{in}}{Z_{in} + R_{sig}} = \frac{2060\,\Omega}{2060\,\Omega + 50\,\Omega} \approx 0.976$$

This is close to unity, so the overall system gain is approximately equal to the stage gain A_v.

3 Summary of Values

The following table summarizes all assumed, given, and calculated values used in this lab analysis.

Table 1: Summary of Circuit Parameters

Parameter	**Symbol**	**Value**
Given & Assumed Constants		
Positive Supply Voltage	V_+	$15\,\text{V}$
Negative Supply Voltage	V_-	$-15\,\text{V}$
Target Collector Current	I_C	$1\,\text{mA}$
Transistor Beta	β	100
Base-Emitter Voltage	V_{BE}	$0.7\,\text{V}$
Thermal Voltage	V_T	$26\,\text{mV}$
Signal Source Resistance	R_{sig}	$50\,\Omega$
Load Resistance	R_L	$10\,\text{k}\Omega$
Base Bias Resistor	R_B	$10\,\text{k}\Omega$
Target Gain	A_v	-200 V/V
Calculated DC Values		
Base Current	I_B	$10\,\mu\text{A}$
Emitter Current	I_E	$1.01\,\text{mA}$
Base Voltage	V_B	$-0.1\,\text{V}$
Emitter Voltage	V_E	$-0.8\,\text{V}$
Emitter Resistor (Calculated)	R_E	$14.06\,\text{k}\Omega$
Collector Resistor (Calculated)	R_C	$10.83\,\text{k}\Omega$
Collector Voltage	V_C	$4.17\,\text{V}$
Calculated AC Values		
Transconductance	g_m	$38.46\,\text{mS}$
Input Resistance (Base)	r_π	$2.6\,\text{k}\Omega$
Input Impedance (Total)	Z_{in}	$2.06\,\text{k}\Omega$
Output Resistance	R_o	$10.83\,\text{k}\Omega$
Input Attenuation Ratio	v_i/v_{sig}	0.976