Key Constants & Values

- **Charge (q):** 1.602×10^{-19} C
- **Thermal Voltage (V_T):** at 300K, $V_T = kT/q \approx$ 25 mV
- **Intrinsic Silicon (n_i):** at 300K, $\approx 1.5 \times 10^{10}$ cm^{-3}
- **Permittivity of Si (ϵ_s):** 1.04×10^{-12} F/cm
- **CVD Model:** $V_D \approx 0.7$ V (Silicon)

1 Chapter 3: Semiconductors

Intrinsic Semiconductors

- Pure silicon. $n = p = n_i$
- **Mass Action Law:** $np = n_i^2$

Doped Semiconductors

- **n-type:** Doped with Donors (N_D, e.g., P).
  - Majority: electrons ($n_n \approx N_D$)
  - Minority: holes ($p_n = n_i^2/N_D$)
- **p-type:** Doped with Acceptors (N_A, e.g., B).
  - Majority: holes ($p_p \approx N_A$)
  - Minority: electrons ($n_p = n_i^2/N_A$)

Current Flow

- **Drift Current:** Due to E-field.

$$J_{drift} = q(n\mu_n + p\mu_p)E$$

- **Diffusion Current:** Due to ∇concentration.

$$J_p = -qD_p\frac{dp}{dx} \quad J_n = qD_n\frac{dn}{dx}$$

Einstein Relation

Connects mobility (μ) and diffusion (D).

$$D_n = V_T\mu_n \quad D_p = V_T\mu_p$$

Conductivity & Resistivity

- **Conductivity (σ):**

$$\sigma = q(n\mu_n + p\mu_p)$$

- **Resistivity (ρ):**

$$\rho = \frac{1}{\sigma} = \frac{1}{q(n\mu_n + p\mu_p)}$$

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2 Chapter 4: Diodes

pn Junction (Open Circuit)

- **Depletion Region:** Forms at junction, clear of carriers.
- **Built-in Voltage (V_0):**

$$V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

- **Depletion Width (W):** (V_R is reverse bias)

$$W = \sqrt{\frac{2\epsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_0 + V_R)}$$

- Drift current I_S balances diffusion current I_D.

Diode I-V Models

1. **Exponential (Shockley):**

$$i_D = I_S(e^{v_D/(nV_T)} - 1)$$

($I_S \approx 10^{-15}$ A, $n \approx 1{-}2$, $V_T \approx 25$ mV). For $v_D \gg V_T$, $i_D \approx I_S e^{v_D/(nV_T)}$.

2. **CVD (Constant Voltage Drop):**
   - ON: $v_D = 0.7$ V (0.7V battery)
   - OFF: $i_D = 0$ (open circuit)
3. **Ideal Diode:**
   - ON: $v_D = 0$ V (short circuit)
   - OFF: $i_D = 0$ (open circuit)

Small-Signal Model (at bias Q)

1. Find DC bias current I_D.
2. Replace diode with **small-signal resistance (r_d)**:

$$r_d = \frac{nV_T}{I_D}$$

Zener Diode (Breakdown)

- Operates in reverse breakdown for voltage regulation.
- Model: $V_Z = V_{Z0} + r_z I_Z$

Diode Capacitance

- **Junction (C_j):** Reverse bias.

$$C_j = \frac{C_{j0}}{(1 + V_R/V_0)^m}$$

- **Diffusion (C_d):** Forward bias.

$$C_d = \left(\frac{\tau_T}{V_T}\right) I_D$$

Rectifiers & Peak Detector

- **Rectifiers:** HW (1 diode), FW-CenterTap (2 diodes), FW-Bridge (4 diodes).
- **Peak Rectifier (with Filter C):** Capacitor C smooths output.
- **Ripple Voltage (V_r):**

$$V_r \approx \frac{V_p}{fCR_L} = \frac{I_L}{fC} \quad \text{(HW)}$$

$$V_r \approx \frac{V_p}{2fCR_L} = \frac{I_L}{2fC} \quad \text{(FW)}$$

- Diode Current (avg):

$$i_{D,avg} \approx I_L(1 + \pi\sqrt{2V_p/V_r})$$

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3 Chapter 5: MOSFETs

(Tables 5.1 & 5.2 provided on exam)

MOSFET Parameters

- **Threshold Voltage:** V_t ($V_{tn} > 0$, $V_{tp} < 0$)
- **Oxide Capacitance:** $C_{ox} = \epsilon_{ox}/t_{ox}$
- **Process Transconductance:** $k'_n = \mu_n C_{ox}$, $k'_p = \mu_p C_{ox}$
- **Transistor Transconductance:** $k_n = k'_n(W/L)$
- **Overdrive Voltage (V_{OV}):**
  - NMOS: $V_{OV} = V_{GS} - V_{tn}$
  - PMOS: $|V_{OV}| = V_{SG} - |V_{tp}|$

Regions (NMOS)

1. **Cutoff:**
   - **Cond:** $V_{GS} < V_{tn}$
   - **Current:** $i_D = 0$
2. **Triode (Linear):**
   - **Cond:** $V_{GS} \geq V_{tn}$ AND $V_{DS} < V_{OV}$
   - **Current:** $i_D = k_n\left[(V_{GS} - V_{tn})V_{DS} - \frac{1}{2}V_{DS}^2\right]$
   - Small V_{DS}: $r_{DS} = 1/(k_n V_{OV})$
3. **Saturation (Amplifier):**
   - **Cond:** $V_{GS} \geq V_{tn}$ AND $V_{DS} \geq V_{OV}$
   - **Current:** $i_D = \frac{1}{2}k_n(V_{GS} - V_{tn})^2 = \frac{1}{2}k_n V_{OV}^2$

Regions (PMOS)

Use V_{SG}, V_{SD}, $|V_{tp}|$, k_p.

1. **Cutoff:** $V_{SG} < |V_{tp}| \rightarrow i_D = 0$
2. **Triode:** $V_{SG} \geq |V_{tp}|$ AND $V_{SD} < |V_{OV}|$

$$i_D = k_p\left[(V_{SG} - |V_{tp}|)V_{SD} - \frac{1}{2}V_{SD}^2\right]$$

3. **Saturation:** $V_{SG} \geq |V_{tp}|$ AND $V_{SD} \geq |V_{OV}|$

$$i_D = \frac{1}{2}k_p(V_{SG} - |V_{tp}|)^2 = \frac{1}{2}k_p|V_{OV}|^2$$

Channel-Length Modulation (λ)

- Models $\uparrow i_D$ with $\uparrow v_{DS}$ in saturation.
- $i'_D = i_D(1 + \lambda v_{DS})$
- **Output Resistance (r_o):**

$$r_o = \frac{V_A}{I_D} \approx \frac{1}{\lambda I_D} \quad (V_A = 1/\lambda)$$

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4 Problem-Solving Steps (HW)

DC Analysis of Diode Circuits

1. Assume a state for each diode (ON/OFF).
2. Model: ON $\rightarrow$ 0.7V source (CVD), OFF $\rightarrow$ open circuit.
3. Solve the linear circuit for i_D and v_D.
4. **Check assumptions:**
   - Assumed ON $\rightarrow$ Check if $i_D > 0$.
   - Assumed OFF $\rightarrow$ Check if $v_D < 0.7$ V.
5. If wrong, change state and re-solve.

DC Analysis of MOSFET Circuits

1. **Assume** region (usually **Saturation**).
2. Write i_D equation for that region.
3. Write KVL/KCL for the circuit (e.g., for V_G, V_S, V_D).
4. Substitute relationships (e.g., $V_{OV} = V_{GS} - V_{tn}$).
5. Solve system for i_D and node voltages.
6. **Check assumption:**
   - Saturation: $V_{DS} \geq V_{OV}$ (NMOS)
   - Triode: $V_{DS} < V_{OV}$ (NMOS)
   - (Use $V_{SD}, |V_{OV}|$ for PMOS)
7. If wrong, re-assume region and re-solve.