ENGR 305 Lab 7 Report

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Introduction

The purpose of this lab was to design, build, and analyze two DC biasing circuits for a 2N3904 NPN Bipolar Junction Transistor (BJT). The first part involved designing a circuit to bias the transistor in the active region, a state essential for analog amplification. The second part involved designing a circuit to bias the transistor in the saturation region, which is commonly used in digital logic and switching applications.

The objective was to achieve specific operating points (e.g., V_C, I_C) by calculating the required resistor values for a four-resistor biasing network. The designs were then constructed and verified through hardware measurements, and the measured results were compared against the theoretical calculations.

Procedure

The lab was divided into two parts, each requiring the design of a circuit based on the general-purpose four-resistor biasing topology shown in Figure 1.

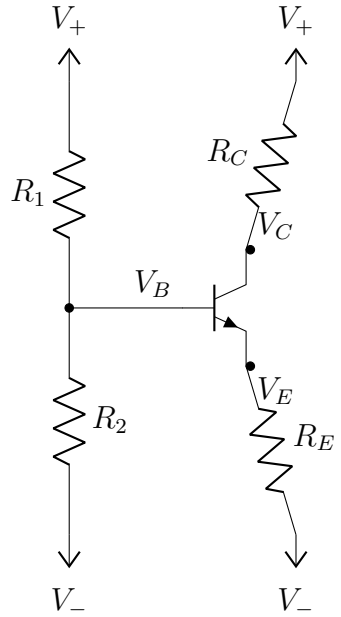

Figure 1: General four-resistor NPN biasing circuit.

Part 1: NPN in Active Mode

The first circuit was designed to bias the 2N3904 NPN transistor in the active region with the following target parameters:

- Collector Current (I_C): 1 mA
- Base Voltage (V_B): 0 V

- Collector Voltage (V_C): +5 V
- Supply Voltages: $V_+ = +15$ V, $V_- = -15$ V
- Assumed DC Current Gain (β): 100

Hand Calculations (Active Mode)

1. Base and Emitter Currents (I_B and I_E)

$$I_B = \frac{I_C}{\beta} = \frac{1 \text{ mA}}{100} = 0.01 \text{ mA} = \mathbf{10\ \mu A}$$

$$I_E = I_C + I_B = 1 \text{ mA} + 0.01 \text{ mA} = \mathbf{1.01\ mA}$$

2. Emitter Voltage (V_E) Assuming the standard V_{BE} drop for the active region:

$$V_{BE} = V_B - V_E \approx 0.7 \text{ V}$$

$$V_E = V_B - 0.7 \text{ V} = 0 \text{ V} - 0.7 \text{ V} = \mathbf{-0.7\ V}$$

3. Resistor Values (R_E and R_C)

$$R_E = \frac{V_E - V_-}{I_E} = \frac{-0.7 \text{ V} - (-15 \text{ V})}{1.01 \text{ mA}} = \frac{14.3 \text{ V}}{1.01 \text{ mA}} \approx \mathbf{14.16\ k\Omega}$$

$$R_C = \frac{V_+ - V_C}{I_C} = \frac{15 \text{ V} - 5 \text{ V}}{1 \text{ mA}} = \frac{10 \text{ V}}{1 \text{ mA}} = \mathbf{10\ k\Omega}$$

4. Voltage Divider Resistors (R_1 and R_2) To set $V_B = 0$ V with symmetric supplies, R_1 must equal R_2.

$$V_B = \frac{R_2 V_+ + R_1 V_-}{R_1 + R_2} \implies 0 = \frac{15R_2 - 15R_1}{R_1 + R_2} \implies \mathbf{R_1 = R_2}$$

To ensure a "stiff" divider, the divider current was set to $10 \times I_B = 0.1$ mA.

$$R_1 + R_2 = \frac{V_+ - V_-}{I_{divider}} = \frac{30 \text{ V}}{0.1 \text{ mA}} = 300 \text{ k}\Omega$$

$$R_1 = R_2 = \mathbf{150\ k\Omega}$$

Part 2: NPN in Saturation Mode

The second circuit was designed to bias the transistor in the saturation region with the following parameters:

- Collector Current (I_C): 1 mA
- Emitter Current (I_E): 1.2 mA
- Collector Voltage (V_C): +2 V
- Assumed Collector-Emitter Saturation Voltage ($V_{CE(sat)}$): 0.2 V

Hand Calculations (Saturation Mode)

1. Emitter and Base Voltages (V_E and V_B)

$$V_E = V_C - V_{CE} = 2\text{ V} - 0.2\text{ V} = \mathbf{1.8\text{ V}}$$

Assuming $V_{BE(sat)} \approx 0.8$ V:

$$V_B = V_E + 0.8\text{ V} = 1.8\text{ V} + 0.8\text{ V} = \mathbf{2.6\text{ V}}$$

2. Resistor Values (R_C and R_E)

$$R_C = \frac{V_+ - V_C}{I_C} = \frac{15\text{ V} - 2\text{ V}}{1\text{ mA}} = \frac{13\text{ V}}{1\text{ mA}} = \mathbf{13\ k\Omega}$$

$$R_E = \frac{V_E - V_-}{I_E} = \frac{1.8\text{ V} - (-15\text{ V})}{1.2\text{ mA}} = \frac{16.8\text{ V}}{1.2\text{ mA}} = \mathbf{14\ k\Omega}$$

3. Forced Beta (β_{forced}) The required base current is $I_B = I_E - I_C = 1.2\text{ mA} - 1\text{ mA} = \mathbf{0.2\text{ mA}}$.

$$\beta_{forced} = \frac{I_C}{I_B} = \frac{1\text{ mA}}{0.2\text{ mA}} = \mathbf{5}$$

Since $5 \ll 100$, this design will drive the transistor into saturation.

4. Voltage Divider Resistors (R_1 and R_2) The divider must provide $V_B = 2.6$ V.

$$2.6 = \frac{15R_2 - 15R_1}{R_1 + R_2} \implies 17.6R_1 = 12.4R_2 \implies R_2 \approx 1.42R_1$$

Using the stiff divider rule ($I_{divider} \approx 10 \times I_B = 2$ mA):

$$R_1 + R_2 = \frac{30\text{ V}}{2\text{ mA}} = 15\text{ k}\Omega$$

Solving the system of equations gives:

$$R_1 + (1.42R_1) = 15\text{ k}\Omega \implies R_1 \approx \mathbf{6.2\ k\Omega}$$

$$R_2 = 15\text{ k}\Omega - 6.2\text{ k}\Omega = \mathbf{8.8\ k\Omega}$$

Results

The circuits for Part 1 and Part 2 were constructed on a breadboard using the nearest available standard resistor values. The actual resistances were measured with a DMM, and the DC voltages at the power supply rails and transistor terminals were recorded.

Table 1: Measured Data for Part 1 (Active Mode)

Parameter	**Measured Value**	**Unit**
V_+	15.02	V
V_-	-15.02	V
R_1	148.2	kΩ
R_2	148.6	kΩ
R_C	9.89	kΩ
R_E	14.01	kΩ
V_C	4.881	V
V_B	-0.0016	V
V_E	-0.7302	V

Table 2: Measured Data for Part 2 (Saturation Mode)

Parameter	**Measured Value**	**Unit**
V_+	15.02	V
V_-	-15.02	V
R_1	6.13	kΩ
R_2	8.75	kΩ
R_C	12.87	kΩ
R_E	13.88	kΩ
V_C	2.054	V
V_B	2.521	V
V_E	1.839	V

Conclusion

The measured data was used to analyze the performance of both circuit designs and verify their operating points. The results were found to be in strong agreement with the pre-lab calculations, validating the design methodology.

Part 1 Analysis (Active Mode)

A comparison of the target versus measured node voltages shows excellent agreement.

Table 3: Part 1: Calculated vs. Measured Voltages

Parameter	Calculated	Measured
V_C	5.0 V	4.881 V
V_B	0.0 V	−0.0016 V
V_E	−0.7 V	−0.7302 V

Based on the measured values of Vc and Ve and your measured resistor values, what are the measured values of Ie, Ic and Ib based on your lab measurements?

The currents were calculated directly from the measured data using Ohm's Law and Kirchhoff's Current Law.

$$I_C = \frac{V_+ - V_C}{R_C} = \frac{15.02\text{ V} - 4.881\text{ V}}{9.89\text{ k}\Omega} \approx \mathbf{1.025\text{ mA}}$$

$$I_E = \frac{V_E - V_-}{R_E} = \frac{-0.7302\text{ V} - (-15.02\text{ V})}{14.01\text{ k}\Omega} \approx \mathbf{1.020\text{ mA}}$$

$$I_B = I_E - I_C = 1.020\text{ mA} - 1.025\text{ mA} = \mathbf{-0.005\text{ mA}}\ (-5\mu\text{A})$$

This small negative value for I_B is physically unrealistic and is a result of minor measurement inaccuracies and component tolerances, which are amplified when subtracting two large, nearly-equal numbers. The true base current is a small positive value, as confirmed by the $\beta \approx 100$ datasheet value, which would imply $I_B = I_C/\beta \approx 1.025\text{ mA}/100 \approx 10.25\mu\text{A}$. Both I_C and I_E are extremely close to the 1.0 mA design target.

Part 2 Analysis (Saturation Mode)

The measured voltages for the saturation circuit also agreed closely with the design.

Table 4: Part 2: Calculated vs. Measured Voltages

Parameter	Calculated	Measured
V_C	2.0 V	2.054 V
V_B	2.6 V	2.521 V
V_E	1.8 V	1.839 V

Based on the measured voltages and resistor values, what are the measured values of Ie, Ic and Ib based on your lab measurements? What is β_f?

The currents were calculated directly from the measured data:

$$I_C = \frac{V_+ - V_C}{R_C} = \frac{15.02\text{ V} - 2.054\text{ V}}{12.87\text{ k}\Omega} \approx \mathbf{1.007\text{ mA}}$$

$$I_E = \frac{V_E - V_-}{R_E} = \frac{1.839\text{ V} - (-15.02\text{ V})}{13.88\text{ k}\Omega} \approx \mathbf{1.215\text{ mA}}$$

$$I_B = I_E - I_C = 1.215\text{ mA} - 1.007\text{ mA} = \mathbf{0.208\text{ mA}}$$

These values are all in excellent agreement with the design targets ($I_C = 1.0$, $I_E = 1.2$, $I_B = 0.2$). The forced beta (β_f) is:

$$\beta_f = \frac{I_C}{I_B} = \frac{1.007\text{ mA}}{0.208\text{ mA}} \approx \mathbf{4.84}$$

Since $\beta_f \approx 4.84$ is much less than the active-mode β of the transistor (typically 100-300), this confirms the device was operating deep in saturation, as designed.

Analysis of V_{BE} and V_{CE}

A full analysis of the junction voltages confirms the operating state of the transistor in both circuits.

Part 1 (Active Mode)

Measured Values:

$$V_{BE} = V_B - V_E = (-0.0016\text{ V}) - (-0.7302\text{ V}) = \mathbf{0.7286\text{ V}}$$

$$V_{CE} = V_C - V_E = (4.881\text{ V}) - (-0.7302\text{ V}) = \mathbf{5.6112\text{ V}}$$

Comparison: The measured V_{BE} of 0.7286 **V** is in excellent agreement with the 0.7 **V** pre-lab assumption. The measured V_{CE} of 5.6112 **V** is also very close to the calculated target of 5.7 **V**. The minor differences are due to standard component tolerances. These values confirm the base-emitter junction is forward-biased and the collector-base junction is reverse-biased ($V_{CB} = V_C - V_B = 4.88\text{ V} > 0$), which is the definition of the active region.

Part 2 (Saturation Mode)

Measured Values:

$$V_{BE} = V_B - V_E = (2.521\text{ V}) - (1.839\text{ V}) = \mathbf{0.682\text{ V}}$$

$$V_{CE} = V_C - V_E = (2.054\text{ V}) - (1.839\text{ V}) = \mathbf{0.215\text{ V}}$$

Comparison: The measured V_{CE} of 0.215 **V** is an excellent match for the pre-lab target of 0.2 **V**. The measured V_{BE} of 0.682 **V** differs from the 0.8 V assumption, but this is expected as 0.8 V is a conservative design rule. The key condition for saturation is that both junctions are forward-biased. This is confirmed, as $V_{BE} > 0$ and $V_{BC} = V_B - V_C = 2.521\text{ V} - 2.054\text{ V} = 0.467\text{ V} > 0$.

Final Summary

Overall, both circuits performed as expected. The measured voltages and calculated currents for the active mode circuit were very close to the design targets. Similarly, the saturation mode circuit was successfully verified, with a measured $V_{CE(sat)}$ of 0.215 V and a forced beta of 4.84. The minor discrepancies between calculated and measured values can be attributed to standard component tolerances and the difference between assumed device parameters (like V_{BE}) and their actual values. The objectives of the lab were successfully met.