Lab 9

NMOS Common-Source Amplifier

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Course: ENGR 305
Date: November 6, 2025

1 Objective

The objective of this laboratory exercise is to study the NMOS common-source (CS) amplifier. This will be accomplished by:

- Completing a DC and small-signal analysis to design an amplifier that meets a specific gain requirement.
- Simulating the designed circuit to compare its performance against the paper analysis.
- Implementing the circuit in an experimental setting, taking measurements, and comparing its performance with both theoretical and simulated results.
- Measuring the output resistance of the prototyped amplifier.

2 Theory

A Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a three-terminal device (Gate, Drain, Source) that can be used for amplification. The common-source (CS) configuration is a fundamental amplifier topology.

DC Analysis To analyze an amplifier, the first step is to determine the DC operating point (Q-point) by eliminating AC signal sources. For the NMOS amplifier, this involves finding the DC drain current (I_D) and drain-to-source voltage (V_{DS}). Assuming the transistor is in the saturation region (the region for amplification) and neglecting channel-length modulation, the drain current is:

$$I_D = \frac{1}{2}k_n(V_{GS} - V_t)^2 = \frac{1}{2}k_n V_{OV}^2$$

where k_n is the process transconductance parameter, V_{GS} is the DC gate-to-source voltage, V_t is the threshold voltage, and V_{OV} is the overdrive voltage. The DC drain voltage is then found using Ohm's law on the drain resistor R_D:

$$V_{DS} = V_{DD} - R_D I_D$$

To confirm the transistor is in saturation, the condition $V_{DS} > V_{OV}$ must be met.

AC Small-Signal Analysis Once the DC operating point is found, the small-signal parameters are calculated. The most important parameter is the transconductance, g_m:

$$g_m = \frac{2I_D}{V_{OV}}$$

Another parameter is the transistor output resistance r_o, caused by channel-length modulation (λ), given by $r_o = 1/(\lambda I_D)$.

Next, all DC sources are set to zero (voltage sources become short circuits, current sources become open circuits) and the transistor is replaced with its small-signal model. For the CS amplifier, the voltage gain A_v is the ratio of the AC output voltage ($v_o = v_{ds}$) to the AC input voltage ($v_i = v_{gs}$). When including the load resistor R_L and the transistor's output resistance r_o, the gain is:

$$A_v = \frac{v_o}{v_i} = -g_m(R_D \parallel r_o \parallel R_L)$$

The negative sign indicates that the output signal is 180° out of phase with the input signal.

The amplifier's input resistance R_{in} is the resistance seen by the signal source. For the CS amplifier, this is dominated by the gate resistor R_G (as the MOSFET gate itself has infinite resistance). The output resistance R_o is the Thevenin equivalent resistance seen looking into the amplifier's output terminal (with R_L removed). For this circuit, $R_o = R_D \parallel r_o$.

3 Experimental Method and Reasoning

A common-source amplifier was designed using an enhancement-type NMOS transistor (2N7000) and dual voltage supplies of $V_+ = 15\,\text{V}$ and $V_- = -15\,\text{V}$.

Part 1: Design and Simulation First, a DC and AC analysis was performed by hand to design the amplifier. The design goals were $I_D = 1\,\text{mA}$ and $A_v \leq -5\,\text{V/V}$, using given transistor parameters (k_n, V_{tn}, λ). This analysis determined the required values for the source resistor R_S and drain resistor R_D.

The circuit was then simulated in LTspice using the calculated resistor values and the provided 2N7000 SPICE model. A 10 $\text{mV}_{\text{pk-pk}}$, 1 kHz sinusoidal input signal (v_{sig}) was applied. The simulation was used to measure the DC operating point (V_{GS}, V_{DS}, I_D) and the AC voltage gain A_v, which were then compared to the hand calculations.

Part 2: Prototyping The circuit was assembled on a breadboard using standard resistor values close to the calculated design values.

Part 3: Measurements Several measurements were taken from the prototyped circuit.

- **DC Bias Point:** A digital multimeter was used to measure the DC voltages at the gate (V_G), source (V_S), and drain (V_D). All resistor values were also measured.

- **AC Voltage Gain:** A function generator applied a 10 $\mathrm{mV_{pk\text{-}pk}}$, 1 kHz sinusoid, and an oscilloscope was used to measure the AC output (v_o) and input (v_i) waveforms to determine the gain A_v.
- **Output Resistance:** The load resistor R_L was replaced with a $1\,\mathrm{M\Omega}$ resistor and the output amplitude was measured. R_L was then adjusted until the output amplitude was 50% of this "open-load" value. This value of R_L is equal to the output resistance R_o.

Finally, post-measurement calculations were performed to find the experimental I_D, A_v, and R_o, and all three sets of results (hand-calculated, simulated, and measured) were compared.

4 Results and Conclusions (Discussion)

4.1 Hand Calculations (Design)

4.1.1 DC Operating Point Analysis

Given Parameters

- **Voltage Supplies:** $V_+ = 15\,\mathrm{V}$, $V_- = -15\,\mathrm{V}$
- **Design Goals:** $I_D = 1\,\mathrm{mA}$, $A_v \leq -5\,\mathrm{V/V}$
- **Circuit Resistors:** $R_{sig} = 50\,\Omega$, $R_L = 10\,\mathrm{k\Omega}$, $R_G = 10\,\mathrm{k\Omega}$
- **Transistor Parameters (2N7000):** $\lambda = 0.0146\,\mathrm{V^{-1}}$, $k_n = 1.08\,\mathrm{mA\,V^{-2}}$, $V_{tn} = 1.45\,\mathrm{V}$

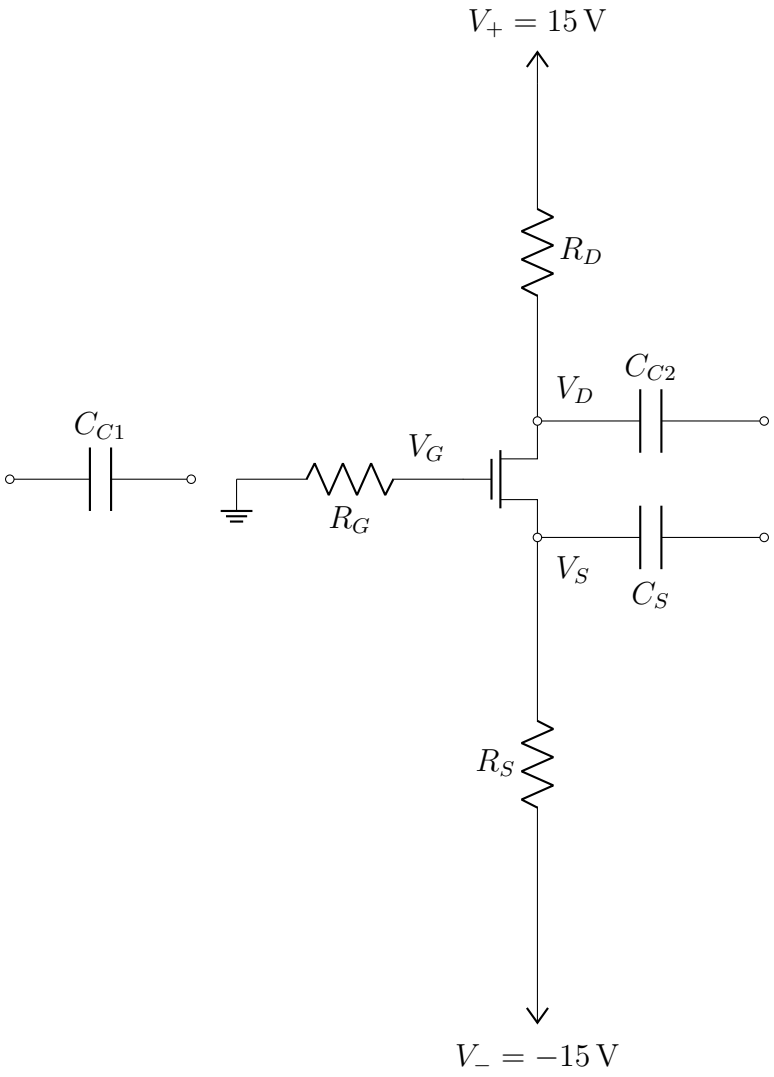

Figure 1: DC Model of the Common-Source Amplifier

1. DC Gate Current and Voltage (I_G, V_G) The DC gate current I_G for a MOSFET is effectively 0 A. Assuming R_G connects the gate to ground, the DC voltage drop is $I_G \cdot R_G = 0\,\mathrm{V}$. Therefore, the DC gate voltage is $V_G = 0\,\mathrm{V}$.

2. Overdrive Voltage (V_{OV}) Using the saturation current equation for the design goal $I_D = 1\,\mathrm{mA}$:

$$I_D = \frac{1}{2} k_n (V_{OV})^2$$

$$1\,\mathrm{mA} = \frac{1}{2}(1.08\,\mathrm{mA\,V^{-2}})(V_{OV})^2$$

$$V_{OV}^2 = \frac{2\,\mathrm{mA}}{1.08\,\mathrm{mA\,V^{-2}}} \approx 1.8519\,\mathrm{V}^2$$

$$V_{OV} = \sqrt{1.8519\,\mathrm{V}^2} \approx 1.361\,\mathrm{V}$$

3. Transconductance (g_m) and Gate-Source Voltage (V_{GS})

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2 \cdot 1\,\mathrm{mA}}{1.361\,\mathrm{V}} \approx 1.4695\,\mathrm{mA\,V^{-1}}\ (\text{or } 1.47\,\mathrm{mS})$$

$$V_{GS} = V_{OV} + V_{tn} = 1.361\,\mathrm{V} + 1.45\,\mathrm{V} = 2.811\,\mathrm{V}$$

4. Early Effect Resistance (r_o)

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{(0.0146\,\mathrm{V^{-1}})(1\,\mathrm{mA})} \approx 68.5\,\mathrm{k\Omega}$$

5. Source Resistor (R_S) First, find the DC source voltage V_S using $V_G = 0\,\mathrm{V}$:

$$V_{GS} = V_G - V_S \implies 2.811\,\mathrm{V} = 0\,\mathrm{V} - V_S \implies V_S = -2.811\,\mathrm{V}$$

R_S connects the source terminal (V_S) to the negative supply ($V_- = -15\,\mathrm{V}$). The DC current through it is $I_S = I_D = 1\,\mathrm{mA}$.

$$R_S = \frac{V_S - V_-}{I_D} = \frac{-2.811\,\mathrm{V} - (-15\,\mathrm{V})}{1\,\mathrm{mA}} = \frac{12.189\,\mathrm{V}}{1\,\mathrm{mA}} = 12.19\,\mathrm{k\Omega}$$

A standard $12.1\,\mathrm{k\Omega}$ resistor will be used.

4.1.2 AC Analysis

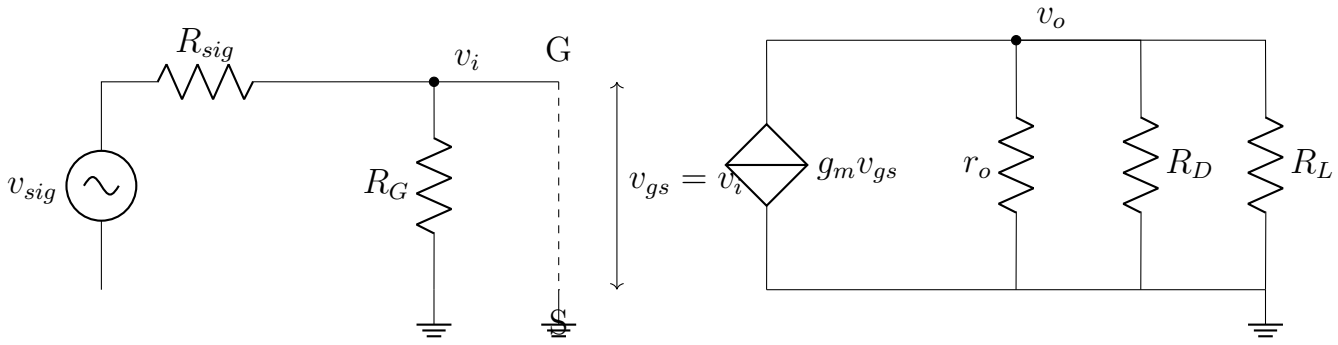

Figure 2: AC Small-Signal Model of the Common-Source Amplifier

1. Input Voltage Ratio (v_i/v_{sig}) The AC input resistance is $R_{in} = R_G = 10\,\mathrm{k\Omega}$.

$$\frac{v_i}{v_{sig}} = \frac{R_G}{R_{sig} + R_G} = \frac{10\,000\,\Omega}{50\,\Omega + 10\,000\,\Omega} \approx 0.995$$

(We will approximate $v_i \approx v_{sig}$).

2. Drain Resistor (R_D) for Gain $A_v = -5$ V/V The AC bypass capacitor C_S shorts R_S to ground. The gain is:

$$A_v = -g_m(r_o \parallel R_D \parallel R_L)$$

Solving for R_D to get $A_v = -5\,\mathrm{V/V}$:

$$-5\,\mathrm{V/V} = -(1.4695\,\mathrm{mS})(68.5\,\mathrm{k\Omega} \parallel R_D \parallel 10\,\mathrm{k\Omega})$$

Let $R'_L = r_o \parallel R_L = 68.5\,\mathrm{k\Omega} \parallel 10\,\mathrm{k\Omega} \approx 8.726\,\mathrm{k\Omega}$.

$$5 = (1.4695\,\mathrm{mS})(R_D \parallel 8.726\,\mathrm{k\Omega})$$

Let $R_{eq} = R_D \parallel 8.726\,\mathrm{k\Omega}$.

$$R_{eq} = \frac{5}{1.4695\,\mathrm{mS}} \approx 3.4025\,\mathrm{k\Omega}$$

Now, solve for R_D:

$$\frac{1}{R_D} = \frac{1}{R_{eq}} - \frac{1}{R'_L} = \frac{1}{3.4025\,\mathrm{k\Omega}} - \frac{1}{8.726\,\mathrm{k\Omega}} \approx 0.1793\,\mathrm{mS}$$

$$R_D = \frac{1}{0.1793\,\mathrm{mS}} \approx 5.577\,\mathrm{k\Omega}$$

A standard $5.6\,\mathrm{k\Omega}$ resistor will be used.

3. DC Drain Voltage (V_D) and Saturation Check Using $R_D = 5.577\,\mathrm{k\Omega}$:

$$V_D = V_+ - I_D R_D = 15\,\mathrm{V} - (1\,\mathrm{mA})(5.577\,\mathrm{k\Omega}) = 9.423\,\mathrm{V}$$

Check saturation condition: $V_{DS} \geq V_{OV}$.

$$V_{DS} = V_D - V_S = 9.423\,\mathrm{V} - (-2.811\,\mathrm{V}) = 12.234\,\mathrm{V}$$

Since $V_{DS}(12.234\,\mathrm{V}) \geq V_{OV}(1.361\,\mathrm{V})$, the transistor is in saturation.

4. Amplifier Output Resistance (R_o) The output resistance R_o is R_D in parallel with r_o.

$$R_o = R_D \parallel r_o = 5.577\,\mathrm{k\Omega} \parallel 68.5\,\mathrm{k\Omega} \approx 5.157\,\mathrm{k\Omega}$$

4.2 Simulation Results

Table 1: Simulation Results (Part 1)

Parameter	**Simulated Value**
V_G	[Enter Value]
V_D	[Enter Value]
V_S	[Enter Value]
V_{GS}	[Enter Value]
V_{DS}	[Enter Value]
I_D	[Enter Value]
$A_v = v_o/v_i$	[Enter Value]

4.3 Measurement Data

Table 2: Measured Component Values (Part 3)

Component	**Measured Value**
R_D (5.600 kΩ nominal)	[Enter Value]
R_S (12.100 kΩ nominal)	[Enter Value]
R_G (10.000 kΩ nominal)	[Enter Value]
R_L (10.000 kΩ nominal)	[Enter Value]

Table 3: Measured DC and AC Values (Part 3)

Parameter	**Measured Value**
V_G	[Enter Value]
V_D	[Enter Value]
V_S	[Enter Value]
v_i (pk-pk)	[Enter Value]
v_o (pk-pk)	[Enter Value]
R_o (from 50% amplitude)	[Enter Value]

Post-Measurement Calculations Using measured values from Tables 2 and 3:

$$V_{GS} = V_G - V_S = [...] = [...]$$

$$V_{DS} = V_D - V_S = [...] = [...]$$

$$I_D = \frac{V_D - V_+}{R_D} = [...] = [...] \text{ (Note: Use measured } V_+ \text{ and } R_D)$$

$$A_v = v_o/v_i = [...] = [...]$$

$$R_o = [\text{Value from Table 3}]$$

4.4 Comparison of Results

Table 4: Comparison of Calculated, Simulated, and Measured Values

Parameter	**Hand Calc (Goal)**	**Simulation**	**Measured**
V_{GS}	2.811 V	[Enter Sim Value]	[Enter Meas Value]
V_{DS}	12.234 V	[Enter Sim Value]	[Enter Meas Value]
I_D	1.000 mA	[Enter Sim Value]	[Enter Meas Value]
A_v	−5.000 V/V	[Enter Sim Value]	[Enter Meas Value]
R_o	5.157 kΩ	(N/A)	[Enter Meas Value]

4.5 Discussion

[This is where you discuss your results. Start by comparing the three sets of values in Table 4. - How close did your simulation (Part 1) get to the hand-calculated goals? - How close did your measured values (Part 3) get to the simulation and the hand calculations? - Discuss discrepancies. The lab manual suggests the biggest source of error will be the transistor's actual V_{tn} varying from the one used in calculations. How does this explain any differences in V_{GS} and I_D? - How did your measured A_v compare to the goal of -5 V/V? Explain any differences. - How did your measured R_o compare to your calculated R_o? Does it follow the hint that $R_o \leq R_D$? - Discuss the "Further exploration": What happened when you increased the input amplitude? At what point did distortion appear? Why does this happen (relate it to the small-signal condition $v_{gs} \ll 2V_{OV}$ and the saturation condition $V_{DS} \geq V_{OV}$)?]

4.6 Conclusion

[This is where you summarize the lab. Restate the objective (e.g., "This lab successfully designed, simulated, and tested an NMOS common-source amplifier..."). State your key findings clearly (e.g., "The designed amplifier achieved a gain of [Meas. A_v]..."). Summarize the agreement between theory, simulation, and measurement. Reiterate the main reasons for any discrepancies (e.g., "Discrepancies between theory and measurement were observed, likely due to variations in the 2N7000's V_{tn}..."). Conclude with a final statement about what you learned or demonstrated.]

5 Bibliography

[1] Fixel, Debora. "ENGR 305 - Lab 9: NMOS Common-Source Amplifier." Trinity College, Hartford, CT, October 2025.

[2] Microchip Technology Inc. "2N7000 N-Channel Enhancement-Mode Vertical DMOS FET." Datasheet, DS20005695A, 2021.