ENGR 305 Lab 9: NMOS Common-Source Amplifier Hand Calculations

Sean Balbale

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1 Part 1: Design and Simulation

1.1 Given Parameters and Design Goals

- **Voltage Supplies:** $V_+ = 15\,\mathrm{V}$, $V_- = -15\,\mathrm{V}$
- **Design Goals:** $I_D = 1\,\mathrm{mA}$, $A_v \leq -5\,\mathrm{V/V}$
- **Circuit Resistors:** $R_{sig} = 50\,\Omega$, $R_L = 10\,\mathrm{k\Omega}$, $R_G = 10\,\mathrm{k\Omega}$
- **Transistor Parameters (2N7000):** $\lambda = 0.0146\,\mathrm{V^{-1}}$, $k_n = 1.08\,\mathrm{mA\,V^{-2}}$, $V_{tn} = 1.45\,\mathrm{V}$

1.2 DC Operating Point Analysis

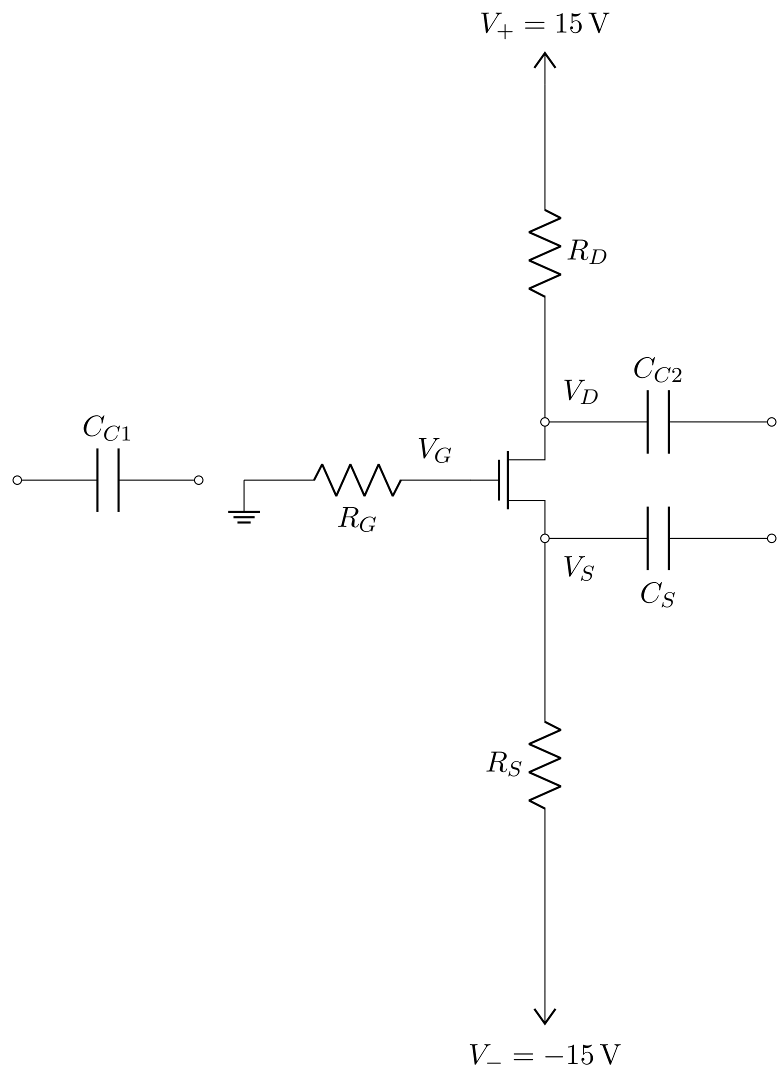

Figure 1: DC Model of the Common-Source Amplifier

1. DC Gate Current and Voltage (I_G, V_G)
The DC gate current I_G for a MOSFET is effectively $0\,\mathrm{A}$. The lab manual specifies a gate resistor R_G. Assuming R_G connects the gate to ground, the DC voltage drop across it is $I_G \cdot R_G = 0\,\mathrm{V}$. Therefore, the DC gate voltage is $V_G = 0\,\mathrm{V}$.

2. Overdrive Voltage (V_{OV})
Using the saturation current equation for the design goal $I_D = 1\,\mathrm{mA}$:

$$I_D = \frac{1}{2} k_n (V_{OV})^2$$

$$1\,\mathrm{mA} = \frac{1}{2}(1.08\,\mathrm{mA\,V^{-2}})(V_{OV})^2$$

$$V_{OV}^2 = \frac{2\,\mathrm{mA}}{1.08\,\mathrm{mA\,V^{-2}}} \approx 1.8519\,\mathrm{V}^2$$

$$V_{OV} = \sqrt{1.8519\,\mathrm{V}^2} \approx 1.361\,\mathrm{V}$$

3. Transconductance (g_m) and Gate-Source Voltage (V_{GS})
The transconductance g_m is:

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2 \cdot 1\,\mathrm{mA}}{1.361\,\mathrm{V}} \approx 1.4695\,\mathrm{mA\,V^{-1}} \text{ (or } 1.47\,\mathrm{mS)}$$

The gate-source voltage V_{GS} is:

$$V_{GS} = V_{OV} + V_{tn} = 1.361\,\mathrm{V} + 1.45\,\mathrm{V} = 2.811\,\mathrm{V}$$

4. Early Effect Resistance (r_o)
The output resistance of the transistor itself is:

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{(0.0146\,\mathrm{V^{-1}})(1\,\mathrm{mA})} = \frac{1}{0.0000146\,\mathrm{S}} \approx 68\,493\,\Omega \text{ or } 68.5\,\mathrm{k\Omega}$$

5. Source Resistor (R_S)
First, we find the DC source voltage V_S using $V_G = 0\,\mathrm{V}$:

$$V_{GS} = V_G - V_S \implies 2.811\,\mathrm{V} = 0\,\mathrm{V} - V_S \implies V_S = -2.811\,\mathrm{V}$$

The resistor R_S connects the source terminal (V_S) to the negative supply ($V_- = -15\,\mathrm{V}$). The DC current through R_S is $I_S = I_D = 1\,\mathrm{mA}$ (since $I_G = 0$).

$$R_S = \frac{V_S - V_-}{I_D} = \frac{-2.811\,\mathrm{V} - (-15\,\mathrm{V})}{1\,\mathrm{mA}} = \frac{12.189\,\mathrm{V}}{1\,\mathrm{mA}} = 12.19\,\mathrm{k\Omega}$$

This value is very close to the standard E24 resistor value of $12.1\,\mathrm{k\Omega}$.

1.3 AC Analysis

For the AC model, all capacitors (C_{C1}, C_{C2}, C_S) are treated as short circuits, and DC supplies (V_+, V_-) are treated as AC ground.

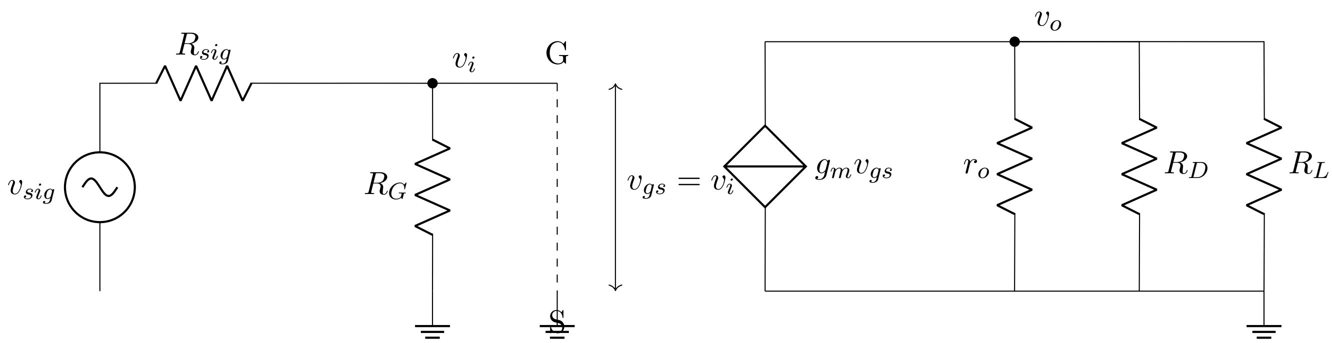

Figure 2: AC Small-Signal Model of the Common-Source Amplifier

1. Input Voltage Ratio (v_i/v_{sig})
The AC input resistance R_{in} of the amplifier is R_G in parallel with the gate's infinite resistance, so $R_{in} = R_G = 10\,\text{k}\Omega$. This forms a voltage divider with the signal source resistance R_{sig}.

$$\frac{v_i}{v_{sig}} = \frac{R_{in}}{R_{sig} + R_{in}} = \frac{R_G}{R_{sig} + R_G} = \frac{10\,000\,\Omega}{50\,\Omega + 10\,000\,\Omega} = \frac{10000}{10050} \approx 0.995$$

This ratio is very close to 1, so for further calculations, we can approximate $v_i \approx v_{sig}$.

2. Drain Resistor (R_D) for Gain $A_v = -5$ V/V
The AC bypass capacitor C_S shorts R_S to ground, so the source is at AC ground. The small-signal voltage gain $A_v = v_o/v_i$ is:

$$A_v = -g_m(r_o \parallel R_D \parallel R_L)$$

We need to solve for R_D to achieve $A_v = -5\,\text{V/V}$.

$$-5\,\text{V/V} = -(1.4695\,\text{mS})(68.5\,\text{k}\Omega \parallel R_D \parallel 10\,\text{k}\Omega)$$

First, let's combine the known parallel resistances $R'_L = r_o \parallel R_L$:

$$R'_L = \frac{68.5\,\text{k}\Omega \cdot 10\,\text{k}\Omega}{68.5\,\text{k}\Omega + 10\,\text{k}\Omega} = \frac{685}{78.5} \approx 8.726\,\text{k}\Omega$$

Now substitute this back into the gain equation:

$$5 = (1.4695\,\text{mS})(R_D \parallel 8.726\,\text{k}\Omega)$$

Let $R_{eq} = R_D \parallel 8.726\,\text{k}\Omega$. We solve for this equivalent resistance:

$$R_{eq} = \frac{5}{1.4695\,\text{mS}} \approx 3.4025\,\text{k}\Omega$$

Now, we can solve for R_D:

$$\frac{1}{R_{eq}} = \frac{1}{R_D} + \frac{1}{R'_L} \implies \frac{1}{R_D} = \frac{1}{R_{eq}} - \frac{1}{R'_L}$$

$$\frac{1}{R_D} = \frac{1}{3.4025\,\mathrm{k\Omega}} - \frac{1}{8.726\,\mathrm{k\Omega}} \approx 0.0002939 - 0.0001146 = 0.000\,179\,3\,\mathrm{k\Omega}^{-1}$$

$$R_D = \frac{1}{0.0001793} \approx 5.577\,\mathrm{k\Omega}$$

A standard $5.6\,\mathrm{k\Omega}$ resistor would be a suitable choice.

3. DC Drain Voltage (V_D) and Saturation Check

Using our calculated $R_D = 5.577\,\mathrm{k\Omega}$, we find the DC drain voltage V_D:

$$V_D = V_+ - I_D R_D = 15\,\mathrm{V} - (1\,\mathrm{mA})(5.577\,\mathrm{k\Omega}) = 15\,\mathrm{V} - 5.577\,\mathrm{V} = 9.423\,\mathrm{V}$$

To be in saturation, the transistor must satisfy $V_{DS} \geq V_{OV}$.

$$V_{DS} = V_D - V_S = 9.423\,\mathrm{V} - (-2.811\,\mathrm{V}) = 12.234\,\mathrm{V}$$

Check: $V_{DS}(12.234\,\mathrm{V}) \geq V_{OV}(1.361\,\mathrm{V})$. The condition is clearly met, so the transistor is operating in the saturation region as assumed.

4. Amplifier Output Resistance (R_o)

The output resistance R_o of the amplifier (as defined in the lab manual, step 2) is the resistance looking into the drain, *before* R_L is attached. This is R_D in parallel with r_o.

$$R_o = R_D \parallel r_o = 5.577\,\mathrm{k\Omega} \parallel 68.5\,\mathrm{k\Omega}$$

$$R_o = \frac{5.577\,\mathrm{k\Omega} \cdot 68.5\,\mathrm{k\Omega}}{5.577\,\mathrm{k\Omega} + 68.5\,\mathrm{k\Omega}} = \frac{381.99}{74.077} \approx 5.157\,\mathrm{k\Omega}$$

2 Summary of Calculated Values

The following table summarizes all the key calculated values from the design and analysis of the NMOS common-source amplifier:

Table 1: Summary of Calculated Design Parameters

Parameter	**Symbol**	**Value**	**Section**
DC Operating Point			
DC Gate Current	I_G	$0\,\text{A}$	1.2
DC Gate Voltage	V_G	$0\,\text{V}$	1.2
Overdrive Voltage	V_{OV}	$1.361\,\text{V}$	1.2
Transconductance	g_m	$1.47\,\text{mS}$	1.2
Gate-Source Voltage	V_{GS}	$2.811\,\text{V}$	1.2
Early Effect Resistance	r_o	$68.5\,\text{k}\Omega$	1.2
DC Source Voltage	V_S	$-2.811\,\text{V}$	1.2
Source Resistor	R_S	$12.19\,\text{k}\Omega$	1.2
AC Analysis and Design			
Input Voltage Ratio	v_i/v_{sig}	0.995	1.3
Drain Resistor	R_D	$5.577\,\text{k}\Omega$	1.3
DC Drain Voltage	V_D	$9.423\,\text{V}$	1.3
Drain-Source Voltage	V_{DS}	$12.234\,\text{V}$	1.3
Voltage Gain	A_v	$-5\,\text{V/V}$	1.3
Output Resistance	R_o	$5.157\,\text{k}\Omega$	1.3
Design Goals & Given Parameters			
Drain Current (Design)	I_D	$1\,\text{mA}$	1.1
Positive Supply	V_+	$15\,\text{V}$	1.1
Negative Supply	V_-	$-15\,\text{V}$	1.1
Signal Source Resistance	R_{sig}	$50\,\Omega$	1.1
Load Resistance	R_L	$10\,\text{k}\Omega$	1.1
Gate Resistance	R_G	$10\,\text{k}\Omega$	1.1
Channel-Length Modulation	λ	$0.0146\,\text{V}^{-1}$	1.1
Transconductance Parameter	k_n	$1.08\,\text{mA}\,\text{V}^{-2}$	1.1
Threshold Voltage	V_{tn}	$1.45\,\text{V}$	1.1

Note: The transistor is confirmed to be in saturation since $V_{DS} = 12.234\,\text{V} \geq V_{OV} = 1.361\,\text{V}$.