Miniproject 1

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1 Schematics

This section includes the screenshots for transistor-level schematics for a CMOS inverter and a two-input NAND gate. Additionally, it contains a symbol level schematic for a two-input AND gate loaded with a 200-fF capacitor for the transient simulation.

1.1 CMOS Inverter

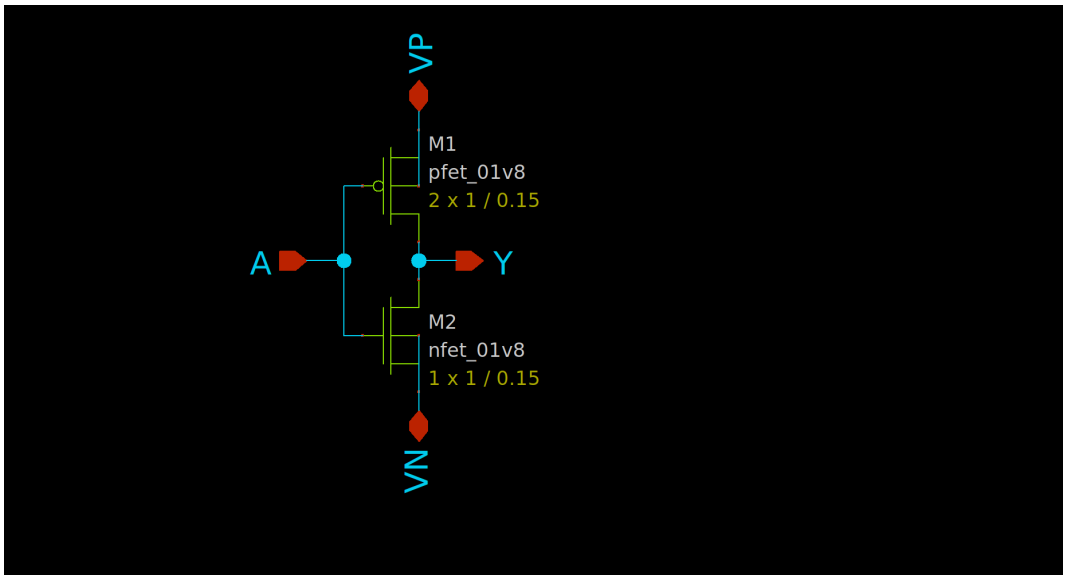

Figure 1: CMOS Inverter Schematic

1.2 Two-input NAND Gate

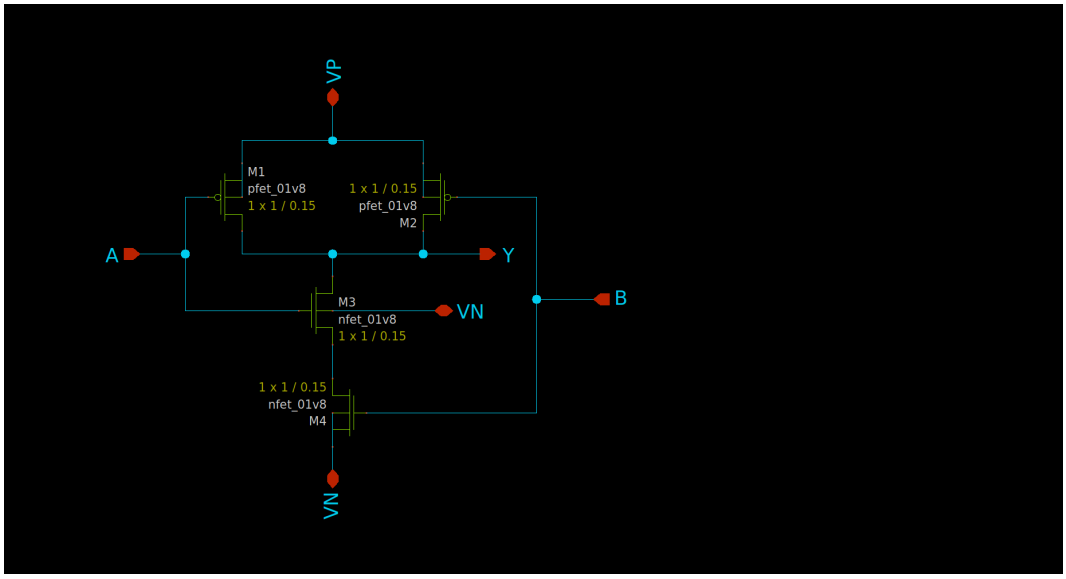

Figure 2: Two-input NAND Gate Schematic

1.3 Two-input AND Gate

1.3.1 Using NAND + Inverter

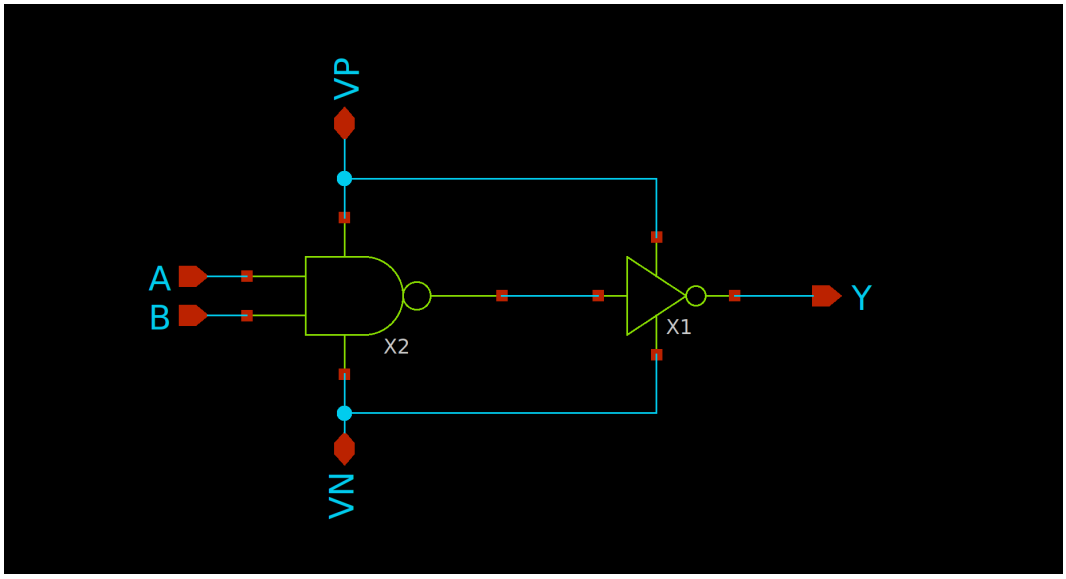

Figure 3: Two-input AND Gate Schematic

1.3.2 Two-input AND Gate

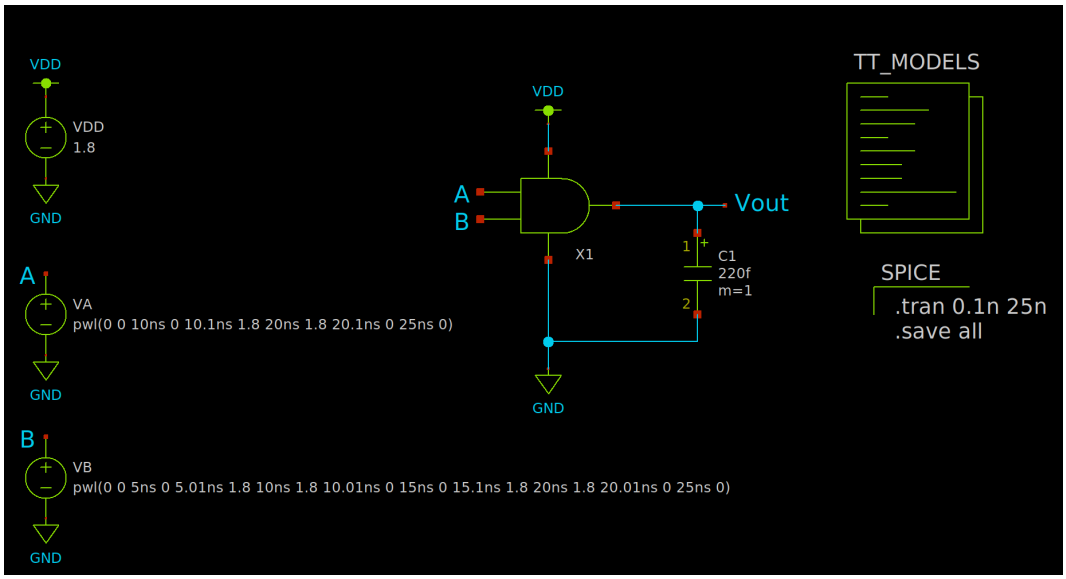

Figure 4: Two-input AND Gate Schematic

1.3.3 Two-input AND Gate Transient Simulation

Simulation inputs and output are summarized below:

A	B	$A\&B$
0	0	0
0	1	0
1	0	0
1	1	1

Note: 0 here stands for 0V, and the 1 would equate to 1.8V input.

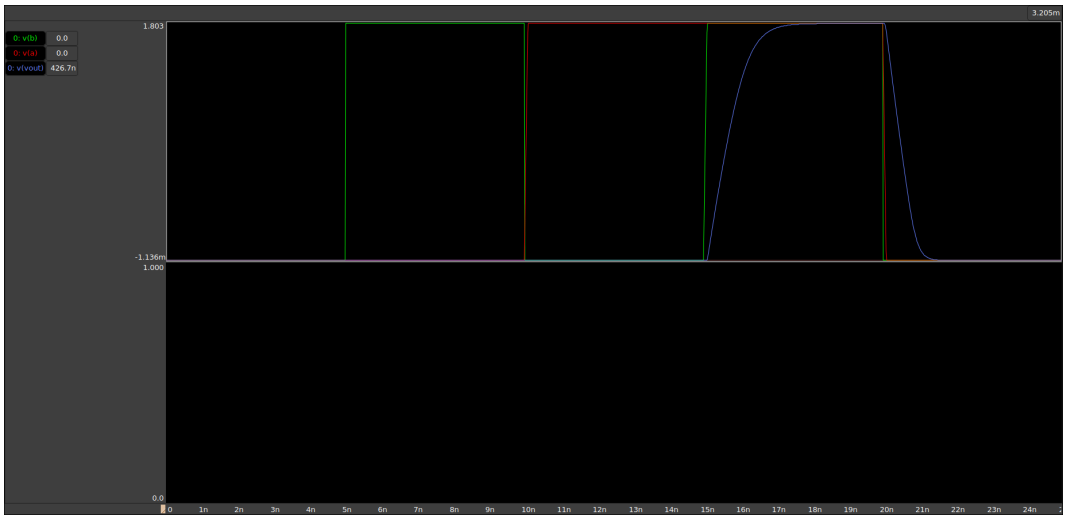

Figure 5: Two-input AND Gate Transient Simulation

2 Layout

This section includes the top-level layout for a 2-input AND gate prepared in Magic. The layout is free of design rule violations, with the AND gate's inputs and output available at the boundary of the top-level cell.

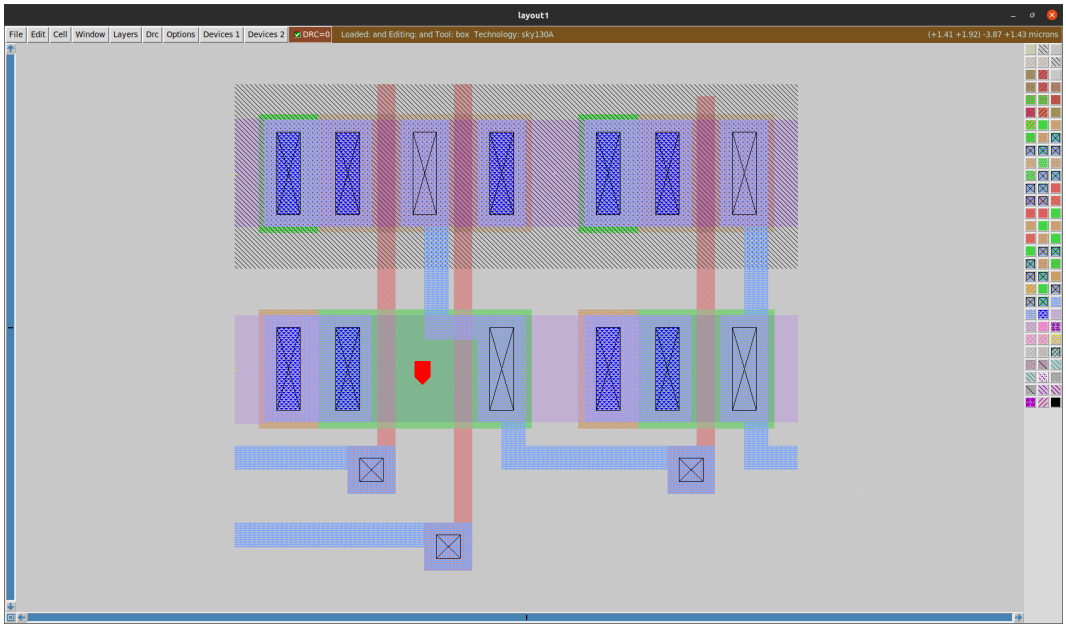

Figure 6: Two-input AND Gate Layout

3 Layout Versus Schematic Report

The netlists from the two-input AND gate from Xschem and Magic are compared to generate the LVS report using Netcomp. The two netlists match uniquely.

```
Equate elements:  no current cell.
Equate elements:  no current cell.

Subcircuit summary:
Circuit 1: inverter                        |Circuit 2: inverter
-------------------------------------------|---------------------------
sky130_fd_pr__pfet_01v8 (1)                |sky130_fd_pr__pfet_01v8 (1)
sky130_fd_pr__nfet_01v8 (1)                |sky130_fd_pr__nfet_01v8 (1)
Number of devices: 2                       |Number of devices: 2
Number of nets: 4                          |Number of nets: 4
-------------------------------------------|---------------------------
Circuits match uniquely.
Property errors were found.
Netlists match uniquely.
There were property errors.
sky130_fd_pr__pfet_01v80 vs. sky130_fd_pr__pfet_01v8M1:
 w circuit1: 1   circuit2: 2   (delta=66.7%, cutoff=1%)

Subcircuit pins:
Circuit 1: inverter                        |Circuit 2: inverter
-------------------------------------------|---------------------------
Y                                          |Y
A                                          |A
VP                                         |VP
VN                                         |VN
-------------------------------------------|---------------------------
Cell pin lists are equivalent.
Device classes inverter and inverter are equivalent.

Subcircuit summary:
Circuit 1: nand                            |Circuit 2: nand
-------------------------------------------|---------------------------
sky130_fd_pr__pfet_01v8 (2)                |sky130_fd_pr__pfet_01v8 (2)
sky130_fd_pr__nfet_01v8 (2)                |sky130_fd_pr__nfet_01v8 (2)
Number of devices: 4                       |Number of devices: 4
Number of nets: 6                          |Number of nets: 6
-------------------------------------------|---------------------------
Circuits match uniquely.
Netlists match uniquely.

Subcircuit pins:
Circuit 1: nand                            |Circuit 2: nand
-------------------------------------------|---------------------------
Y                                          |Y
VN                                         |VN
A                                          |B **Mismatch**
B                                          |A **Mismatch**
VP                                         |VP
```

```
-------------------------------------------|----------------------------
Cell pin lists are equivalent.
Device classes nand and nand are equivalent.

Subcircuit summary:
Circuit 1: and.spice                       |Circuit 2: and_xschem.spice
-------------------------------------------|----------------------------
inverter (1)                               |inverter (1)
nand (1)                                   |nand (1)
Number of devices: 2                       |Number of devices: 2
Number of nets: 6                          |Number of nets: 6
-------------------------------------------|----------------------------
Circuits match uniquely.
Netlists match uniquely.
Cells have no pins;  pin matching not needed.
Device classes and.spice and and_xschem.spice are equivalent.
Circuits match uniquely.
The following cells had property errors: inverter
```

4 Design Files

All of the design file are available on a GitHub repository that is linked here.