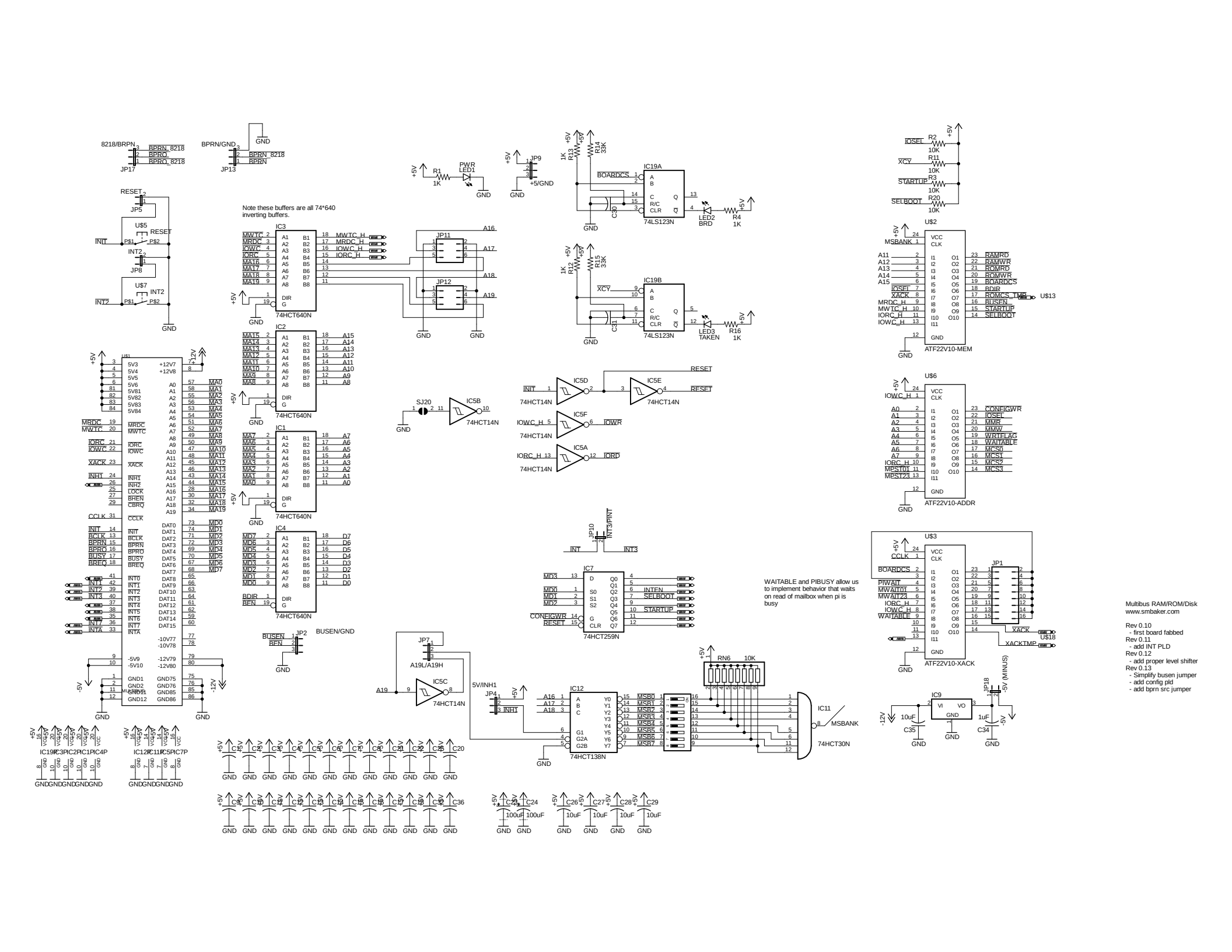
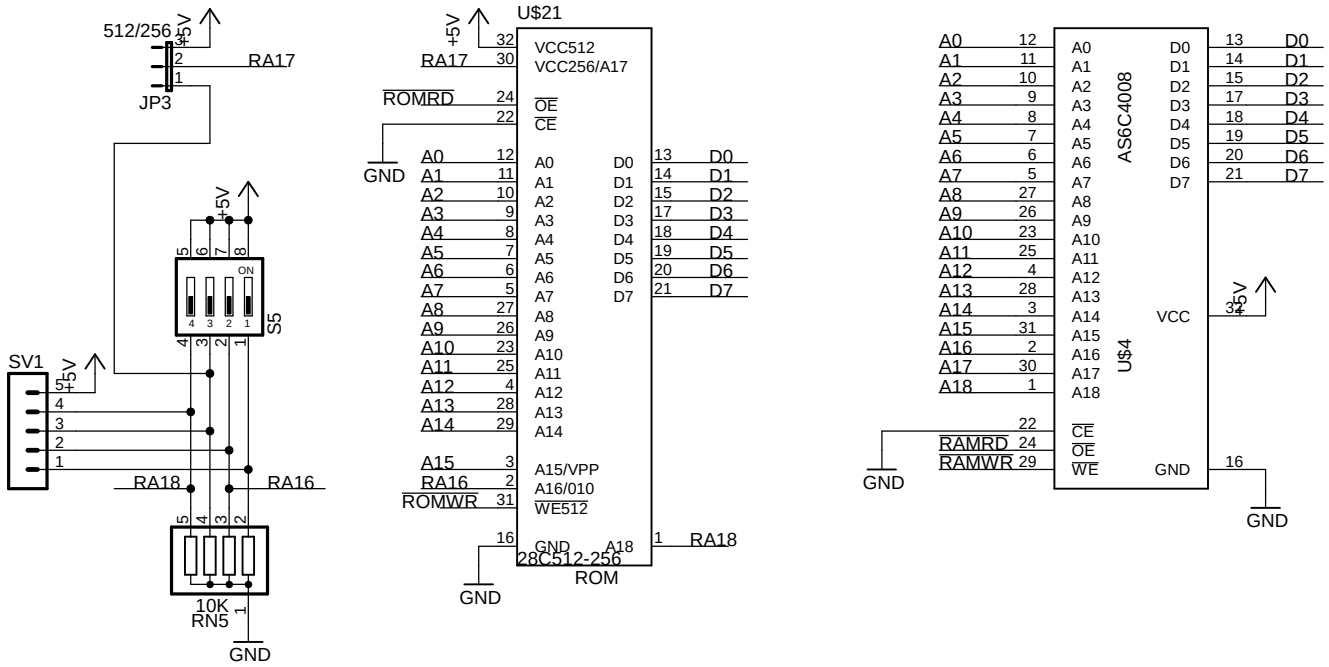
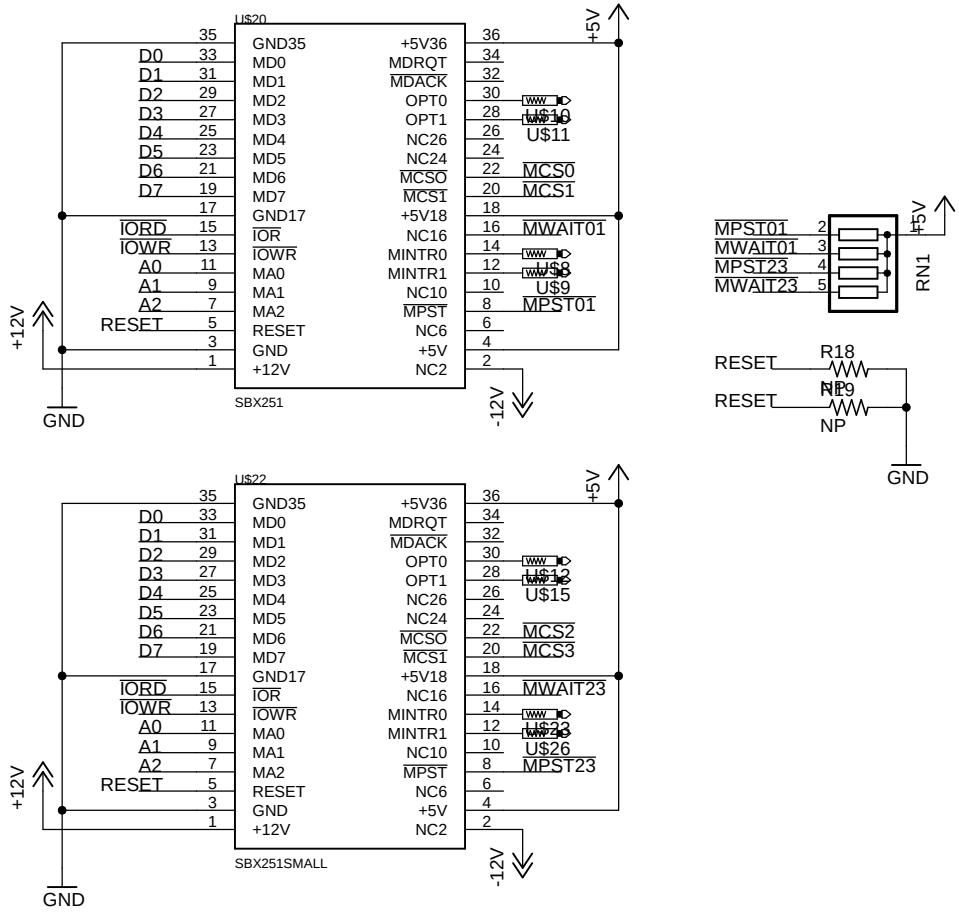
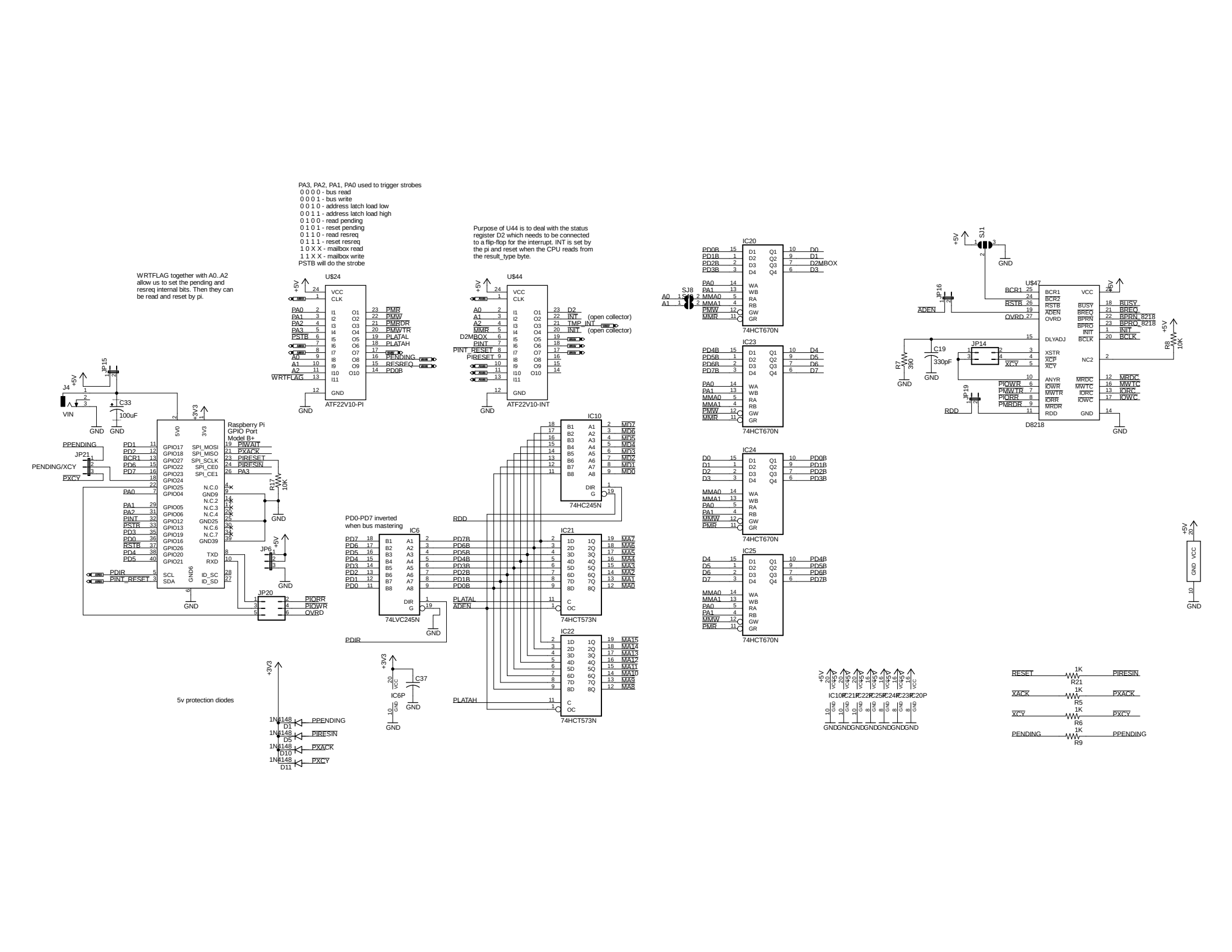

8218/BRPN
BPRN_8218
BPRO
BPRO_8218
JP17
BPRN/GND
BPRN_8218
BPRN
JP13
GND
RESET
JP5
U$5
RESET
INIT
P$1
P$2
INT2
JP8
U$7
INT2
INT2
P$1
P$2
GND
PWR
LED1
R1
1K
GND
JP9
+5V
+5/GND
GND
Note these buffers are all 74*640
inverting buffers.
IC3
MWTC
MRDC
IOWC
IORC
MA16
MA17
MA18
MA19
MWTC_H
MRDC_H
IOWC_H
IORC_H
74HCT640N
JP11
JP12
A16
A17
A18
A19
IC2
MA15
MA14
MA13
MA12
MA11
MA10
MA9
MA8
A15
A14
A13
A12
A11
A10
A9
A8
74HCT640N
IC1
MA7
MA6
MA5
MA4
MA3
MA2
MA1
MA0
A7
A6
A5
A4
A3
A2
A1
A0
74HCT640N
IC4
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
D7
D6
D5
D4
D3
D2
D1
D0
BDIR
BEN
74HCT640N
BUSEN
BEN
JP2
BUSEN/GND
GND
SJ20
IC5B
74HCT14N
IC5D
IC5E
IC5F
IC5A
INIT
IOWC_H
IORC_H
RESET
IOWR
IORD
74HCT14N
JP10
INT3/PINT
INT
INT3
IC7
MD3
MD0
MD1
MD2
CONFIGWR
RESET
INTEN
SELBOOT
STARTUP
74HCT259N
WAITABLE and PIBUSY allow us
to implement behavior that waits
on read of mailbox when pi is
busy
JP7
A19L/A19H
A19
IC5C
74HCT14N
5V/INH1
JP4
INH1
IC12
A16
A17
A18
MSB0
MSB1
MSB2
MSB3
MSB4
MSB5
MSB6
MSB7
74HCT138N
RN6
10K
IC11
MSBANK
74HCT30N
IC19
IC3
IC2
IC1
IC4
IC12
IC11
IC5
IC7
IC19A
IC19B
BOARDCS
XCY
74LS123N
C30
C31
LED2
BRD
LED3
TAKEN
R4
1K
R16
1K
R13
1K
R14
33K
R12
1K
R15
33K
IOSEL
XCY
STARTUP
SELBOOT
R2
10K
R11
10K
R3
10K
R20
10K
U$2
MSBANK
A11
A12
A13
A14
A15
IOSEL
XACK
MRDC_H
MWTC_H
IORC_H
IOWC_H
RAMRD
RAMWR
ROMRD
ROMWR
BOARDCS
BDIR
ROMCS_TWO
BUSEN
STARTUP
SELBOOT
U$13
ATF22V10-MEM
U$6
IOWC_H
A0
A1
A2
A3
A4
A5
A6
A7
IORC_H
MPST01
MPST23
CONFIGWR
IOSEL
MMR
MMW
WRTFLAG
WAITABLE
MCS0
MCS1
MCS2
MCS3
ATF22V10-ADDR
U$3
CCLK
BOARDCS
PIWAIT
MWAIT01
MWAIT23
IORC_H
IOWC_H
WAITABLE
JP1
XACK
XACKTMP
U$18
ATF22V10-XACK
IC9
VI
VO
GND
10uF
1uF
C35
C34
-5V (MINUS)
JP18
-12V
+5V
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
C30
C31
C32
C33
C34
C35
C36
100uF
10uF
Multibus RAM/ROM/Disk
www.smbaker.com
Rev 0.10
- first board fabbed
Rev 0.11
- add INT PLD
Rev 0.12
- add proper level shifter
Rev 0.13
- Simplify busen jumper
- add config pld
- add bprn src jumper


512/256
+5V
JP3
RA17
+5V
ON
S5
SV1
+5V
RA18
RA16
10K
RN5
GND
U$21
+5V
RA17
ROMRD
GND
VCC512
VCC256/A17
OE
CE
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15/VPP
A16/010
WE512
GND
A18
D0
D1
D2
D3
D4
D5
D6
D7
A15
RA16
ROMWR
RA18
28C512-256
ROM
GND
AS6C4008
U$4
VCC
+5V
RAMRD
RAMWR
GND
GND


U$20
GND35
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
GND17
IOR
IOWR
MA0
MA1
MA2
RESET
GND
+12V
+5V36
MDRQT
MDACK
OPT0
OPT1
NC26
NC24
MCSO
MCS1
+5V18
NC16
MINTR0
MINTR1
NC10
MPST
NC6
+5V
NC2
D0
D1
D2
D3
D4
D5
D6
D7
IORD
IOWR
A0
A1
A2
RESET
U$10
U$11
MCS0
MCS1
MWAIT01
U$8
U$9
MPST01
+5V
-12V
GND
SBX251
U$22
MCS2
MCS3
MWAIT23
U$12
U$15
U$23
U$26
MPST23
SBX251SMALL
MPST01
MWAIT01
MPST23
MWAIT23
RN1
R18
R19
NP
GND


PA3, PA2, PA1, PA0 used to trigger strobes
0 0 0 0 - bus read
0 0 0 1 - bus write
0 0 1 0 - address latch load low
0 0 1 1 - address latch load high
0 1 0 0 - read pending
0 1 0 1 - reset pending
0 1 1 0 - read resreq
0 1 1 1 - reset resreq
1 0 X X - mailbox read
1 1 X X - mailbox write
PSTB will do the strobe
WRTFLAG together with A0..A2 allow us to set the pending and resreq internal bits. Then they can be read and reset by pi.
Purpose of U44 is to deal with the status register D2 which needs to be connected to a flip-flop for the interrupt. INT is set by the pi and reset when the CPU reads from the result_type byte.
U$24
ATF22V10-PI
U$44
ATF22V10-INT
(open collector)
(open collector)
Raspberry Pi GPIO Port Model B+
PD0-PD7 inverted when bus mastering
IC6
74LVC245N
IC10
74HC245N
IC20
IC21
IC22
74HCT573N
IC23
IC24
IC25
74HCT670N
U$47
D8218
5v protection diodes
1N4148 D1
1N4148 D5
1N4148 D10
1N4148 D11
IC6P
IC10
IC21
IC22
IC25
IC24
IC23
IC20
R21 1K
R5 1K
R6 1K
R9 1K