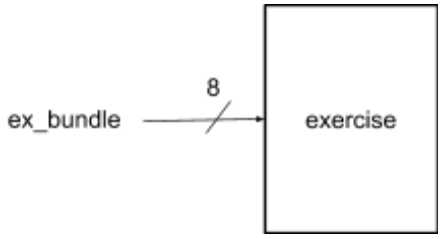
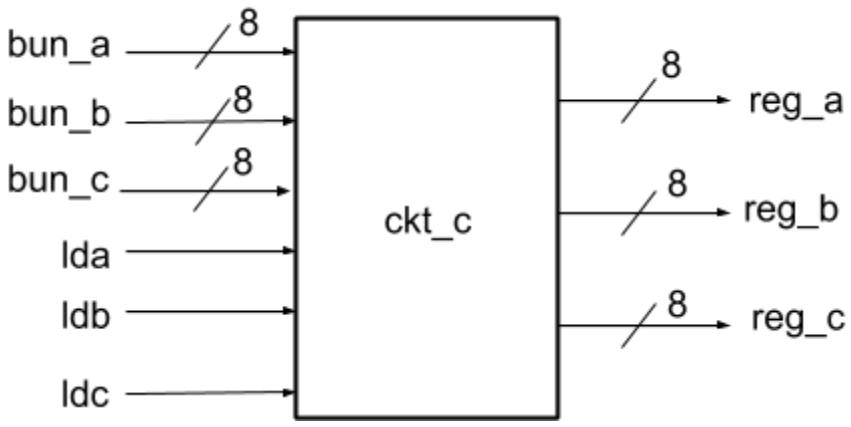
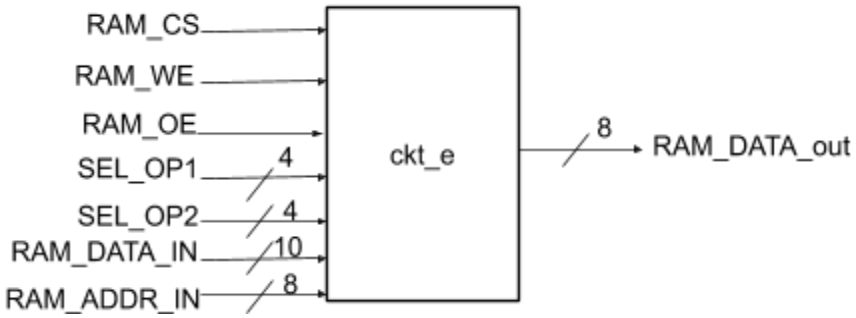
1. The word bundle refers to a bus, or multiple signals with a similar purpose within one.
2. Bundles are usually represented in black-box diagrams as a single arrow with a line going through it and a number denoting how many signals are in that bundle:



3. Drawing a black-box diagram when using VHDL to model digital circuits is a good approach because it makes it easier to understand the overall circuit, what its inputs and output are, and aids in defining the entity in the VHDL code.
4.
    a.
    ```
    entity sys1 is
    port( a_in1, b_in1, clk, ctrl_int: in std_logic;
          Out_b:                       out std_logic);
    end sys1;
    ```
    b.
    ```
    entity sys2 is
    port( input_w, clk:      in std_logic;
          a_data, b_data: in std_logic_vector(7 downto 0);
          dat_4:             out std_logic_vector(7 downto 0);
          dat_5:             out std_logic_vector(2 downto 0);
    end sys2;
    ```
5.
    a.



b.



6.

a. There should be a semicolon at the end of the CLK line:
   CLK : in std_logic;
b. There should be a parentheses at the end of the last port line to indicate there are no additional ports:
   byte_out : out std_logic_vector(3 downto 0));