BIAN, Song

Email   sbian@buaa.edu.cn
Department/Institution   School of Cyber Science and Technology
                                   Beihang University

Address
No. 37 Xueyuan Rd., Haidian, Beijing, 100191, China
Webpage
https://sbian3.github.io/

Employment	**Tenure-Track Associate Professor (2021–present)** School of Cyber Science and Technology, Beihang University **Assistant Professor (2019–2021)** Department of Communications and Computer Engineering, Graduate School of Informatics, Kyoto University
Education	**Kyoto University (2014–2019)** Department of Communications and Computer Engineering, Graduate School of Informatics Ph.D., Informatics, 2019. Fields: Hardware Security, Applied Cryptography M.Sc., Informatics, 2017 (GPA 4/4). **University of Wisconsin-Madison (2011–2014)** Department of Electrical and Computer Engineering, College of Engineering B.Sc., Computer Engineering, 2014 (GPA 4/4).
Dissertation	"Realizing Homomorphic Secure Protocols through Cross-Layer Design Techniques"
Professional Services	Technical Program Committee/Reviewer AAAI 2021; ASP-DAC 2021, 2020 Journal of Cryptology ACM Transactions on Design Automation of Electronic Systems IEEE Transactions on Circuits and Systems I
Fellowships	**Kyoto University** 2017–2019 JSPS Research Fellow

Project: Aging Prediction and Fault Prevention for Large-Scale Integrated Circuits from Cross-Layer Design Methods

Awards and Fellowships	**International Student Scholarship, Marietta College** 2009-2011
	Dean's Honor List 2012-2014
	Edgar H. and Laverne R. Krainer Memorial Scholarship 2013
	Graduated with Highest Distinction 2014
	ACM/IEEE GLSVLSI 2016 Student Travel Award 2016
	IPSJ DA Symposium 2015 Excellent Student Presentation Award 2016
	IPSJ DA Symposium 2016 Excellent Student Presentation Award 2017
	IPSJ DA Symposium 2016 Best Paper Award 2017
	IPSJ Computer Science Research Award for Young Scientists 2017
	IEEE Kansai Section Student Paper Award 2018
	IEICE VLD Excellent Student Author Award for ASP-DAC 2019 2019
	IEEE Services 2020 Hackathon Top Winning Award 2020
Languages	Chinese (native), Japanese (JLPT N1), English (TOEFL iBT 111/120)

List of Publications

Peer-Reviewed Journal and Conference Publications

1. Ryotaro Banno, Kotaro Matsuoka, Naoki Matsumoto, **Song Bian**, Masaki Waga, Kohei Suenaga, Oblivious Online Monitoring for Safety LTL Specification via Fully Homomorphic Encryption, Computer Aided Verification (CAV), August 2022.

2. Tianchen Wang, Jiawei Zhang, Jinjun Xiong, **Song Bian**, Zheyu Yan, Meiping Huang, Jian Zhuang, Takashi Sato, Yiyu Shi, and Xiaowei Xu, VisualNet: An End-to-End Human Visual System Inspired Framework to Reduce Inference Latency of Deep Neural Networks, IEEE Transactions on Computers, June 2022.

3. Shumpei Morita, **Song Bian**, Michihiro Shintani, and Takashi Sato, Efficient Analysis for Mitigation of Workload-dependent Aging Degradation, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), February 2022.

4. Kotaro Matsuoka, Yusuke Hoshizuki, Takashi Sato and **Song Bian**, Towards better standard cell library: Optimizing compound logic gates for TFHE, Proc. ACM 9th Workshop on Encrypted Computing & Applied Homomorphic Cryptography (WAHC), November 2021.

5. **Song Bian**, Dur E Shahwar Kundi, Kazuma Hirozawa, Weiqiang Liu, and Takashi Sato, APAS: Application-Specific Accelerators for RLWE-based Homomorphic Linear Transformations, IEEE Transactions on information Forensics and Security (TIFS), September 2021.

6. Kotaro Matsuoka, Ryotaro Banno, Naoki Matsumoto, Takashi Sato, and **Song Bian**, Virtual Secure Platform: A Five-Stage Pipeline Processor over TFHE, *USENIX* Security Symposium (Virtual), August 2021.

7. **Song Bian**, Weiwen Jiang, and Takashi Sato, Privacy-Preserving Medical Image Segmentation via Hybrid Trusted Execution Environment, ACM/IEEE Design Automation Conference (DAC), July 2021.

8. Tatsuki Ono, **Song Bian**, Takashi Sato, Automatic Parallelism Tuning for Module Learning with Errors Based Post-Quantum Key Exchanges on GPUs, Proc. of IEEE International Symposium on Circuits and Systems (ISCAS) (Hybrid), May 2021.

9. Yuki Tanaka, **Song Bian**, Takashi Sato, Clonable PUF: on the Design of PUFs That Share Equivalent Responses, Proc. of IEEE International Symposium on Circuits and Systems (ISCAS) (Virtual), May 2021.

10. Qian Lou, **Song Bian**, and Lei Jiang, AutoPrivacy: Automated Layer-wise Parameter Selection for Secure Neural Network Inference, in Proc. of Conference on Neural Information Processing Systems (NeurIPS) (Virtual), December 2020.

11. **Song Bian**, Xiaowei Xu, Weiwen Jiang, Yiyu Shi, and Takashi Sato, BUNET: Blind Medical Image Segmentation Based on Secure UNET, in Proc. of International Conference on Medical Image Computing and Computer-Assisted Intervention (MICCAI) (Virtual), October 2020.

12. Akira Dan, Riu Shimizu, Takeshi Nishikawa, **Song Bian** and Takashi Sato, Clustering Approach for Solving Traveling Salesman Problems via Ising Model Based Solver, in Proc. of ACM/IEEE Design Automation Conference (DAC) (Virtual), pp.1-6, July 2020.

13. **Song Bian**, Weiwen Jiang, Qing Lu, Yiyu Shi, and Takashi Sato, NASS: Optimizing Secure Inference via Neural Architecture Search, in Proc. of European Conference on Artificial Intelligence (ECAI) (Virtual), June 2020.

14. **Song Bian**, Tianchen Wang, Masayuki Hiromoto, Yiyu Shi, and Takashi Sato, ENSEI: Efficient Secure Inference via Frequency-Domain Homomorphic Convolution for Privacy-Preserving Visual Recognition, in Proc. of IEEE/CVF Conference on Computer Vision and Pattern Recognition (CVPR) (Virtual), pp.9403-9412, June 2020.

15. Dur E Shahwar Kundi, **Song Bian**, Ayesha Khalid, Chenghua Wang, Maire O'Neill, and Weiqiang Liu, AxMM: Area and Power Efficient Approximate Modulo Multiplier for R-LWE Cryptosystem, in Proc. of IEEE International Symposium on Circuits and Systems (ISCAS) (Virtual), May 2020.

16. Yuki Kume, **Song Bian**, and Takashi Sato, A Tuning-Free Hardware Reservoir Based on MOSFET Crossbar Array for Practical Echo State Network Implementation, in Proc. of ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC) (Beijing, China), pp.458-463, January 2020.

17. Kunihiro Oshima, **Song Bian** and Takashi Sato, Estimation of NBTI-Induced Timing Degradation Considering Duty Ratio, Proc. The 22nd workshop on synthesis and system integration of mixed information technologies (SASIMI), October 2019.

18. Tatsuki Ono, **Song Bian** and Takashi Sato, Improved Multiplier Architecture on ASIC for RLWE-based Key Exchange, Proc. The 22nd workshop on synthesis and system integration of mixed information technologies (SASIMI), October 2019.

19. **Song Bian**, Masayuki Hiromoto, and Takashi Sato, Filianore: Better Multiplier Architectures for LWE-based Post-Quantum Key Exchange, in Proc. of ACM/IEEE Design Automation Conference (DAC) (Las Vegas, NV), pp.1-6, June 2019.

20. **Song Bian**, Masayuki Hiromoto, and Takashi Sato, DArL: Dynamic Parameter Adjustment for LWE-based Secure Inference, in Proc. of Design, Automation and Test in Europe (DATE) (Florence, Italy), pp.1718-1723, March 2019.

21. **Song Bian**, Masayuki Hiromoto, and Takashi Sato, Hardware-Accelerated Secured Naive Bayesian Filter Based on Partially Homomorphic Encryption, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E102-A, No.2, pp.430-439, Febuary 2019.

22. **Song Bian**, Masayuki Hiromoto, and Takashi Sato: Towards Practical Homomorphic Email Filtering: A Hardware-Accelerated Secure Naive Bayesian Filter, in Proc. of Asia and South Pacific Design Automation Conference (ASP-DAC) (Tokyo Odaiba Waterfront, Japan), pp.621-626, January 2019.

23. **Song Bian**, Masayuki Hiromoto, and Takashi Sato, DWE: Decrypting Learning with Errors with Errors, in Proc. of ACM/IEEE Design Automation Conference (DAC) (San Francisco, CA), 10.3, June 2018.

24. Yuki Tanaka, **Song Bian**, Masayuki Hiromoto, and Takashi Sato: Coin Flipping PUF: A Novel PUF with Improved Resistance Against Machine Learning Attacks, IEEE Transactions Circuits and Systems II: Express Briefs, Vol.65, No.5, pp.602-606, May 2018.

25. Yuki Tanaka, **Song Bian**, Masayuki Hiromoto, and Takashi Sato, Coin Flipping PUF: a New PUF with Improved Resistance Against Machine Learning Attacks, in Proc. of IEEE International Symposium on Circuits and Systems (ISCAS) (Florence, Italy), pp.1-6, May 2018.

26. Zuitoku Shin, Shumpei Morita, **Song Bian**, Michihiro Shintani, Masayuki Hiromoto, and Takashi Sato, A Study on NBTI-induced Delay Degradation Considering Stress Frequency Dependence, in Proc. of International Symposium on Quality Electronic Design (ISQED) (Santa Clara, CA), pp.251-256, March 2018.

27. Zuitoku Shin, Shumpei Morita, **Song Bian**, Michihiro Shintani, Masayuki Hiromoto, and Takashi Sato, Comparative Study of Delay Degradation Caused by NBTI Considering Stress Frequency Dependence, in Proc. of the 21st Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI2018) (Kunibiki Messe, Matsue, Japan), pp.194-199, March 2018.

28. Yuki Tanaka, **Song Bian**, Masayuki Hiromoto, and Takashi Sato, A PUF Based on the Instantaneous Response of Ring Oscillator Determined by the Convergence Time of Bistable Ring, in Proc. of the 21st Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI2018) (Kunibiki Messe, Matsue, Japan), pp.30-34, March 2018.

29. Shumpei Morita, **Song Bian**, Michihiro Shintani, Masayuki Hiromoto, and Takashi Sato, Efficient exploration of worst case workload and timing degradation under NBTI, in Proc. of Asia and South Pacific Design Automation Conference (ASP-DAC) (Jeju Island, Korea), pp.631-636, January 2018.

30. **Song Bian**, Shumpei Morita, Michihiro Shintani, Hiromitsu Awano, Masayuki Hiromoto, and Takashi Sato, Identification and Application of Invariant Critical Paths Under NBTI Degradation, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E100-A, No.12, pp.2797-2806, December 2017.

31. Shumpei Morita, **Song Bian**, Michihiro Shintani, Masayuki Hiromoto, and Takashi Sato, Utilization of Path-Clustering in Efficient Stress-Control Gate Replacement for NBTI Mitigation, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E100-A, No.7, pp.1464-1472, July 2017.

32. **Song Bian**, Michihiro Shintani, Masayuki Hiromoto, and Takashi Sato, LSTA: Learning-Based Static Timing Analysis for High-Dimensional Correlated On-Chip Variations, in Proc. of ACM/IEEE Design Automation Conference (DAC) (Austin, TX), 73.3, June 2017.

33. **Song Bian**, Masayuki Hiromoto, and Takashi Sato, SCAM: Secured Content Addressable Memory Based on Homomorphic Encryption, in Proc. of Design, Automation and Test in Europe (DATE) (Lausanne, Switzerland), pp.984-989, March 2017.

34. Shumpei Morita, **Song Bian**, Michihiro Shintani, Masayuki Hiromoto, and Takashi Sato, Comparative Study of Path Selection and Objective Function in Replacing NBTI Mitigation Logic, Proc. of International Symposium on Quality Electronic Design (ISQED), March 2017.

35. **Song Bian**, Michihiro Shintani, Zheng Wang, Masayuki Hiromoto, Anupam Chattopadhyay, and Takashi Sato, Runtime NBTI Mitigation for Processor Lifespan Extension via Selective Node Control, in Proc. of IEEE Asian Test Symposium (ATS) (Hiroshima, Japan), pp.234-239, November 2016.

36. Shumpei Morita, **Song Bian**, Michihiro Shintani, Masayuki Hiromoto, and Takashi Sato, Path Grouping Approach for Efficient Candidate Selection of Replacing NBTI Mitigation Logic, in Proc. of the 20th Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI2016) (Kyoto Research Park, Kyoto, Japan), pp.242-247, October 2016.

37. **Song Bian**, Michihiro Shintani, Masayuki Hiromoto, and Takashi Sato: Fast Estimation of NBTI-Induced Delay Degradation Based on Signal Probability, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E99-A, No.7, pp.1400-1409, July 2016.

38. **Song Bian**, Michihiro Shintani, Shumpei Morita, Hiromitsu Awano, Masayuki Hiromoto, and Takashi Sato, Workload-Aware Worst Path Analysis of Processor-Scale NBTI Degradation, in Proc. of Great Lakes Symposium on VLSI (GLSVLSI) (Boston, MA), pp.203-208, May 2016.

39. **Song Bian**, Michihiro Shintani, Zheng Wang, Masayuki Hiromoto, Anupam Chattopadhyay, and Takashi Sato, Mitigation of NBTI-induced Timing Degradation in Processor, in Proc. of ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU) (Santa Rosa, CA), pp.50-55, March 2016.

40. **Song Bian**, Michihiro Shintani, Shumpei Morita, Masayuki Hiromoto, and Takashi Sato, Nonlinear Delay-Table Approach for Full-Chip NBTI Degradation Prediction, in Proc. of International Symposium on Quality Electronic Design (ISQED) (Santa Clara, CA), pp.307-312, March 2016.

41. Kai-wen Hsu, He Ren, Robert J. Agasie, **Song Bian**, Yoshi Nishi, and Leon J. Shohet: Effects of neutron irradiation of ultra-thin HfO2 films. Applied Physics Letters, Vol.104, No.3, 032910, 2014.