DESIGN AND DEVELOPMENT OF 4-BIT ADDER PROGRAMMABLE QCA DESIGN USING ALU TECHNIQUE

(CONTINUOUS ACCESSMENT AND MINI PROJECT)

by

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DECLARATION

I declare that this written submission represents my ideas in my own words and where others' ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

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CERTIFICATE

It is certified that the work contained in the Continuous Assessment and Mini project(CAMP) titled “DESIGN AND DEVELOPMENT OF 4-BIT ADDER PROGRAMMABLE QCA DESIGN USING ALU TECHNIQUE,” by “Ramakrishnan R, bearing Roll No: 21BLC1013” has been carried out under my supervision and that this work has not been submitted elsewhere for a degree*

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ABSTRACT :

The design and development of a 4-bit adder programmable using the Quantum-dot Cellular Automata (QCA) technology and the Arithmetic Logic Unit (ALU) technique is an innovative approach to achieve high-speed and low-power digital computation. This project aims to explore the potential of QCA-based circuits in implementing complex arithmetic operations, offering promising prospects for future advancements in the field of digital design and computation. QCA technology leverages room-temperature electron transport to construct nanoscale circuits. It exhibits the potential to supplant conventional CMOS technology in low-power and high-performance applications QCA circuits consist of arrays of quantum dots that interact to perform binary calculations, offering a promising avenue for future advancements in digital computation.

CONTENTS

INTRODUCTION:

QCA as the name suggests stands for Quantum dot Cellular Automata is a domain in nano-technology employed in several digital circuits and stupendously used in electronics world. With the advancement in VLSI designs and technology, QCA design acts a powerful tool in modern day electronics in solving adder circuits. QCA cells can be utilized in many ways to study PLD design. This method basically proposes specialized architecture procedure to program devices and simulation is also done to tune QCA cells aimed for this specialized development design. This design provides an insight and idea about how adders are implemented in measuring and electronic instruments and their applications in the digital world. The performance of the respective QCA cell structures are simulated and it is tested by designer tools. It is cost – effective and relatively uses very less equipment. This mainly discusses about the area and transistor count with propagation delay. The main idea of this paper is to show how QCA cells are implemented by ALU technique with 4-bit adder circuit.

LITERATURE REVIEW

Introduction:
The design and development of digital circuits using Quantum-dot Cellular Automata (QCA) technology has gained significant attention in recent years due to its potential for ultra-low power and high-performance computing. In this literature review, we will focus on the design and development of a 4-bit adder using programmable QCA design with the utilization of Arithmetic Logic Unit (ALU) techniques. The aim is to explore the existing research and advancements in this area, highlighting key methodologies, challenges, and potential future directions.

Overview of Quantum-dot Cellular Automata (QCA):
This section provides an introduction to the fundamental concepts of QCA, explaining its principles of operation, benefits, and limitations. It discusses the key components of QCA, such as cells, wires, and clocks, and how they contribute to the design of digital circuits.

Design and Implementation of 4-Bit Adders in QCA:
This section focuses on various approaches and techniques used for designing and implementing 4-bit adders in QCA. It discusses the basic building blocks required for constructing a 4-bit adder, such as XOR and AND gates, and how they can be realized using QCA. The section explores different architectural designs, including ripple carry and carry look-ahead adders, and their performance characteristics in terms of area, power consumption, and delay.

Programmable QCA Design:
In this section, the concept of programmable QCA design is explored. It discusses the advantages of programmability in QCA circuits, allowing for reconfiguration and flexibility. Various techniques for achieving programmability in QCA are reviewed, such as using full adders, look-up tables, or configurable logic blocks. The section then focuses on the application of programmability in designing a 4-bit adder and its impact on circuit performance and functionality.

ALU Techniques in QCA Design:
This section investigates the utilization of Arithmetic Logic Unit (ALU) techniques in the design of QCA-based 4-bit adders. It discusses the role of ALU in performing arithmetic and logical operations, such as addition, subtraction, and bitwise operations. Different ALU architectures, including carry-select and carry-skip adders, are analyzed in the context of QCA design. The section also explores the challenges and considerations of implementing ALU techniques in QCA, such as signal propagation and circuit complexity.

Performance,Evaluation and Comparison:
This section presents a comparative analysis of the designed 4-bit adder using ALU techniques in QCA with other existing approaches. It discusses the metrics used for performance evaluation, such as area, power consumption, delay, and fault tolerance. The section highlights the advantages and limitations of the proposed design and provides insights into potential improvements and optimizations.

Challenges and Future Directions:
The final section discusses the challenges and open research questions in the design and development of 4-bit adder programmable QCA designs using ALU techniques. It addresses potential issues related to scalability, manufacturing processes, and integration with conventional computing architectures. The section also suggests future directions for research, including exploring advanced ALU architectures, optimization algorithms, and error correction techniques.

Conclusion:
This literature review provides a comprehensive overview of the design and development of 4-bit adder programmable QCA designs using ALU techniques. It covers the fundamental concepts of QCA, different design methodologies, programmability, and the role of ALU in enhancing circuit functionality. The review highlights the performance characteristics of the proposed designs, challenges faced, and potential future research directions. This knowledge can serve as a foundation for further exploration and innovation in the field of QCA-based digital circuit designing.

CHAPTER – 1

FUNDAMENTALS OF QCA CELLS:

QCA Cells: Basically QCA cells are also termed in emergency technologies and have the potential to build future computers through ALU. In QCA, a device which is sensitive called QCA cell is used as a fundamental unit of QCA block for growth or maturation of small number of constituent particles applied in a circuit. We arrive at a term called quantum dot placed at a proper diagonal square cut in a linear order. Polarization is a process where it is used in field of electromagnetic radiations in which the direction and magnitude are specified of a vibrating particle.

CHAPTER - 2

QCA CLOCKING :

QCA is a field of nanotechnology that is utilised in contemporary sciences, proven in the present, and occasionally taught in CMOS semiconductor . The most crucial aspect of constructing circuits is reaching a dimension where possibility is a problem. High power and leakage current are used. It is a well-known, practical technology with few flaws. A QCA cell is made up of a few free electrons that are most likely constrained in a potential . It uses CMOS technology, and an ALU design is used to manage QCA processes. Four clocking systems are performed on polarised data on a periodic basis. Every digital logic design involves a lot of work. Engineers were able to reduce the size of the semiconductor thanks to considerable new work in the field of frilled technology. Finding a 4-bit adder using carbon nanotubes and QCA cells based on the

existing CMOS-based VLSI technology is unique since it may boost scaling by reducing or preventing high power consumption.

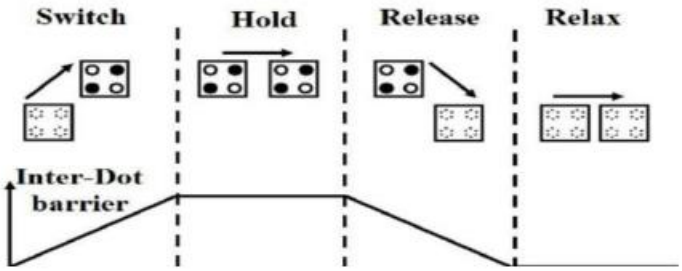


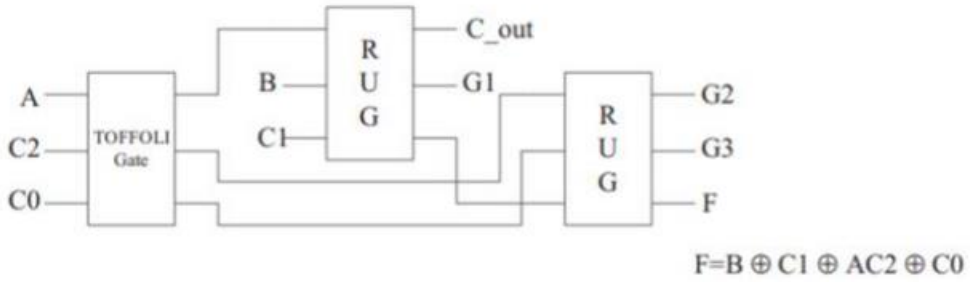
Fig 1(b): process of QCA

CHAPTER – 3

FUNCTIONALITIES OF ARITHMETIC LOGIC UNIT (ALU):

3.1 Reversible ALU:

It is an arithmetic circuit and an integral component of CPU in the monitor system. The number of logical calculations selected varies depending on the number of inputs and outputs according to the circuit. It is widely used in QCA cells to interpret output using arithmetic logic [2]. The implementation of ALU in CPU and few other applications have complex design and cost-effective [4]. It is basically divided into two modules reverse logic unit (RLU) and reversible arithmetic unit (RAU), ALU is flexible is implemented in logic gates.



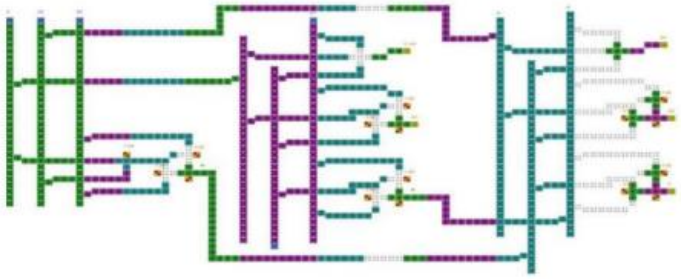
3.2. Reversible Logic Unit (RLU):

Usually 4:1 Mux is generally preferred multiplexer and it is a 1 bit logic gates and acts a CNOT gate and uses 4RM gates connected in linear fashion. This can be then advanced to 4-bit adder gates also [2].The combinations of binary numbers such as 0 and 1 are tried in varied combinations in various gates and realized through A0,A1,A2,A3 by gates such as NOR,NAND,AND,OR and EX-OR gates.

The functional description is shown below in Fig 2 (b) and QCA cells representation in 2(c).

A0	A1	A2	A3	Operation
0	0	0	0	NOT
0	0	1	0	NAND
0	0	1	1	XOR
0	1	0	0	NOR
0	1	0	1	-
0	1	1	0	NOT
1	0	0	1	COPY
1	0	1	0	Constant
1	0	1	1	OR
1	1	0	0	XNOR
1	1	0	1	AND
1	1	1	1	COPY

Fig 2(b): Functional description of RLU



3.3. Reverse Arithmetic Unit:

A reverse arithmetic unit being a fundamental unit of ALU does the inverse operation of ALU .It consists of a full adder which has 5 input and 2 outputs. To this contrary there are 6 garbage outputs (G0, G1, G2, G3, G4, G5).These are the fundamental functionalities of RAU .It has the following inputs: M, N, O', O'', O''', O4. It clocks nearly 6 clock delays with a time delay.

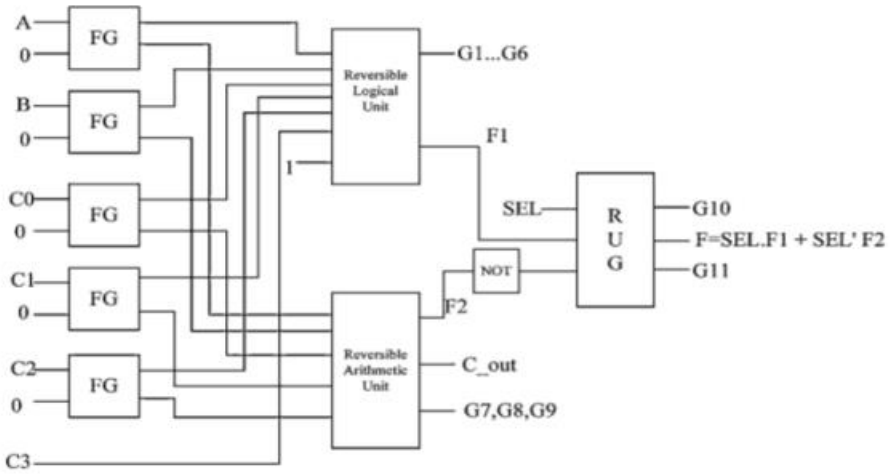
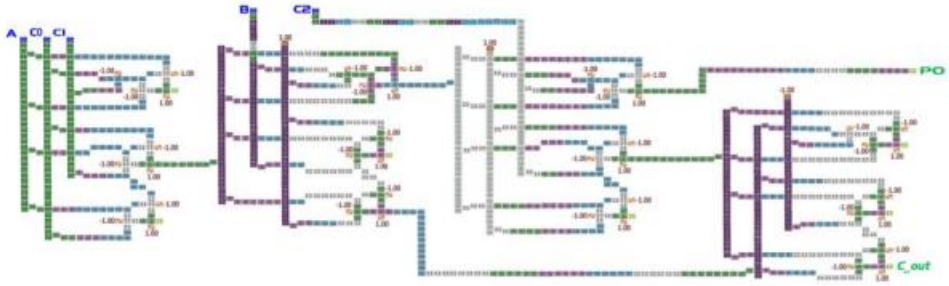


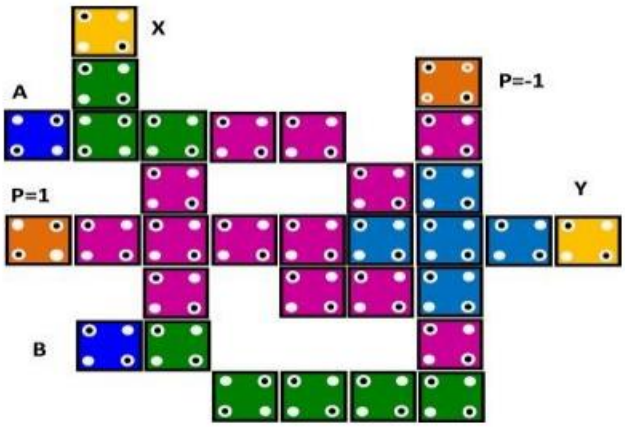
Fig 2(d): Functional description of RAU using decoders



3.4. Fault tolerance of RUG:

This process occurs during QCA manufacturing which consists of various phases that include both deposition and synthesis phase it includes additional cells and cell misalignment in reverse unit logic design. We use Verilog library for the implementation of QCA cells, this can be

converted into hardware language that majorly includes Verilog HDL definitions and elements of QCA like fan-out, fan-in, and many other applications of logic design. These QCA cells come from fault injection capability. It has a respective HDLQ Model of RUG. We assign certain variables like A, B, Y, where P=1.



EXPERIMENTAL PROCEDURE :

SOFTWARES USED :

- **QCADESIGNER**
- **CADENCE VIRTUOSO**
- **VERILOG HDL**

Method of approach

This method basically proposes specialized architecture procedure to program devices and simulation is also done to tune QCA cells aimed for this specialized development design meaning it can be manipulated to serve many operations and not specifically manufactured for a particular implementer.

Design Strategy

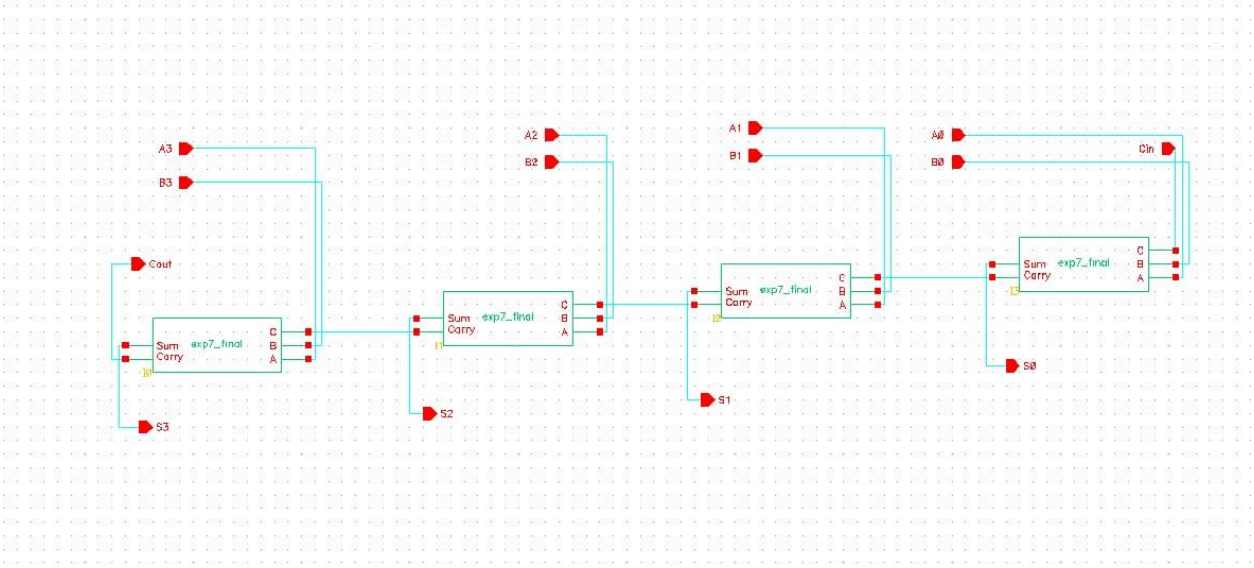
The design was simulated and optimized using QCADesigner and Verilog. The design was then fabricated using Cadence Virtuoso and the design was tested with input-output waveform.

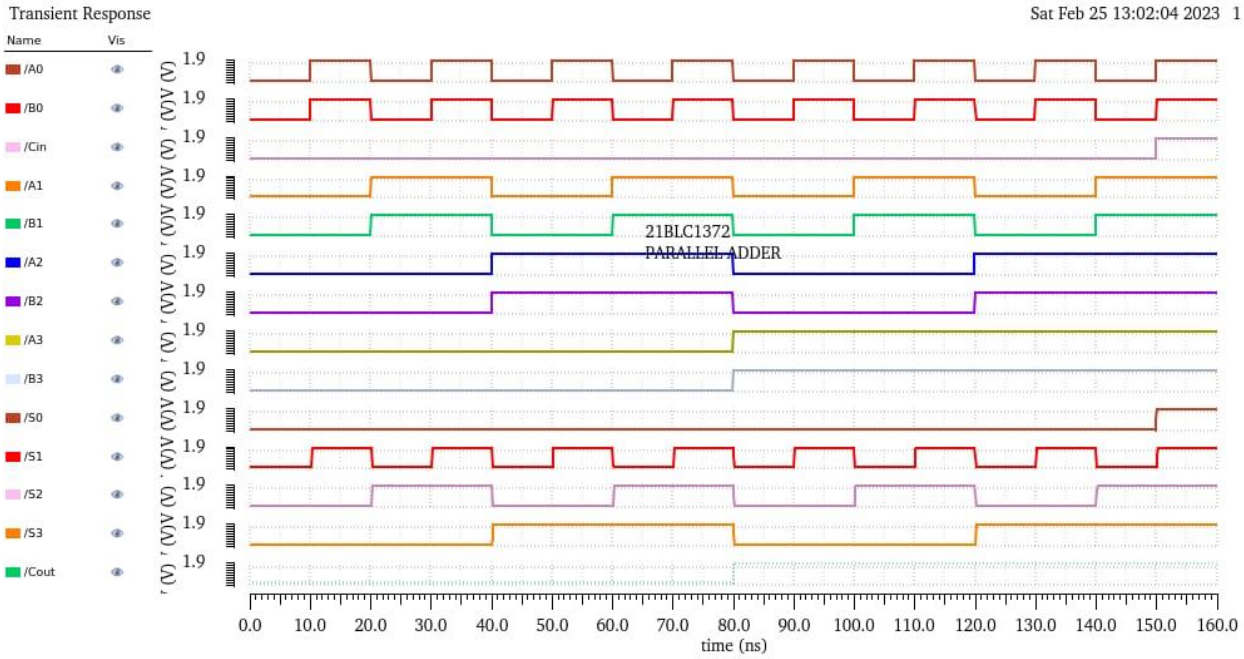
Simulation and Optimization

The circuit was simulated to analyze its performance and was optimized to increase performance and reduce spatial complexity via the ALU technique.

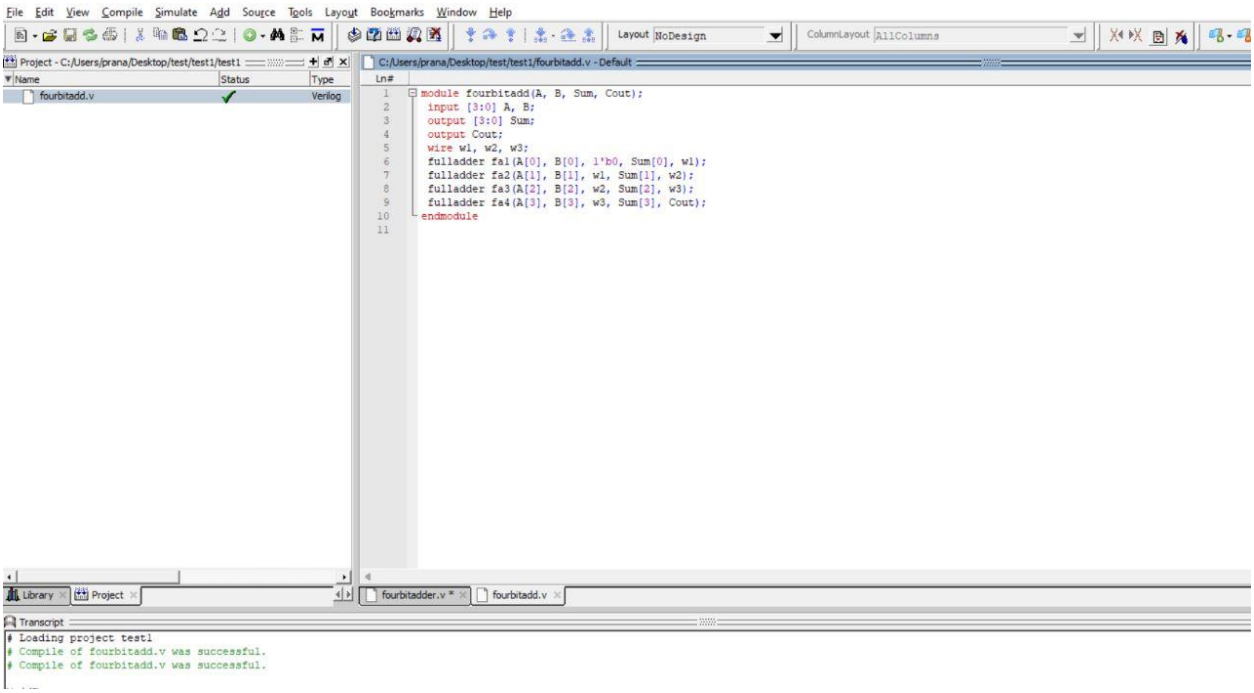
RESULTS :

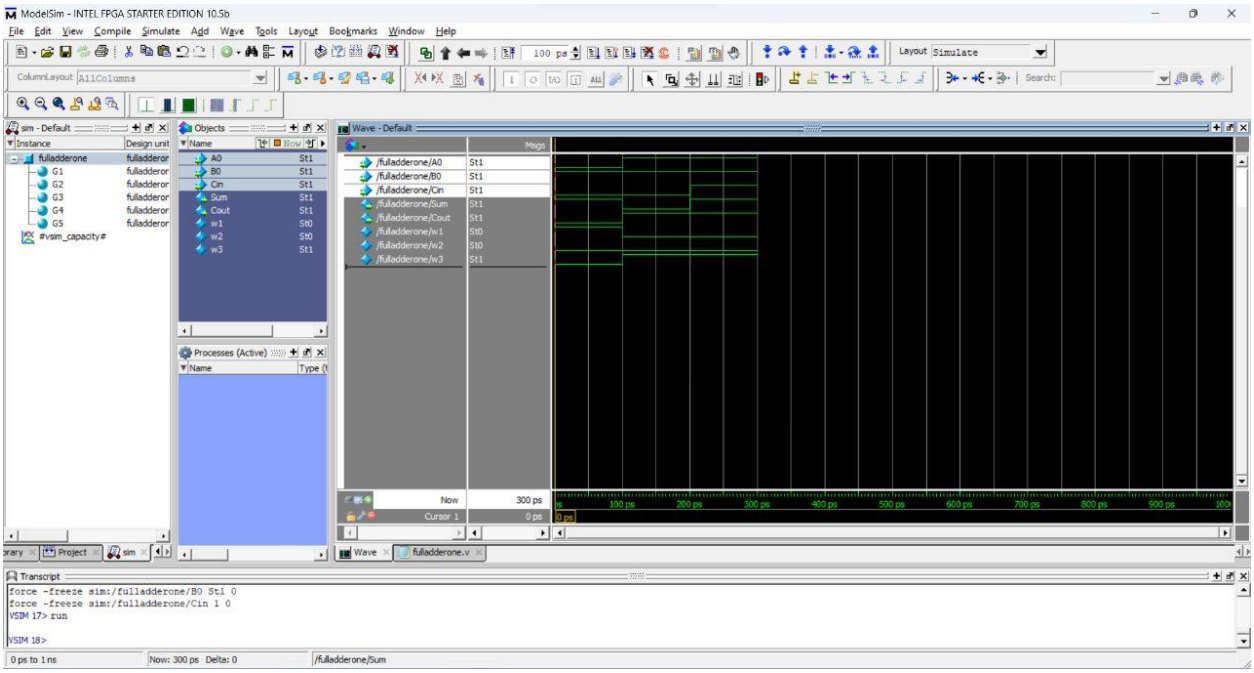
CADENCE CIRCUIT AND OUTPUT :



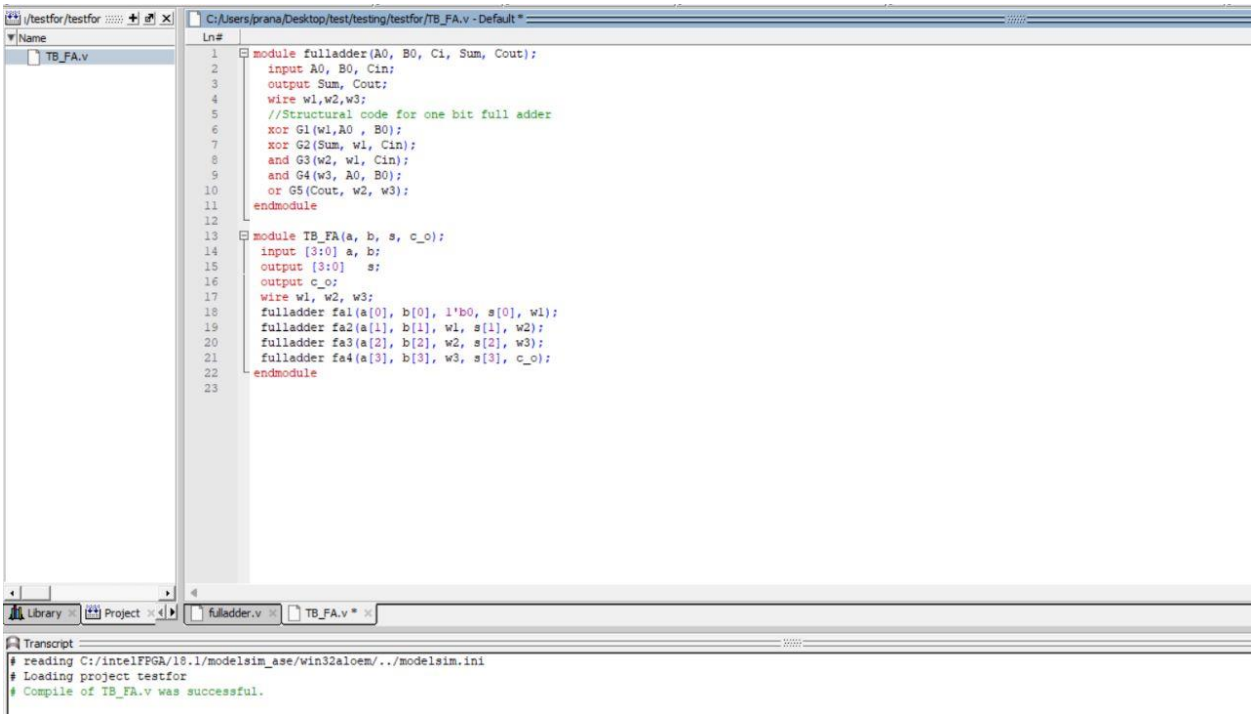


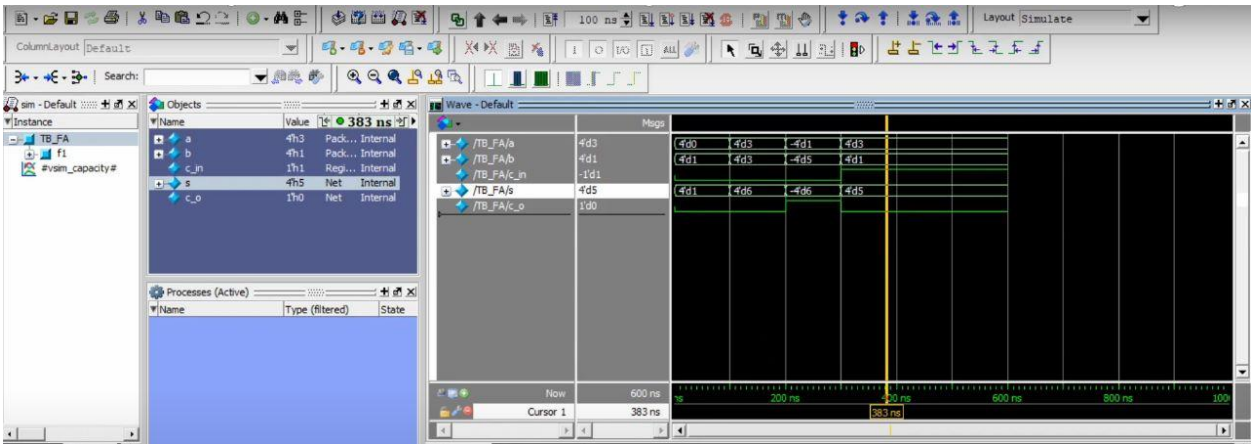
VERILOG CODE AND OUTPUT FOR CMOS :



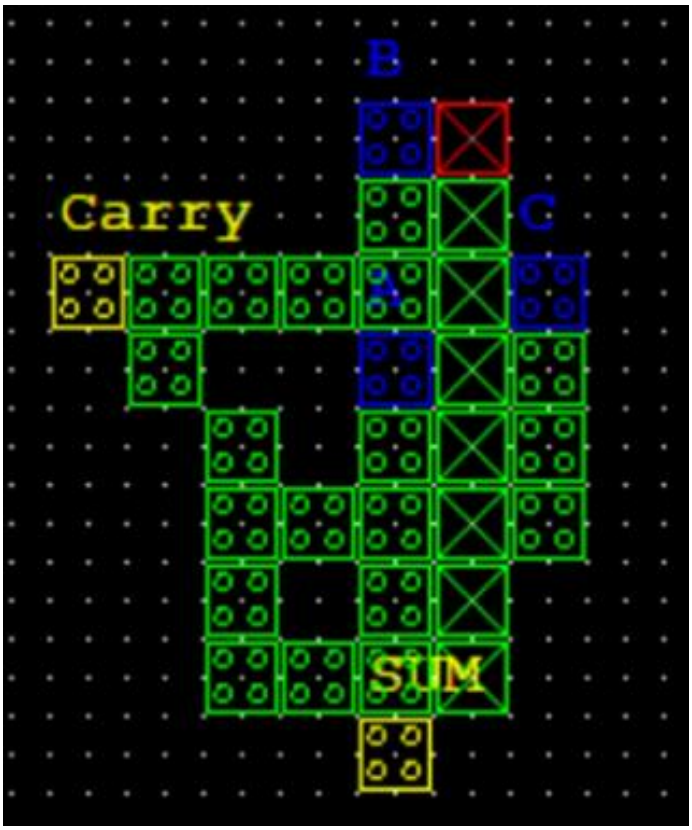


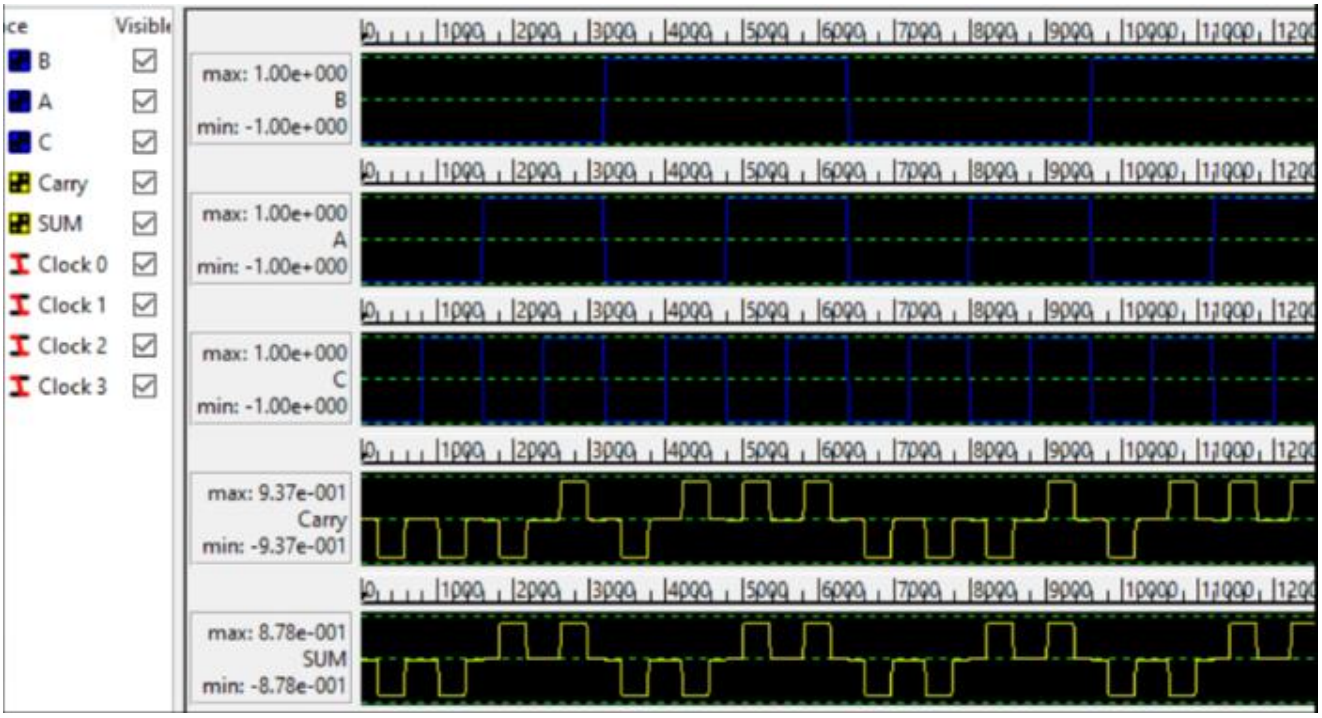
VERILOG CODE AND OUTPUT FOR 4 BIT ADDER :





QCA REPRESENTATION USING QCA DESIGNER :





Understanding the results:

While the traditional CMOS circuits simulated using Verilog and the real world model using cadence provide accurate outputs they take time on the degree of nanoseconds. The same simulation in QCA takes far less time as seen in the simulation popup of QCADesigner tool. Apart from this the range of temperature where qca cells can implement logic is far superior to CMOS as there is minimal current flow in qca due to electrons moving using quantum tunnelling whereas in transistors there's a current flow through the channel and when millions of such transistors are used it results in emitting heat which slows down the processor as a whole. The model we have simulated if optimized and established physically can help a great deal in resolving the heat issues.

FUTURE SCOPE IN THIS AREA:

- With the use of the ALU technique, several QCA design techniques are used, including the 3 bit, 4 bit, and 5 bit binary to grey converter and the grey to BCD converter. To save exact data and information through codes, this ishelpful.
- Using the QCA Designer tool, the suggested layout is simulated and the layout circuits are designed. The suggesteddesigns are created using the least amount of cells and the shortest possible clock delays. Studies indicate that the designs have high switching speeds and are both area-efficient and fast. K-maps and truth tables are used to double-check the expected findings. A detailed explanation of the implementation is provided by QCA code

  converters logic circuits. These could reduce error detection in the not too distant future, leading to technology thatis mistake-free. ALU is essentially employed in all software applications, and the integration of QCA cells made it possible to combine computer science and electronics in the near future thanks to the development of the VLSI technology network globally.

CONCLUSIONS:

In the proposed work we have earlier discussed about the development of 4-Bit Adder circuits using QCA design by ALU technique which has provided a framework for advancement of 16-bit adders using VLSI technique. It had also confirmed the acceptability of the counter design of the circuit. This journal mainly speaks about various ALU techniques and how they are used to form a 4-bit adder circuit by many processes which include polarization. The circuits will hold the operation stability on hold and makes the QCA cells in ALU effective and sustainable thus being useful to majority of people around the world. The given XOR gate carried out by QCA cells turned out to be a significant logic gate for composite QCA structure domain which further were fully utilized for complex configuration systems. The expected input and output waveforms were taken from the designer kit. The proposed methods uses very new complex values in Lab View. The proposed power and propagation delay of CMOS and normal ALU are calculated in a tabular column. Thus, in this paper the main objectives of reversible ALU which all together had two domains name, i.e.: RLU and RAU which thoroughly justified by providing an area efficient model for 4 bit adder circuits design. This reflects the work that has more pros or advantages in the field of VLSI in the near future because of less power dissipation and efficient noise removal.

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