6.334 Design Project

Rod Bayliss III

16 May, 2018

Contents

Chapter 1

Overview

Starting out I looked at what was going on in the device beyond what was given to me. First the max current at the load was 8.33 A while the min current was 2.083 A. Corresponding to the 100 W and 25 W power points respectively. This also meant if it was a resistive load at max power it would be 1.44 Ω while at min power it would be 5.76 Ω. Additionally the maximum duty cycle I had to run the FET as was $\frac{2}{3}$ corresponding to an input voltage of 18 V and the maximum was 0.4 correponding to a 30 V input. Lastly I knew I wanted to design this converter to operate in CCM which impacted my output inductor choice.

1.1 Component Choices

For the FET I chose to use the NVMFS5C628NL Power MOSFET with the 527-45AB heat sink from wakefield-vette.
For the diode I chose the PMEG045V100EPD Schottky barrier using the same heatsink.
Based on losses in the switching devices I set my switching frequency to 700 kHz.
$C_{out} = 1\ \mu$ F. For this I chose a NTS ceramic cap rated for $25V_{dc}$, the first capacitor in the NTS ceramic chip capcitor series.
$L_{out} = 25\ \mu$ H. I chose an RM10 core which an $A_L = 315$ nH corresponding to a gap length of 400 μm using 9 turns.
$L_{in} = 100$ nH. I used a RM7 core with a gap of 800 μm and one turn
$C_{in} = 82\ \mu$F. I used the 82 μF cap from the Panasonic OS-CON series rated for 35 V_{dc}.
My compensator transfer function is: $K_p = 500$
Finally here is how the predicted performance compares to the specifications.

	Predicted Performance	**Requirement**
Output Voltage (static)	12.2	12 V±3%
Output Voltage (transient)	14 V	12 V ±20%
Output voltage ripple	70 mV	100 mV p-p
Input current ripple	68 mA	75 mA
Minimum efficiency	90.975%	90%

Chapter 2

Power Stage

2.1 FET

2.1.1 FET selection

After surveying the FETs I wanted to choose one that had the lowest $R_{DS,on}$ to minimize my conduction loss and was able to block the sufficient voltage and carry enough current. Because this is a direct converter both of the switching devices had to block the maximum voltage of the input and output and carry the maximum of the input and output current. This means the FET has to block 30 V and at the heaviest load of 100 W carry 8.33 A. Since all of the FETs satisfied this I searched for ones with the lowest $R_{DS,on}$. In hindsight this was not the smartest decision as I didn't find the optimal FET as conduction loss is traded with switching loss. Regardless I chose the NVMFS5C628NL Power MOSFET which had an $R_{DS,on,max}$ OF 2.4 mΩ.

2.1.2 Thermal

After choosing my MOSFET I then looked at the thermal characteristics of the device. First I characterized what heat sink I would use and how I would transfer heat from the device to the air. I used the largest copper area to connect my FET to my heatsink (Pin 5). This had an area of 18.798 mm^2. Using vias that had 1 oz plating, 12 mil of diameter and a minimum distance of 8 mil apart I ound that I could place 10 across the pad and 7 along it, yielding 70 vias in total. Using TI's AN-2020 paper,

$$R = \frac{\rho_{cu} t}{A}$$
$$R = \frac{1.6mm}{\pi(6mil)^2 - \pi(117.4\mu m)^2 * 4}$$
$$R = 135°C/W$$

Given this I know that the total thermal resistance from case to my sink is $\frac{135}{70} = 1.93°$ C/W. After finding this I wanted a heat sink that had a small footpint and would pay for the increased sink to ambient resistance through switching frequency if the losses was thermally and not efficiency limited. I then chose the 527-45AB heat sink from wakefield-vette which had a footprint of $57.9x2.4$ mm^2. Giving me a thermal resistance of 2.3° C/W. Lastly was the max junction to case ressitance which was given at 1.3° C/W. Having the full thermal model of $R_{\Theta,jc} = 1.3 + R_{\Theta,via} = 1.93 + R_{\Theta,sa} = 2.3$ I looked into my power dissipation limits for the FET.

Power dissipation in the FET is composed of two components: the conduction loss from having current flowing through a lossy element (namely the resistance between the drain and source), and the switching loss from both the output capacitance and turn on/off of the FET. Looking first at the conduction loss in the FET:

$$\langle P_{FET,cond} \rangle = \frac{1}{T} \int_0^{DT} i^2(t) R_{DS,on} \, dt$$
$$\langle P_{FET,cond} \rangle = D I_L^2 R_{DS,on}$$

From this it's clear that the worse conduction looses come from an 18 V input and a 100 W load. However even in the worse case this loss is 66.6 mW. Thus given that the junction temperature had to be limited to 150° C (which is 25° C below the maximum temperature) and the worst ambient temperature of 40° C, the maxixmum power dissipation due to the switching loss is:

$$150 = 40 + P_{diss,tot}(R_{\Theta,tot})$$
$$P_{diss,tot} = 19.892 \; W$$
$$P_{diss,sw} = 19.825 \; W$$

This gives me a limit on how fast I can switching (switching faster is nicer because smaller passives) due to switching losses scaling linearly with the switching frequency.

$$P_{FET,switching} = \frac{1}{2} f_{sw} C_{OSS} V_{IN}^2 + \frac{1}{2} I_L V_{IN} f_{sw} (t_{on} + t_o ff)$$
$$t_{on} = 55 \; ns$$
$$t_{off} = 8.5 \; ns$$
$$C_{OSS} = 1700 \; pF$$
$$f_{sw,max,thermal} = 2.28 MHz$$

Thus if I was only limited by the thermal capabilities by my device (which isn't the case, my switching frequency is determined by minimum efficiency requirements), I would choose to switch at 2.28 MHz

2.2 Diode

When choosing the diode I simply wanted the diode with the lowest forward voltage drop which would give me the nicest conduction losses. Thankfully, in contrast with the FET, I didn't have to play balancing games with the resistance of the diode and any capacitances. Thus I chose the PMEG045V100EPD Schottky barrier rectifier which had a forward voltage drop of .42 V. The diode is a little simpler to analyze since we can approximate away the switching losses inside the diode. Again, looking at the average power burned while conducting:

$$\begin{aligned}\langle P_{diode,conduction}\rangle &= \frac{1}{T}\int_{DT}^{T} V_F i_L \; dt \\ V_F &= .42 \; V \\ \langle P_{diode,conduction}\rangle &= V_F I_L (1-D) \\ \langle P_{diode,conduction,max}\rangle &= 2.099 \; W\end{aligned}$$

This maximum loss point comes from the 100 W load and the 30 V input.

2.2.1 Thermal

To deal with this conduction loss I will choose the same type of heat sink as the FET. The area of my largest pad was 14.88 mm^2. I could place 6 vias across and 9 across giving me 54 vias total. Using the same math as with the FET this gives me a total via thermal resistance of 2.5° C/W. From the datasheet my $R_{\Theta,jc} = 3°$ C/W. Again using the same $R_{\Theta,sa} = 2.3°$ C/W. Thus I have a circuit model and to keep the junction temperature below 150° C I had to dissipate less than 14.1 W, which I'm well below.

2.3 Efficiency Limits

After calculating all this I would have a converter that would work without the devices burning up and stop functioning however they are far from the efficiency limit of $\eta = 90\%$. So to reach this I looked at how much total power could be burned in my converter to meet this limit. Since my switch and diode were the only lossy elements in the converter (I'm ignoring the losses associated with the inductor), the limit I came up with would only apply to my switching elements.

$$\begin{aligned}P_{in} &= P_{out} + P_{burned} \\ \eta &= \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{burned}}\end{aligned}$$

For 100 W this meant I had to burn less than 11.1 W and for 25 W I had to burn less than 2.78 W. First looking at the 25 W case my diode performs worse at a 30 V. I care about the worse case for the diode since my FET losses are

dominated by the switching losses which don't scale with duty cycle. So at 25 W and 30 V my diode burns .525 W leaving my fet only able to burn 1.975 W. Given this my maximum switching fequency to meet baseline efficiency is 718 kHz. Looking at the 100 W case. Again, my diode burns 2.099 W and my FET frequency is limited to 994 kHz. Given that I must meet the baseline efficiency at all frequencies I chose the smaller of these two values. Leaving some room for error my converter switches at 700 kHz.
Thus I have rated my switches, provided adequate thermal management, and determined a switching frequency.

Chapter 3

Output Filter

The purpose of the output filter is to both mantain a small enough voltage ripple at the load and determine what mode of operation the converter lives in (Deep CCM, vs. boundary CCM, vs. DCM)

3.1 Inductor

The purpose of sizing the inductor is to pick what regime the converter operates in. At the light load (where the inductor ripple is the worst), the load is drawing 2.083 A. To stay in moderately deep CCM I chose my peak to peak inductor current to be 0.5 A. Given a liner inductor current slope of $\frac{V_{out}-V_{out}}{L}$ during the on-state and that the average derivative of the inductor current must be zero to satisfy PSS assumptions (so our converter doesn't blow up) we know the minimum inductance to obtain a specified inductor current ripple.

$$\begin{aligned} \triangle i_{L,pp} &= \frac{(V_{in} - V_{out})D}{f_{sw}L} \\ 0.5 &< \frac{(V_{in} - V_{out})D}{f_{sw}L} \\ L &> 20.57\ \mu H \end{aligned}$$

Knowing a minimum inductance I then designed my inductor to ensure that I didn't violate the maximum flux density of 300 mT. I knew that I wouldn't be able to meet this requirement with an ungapped core so I made sure to use an ungapped core and approximated the core reulactance to be much smaller than

my gap reluctance

$$\mathcal{R}_g = \frac{l_g}{\mu_o A}$$
$$\phi = \frac{Ni}{\mathcal{R}_g}$$
$$B_{max} = \frac{Ni_{max}\mu_o}{l_g}$$

After iterating several designs and rating my inductor current to be 10 A (a couple amps higher than my steady state max of 8.33 A), I chose an RM10 core which an $A_L = 315$ nH corresponding to a gap length of 400 μm. Using 9 turns this gave me a max B field of 283 mT and an inductance of 25.515 μH, a little bit under my saturation limit, maybe a little too close for comfort.

3.2 Capacitor

Next comes the output capacitor. It's role is to absorb all ac current ripple from the inductor and maintain the output voltage across the load to having less than 100 mV, pp.

$$i_c = C\frac{dV_c}{dt}$$
$$v_c = \frac{1}{C}\int i_c \, dt$$

From before I know my peak to peak inductor current is approximately 500 mA which shows up as a zero-centered triangle wave into my capacitor since I assume that all ac current goes into the capacitor and not my load. The area of this triangle above 0 is $\frac{T}{2} \cdot \frac{.5}{2} \cdot \frac{1}{2}$. Thus the minimum capacitance is:

$$\frac{T}{16C} < 0.1$$
$$C > 893 \; nF$$

Thus I chose a ceramic cap with a microFarad of capacitance rated for $25V_{dc}$, the first capacitor in the NTS ceramic chip capcitor series. Since it's a ceramic cap the ESR is insignificant so I will approximate it away.

Chapter 4

Input Filter

The purpose of the input filter is to ensure that the current ripple into the source is small enough to meet regulation, in this case 75 mA. To achieve this filtering I'll use an L section filter with a series inductor and parallel capacitor. In an AC model, our circuit is a inductor in parallel with a capacitor and a current source. This current source is a zero-centered square wave swinging between $\frac{I_L}{2}$ and $-\frac{I_L}{2}$. The fundamental component of this has amplitude $\frac{4}{\pi} I_L 2$ Which at full load is 5.303 A and peak to peak 10.606. Considering our filter has to turn that into 75 mA it must attenuate this fundamental by 21 dB. With this second order system we get attenuation of 40 dB per decade. Thus at minimum the resonance must be half a decade from the switching frequency but I'll choose it to be a full decade away from 700 kHz giving me a resonant frequency of $4.4 * 10^5$ rad/s. I will set L to be 100 nH. Thus my capacitor must be at least 51.6 μF. I'll use the 82 μF cap from the Panasonic OS-CON series rated for 35 V_{dc}. For the inductor I'll use a RM7 core with a gap of 800 μm and one turn. With this geometry, using the same calculations as for the output inductor, I find the max flux is 16 mT, well below the saturation flux density when carrying 10 A.

Chapter 5

Controls

For state space averaging we look at the state variables i_L and v_o.

$$\frac{di_L}{dt} = \frac{1}{L}q(t)(V_{IN} - v_o) + \frac{1}{L}(1 - q(t))(-v_o)$$
$$\frac{dv_o}{dt} = q(t)\frac{1}{C}(i_L - \frac{v_o}{R}) + (1 - q(t))\frac{1}{C}(i_L - \frac{v_o}{R})$$
$$\frac{dv_o}{dt} = \frac{1}{C}(i_L - \frac{v_o}{R})$$
$$\frac{di_L}{dt} = \frac{1}{L}q(t)V_{IN} - \frac{v_o}{L}$$

Then we average and make the assumption that the inductor current and output voltage ripple are small enough such that the product of them with the respective

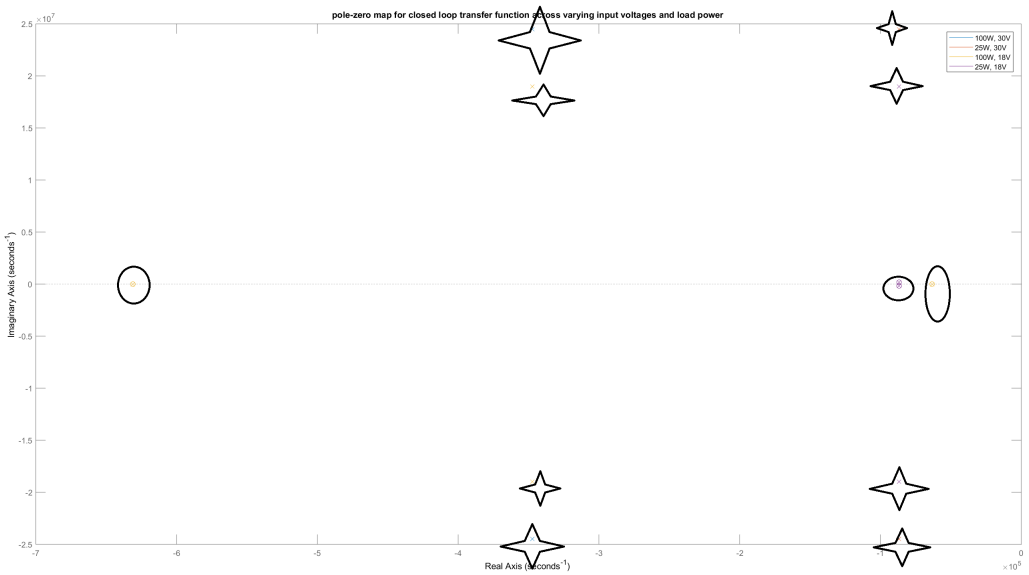
duty ratio variables is equal to the product of the averages.

$$\begin{aligned}
\frac{d\overline{v_o}}{dt} &= \frac{\overline{i_L}}{C} - \frac{\overline{v_o}}{RC} \\
\frac{d\overline{i_L}}{dt} &= d\frac{\overline{V_{IN}}}{L} - \frac{\overline{v_o}}{L} \\
\frac{d\overline{v_o}}{dt} &= \frac{\overline{i_L}}{C} - \frac{\overline{v_o}}{RC} \\
\frac{d\tilde{v_o}}{dt} &= \frac{I_L}{C} + \frac{\tilde{i_L}}{C} - \frac{V_o}{RC} - \frac{\tilde{v_o}}{RC} \\
\frac{I_L}{C} &= \frac{I_R}{C} = \frac{V_O}{RC} \\
\frac{d\tilde{v_o}}{dt} &= \frac{\tilde{i_L}}{C} - \frac{\tilde{v_o}}{RC} \\
\frac{d\overline{i_L}}{dt} &= d\frac{\overline{V_{IN}}}{L} - \frac{\overline{v_o}}{L} \\
\frac{d\tilde{i_L}}{dt} &= \frac{1}{L}(D+\tilde{d})(V_{IN}+\tilde{v_{in}}) - \frac{V_o}{L} - \frac{\tilde{v_o}}{L} \\
\frac{d\tilde{i_L}}{dt} &= \frac{1}{L}(DV_{IN} + D\tilde{v_{in}} + \tilde{d}V_{IN}) - \frac{V_o}{L} - \frac{\tilde{v_o}}{L} \\
V_o &= DV_{IN} \\
\frac{d\tilde{i_L}}{dt} &= \frac{D}{L}\tilde{v_{in}} + \frac{V_{IN}}{L}\tilde{d} - \frac{1}{L}\tilde{v_o}
\end{aligned}$$

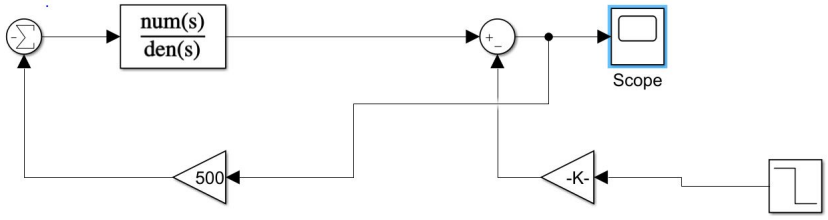
After finding these relationships I can then get a transfer function from perturbation in duty ratio to perturbtion in output voltage. Assuming no perturbation in input voltage:

$$\begin{aligned}
s\tilde{i_L} &= \frac{V_{IN}}{L}\tilde{d} - \frac{1}{L}\tilde{v_o} \\
s\tilde{v_o} &= \frac{1}{C}\tilde{i_L} - \frac{1}{RC}\tilde{v_o} \\
s\tilde{v_o} + \frac{1}{RC}\tilde{v_o} &= \frac{1}{sC}(\frac{V_{IN}}{L}\tilde{d} - \frac{1}{L}\tilde{v_o}) \\
\tilde{v_o}(s + \frac{1}{RC} + \frac{1}{sLC}) &= \frac{V_{IN}}{sLC}\tilde{d} \\
\frac{\tilde{v_o}}{\tilde{d}} &= \frac{V_{IN}}{s^2LC + \frac{sL}{R} + 1}
\end{aligned}$$

When designing my controller I have to ensure that it accomplishes two things, first that the system is stable with my compensator gain and doesn't violate the transient specification set. I decided to use a proportional controller with a gain of 500 to do this. After simulating in matlab I came up with the following pole-zero plot.



. This proved that my converter was stable as all of the poles were in the left half of the plane. For simulating the transient load step I used the following simulink simulation.



.

Where the transfer function box was the ratio of perturbations in duty cycle to perturbations in output voltage, the step is the current step changing from ≈ 2 A to ≈ 8 A and the gain block from the step is the impedence of the RLC trio. From this I found that my worse perturbation in output voltage during a transient was a power step down with a 30 V input. In this case the output voltage perturbtion maxed at 2 V which is just under the transient limit of 2.4 V.

Chapter 6

Simulation

To guarantee that my design met the specifications of the project I simulated my converter in LTSpice. The worse input current ripple occurs at the 18 V input voltage and 100 W a little below 70 mA. The worse output voltage ripple occurs at the 30 input voltage and 25 W load at 70 mV p-p, still below the upper limit of 100.

6.1 Waveforms

Below are the output voltage and input current waveforms associated with the boundary load and input voltage specifications.

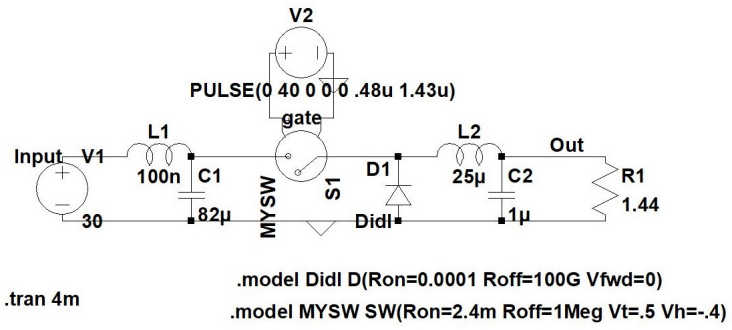


Figure 6.1: LTSpice Schematic

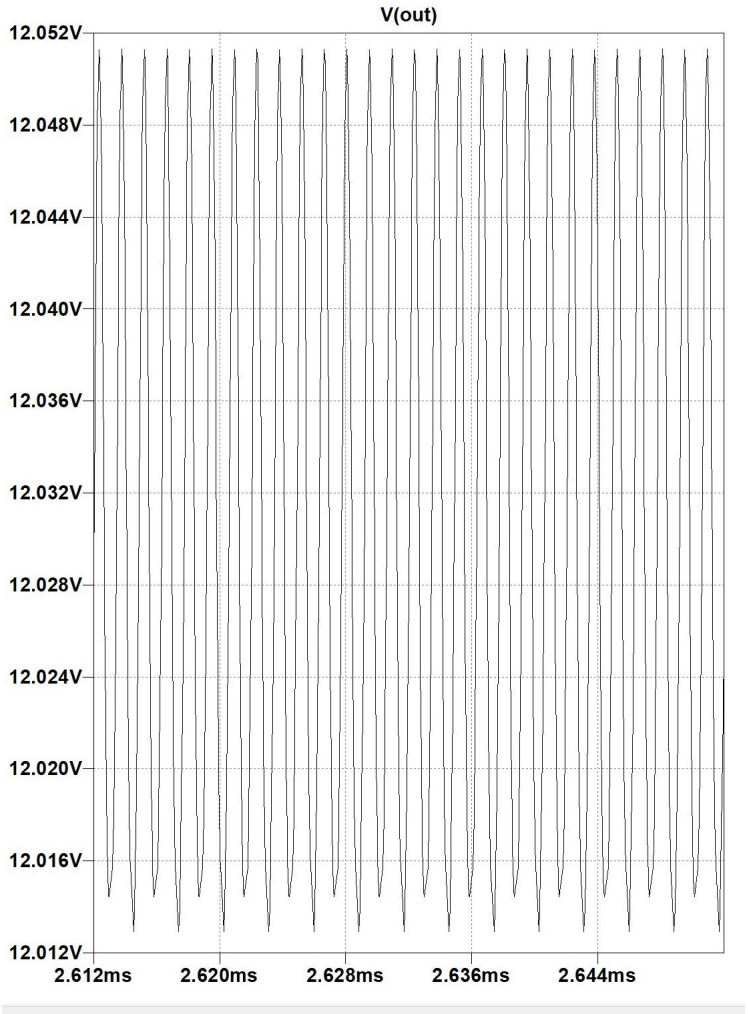


Figure 6.2: Output Voltage with 18 V input and 100 W load

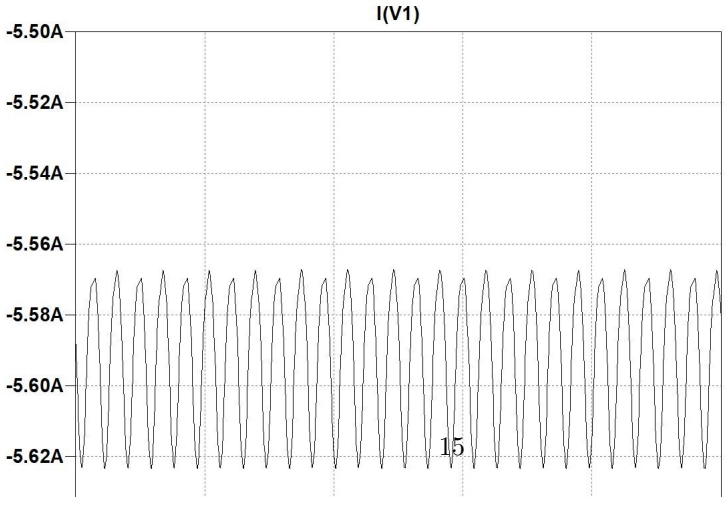


Figure 6.3: Input Current with 18 V input and 100 W load

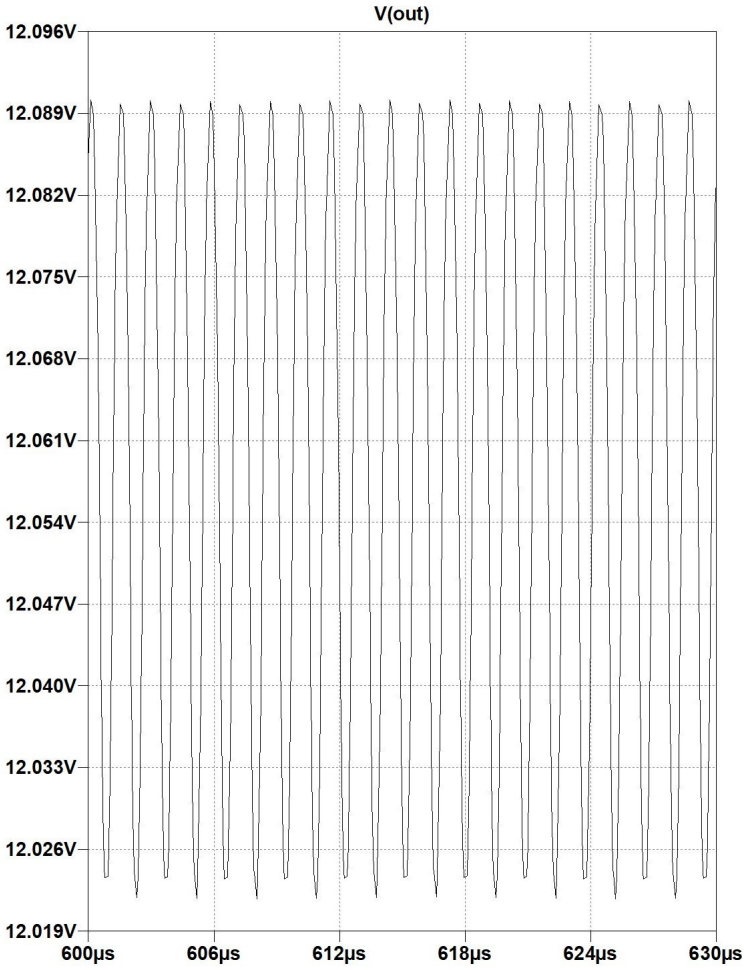


Figure 6.4: Output Voltage with 30 V input and 100 W load

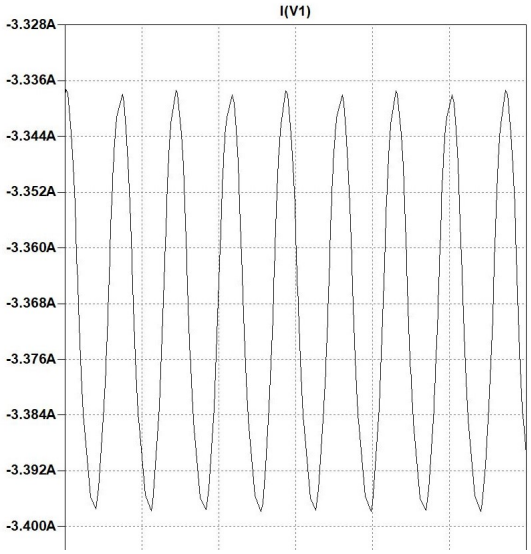


Figure 6.5: Input Current with 30 V input and 100 W load

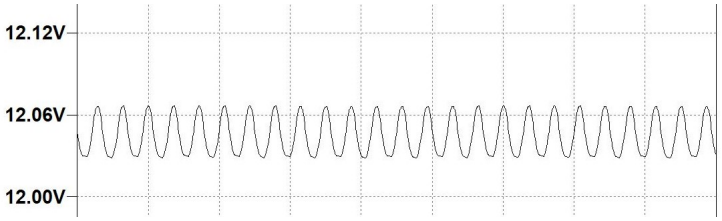


Figure 6.6: Output voltage with 18 V input and 25 W load

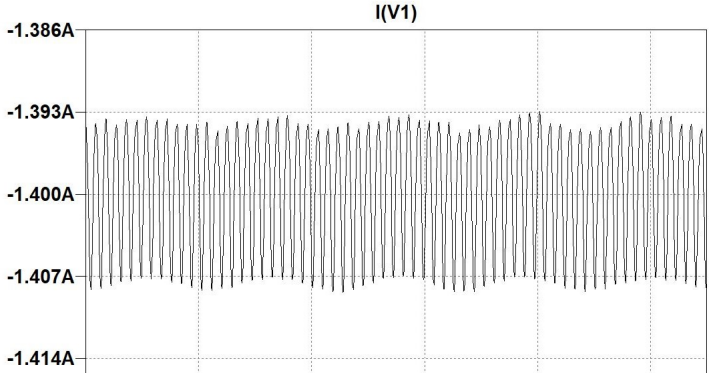


Figure 6.7: Input current with 18 V input and 25 W load

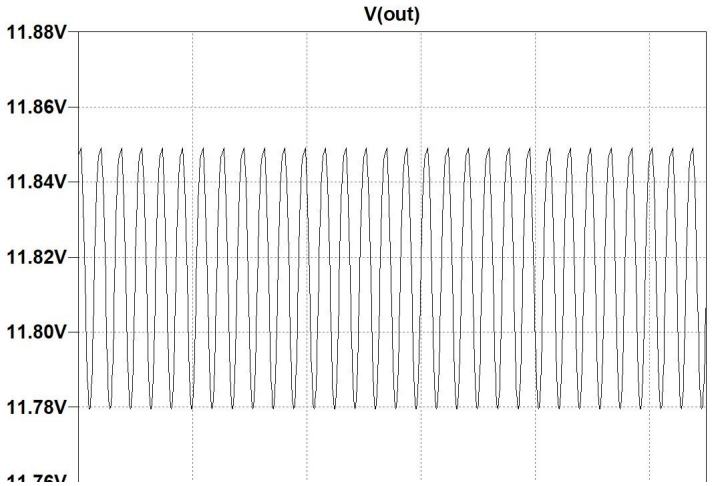


Figure 6.8: Output voltage with 30 V input and 25 W load

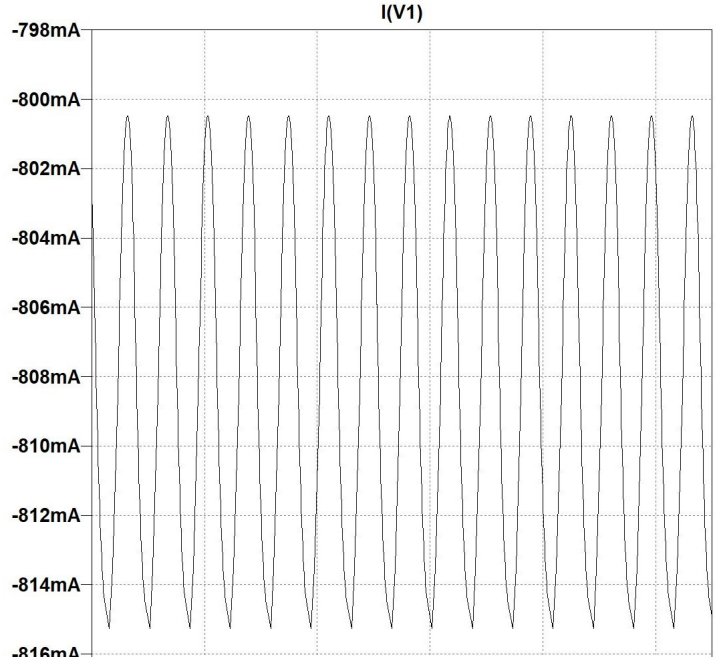


Figure 6.9: Input current with 30 V input and 25 W load

6.2 Efficiency

Finally using the same calculations to determine the switching frequency I can find the worse efficiency of the converter. This occurs at full load and the lowest input voltage because the fet switching loss dominates over the conduction loss.

$$\begin{aligned}
\eta = \frac{P_{out}}{P_{in}} &= \frac{P_{out}}{P_{out} + P_{burned}} \\
P_{burned} &= P_{FET,sw} + P_{FET,conduction} + P_{dide,conduction} \\
P_{out} &= 25\ W \\
V_{in} &= 30\ V \\
P_{burned} &= 2.48\ W \\
\eta_{min} &= 90.975\%
\end{aligned}$$