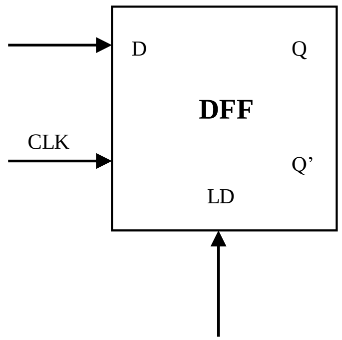
Design of a Sequence Detector Worked Example

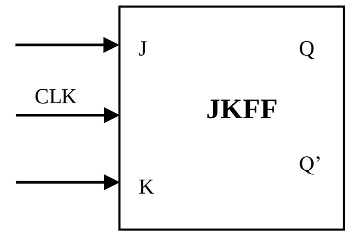
Implemented Using the Moore Machine Design Process

Flip-Flop Characteristic Equations

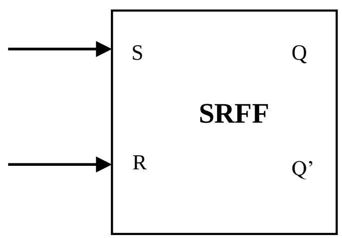
$Q^+ = D$



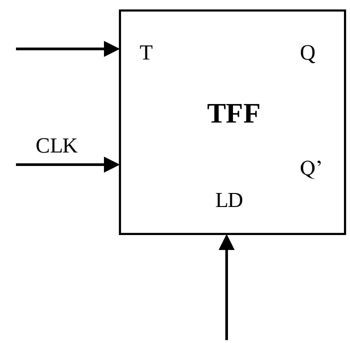
$Q^+ = JQ' + K'Q$



$Q^+ = S + R'Q$



$Q^+ = T \oplus Q$

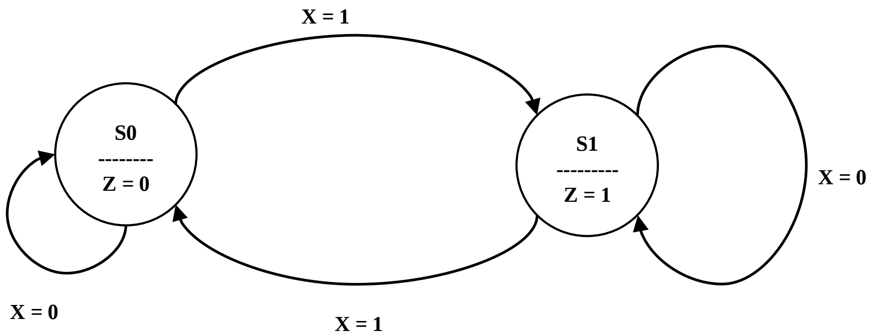


This is a reminder of the 4 types of flip-flops and their associated characteristic equations.

The Moore Machine

- The Moore machine was named after Edward Moore
- It has the characteristic of associating its outputs with the states
  - The outputs are represented within the vertex or in close proximity to the vertex

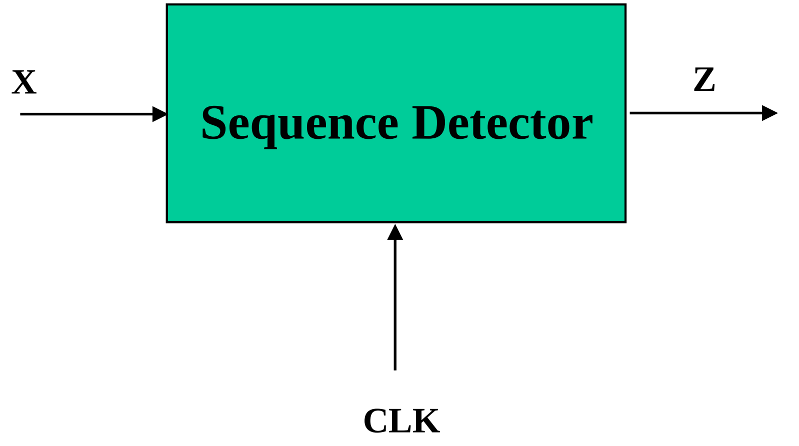
Moore Machine State Graph and State Table



Present State	Next State		Z
	X = 0	X = 1	
S0	S0	S1	0
S1	S1	S0	1

Notice the vertices. The state name is shown along with the output value Z. The Moore machine state graph is always represented in this fashion. Notice that the output Z is not dependent on the input X.

Macro View of the Sequence Detector



This sequence detector will be designed to recognize the pattern "1010". The behavior of the machine calls for the Z output to equal 1 whenever the programmed pattern is observed in the input bit stream X.

Example:

X = 0011011001010110

Z = 0000000000001000

Source: Fundamentals of Logic Design by Charles H. Roth

Design Strategy

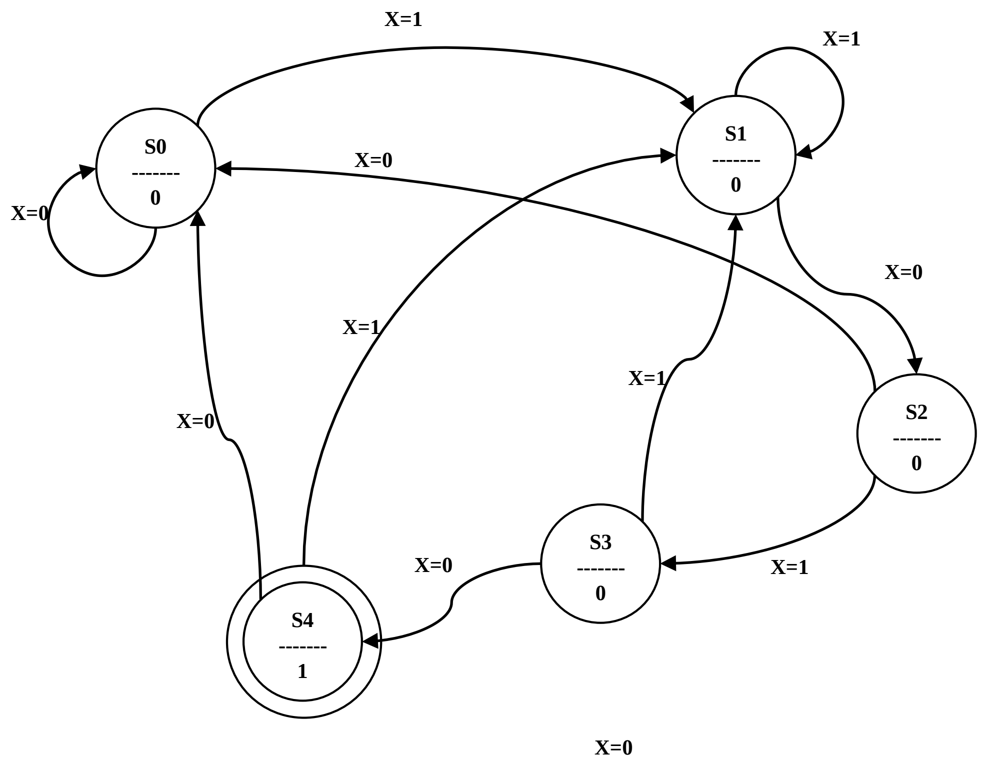
- For the design of the sequence detector, we will select the Moore machine model
- For this design, we will use the following process:
  1. Generate the state graph
  2. Create the state table
  3. Create the state transition table
  4. Generate the input expressions for the DFF
  5. Realize the final logic design

Generate the State Graph

LEGEND: **State**

Output Z

Pattern: 1010



Note: The Moore machine graph has one more state than the Mealy machine implementation. Since the output is represented within a state, an additional state must be created because it is the only state that can show an output of ‘1’ for this FSM.

Create the state table

Present State	Next State		Z
	X = 0	X = 1	
S0	S0	S1	0
S1	S2	S1	0
S2	S0	S3	0
S3	S4	S1	0
S4	S0	S1	1

Notice that the Moore machine model has an output value Z that is not dependent on the value of X.

Create the State Transition Table

State Table

Present State	Next State		Z
	X = 0	X = 1	
S0	S0	S1	0
S1	S2	S1	0
S2	S0	S3	0
S3	S4	S1	0
S4	S0	S1	1

Let S0 = 000

S1 = 001

S2 = 010

S3 = 011

S4 = 100

State Transition Table

Present State	Next State		Z
	X = 0	X = 1	
000	000	001	0
001	010	001	0
010	000	011	0
011	100	001	0
100	000	001	1

Generate the Input Expressions for the DFF

Present State	**Next State**		**Z**
	X = 0	**X = 1**	
000	000	001	0
001	010	001	0
010	000	011	0
011	100	001	0
100	000	001	1

$D_{A\text{-Map}}$

BC \ XA	00	01	11	10
00	0	0	0	0
01	0	X	X	0
11	1	X	X	0
10	0	X	X	0

$D_A = X'BC$

$D_{B\text{-Map}}$

BC \ XA	00	01	11	10
00	0	0	0	0
01	1	X	X	0
11	1	X	X	0
10	0	X	X	1

$D_B = X'C + XBC'$

$D_{C\text{-Map}}$

BC \ XA	00	01	11	10
00	0	0	1	1
01	0	X	X	1
11	0	X	X	1
10	0	X	X	1

$D_C = X$

$Z_{\text{-Map}}$

BC \ XA	00	01	11	10
00	0	1	1	0
01	0	X	X	0
11	0	X	X	0
10	0	X	X	0

$Z = A$

Realize the final logic design