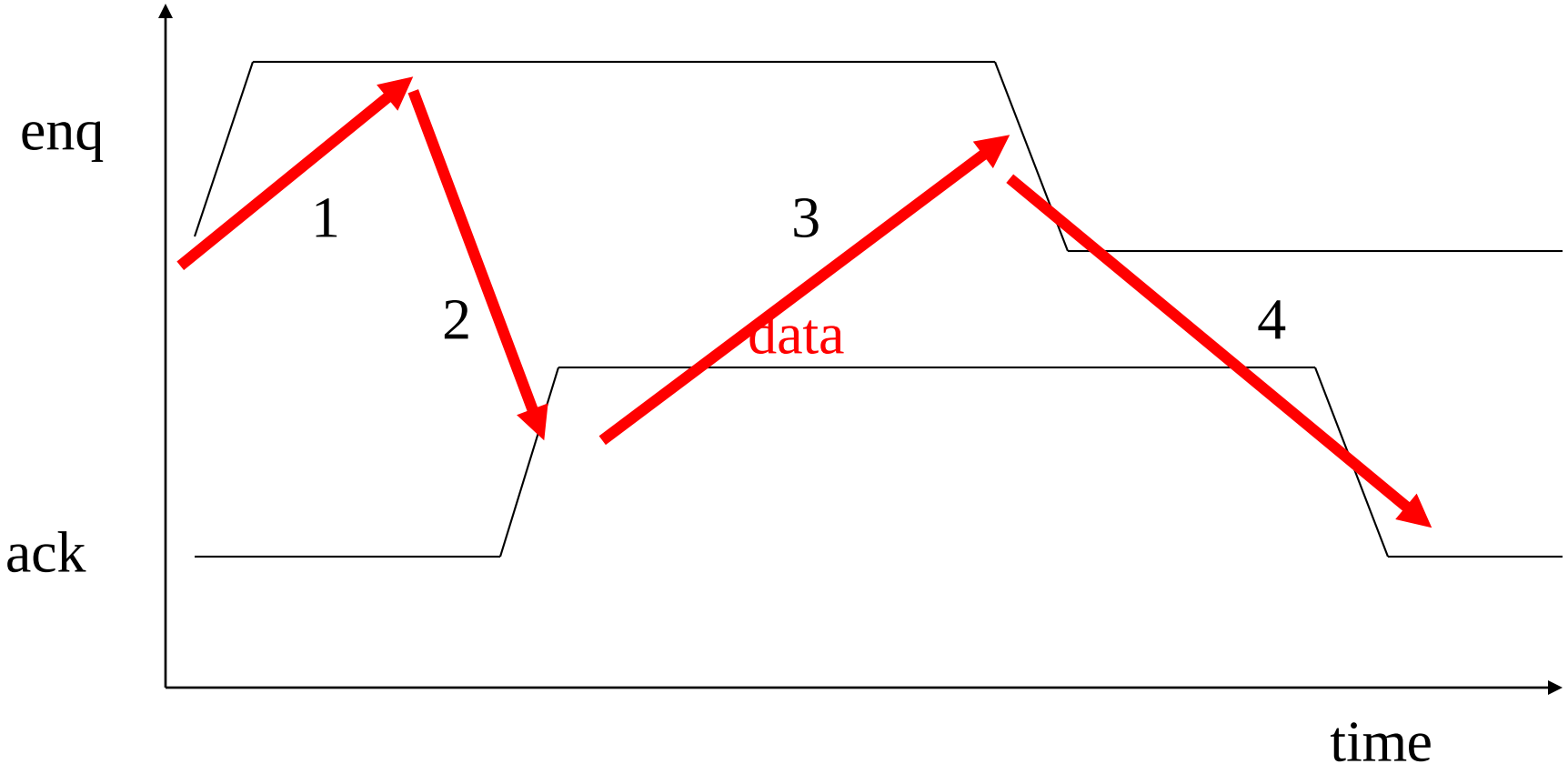
Timing Diagram w/Handshake

Example is an excerpt from the book: Computers as Components by Wolf

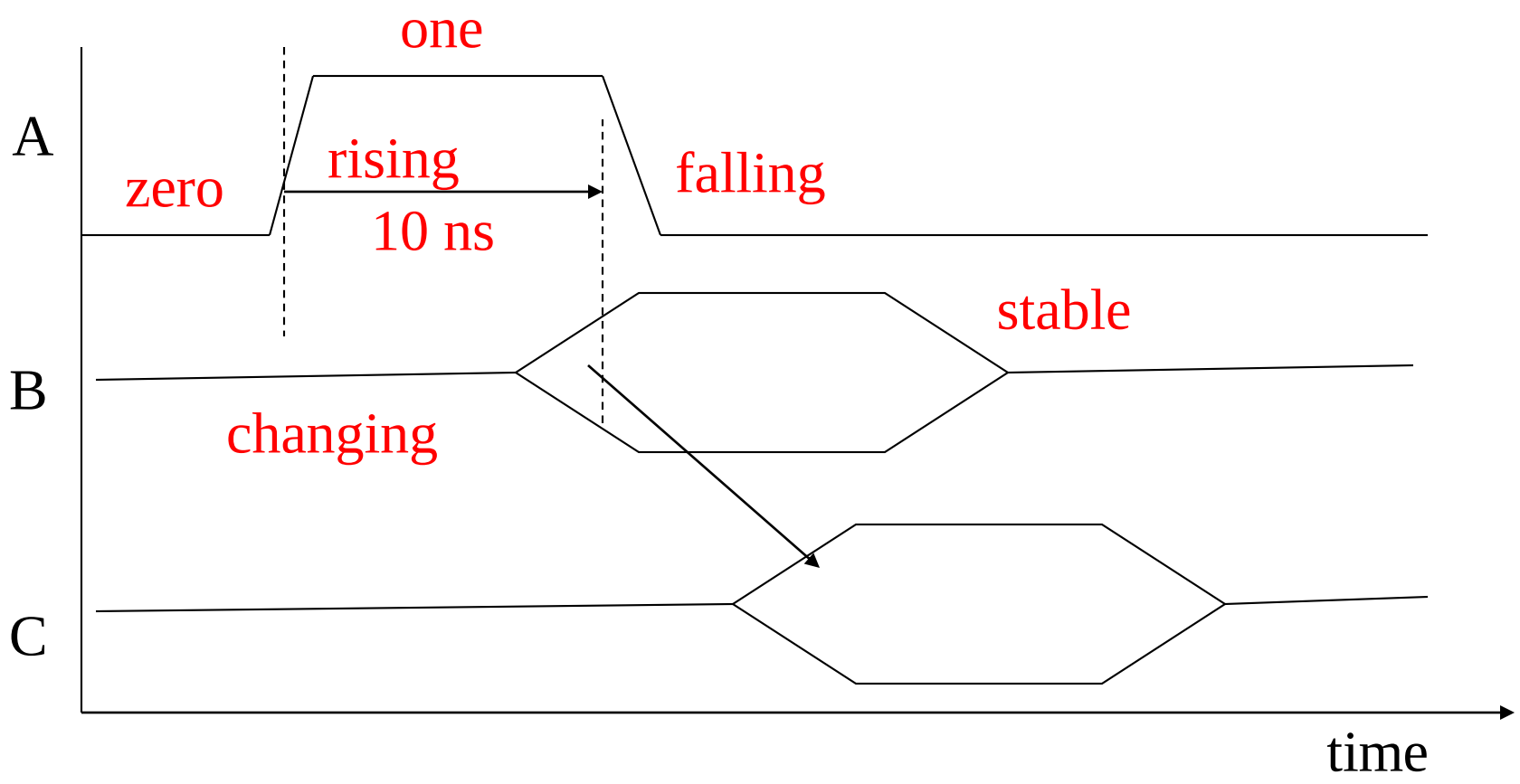
Four-cycle example



Typical bus signals

- Clock.
- R/W’: true when bus is reading.
- Address: a-bit bundle.
- Data: n-bit bundle.
- Data ready’.

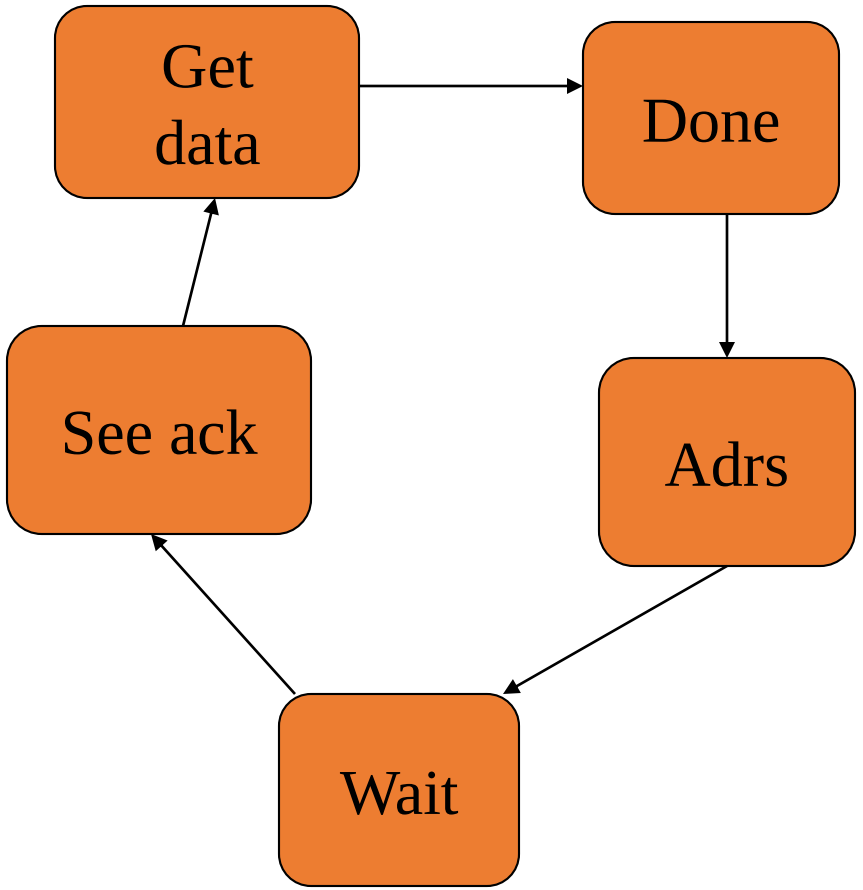
Timing diagrams



Typical bus timing for read

- CPU:
  - set R/W’=1;
  - asserts address, address enable.
- Memory:
  - asserts data;
  - asserts data ready’.
- CPU:
  - deasserts address, address enable.

Bus read state diagram



CPU asserts address here!

Wait State

- Wait state:
  - state in a bus transaction to wait for acknowledgment.
  - This is typical in systems where the CPU runs at much higher speed that the memory sub-system or other devices in the system

Transaction types

- Wait state:
  - state in a bus transaction to wait for acknowledgment.
- Burst:
  - multiple transfers.