

today: ☐ logistics: HW1 due Fri Oct 15  
HW2 due Fri Oct 22

☐ group work

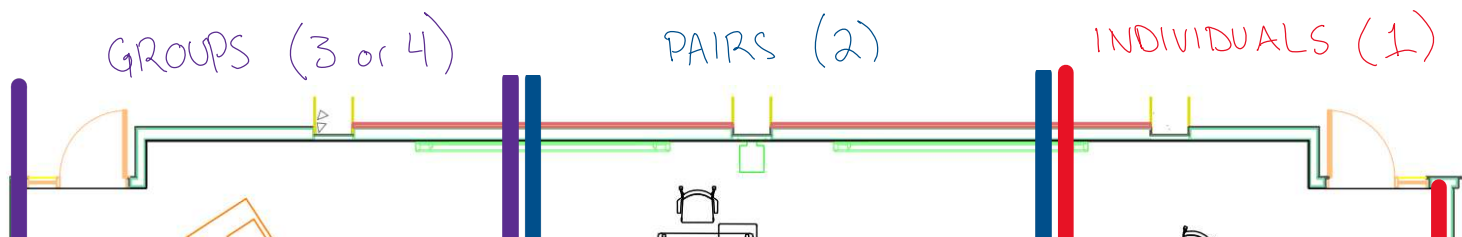
☐ break

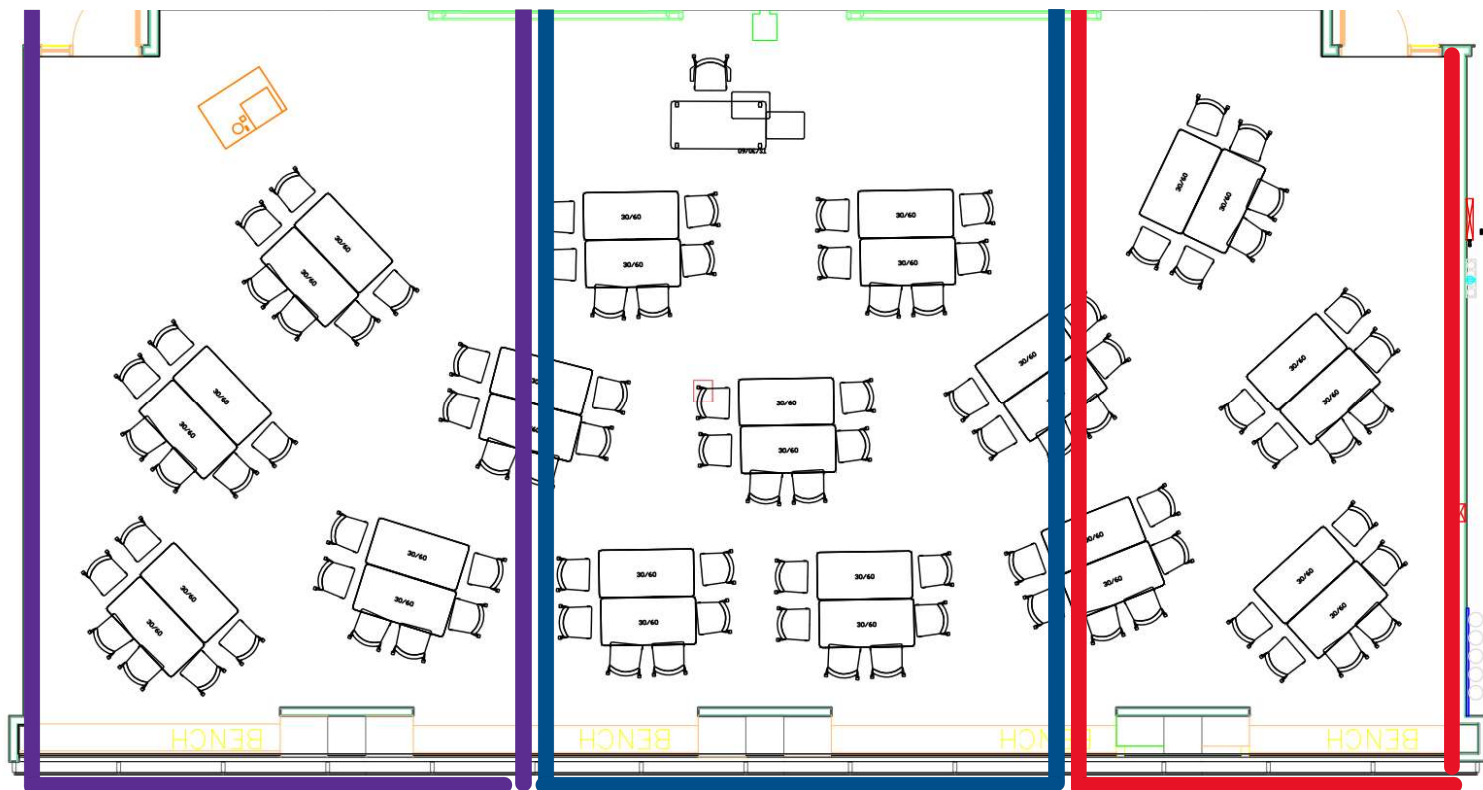
☐ office hour

Prof Burden TODO: ☒ enable participant screen sharing  
☒ advertise TA OH (currently virtual)  
☒ clarify  $y_2$  in HW/p39  
☒ pdf or ipynb both OK

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group work





## 1. RLC circuit interconnection

Consider the model of a series RLC circuit from lecture,

$$L\ddot{q} + R\dot{q} + q/C = v,$$

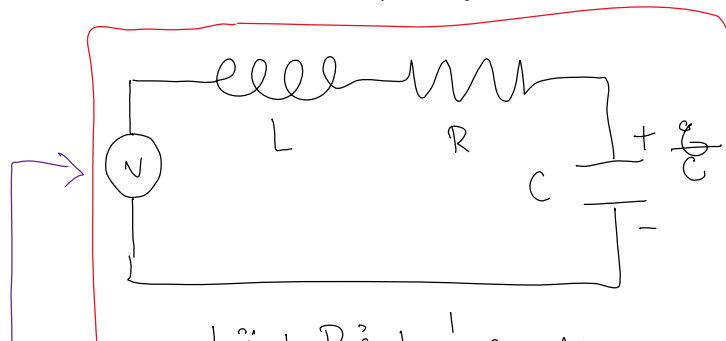
where  $q$  denotes the charge on the capacitor,  $(R, L, C)$  denote the (resistor, inductor, capacitor) parameters, and  $v$  denotes a series voltage source.

Now suppose that the input voltage  $v$  to the circuit above is actually the output from a second series RLC circuit

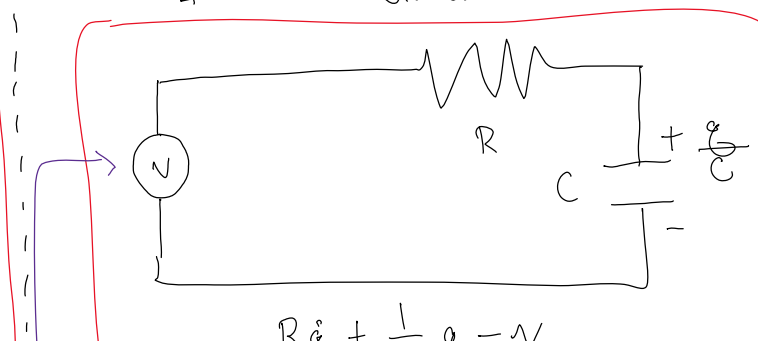
$$L_2 C_2 \ddot{v} + R_2 C_2 \dot{v} + v = w,$$

where  $v$  denotes the voltage across the second circuit's capacitor,  $(R_2, L_2, C_2)$  denote the second circuit's (resistor, inductor, capacitor) parameters, and  $w$  denotes a series voltage source for the second circuit.

2nd-order circuits:

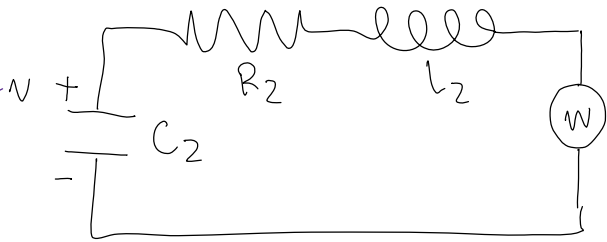


1st-order circuits



$$L\ddot{q} + R\dot{q} + \frac{1}{C}q = v$$

$$L_2 C_2 \ddot{v} + R_2 C_2 \dot{v} + v = w$$



$$R\dot{q} + \frac{1}{C}q = v$$

$$R_2 C_2 \dot{v} + v = w$$

