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SENAI CIMATEC
Supercomputing Center

Accelerating 3D Seismic Modeling with Alveo FPGA

Sistema FIEB | SENAI CIMATEC

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Brazilian Research and Development Institute

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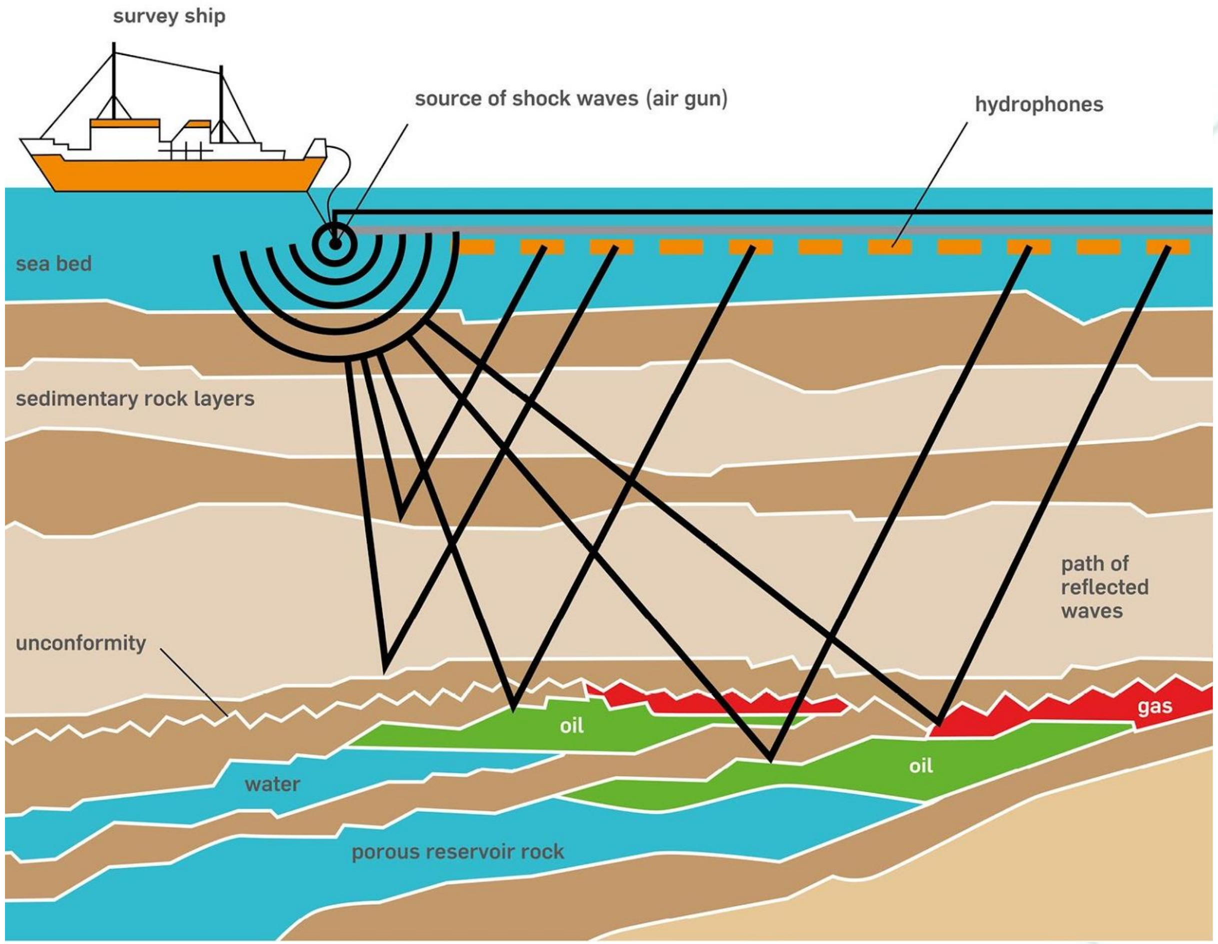
Contents:

Seismic Inversion: Subsurface Imaging with RTM

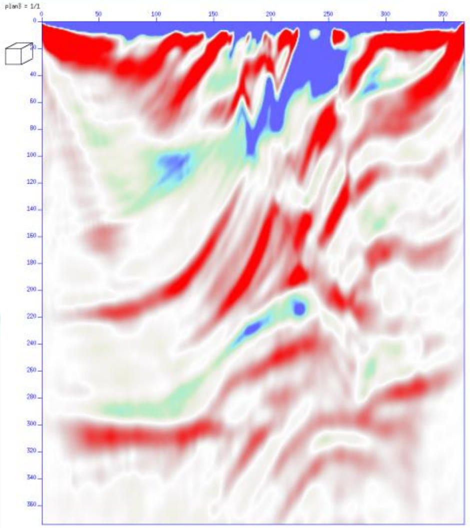
- **Seismic Inversion** is a set of techniques used to create an image of the subsurface from field recorded data;

- **RTM** is a diversified class of algorithms used in seismic inversion processes. It relies on two known parameters:
  - ***Field data*** - or also called recorded data. This is a shot record corresponding to the true velocity model collected in field during Seismic Survey;
  - ***Background velocity model*** - This is a velocity model that has been obtained by processing and inverting the field data. This velocity model is usually a smooth version of the true velocity model.

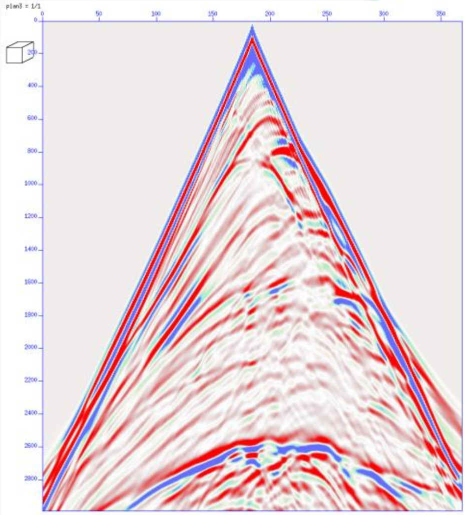


Seismic Inversion: Subsurface Imaging with RTM

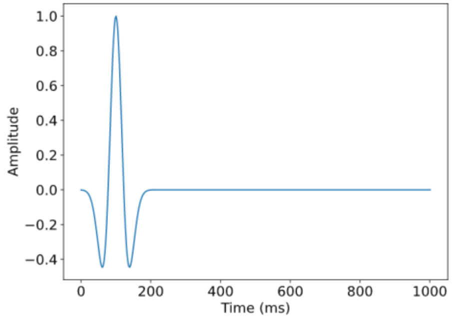
Smooth Velocity Model



Seismic Shot Record

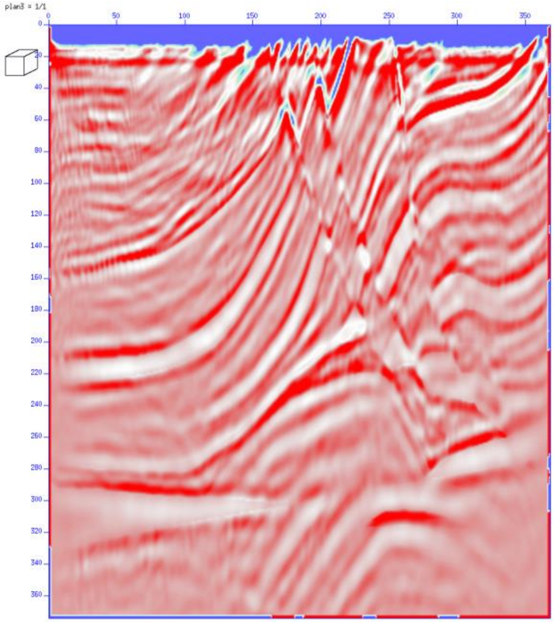


RTM Imaging



Shot Signature

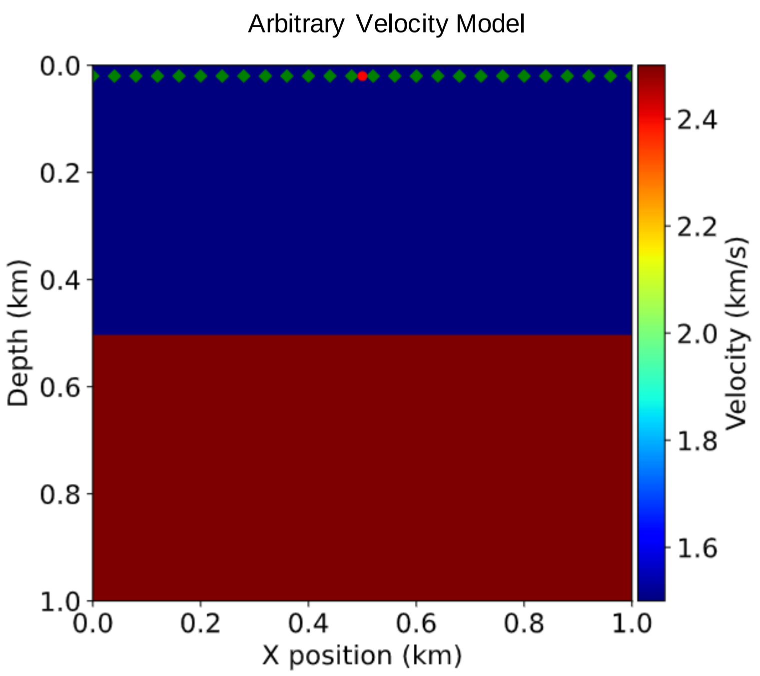
Enhanced Velocity Model



- Compute intensive PDE solver;
- Memory Bound stencil operators;
- Requires large quantities of memory;
- Time Dependent Domain Partitioning;

Seismic Modeling: Generating Synthetic Shot Records

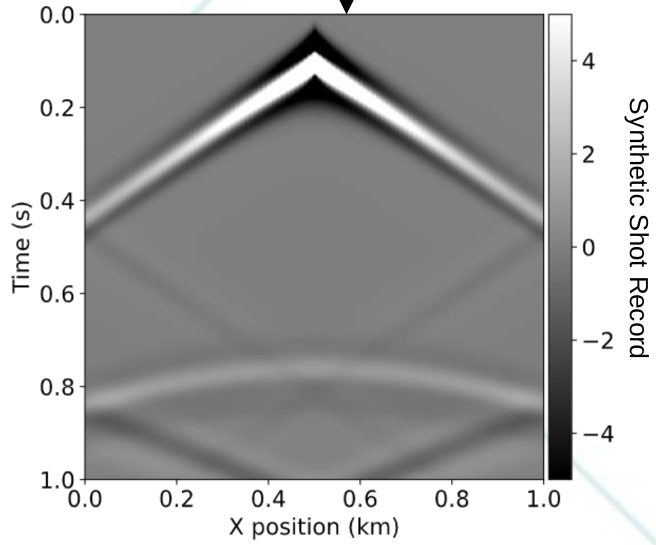
- Fine-tunning of RTM implementations require the ability to experiment on:
  - Different acquisition geometries;
  - Multiple source signatures parameters (Peak frequency, number of time steps, source position, etc.)
  - Multiple boundary absorbing conditions;
- Real world shot records are expensive and hard to acquire;
- They are also tied to the specific **acquisition geometry** used in the field;
- **Synthetic Shot Records** are an essential part of the RTM prototyping process;
- They can be used to validate RTM flow and fine-tunning adjustments;



Seismic receivers distributed across the X direction;

Seismic shot positioned at the top-center position;

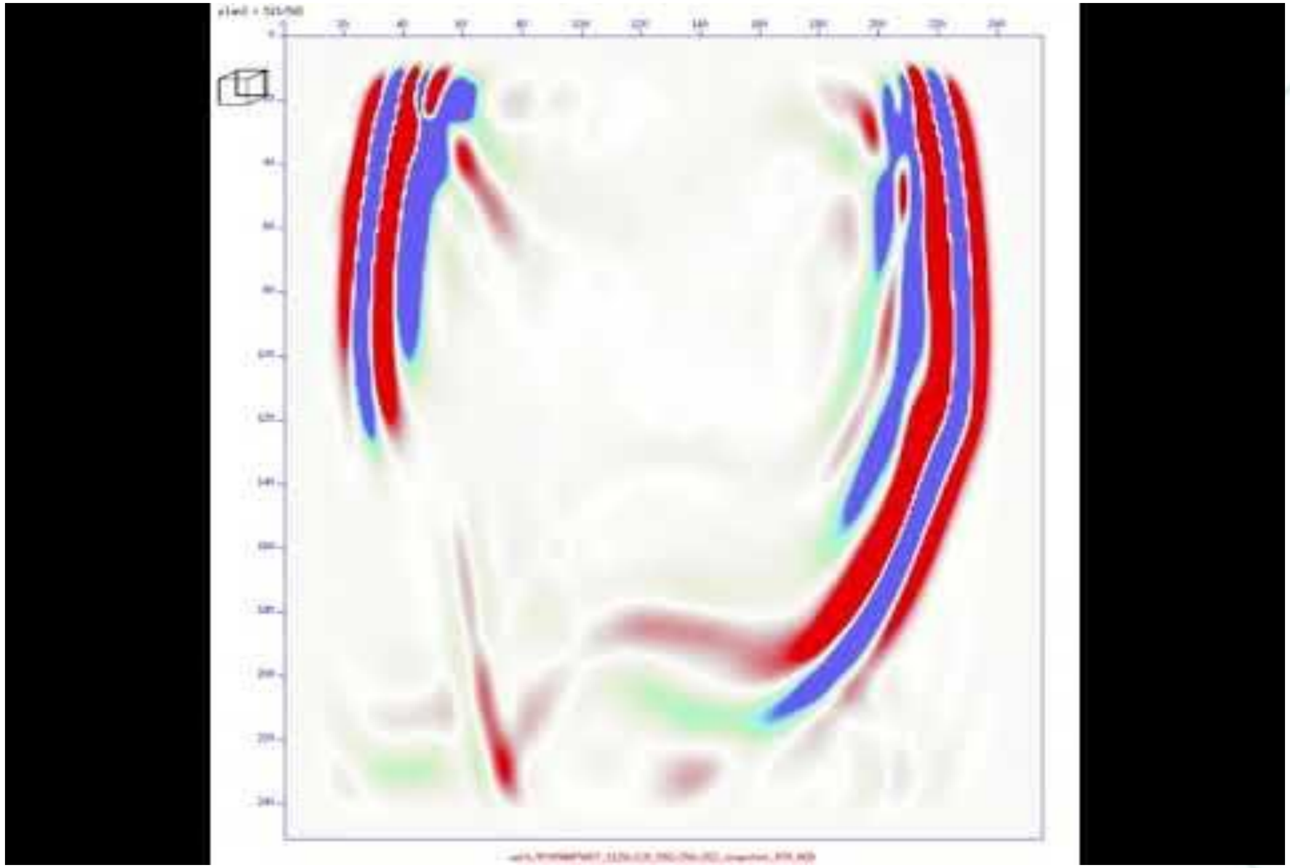
Time-Forward Source Wave Propagation



Seismic Modeling: Generating Synthetic Shot Records

- **The time-forward propagation** is the simulation of the source wave propagation across the input velocity model;
- It generates the source wavefield snapshots that are then used in the cross-correlation with the reconstructed Shot Record wavefield (time-backward propagation);
- It is part of most RTM implementations normally corresponding to **40% of the execution time**;
- The Seismic Modeling process consists of a time-forward propagation where wave values are recorded at given acquisition geometry points;

Time-Forward Source Wave Propagation

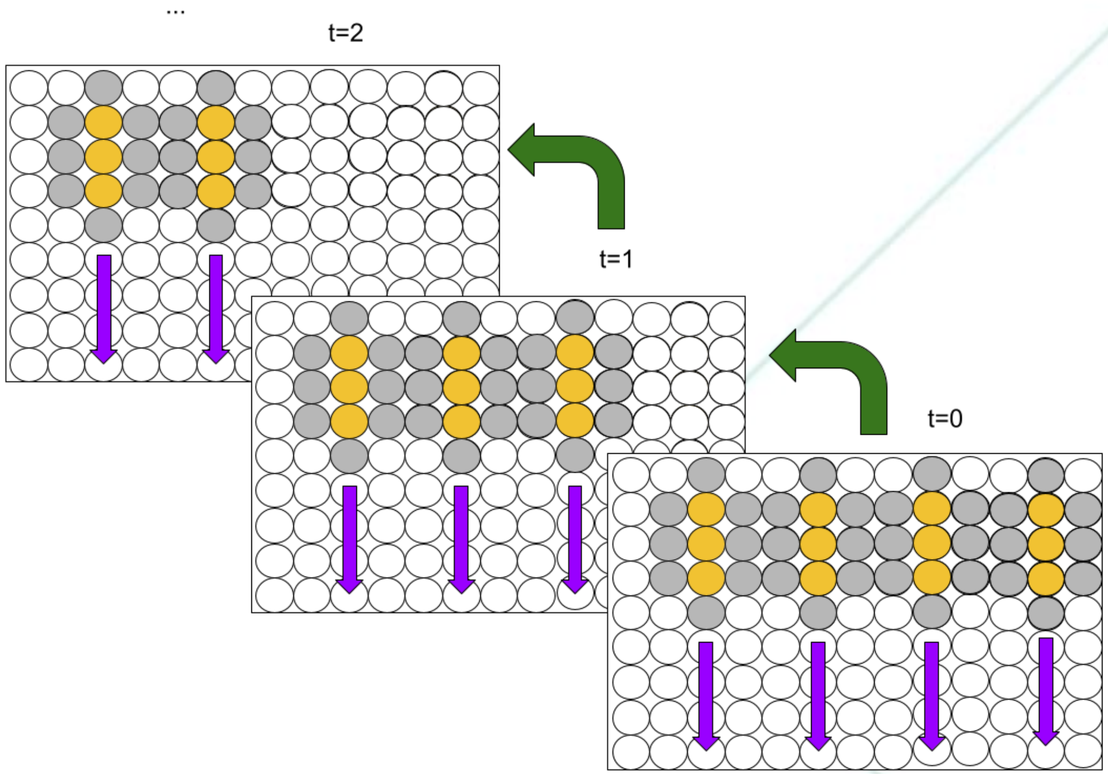


Seismic Modeling: Generating Synthetic Shot Records

- **The time-forward propagation** implements a PDE solver of the acoustic wave equation to compute pressure fields across multiple time steps (duration);
- A discrete solution of the Acoustic Wave Equation can be expressed as:

$$P[\ t{+}1\ ] = 2P[\ t\ ] - P[\ t{-}1\ ] + c^2\ L\ \Delta t^2$$

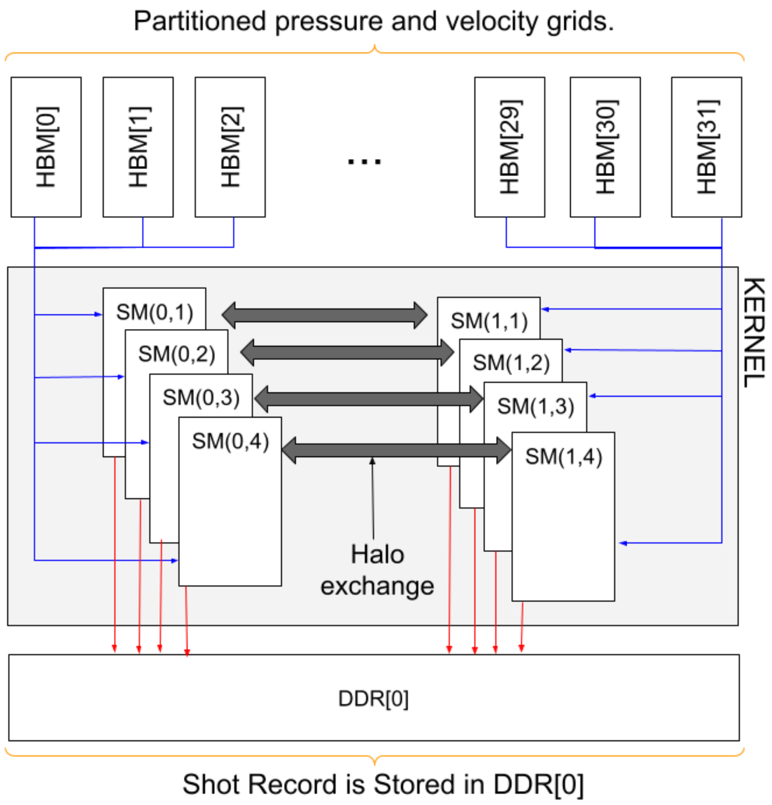
  - 2nd order in time;
  - n-th order in space;
- Two opportunities for parallelism:
  - **Spatial parallelism**: multiple points can be updated within the same time step;
  - **Temporal parallelism**: as soon as a point is updated, it can be used as input for the next time step (Pipelining);



- **Great opportunity for hardware-based acceleration!**

Seismic Modeling: FPGA Implementation

- Using Alveo U280, we have developed an FPGA-based accelerator that computes the time-forward propagation across a 3D velocity model;
- Our architecture can be used to accelerate the 3D Seismic Modeling and the RTM Forward Propagation processes;
- Features:
  - C++ implementation (no Verilog);
  - PCIe based transfers between host program and the accelerator (just like GPUs);
  - Significant power efficiency when compared to GPUs and CPUs;



Seismic Modeling: FPGA Implementation

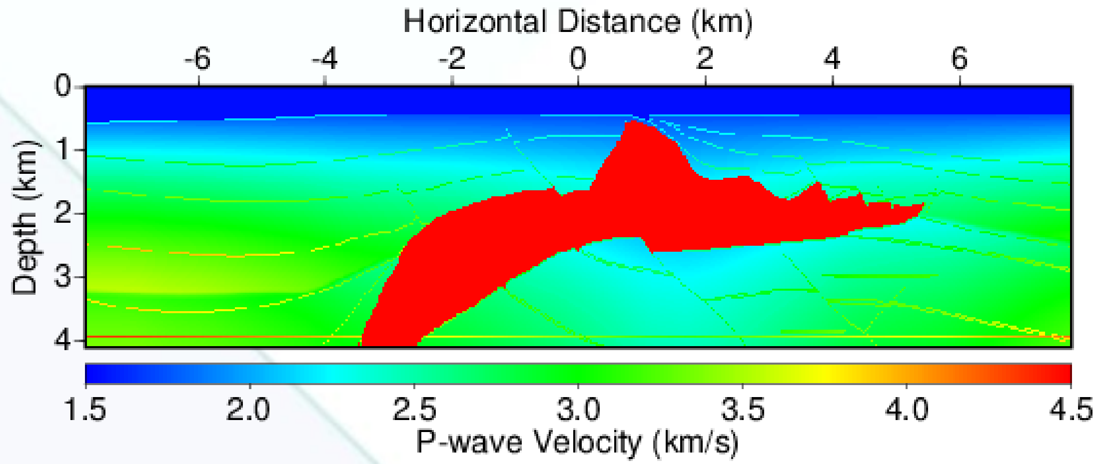
FPGA Kernel Resource Utilization

Resource	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-		-	
Expression	-	-	0	3088	
FIFO	-	-	-	-	
Instance	804	2081	309914	182669	200
Local Memory	0	-	896	48	
Multiplexer	-	-	-	1938	
Register	-	-	7115	352	
Total	804	2081	317925	188095	200
Available on SRL0	1344	3008	869120	434560	320
Utilization on SLR0 (%)	**59**	**69**	**36**	**43**	**62**
Available on U280 FPGA	4032	9024	2607360	1303680	960
Utilization (%)	**19**	**23**	**12**	**14**	**20**

U280 Available Memory

Type		Total
Global	DDR4	2x16GB (32GB)
	HBM2	8GB
Local	Block RAM	4032
	UltraRAM	960

Seismic Modeling: FPGA vs. CPU Performance Comparison



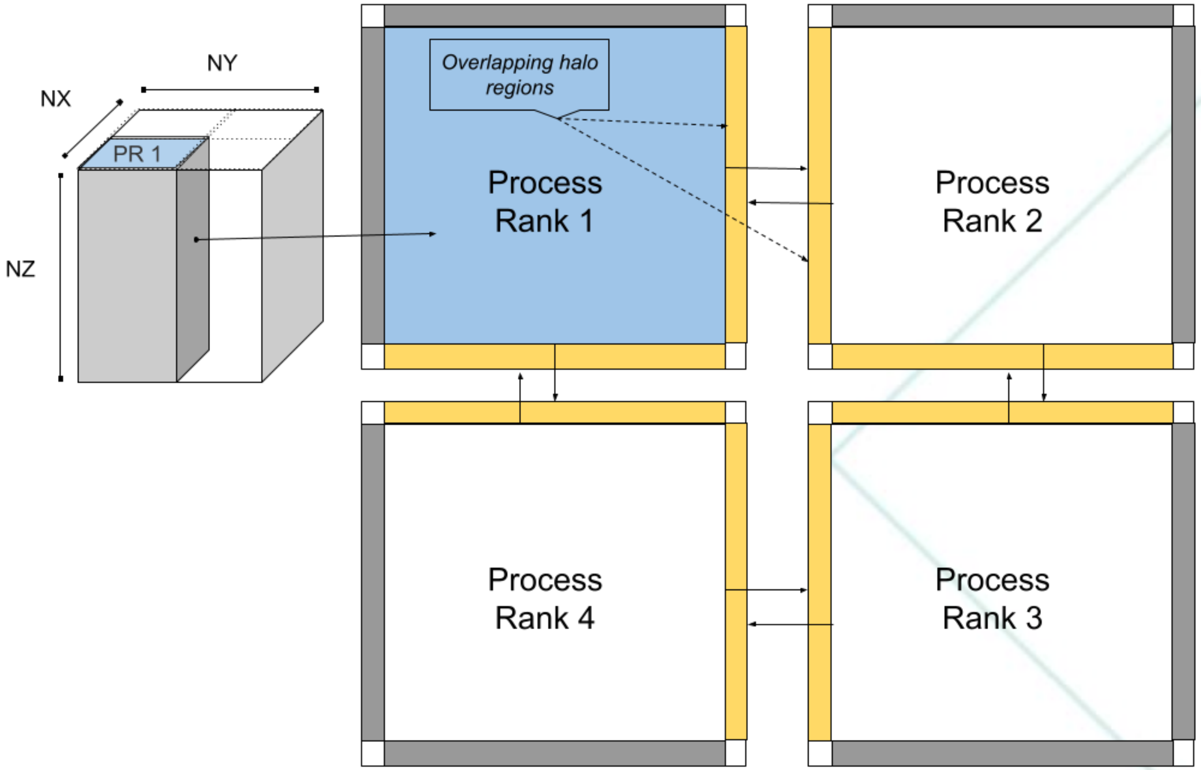
Input Velocity Model	
Name	SEG/EAGE 3D Salt Model
Grid	676x676x210
(dx,dy,dz)	(20,20,20)
dt	0.00085
Size (km)	13.52x13.52x4.2
Duration (s)	2.8
Time steps	3300
Virtual Border	21
Shot Record (MB)	6032.08
Grid Size (MB)	3x520 (1560)
Required Memory (MB)	7600

	CPU-Node	
16x	Architecture	x86_64
	CPU(s)	72
	On-line CPU	0-71
	Threads	2
	Cores	18
	Socket(s)	2
	CPU family	6
	Model	85
	Model name	Intel(R) Xeon(R) Gold 6240 CPU @ 2.60GHz
	L1d cache	32K
	L1i cache	32K
	L2 cache	1024K
	L3 cache	25344K
	Interconnect	InfiniBand
	RAM (GB)	376
	Distributed FS	Lustre

Seismic Modeling: FPGA vs. CPU Performance Comparison

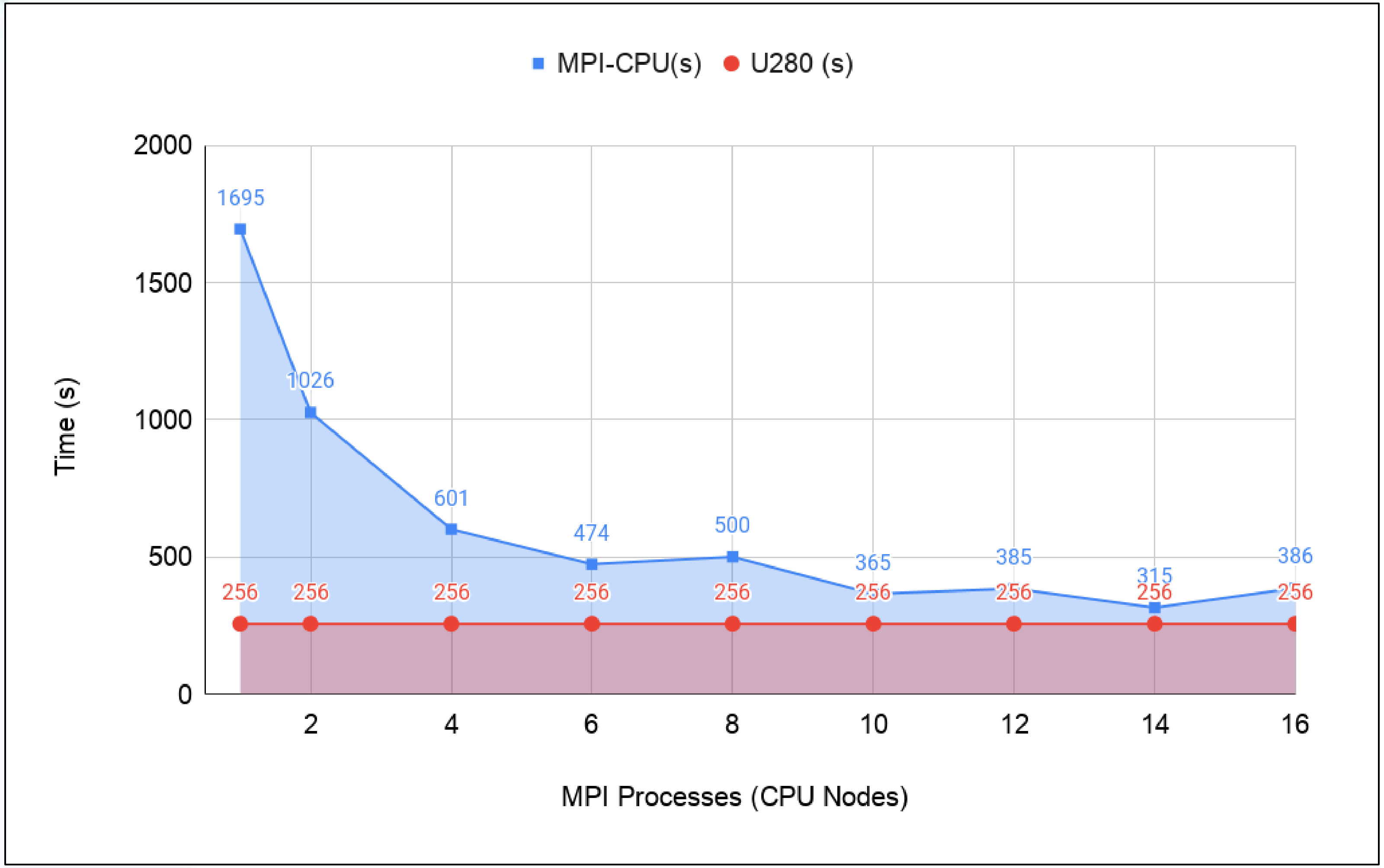
- 1 MPI-Rank per CPU-Node (up to 16 nodes), 72 threads per rank;
- We recorded the time it took to generate a Shot Record both on CPU and FPGA-accelerated implementations;
- FPGA-time includes Host time as well;
- Stencil computation requires halo-regions to be synchronized at every time step, which is bed for small volumes;
- Both FPGA and CPU outputs were compared for validation;
- Number of shots: 1;

Domain Partitioning Strategy for MPI-based CPU

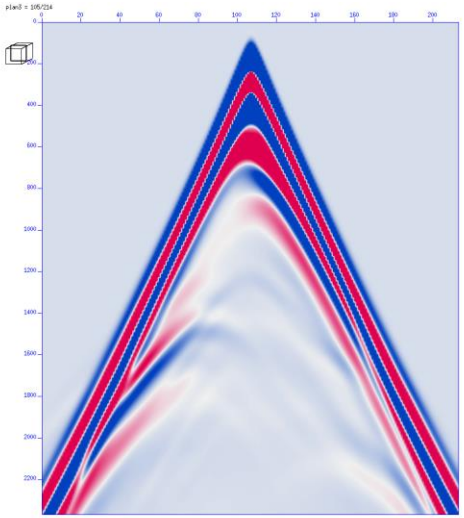


Seismic Modeling: FPGA vs. CPU Performance Comparison

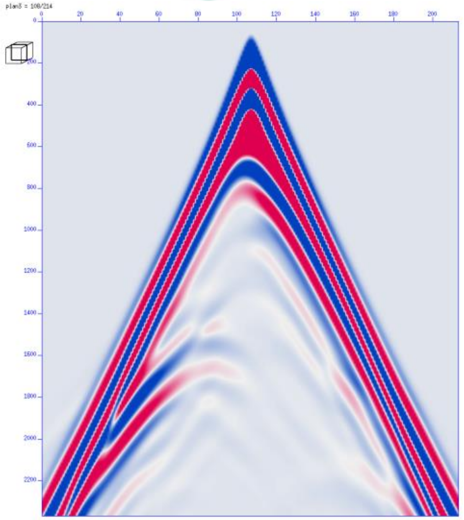
Seismic Modeling Time:



Output Synthetic Shot Records:



Alveo U280



CPU

Seismic Modeling: Final Considerations

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- Results have shown that a single U280 FPGA board can provide performance superior to 16 CPU nodes for 3D Seismic Modeling;
- Equivalent performance results can be expected for a full 3D-RTM implementation;
- Future improvements may include:
  - Include Time-Backward and Image Condition kernels for full RTM implementation;
  - Domain partitioning with direct network communication between FPGAs;

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