Good Display	SPECIFICATIONS	SPEC NO	
	GDEW0213T1	REV NO	

Good Display Specifications

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Good Display

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Revision History

Rev.	Issued Date	Revised Contents
1.0	Jan.12.2014	Preliminary
1.1	Apr.08.2014	1. Modify the specification's name
1.2	Apr.16.2014	1. In part 4: Modify Mechanical Drawing of EPD module.
1.3	Jun.12.2014	1. In part 4: Modify Mechanical Drawing of EPD module.
1.4	Jul.01.2014	1. In part 9-2): Add program code. 2. In part 2: Modify Low current deep sleep mode to Low current sleep mode 3. In part 74-1): Delete oscillator frequency. 4. In part 7-4-2): Modify timing characteristics of serial interface. 5. In part 5-1): Modify pin VPP to NC.
1.5	Jul.28.2014	1. Modify the specification's name
1.6	Nov.18.2014	1. In part 15：Modify Reliability test.
1.7	Jan.04.2015	1. In part 4: Modify Mechanical Drawing of EPD module.

TECHNICAL SPECIFICATION

CONTENTS

1. Over View

The display is a TFT active matrix electrophoretic display, with interface and a reference system design. The 2.13" active area contains 212×104 pixels, and has 1-bit full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

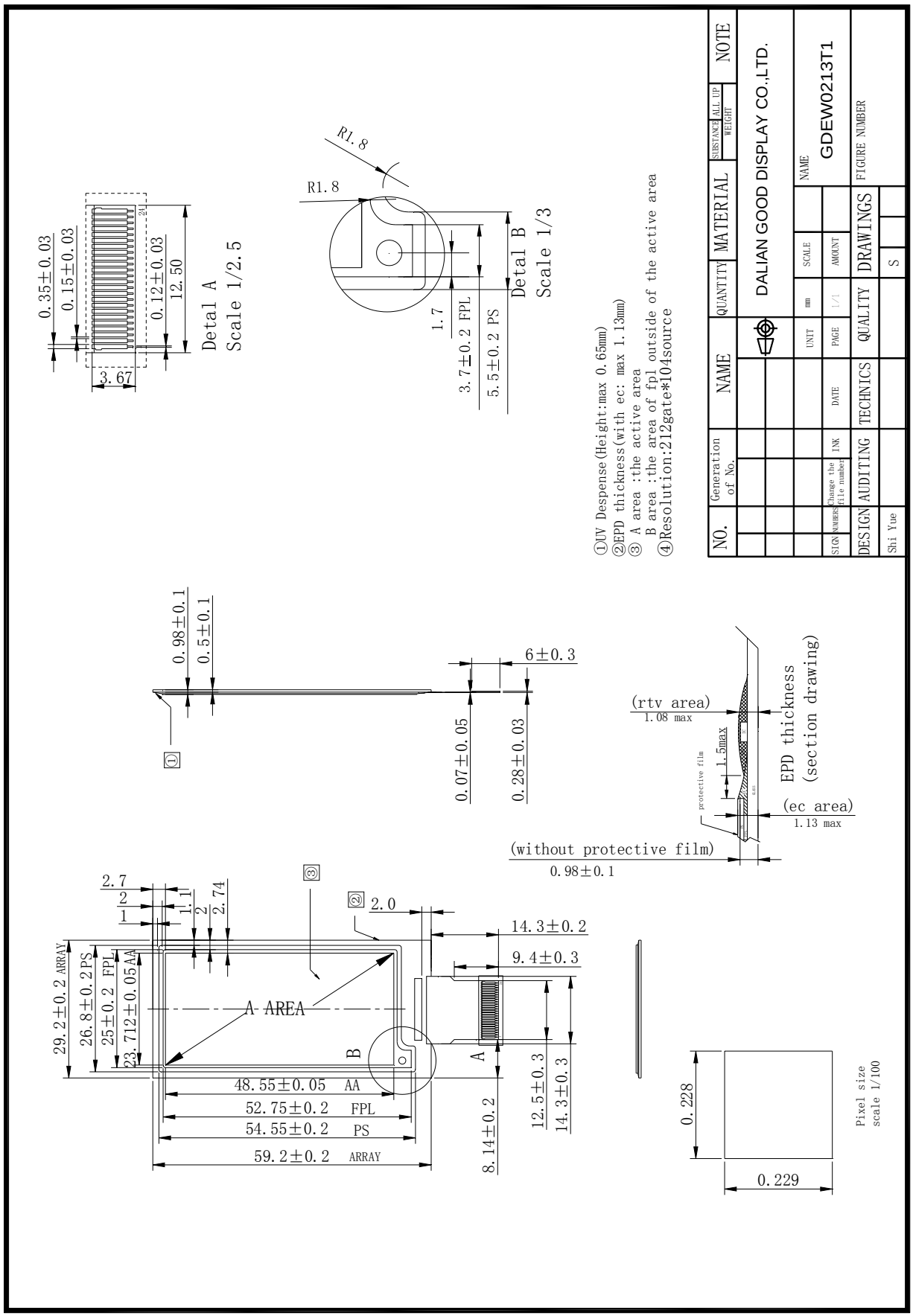
2. Features

- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current sleep mode
- On chip display RAM
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and source driving voltage
- I^2C Signal Master Interface to read external temperature sensor
- Available in COG package IC thickness 300um

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.13	Inch	
Display Resolution	212 (H)×104 (V)	Pixel	Dpi:111
Active Area	48.55 (H)×23.71(V)	mm	
Pixel Pitch	0.229×0.228	mm	
Pixel Configuration	Rectangle		
Outline Dimension	59.2 (H)×29.2 (V) ×0.98(D)	mm	
Weight	3.36±0.5	g	

4. Mechanical Drawing of EPD module



5. Input/Output Terminals

5-1) Pin out List

Pin #	Type	Single	Description	Remark
1		NC	No connection and do not connect with other NC pins	Keep Open
2	O	GDR	N-Channel MOSFET Gate Drive Control	
3	O	RESE	Current Sense Input for the Control Loop	
4	C	VGL	Negative Gate driving voltage	
5	C	VGH	Positive Gate driving voltage	
6	O	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	I/O	TSDA	I2C Interface to digital temperature sensor Date pin	
8	I	BS1	Bus selection pin	Note 5-5
9	O	BUSY	Busy state output pin	Note 5-4
10	I	RES #	Reset	Note 5-3
11	I	D/C #	Data /Command control pin	Note 5-2
12	I	CS #	Chip Select input pin	Note 5-1
13	I/O	D0	serial clock pin (SPI)	
14	I/O	D1	serial data pin (SPI)	
15	I	VDDIO	Power for interface logic pins	
16	I	VCI	Power Supply pin for the chip	
17		VSS	Ground	
18	C	VDD	Core logic power pin	
19		NC	No connection and do not connect with other NC pins	Keep Open
20	C	VSH	Positive Source driving voltage	
21	C	PREVGH	Power Supply pin for VGH and VSH	
22	C	VSL	Negative Source driving voltage	
23	C	PREVGL	Power Supply pin for VCOM, VGL and VSL	
24	C	VCOM	VCOM driving voltage	

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note 5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled High, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active Low.

Note 5-4: This pin (BUSY) is Busy state output pin. When Busy is Low the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin Low when the driver IC is working such as:

- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 5-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits SPI

6. Command Table

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R01H	**PWR**	W	0	0	0	0	0	0	0	0	1	(01H)
	1st Para	W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03H
	2nd Para	W	1	-	-	-	-	-	-	0	0	00H
R02H	**POF**	W	0	0	0	0	0	0	0	1	0	(02H)
R04H	**PON**	W	0	0	0	0	0	0	1	0	0	(04H)
R06H	**BTST**	W	0	0	0	0	0	0	1	1	0	(06H)
	1st Para	W	1	-	0	0	BT_PHA4	BT_PHA3	1	1	1	0FH
	2nd Para	W	1	-	0	0	BT_PHB4	BT_PHB3	1	1	0	0EH
	3rd Para	W	1	-	-	-	BT_PHC4	BT_PHC3	1	0	1	0DH
R10H	**DTM1**	W	0	0	0	0	1	0	0	0	0	(10H)
	1st Para	W	KPxI1[1]	KPxI1[0]	KPxI2[1]	KPxI2[0]	KPxI3[1]	KPxI3[0]	KPxI4[1]	KPxI4[0]	KPxI1[1]	00H
	……	W	1									00H
	Mth Para	W	1	KPxI(N-1)[1]	KPxI(N-1)[0]	KPxIN[1]	KPxIN[0]					00H
R12H	**DRF**	W	0	0	0	0	1	0	0	1	0	(12H)

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R30H	**PLL**	W	0	0	0	1	1	0	0	0	0	(30H)
	1st Para	W	0	-	-	M2	M1	M0	N2	N1	N0	2AH
R40H	**TSC**	W	0	0	1	0	0	0	0	0	0	(40H)
	1st Para	R	1	D10	D9	D8	D7	D6/TS3	D5/TS2	D4/TS1	D3/TS0	00H
	2ndPara	R	1	D2	D1	D0	-	-	-	-	-	00H
R41H	**TSE**	W	0	0	1	0	0	0	0	0	1	(41H)
	1st Para	W	1	TSE	-	-	-	-	-	-	-	00H
R42H	**TSW**	W	0	0	1	0	0	0	0	1	0	(42H)
	1st Para	W	1	WATTR7	WATTR6	WATTR5	WATTR4	WATTR3	WATTR2	WATTR1	WATTR0	00H
	2ndPara	W	1	WMSB7	WMSB6	WMSB5	WMSB4	WMSB3	WMSB2	WMSB1	WMSB0	00H
	3rd Para	W	1	WLSB7	WLSB6	WLSB5	WLSB4	WLSB3	WLSB2	WLSB1	WLSB0	00H
R43H	**TSR**	W	0	0	1	0	0	0	0	1	1	(43H)
	1st Para	R	1	RMSB7	RMSB6	RMSB5	RMSB4	RMSB3	RMSB2	RMSB1	RMSB0	00H
	2ndPara	R	1	RLSB7	RLSB6	RLSB5	RLSB4	RLSB3	RLSB2	RLSB1	RLSB0	00H
R50H	**CDI**	W	0	0	1	0	1	0	0	0	0	(50H)
	1st Para	W	1	-	-	-	DDX	CDI3	CDI2	CDI1	CDI0	17H
R61H	**TRES**	W	0	0	1	1	0	0	0	0	1	(61H)
	1st Para	W	1	HRES7	HRES6	HRES5	HRES4	HRES3	HRES2	HRES1	0	00H
	2ndPara	W	1	-	-	-	-	-	-	-	VRES8	00H
	3rd Para	W	1	VRES7	VRES6	VRES5	VRES4	VRES3	VRES2	VRES1	VRES0	00H
R82H	**VDCS**	W	0	1	0	0	0	0	0	1	0	(82H)
	1st Para	W	1	-	-	VDCS5	VDCS4	VDCS3	VDCS2	VDCS1	VDCS0	00H

Power Setting Register

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R01H	**PWR**	W	0	0	0	0	0	0	0	0	1	(01H)
	1st Para	W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03H
	2ndPara	W	1	-	-	-	-	-	-	0	0	00H

Name	Control	Value	Function Description
VDS_EN	Source Power Selection	0	External positive source voltage from VDH pin and negative source voltage from VDL pin
		1	Internal voltage generation circuit for both VDH/VDL
VDG_EN	Gate Power Selection	0	External positive source voltage from VDH pin and negative source voltage from VDL pin
		1	Internal voltage generation circuit for both VDH/VDL

Note: For this panel the 2ndPara must set as 0x00.

Power OFF

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R02H	**POF**	W	0	0	0	0	0	0	0	1	0	(02H)

After the Power Off command, driver will power off based on the power off Sequence, BUSY will become "0". This command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD becomes OFF.

SD output and Vcom will base on previous condition. It may have 2 conditions: 0V or floating.

This command can be active only when BUSY = "1".

Power ON / Setting

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R04H	**PON**	W	0	0	0	0	0	0	1	0	0	(04H)
R06H	**BTST**	W	0	0	0	0	0	0	1	1	0	(06H)
	1st Para	W	1	-	0	0	BT_PHA4	BT_PHA3	1	1	1	0FH
	2ndPara	W	1	-	0	0	BT_PHB4	BT_PHB3	1	1	0	0EH
	3rd Para	W	1	-	-	-	BT_PHC4	BT_PHC3	1	0	1	0DH

Name	Control	Value	Description
BT_PHA[4:3] BT_PHB[4:3] BT_PHC[4:3]	Driving Strength	00	1
		01	2
		10	3
		11	4

Note: For this panel, You 'd better to set these bits's (BT_PHA \BT_PHB\BT_PHC) value to 00.

Data Start Transmission 1 / Data Stop Command (B/W)

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R10H	**DTM1**	W	0	0	0	0	1	0	0	0	0	(10H)
	1st Para	W	1	KPixel1[1:0]		KPixel2[1:0]		KPixel3[1:0]		KPixel4[1:0]		00H
		W	1	…		…		…		…		00H
	Mth Para	W	1	KPixel(n-1)[1:0]		KPixel(n)[1:0]		-	-	-	-	00H

This Command starts transmitting data and write them into SRAM. To complete data transmission, command DSP(Data transmission Stop) must be issued. Then the chip will start to send data/VCOM for panel.

	KPixel(x)[1:0]	LUT
When DDX=0	00	White
	11	Black
When DDX=1	00	Black
	11	White

This command can be active only when BUSY = “1”.

Data Refresh Command

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R12H	**DRF**	W	0	0	0	0	1	0	0	1	0	(12H)

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

This command can be active only when BUSY =“1”. After display refresh command, BUSY signal will become “0”.

PLL Control

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R30H	**PLL**	W	0	0	0	1	1	0	0	0	0	(30H)
	1st Para	W	0	-	-	M2	M1	M0	N2	N1	N0	2AH

Note: For this panel the R30H Must be set as 0x39.

Temperature Sensor Command

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R40H	**TSC**	W	0	0	1	0	0	0	0	0	0	(40H)
	1st Para	R	1	D10	D9	D8	D7	D6/TS3	D5/TS2	D4/TS1	D3/TS0	00H
	2nd Para	R	1	D2	D1	D0	-	-	-	-	-	00H

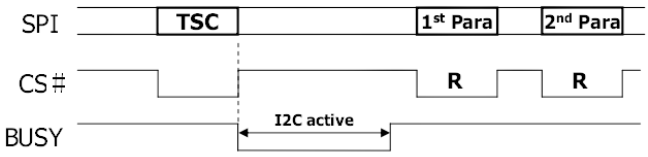
Internal Sensor Mapping

TS[3:0]	temperature
0000	0 ℃
0001	5 ℃
0010	10 ℃
0011	15 ℃
0100	20 ℃
0101	25 ℃
0110	30 ℃
0111	35 ℃
1000	40 ℃
1001	45 ℃
1010	50 ℃

External LM75 Sensor Mapping (D10~D0)

Table 10. Temp register value

11-bit binary (2's complement)	Hexadecimal value	Decimal value	Value
011 1111 1000	3F8	1016	+127.000 °C
011 1111 0111	3F7	1015	+126.875 °C
011 1111 0001	3F1	1009	+126.125 °C
011 1110 1000	3E8	1000	+125.000 °C
000 1100 1000	0C8	200	+25.000 °C
000 0000 0001	001	1	+0.125 °C
000 0000 0000	000	0	0.000 °C
111 1111 1111	7FF	–1	–0.125 °C
111 0011 1000	738	–200	–25.000 °C
110 0100 1001	649	–439	–54.875 °C
110 0100 1000	648	–440	–55.000 °C



Typical External Sensor Cycles

Temperature Sensor Setting

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R41H	**TSE**	W	0	0	1	0	0	0	0	0	1	(41H)
	1st Para	W	1	TSE	0	0	0	0	0	0	0	00H

Name	Control	Value	Description
TSE	Temperature Sensor Selection	0	Internal temperature sensor
		1	External temperature sensor

VCOM and Data Interval Setting Command

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R50H	**CDI**	W	0	0	1	0	1	0	0	0	0	(50 H)
	1st Para	W	1	-	-	-	DDX	CDI3	CDI2	CDI1	CDI0	17H

Note: For this panel the R50H Must be set as 0x17.

Resolution Setting Command

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R61H	**TRES**	W	0	0	1	1	0	0	0	0	1	(61H)
	1st Para	W	1	HRES7	HRES6	HRES5	HRES4	HRES3	HRES2	HRES1	0	00H
	2nd Para	W	1	-	-	-	-	-	-	-	VRES8	00H
	3rd Para	W	1	VRES7	VRES6	VRES5	VRES4	VRES3	VRES2	VRES1	VRES0	00H

Name	Control	Description
HRES[7:0]	Horizontal Resolution	(1) Horizontal resolution setting (HRES[0] is forced to '0') (2) Minimum active SD channel = S0 (3) Maximum active SD channel = min_active SD + HRES[7:0] - 1
VRES[8:0]	Vertical Resolution	(1) Vertical resolution setting (2) Minimum active GD channel = G0 (3) Maximum active GD channel = min_active GD + VRES[8:0] - 1

Resolution setting (R61H) has higher priority than RES [1:0](R00H).

Note : For this panel R61H ‘s value must be 0x68、0x00、0xD4.

VCOM-DC Setting

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R82H	**VDCS**	W	0	1	0	0	0	0	0	1	0	(82H)
	1st Para	W	1	-	-	VDCS5	VDCS4	VDCS3	VDCS2	VDCS1	VDCS0	0CH

VDCS[5:0]	VCOM Value		VDCS[5:0]	VCOM Value
000000	0v		……	……
000001	-0.1v		011011	-2.7v
000010	-0.2v		011100	-2.8v
000011	-0.3v		011101	-2.9v
000100	-0.4v		011110	-3.0v
000101	-0.5v		……	
000110	-0.6v		111111	

7. Electrical Characteristics

7-1) Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V_{CI}	-0.5 to +3.6	V
Logic Input Voltage	V_{IN}	-0.5 to VCI +0.5	V
Logic Output Voltage	V_{OUT}	-0.5 to VCI +0.5	V
Operating Temp. range	T_{OPR}	0 to +40	℃
Storage Temp. range	T_{STG}	-25 to +70	℃

7-2) Panel DC Characteristics

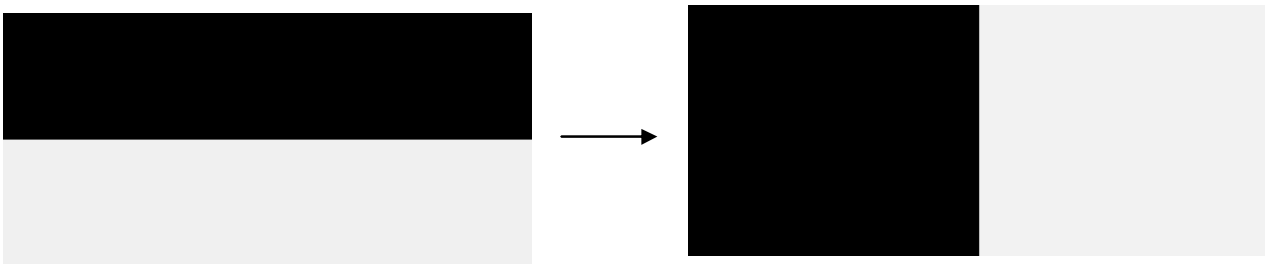
The following specifications apply for: VSS = 0V, VCI = 3.0V, TA = 25℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Single ground	V_{SS}	-	-	0	-	V
Logic Supply Voltage	VCI	-	2.3	3.0	3.6	V
High level input voltage	VIH	-	0.8VCI	-	-	V
Low level input voltage	VIL	-	-	-	0.2VCI	V
High level output voltage	VOH	IOH= -100uA	0.9VCI	-	-	V
Low level output voltage	VOL	IOH= 100uA	-	-	0.1VCI	V
Image update current	I_{UPDATE}	-	-	8	12	mA
Standby panel current	Istandby	-	-	-	5	uA
Power panel (update)	P_{UPDATE}	-	-	26.4	40	mW
Standby power panel	P_{STBY}	-	-	-	0.0165	mW
Operating temperature	-	-	0	-	40	℃
Storage temperature	-	-	-25	-	70	℃
Image updateTime at 25℃	-	-	-	3000	-	ms
Sleep mode current	VCI	DC/DC off No clock No input load Ram data not retain	-	2	5	uA

- The Typical power consumption is measured with following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern. (Note 7-1)
- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display
- Vcom is recommended to be set in the range of assigned value ± 0.1V.

Note 7-1

The Typical power consumption



7-3) Panel AC Characteristics

7-3-1) MCU Interface

7-3-1-1) MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS1 pins. When it is "Low", 4-wire SPI is selected. When it is "High", 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	D1	D0	CS#	D/C#	RES#
SPI4	SDin	SCLK	CS#	D/C#	RES#
SPI3	SDin	SCLK	CS#	L	RES#

Table 7-1: MCU interface assignment under different bus interface mode

Note **7-2**: L is connected to VSS

Note 7-3: H is connected to VCI

7-3-1-2) MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN.

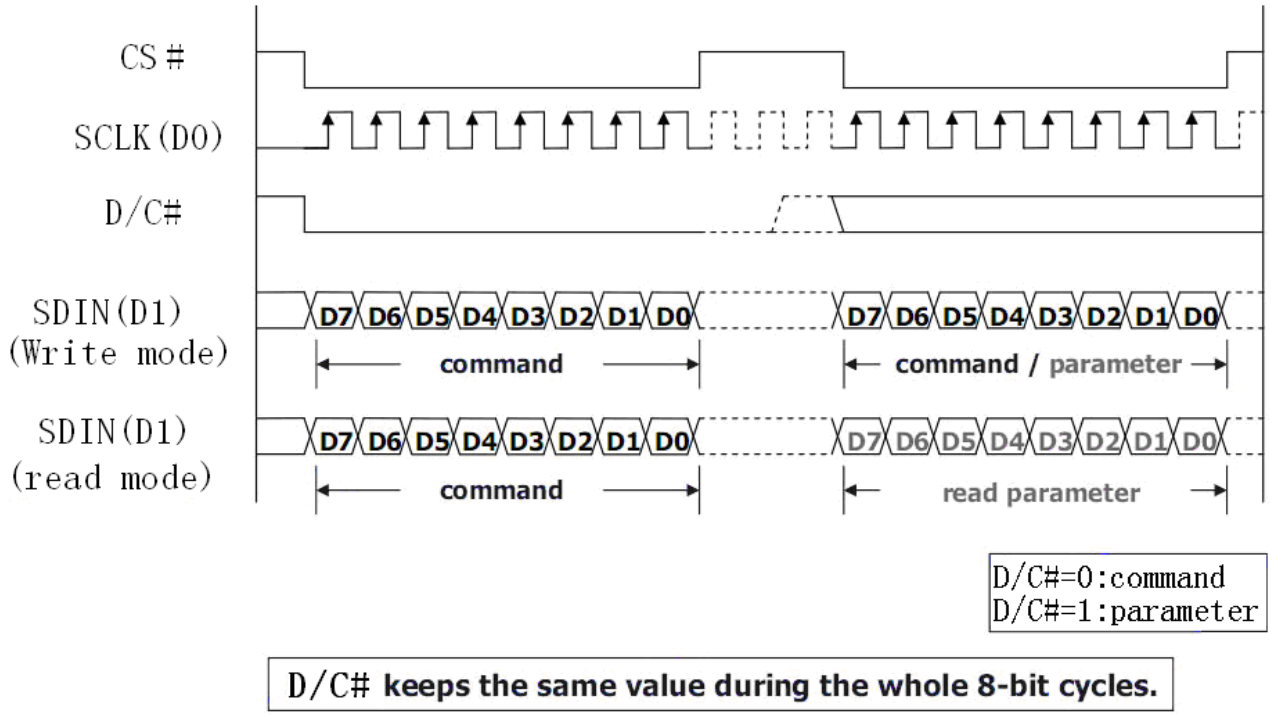
Function	CS#	D/C#	SCLK
Write Command	L	L	↑
Write data	L	H	↑

Table 7-2: Control pins of 4-wire Serial Peripheral interface

Note 7-9: ↑stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.
Under serial mode, only write operations are allowed.

Figure 7-1: Write procedure in 4-wire Serial Peripheral Interface mode



7-3-1-3) MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.

In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN, The pin D/C# can be connected to an external ground.

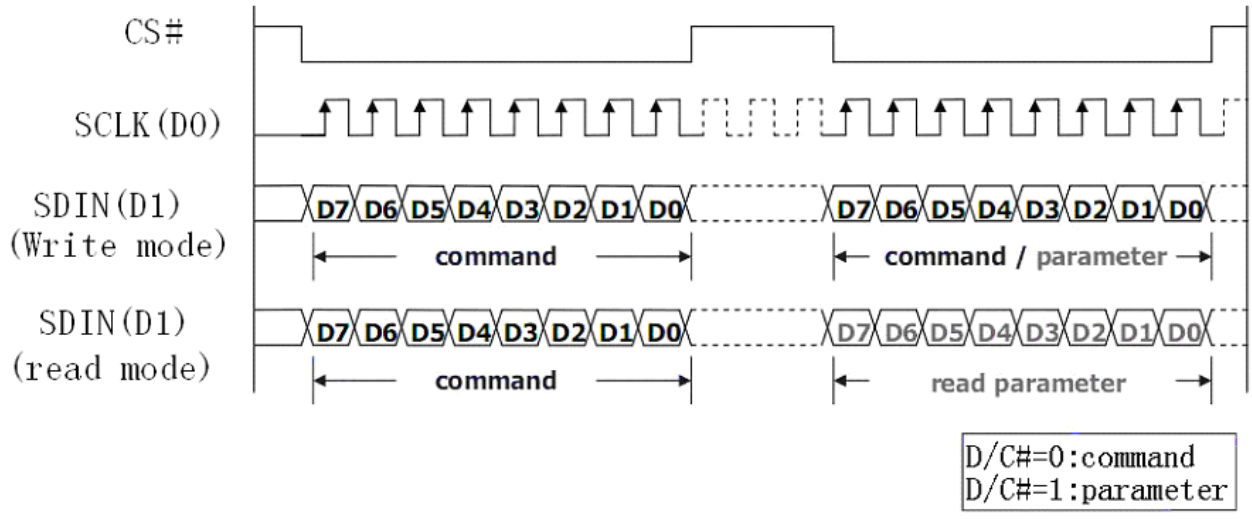
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write Command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

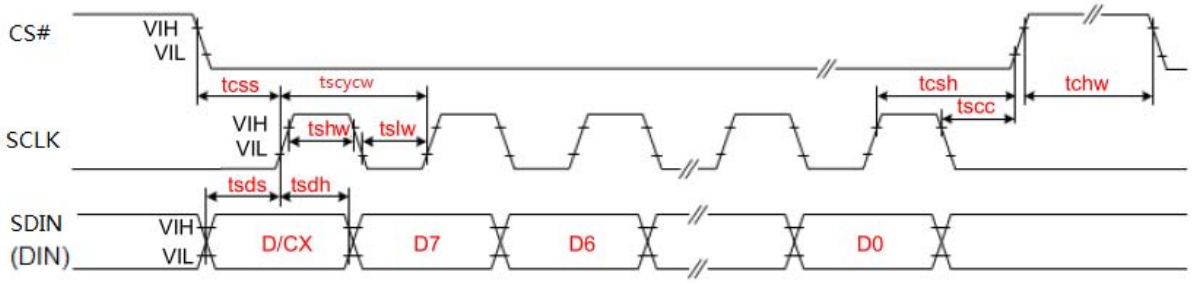
Table 7-3: Control pins of 3-wire Serial Peripheral Interface

Note 7-10: ↑stands for rising edge of signal

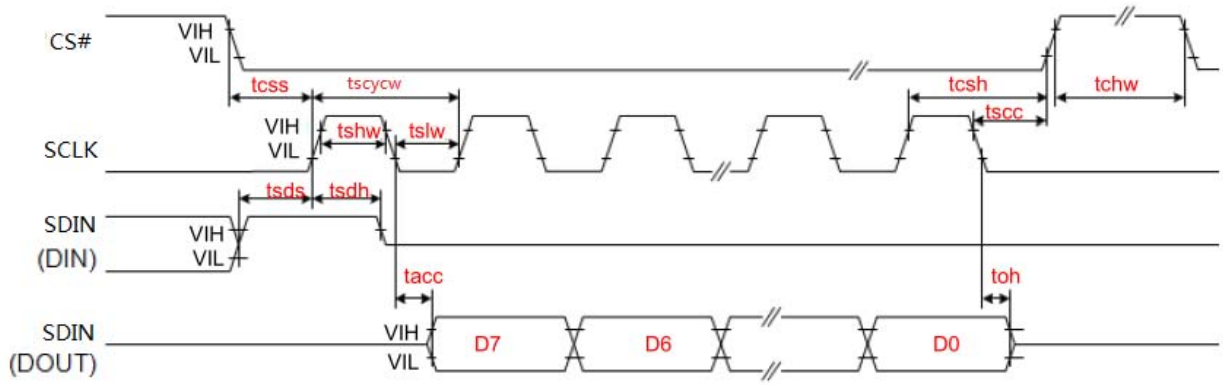
Figure 7-2: Write procedure in 3-wire Serial Peripheral Interface mode



7-3-2) Timing Characteristics of Series Interface



3-wire Serial Interface – Write



3-wire Serial Interface – Read

Symbol	Signal	Parameter		Min	Typ	Max	Unit
SERIAL COMMUNICATION							
tcss	CSB	Chip Select Setup Time		60	-	-	ns
tcsh		Chip Select Hold Time		65	-	-	ns
tscc		Chip Select Setup Time		20	-	-	ns
tchw		Chip Select Setup Time		40	-	-	ns
tscycw	SCL	Serial clock cycle (write)		100	-	-	ns
tshw		SCL “H” pulse width (write)		35	-	-	ns
tslw		SCL“L” pulse width (write)		35	-	-	ns
tscycr		Serial clock cycle (Read)		150	-	-	ns
tshr		SCL “H” pulse width (Read)		60	-	-	ns
tslr		SCL “L” pulse width (Read)		60	-	-	ns
tsds	SDIN (DIN) (DOUT)	Data setup time		30	-	-	ns
tsdh		Data hold time		30	-	-	ns
tacc		Access time		10	-	-	ns
toh		Output disable time		15	-	-	ns

7-4) Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	26.4	40	mW	-
Power consumption in standby mode	-	25℃	-	0.0165	mW	-

7-5) Reference Circuit

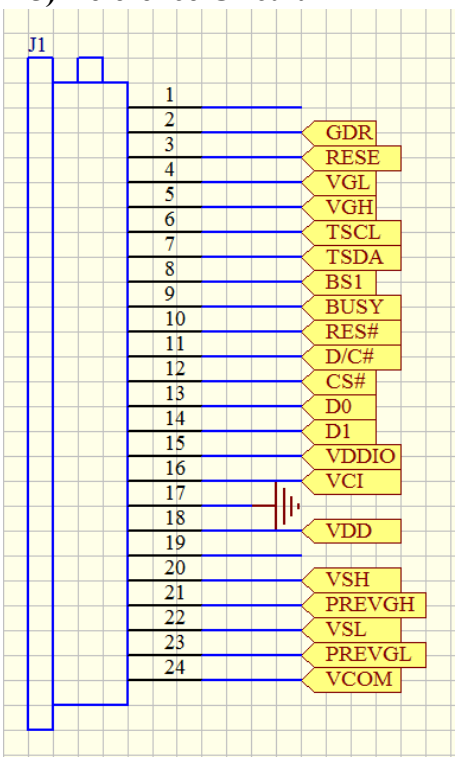


Figure . 7-5 (1)

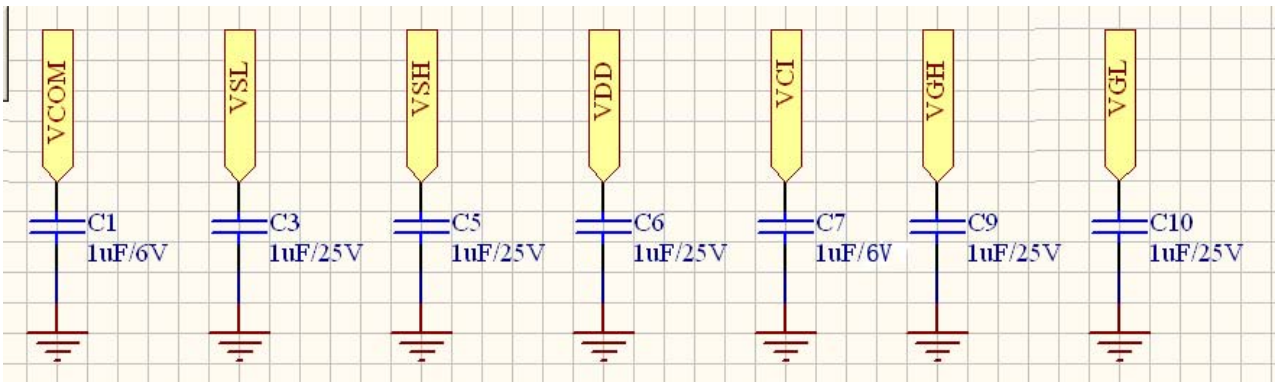


Figure . 7-5 (2)

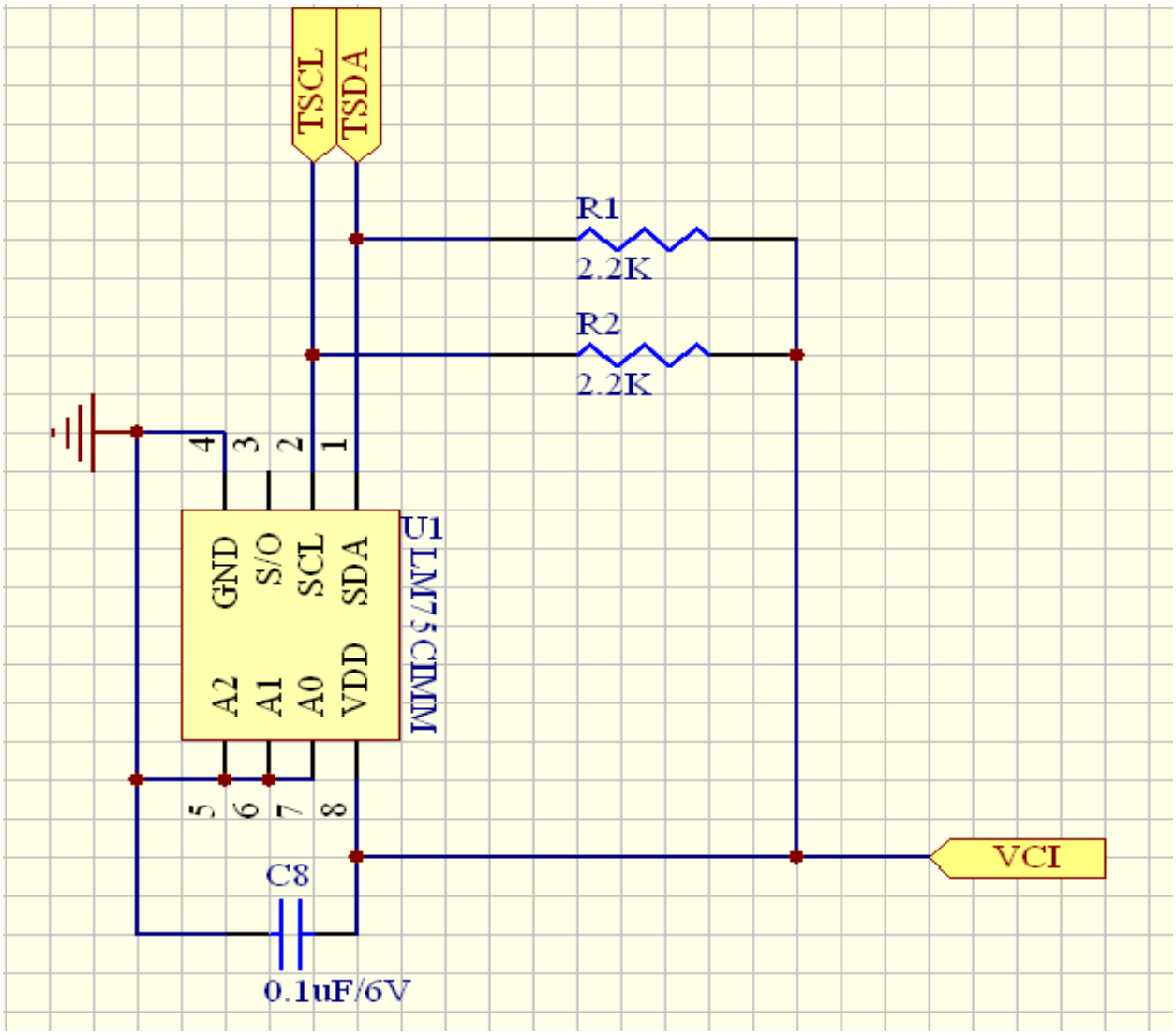

TSCL
TSDA
R1
2.2K
R2
2.2K
4
3
2
1
GND
S/O
SCL
SDA
A2
A1
A0
VDD
U1
LM75CIMM
5
6
7
8
VCI
C8
0.1uF/6V

Figure . 7-5 (3)

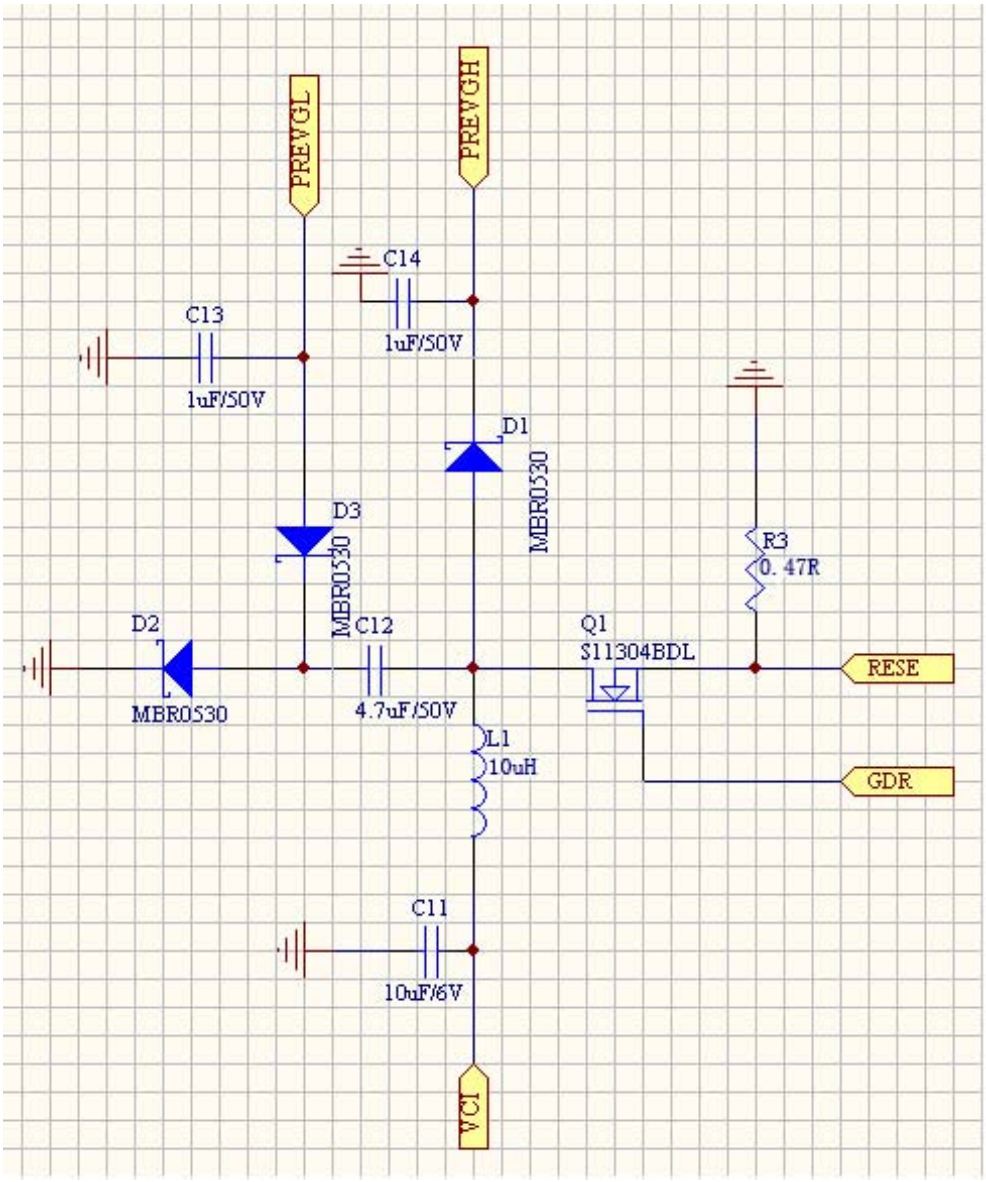

PREVGL
PREVGH
C14
1uF/50V
C13
1uF/50V
D1
MBR0530
D3
MBR0530
R3
0.47R
D2
MBR0530
C12
4.7uF/50V
Q1
SI1304BDL
RESE
L1
10uH
GDR
C11
10uF/6V
VCI

Figure . 7-5 (4)

8. Waveform LUT control software

For every bunch of EPD the waveform data is different, so you may receive the waveform LUT from Good Display. You just need to use the follow sequence to download the waveform into driver IC.

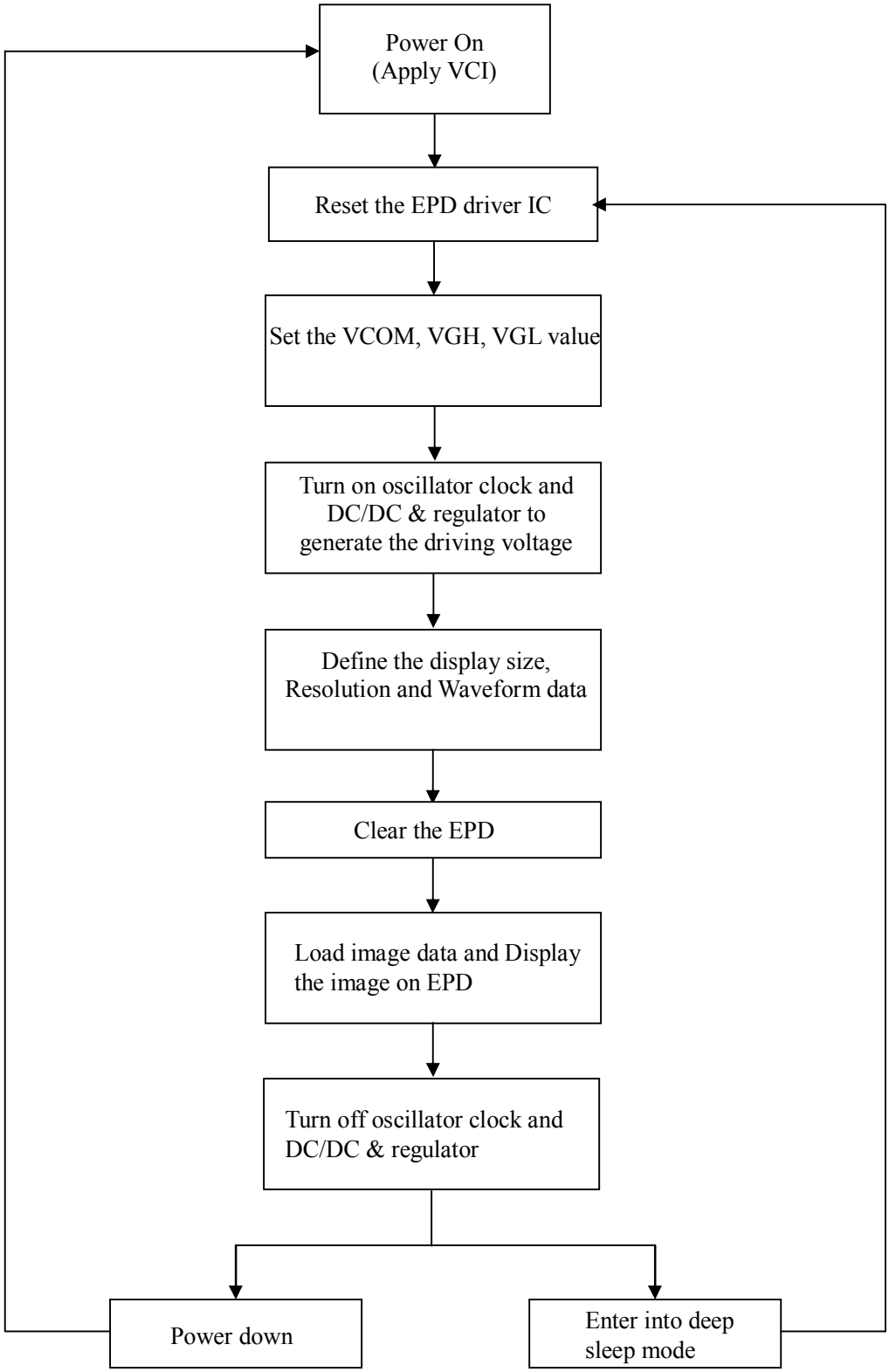
sequence	command	Action Description	remark
1	04	Power on	Send cmd 04
2	20	VCOM LUT Setting	Send cmd 20 data lut_vcom0[]
3	21	White LUT Setting	Send cmd 21 data lut_w[]
4	22	Black LUT Setting	Send cmd 22 data lut_b[]

Note: To download the waveform into driver ic, you must send command 04 first, then send 20, 21, 22 command.

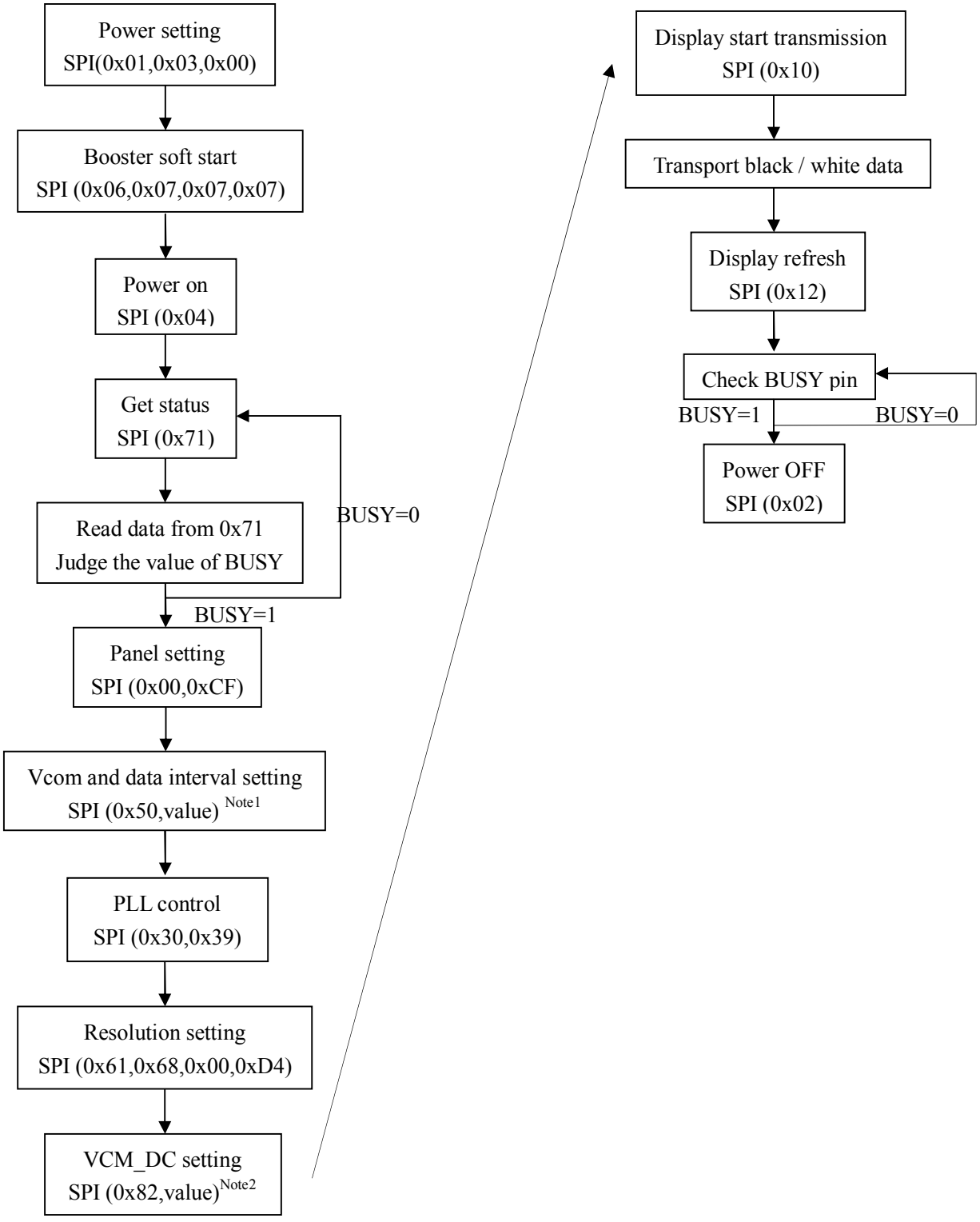
The data of lut_vcom0[], lut_w[], lut_b[], each batch of EPD is different.Good Display will support the data after you receive the EPD.

9. Typical Operating Sequence

9-1) Normal Operation Flow



9-2) Reference Program Code



Note1: When value=0x57, border will be drive to black after refresh. When value=0x17, the border is set to floating.

Note2: Different EPD with different VCOM value,Good Displaywill provide different values according to different batches of EPD.

10. Optical characteristics

10-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 10-1
Gn	2Grey Level	-	-	DS+(WS-DS) xn (m-1)	-	L*	-
CR	Contrast Ratio	indoor	8		-	-	-
Panel's life		0℃~40℃		1000000 times or 5 years			Note 10-2

WS: White state, DS: Dark state

Gray state from Dark to White : DS、WS

m: 2

Note 10-1: Luminance meter: Eye – One Pro Spectrophotometer

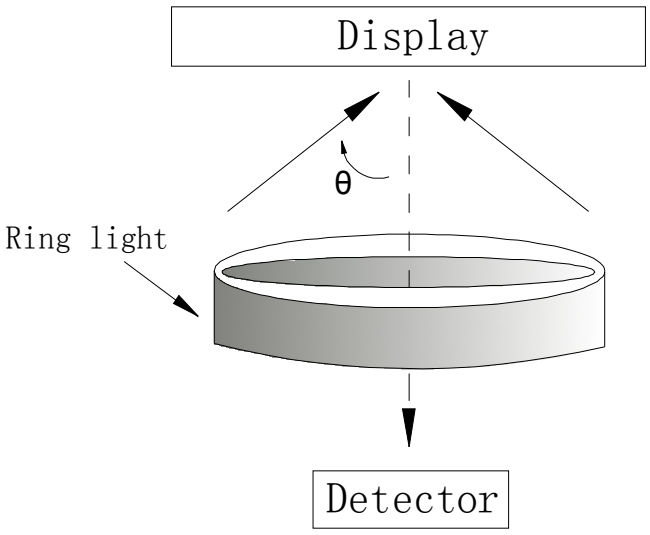
Note 10-2: When work in temperature below 0 degree or above 40 degree, we do not recommend because the panel's life will not be guaranteed.

10-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd)() :

R1: white reflectance Rd: dark reflectance

CR = R1/Rd

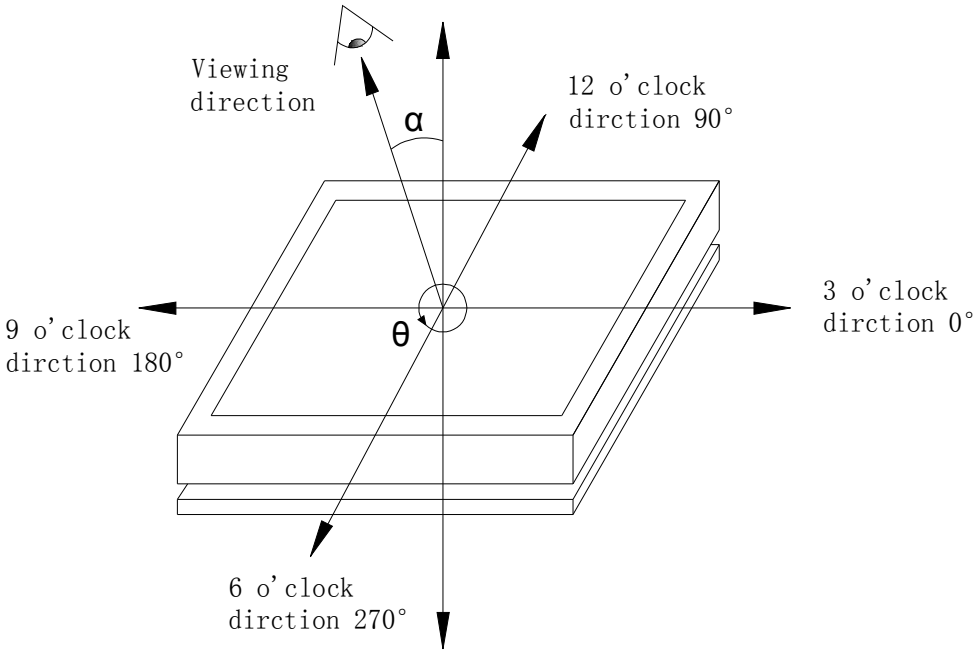


10-3) Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



10-4) Bi-stability

The Bi-stability standard as follows:

Bi-stability	Result		
24 hours Luminance drift		AVG	MAX
	White state △L*	-	3
	Black state △L*	-	3

11. HANDLING，SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
RoHS

12. Reliability test

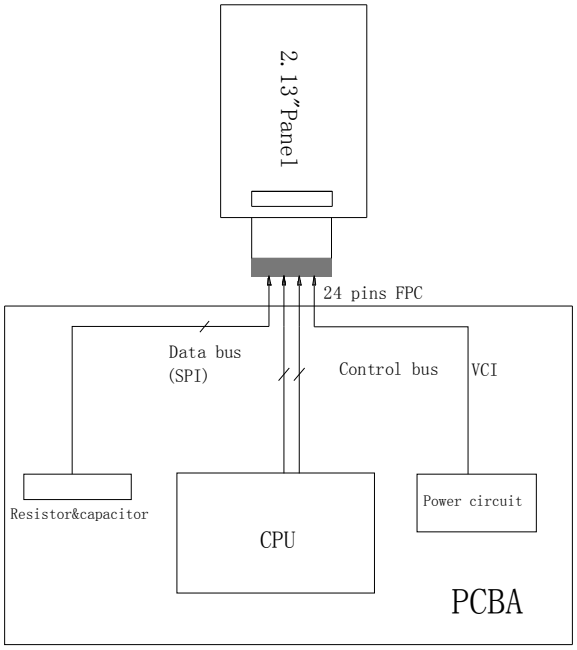
	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = 40℃,30% for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard# IEC 60 068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
2	Low-Temperature Operation	T = 0℃ for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return room temperature, testers will observe the appearance, and test electrical and optical performance based on standard# IEC 60 068-2-2Ab.	When experiment finished, the EPD must meet electrical and optical performance standards.
3	High-Temperature Storage	T = +70℃, 23% for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard# IEC 60 068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
4	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard# IEC 60 068-2-2Ab	When experiment finished, the EPD must meet electrical and optical performance standards.
5	High Temperature, High-Humidity Operation	T=+40℃,RH=90 % for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard# IEC 60 068-2-3CA.	When experiment finished, the EPD must meet electrical and optical performance standards.
6	High Temperature, High-Humidity Storage	T=+60℃,RH=80 % for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard# IEC 60 068-2-3CA.	When experiment finished, the EPD must meet electrical performance standards.

7	Temperature Cycle	[-25℃ 30mins]→[Temperature rise 30mins] [+70℃ 30mins] →[Temperature drop 30mins], 1cycle=2hrs, 70cycles Test in white pattern	1. Samples are put in the Temp & Humid. Environmental Chamber. Temperature cycle starts with -25℃, storage period 30 minutes. After 30 minutes, it needs 30min to let temperature rise to 70℃. After 30min, temperature will be adjusted to 70℃ and storage period is 30 minutes. After 30 minutes, it needs 30min to let temperature rise to -25℃. One temperature cycle (2hrs) is complete. 2. Temperature cycle repeats 70 times. 3. When 70 cycles finished, the samples will be taken out from experiment chamber and set aside a few minutes. As EPDs return to room temperature, tests will observe the appearance, and test electrical and optical performance based on standard# IEC 60 068-2-14NB.	When experiment finished, the EPD must meet electrical and optical performance standards.
8	UV exposure Resistance	765 W/m2 for 168 hrs,40℃	Standard# IEC 60 068-2-5 Sa	
9	Electrostatic discharge	Machine model:+/-250V, 0Ω, 200pF	Standard# IEC61000-4-2	
10	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
11	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment	

Actual EMC level to be measured on customer application.

Note : The protective film must be removed before temperature test.

13. Block Diagram



14. Point and line standard

Shipment Inseption Standard

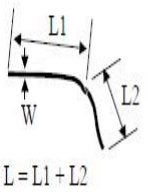
Equipment: Electrical test fixture, Point gauge

Outline demension:

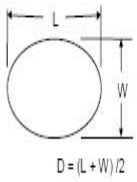
59.2 (H)*29.2(V)*0.98(D) Unit: mm

Environment	Temperature	Humidity	Illumination	Distance	Time	Angle
	20℃～25℃	40%～55%RH	800～1200Lux	200～300 mm	35Sec	

appearance standard	Defet type	Inspection	Standard	Part-A	
	1. dead/ switch point (point overproof)	Electric Display	D≤0.25 mm	Ignore	
			0.25 mm<D≤0.40 mm	N≤2	
			0.40 mm<D	Not Allow	
	2. Line (No switch)	Electric Display	L≤0.24; W≤0.06	Ignore	
			0.24≤L≤0.4; 0.06<W≤0.1	N≤2	
			L>0.4; W>0.1	Not Allow	
	3.line (Switching line)	Electric Display	Ignore in gray scale viewing In Black&white viewing Follow Non-Switching Criteria		
	4.Display unwork	Electric Display	Not Allow		
	5.Display error	Electric Display	Not Allow		
	6.PS PET warping	Visual	cannot beyond 1/2 of the border		
	7.Protector hurt	Visual	L≤2 mm, W≤0.05 mm, Ignore;		
			L>2 mm, W>0.05 mm, Not Allow;		
	8.Adhesive coating	Visual	Bubble: 0.1mm≤D<0.3mm & N≤2		
	9.Packing	Visual	cannot be dirty and breakdown;must be marked and identified		
Remark	1.Cannot be defect & failure cause by appearance defect;				
	2.Cannot be larger size cause by appearance defect;				



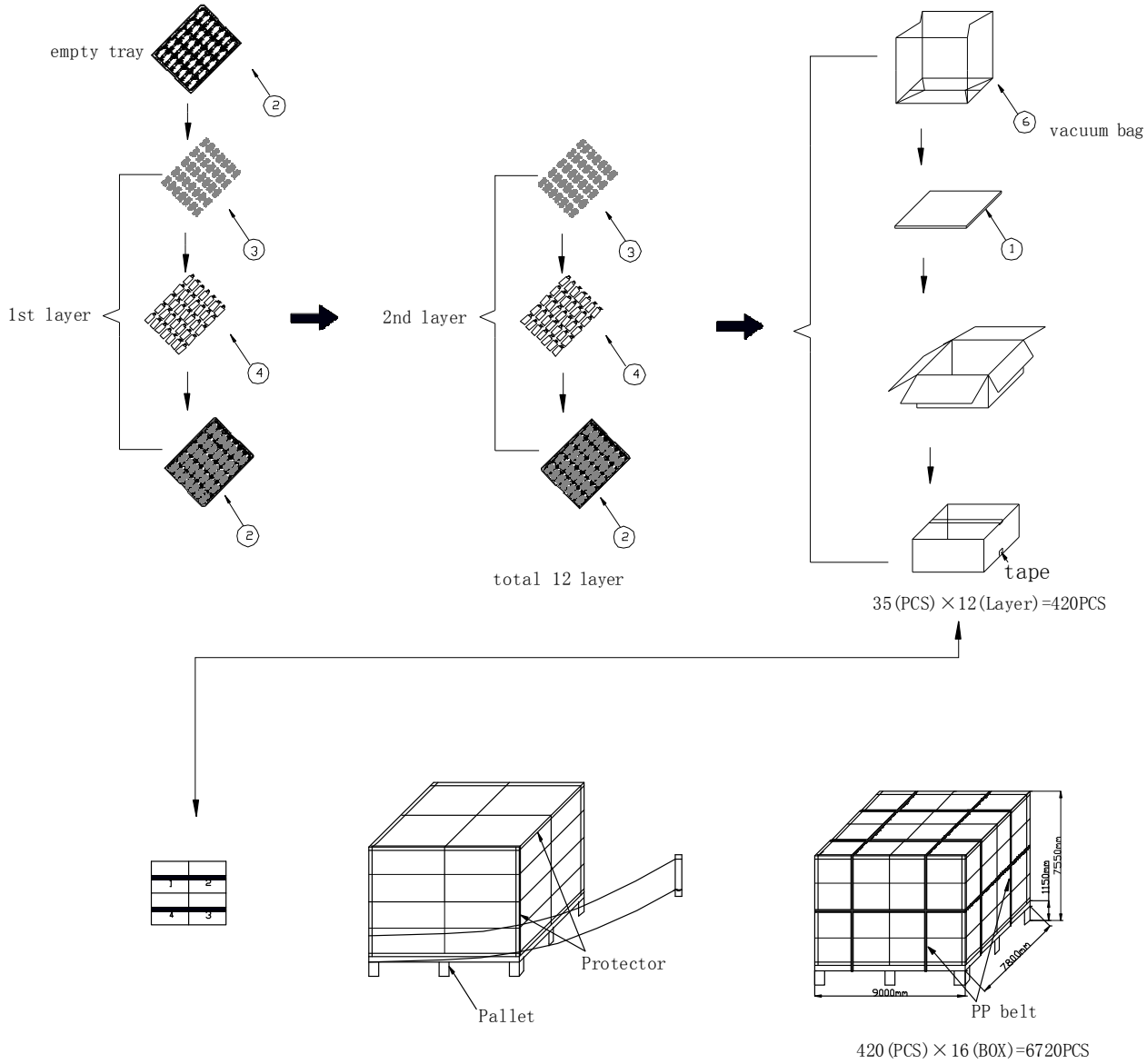
Line Defect



Spot Defect

L=long W=wide D=point size

15. Packing


empty tray
2
3
1st layer
4
2
2nd layer
3
4
2
total 12 layer
6
vacuum bag
1
tape
35(PCS)×12(Layer)=420PCS
1
2
4
3
Protector
Pallet
1150mm
755mm
2800mm
9000mm
PP belt
420(PCS)×16(BOX)=6720PCS