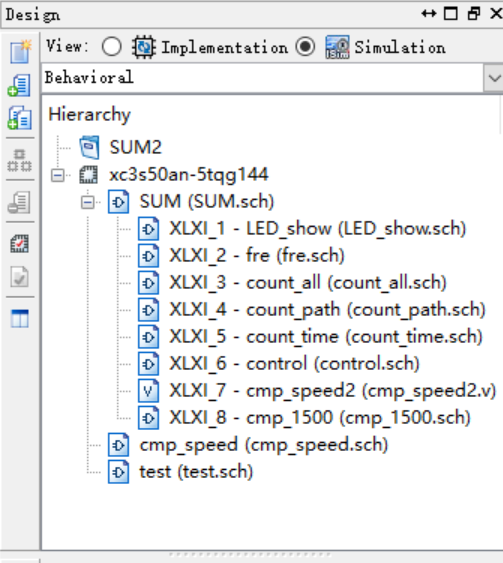
**总体模块说明**



SUM:总体电路结构+部分辅助模块

LED\_show:数码管显示模块。

Fre:分频与控制模块。

Count\_path:快车速计费模块

Count\_time:慢车速计费模块

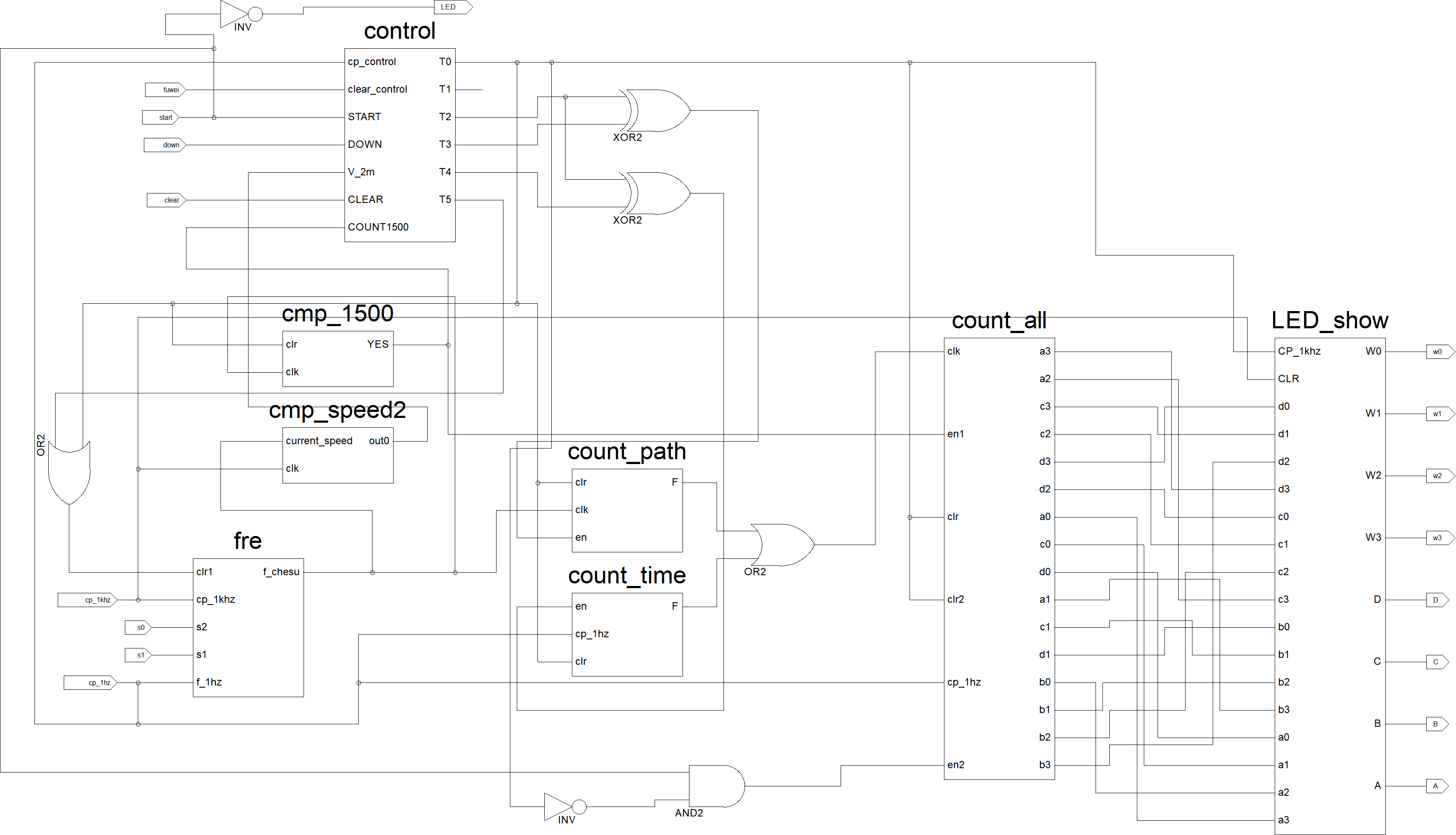
Control：一态一位控制器

Cmp\_speed2:快慢速判断模块

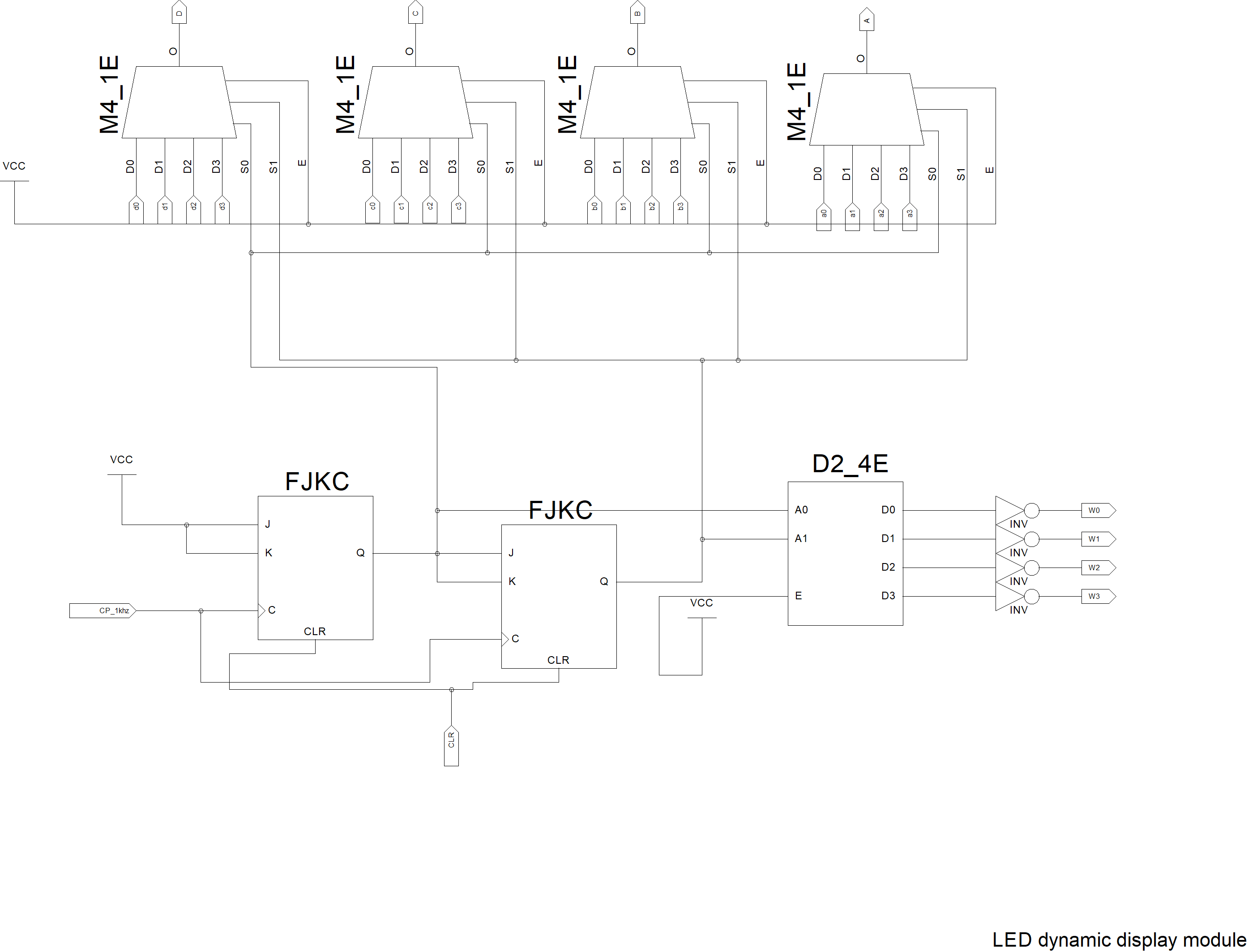
Cmp\_1500:3公里路程判断模块

**部分模块截图**

SUM

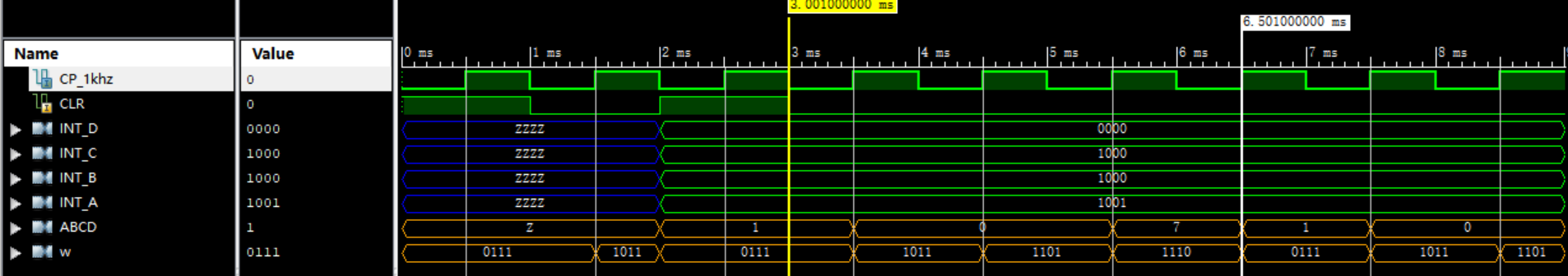


LED\_show

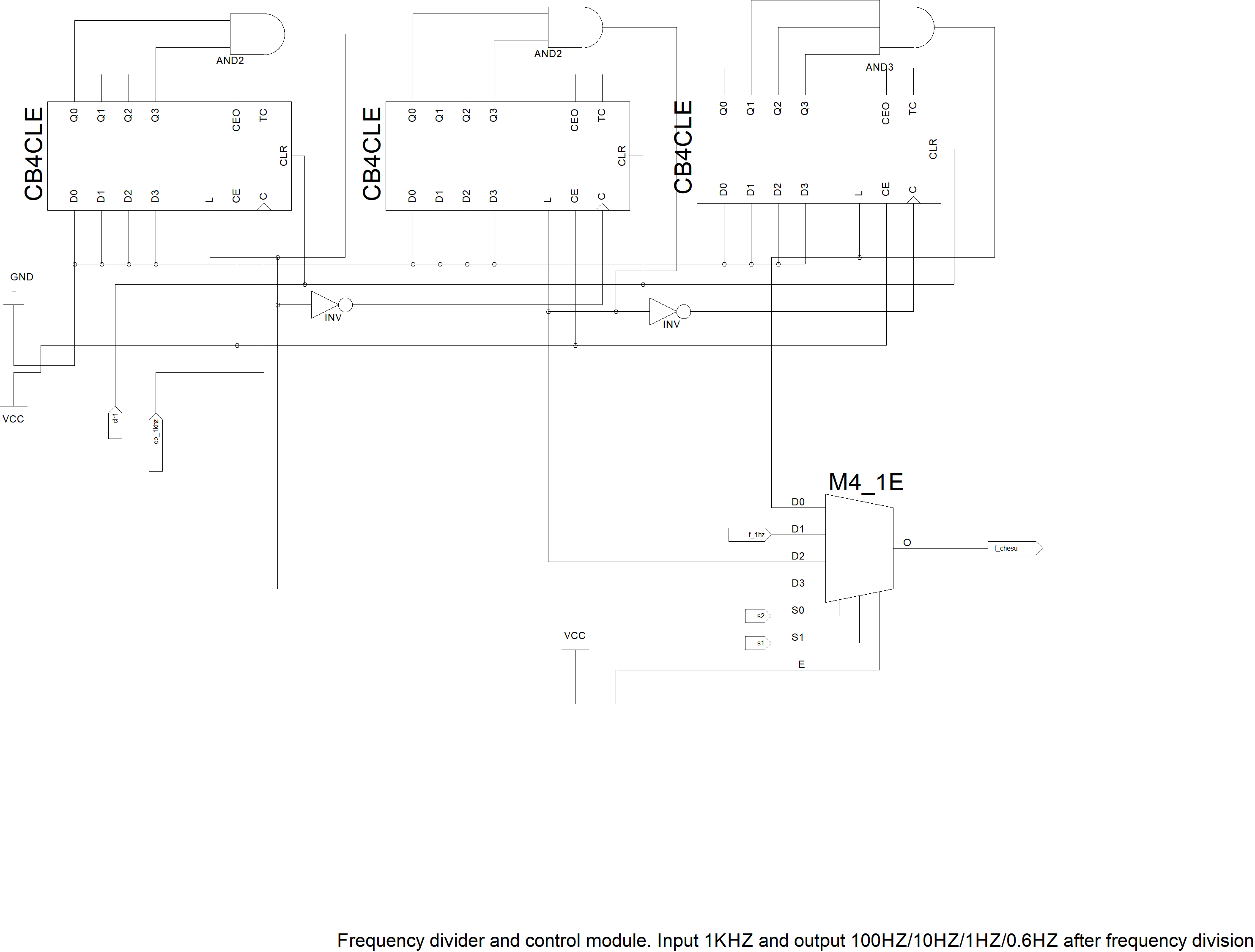


测试：

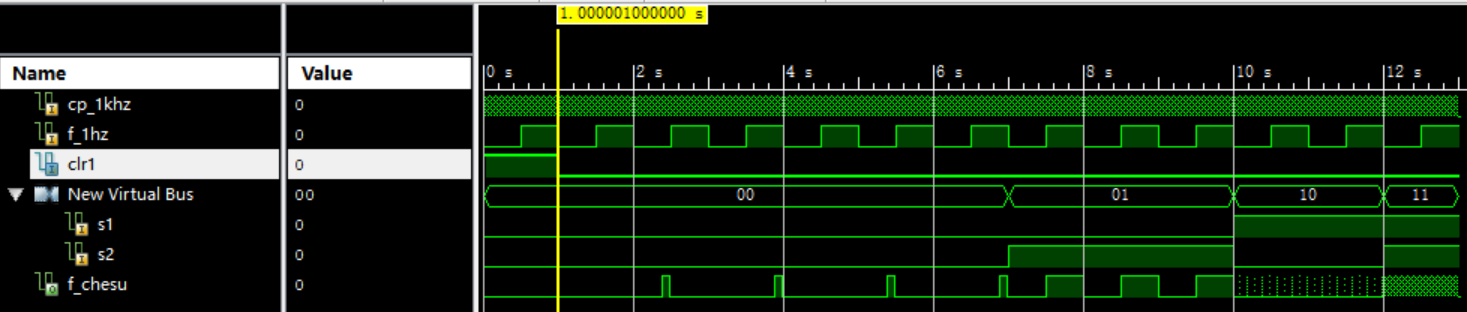
当输入为d0c0b0a0=0001 d1c1b1a1=0000 d2c2b2a2=0000 d3c3b3a3=0111时，输出DCBA为循环1007

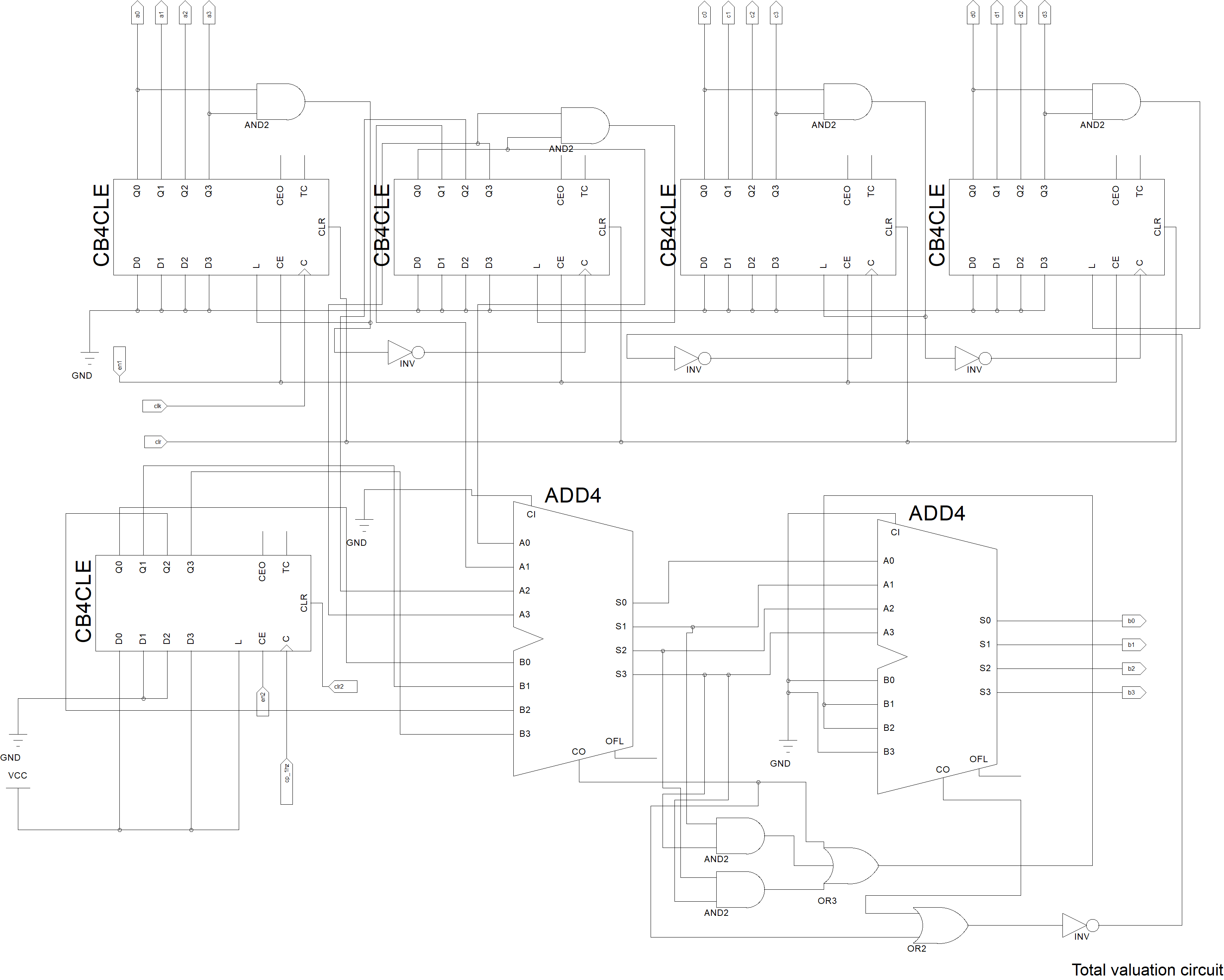


Fre

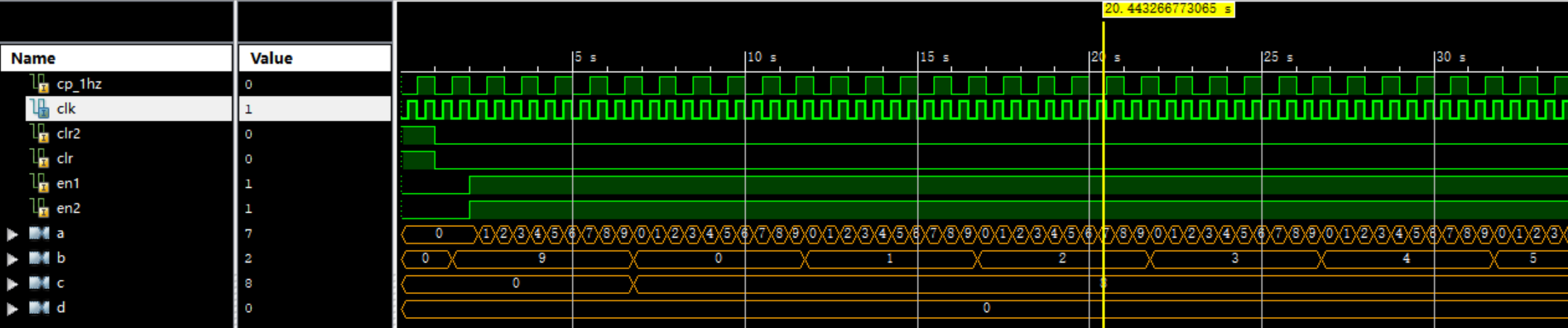


测试

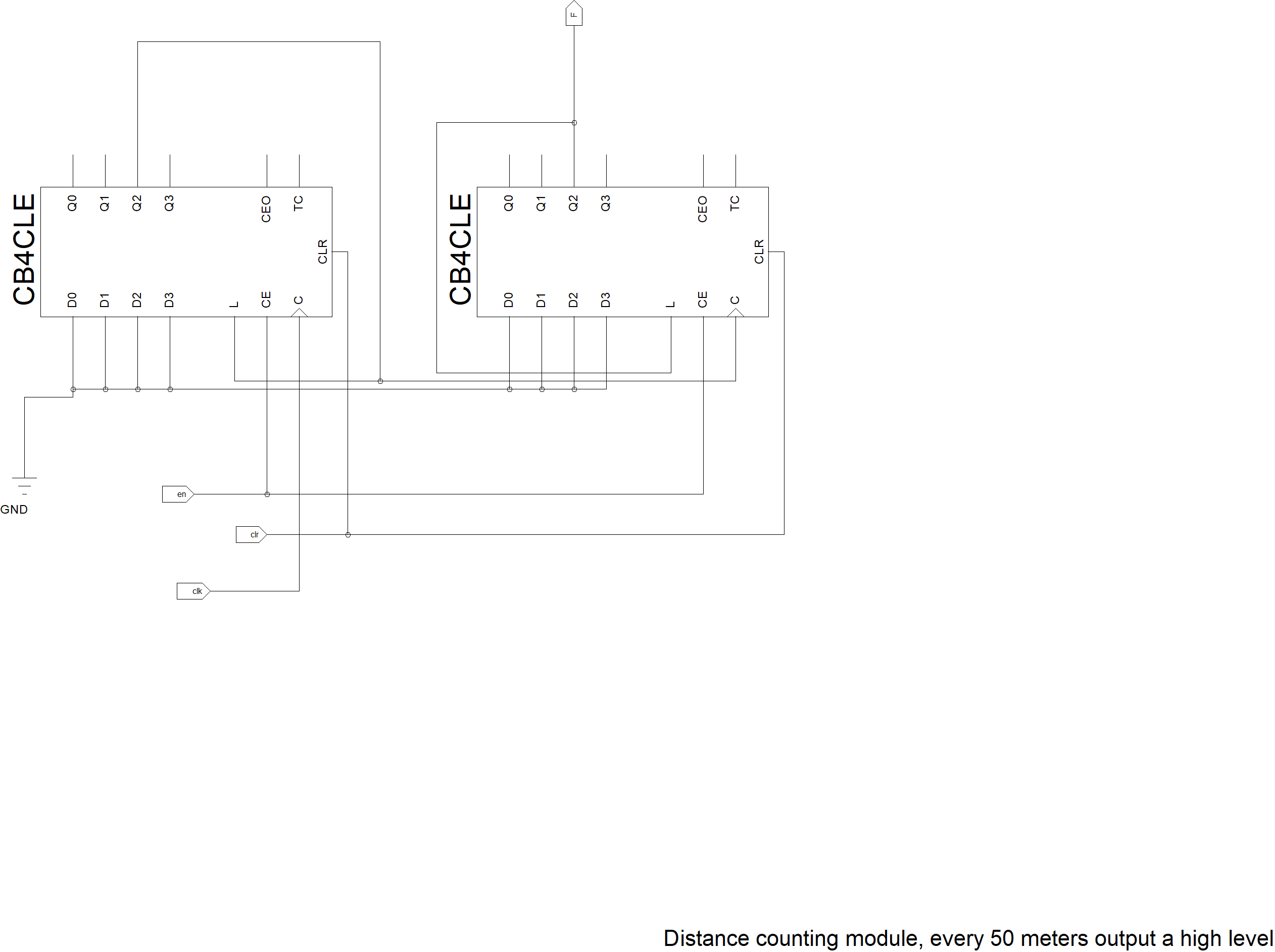




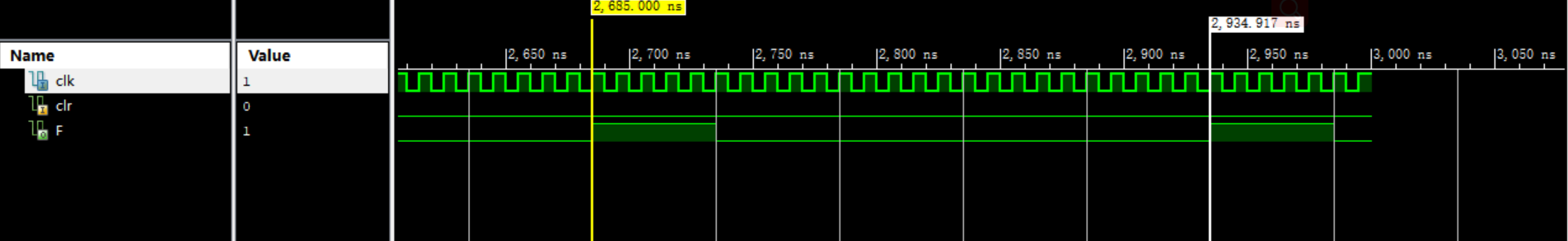
测试



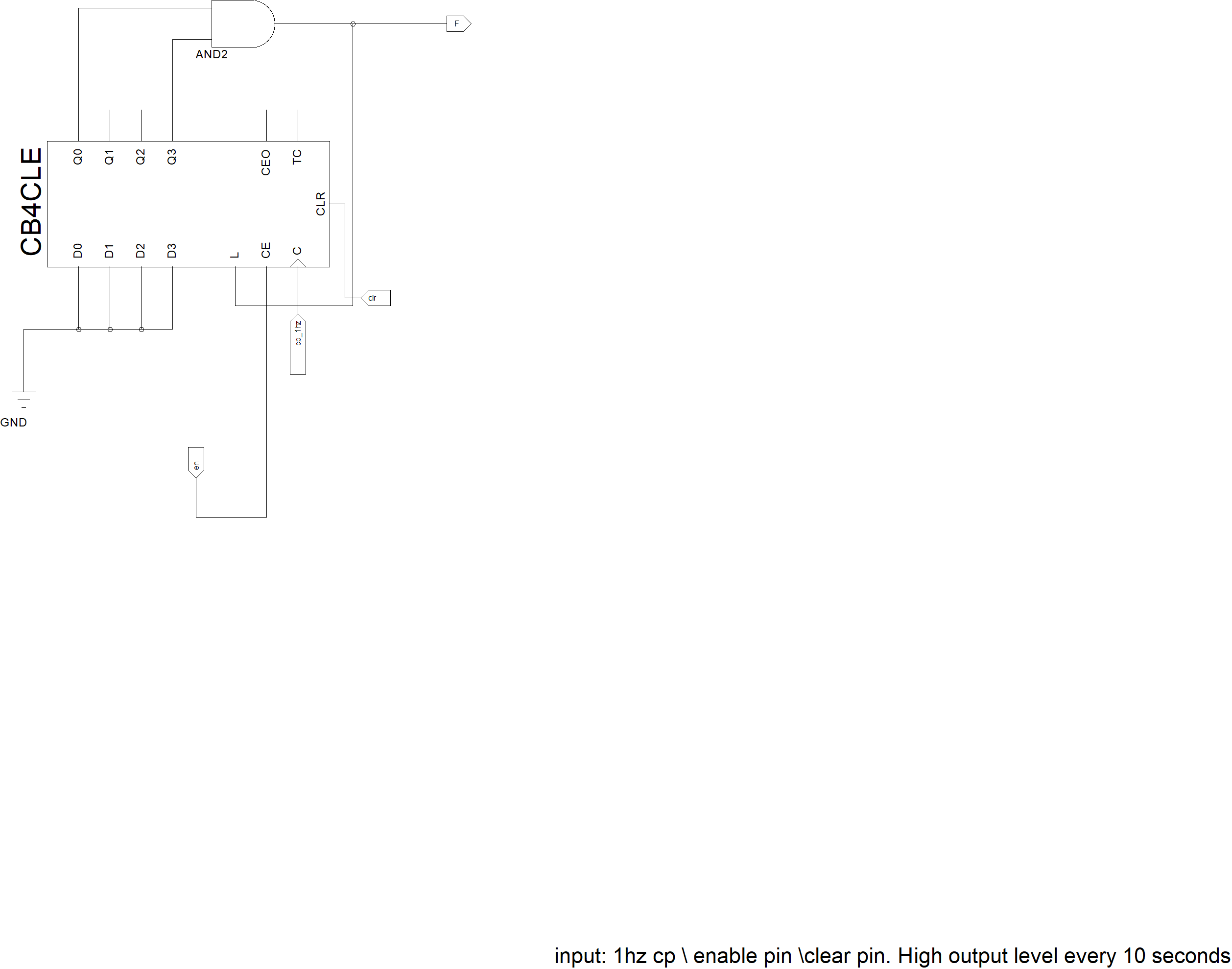
Count\_path



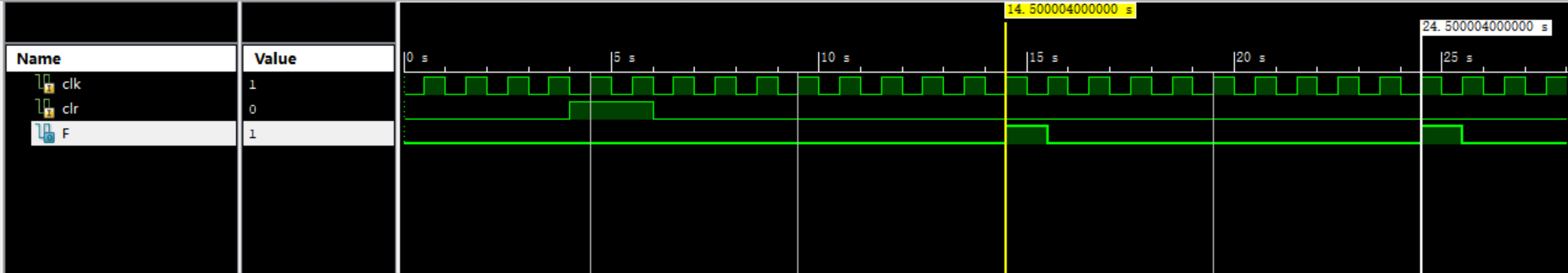
测试



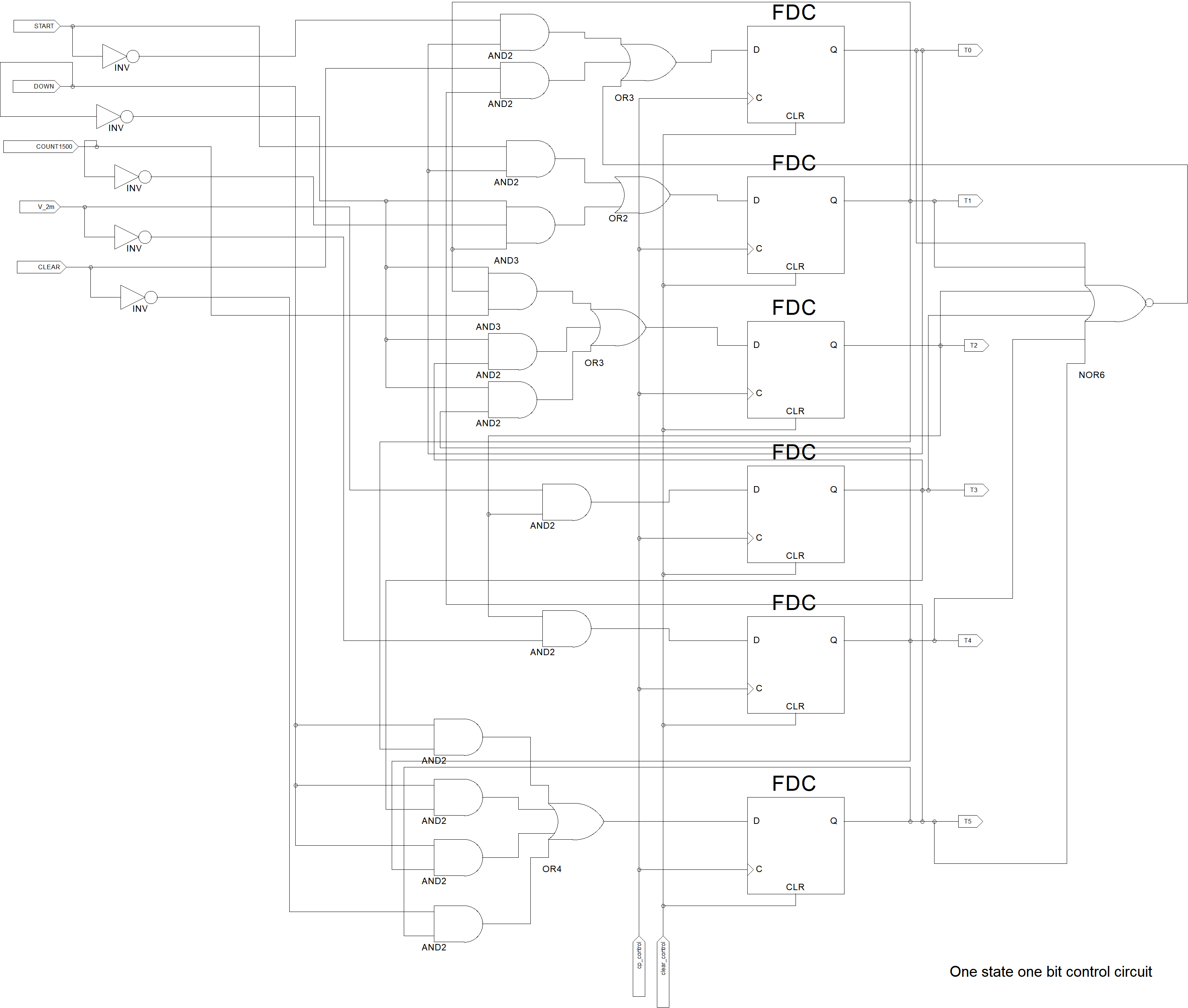
Count\_time



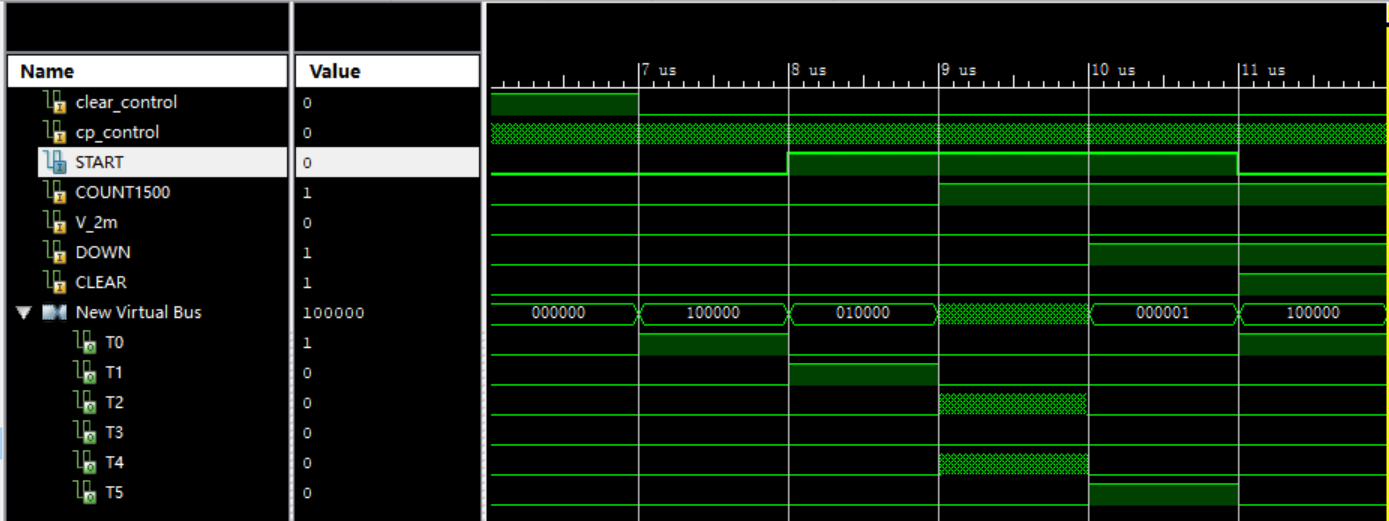
测试



Control



测试



Cmp\_speed2

module cmp\_speed2

( input chesu\_speed,

input clk, //输入

output out

);

reg temp1=0;

reg rst=0;

reg [4:0] cnt1=5'b0\_0000; //单位时间内脉冲数

reg [9:0] cnt2=10'b00\_0000\_0000; //计时

always@(posedge clk) //每秒读一次数据

begin

if(cnt2==999)

begin

f(cnt1>1)

begin

temp1<=1;

rst<=1;

cnt2<=0;

end

else

begin

temp1<=0;

rst<=1;

cnt2<=0;

end

end

else

begin

rst<=0;

cnt2<=cnt2+1;

end

end

always@(posedge current\_speed or posedge rst)

begin

if(rst)

cnt1<=0;

else

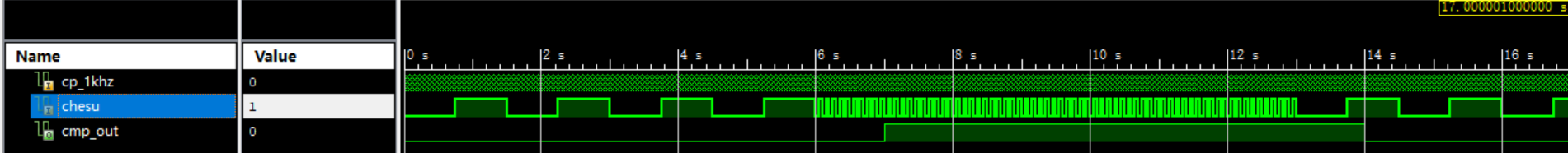
cnt1<=cnt1+1;

end

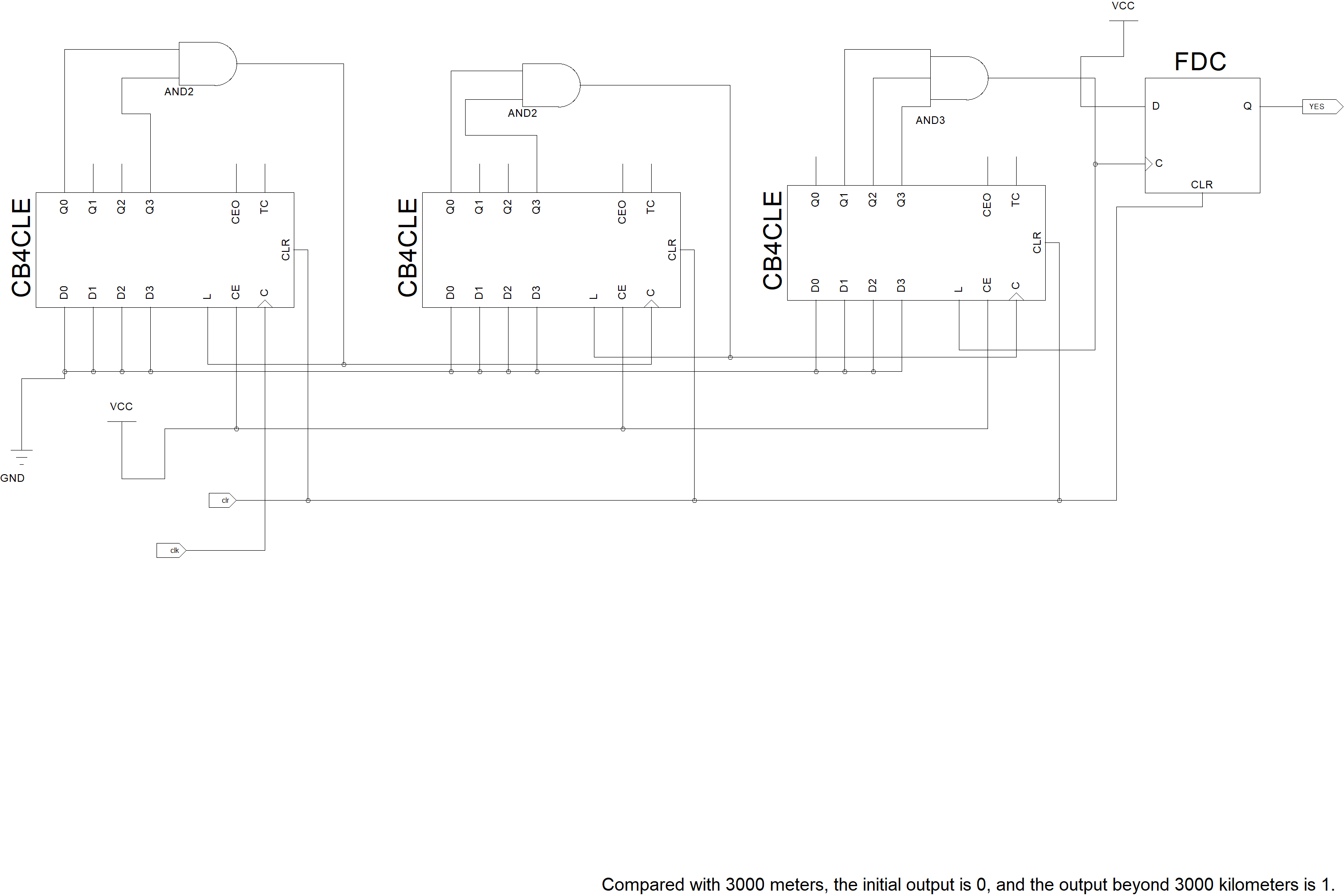
assign out0=temp1;

endmodule

测试



Cmp\_1500:3



测试

