Circuit: g48_exp

Description:

This VHDL code describes a circuit that computes the following function:

$$f(N) = P * 2^{-N/12}$$

The input for this function is a 4 bit binary input called "notenumber' (representing values between 0 and 11), and the output f(N) is the 21-bit binary signal "pitchperiod". Pitchperiod is chosen by having each of the 16 distinct binary input values of notenumber linked to a specific binary value for pitchperiod, that corresponds with plugging notenumber into the function f(N). Since notenumber is only supposed to be a number going up to 11, values 12 through 15 are invalid. As such, we have mapped pitchperiod to all 1's for the invalid inputs.



Figure 1: 21-bit exp circuit with a 4-bit input

Discussion:

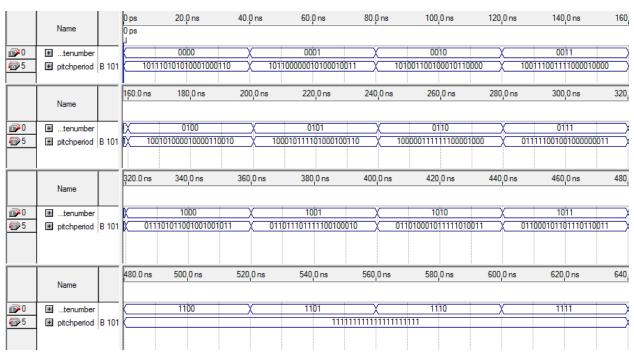


Figure 2: Analysis of the exp circuit

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In order to test this exponential circuit, we instructed the input notenumber to cycle through values 0000 to 1111, and then went through by hand to see that each value of the output matched what the function should produce for those values. Given the small range of notenumber (only sixteen possible combinations), we were able to test every possible input value. This allowed us to perform a very complete test, for which our circuit produced perfect outputs for every input value.

Circuit: g48_sine

Description:

The function of this circuit is to compute the sine of a given angle. The input, angle, is a 9-bit binary number representing the measure of an angle in degrees. The output, sine, is a 16-bit output that corresponds to (2^15)*sin(angle). The output sine is determined by mapping all input values to

appropriate, pre-.mif file

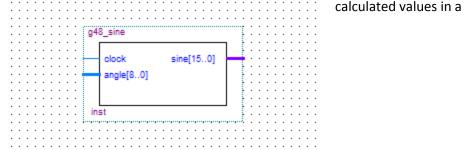


Figure 3: Clocked 16-bit sine with a 9-bit input

Discussion:

Using a clock period set to 10 nanoseconds allowed us to load the input signal on the rising edge of each clock signal. Since we used a lookup table to generate the output we were able to test all 512 input patterns quite easily. Shown below are portions of our functional simulation that include results for some notable values (i.e, angles of 0, 90, and 180 degrees).

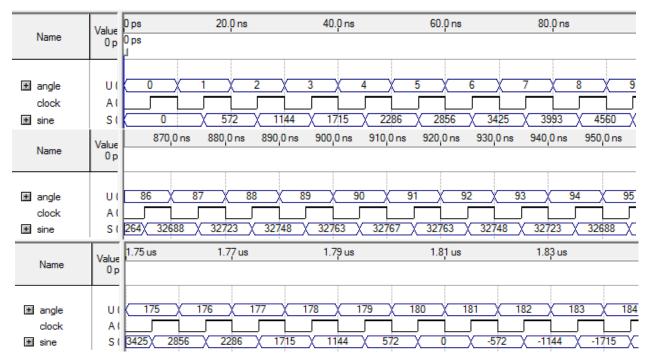


Figure 4: Selected values of the functional simulation results.

Next we looked at the Timing Analyzer Summary section of the compliation report. The path in our circuit with the largest propagation delay, 12.299 ns, was the too path to sine[1].

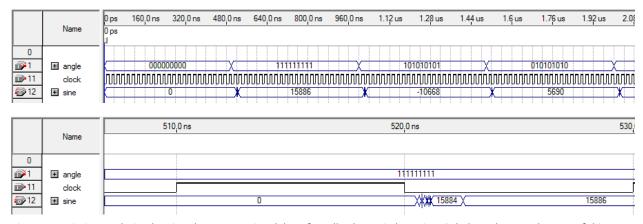


Figure 5.1: Timing analysis, showing the propagation delay after all value switches. Fig 5.2, below, shows a close-up of this delay.

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After the value of angle changes, the circuit will wait until the next valid clock edge to assert the corresponding value of sine. Referring to Fig. 5.2, it takes 10.55 ns from the clock edge at 510.0 ns for sine to begin adjusting itself. After 520.55 ns, our sine output remains uncertain until 522.55 ns, by which time it has settled to its proper value. The amount of time spent on setup is the same for each time angle changes value, as shown in Fig. 5.1; note the set up time for "000000000" is non-existent since the initial value of sine is 0, which happens to be the result of sn inout of 0. In total, this process takes approximately 12.55 ns, which is very similar to the largest propagation delay of 12.299 ns we previously discussed.

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