Group 48
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Stephen Carter – 260500858
Lab 4

g48_note_timer:

Description:

The note timer circuit was designed to produce a tone based on various inputs. Each tone is defined as a 16-bit string of information, and is divided up as follows:

- Bits 0-3: Note Number. This indicates the specific note that is to be played, in accordance with a 12 note musical scale (because this string can go up to 15, values 12-15 correspond to the same note).
- Bits 4-6: Octave Number: This value controls the frequency at which the note is to be played. An increase of 1 in this value corresponds to doubling the frequency.
- Bits 7-9: Note Duration: How long the note is to play, based on the beat. 0 is one eighth of a beat, 1 is one quarter of a beat, etc.
- Bit 10: Triplet: This is a simple yes/no, indicating whether or not the note should be given a duration that's 2/3 that of a regular note.
- Bits 11-14: Loudness: Determines the amplitude of the note's wave.
- Bit 15: End of Song Marker: Marks the end of the song.

Our circuit took in as input a clock signal (clk), an asynchronous reset (reset), note_duration (see above), triplet (see above), and a tempo_enable signal that set the basic tempo of the circuit (creating a pulse at every beat). The circuit gave output signals of count_out, which was essentially a count up to the duration of the note (effectively signaling when it's okay to play a note), and TRIGGER, which. The circuit used a lookup table process block to select the note to be played, based on the note_duration and triplet signals.

The circuit also implemented a counter process block based on the reset and clk signals. When reset is pressed, the count_out output is set to 0, and TRIGGER is set to 1. When the clock is high (and on a rising edge), tempo enable is then checked; if that signal is also high, then the count is incremented. If the count is already 1, then TRIGGER is set back to a value of 0. Finally, the count is checked in this process block. As it has been incremented at each clock cycle, if the count ever reaches a value equal to target-1 while tempo_enable is high, then the count is reset back to 0 and TRIGGER is set to 1.

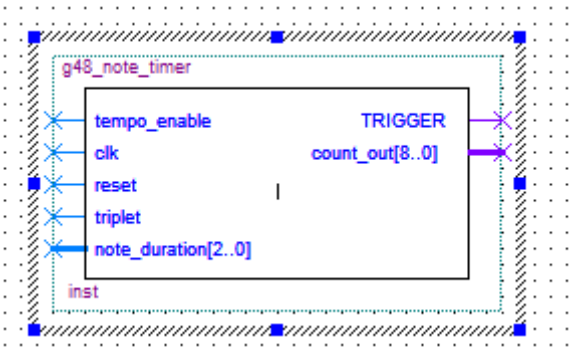

Figure 1: Pinout diagram of the note_timer circuit.

Testing:

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First we preformed simulation tests on the note_timer circuit. We tested the circuit over several different inputs. The tempo_enable pulses were entered by hand as requested by the testing specifications. The testing performed was successful and confirmed by the TA on duty at the time. The results are displayed below.

After completing the simulation tests we created a test bed circuit. This entailed setting the bpm input to correspond to the switches on the board, allowing us to dynamically test different input values on the board. The TRIGGER output was set to a single LED, which would blink if the signal was high, allowing us to further gauge whether our circuit was functioning properly. The count_out output was left open, as it was only used for the timing analysis on the computer. The note_duration and triplet inputs were also attached to the switches on the FPGA, for the same reason as the bpm input, allowing us to do a full test of the circuit. Internally, we included two components: the Tempo and note_timer circuits. Using bpm as an input to the Tempo component we were able to use the tempo_enable output and connect it to the tempo_enable signal of the note_timer circuit. This allowed for the final desired output of TRIGGER to be set to a LED, location on the Altera DE1 board. By adjusting the three inputs bpm, triplet and note_duration by using the switches we were able to test many different inputs that yielded correct results as confirmed by the TA.

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Timing Performance and Resource Utilization

For the note_timer circuit our timing performance and Resource Utilization were as follows:

Flow Status	Successful - Sun Apr 05 16:21:40 2015
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Full Version
Revision Name	g48_Lab4
Top-level Entity Name	g48_note_timer
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Met timing requirements	Yes
Total logic elements	41 / 18,752 (< 1 %)
Total combinational functions	41 / 18,752 (< 1 %)
Dedicated logic registers	10 / 18,752 (< 1 %)
Total registers	10
Total pins	17 / 315 (5 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tsu	N/A	None	11.222 ns	note_duration[0]	count[2]	--	clk	0
2	Worst-case tco	N/A	None	8.536 ns	TRIGGER~reg0	TRIGGER	clk	--	0
3	Worst-case th	N/A	None	-4.393 ns	tempo_enable	count[0]	--	clk	0
4	Clock Setup: 'clk'	N/A	None	250.82 MHz (period = 3.987 ns)	count[1]	count[2]	clk	clk	0
5	Total number of failed paths								0

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For the note_timer_testbed circuit our timing performance and Resource Utilization were as follows:

Flow Status	Successful - Sun Apr 05 16:14:17 2015
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Full Version
Revision Name	g48_Lab4
Top-level Entity Name	g48_note_timer_testbed
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Met timing requirements	Yes
Total logic elements	70 / 18,752 (< 1 %)
Total combinational functions	70 / 18,752 (< 1 %)
Dedicated logic registers	32 / 18,752 (< 1 %)
Total registers	32
Total pins	24 / 315 (8 %)
Total virtual pins	0
Total memory bits	5,632 / 239,616 (2 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tsu	N/A	None	11.242 ns	triplet	g48_note_timer:timer|count[6]	--	clk	0
2	Worst-case tco	N/A	None	10.144 ns	g48_note_timer:timer|count[2]	count_out[2]	clk	--	0
3	Worst-case th	N/A	None	-3.581 ns	bpm[6]	g48_Tempo:tempo|lpm_rom:temp...	--	clk	0
4	Clock Setup: 'clk'	N/A	None	163.11 MHz (period = 6.131 ns)	g48_Tempo:tempo|lpm_rom:tempo...	g48_Tempo:tempo|lpm_counter:l...	clk	clk	0
5	Total number of failed paths								0

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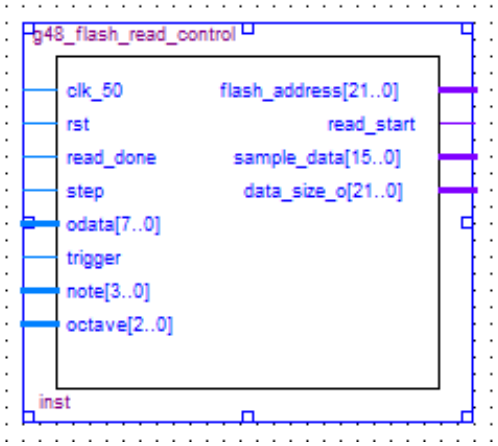
g48_flash_read_control:

Description:

The flash_read_control provided in the lab allows us to interact with the Flash memory chip on our Altera board. The g48_flash_read_control circuit is designed to read a 16-bit wave data from the flash memory, and play it back to the user as a mono audio output via the AUDIO_OUT on the board.

Initially, the circuit modification we implemented was to help read the wave data provided to the circuit. The first modification we made was to wait until the step signal went low. Once this happened we loaded the appropriate address and waited until the step went high and the previous read was complete. Once this happened we signalled for the read to begin, once this was completed and the read was done, the data was loaded into sample_data and the address incremented. After this step the second read was performed, once complete the data was loaded and the address was incremented. Finally we return to our first modification (state = 6) to start the next data read sequence until the wavefile reaches its end.



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Testing, Timing Performance and Resource Utilization

Testing for the g48_flash_read_control circuit was performed on the Altera DE1 board using a testbed circuit called g48_Sound_Testbed. The note and octave inputs of this testbed were connected to switches to allow for testing of several different pitches and notes. The flash_read_control was used as a component for reading the data of the provided wavefile, which was a guitar strum. The testing was done by changing the input values through the use of switches, our tests were successful and our outputs were verified by the TA.

The timing performance and resource utilization of the g48_Sound_Testbed are as follows:

Flow Status	Successful - Sun Apr 05 17:08:36 2015
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Full Version
Revision Name	g48_Lab4
Top-level Entity Name	g48_Sound_Testbed
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Met timing requirements	Yes
Total logic elements	568 / 18,752 (3 %)
Total combinational functions	496 / 18,752 (3 %)
Dedicated logic registers	309 / 18,752 (2 %)
Total registers	309
Total pins	73 / 315 (23 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tsu	N/A	None	10.233 ns	note[0]	g48_flash_read_control:readFlas...	--	clk_50	0
2	Worst-case tco	N/A	None	9.795 ns	g48_flash_read_control:readFlash|...	data_size_o[8]	clk_50	--	0
3	Worst-case th	N/A	None	-0.159 ns	octave[2]	g48_flash_read_control:readFlas...	--	clk_50	0
4	Clock Setup: 'clk_50'	N/A	None	134.39 MHz (period = 7.441 ns)	g48_flash_read_control:readFlash|...	g48_flash_read_control:readFlas...	clk_50	clk_50	0
5	Total number of failed paths								0

Grade Sheet for Lab #4

Winter 2015.

Group Number: 48

Group Member Name: Stephen Carter. Student Number: 260500858

Group Member Name: Greg Rohlicek. Student Number: 260516980

Marks			TA Signatures
2	1.	VHDL description of the note timer circuit	
2	2.	Simulation of the note timer circuit	
2	3.	Testing of the note timer circuit on the Altera DE1 board	
2	4.	Observing the wave data section size on the control panel	
2	5.	Reading the wave data section size on the Altera DE1 board	
2	6.	Modified VHDL code for the flash read control module	
2	7.	Playback of the wave on the Altera DE1 board	

Each part should be demonstrated to one of the TAs who will then give a grade and sign the grade sheet. Grades for each part will be either 0, 1, or 2. A mark of 2 will be given if everything is done correctly. A grade of 1 will be given if there are significant problems, but an attempt was made. A grade of 0 will be given for parts that were not done at all, or for which there is no TA signature.

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