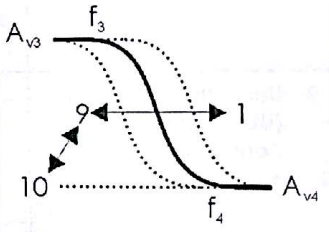
10.2.2 Description of Operator Controls

1 ON/OFF Switch	The ON/OFF Switch controls the power supply of the entire FALC 110 circuit.
2 Input Offset Range Selector • DIP-switch	Switch 1 and 2 on (left position): input offset adjust range is -2...+2 V at input gain (4) =1 Switch 1 and 2 off (right position): input offset adjust range is -0.2...+0.2 V at input gain (4) =1
3 Input Offset Adjust • Trimpot	Turn clockwise to rise input offset; adjustment range is set by DIP-switch (2). Input Section Gain Formula: $(V_{noninv\text{-}input} - V_{inv\text{-}input}) \times$ Input gain + Input offset
4 Input Gain (IG) Adjust • Trimpot	Turn clockwise to rise input gain. The voltage gain of the input section can be adjusted between 1 and 10. Input Section Gain Formula: $(V_{noninv\text{-}input} - V_{inv\text{-}input}) \times$ Input gain + Input offset **NOTE !** Rising the input gain above 1 affects the performance of the fast circuit branch in the MHz range (See Figure 103 and Figure 104). Therefore, always start a new FALC 110 adjustment procedure with minimum input gain (turn trimpot (4) more than 15 turns counter-clockwise to ensure an IG of 1)
5 Slow Limited Integrator (SLI) Adjust • DIP-switch	The SLI is the lag-lead filter element of the fast circuit branch that covers the lower frequency range. The SLI is connected in series with other filter elements. For calculation of the total gain from the inputs to the main output please refer to Figure 89. DIP switch positions at the front panel: left position = on, right position = off A_V = voltage amplification

SLI Corner Frequency Table

	A_{V3} = 37 dB	A_{V4} = 1.6 dB
Switch # on	f_3/Hz	f_4/Hz
1	5k	300k
2	2.4k	140k
3	1.1k	65k
4	500	30k
5	240	14k
6	110	6.5k
7	50	3k
8	24	1.4k
9	11	650
10	flat level A_{V4} (noted *)	



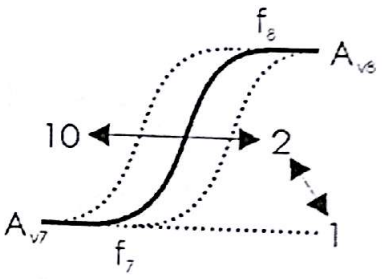
10 Fast Limited Differentiator (FLD) Adjust

- DIP-switch

The FLD is the lead-lag filter element of the fast circuit branch that covers the highest frequency range. The FLD is connected in series with other filter elements. For calculation of the total gain from the inputs to the main output please refer to Figure 89.

DIP switch positions at the front panel: left position = on, right position = off
A_V = voltage amplification

FLD Corner Frequency Table		
	A_{v7} = 0 dB	A_{v8} = 15 dB
Switch # on	f_7/Hz	f_8/Hz
1	flat level A_{v7} (noted °)	
2	8.5M	*
3	4.2M	*
4	1.9M	*
5	900k	4.8M
6	420k	2.3M
7	190k	1M
8	90k	480k
9	42k	230k
10	19k	100k



* At these FLD settings there does not exist a clearly visible upper corner frequency in the transfer function, because at 10 MHz and above the overall bandwidth limit of the FALC 110 interferes with the ideal FLD curve. Refer to Figure 94, Figure 95 and Figure 96 to view network analysis graphs of the actual high frequency behavior of the FLD.

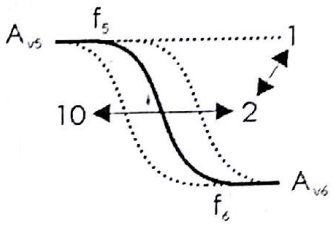
NOTE ! Only one DIP switch element should be in the ON position at a time. However, intermediate values between the corner frequencies listed in the table can be achieved by switching on more than one DIP switch element: Switching on the next lower number switch in addition to a certain switch will lower both corner frequencies to an intermediate value.

11 Fast Limited Integrator (FLI) Adjust
- DIP-switch

The FLI is the lag-lead filter element of the fast circuit branch that covers the high frequency range. The FLI is connected in series with other filter elements. For calculation of the total gain from the inputs to the main output please refer to Figure 89.

DIP switch positions at the front panel: left position = on, right position = off
A_V = voltage amplification

FLI Corner Frequency Table		
	A_{V5} = 0 dB	A_{V6} = 15 dB
Switch # on	f_5/Hz	f_6/Hz
1	flat level A_{V5} (noted °)*	
2	650k	7.5M
3	300k	3.5M
4	140k	1.6M
5	65k	800k
6	30k	370k
7	14k	170k
8	6.5k	80k
9	3k	37k
10	1.4k	100k



* This setting enables an entirely flat frequency response of the fast circuit branch in conjunction with the 'flat' settings of the other filter elements (FLD = 1, SLI = 10, XSLI = 6). However, this response has a reduced bandwidth (below 10 MHz), refer to Figure 93 for a graph.

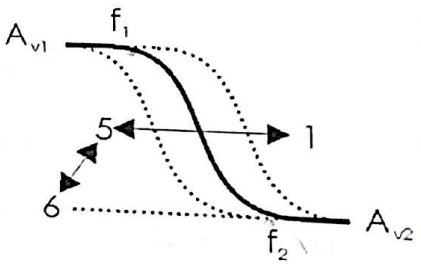
NOTE ! Only one DIP switch element should be in the ON position at a time. However, intermediate values between the corner frequencies listed in the table can be achieved by switching on more than one DIP switch element: Switching on the next lower number switch in addition to a certain switch will lower both corner frequencies to an intermediate value.

12 Extra Slow Limited Integrator (XSLI) Adjust
- DIP-switch

The XSLI is the lag-lead filter element of the fast circuit branch that covers the lowest frequency range. Activation of the XSLI together with SLI and FLI is recommended to achieve maximum DC gain for control loops that use only the fast circuit branch. The XSLI is connected in series with other filter elements. For calculation of the total gain from the inputs to the main output please refer to Figure 89.

DIP switch positions at the front panel: left position = on, right position = off
A_V = voltage amplification

XSLI Corner Frequency Table		
	A_{v1} = 26 dB	A_{v2} = 0 dB
Switch # on	f_1/Hz	f_2/Hz
1	90	2000
2	25	600
3	9	200
4	2.5	60
5	0.9	20
6	flat level A_{v2} (noted °)	



NOTE ! Only one DIP switch element should be in the ON position at a time. However, intermediate values between the corner frequencies listed in the table can be achieved by switching on more than one DIP switch element: Switching on the next lower number switch in addition to a certain switch will lower both corner frequencies to an intermediate value.

13 Main Gain (MG) Adjust
- Potentiometer

The main gain potentiometer controls the output scaling of the main output (16).
The voltage gain can be adjusted between 0 and 1 like a volume control. It is used to tune in the correct overall gain of the fast circuit path, starting from zero.

14 Unlimited Integrator (ULI) Output
- BNC-connector

Low-speed output of the unlimited integrator
age range of +/- 5 V. It is int

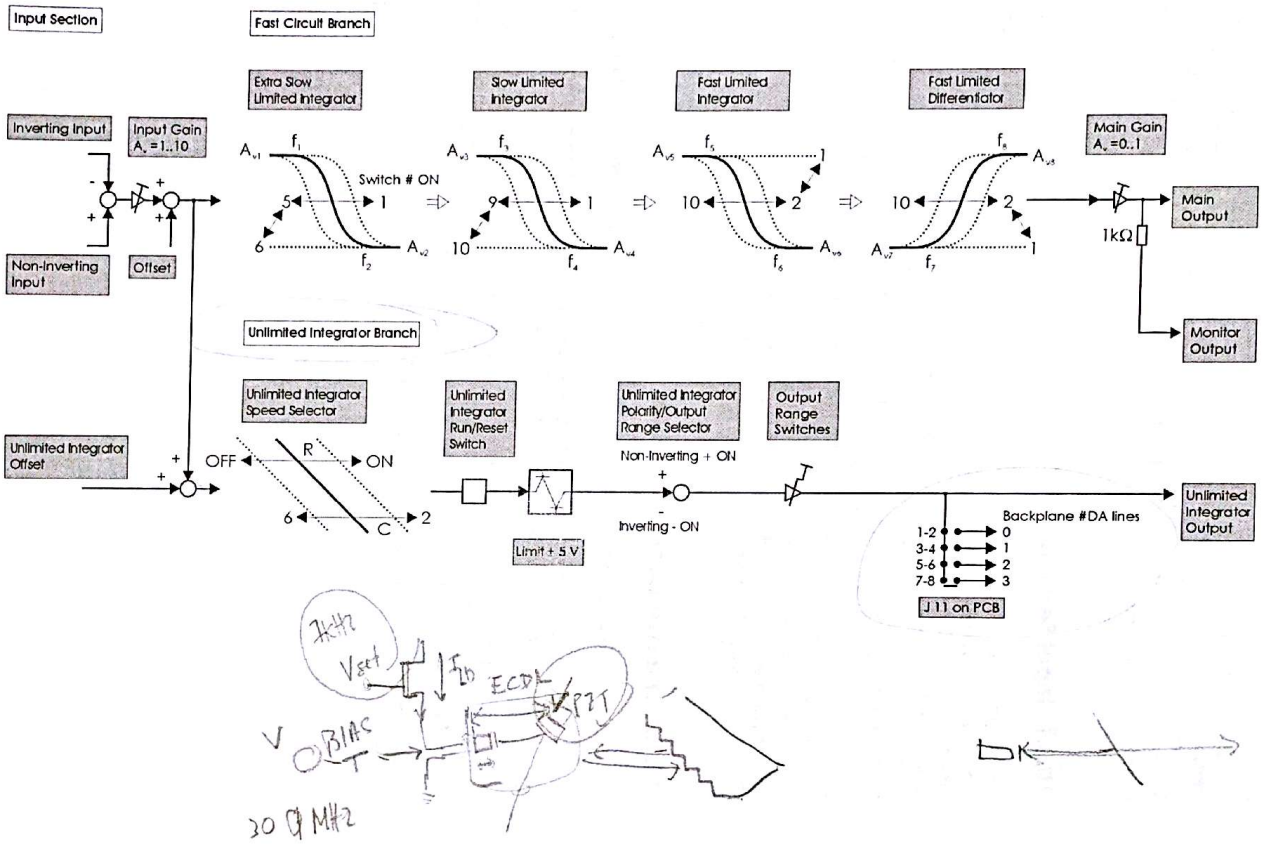


Figure 89 FALC 110 Block Diagram

10.3.2.1 Description of the Fast Circuit Branch

The principle of the FALC 110 transfer function adjustment is different from the PID 110 and other control amplifiers.

The overall transfer function of the fast circuit branch is set by configuring three different lag-lead filter stages (called Limited Integrators: Extra Slow, Slow and Fast) and a lead-lag filter (called Fast Limited Differentiator).

The filter stages have gain levels that usually stay fixed (for gain adjustment see Paragraph 10.3.2.2). The gain slopes of the individual filter stages are shifted along the frequency axis by setting the DIP switches. Further, all filter stages can be disabled (i.e. set to a flat frequency response at a certain gain) individually.

The main focus is on the integrating part of the transfer function, as the frequency noise of diode lasers commonly decreases with frequency. The differentiator allows for phase advance in the control loop at high frequencies.

Figure 3 shows the transfer function from the non-inverting input to the main output of the FALC 110 with a typical setup of the fast branch parameters. Two of three integrators and the differentiator are running. The integrator slopes need not to be set consecutively; they also may overlap or have gaps between them that cause plateau sections along the magnitude curve. This allows for advanced control of the phase.

In Figure 90, the slight gap between SLI and FLI reduces the phase lag from -90 to -60 degrees around 100 kHz.

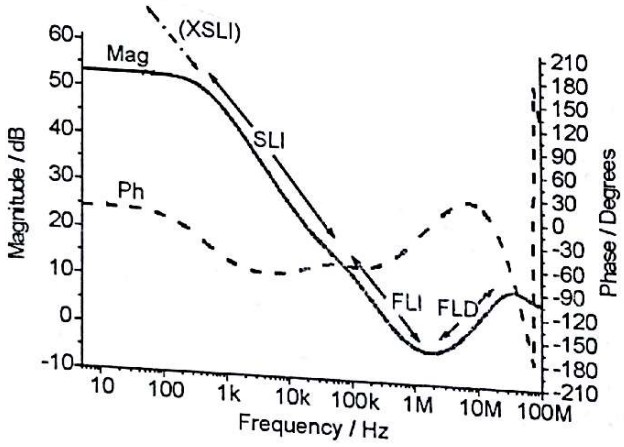


Figure 90 Typical Bode plot of the FALC 110 fast circuit branch with responsible filter stages, taken from actual FALC 110 network analysis. Settings: **IG=1 XSLI=6 SLI=4 FLI=5 FLD=3 MG=1**