Introduction

Error Correction Code (ECC) is a function used to detect and remove data corruption in code or data flash memory.

This document describes how to use ECC on ABOV 32-bit microcontrollers and important ECC-related issues you should know before using ECC.

The basic examples and explanations in this document are based on the A33G53x. For basic examples and explanations for other devices, refer to the documentation for those devices.

This document applies to products with part numbers listed in Table 1.

Table 1. Applicable Devices

Base Product	Part Number
A33G53x	A33G539VQ, A33G539VL, A33G539MM, A33G539RL, A33G538VQ, A33G538VL, A33G538MM, A33G538RL
A34M420	A34M420YL, A34M420VL, A34M420RL
A34L716	A34L716VL, A34L716RL

Reference Document

The following documents are available on www.abovsemi.com.

- Datasheets for products in Table 1
- User's Manuals for products in Table 1

Contents

List of Tables

List of Figures

1. Error Correction Code (ECC)

1.1 Introduction

Error Correction Code (ECC) is constructed based on a class of optimal minimum odd-weighted error parity code that performs better than Sigle Error Correction, Double Error Detection (SECDED), based on the Hamming code theory. Using ECC improves protection against bit flipping in flash memory.

By default, when writing words (32-bit) to the code flash area or data flash area, normal ECC parity (7-bit) is generated for each word. The parity bits are unreadable.

It is possible to detect single-bit or double-bit errors by comparing the generated parity bits to the words in the code flash or data flash area when reading the flash memory and to prevent them. The ECC Controller can correct single-bit errors, but double-bit errors are difficult to correct; therefore, additional software functions must be implemented using error flags.

Table 2 and Table 3 show each device's code and data flash memory information. For more information about each device in Table 1, refer to the appropriate documentation for the product.

Table 2. Code Flash Memory Summary

Device	Code Size	Start Address	End Address	Program Unit for ECC
A33G538	512 KB	0x0000_0000	0x0007_FFFF	4 bytes (1 word)
A33G539	768 KB	0x0000_0000	0x000B_FFFF	
A34M420	1024 KB	0x0000_0000	0x000F_FFFF	
A34L716	256 KB	0x0000_0000	0x0003_FFFF	

Table 3. Data Flash Memory Summary

Device	Data Size	Start Address	End Address	Program Unit for ECC
A33G538(1)	32 KB	0x0F00_0000	0x0F00_7FFF	4 bytes (1 word)
A33G539(1)				
A34M420	32 KB	0x0E00_0000	0x0E00_7FFF	4 bytes (1 word)
A34L716				

NOTES:

1. On the A33G53x, data flash memory can be programmed in 1-byte units, but ECC is not available in that case. To use ECC, the program unit must be 1-word.
2. To use ECC, each device's program unit must meet the conditions described in Table 2 and Table 3. If the device with ECC enabled operates with PGM units (ex, 1 byte, 2 byte, etc.) that do not match the conditions in Table 2 and Table 3, many ECC errors may occur.

1.2 Block Diagram

The ECC block stores the 39 bits, including the parity's 7 bits, in the flash memory via the encoder. Similarly, when reading, the decoder can verify that the values stored in the flash memory are not changed.

If ECC errors occur, ECC error information can be recorded via the decoder, as shown in the figures below (Figure 1 and Figure 2). The ECC register information, including the error information, is shown in Table 6 and Table 7,.

Figure 1. ECC Block Diagram (Code and Data Flash Memory: 1-word Read)

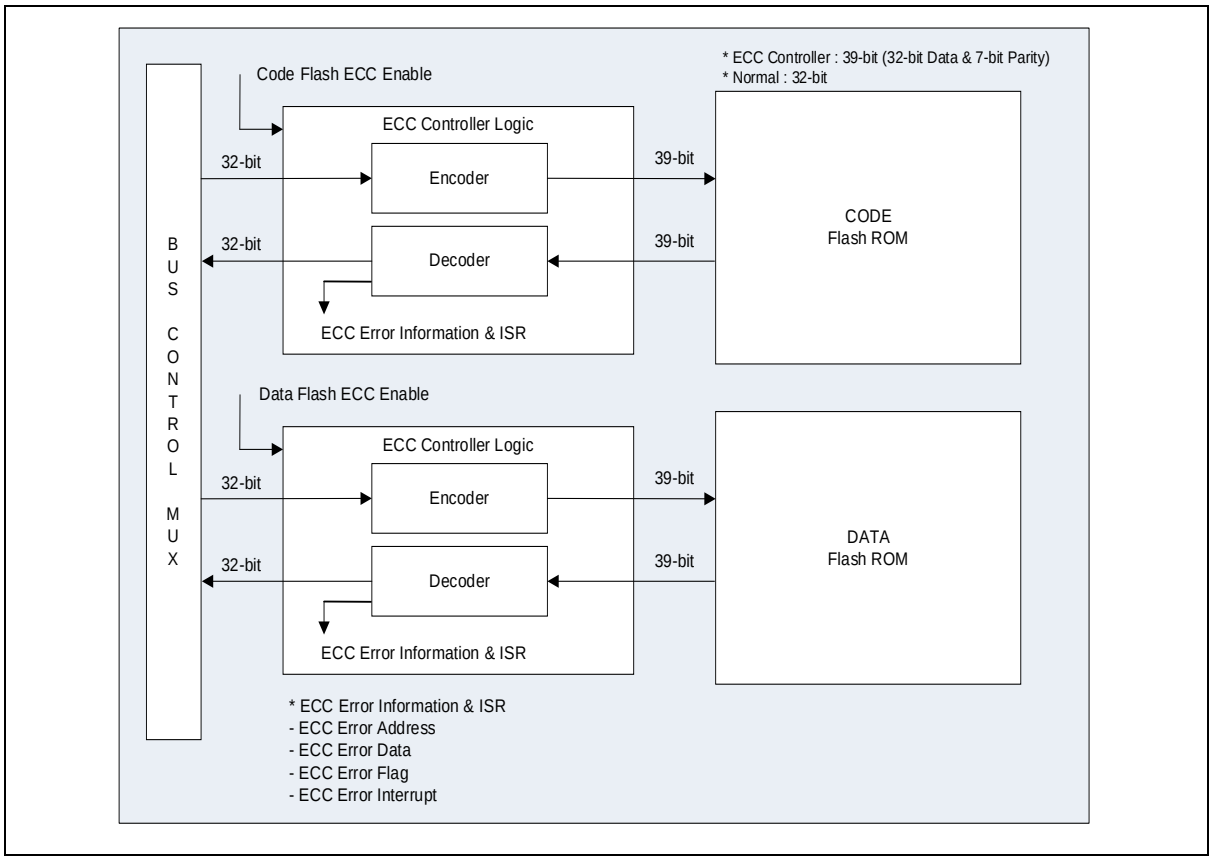


Table 4. Code and Data Flash Memory: 1-word Read Devices

Device	Part Number
A33G53x	A33G539VQ, A33G539VL, A33G539MM, A33G539RL A33G538VQ, A33G538VL, A33G538MM, A33G538RL

Figure 2. ECC Block Diagram (Code Flash: 4-word Read/ Data Flash: 1-word Read)

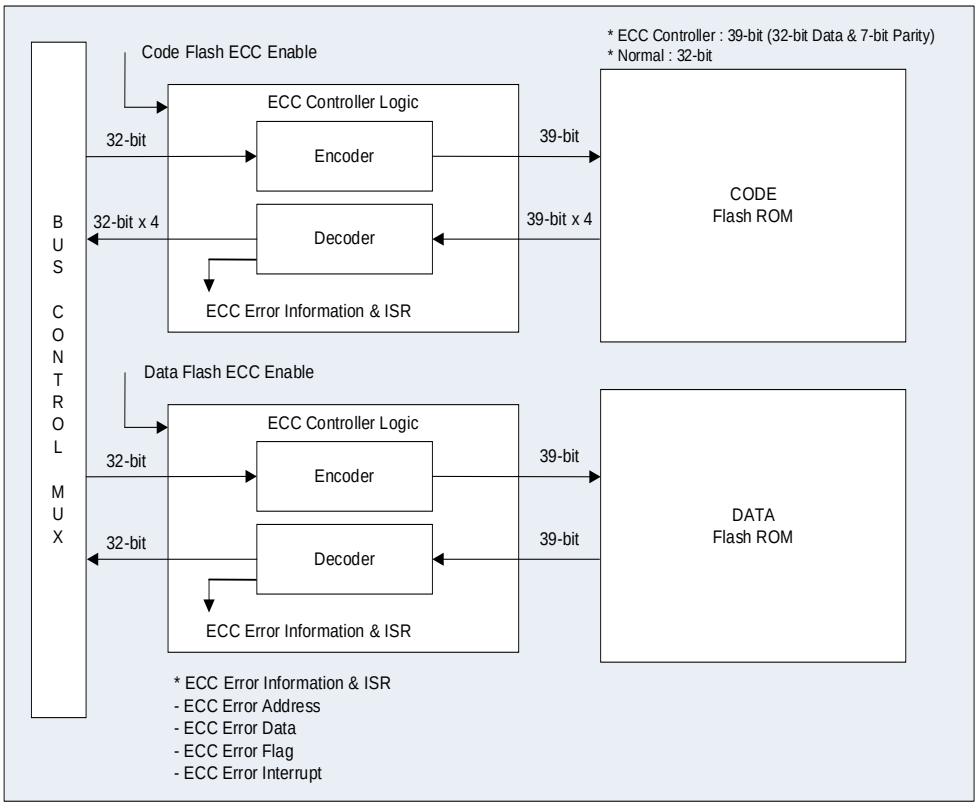


Table 5. Code Flash:4-word Read/ Data Flash: 1-word Read Devices

Device	Part Number
A34M420	A34M420YL, A34M420VL, A34M420RL
A34L716	A34L716VL, A34L716RL

1.3 ECC Interrupt Service Routine (ISR)

The ECC Interrupt Service Routine (ECC ISR) allows the microcontroller to handle ECC errors as soon as they occur. If an ECC error occurs with the ECC interrupt enabled, for example, the A33G53x's process branches into the flash memory Interrupt Service Routine (FMC ISR). For other devices' processes regarding ECC errors, refer to their respective User's Manual.

When reading the flash memory, the single-bit error is corrected automatically by the ECC controller, and the corrupted data value is also corrected. It is recommended that the corrected data be written to the address where the ECC error occurred. Other bits within the data word can be further corrupted later, resulting in a double-bit error occurrence. Therefore, when writing the corrected data, you must write to the area that contains the ECC error address in page units or sector units. For more information about the ECC operation sequence, refer to Figure 3.

Further data corruption may cause double-bit errors, making it difficult to correct the data because the ECC controller can correct single-bit errors but not double-bit errors, only showing the error flags.

Table 6 and Table 7 show the addresses of the ECC-related registers. For the information on the register map (for each product in Table 1), refer to the User's Manual of the product.

Table 6. Code Flash Memory ECC Information

Device	Address	Data	Error Interrupt	Error Flag
A33G53x	0x4000_0164	0x4000_0168	0x4000_0180	0x4000_0184
A34M420	0x4100_0060	0x4100_0064 0x4100_0068 0x4100_006C 0x4100_0070	0x4100_0018	0x4100_001C
A34L716				

Table 7. Data Flash Memory ECC Information

Device	Address	Data	Error Interrupt	Error Flag
A33G53x	0x4000_0170	0x4000_0174	0x4000_0180	0x4000_0184
A34M420	0x4100_1050	0x4100_1054	0x4100_1014	0x4100_0018
A34L716				

If an ECC error occurs when reading the flash in 1-word units, the ECC error is stored at the ECC error address.

On the other hand, if an ECC error occurs while reading the flash in 4-word units, xxxx_xxx0 of the read address is stored at the ECC error address, and the data is stored at the location of ECC error data 0, 1, 2, or 3 according to the stored ECC error address.

Table 8. How To Determine Address of ECC Error When Reading in 1-word Units

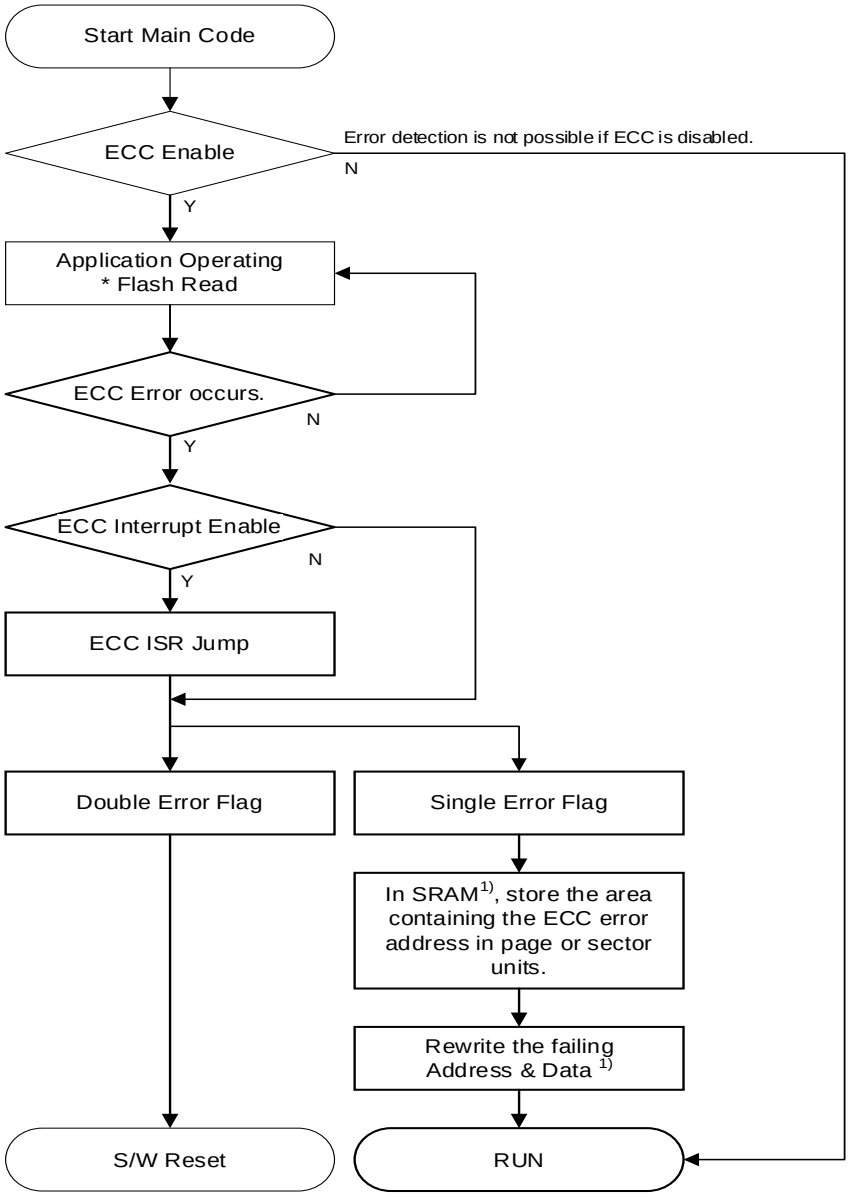
Read Address	ECC Error Address	ECC Error Data
0x0000_7000	0x0000_7000	ECC error data
0x0000_7004	0x0000_7004	ECC error data
0x0000_7008	0x0000_7008	ECC error data
0x0000_700C	0x0000_700C	ECC error data
0x0000_7010	0x0000_7010	ECC error data

Table 9. How To Determine Address of ECC Error When Reading in 4-word Units

Read Address	ECC Error Address	ECC Error Data
0x0000_7000	0x0000_7000	ECC error data 0
0x0000_7004	0x0000_7000	ECC error data 1
0x0000_7008	0x0000_7000	ECC error data 2
0x0000_700C	0x0000_7000	ECC error data 3
0x0000_7010	0x0000_7010	ECC error data 0

1.4 Sequence of ECC

Figure 3. Sequence of ECC



NOTES:

1. If single errors occur, check the ECC error address. Then in page or sector units, store the data of the address area in SRAM. Next, erase or write the address where the error occurred.
   For example, if an ECC error occurs at the address 0x7300, store the data in the address from 0x7200 to 0x73FF in SRAM. Next, erase or write SRAM from 0x7200 to 0x73FF.
2. If double errors occur, it is recommended to force termination because it is not possible to know which application is operating at the address where the error occurred, unless otherwise implemented in software.

1.5 Register Description (Example: A33G53x)

The interrupts described in this section are based on the A33G53x, and each device in Table 1 may have slightly different register and flag names. Therefore, for register and flag information specific to each device, refer to the corresponding User's Manual.

The ECC flag consists of two types: single error flag and double error flag. The ECC flags can generate FMC interrupts.

1.5.1 ECC for Code Flash Memory

Code flash ECC checks the integrity of code flash memory. A code flash ECC error occurs when a changed value is read from a code flash rather than the original value.

1.5.1.1 CECCSERR (Code Flash ECC Single Error Status)

This flag is set to '1' when the value of the code flash differs from the original value by only one bit and is corrected by the ECC Controller.

1.5.1.2 CECCDERR (Code Flash ECC Double Error Status)

This flag is set to '1' when the value of the code flash differs from the original value by more than two bits and is not corrected.

1.5.1.3 CECCIEN (Code Flash ECC Error Interrupt)

Setting this bit to '1' allows the FMC (Flash Memory Controller) interrupt to be generated when the Code Flash ECC Double Error (CECCDERR) flag or Code Flash ECC Single Error (CECCSERR) flag occurs.

1.5.2 ECC for Data Flash Memory

Data flash ECC checks the integrity of data flash memory. A data flash ECC error occurs when a changed value is read from a data flash rather than the original value.

1.5.2.1 DECCSERR (Data Flash ECC Single Error Status)

This flag is set to '1' when the value of the data flash differs from the original value by only 1 bit and is corrected by the ECC Controller.

1.5.2.2 DECCDERR (Data Flash ECC Double Error Status)

Setting this bit to '1' when the value of the data flash differs from the original value by more than 2 bits and is not corrected.

1.5.2.3 DECCIEN (Data Flash ECC Error Interrupt)

Setting this bit to '1' allows the FMC (Flash Memory Controller) interrupt to be generated when the Data Flash ECC Double Error (DECCDERR) flag or Data Flash ECC Single Error (DECCSERR) flag occurs.

1.5.3 FMC_IER: Flash Memory Interrupt Enable Register

The FMC_IER register is the internal flash memory's interrupt enable register. It is a 32-bit register.

FMC_IER=0x4000_0180

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13	12	11 10 9	8	7 6 5	4	3 2 1	0
Reserved			WDIEN	WEIEN	Reserved	BSEN	Reserved	DECCIEN	Reserved	CECCIEN
-			0	0	-	0	-	0	-	1
-			RW	RW	-	RW	-	RW	-	RW

4	DECCIEN	Data flash ECC error interrupt	
		0	Disable
		1	Enable
0	CECCIEN	Code flash ECC error interrupt	
		0	Disable
		1	Enable

1.5.4 FMC_ISR: Flash Memory Interrupt Status Register

The FMC_ISR register is the internal flash memory's interrupt status register. It is a 32-bit register.

FMC_ISR=0x4000_0184

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13	12	11 10 9	8	7 6	5	4	3 2	1	0
Reserved			WDF	WEF	Reserved	BSERR	Reserved	DECCDERR	DECCSERR	Reserved	CECCDERR	CECCSERR
-			0	0	-	0	-	0	0	-	0	1
-			WC	WC	-	WC	-	WC	WC	-	WC	WC

5	DECCDERR	Data flash ECC double error status	
		0	No Error
		1	Error (To clear the error flag bit, Write "1" to this bit.)
4	DECCSERR	Data flash ECC single Error status	
		0	No Error
		1	Error (To clear the error flag bit, Write "1" to this bit.)
1	CECCDERR	Code flash ECC double Error status	
		0	No Error
		1	Error (To clear the error flag bit, Write "1" to this bit.)
0	CECCSERR	Code flash ECC single Error status	
		0	No Error
		1	Error (To clear the error flag bit, Write "1" to this bit.)

1.6 Caution

1.6.1 Programming Results Depending on ECC Settings

When programming flash memory, ECC generation operates as shown in Table 2, depending on the ECC Enable bit.

Table 10. Programming Results Based on ECC Settings

Device	ECC Off	ECC On
A33G53x	ECC Parity generation: X	ECC Parity generation: O
A34M420	ECC Parity generation: O	ECC Parity generation: O
A34L716		

Users must enable ECC before programming the flash memory to use the ECC function. If the ECC function is turned off while programming the flash memory, the ECC parity bit will not be generated because the ECC controller is not activated.

Table 11 shows the results of reading flash memory after programming with each ECC setting.

Table 11. Read Results After Program depend on ECC Settings

Device	Program	ECC Off		ECC On	
	Read	ECC Off	ECC On	ECC Off	ECC On
A33G53x		Normal	ECC Error	Normal	Normal
A34M420		Normal	Normal	Normal	Normal
A34L716					

While using the A33G53x, programming the flash memory in the ECC-disable state followed by reading the flash memory in the ECC-enable state does not generate an ECC parity bit, as shown in Table 10. If the ECC controller decodes with an incorrect parity bit, more than one bit in the normal flash value may change, and therefore, a change of more than two bits will generate an ECC error flag.

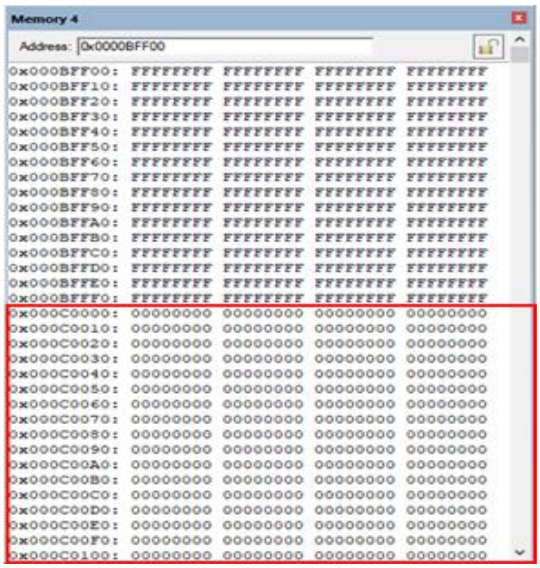
1.6.2 Debugger Memory Display (Debug Memory Window)

Opening a debug memory window for a non-code flash area with ECC enabled will generate the Code Flash ECC flag. Therefore, the non-code flash area should not be enabled.

Table 12. Access-Prohibited Area in Debug Memory Window When ECC Is Enabled

Device	Start Address	End Address
A33G539	0x000C_0000	0x000D_FFFF

Figure 4. Non-Code Flash Area (where Code Flash ECC Flag Occurs) in Debug Memory Window



Glossary

Table 13 lists the terms, abbreviations, and acronyms used in this document.

Table 13. Glossary of Terms, Abbreviations, and Acronyms

Term	Description
HCLK	High-Speed Clock
PCLK	Peripheral Clock
MCLK	Main Clock
LSI / RingOSC	Low-Speed Internal Oscillator
HSI	High-Speed Internal Oscillator
HSE	High-Speed External Oscillator
PLL	Phase-Locked Loop
XTAL	External Crystal Oscillator
SXTAL	External Sub-Crystal Oscillator
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
SCU	System Control Unit
MXOSC, HSE	External Main Oscillator
SXOSC, LSE	External Sub-Oscillator
ECC	Error Correction Code
FMC	Flash Memory Controller

Revision History

Revision	Date	Notes
1.00	Jan. 23, 2024	Initial release
1.01	May. 27, 2024	Added A34L716 device
1.02	Dec. 2, 2024	Updated the disclaimer.

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