Introduction

The purpose of this handbook is to help the system designers who implement hardware such as power supply, clock management, reset control, boot mode setting, and debug interfaces on the development board.

Specifically, this document provides hardware design guidelines to optimize the performance of user applications and minimize noise transmitted from the outside to the PCB.

This handbook applies to the products with part numbers listed in Table 1.

Table 1. Applicable Devices

Base Product	Part Number
A31G11x	A31G112GR, A31G112KN, A31G112KU, A31G112KY, A31G112LU, A31G112SQ, A31G112CL, A31G111GR, A31G111KN, A31G111KU, A31G111LU
A31G12x	A31G123ML, A31G123MM, A31G123RL, A31G123RM, A31G123RN, A31G123SQ, A31G123CL, A31G122ML, A31G122MM, A31G122RL, A31G122RM
A31G21x	A31G213CL, A31G213SQ, A31G213KN, A31G213GR, A31G212CL, A31G212SQ, A31G212KN, A31G212GR
A31G22x	A31G226ML, A31G226MM, A31G226RM, A31G226RL, A31G226RL A31G224ML, A31G224MM, A31G224RM, A31G224RL, A31G224RL
A31G31x	A31G316MM, A31G316ML, A31G316RM, A31G316RL, A31G314MM, A31G314ML, A31G314RM, A31G314RL, A31G314CL, A31G314CU, A31G314SN, A31G313RM, A31G313RL, A31G313CL, A31G313CU, A31G313SN
A31G32x	A31G323CL, A31G323RL, A31G324CL, A31G324CU, A31G324RL
A33G52x	A33G527RL, A33G527VL, A33G527VQ, A33G526MM, A33G526RL, A33G526RM, A33G526VL, A33G526VQ, A33G524ML, A33G524MM, A33G524RL, A33G524RM, A33G526ML
A33G53x	A33G539VQ, A33G539VL, A33G539MM, A33G539RL A33G538VQ, A33G538VL, A33G538MM, A33G538RL
A31T21x	A31T216RL, A31T216CL, A31T216SN, A31T214RL, A31T214CL, A31T214SN
A31M22x	A31M223CL, A31M223KN, A31M223GR
A33M11x	A33M116RL, A33M116RM, A33M116CL, A33M114RL, A33M114CL
A34M41x	A34M418YL, A34M418VL, A34M418RL, A34M416VL, A34M416RL, A34M414VL, A34M414RL
A34M420	A34M420YL, A34M420VL, A34M420RL
A34M456	A34M456VL, A34M456RL, A34M456RK
A34L716	A34L716VL, A34L716RL, A34L716JY
AC30M1x64	AC30M1464LBN, AC30M1364LBN, AC30M1364UB
AC33Mx064	AC33M4064(T), AC33M3064(T)
AC33Mx128	AC33M8128, AC33M8128L, AC33M6128L

Reference Document

The following documents are available on www.abovsemi.com.

- Datasheets for the 32-bit microcontrollers shown in Table 1.
- User's Manuals for the 32-bit microcontrollers shown in Table 1.

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1. Filter and Bypass Capacitor

1.1 Filter Capacitor: EC1 (Electrolytic Capacitor)

- To reduce external noise, such as EFT, it is recommended to place a capacitor at a power source.
- When using an electrolytic capacitor with leads, the Equivalent Series Inductance (ESL) and Equivalent Series Resistance (ESR) values are typically high, resulting in a lower Self Resonant Frequency (SRF).
- Using a filter capacitor EC1 is recommended to prevent low frequency noise. It should be placed close to the power pins (within 30 mm) rather than close to a microcontroller.

1.2 Bypass Capacitor: C1 and C2

- To reduce high-frequency noise, it is recommended to place ceramic capacitors at a power source.
- For decoupling purposes, two hundred times different capacitors can be used instead of 100 nF capacitor.
- The bypass capacitors should be placed as close as possible to the microcontroller's power pins (within 10 mm) as they block high-frequency noise.
- The purpose of using 1 µF and 10 nF capacitors in parallel instead of 100 nF is to improve the stability of the power supply and effectively eliminate noise that may occur in a wide frequency range. In addition, a 22 µF capacitor can be connected in parallel to stabilize the lower frequency range and large fluctuations in the power supply.
  - High-frequency filtering (10 nF): Small-capacity capacitors provide low impedance at high frequencies, effectively eliminating high-frequency noise.
  - Low-pass filtering (1 µF): Large capacitors provide low impedance at low frequencies, which helps eliminate low-frequency noise and smooth out power supply fluctuations.
- Why the capacitances of C1 and C2 are 100 times different?
  - Frequency range coverage
    - Small capacitors work at high frequencies, while large capacitors work at low frequencies. If the capacitance difference is about 100 times, the two capacitors can complement each other and cover a very wide frequency range. For example, a 10 nF capacitor is effective at high frequencies above several MHz, while a 1 µF capacitor is effective at low frequencies below several kHz.
  - Prevent resonance phenomenon
    - Using capacitors of the same capacity in parallel can cause resonance at a certain frequency. Using two capacitors of significantly different capacitance in parallel can reduce this resonance.

Table 2. Filter and Bypass Component Value

Item	Component	Value
Bypass capacitor (decoupling)	C1	10 nF to 100 nF
	C2	100 times capacitance of C1
Filter capacitor	EC1	Typ. 22 µF

Figure 1. Filter and Bypass Capacitor Design Diagram

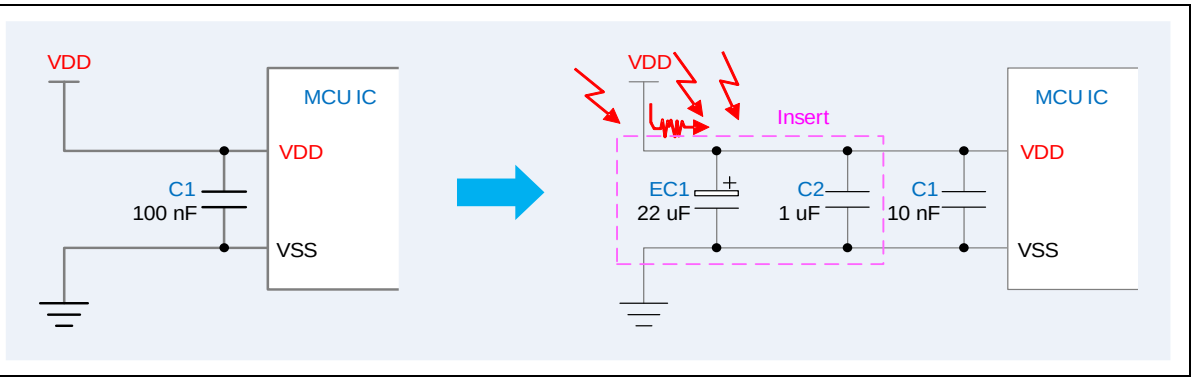
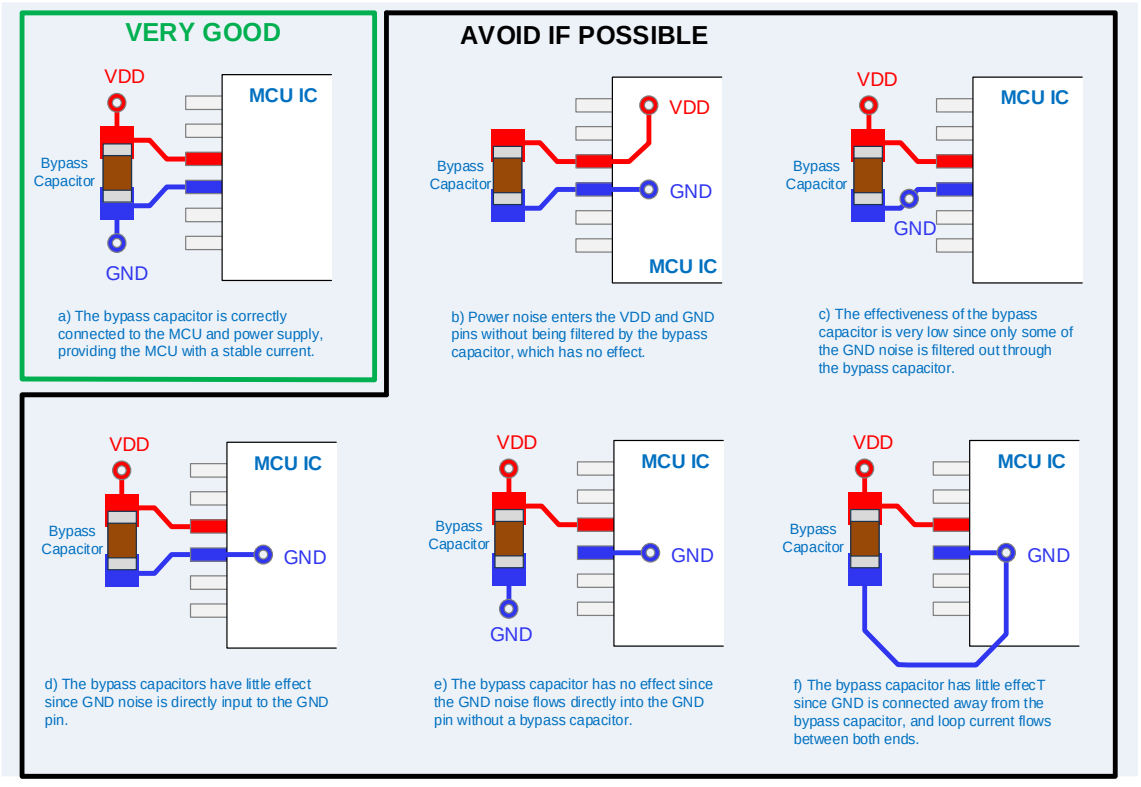


Figure 2. Examples of Bypass Capacitor Placement



2. Reset Pin

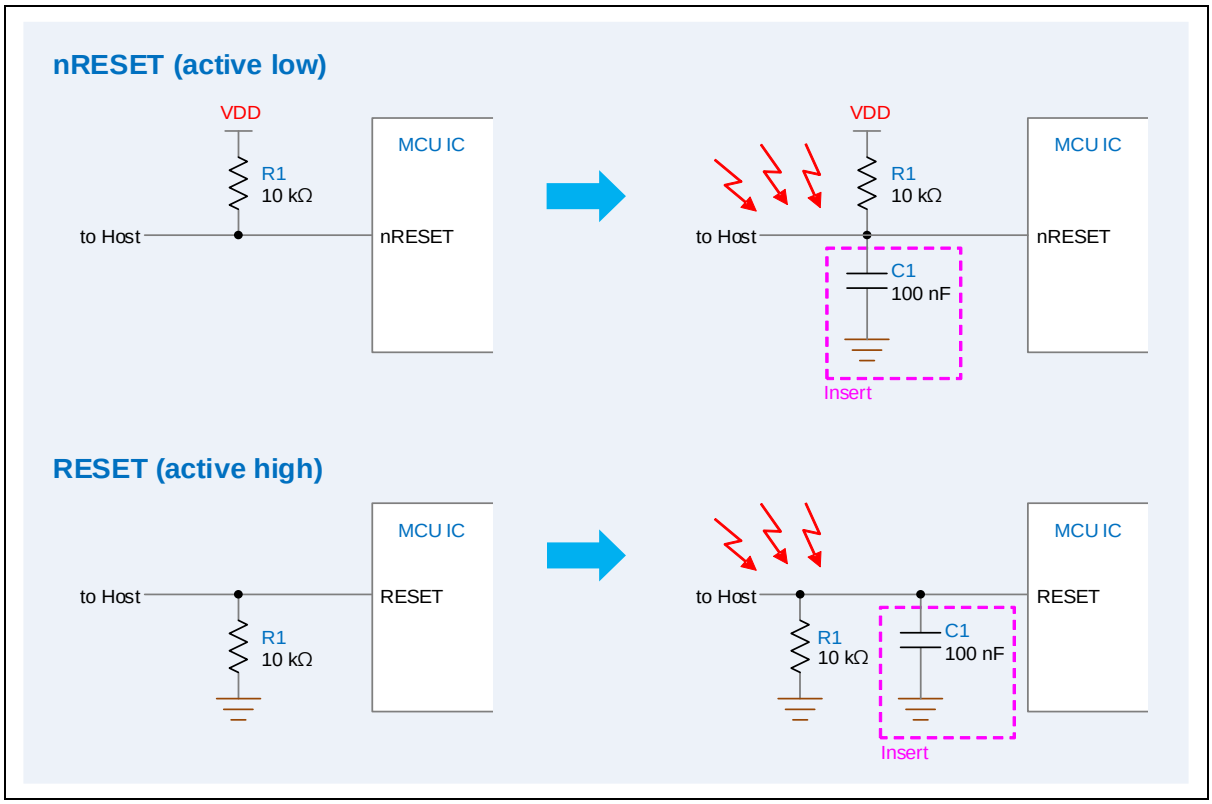
2.1 Filters Used on a Reset Pin

- For stable operations, resistors and capacitors must be placed on a reset pin, regardless of whether a reset pin is used.
- A circuit selection should carefully consider the characteristics of the reset pin.

Table 3. Reset Pin Component Value

Item	Component	Value
Pull-up resistor (for active high) pull-down resistor (for active low)	R1	10 kΩ
Filter capacitor	C1	Typ. 100 nF

Figure 3. Filters Used on a Reset Pin Diagram



3. Boot Pin

3.1 Pull-Up / Pull-Down Resistor on a Boot Pin

- For stable operations, resistors must be placed on a boot pin, regardless of whether a boot pin is used.
- Do not connect a filter capacitor to the boot pin.

Depending on the device, the boot pins may have different configurations of pull-up or pull-down resistor. Please refer to Table 5.

Table 4. Boot Pin Component Values

Item	Component	Value
Pull-up, pull-down resistor	R1	10 kΩ

Figure 4. Pull-Up and Pull-Down Resistor Used on a Boot Pin Diagram

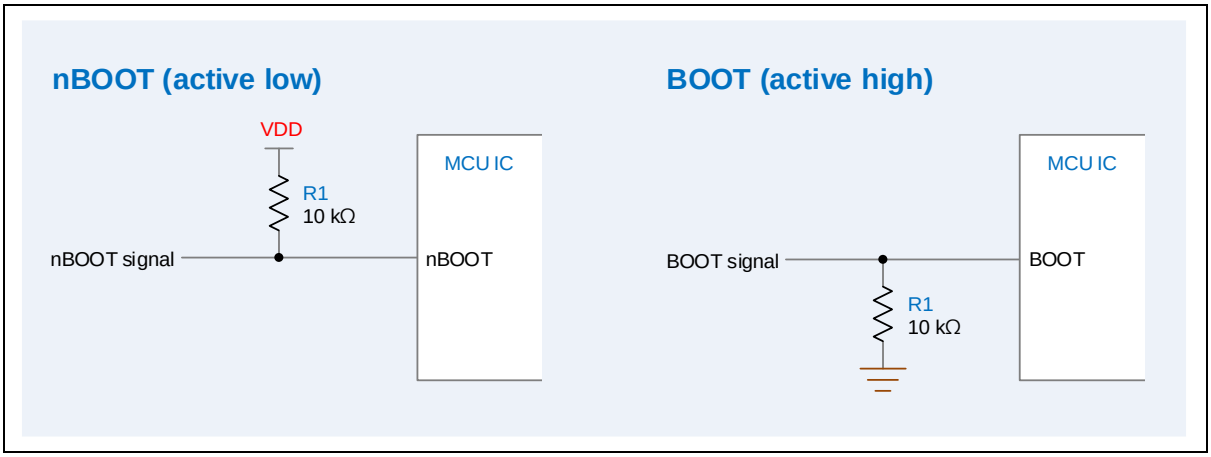


Table 5. External Pull-up or Pull-down Resistors for the BOOT Pin

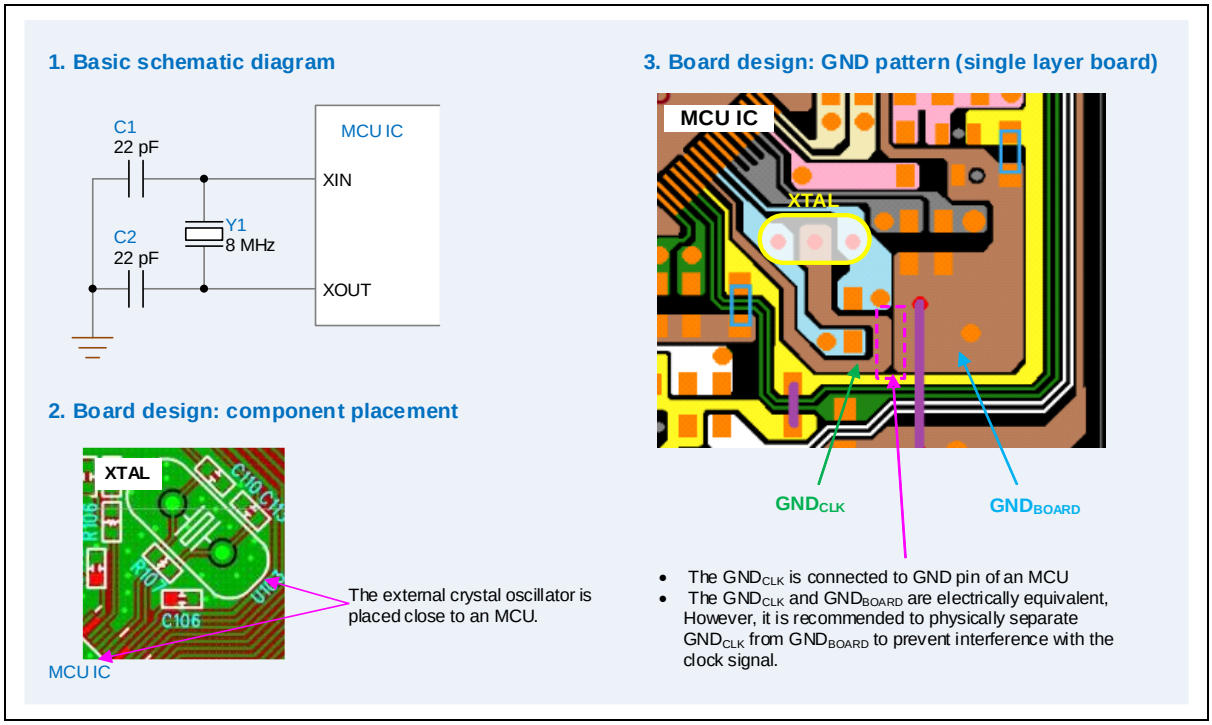
Device	BOOT pin	Boot Mode Condition
A31G11x	Pull-up, 10 kΩ	Active low
A31G12x	Pull-up, 10 kΩ	Active low
A31G21x	Pull-up, 10 kΩ	Active low
A31G31x	Pull-up, 10 kΩ	Active low
A31G22x	Pull-up, 10 kΩ	Active low
A33G52x	Pull-down, 10 kΩ	Active high
A33G53x	Pull-down, 10 kΩ	Active high
A31T21x	Pull-up, 10 kΩ	Active low
A31M22x	Pull-up, 10 kΩ	Active low
A33M11x	Pull-up, 10 kΩ	Active low
A34M41x	Pull-up, 10 kΩ	Active low
A34M420	Pull-up, 10 kΩ	Active low
A34M456	Pull-up, 10 kΩ	Active low
A34L716	Pull-up, 10 kΩ	Active low
AC30M1x64	Pull-up, 10 kΩ	Active low
AC33Mx064	Pull-up, 10 kΩ	Active low
AC33Mx128	Pull-up, 10 kΩ	Active low

4. External Clock

4.1 GND Shielding

- When using an external clock source, such as a crystal oscillator or ceramic resonator, it is recommended to create a ground shielding pattern (also known as a ground guard) around the clock source's XIN and XOUT lines.
  - This pattern helps to minimize EMI emissions and the effects of external noise.
  - To ensure proper operation, the clock source's ground pin and a microcontroller's ground pin should be connected correctly. If a ground connection is made to a different layer, it can create an inflow route of external noise, which can generate unwanted oscillation and offset the clock signal.

Figure 5. GND Shielding Diagram



- Placing feedback resistors on XTAL and Sub-XTAL is not recommended.

4.2 Reduce External Noise

- To improve the immunity to external noise of XTAL, you can select the current capability and noise filter of HSE (XTAL) and LSE (Sub-XTAL) in the EOSCR register of SCU (System Control Unit).
- The tables below show the noise filter selection values based on the A34M41x. You should refer to the manual for each device to set them accordingly.

Table 6. HSEISEL and HSENFSEL

Value (Bit)	HSENFSEL (noise filter)	HSEISEL (current capability)
00	23 ns	12 MHz < f_{OUT} ≤ 16 MHz
01	18 ns	8 MHz < f_{OUT} ≤ 12 MHz
10	13 ns	4 MHz < f_{OUT} ≤ 8 MHz
11	8 ns	1 MHz < f_{OUT} ≤ 4 MHz

Table 7. External Oscillator Control Settings

Frequency (MHz)	HSENFSEL	HSEISEL	NC delay (ns)
4	00	11	23
8	01	10	18
12	10	01	13
16	11	00	8

5. Debugging Interface

5.1 JTAG Interface

- JTAG interface is used for downloading and debugging the ABOV 32-bit microcontroller.
  - Table 8 shows a list of devices that support the JTAG interface.
- When using the JTAG interface, a pull-up or pull-down resistor must conform to the specifications shown in Table 8.

Table 8. JTAG Interface Resistor Value

Device	nTRST(1)	TDI(2)	TMS(2)	TCK(2)	TDO(2)
A33G52x, A33G53x	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 1 MΩ
A34M41x	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 1 MΩ
A34M420	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 1 MΩ
A34L716	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 1 MΩ
AC33Mx064	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 1 MΩ
AC33Mx128	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 10 kΩ	Pull-up, 1 MΩ

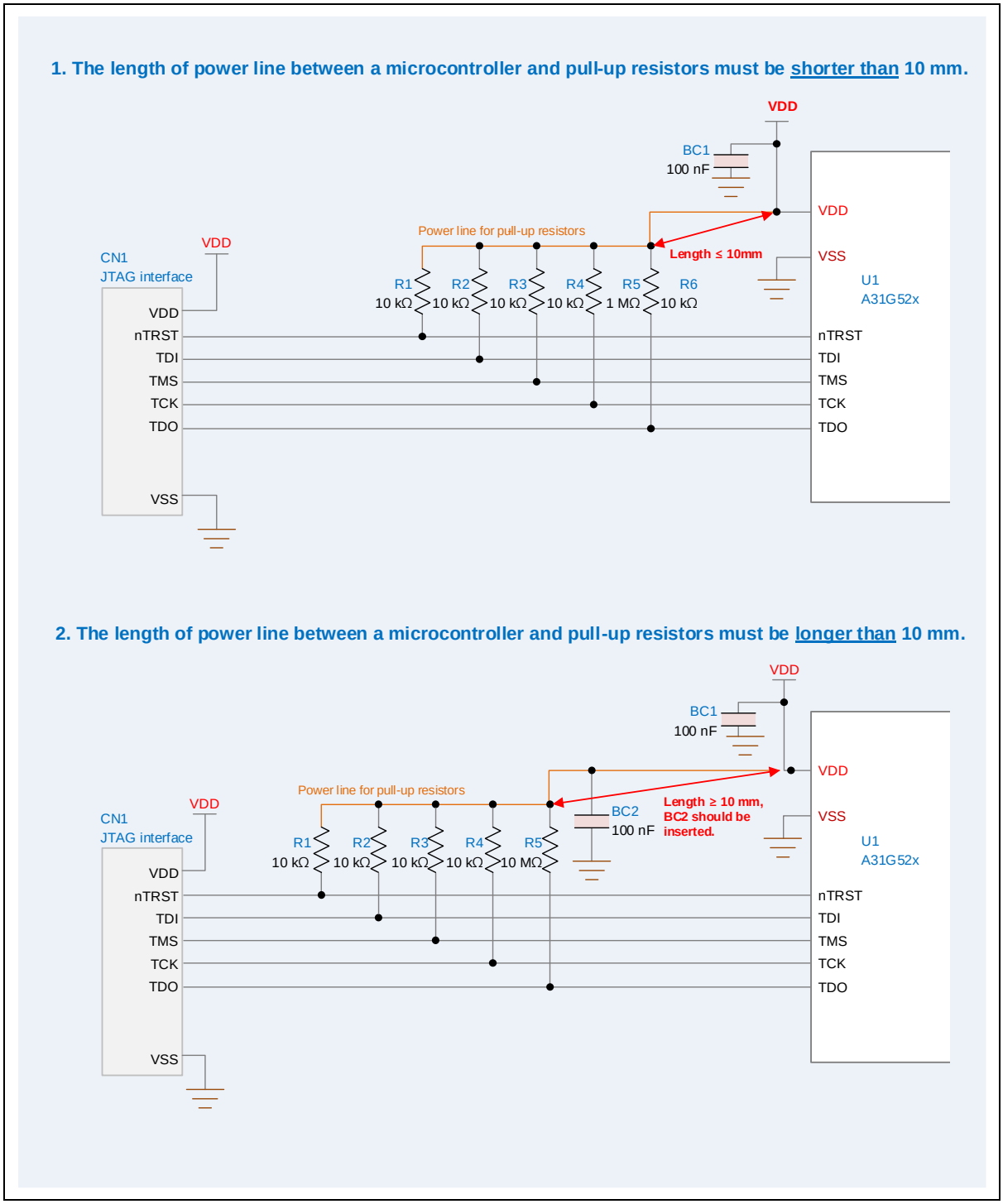
NOTES:

1. When the nTRST pin is connected to GND, the JTAG interface is disabled.
2. The application can set the JTAG pins (TDI, TMS, TCK, TDO) to alternative functions. To debug the target microcontroller when the JTAG pins are set to other alternative functions, the microcontroller must be restarted in boot mode using the BOOT pin and nRESET pin, and then the JTAG pins are initialized to TDI, TMS, TCK, and TDO. Therefore, the nRESET and BOOT pin of the target microcontroller should be considered when designing JTAG interface circuits. (Refer to section 2 and section 3.)

- After the development stage, if the JTAG pins are left unconnected, they may be affected by external noise. Therefore, production boards require the pull-up and the pull-down resistors to be installed.
- As a reference, a device that supports the JTAG interface is described in the following page:
  - If a device's interface is left unconnected during development, the firmware can later configure it to output a low or high signal. Therefore, it is acceptable to set the unused interface pin to NC.
- Resistors should be placed close to the JTAG pins (within 10 mm).
- Pull-up resistor power must be connected to the microcontroller's VDD power.
- Suppose the power connection of the pull-up resistor is located more than 10 mm away from the microcontroller's VDD power. In that case, it is recommended to add a 0.1 µF bypass capacitor between the microcontroller's VDD pin and ground. It is also important to ensure a strong connection between the ground pin of the bypass capacitor and the ground pin of the microcontroller.

5.1.1 JTAG Interface Design

Figure 6. JTAG Interface Example: A33G52x, A33G53x



5.2 SWD (Serial Wire Debug) Interface

- SWD interface is used for downloading and debugging the ABOV 32-bit microcontroller. Table 9 shows a list of devices that support the SWD interface.
- When using the SWD interface, pull-up/pull-down resistors must conform to the specifications shown in Table 9.

Table 9. External Resistor Values for SWD Interface

Device	SWDIO	SWCLK
A31G11x	Pull-up, 10 kΩ	Pull-down, 10 kΩ
A31G12x	Pull-up, 10 kΩ	Pull-down, 10 kΩ
A31G21x	Pull-up, 10 kΩ	Pull-up, 10 kΩ
A31G22x	Pull-up, 10 kΩ	Pull-up, 10 kΩ
A31G31x	Pull-up, 10 kΩ	Pull-up, 10 kΩ
A31G32x	Pull-up, 10 kΩ	Pull-up, 10 kΩ
A33G52x	Pull-up, 10 kΩ	Pull-up, 10 kΩ
A33G53x	Pull-up, 10 kΩ	Pull-up, 10 kΩ
A31T21x	Pull-up, 10 kΩ	Pull-up, 10 kΩ
A31M22x	Pull-up, 10 kΩ	Pull-up, 10 kΩ
A33M11x	Pull-up, 10 kΩ	Pull-up, 10 kΩ
A34M41x	Pull-up, 10 kΩ	Pull-up, 10 kΩ
A34M420	Pull-up, 10 kΩ	Pull-up, 10 kΩ
A34M456	Pull-up, 10 kΩ	Pull-up, 10 kΩ
A34L716	Pull-up, 10 kΩ	Pull-up, 10 kΩ
AC30M1x64	Pull-up, 10 kΩ	Pull-up, 10 kΩ
AC33Mx064	Pull-up, 10 kΩ	Pull-up, 10 kΩ
AC33Mx128	Pull-up, 10 kΩ	Pull-up, 10 kΩ

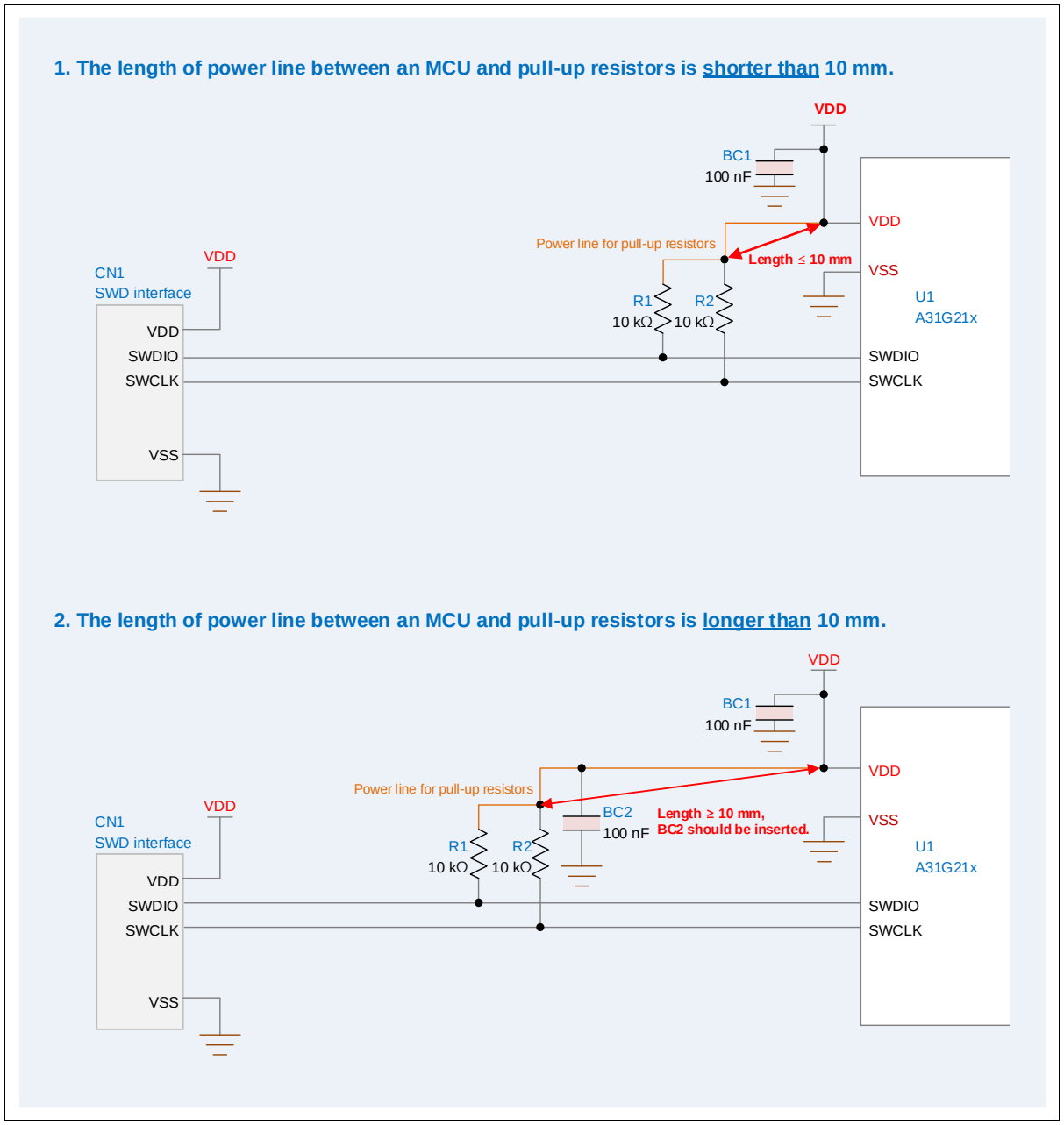
NOTE:

1. The application can set the SWD pins (SWCLK, SWDIO) to alternative functions. To debug the target microcontroller when the SWD pins are set to other alternative functions, the microcontroller must be restarted in boot mode using the BOOT pin and nRESET pin, and then the SWD pins are initialized to SWCLK and SWDIO. Therefore, the nRESET and BOOT pin of the target microcontroller should be considered when designing SWD interface circuits. (Refer to section 2 and section 3.)

- After the development stage, if the SWD pins are left unconnected, they may be affected by external noise. Therefore, production boards require the pull-up and the pull-down resistors to be installed.
- As a reference, a device that supports JTAG and SWD interfaces is described in the following page:
  - If a device's interface is left unconnected during development, the firmware can later configure it to output a low or high signal. Therefore, it is acceptable to set the unused interface pin to NC.
- Resistors should be placed close to the SWD pins (within 10 mm).
- Pull-up resistor power must be connected to the microcontroller's VDD power.
- Suppose the power connection of the pull-up resistor is located more than 10 mm away from microcontroller's VDD power. In that case, it is recommended to add a 0.1 µF bypass capacitor between the microcontroller's VDD pin and ground. It is also important to ensure a strong connection between the ground pin of the bypass capacitor and the ground pin of the microcontroller.

5.2.1 SWD Interface Design

Figure 7. SWD Interface Example: A31G21x

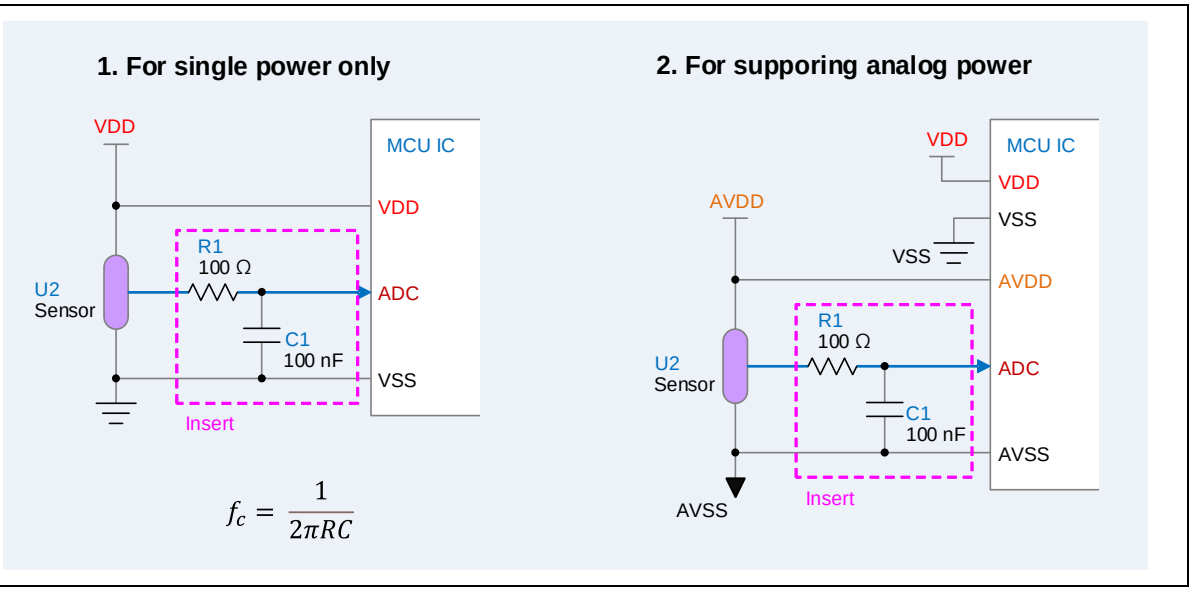


6. ADC Input

6.1 Power Selection

- If a microcontroller has separate analog power (AVDD and AVSS) and digital power (VDD and VSS) pins, it is recommended to use analog power for circuit design.
- When a microcontroller supports single power internally, it is advisable to use a single power source. It is important to ensure that external noise does not affect the analog power and the input traces.
- To further reduce noise, an RC filter (low-pass filter) can be used on the ADC input trace. The filter should have an RC time constant that is three times the stabilization time.

Figure 8. Power Selection Diagram



7. I2C Line

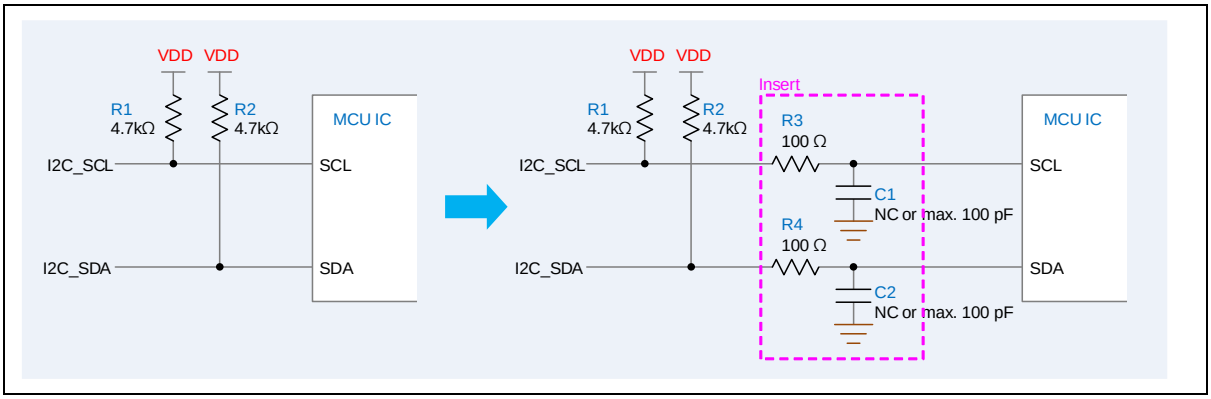
7.1 Filters used on I2C Line

- Pull-up resistors, series resistors, and filter capacitors can be used to implement filters on the I2C lines.
- To achieve optimal performance, the placement and order of filter components are crucial. Adding a series resistor can help reduce noise, while a filter capacitor can effectively bypass noise to GND.
- The filter components for SCL (R3 and C1) and SDA (R4 and C2) lines must be placed close to the I2C pins of a microcontroller (within 30 mm).
- The same guideline is applied to SPI lines.

Table 10. I2C Line Component Value

Item	Component	Value
Pull-up resistor	R1, R2	4.7 kΩ to 10 kΩ
Series resistor	R3, R4	100 Ω to 330 Ω
Filter capacitor	C1, C2	NC (Not connected) or to 100 pF

Figure 9. Filters Used on an I2C Line Diagram



8. Unused Pin

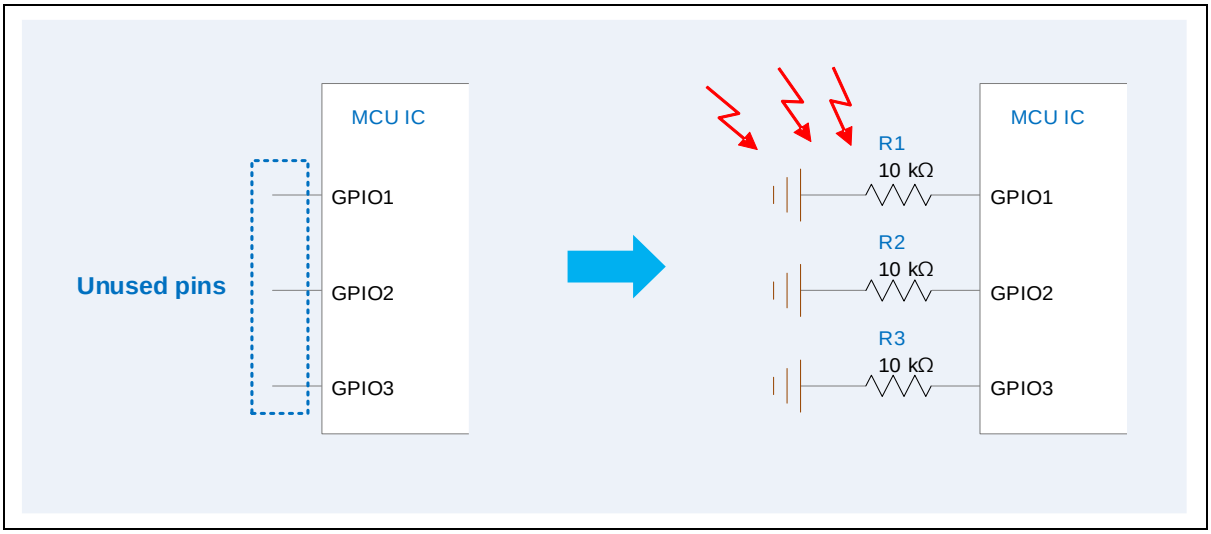
8.1 Handling Unused Pin

- To improve the noise immunity and robustness of a microcontroller, it is recommended to terminate all unused pins properly by connecting them to each pull-down resistor.
- Resistors should be placed as close to a microcontroller as possible (within 20 mm).
- For not connected (NC) pins, it is recommended to configure them as a push-pull output and set them to low by software.
  - Alternatively, the pins can be configured as an input using an internal pull-up resistor. In this case, the external pull-down resistor should not be used.

Table 11. Unused Pins Circuit Component Value

Item	Component	Value
Pull-down resistor	R1	1 kΩ to 10 kΩ

Figure 10. Circuit Recommendation for Unused Pins



9. Power Line

9.1 Filter Circuit for Power Line

Filter circuits implemented on power lines may enhance board performance in cases of failure.

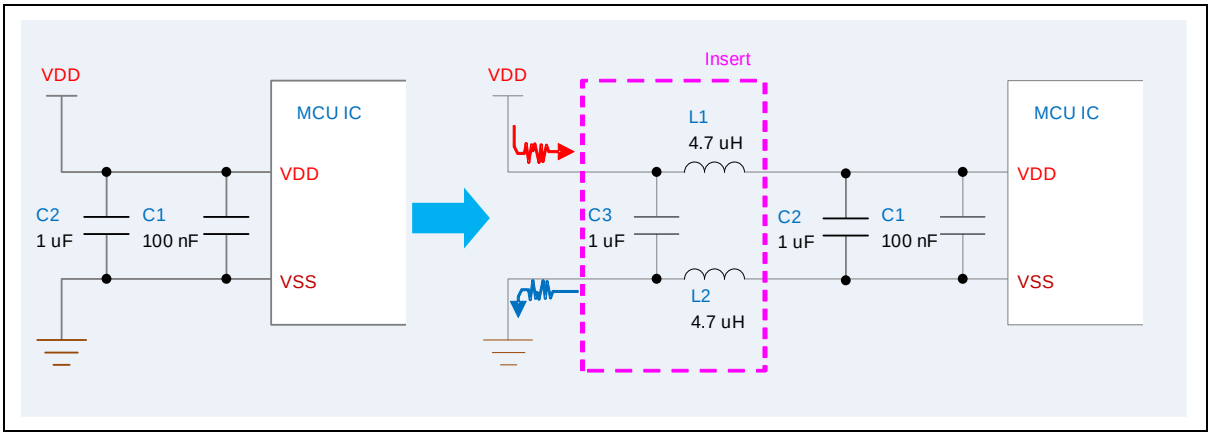
9.2 Filters Used on a Microcontroller Power Input

Filter components (L1 and L2) must be placed close to noise sources (e.g., within 30 mm of the power pins) rather than close to a microcontroller.

Table 12. Power Lines Component Value

Item	Component	Value
Decoupling capacitor	C1	10 nF to 100 nF
	C2	1 μF
Series inductor (Power Filter)	L1, L2	Typ. 4.7 μH
Capacitor (Power Filter)	C3	Typ. 1 μF

Figure 11. Power Lines Diagram

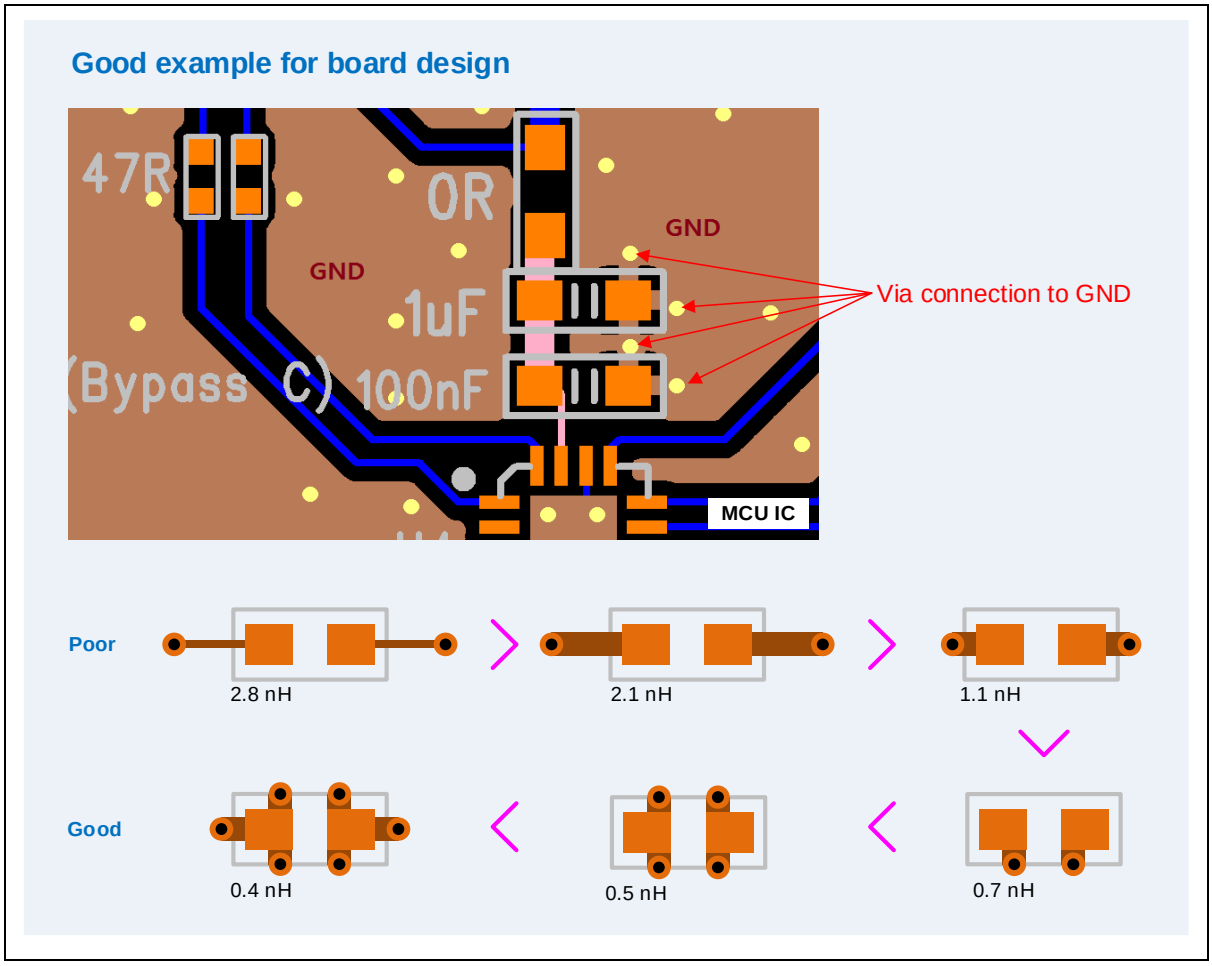


10. Via Connection

10.1 Case 1: Via Connection to Power and Ground Plane

- In circuit board design, vias can be utilized to connect a bypass and filter capacitor from one layer to the power or ground plane in another layer.
  - At this point, traces connecting the capacitor through the via create a single inductance value.
- A larger unwanted inductance value will result in increased sensitivity to external noise.
  - To reduce the inductance value and improve the effectiveness of the noise bypassing to ground, it is recommended to use multiple vias and widen the distance between traces.

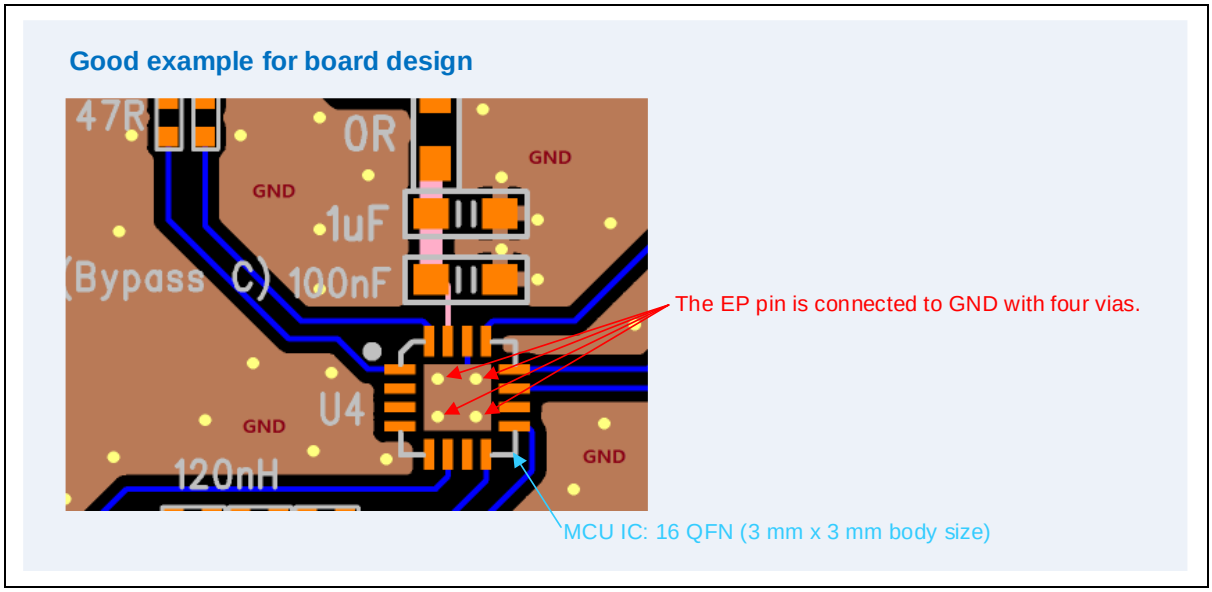
Figure 12. Via Connection to Power and Ground Plane



10.2 Case 2: Via Connection to Exposed Pad (EP) of a Microcontroller

- Packages such as Quad Flat No-lead (QFN) often have Exposed Pads (bottom pads) that are typically connected to the ground.
- To ensure a low impedance path to ground, it is recommended to place as many vias as possible on the EP pin. For example, a 16-pin QFN package (3 mm x 3 mm) should have at least two vias in the EP.

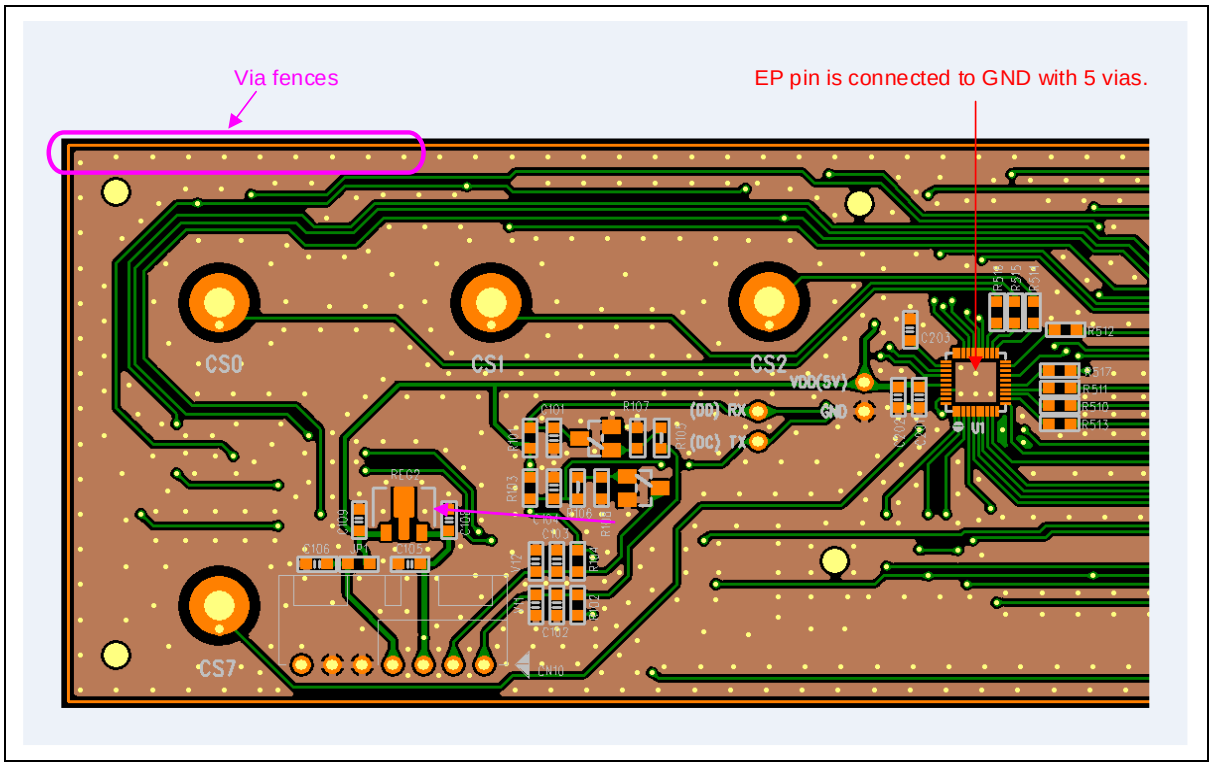
Figure 13. Via Connection to EP of a Microcontroller Diagram



10.3 Case 3: Via Fences

1. The ground vias should be arranged at a consistent distance (typ. 5 mm pitch) from each other within the boundaries of the board.
2. The ground vias should be placed at a consistent distance on the internal GND pattern.
3. Following step 1 and step 2 may reduce external noise and Electromagnetic Interferences (EMI) emission.

Figure 14. Via Fences Diagram

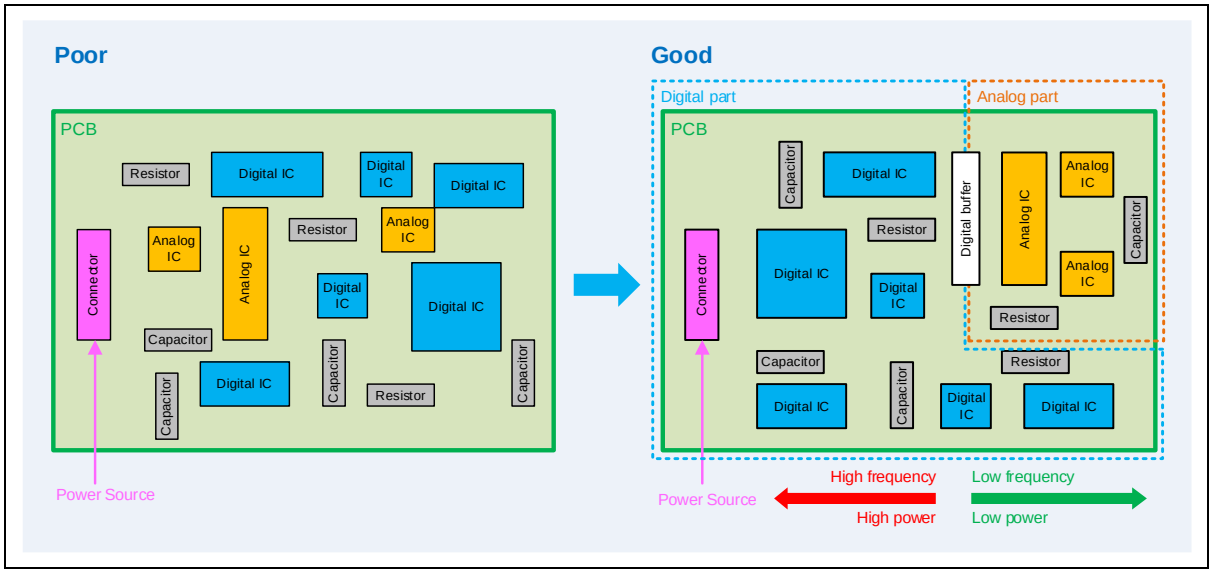


11. Component Placement

11.1 Component Placement Guidelines

- When placing components, you must divide the components into digital and analog components based on a reference point. The reference point is typically the point of power supply, which is the 'Connector' in Figure 15.
- It is recommended to place a digital component that consumes the highest power and operates at the highest frequency closest to the 'Connector.'
- However, if an analog component is placed in this position instead, it may be subjected to high frequency and large current, which could adversely affect its performance.

Figure 15. Component Placement Diagram



12. Power Line Routing

12.1 Case 1: Basic Routing for Power Lines (VDD and GND)

- To minimize current loops on PCB layouts, it is advisable to use wider or thicker traces in parallel without jumpers. It is recommended to fill the ground with a copper pattern.
- Additionally, VDD and ground power lines should be routed close to and parallel to each other to minimize the surface area of the loop pattern of the power line.

Figure 16. Basic Routing for Power Lines (VDD and GND) Diagram

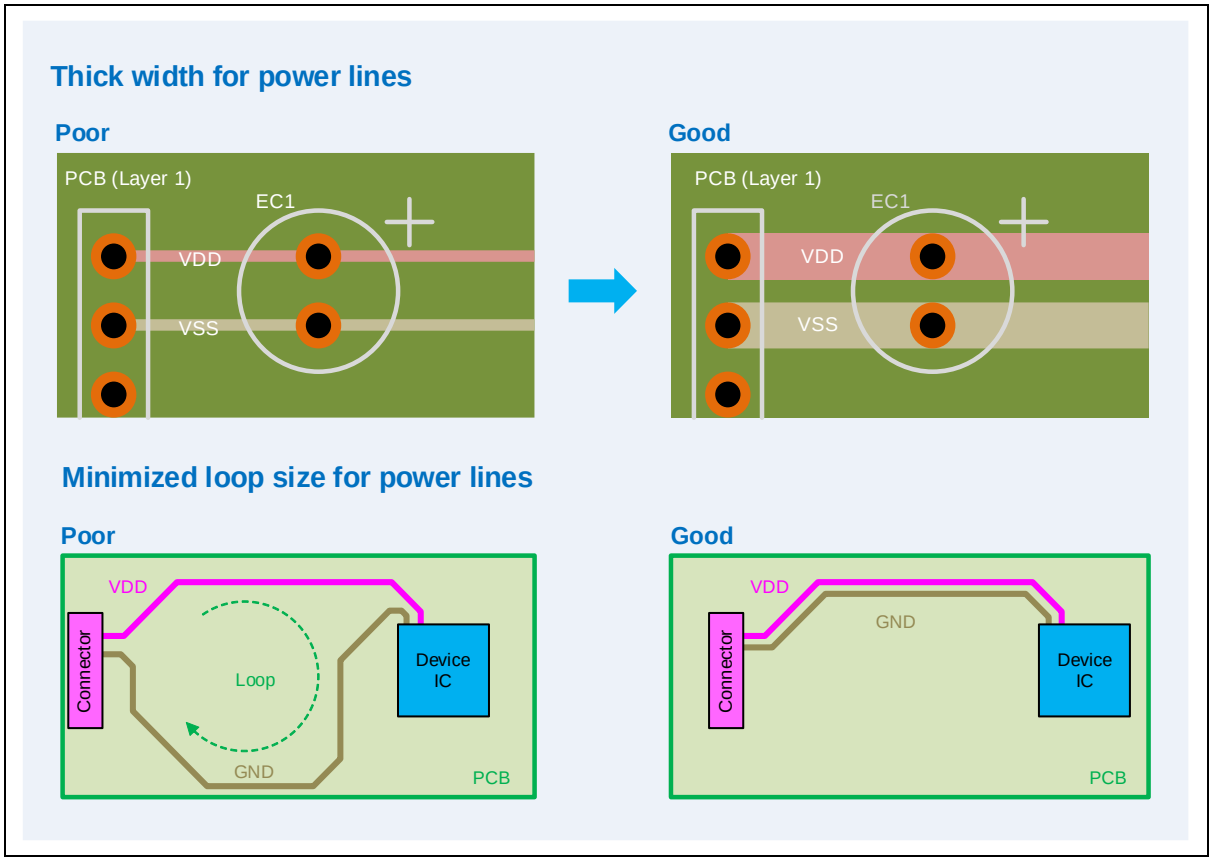
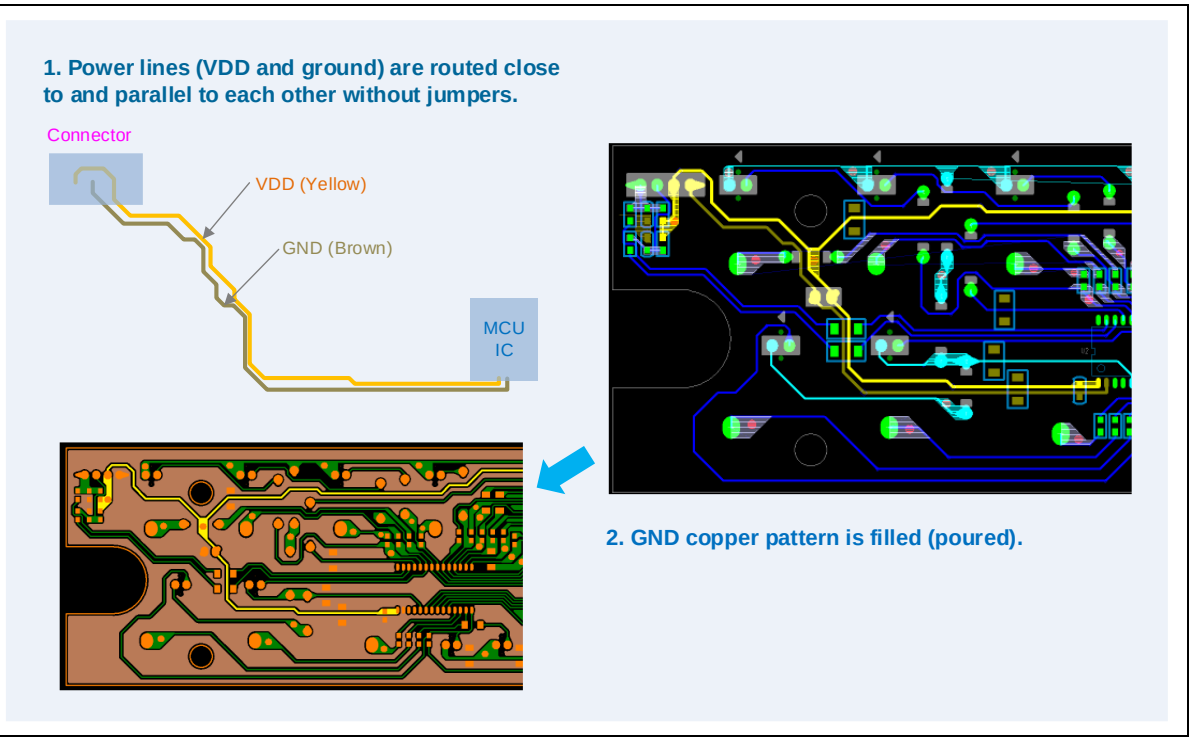


Figure 17 shows a design case for a single layer PCB board.

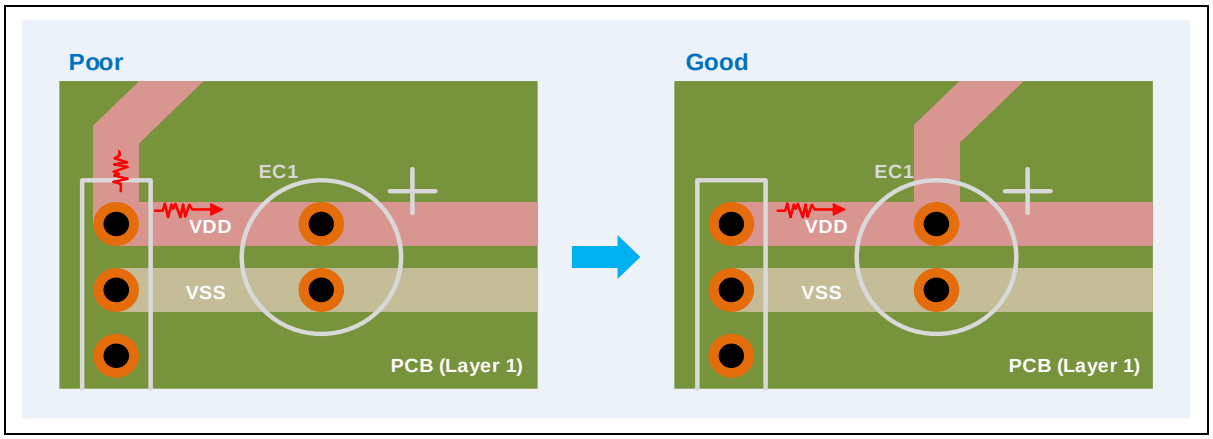
Figure 17. Single-Layer Board Design Diagram



12.2 Case 2: Branch of Power Lines

- Prior to routing, power lines must be filtered to reduce noise.
- In Figure 18, the poor case shows a power line that is not filtered by EC1 (filter capacitor), making it susceptible to external noise. This case can result in poor signal quality and reliability issues.

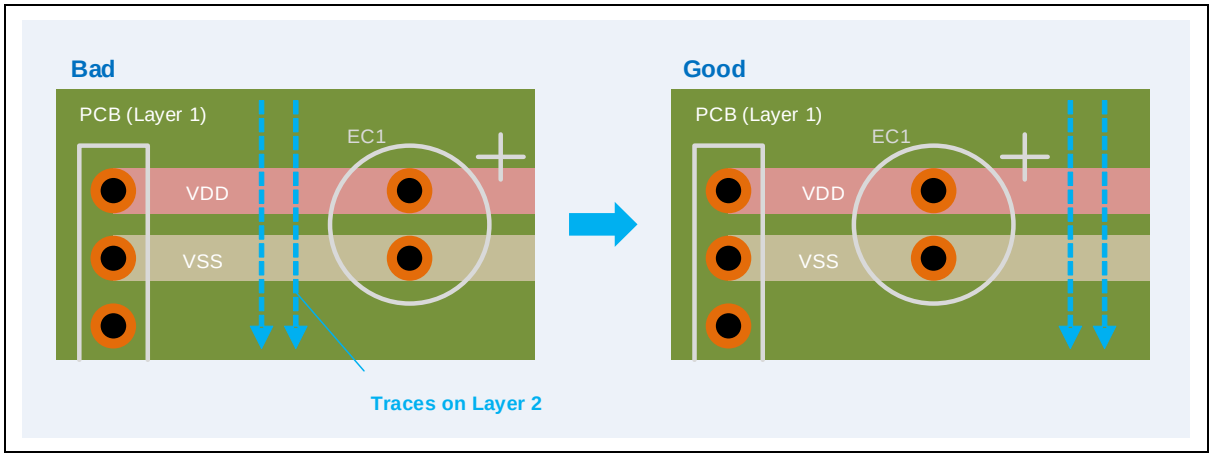
Figure 18. Power Lines Routed as Separated Paths at Multiple Locations



12.3 Case 3: Overlapped Routing with Power Line

- It is recommended to avoid overlapping traces of different signals or powers. However, if it is necessary for traces to overlap with power lines, place overlapped routing after the filtered power line.
- In Figure 19, the bad case shows signal traces overlapping unfiltered power lines, resulting in susceptibility to external noise.
- This bad case can lead to poor signal quality for both the power and communication lines.

Figure 19. Cases of Overlapped Routing with Power Lines



Revision History

Revision	Date	Notes
1.00	Mar. 29, 2023	Initial release
1.01	Apr. 19, 2023	Added A31M22x device.
1.02	Oct. 24, 2023	Added A33G53x device.
1.03	Aug. 07, 2024	Added A34M420 and A34L716 devices.
1.04	Nov. 8, 2024	Corrected typos.
1.05	Nov. 15, 2024	Updated the disclaimer.
1.06	Nov. 22, 2024	Added A34M456 device.

Korea
Regional Office, Seoul
R&D, Marketing & Sales
8th Fl., 330, Yeongdong-daero,
Gangnam-gu, Seoul,
06177, Korea

Tel: +82-2-2193-2200
Fax: +82-2-508-6903
www.abovsemi.com

HQ, Ochang
R&D, QA, and Test Center
37, Gangni 1-gil, Ochang-eup,
Cheongwon-gun,
Chungcheongbuk-do,28126, Korea

Tel: +82-43-219-5200
Fax: +82-43-217-3534
www.abovsemi.com

Domestic Sales Manager
Tel: +82-2-2193-2206
Fax: +82-2-508-6903
Email: sales_kr@abov.co.kr

Global Sales Manager
Tel: +82-2-2193-2281
Fax: +82-2-508-6903
Email: sales_gl@abov.co.kr

China Sales Manager
Tel: +86-755-8287-2205
Fax: +86-755-8287-2204
Email: sales_cn@abov.co.kr