Clock Monitoring Using Internal Timer Peripherals

AN Rev. 1.05

Introduction

This document describes how to implement the function to monitor the system clock using WDT, FRT, and timers embedded in the ABOV 32-bit microcontroller. In addition, this document describes the precautions required for the implementation.

This document applies to the products with part numbers listed in Table 1.

Table 1. Applicable Devices

Base Product	Part Number
A33M11x	A33M116RL, A33M116RM, A33M116CL, A33M114RL, A33M114CL
A34M41x	A34M418YL, A34M418VL, A34M418RL, A34M416VL, A34M416RL, A34M414VL, A34M414RL
A31M22x	A31M223CL, A31M223KN
A34M420	A34M420YL, A34M420VL, A34M420RL
A34L716	A34L716VL, A34L716RL
A34M456	A34M456VL, A34M456RL, A34M456RK

Reference Document

The following documents are available on www.abovsemi.com.

- Datasheets for 32-bit Microcontrollers in Table 1
- User's Manuals for 32-bit Microcontrollers in Table 1

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1.1 System Clock Monitoring using Watchdog Timer (WDT)

A Watchdog Timer (WDT) is a timer that monitors microcontrollers to see if they are operating normally or out of control. The WDT operates as a monitoring device to monitor the operation of the microcontroller.

The microcontrollers adopted in various electronics are programmed with function codes in software to control these electronics. The programs in the microcontroller may become out of control or stop operating, which may cause the electronics to malfunction. At worst, this situation can lead to accidents or damage to electronics. Therefore, it is important to ensure the normal operation of the microcontrollers.

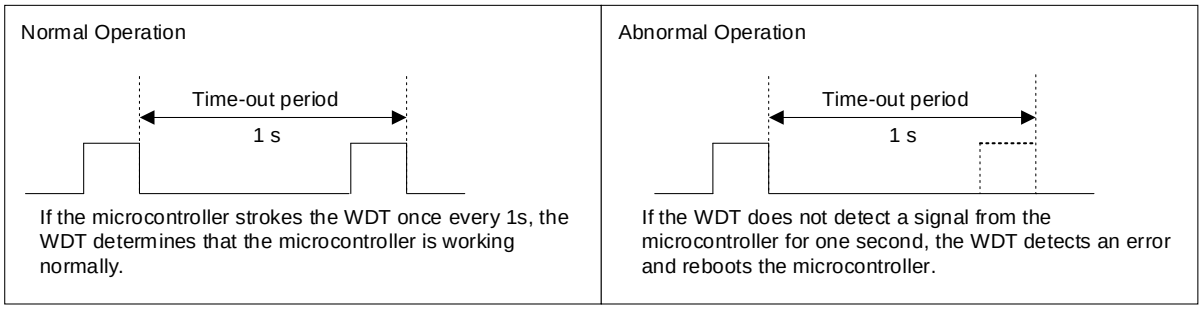
To prevent such accidents, the WDT checks if the microcontroller operates normally and continuously monitors the microcontroller. While communicating with the microcontroller, the WDT recognizes the microcontroller as out of control if the microcontroller does not output a signal at predefined time intervals or if it outputs a signal different from the predefined pattern.

Once the WDT detects a malfunction, it sends a reset signal to the microcontroller to initialize the system or generates a WDT interrupt event.

Figure 1 shows the WDT operations under two conditions:

- Normal operation: The WDT receives a signal from the microcontroller within a predefined time interval.
- Abnormal operation: The WDT determines the microcontroller malfunctions by a signal reception error and then resets the microcontroller.

Figure 1. WDT Operations



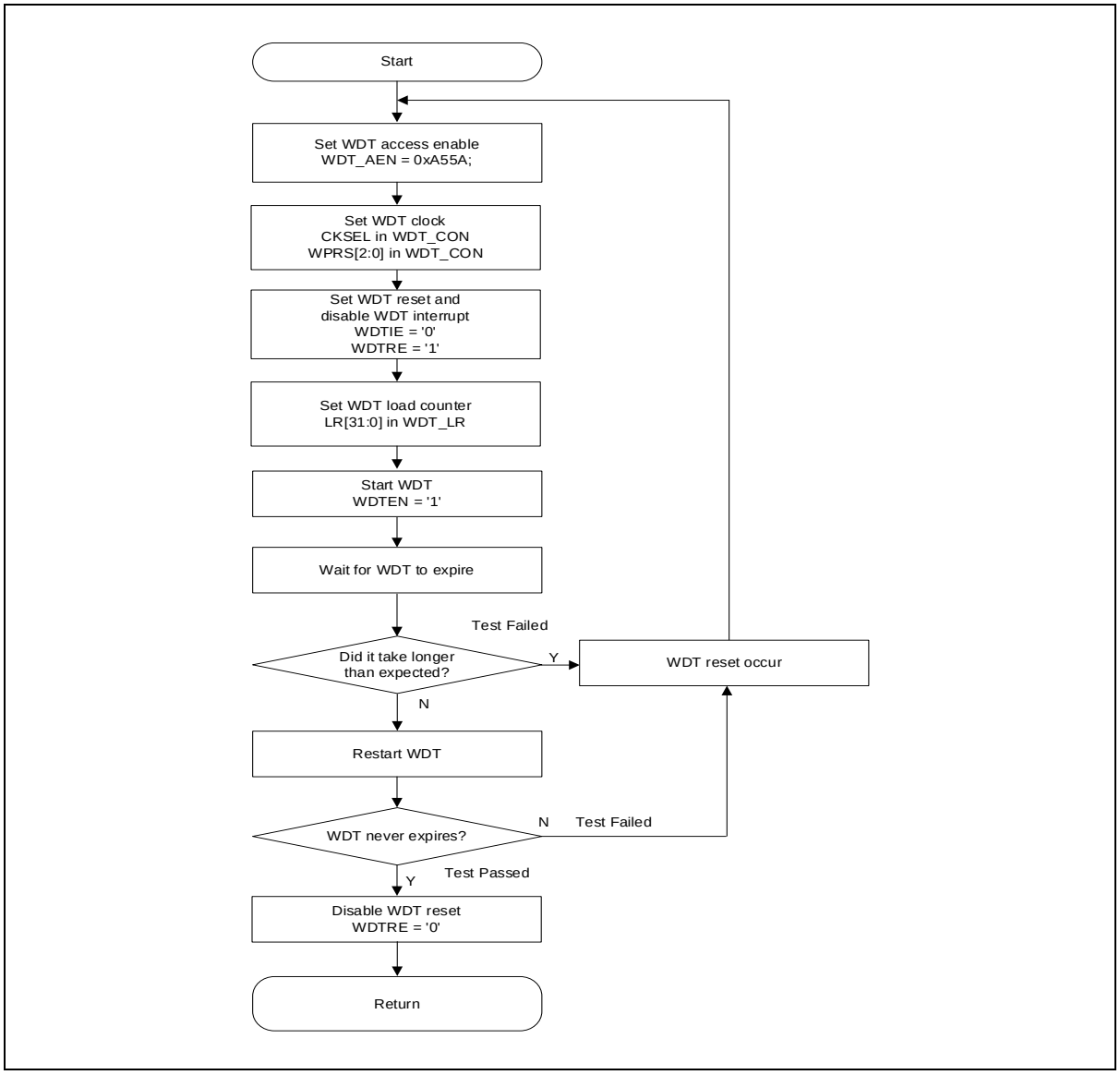
1.1.1 How to Implement Software

This section describes a software implementation that uses the WDT to monitor the system clock.

Figure 2 is an example flowchart of the time-out test for the WDT. If the WDT operates in the order shown in Figure 2, the WDT operating conditions are as follows:

- System clock source (monitoring target clock): HSE, 4 to 16 MHz
- WDT
  - Clock source (monitoring base clock): HSI, 32 MHz
  - Counter period: 1 s
  - Counter match event: Warm reset event

Figure 2. WDT Time-out Test Flowchart



1.2 System Clock Monitoring using FRT and Timer

When monitoring clock speed using the WDT, the WDT can detect only clocks that slow down and cannot detect clocks that speed up. To detect errors in which the clock speed increases, it is necessary to implement clock monitoring software using Free-Run Timer (FRT) and timers.

The FRT generates an interrupt event within a predefined time interval, and the FRT interrupt can be used to implement the system clock monitoring software.

The steps below describe the FRT operation:

1. Set the operation periods both for the timer and FRT.
2. When the FRT interrupt event generates, read the counter values of the timer.
3. Proceed with the Validation Check to verify that the count value of the timer is within the predefined range.
4. Depending on the Validation Check result, run the timer in the event of a pass and configure the system to restart or proceed with the follow-up process in the event of a failure.

1.2.1 How to Implement Software

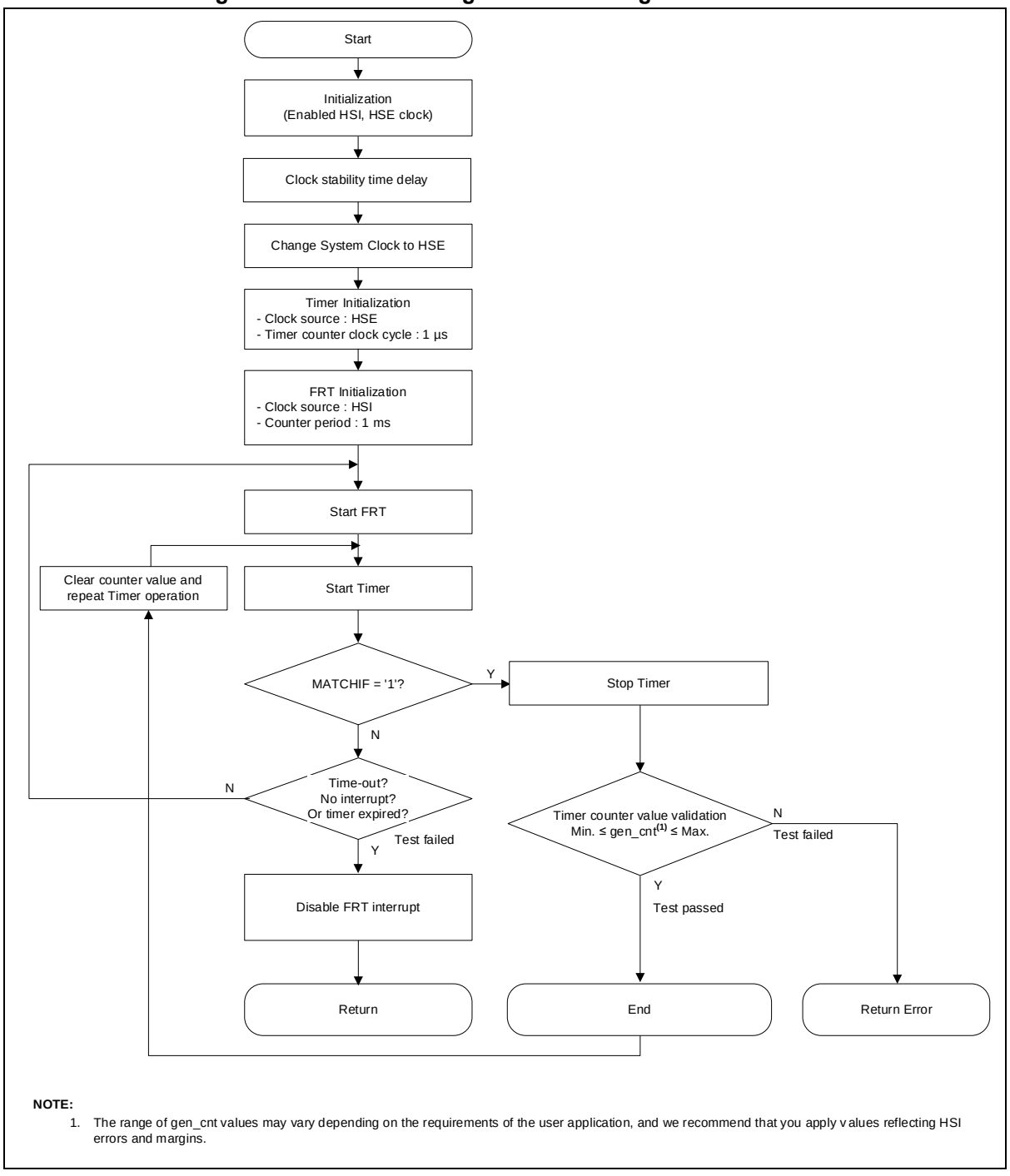
This section describes a software implementation that uses FRT and a timer to monitor the HSE clock.

The operating conditions are as follows:

- System clock source (monitoring target): HSE, 4 to 16 MHz
- Timer
  - Clock source: HSE, 4 to 16 MHz
  - Counter clock cycle: 1 µs
- FRT
  - Clock source (monitoring base clock): HSI, 32 MHz
  - Counter period: 1 ms
  - Counter match event: FRT interrupt event
- Monitoring
  - In the event of the FRT interrupt, the timer stops operating and reads its count value to determine pass or fail.

Figure 3 is a flowchart of software implementation for detecting clock source errors using FRT and timer.

Figure 3. Clock Monitoring Flowchart using FRT and Timer



NOTE:

1. The range of gen_cnt values may vary depending on the requirements of the user application, and we recommend that you apply values reflecting HSI errors and margins.

The following steps describe the sequence in Figure 3.

1. Set the HSICON and HSECON in the SCU_CSCR register to '1' to activate the HSI and HSE clock sources.
2. Wait for each stabilization time of HSI and HSE.
   A. HSI: 100 µs
   B. HSE: 10 ms
3. By configuring the MCLKSEL[2:0] in the SCU_SCCR register, select the HSE as a system clock source.
4. Set the timer to use the external HSE as a clock source and set the timer counter clock cycle to 1 µs.
5. Set the FRT to use the internal HSI[(1)(2)] as a clock source and set it to generate interrupts at 1 ms intervals.
6. Activate the timers and FRT.
7. When the FRT interrupt event occurs, stop the timer and read counter values in the timer counter register.
8. Validate by ensuring that the timer counter value is within the expected range.
   A. Assuming that a target with an expected clock error rate of ±1.5% is monitored, if the FRT interrupt event occurs at 1 ms intervals, the counter value of the timer that operates at 1 µs intervals is recognized as a normal operation when additional margin[(3)] is applied, and the error rate is set to approximately ±30% that ranges from 700 to 1,300.
9. After passing the test in step 8, the timer counter is initialized, and the timer restarts. However, if the test in step 8 fails, the system enters a while-loop state.

NOTES:

1. Because HSE is used as the system clock, the clock source for FRT monitoring the system clock must be set to HSI, not HSE.
2. HSI is a High-Speed Oscillator embedded in the microcontroller. Its clock error rate varies depending on the device.
3. For more information on clock monitoring, see section 1.3.3.

1.3 Precautions for Clock Monitoring

1.3.1 Configuring System Clock and Monitoring Clock Source

Configuring clock sources is important for monitoring the system clock.

The clock source of the timer peripheral that monitors the system clock must be set differently from the system clock or the clock source of the timer peripheral that uses the system clock sources.

If the system clock source and the timer peripheral clock source monitoring the system clock are set to have the same clock source, the system may malfunction, and the causes may not be determined.

1.3.2 Identifying Clock Source Characteristics

Even if external noise causes crystal oscillator errors or clock cycle changes, the clocks used for monitoring must ensure stable operation. Therefore, the microcontroller's internal oscillator, HSI, is used as the monitoring clock.

If the microcontroller's internal oscillator, such as LSI and HSI, is used as a clock source, oscillator error characteristics are reflected as they are. Therefore, the oscillator characteristics used in user applications must be identified and considered prior to designing hardware and implementing software.

For more information on the oscillator characteristics, refer to the User's Manual and Datasheet for your device.

1.3.3 Setting Validation Range of Clock Monitoring

While monitoring the system clock, the validation decision depends on the range of timer counter values. If the validation range of timer counter values is set narrowly and strictly using the oscillator error rate only, the system can generate clock monitoring errors very often.

Therefore, the validation range of timer counter values must be adjusted by adding margin values. The margin value of the timer counter value varies depending on the requirements of the user system.

Revision History

Revision	Date	Notes
1.00	Feb. 13, 2023	Initial release.
1.01	Apr. 28, 2023	Added the device and part number for the A31M22x.
1.02	Dec. 18, 2023	Added the device and part number for the A34M420 to Table 1.
1.03	May. 27, 2024	Added the device and part number for the A34L716 to Table 1.
1.04	Nov. 15, 2024	Updated the disclaimer
1.05	Nov. 22, 2024	Added A34M456 device.

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