Setting System Main Clock Using PLL

AN Rev. 1.05

Introduction

A PLL clock is used to set the high-speed clock frequency as the main clock of the microcontroller.

This document describes how to use the embedded PLL as the system main clock in ABOV 32-bit microcontrollers. In addition, this document introduces precautions required when using the PLL.

This document applies to products with part numbers listed in Table 1.

Table 1. Applicable Devices

Base Product	Part Number
A31G21x	A31G213CL, A31G213SQ, A31G213KN, A31G213GR, A31G212CL, A31G212SQ, A31G212KN, A31G212GR
A31G22x	A31G226ML, A31G226MM, A31G226RM, A31G226RL, A31G226RL A31G224ML, A31G224MM, A31G224RM, A31G224RL, A31G224RL
A31G31x	A31G316MM, A31G316ML, A31G316RM, A31G316RL, A31G314MM, A31G314ML, A31G314RM, A31G314RL, A31G314CL, A31G314CU, A31G314SN, A31G313RM, A31G313RL, A31G313CL, A31G313CU, A31G313SN
A31G32x	A31G324RL, A31G324CL, A31G324CU, A31G323RL, A31G323CL, A31G323CU
A33M11x	A33M116RL, A33M116RM, A33M116CL, A33M114RL, A33M114CL
A34M41x	A34M418YL, A34M418VL, A34M418RL, A34M416VL, A34M416RL, A34M414VL, A34M414RL
A34M420	A34M420YL, A34M420VL, A34M420RL
A31T21x	A31T216RL, A31T216CL, A31T216SN, A31T214RL, A31T214CL, A31T214SN
A31M22x	A31M223CL, A31M223KN
A34L716	A34L716VL, A34L716RL
A34M456	A34M456VL, A34M456RL, A34M456RK

Reference Document

The following documents are available on www.abovsemi.com.

- Datasheets for products in Table 1
- User's Manuals for products in Table 1

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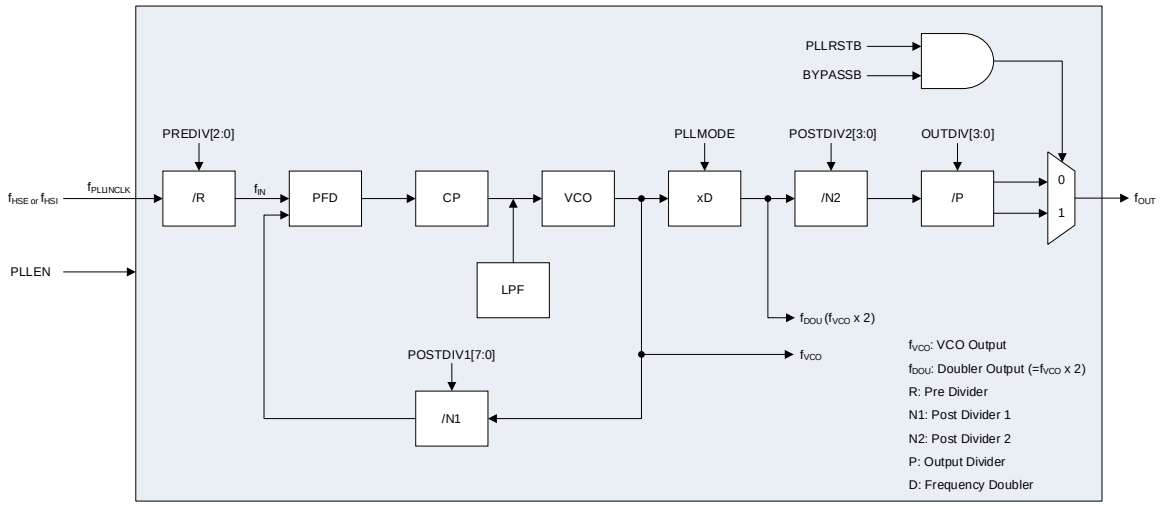
1. PLL Structure

Figure 1 shows a block diagram of the PLL.

Figure 1. PLL Block Diagram



Register	Bit	Symbol	Description
SCU_PLLCON	PREDIV[2:0]	R	PLLINCLK Pre-divider value
	POSTDIV1[7:0]	N1	Post Multiplier value
	POSTDIV2[3:0]	N2	Post Divider value
	OUTDIV[3:0]	P	Output Divider value
	PLLMODE	D	Frequency Doubler value

NOTES:

1. PLLEN =' 1' ➔ Min. 1 us Delay ➔ PLLRSTB = '1' to enable PLL block & set PLL frequency.
2. Wait 500 us for the stabilization of the PLL output.
3. Wait until the PLLLOCK (= LOCKSTS) flag occurs.
4. Refer to section 2.2 for PLL output frequency calculation.
5. PLLMODE (D) must be set to ‘0’.

CAUTION:

1. For A31M22x microcontroller, POSTDIV2 (N2) must be set to '1'.

2. PLL Frequency Settings

2.1 PLL Clock Sources

The internal PLL is used to multiply the output clock frequency of HSI or HSE. The PLL clock source is used as the input frequency (f_{lick}) of the PLL block.

Since the tolerance characteristics of the $f_{PLLINCLK}$ affect PLL frequency, the clock source characteristics of the PLL need to be carefully checked.

This section describes a method to use the clock source HSI and HSE as inputs to the PLL block.

2.1.1 Stabilization Time for Clock Sources

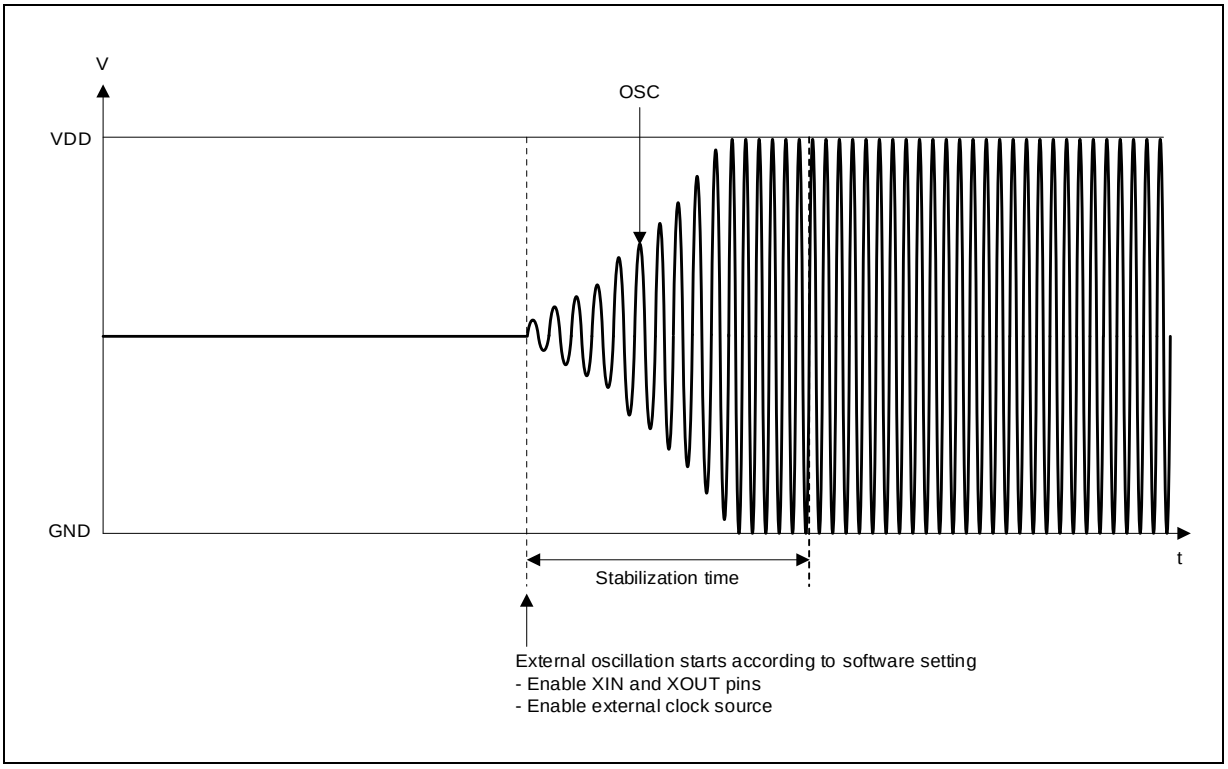
Each clock source must have a stabilization time after activation until it generates a stable frequency.

- Stabilization time after activation:
  - HSI clock source: Typ. 100 μs
  - HSE clock source: Typ. 5 ~ 10 ms (1) (2)

NOTES:

1. In this document, the HSE stabilization time is presented with an approximate recommendation value. For the exact specification value, refer to the HSE characteristics in the datasheet of the corresponding product.
2. The stabilization time of the HSE varies according to the configuration method of the external oscillation circuit and the oscillation element's characteristics. Therefore, it is recommended to apply the appropriate stabilization time according to the configuration of the user application.

Figure 2. Enabling and Stabilization of Clock Source



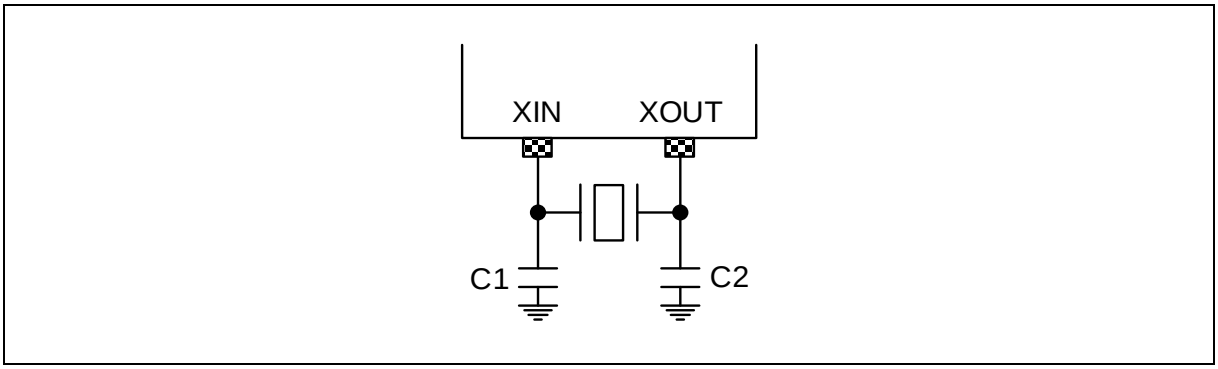
2.1.2 Oscillation Circuit Configuration for External Clock Sources

The HSE clock can be enabled by software. It can be divided using a prescaler to set the accurate frequency.

When external oscillation elements such as crystals and resonators are used to set the accurate frequency for the system at a low cost, the external oscillation circuit of Figure 3 is required.

The tolerance of the HSE clock is affected by the characteristics of the XTAL element. Therefore the user must refer to the datasheet of the corresponding crystal. In addition, since external load capacitance (C1 and C2) must be configured based on the HSE's operation frequency that is required by the microcontroller, the user must refer to the HSE characteristics in the datasheet before designing the circuit.

Figure 3. External Oscillation Circuit



2.1.3 Precautions when using External Oscillation Circuit

When using external clock sources, the pins assigned for the HSE must be used only for the external oscillation circuit. These pins cannot be used for other purposes, such as GPIOs or analog input pins.

2.1.4 Precautions when using only Internal Oscillators (External Oscillators are not used)

If only the internal oscillator (LSI or HSI) is used to supply the clock to the microcontroller in a user application, the XIN and XOUT pins multiplexed with the HSE can be used as GPIOs. Before using these pins as GPIOs, make sure that the HSE clock is disabled.

If these pins are set to open drain or push-pull and are set to the function of the external clock sources, the microcontroller may malfunction.

2.2 PLL Output Frequency Calculation

The PLL can set the output frequency f_{OUT} to generate an accurate value.

The input clock frequency f_{IN} of the PLL block follows the input bandwidth characteristics of the PLL specifications. By applying the pre-divider value shown in the formula below, the f_{IN} can be obtained from the clock source frequency of the PLL block, $f_{PLLINCLK}$.

The input range of the f_{IN} frequency is allowed from 1 MHz to 3 MHz. However, up to 2 MHz is recommended:

$$f_{\mathrm{IN}}\,[\mathrm{MHz}] = \frac{f_{\mathrm{PLLINCLK}}}{(\mathrm{R}+1)}, \qquad \text{Where } 1\ \mathrm{MHz} \le f_{\mathrm{IN}} \le 3\ \mathrm{MHz}\ (\text{Recommended } f_{\mathrm{IN}} = 2\ \mathrm{MHz})$$

At this time, the range of VCO frequency, f_{VCO}, should be set to Max. VCO frequency (Max. f_{VCO}) or less, and the calculation formula is as follows. (Refer to PLL electrical characteristics in the datasheet.):

$$f_{\mathrm{VCO}}\,(\mathrm{MHz}) = f_{\mathrm{IN}} \times (\mathrm{N}_1 + 1), f_{\mathrm{VCO}} \le \mathrm{Max.}\, f_{\mathrm{VCO}}$$

As a result, the final frequency of the PLL block, f_{PLLOUT}, can be obtained from the formula below:

$$\begin{aligned} f_{\mathrm{PLLOUT}}\,[\mathrm{MHz}] &= \frac{f_{\mathrm{PLLINCLK}} \times (\mathrm{N}_1 + 1)}{(\mathrm{R}+1) \times (\mathrm{N}_2 + 1) \times (\mathrm{P}+1)} \times (\mathrm{D}+1) \\ &= \frac{f_{\mathrm{IN}} \times (\mathrm{N}_1 + 1)}{(\mathrm{N}_2 + 1) \times (\mathrm{P}+1)} \times (\mathrm{D}+1) \\ &= \frac{f_{\mathrm{VCO}}}{(\mathrm{N}_2 + 1) \times (\mathrm{P}+1)}, \qquad when\ D = 0\ (D\ \ must\ be\ set\ to\ 0.) \end{aligned}$$

Additionally, using N_1 to make f_{VCO} twice the target frequency, and then using N_2 to divide f_{VCO} by 2 to generate a more stable f_{PLLOUT} than using f_{VCO} as is as f_{PLLOUT}.

CAUTION:

1. To normally output PLL frequency in the A31M22x microcontroller, the N_2 value must be set to '1'. With this setup, the formula for calculating PLL frequency f_{PLLOUT} is as follows:

$$f_{\mathrm{PLLOUT}}\,[\mathrm{MHz}] = \frac{\mathrm{f_{VCO}}}{2 \times (\mathrm{P}+1)}, \qquad when\ N_2 = 1\ (N_2\ must\ be\ \text{set to } 1.)$$

2.3 How to use PLL Output as System Main Clock

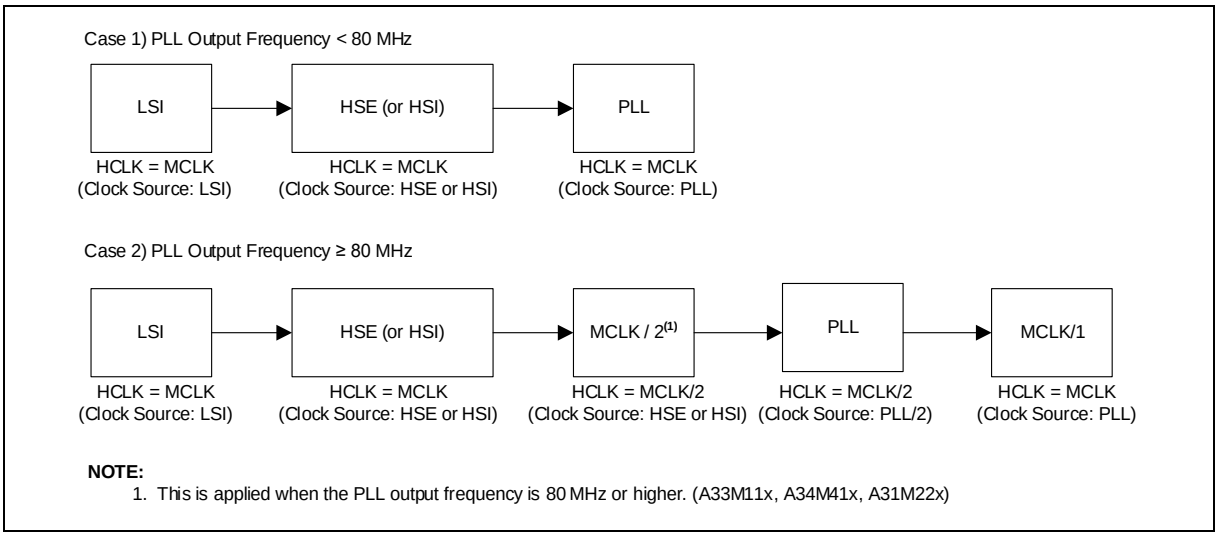
PLL clock is used to set the high-speed clock frequency as the main clock (MCLK) of the microcontroller. The two clock sources, HSI and HSE are used as input clocks of the PLL.

Tolerance of the PLL reflects the characteristics of the input clock sources. Based on the PLL input clocks, the PLL frequency divider can be used to output a more accurate frequency, and the main clock of the microcontroller can be set up to max. operating frequency using PLL output frequency.

To use the PLL clock as the main clock of the microcontroller, the following settings must precede:

1. Before and after using the PLL clock to set the main clock, the current clock source and the clock source you want to change must be alive (refer to Section 2.1 PLL Clock).
2. To use the PLL output frequency set in the PLL block as the main system clock, set the MCLK to the input clock (HSE or HSI) of the PLL block and then change the MCLK to stabilized PLL output frequency of the PLL block.
   If the MCLK is set directly from the LSI block to the PLL output frequency of the PLL block, the microcontroller may malfunction. Therefore, the MCLK must be set to HSI or HSE clock source before the PLL block outputs frequency. (Refer to Case 1 in Figure 4.)
3. If the PLL output frequency is 80 MHz or higher, the software should set the PLL in the following order:
   A. Set the MCLK as the PLL input clock source HSI (or HSE).
   B. Set the MCLK to apply the HCLK divided by two.
   C. Set the MCLK to the output frequency of the PLL block.
   D. Lastly, set the MCLK to apply the HCLK divided by one. Then, the MCLK uses the output frequency of the PLL block (refer to Case 2 in Figure 4).

Figure 4. Two Ways to Set PLL to MCLK (LSI and PLL)

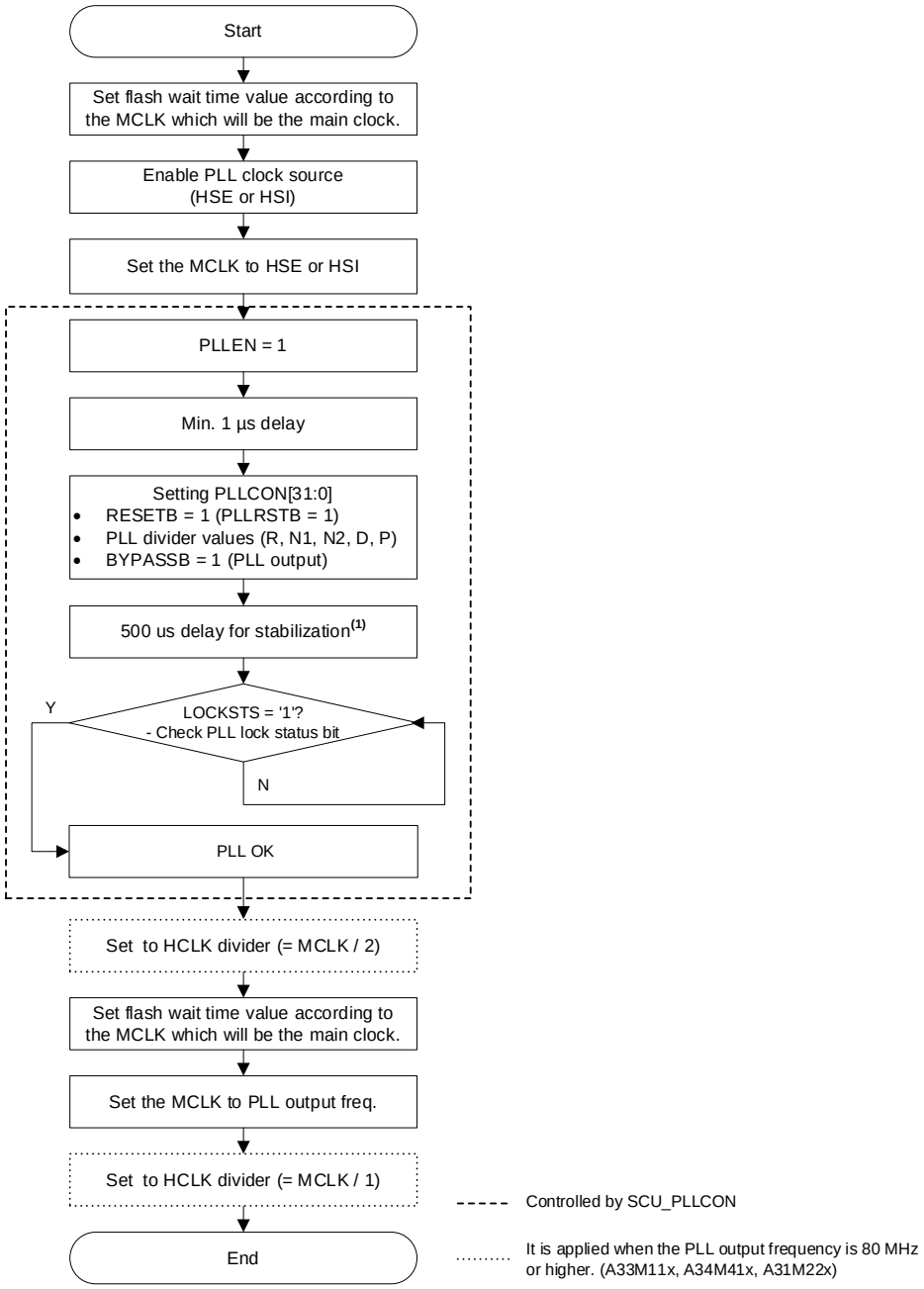


4. Before changing the system clock, the flash memory wait value must be set not to exceed the max. flash memory access speed (refer to Chapter 3).

2.4 PLL Flowchart

Figure 5 shows the setup procedure for using the output frequency of PLL embedded in the 32-bit microcontrollers (refer to Table 1).

Figure 5. PLL Settings Flowchart



NOTE:

1. This means the stabilization time of PLL may vary depending on the IC.

2.5 PLL Lock Status Flag

When the PLL output frequency value is set to the software-setting value after PLL activation, the PLL Lock Status flag is enabled.

The user can check the status of the PLL in the 32-bit microcontroller by polling the PLLLOCK (= LOCKSTS) flag.

NOTE:

1. A31T21x device uses the PLLRDY status flag to provide the functionality of the PLL lock status flag. After PLLEN is enabled, the PLLRDY flag indicates the PLL is locked. (When the pre-divider clock is 2 MHz, PLL delay time is estimated to be about 500 μs.)

3. Flash Memory Access Timing

3.1 Flash Memory Wait-time Configuration

The users can use software to set the wait-time in FMC_CFG (CFMC_CFG or DFMC_CFG) register after setting the system main clock. The wait-time setting affects the flash memory access speed and system performance.

Table 2 shows the max. available clock frequency of each device's flash memory. (Please refer to the flash memory characteristics in the datasheet of the corresponding device.)

Table 2. Max. Available Clock Frequency of 32-bit microcontrollers

Device	Range of Wait-Time	Max. Available Clock Frequency(1)
A31G21x	0 to 4	20 MHz
A31G22x	0 to 5	20 MHz
A31G31x	0 to 3	20 MHz
A31G32x	0 to 3	20 MHz
A33M11x	0 to 15	28 MHz
A34M41x	0 to 15	28 MHz
A34M420	0 to 15	28 MHz
A31T21x	0 to 4	20 MHz
A31M22x	0 to 15	27 MHz
A34L716	0 to 15	25 MHz

NOTE:

1. "Max. available clock frequency" is the available clock frequency of the microcontroller's flash memory when the wait time is zero (WAIT = 0).

The user can set the access timing of code flash (or data flash) memory to a value shown in Table 3. The access timing can also be calculated by the following formula, which depends on the system main clock and wait time.

$$\text{Flash access timing [MHz]} = \frac{\text{HCLK}}{(1 + \text{WAIT})} \leq \text{Max. available clock frequency}$$

Table 3. Flash Wait-time Values

Register Field	WAIT Value	Description
(C)WAIT or (D)WAIT	000	Flash memory access in 1 cycle (0-wait)
	001	Flash memory access in 2 cycles (1-wait)
	010	Flash memory access in 3 cycles (2-wait)
	011	Flash memory access in 4 cycles (3-wait)
	100	Flash memory access in 5 cycles (4-wait)
	101	Flash memory access in 6 cycles (5-wait)
	111	Flash memory access in 7 cycles (6-wait)
	…	…
	n(1)	Flash memory access in (n+1) cycles (n-wait)

NOTE:

1. Each device has a different max. wait-time value. For more information on the max. Wait-time value, refer to (C/D) FMC_CFG register in the corresponding device's User's Manual.

The example below shows how the flash memory access timing is calculated.

Set the flash memory wait-time to '2' for the system with 48 MHz MCLK (for A31G22x). With this setting, the flash memory access speed is 16 MHz, as shown in the calculation below:

$$\begin{aligned}\text{Flash access speed [MHz]} &= 48\ \text{MHz} / (1 + 2) \\ &= 48\ \text{MHz} / 3 \\ &= 16\ \text{MHz}\ (62.5\ \text{ns}) \leq 20\ \text{MHz}\ (50\ \text{ns})\end{aligned}$$

Glossary

Table 4 lists the terms, abbreviations, and acronyms used in this document.

Table 4. Glossary of Terms, Abbreviations, and Acronyms

Term	Description
HCLK	High-Speed Clock
PCLK	Peripheral Clock
MCLK	Main Clock
LSI	Low-Speed Internal Clock
HSI	High-Speed Internal Clock
HSE	High-Speed External Clock
PLL	Phase Locked Loop Clock
XTAL	External Crystal Oscillator
SXTAL	Sub External Crystal Oscillator
SCU	System Control Unit

Revision History

Revision	Date	Notes
1.00	Jan. 13, 2023	Initial release
1.01	Apr. 28, 2023	Added device and part number for A31M22x to Table 1. Added CAUTION and Description to Figure 1. Updated Section 2.2 for A31M22x PLL formula. Updated descriptions of Figure 4 and Figure 5. Added A31M22x device to Table 2.
1,02	Dec. 18, 2023	Updated Section 3.2 for PLL formula. Added A34M420 device to Table 1 Added A34M420 device to Table 2
1.03	May. 24, 2024	Added A34L716 device to Table 1. Added A34L716 device to Table 2.
1.04	Nov. 15, 2024	Updated the disclaimer
1.05	Nov. 22, 2024	Added A34M456 device

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