# Flag Clearing Issue in UART IIR Registers

ET Rev. 1.00

## Introduction

Among the flags in the UARTn_IIR Register, TXE and DMA RX Complete flags are sometimes cleared regardless of user intent.

This document explains why unintentional “Clear” issues occur and provides software solutions to prevent them.

This document applies to the devices listed in Table 1.

**Table 1. Device Identification**

| Base Product | Part Number |
|---|---|
| AC30M1xxx | AC30M1464LBN, AC30M1364LBN, AC30M1364UB, AC30M1332LBN, AC30M1332UB |
| A31G21x | A31G213CL, A31G213SQ, A31G213KN, A31G213KU, A31G213GR, A31G212CL, A31G212SQ, A31G212KN, A31G212KU, A31G212GR |
| A31T21x | A31T216RL, A31T216CL, A31T216SN, A31T214RL, A31T214CL, A31T214SN, A31T214IU, A31T216RL2, A31T216CL2, A31T216SN2, A31T214RL2, A31T214CL2, A31T214SN2, A31T214IU2 |
| A31G22x | A31G226ML2, A31G226MM2, A31G226RM2, A31G226RL2, A31G226CL2, A31G224MM2, A31G224ML2, A31G224RM2, A31G224RL2, A31G224CL2, A31G226ML, A31G226MM, A31G226RM, A31G226RL, A31G226CL, A31G224MM, A31G224ML, A31G224RM, A31G224RL, A31G224CL, |
| A31G31x | A31G316MM, A31G316ML, A31G316RM, A31G316RL, A31G314MM, A31G314ML, A31G314RM, A31G314RL, A31G314CL, A31G314CU, A31G314SN, A31G313RM, A31G313RL, A31G313CL, A31G313CU, A31G313SN |
| A31M22x | A31M223CL2N, A31M223KN2N, A31M223GR2N |
| A33Mx064 | A33M3064LB, A33M4064LB |
| AC33Mx128 | AC33M8128, AC33M8128L, AC33M6128L |
| A33M11x | A33M116RL, A33M116RM, A33M114RL, A33M116CL, A33M114CL, A33M114SN |
| A34M41x | A34M418YL, A34M418VL, A34M418RL, A34M416VL, A34M416RL, A34M414VL, A34M414RL, |
| A34M420 | A34M420YL, A34M420VL, A34M420RL |
| A34M456 | A34M456VL, A34M456RL |
| A34L716 | A34L716VL, A34L716RL |
| A31G112 * | A31G112CL, A31G112SN, A31G112SQ, A31G112KN, A31G112KU, A31G112KY, A31G112GR, A31G112LU, A31G111KN, A31G111KU, A31G111GR, A31G111LU |
| A31G123 * | A31G123ML, A31G123MM, A31G123RL, A31G123RM, A31G123RN, A31G123CL, A31G123SQ, A31G123KN, A31G123KU, A31G123KY, A31G122ML, A31G122MM, A31G122RL, A31G122RM |
| A31R713 * | A31R713CL, A31R713ML, A31R713RT |
| A31L123 * | A31L123RL, A31L123CL, A31L123KN, A31L123KU, A31L123GR, A31L123LU, A31L122RL, A31L122CL, A31L122KN, A31L122KU, A31L122GR, A31L122LU |
| A31L214 * | A31L214ML, A31L214RL, A31L214CL, A31L214KN, A31L214KU, A31L213ML, A31L213RL, A31L213CL, A31L213KN, A31L213KU |
| A31L222 * | A31L222FR, A31L222FU, A31L222AR, A31L221FR, A31L221FU, A31L221AR |
| A31S134 * | A31S134RL, A31S134CL, A31S134SN, A31S134KN, A31S134KU |

* The DMA information described in this document does not apply to the products marked with an “*”.

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# 1. Flag Clearing in UART IIR Register

## 1.1 Description of Limitation

### 1.1.1 TXE Flag Clearing

If the Transmit Complete (TXE) occurs at the time of reading the UARTn_IIR, a TXE flag can be unintentionally cleared, in which case a TXE interrupt will not occur.

UARTn_IIR is a Read Clear register. If a TXE occurs “after the Read is executed and before the Clear is executed” for this register, the TXE flag will also be cleared during the Read and Clear process of UARTn_IIR.

### 1.1.2 DMA RX Complete Flag Clearing

If any of the Receive Line Status (RLS), Data Received (DR), or Transmit Hold Register Empty (THRE) interrupts are enabled with the DMA RX Complete interrupt, the DMA RX Complete Interrupt flag may be cleared regardless of intent, in which case the DMA RX Complete interrupt will not occur.

If DMA RX Complete is pending at the same time as a higher priority interrupt, reading the IIR when the higher priority interrupt is executed will clear the DMA RX Complete flag as well.

## 1.2 Workaround

To prevent unintentional clearing of these flags, you should use a method that replaces the TXE and DMA RX Complete flags.

### 1.2.1 Software Solutions

**Clear TXE Flag**

We recommended using the THRE interrupt instead of the TXE interrupt.

If you need to use the TXE interrupt, you must first check the status of TEMT in the UARTn_LSR register, which corresponds to the root of the TXE flag, and TXEIE in the UARTn_IER register, which is the TXE interrupt permission register.

When using the fallback code, the TXEIE in the UARTn_IER register must be set to '0' if the transmission is not required, and the TXEIE in the UARTn_IER register must be set to '1' if the transmission is required.

**Clear DMA RX Complete Flag**

It is not a problem to use DMA RX Complete interrupt and lower priority interrupt at the same time.

If you must use the DMA RX Complete interrupt and higher priority interrupt simultaneously, you must first check the status of DRXIEN of the UARTn_IER register and EOT of the DMAn_SR register.

After the processing, DRXIEN in the UARTn_IER register should be set to '0' or DMA should be reset so that EOT in the DMAn_SR register becomes '0'.

## Software Solution Guide Code

Figure 1 is an example code that applies the defense code described above. It uses the Interrupt Handler code for the channel UART0 as an example.

**Figure 1. Example Code: Interrupt Handler Code on UART0 Channel**

```
1     uint8_t g_un8RxBuf;
2     void UARTn_IRQHandler (void)
3     {
4         uint32_t status_IIR = 0;
5         uint32_t status_LSR = 0;
6
7         status_IIR = UART0->IIR;                  /* Make sure to read and process it only once */
8         if (status_IIR & 0x06)                    /* Handling by RLS */
9         {
10            status_LSR = UART0->LSR;
11            /* ERROR processing routine */
12        }
13        else
14        {
15            /* Issue with clearing the DMA RX Complete Flag */
16            if (((status_IIR & 0x0C) == 0x0C) ||
17                ((UART0->IER & UART_IER_DRXIEN_Msk) && (DMA0->SR & DMA_SR_EOT_Msk)))
18            {
19              UART0->IER &= ~UART_IER_DRXIEN_Msk;
20              /* DMA RX completion handling */
21              /* (Reconfigure DMA RX options and initiate DMA RX Start) */
22            }
23            else if (status_IIR & 0x04)           /* Handling by DR */
24            {
25              status_LSR = UART0->LSR;
26              g_un8RxBuf = UART0->RBR;
27                /* RX processing routine */
28            }
29
30            if ((status_IIR & 0x0A) == 0x0A)      /* Handling by DMA TX Complete */
31            {
32                /* DMA TX completion handling */
33            }
34            else if (status_IIR & 0x02)           /* Handling by THRE */
35            {
36              /* TX processing routine */
37            }
38        }
39        /* Issue with clearing the TXE flag */
40        if ((status_IIR & 0x10) ||
41            ((UART0->IER & UART_IER_TXEIE_Msk) && (UART0->LSR & UART_LSR_TEMT_Msk)))
42        {
43            /* TX processing routine */
44            /* (Set UARTn_IER &= ~UART_IER_TXEIE_Msk when packet transmission is complete) */
45            /* (Set UARTn_IER |= UART_IER_TXEIE_Msk when transmission starts) */
46        }
47    }
```

# Revision History

| Revision | Date | Notes |
|---|---|---|
| 1.00 | Nov. 29, 2024 | Initial release. |

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