UART Sampling Timing Guide

AN Rev. 1.06

Introduction

This document describes key points that users should know for UART receive operation, focusing on data sampling timing among the UART operations of ABOV 32-bit microcontrollers (Arm Cortex-M4F / M3 / M0+).

This document applies to the part number listed in Table 1.

Table 1. Applicable Devices

Base Product	Part Number
A31G11x	A31G111GR, A31G111KN, A31G111KU, A31G111LU, A31G112CL, A31G112GR, A31G112KN, A31G112KU, A31G112KY, A31G112LU, A31G112SQ
A31G12x	A31G122ML, A31G122MM, A31G122RL, A31G122RM, A31G123CL, A31G123ML, A31G123MM, A31G123RL, A31G123RM, A31G123RN, A31G123SQ
A31G21x	A31G213CL, A31G213SQ, A31G213KN, A31G213GR, A31G212CL, A31G212SQ, A31G212KN, A31G212GR
A31G22x	A31G226ML, A31G226MM, A31G226RM, A31G226RL, A31G226RL A31G224ML, A31G224MM, A31G224RM, A31G224RL, A31G224RL
A31G31x	A31G316MM, A31G316ML, A31G316RM, A31G316RL, A31G314MM, A31G314ML, A31G314RM, A31G314RL, A31G314CL, A31G314CU, A31G314SN, A31G313RM, A31G313RL, A31G313CL, A31G313CU, A31G313SN
A31G32x	A31G323CL, A31G323RL, A31G324CL, A31G324CU, A31G324RL
A33G52x	A33G524ML, A33G524MM, A33G524RL, A33G524RM, A33G526ML, A33G526MM, A33G526RL, A33G526RM, A33G526VL, A33G526VQ, A33G527RL, A33G527VL, A33G527VQ
A33G53x	A33G539VQ, A33G539VL, A33G539MM, A33G539RL A33G538VQ, A33G538VL, A33G538MM, A33G538RL
A33M11x	A33M116RL, A33M116RM, A33M116CL, A33M114RL, A33M114CL
A31M22x	A31M223CL, A31M223KN
A34M41x	A34M418YL, A34M418VL, A34M418RL, A34M416VL, A34M416RL, A34M414VL, A34M414RL
A31T21x	A31T216RL, A31T216CL, A31T216SN, A31T214RL, A31T214CL, A31T214SN
A34M420	A34M420YL, A34M420VL, A34M420RL
A34L716	A34L716VL, A34L716RL
A34M456	A34M456VL, A34M456RL, A34M456RK

Reference Documents

The following documents are available at www.abovsemi.com.

- Datasheet for 32-bit Microcontroller in Table 1
- User’s manual for 32-bit Microcontroller in Table 1

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1. Main Features

The UART functionalities of ABOV 32-bit microcontrollers are briefly described below. For more information on each device, please refer to the User's Manual of that device:

- 16450 full-duplex asynchronous serial communication ports are supported.
- Configurable standard asynchronous communication bits (Start, Stop, and Parity) are supported.
- User-programmable serial communication is available.
  - 5, 6, 7, or 8 data bits
  - Even, Odd or No Parity generation and checking
  - 1-, 1.5-, or 2-Stop bit generation and checking
- A 16-bit baud-rate generator and an 8-bit fractional compensator are included.
- Single-sampling or multi-sampling for Start and data bits
- A delay between data frames is possible.
- Separate signal polarity control for transmission and reception
- Transfer status indicated by the interrupt ID and line status registers
  - Stop bit error detection
  - Display of information about the current state of a transmission channel
  - Line break generation and checking
  - Receive error diagnosis
- A priority-based interrupt system
- Continuous communication is possible using DMA.
- Received and transmitted bytes are buffered in reserved SRAM using centralized DMA.

2. UART Receiver

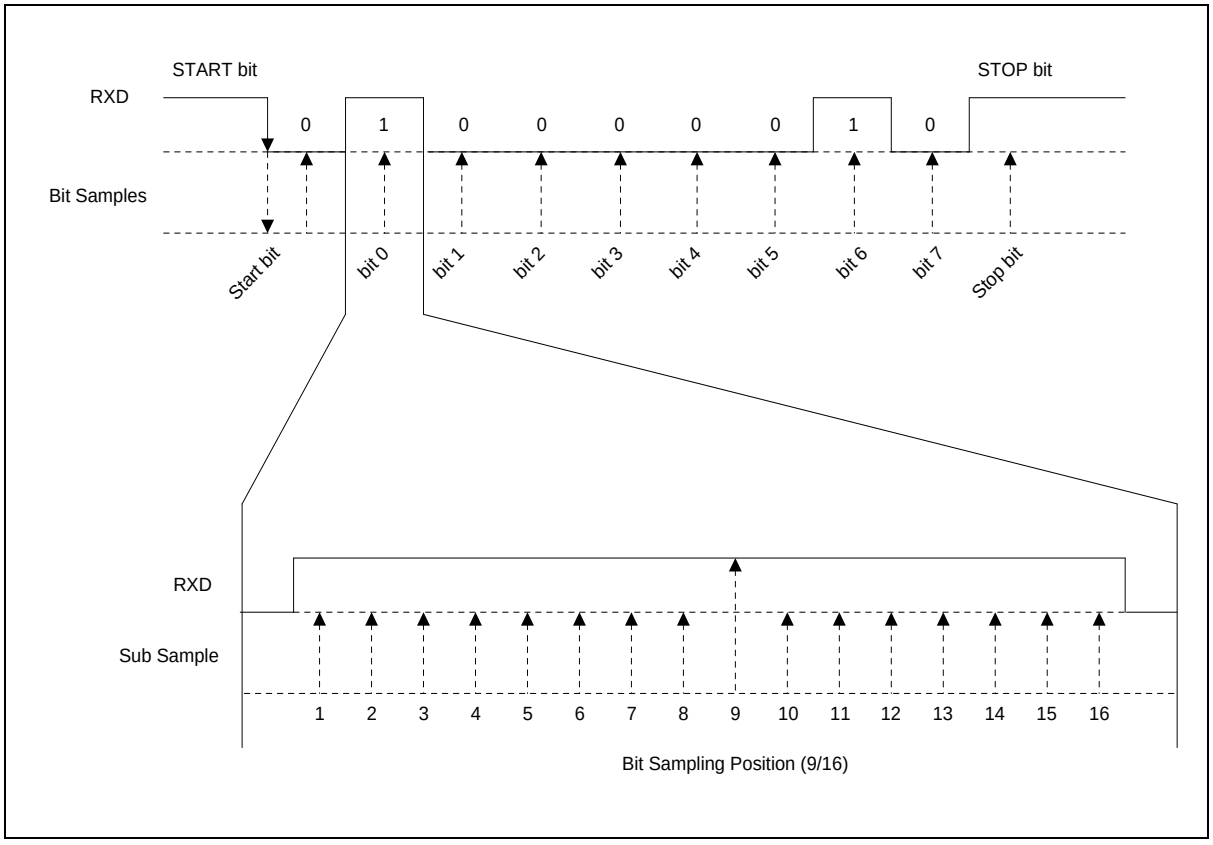
2.1 UART Receive Data Sampling Timing

In this section, the sampling timing of the UART operation is described.

Once a falling edge is detected in the receive line, the UART determines that a Start bit is being received. The UART oversamples the received data 16 times per bit beginning from the Start bit. Among the 16 samples, the value at the 9th clock pulse is determined to represent the value of the bit.

The UART receiver can receive data words of either 5, 6, 7, or 8 bits, depending on the DLEN[1:0] in the UARTn_LCR register.

Figure 1. Sampling Timing of UART Receiver



To enhance protection against external glitch noise, it is recommended to enable port debouncing in the PCU (Port Control Unit) module.

NOTE:

1. To use the port debounce function, the debounce clock must be enabled first. If the debounce function is activated without setting the debounce clock, the port may malfunction. (For detailed instructions on how to enable the debounce clock, please refer to each manual of the device.)

2.2 Start Bit Detection

On a falling edge of the Start bit, a digital filter rejects the noise signal. A pulse shorter than ((3 × (1 / baud_rate)) / 16) seconds is rejected by this filter, and a pulse longer than ((3 × (1 / baud_rate)) / 16) seconds is rejected under the multi-sampling strategy during the Start-bit sampling.

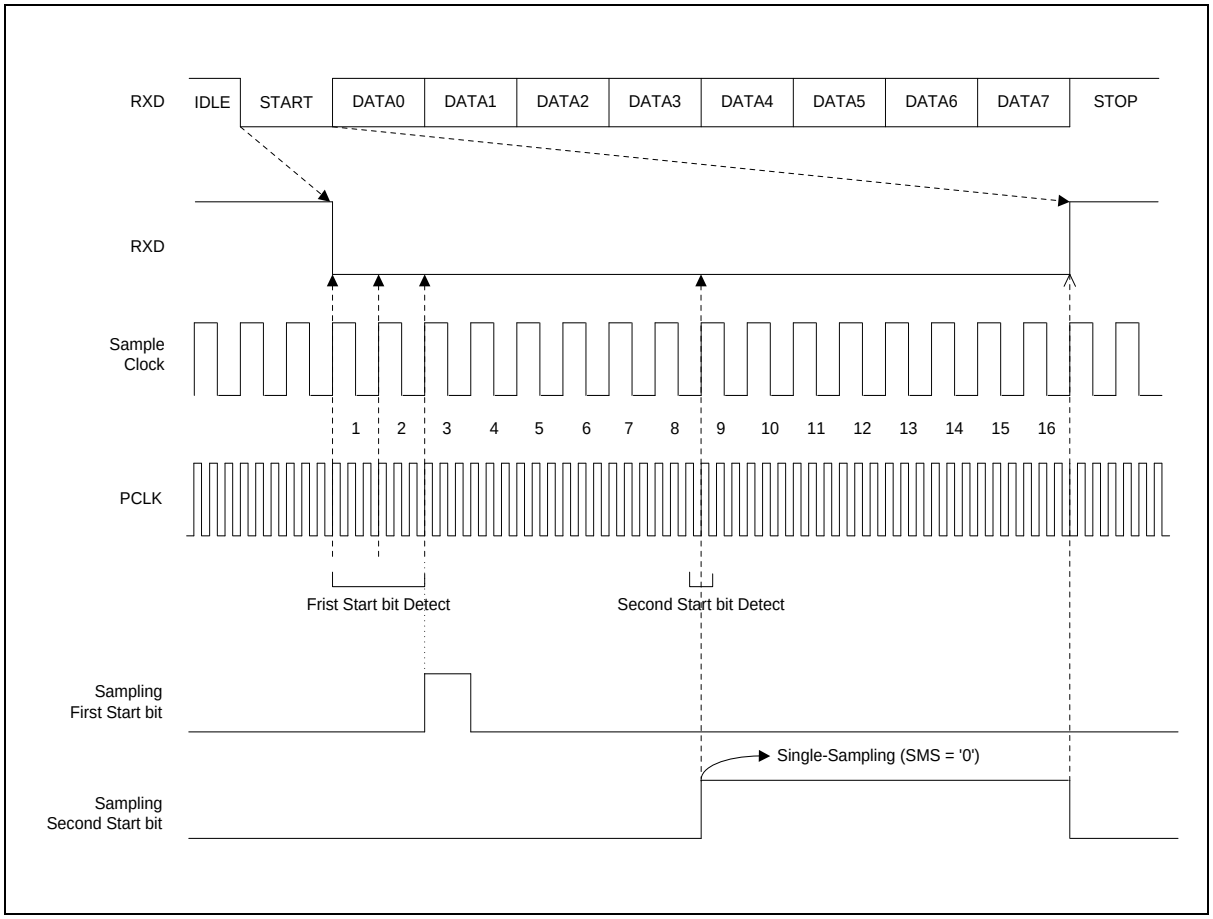
In the UART, the Start bit is detected when a specific sequence of samples is recognized, as shown below:

- Single-sampling sequence: 1 1 1 0 0 0 X X X X X 0 X X X X X X X
- Multi-sampling sequence: 1 1 1 0 0 0 X X X X 0 0 0 X X X X X X

The Start bit is confirmed (The DR in the UARTn_LSR register is set, and an interrupt is generated if the DRIE in the UARTn_IER register is set to '1') if the sampled values are at '0' in single-sampling mode.

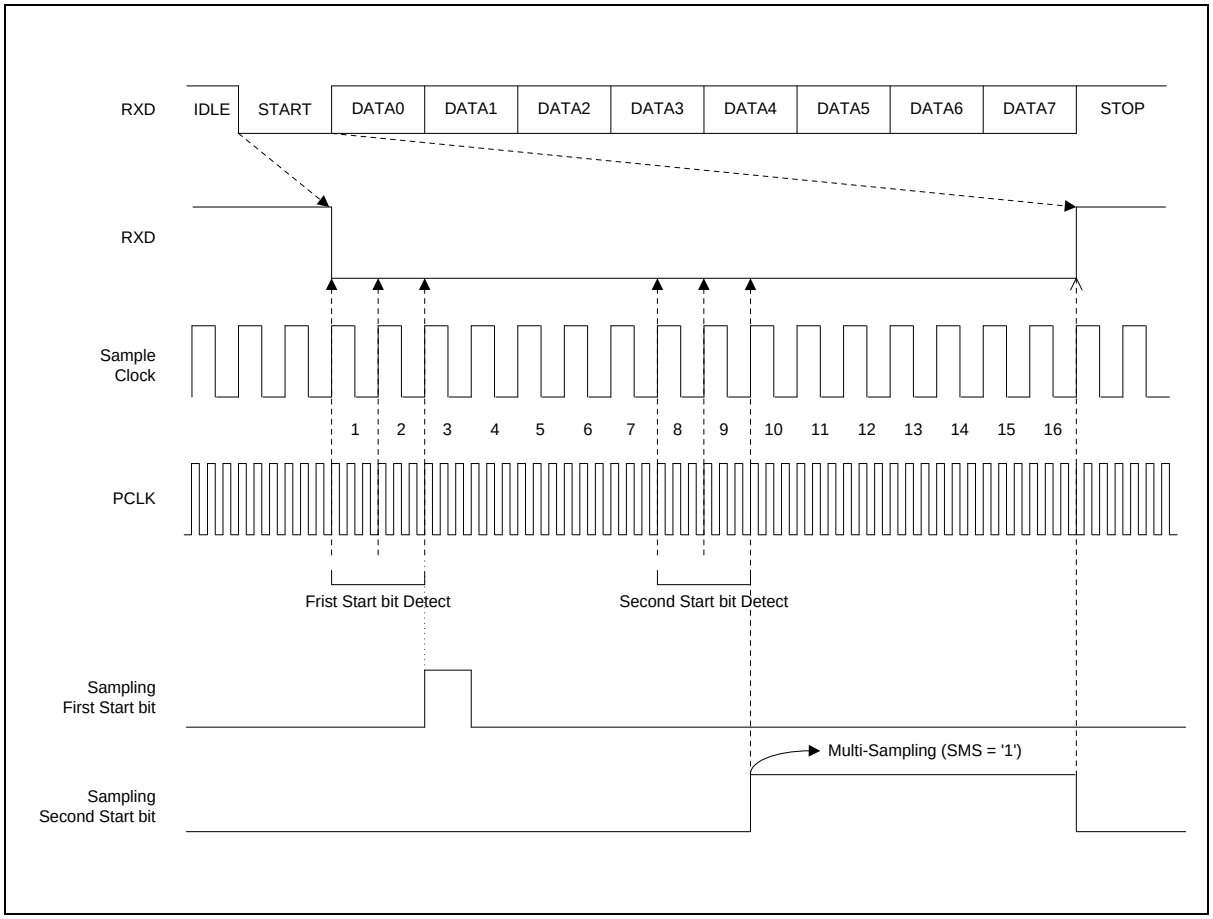
As shown in Figure 2, the first sampling on the 1st, 2nd, and 3rd sample clocks detects that all three bits are '0', and the second sampling on the 9th sample clock also detects that the bit is '0'.

Figure 2. Start Bit Detection of Single-sampling Timing



Similarly, the Start bit is confirmed (The DR in the UARTn_LSR register is set, and an interrupt is generated if the DRIE in the UARTn_IER register is set to '1'), if the 3 sampled bits are at '0' in multi-sampling mode. As shown in Figure 3, the first sampling on the 1st, 2nd, and 3rd sample clocks detects that all three bits are '0', and the second sampling on the 8th, 9th, and 10th sample clocks also detects that all three bits are '0'.

Figure 3. Start Bit Detection of Multi-sampling Timing



NOTE:

1. If the sequence is not complete, the Start bit detection stops, and the receiver returns to the Idle state, waiting for a falling edge on the RXD line.

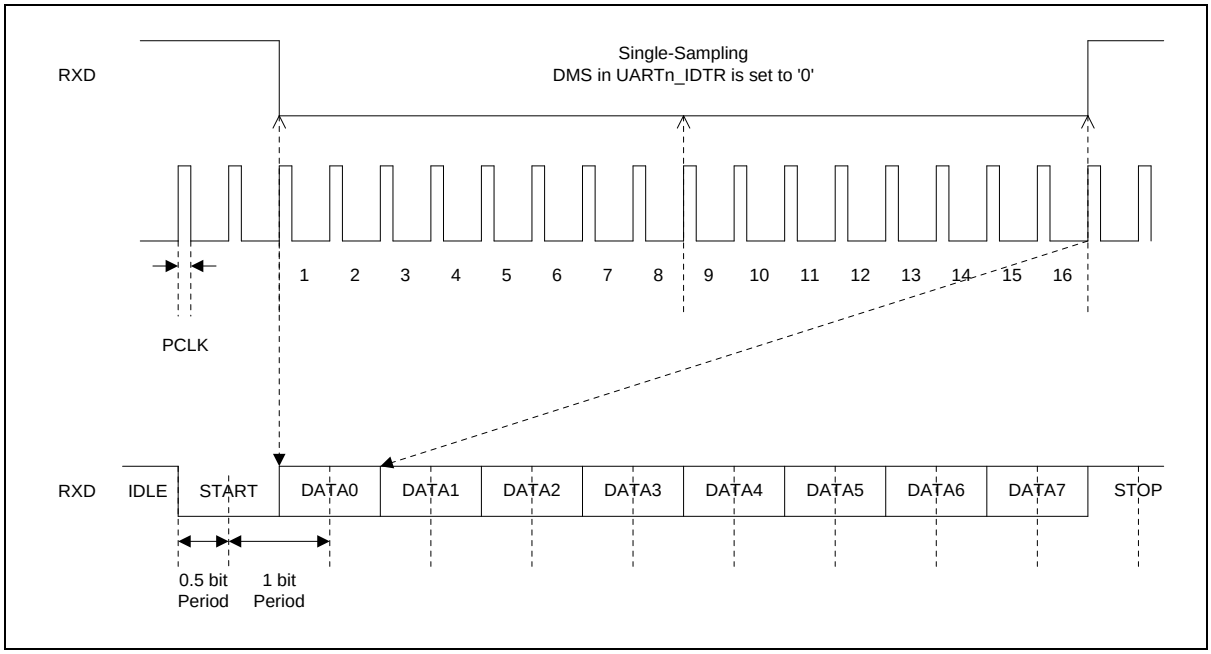
2.3 Data Bit Sampling

The DMS in the UARTn_IDTR register defines the sampling strategy for the data bits. If the DMS bit is set enabled, the value of each data bit is determined at multiple clock pulses, while if the DMS bit is set disabled, the single-sampling process determines the value of each data bit at a single clock pulse.

When the DMS in the UARTn_IDTR register is set to ‘1’, the values sampled at the 8th, 9th, and 10th clock pulses are used to represent the value of the receive data bit. The multi-sampling technique is used for data recovery by discriminating between valid incoming data and noise.

Figure 4 shows the single-sampling of data bits when the DMS is set to zero.

Figure 4. Single-Sampling Timing of Data Bit



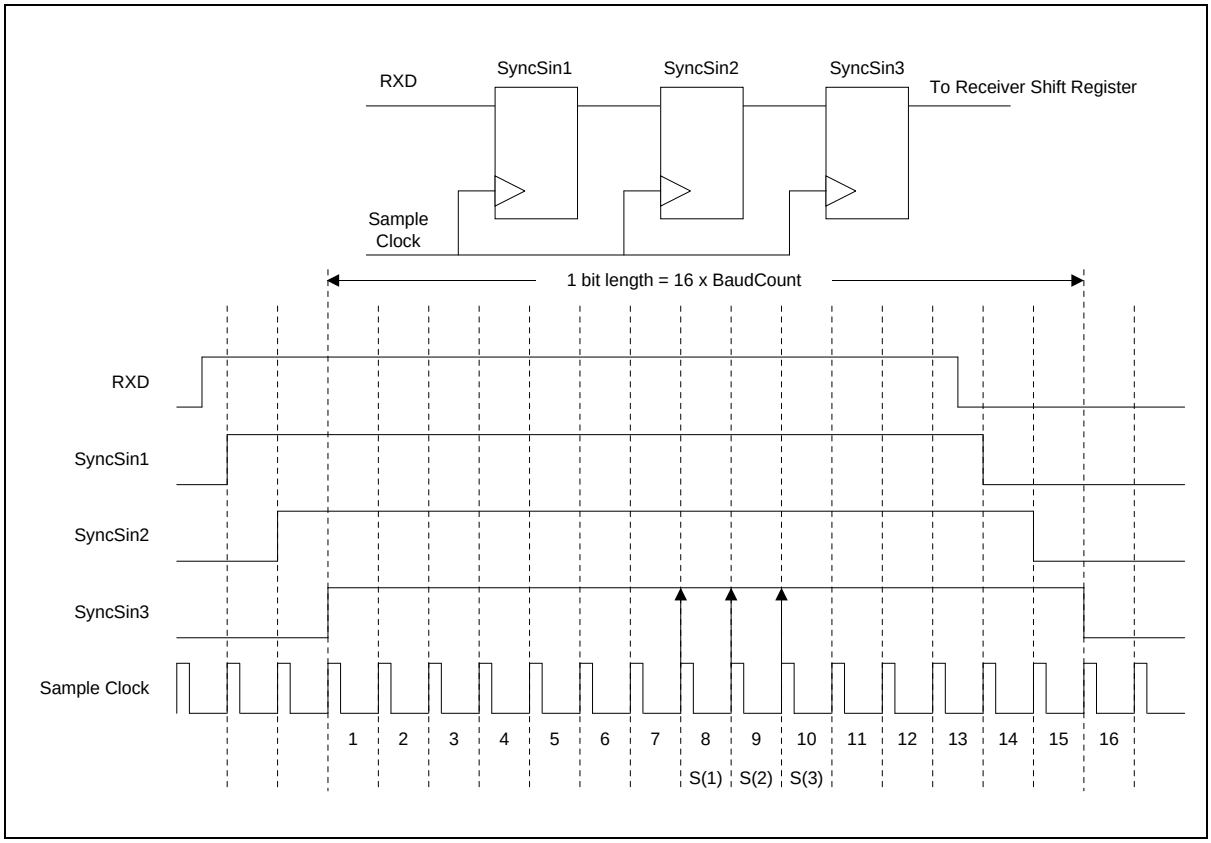
2.4 Data Sampling Strategy

An internal synchronous circuit is used in the receiver block to prevent abnormal noises in the RXD signal line.

The Start bit and data bits can be either single-sampled or multi-sampled. The SMS in the UARTn_IDTR register defines the sampling strategy for the Start bit, and the DMS in the UARTn_IDTR register defines the sampling strategy for the data bits.

Figure 5 shows a block diagram and a sampling timing diagram of the anti-noise synchronous circuit.

Figure 5. Data Sampling Timing Diagram and Block Diagram of Anti-noise Synchronous Circuit



If the DMS bit is set enabled, the value of each bit is sampled at multiple clock pulses. For the length of each data bit, values at S(1), S(2), and S(3) are taken out of 16 samples to determine the bit's value by taking the value indicated by a majority of the samples. (Refer to Table 2.)

If the DMS bit is set disabled, on the other hand, the single-sampling process takes the value at S(2) only. The DMS bit does not affect the Start bit, but the SMS bit works in a similar way for the Start bit.

Table 2. Received Bit Value determined by Sampled Data

Sampled Value	Received Bit Value	Sampled Value	Received Bit Value
000	0	100	0
001	0	101	1
010	0	110	1
011	1	111	1

2.5 Character Reception

When the falling edge is detected on the RXD Pin, the Receiver determines it as a Start bit and starts the reception operation. A data frame following the Start bit is transferred one bit at a time (LSB first) and stored in the Receiver Shift Register.

Receiving the Stop bit means that a set of communication is completed. If the UARTn_RBR (Receive data Buffer Register) register is empty, data in the Receiver Shift Register is transferred into this register and kept until it is read out over the Bus.

2.5.1 Character Reception Procedure

Once the communication is complete, data can be read from the UARTn_RBR register using DMA, Interrupt, and Polling, as described below:

- With DMA enabled, the DMA Rx Request signal is generated when data in the UARTn_RBR register is updated. The DMA stores data of the UARTn_RBR register into Memory as many times as set in the DMA counter and then sends the DMA Done signal to the UART. The UART outputs the DMA Rx Complete interrupt upon receiving the DMA Done signal.
- If the interrupt is generated, the IID[2:0] in the UARTn_IIR register must be checked. If the IID[2:0] is set to ‘010’, this means that the Reception operation is completed and the UARTn_RBR register can be read.
- To confirm the reception is completed using Polling, the DR in the UARTn_LSR register must be checked. If data is received successfully, the DR bit is set to ‘1’, and data in the UARTn_RBR register can be read. Reading the UARTn_RBR register clears the DR bit.

Revision History

Revision	Date	Notes
1.00	Dec. 27, 2021	Initial release
1.01	Jan. 5, 2022	Corrected typo.
1.02	Oct. 17, 2022	Updated the template of this document.
1.03	Dec. 19, 2023	Added A31M22x, A33G53x, A34M420 devices.
1.04	May. 27, 2024	Added A34L716 device to Table 1.
1.05	Nov. 15, 2024	Updated the disclaimer
1.06	Nov. 22, 2024	Added A34M456 device

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