A31L123, A31L122

Ultra-Low Power Cortex-M0+ Microcontroller
Flash 64/32KB, SRAM 8KB, ADC, Comparator, LCD Driver

Datasheet version 1.50

Features

- High performance Cortex-M0+ core
- 64/32KB code flash memory
- 8KB SRAM, 32-byte backup register
- Watchdog Timer
- Real time clock and calendar
- Five general purpose timers
  - Periodic, one-shot, PWM, capture
- 12-bit ADC, 1Msps, down to 1.65V
  - 16-channel inputs
- Two comparators, down to 1.65V
- External communication ports
  - 1xUSART, 2xUART, 1xLPUART, 2xSC
  - 2xI2C, up to 1Mbps
  - 2xSPI, up to 16Mbps
- Clock monitoring function for system clock
- LCD driver for up to 8x29 segments
  - 16-step contrast control
- 8/16/32-bit CRC unit, 128-bit unique ID
- Five DMA channels
- SWD debug interface
- Supports USART (UART + SPI) ISP
- Ultra-low power tech
  - 1.65V to 3.6V Supply voltage
  - 78uA/MHz in Run mode
  - 12uA in Run mode (32.768kHz, 40kHz)
  - 1.3uA Deep sleep + RTCC + retention
  - 0.6uA Deep sleep with power control
  - 8us wakeup time from all power modes
- Six types of package options
  - LQFP64-1010, LQFP48-0707
  - LQFP32-0707, QFN32-0505
  - TSSOP28, QFN24-0404
- Operating temperature, -40℃ to +105℃
  - Commercial and Industrial grade

Applications

- Smart meters, Smart card readers
- Door lock, Building & Home control
- IoT devices, Wireless sensor networks
- Portable healthcare
- Portable consumer electronics, etc.

Product Selection Table

Table 1. Device Summary

Part Number	Flash	SRAM	USART	UART	LPUART	SC	I2C	SPI	TIMER	ADC	I/O	Package
A31L123RL	64KB	8KB	1	2	1	2	2	2	5	16ch	52	64LQFP-1010
A31L123CL*	64KB	8KB	1	2	1	2	2	1	5	10ch	38	48LQFP-0707
A31L123KN*	64KB	8KB	1	2	0	2	1	1	5	10ch	26	32LQFP-0707
A31L123KU*	64KB	8KB	1	2	0	2	1	1	5	10ch	28	32QFN-0505
A31L123GR*	64KB	8KB	1	1	0	1	1	1	4	9ch	24	28TSSOP
A31L123LU*	64KB	8KB	1	1	0	0	1	1	4	9ch	20	24QFN
A31L122RL*	32KB	8KB	1	2	1	2	2	2	5	16ch	52	64LQFP-1010
A31L122CL*	32KB	8KB	1	2	1	2	2	1	5	10ch	38	48LQFP-0707
A31L122KN*	32KB	8KB	1	2	0	2	1	1	5	10ch	26	32LQFP-0707
A31L122KU*	32KB	8KB	1	2	0	2	1	1	5	10ch	28	32QFN-0505
A31L122GR*	32KB	8KB	1	1	0	1	1	1	4	9ch	24	28TSSOP
A31L122LU*	32KB	8KB	1	1	0	0	1	1	4	9ch	20	24QFN

* For available options or further information on the devices with "*" marks, please contact the ABOV Sales Office.

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1 Description

The ultra-low power A31L12x series is a microcontroller based on ARM Cortex-M0+ core with a flash memory of up to 64KB, and an SRAM of 8KB. Operation voltage of the device is 1.65V to 3.6V. It provides a highly flexible and cost effective solution for many embedded control applications.

The ultra-low power A31L12x series has 16-bit timers, Real timer and calendar, 12-bit ADC, Comparator, CRC generator, UART, USART, LPUART, I2C, SPI, Smart card interface, LCD driver/controller, DMA, etc. The A31L12x series also has a POR, LVR, LVI, and an internal RC oscillator. The ultra-low power A31L12x series support sleep and deep sleep modes to reduce power consumption. The A31L12x series is suitable for ultra-low power applications.

1.1 Device overview

Table 2. A31L12x series features and peripheral counts

Device / Peripheral	A31L12x
CPU	Cortex-M0+
Flash ROM (Kbytes)	32/64
SRAM (bytes)	8KB, 32-byte backup register
I/O	52 programmable
Timers	Watchdog timer
	Real time clock and calendar
	Four general purpose timers and one low power timer — Periodic, one-shot, PWM, capture mode
LCD driver	• 29 segments and 8 commons • Duty selectable, resistor bias, and 16-step contrast control
DMA	Five DMA channels, ADC/USART/UART/I2C/SPI/SCI
ADC	16-channel input, 12-bit ADC with 1Msps, down to 1.65V
Comparator	• Two comparators, down to 1.65V
CRC generator	• 8/16/32-bit CRC generator, CRC-8/16/32, CRC-CCITT
External communication ports	• 1 USART (UART + SPI), 2 UARTs, 2 SCIs • 1 LPUART, up to 9600bps with 32.768kHz • 2 I^2Cs, up to 1Mbps • 2 SPIs, up to 16Mbps
128-bit Unique ID	Supported
System fail-safe function	Clock monitoring
Debug interface	SWD debug interface
Ultra-low power tech	• 1.65V to 3.6V supply voltage • 78uA/MHz in Run mode • 12uA in Run mode (32.768kHz, 40kHz) • 1.3uA deep sleep + RTCC + SRAM retention • 0.6uA deep sleep with power control • 8us wakeup time from all power modes
Packages	LQFP 64-1010 (0.5mm pitch)
	LQFP 48-0707 (0.5mm pitch)
	LQFP 32-0707 (0.8mm pitch)
	QFN 32-0505 (0.5mm pitch)
	TSSOP 28
	QFN 24-0404 (0.4mm pitch)
Operating temperature	-40℃ to +85℃ (commercial grade)
	-40℃ to +105℃ (industrial grade)

1.2 Block diagram

Figure 1 shows a block diagram of A31L12x series.

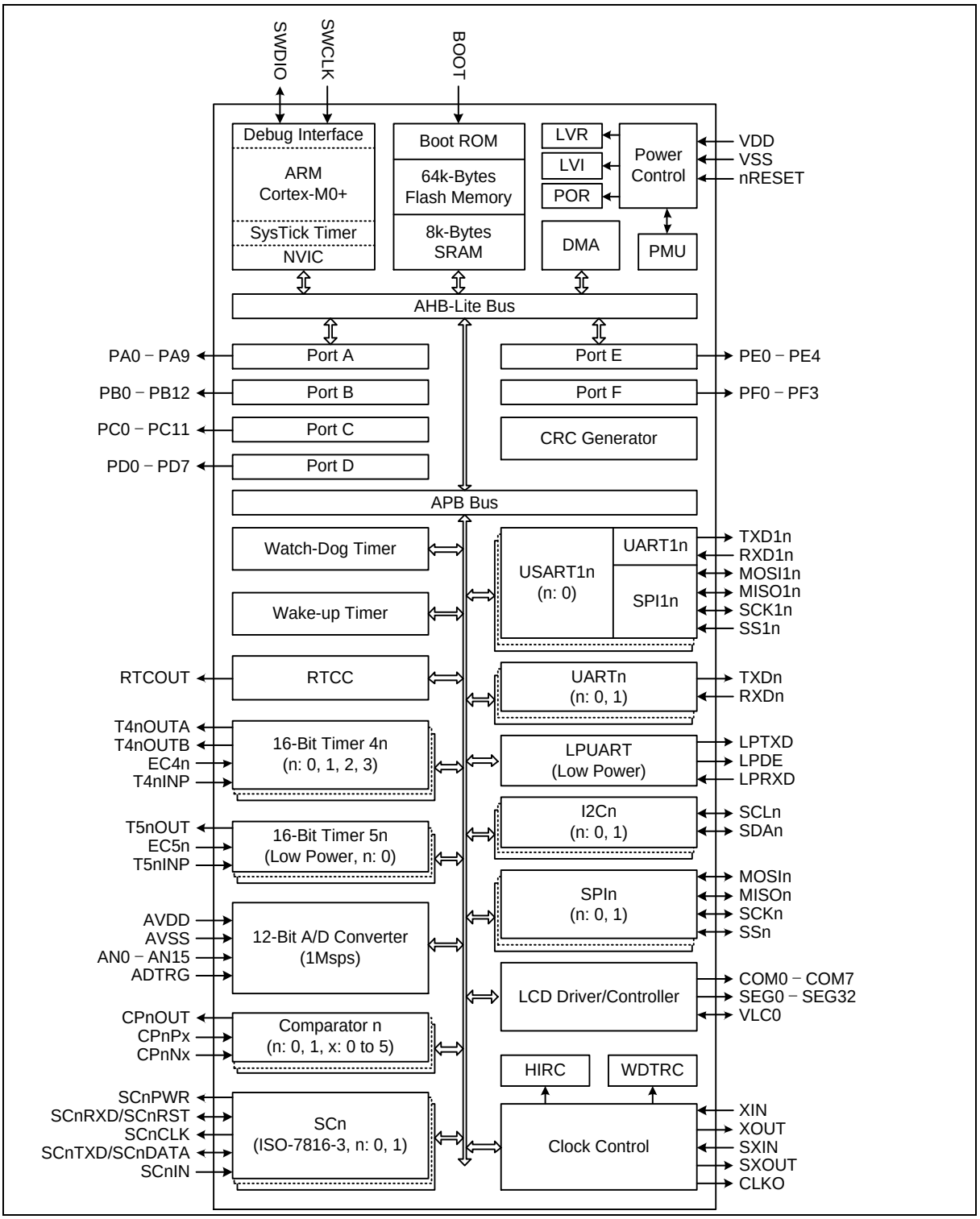


Figure 1. A31L12x Series Block Diagram

1.3 Functional description

The following section provides an overview of the features of the A31L12x series microcontroller.

1.3.1 ARM Cortex-M0+

Cortex-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area-optimized, low-power processor.

On core system timer (SYSTICK) provides a simple 24-bit timer to use as a real time operating system (RTOS) or as a simple counter. The processor implements the ARMv6-M Thumb instruction set, including a number of 32-bit instructions that use Thumb-2 technology. Hardware single-cycle multiplication is available.

Integrated Nested Vectored Interrupt Controller (NVIC) provides deterministic interrupt handling.

It also supports SWD debugging features.

1.3.2 Nested Vector-Interrupt Controller (NVIC)

External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC embedded in the Cortex-M0+ processor core is capable of low latency interrupts processing and efficient processing of late arriving interrupts.

All NVIC registers are only accessible using word transfers.

1.3.3 64KB Internal Code Flash Memory

A31L12x series has built-in 64KB code flash memory. It supports self-programming feature, and supports ISP and JTAG programming in boot or debug mode.

1.3.4 8KB Internal SRAM

On-chip 8KB SRAM is used as a working memory space and as a program code area temporarily.

1.3.5 Boot Logic

A boot logic supports flash programming. The boot logic will be activated when the external boot pin was set to boot mode.

1.3.6 System Control Unit (SCU)

An SCU block manages internal power, clock, reset and operation mode. It also controls the analog blocks (Oscillator Block, VDC and LVR).

1.3.7 Power Management Unit (PMU)

A PMU block manages power of internal core, flash, SRAM, logic, and peripheral block in run, sleep, and deep sleep mode. It also controls the wake-up time from sleep and deep sleep mode

1.3.8 24-bit Watchdog Timer (WDT)

A Watchdog timer monitors the system. It generates internal reset or interrupt to notice abnormal status of the system.

1.3.9 Multi-purpose 16-bit Timer

Four-channel 16-bit timers and one-channel low power general-purposed 16-bit timers support the functions introduced below:

- Periodic timer mode
- Counter mode
- PWM mode
- Capture mode

1.3.10 Real time clock and calendar

A real time clock and a calendar can run in sleep and deep sleep mode. The RTCC is not reset by a system reset except a power-on reset.

1.3.11 USART (UART and SPI)

USART supports UART and SPI mode. The A31L12x series has 1 channel USART module.

Boot mode uses this USART block to download flash program.

1.3.12 Inter-Integrated Circuit Interface (I2C)

A31L12x series has two channels of I2C block and supports up to 1MHz I2C communication. Master and slave modes are available.

1.3.13 Serial Peripheral Interface (SPI)

A31L12x series has two channels of SPI block and supports up to 16MHz communication. Master and slave modes are available.

1.3.14 Universal Asynchronous Receiver/Transmitter (UART)

A31L12x series has two channels of UART block. For accurate baud rate control, a fractional baud-rate generation feature is available.

1.3.15 Low Power Universal Asynchronous Receiver/Transmitter (LPUART)

A31L12x series has one channel of low power UART block. The LPUART is available up to 9600bps with 32.768KHz sub oscillator.

1.3.16 Smartcard Interface (SC)

A31L12x series has two channels of SC blocks. The block supports UART and smartcard mode. The block has also baud-rate compensation, receive time out data, and extra guard time registers.

1.3.17 General PORT I/Os

10-bit PA port, 13-bit PB port, 12-bit PC port, 8-bit PD port, 5-bit PE port, and 4-bit PF port are available and provide multiple functions.

- General I/O port
- External interrupt input port and on-chip input debounce filter
- Programmable pull-up, pull-down, and open-drain selection

1.3.18 12-bit Analog-to-Digital Converter (ADC)

An ADC can convert analog signal at a conversion rate of up to 1Msps. 16-channel analog MUX provides various combinations of data from external analog signals.

1.3.19 Comparator

A31L12x series has two comparator blocks. The block has an internal reference for channel.

1.3.20 LCD Driver/Controller

An LCD driver supports an internal resistor bias, 16-step contrast control, automatic bias control, and various duties.

1.3.21 Cyclic Redundancy Check (CRC) Generator

A31L12x series has four polynomials for the CRC generator: CRC-CCITT, CRC-8, CRC-16, and CRC-32.

2 Pinouts and pin descriptions

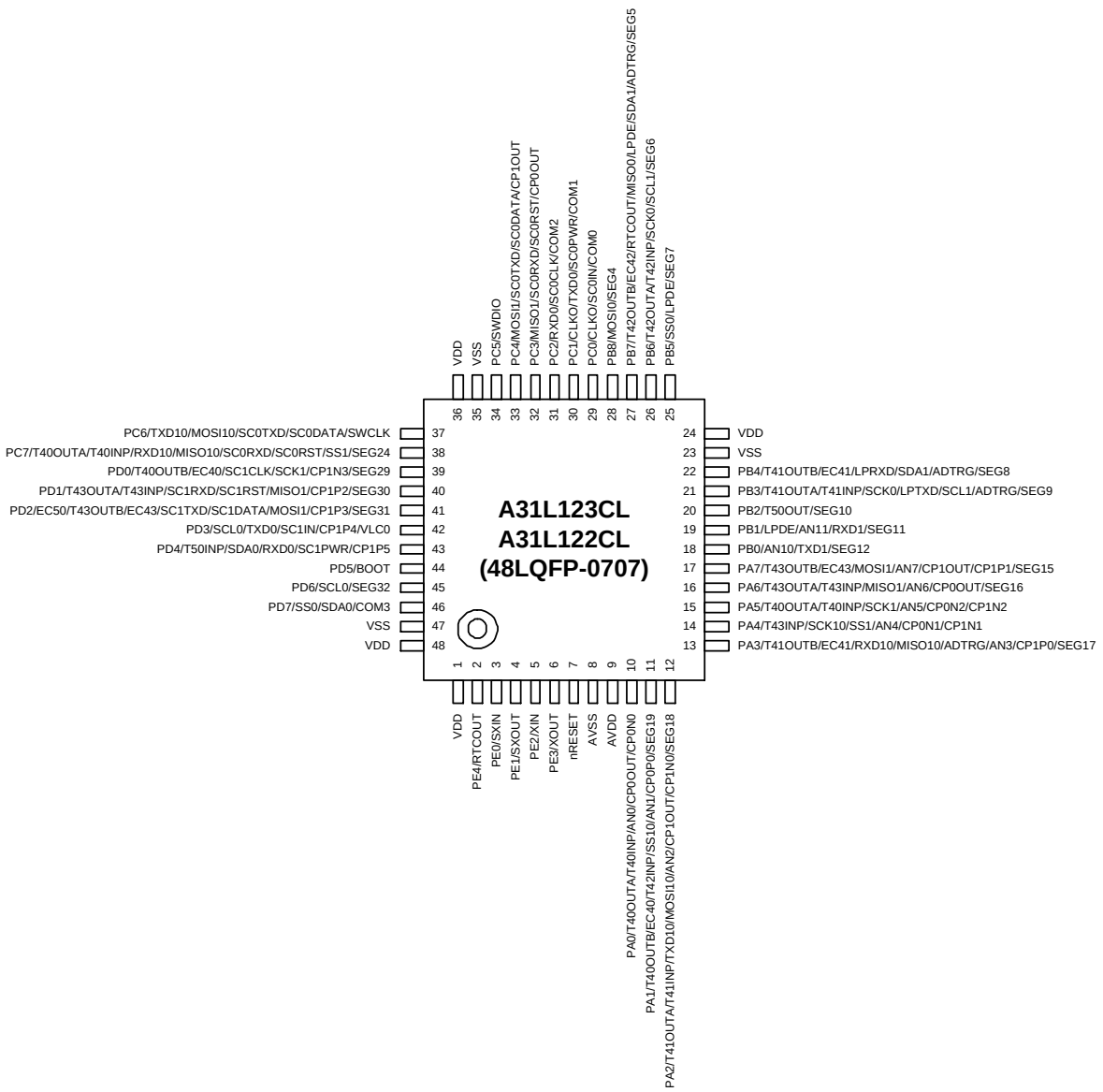
In chapter 2, pinouts and pin descriptions of A31L12x series are introduced.

2.1 Pinouts

NOTES:

1. PD[4:1] pins are 5V tolerant I/O. The corresponding internal resistor must be disabled by s/w to use as 5V I/O. To use as 5V tolerant output, an external pull-up resistor must be used by application and the corresponding pins must be configured with open-drain output by s/w.
2. VDD should be greater than or equal to 2.0V if CP1P2, CP1P3, CP1P4, and CP1P5 are used as comparator pins for alternative function.

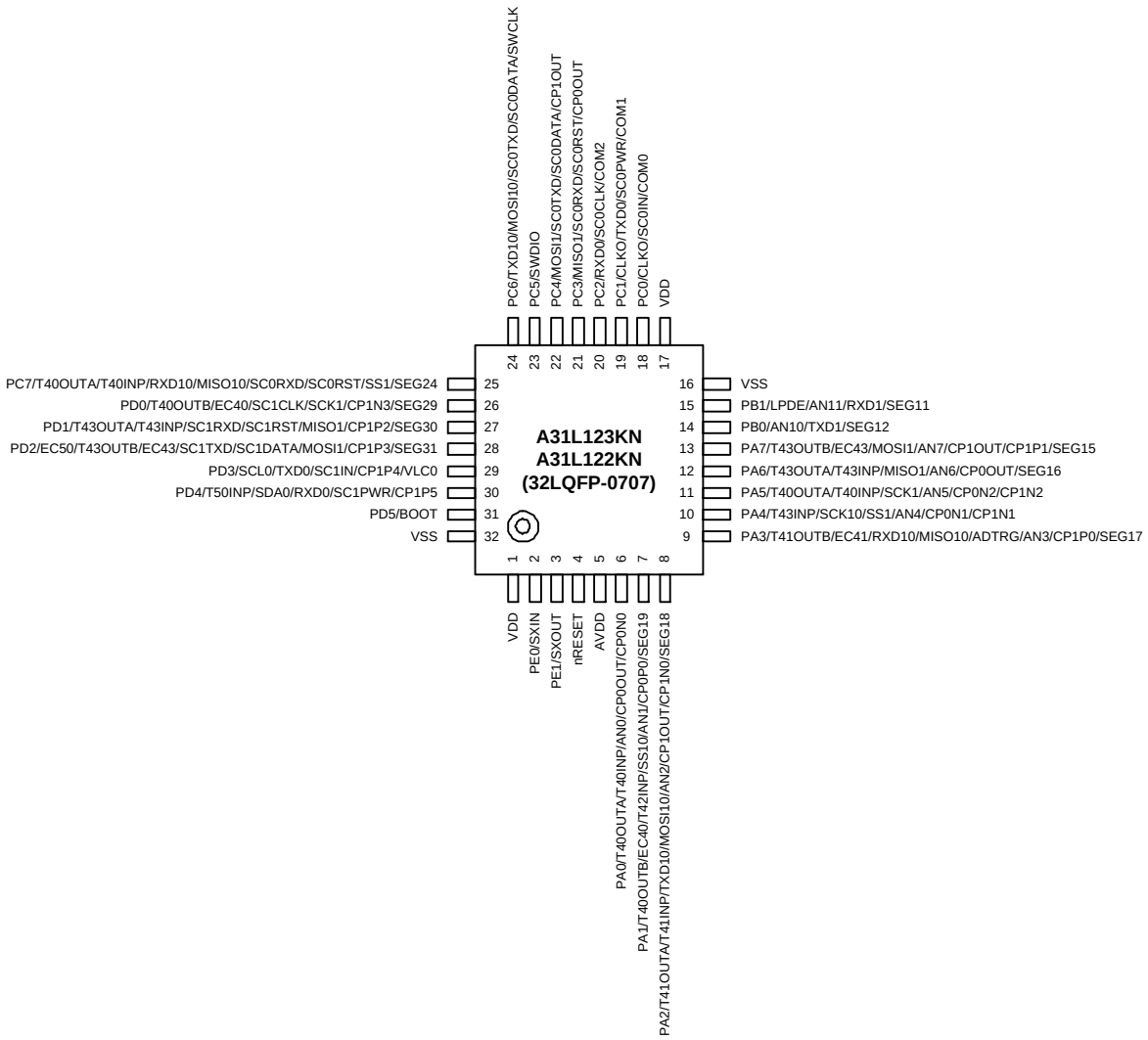
Figure 2. LQFP-64 Pinouts



NOTES:

1. The PA8-PA9, PB9-PB12, PC8-PC11 and PF0-PF3 pins should be selected as a push-pull output or an input with pullup or pull-down resistor by software control when the 48LQFP package is used.
2. PD[4:1] pins are 5V tolerant I/O. The corresponding internal resistor must be disabled by s/w to use as 5V I/O. To use as 5V tolerant output, an external pull-up resistor must be used by application and the corresponding pins must be configured with open-drain output by s/w.
3. VDD should be greater than or equal to 2.0V if CP1P2, CP1P3, CP1P4, and CP1P5 are used as comparator pins for alternative function.

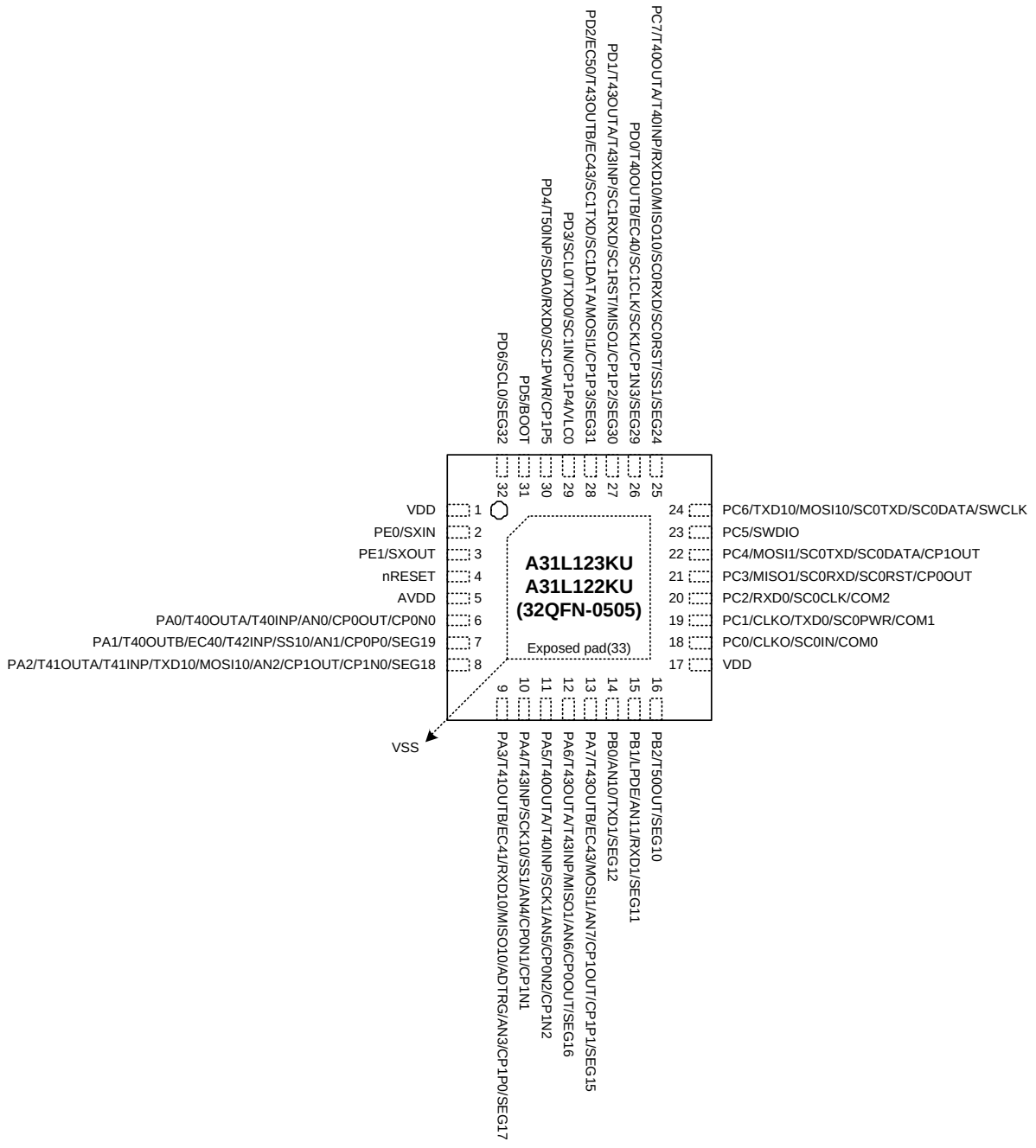
Figure 3. LQFP-48 Pinouts



NOTES:

1. The PA8-PA9, PB2-PB12, PC8-PC11, PD6-PD7, PE2-PE4 and PF0-PF3 pins should be selected as a push-pull output or an input with pullup or pull-down resistor by software control when the 32LQFP package is used.
2. PD[4:1] pins are 5V tolerant I/O. The corresponding internal resistor must be disabled by s/w to use as 5V I/O. To use as 5V tolerant output, an external pull-up resistor must be used by application and the corresponding pins must be configured with open-drain output by s/w.
3. VDD should be greater than or equal to 2.0V if CP1P2, CP1P3, CP1P4, and CP1P5 are used as comparator pins for alternative function.

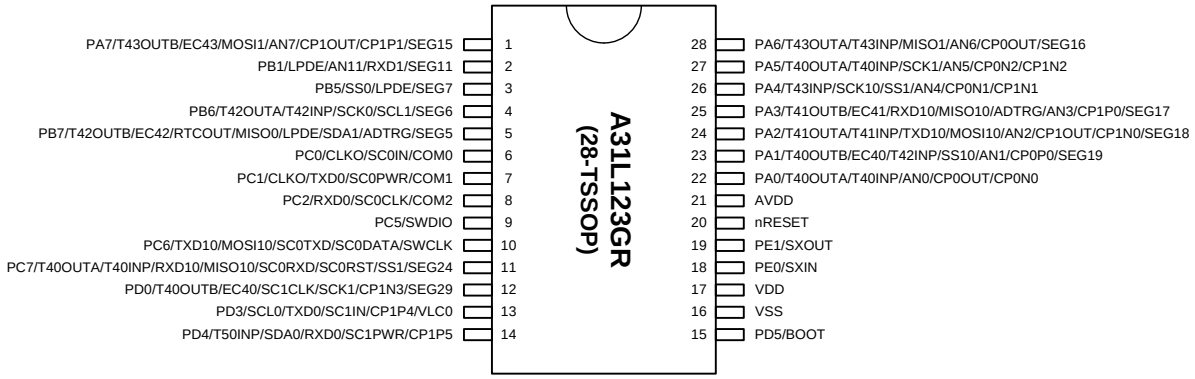
Figure 4. LQFP-32 Pinouts



NOTES:

1. The PA8-PA9, PB3-PB12, PC8-PC11, PD7, PE2-PE4 and PF0-PF3 pins should be selected as a push-pull output or an input with pullup or pull-down resistor by software control when the 32QFN package is used.
2. PD[4:1] pins are 5V tolerant I/O. The corresponding internal resistor must be disabled by s/w to use as 5V I/O. To use as 5V tolerant output, an external pull-up resistor must be used by application and the corresponding pins must be configured with open-drain output by s/w.
3. VDD should be greater than or equal to 2.0V if CP1P2, CP1P3, CP1P4, and CP1P5 are used as comparator pins for alternative function.

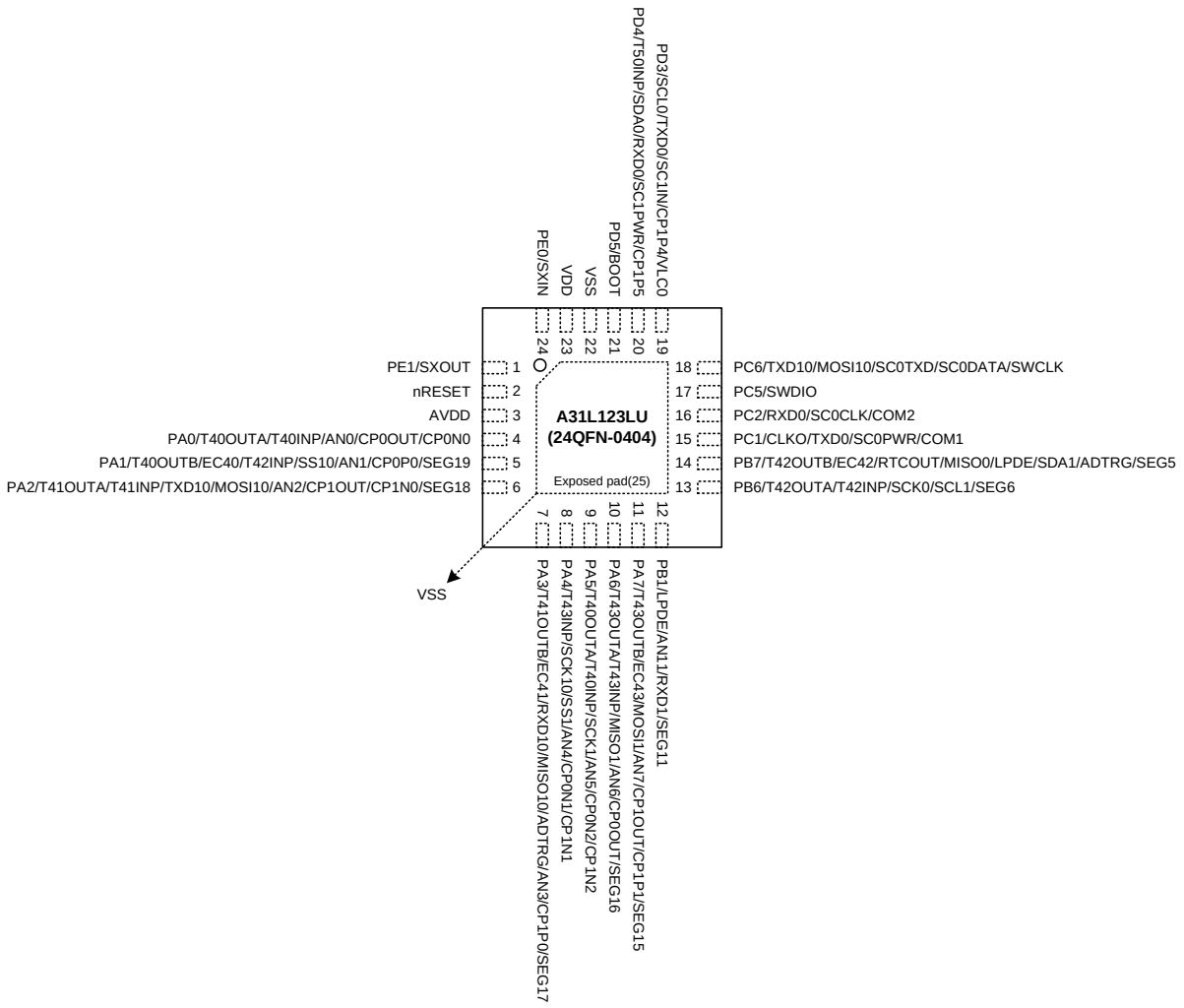
Figure 5. QFN-32 Pinouts



NOTES:

1. The PA8-PA9, PB0, PB2-PB4, PB8-PB12, PC3-PC4, PC8-PC11, PD1-PD2, PD6-PD7, PE2-PE4 and PF0-PF3 pins should be selected as a push-pull output or an input with pullup or pull-down resistor by software control when the 28TSSOP package is used.
2. PD[4:1] pins are 5V tolerant I/O. The corresponding internal resistor must be disabled by s/w to use as 5V I/O. To use as 5V tolerant output, an external pull-up resistor must be used by application and the corresponding pins must be configured with open-drain output by s/w.
3. VDD should be greater than or equal to 2.0V if CP1P2, CP1P3, CP1P4, and CP1P5 are used as comparator pins for alternative function.

Figure 6. TSSOP-28 Pinouts



NOTES:

1. The PA8-PA9, PB0, PB2-PB5, PB8-PB12, PC0, PC3-PC4, PC7-PC11, PD0-PD2, PD6-PD7, PE2-PE4 and PF0-PF3 pins should be selected as a push-pull output or an input with pullup or pull-down resistor by software control when the 24QFN package is used.
2. PD[4:1] pins are 5V tolerant I/O. The corresponding internal resistor must be disabled by s/w to use as 5V I/O. To use as 5V tolerant output, an external pull-up resistor must be used by application and the corresponding pins must be configured with open-drain output by s/w.
3. VDD should be greater than or equal to 2.0V if CP1P2, CP1P3, CP1P4, and CP1P5 are used as comparator pins for alternative function.

Figure 7. QFN-24 Pinouts

2.2 Pin description

Table 3 shows pin configuration containing several pairs of power/ground and other dedicated pins. Multi-function pins have up to eight selections of functions including GPIO.

Table 3. Pin Description

Pin number						Pin name	Type	Description	Remark
LQFP-64	LQFP-48	LQFP-32	QFN-32	TSSOP-28	QFN-24				
1	1	1	1	-	-	VDD	P	VDD	
2	2	-	-	-	-	PE4*	IOUDS	PORT E Bit 4 Input/Output	
						RTCOUT	O	Real Time Clock Output	
3	3	2	2	18	24	PE0*	IOUDS	PORT E Bit 0 Input/Output	
						SXIN	IA	Sub Oscillator Input	
4	4	3	3	19	1	PE1*	IOUDS	PORT E Bit 1 Input/Output	
						SXOUT	OA	Sub Oscillator Output	
5	5	-	-	-	-	PE2*	IOUDS	PORT E Bit 2 Input/Output	
						XIN	IA	Main Oscillator Input	
6	6	-	-	-	-	PE3*	IOUDS	PORT E Bit 3 Input/Output	
						XOUT	OA	Main Oscillator Output	
7	7	4	4	20	2	nRESET	Input	External Reset Input	Always pull-up
8	-	-	-	-	-	PF0*	IOUDS	PORT F Bit 0 Input/Output	
						EC50	I	Timer 50 Event Count Input	
						AN12	IA	A/D Converter Analog Input 12	
						SEG23	OA	LCD Segment Signal Output	
9	-	-	-	-	-	PF1*	IOUDS	PORT F Bit 1 Input/Output	
						T50OUT	O	Timer 50 Pulse Output	
						AN13	IA	A/D Converter Analog Input 13	
						SEG22	OA	LCD Segment Signal Output	
10	-	-	-	-	-	PF2*	IOUDS	PORT F Bit 2 Input/Output	
						T50INP	I	Timer 50 Capture/Clear Input	
						MISO0	I/O	SPI Master Input, Slave Output	
						AN14	IA	A/D Converter Analog Input 14	
						SEG21	OA	LCD Segment Signal Output	
11	-	-	-	-	-	PF3*	IOUDS	PORT F Bit 3 Input/Output	
						MOSI0	I/O	SPI Master Output, Slave Input	
						AN15	IA	A/D Converter Analog Input 15	
						SEG20	OA	LCD Segment Signal Output	
12	8	-	-	-	-	AVSS	PA	Analog Ground	
13	9	5	5	21	3	AVDD	PA	Analog Power	

Table 3. Pin Description (continued)

Pin number						Pin name	Type	Description	Remark
LQFP-64	LQFP-48	LQFP-32	QFN-32	TSSOP-28	QFN-24				
14	10	6	6	22	4	PA0*	IOUDS	PORT A Bit 0 Input/Output	
						T40OUTA	O	Timer 40 Pulse Output	
						T40INP	I	Timer 40 Capture/Force Input	
						AN0	IA	A/D Converter Analog Input 0	
						CP0OUT	OA	Comparator 0 Output	
						CP0N0	IA	Comparator 0 Negative Input	
15	11	7	7	23	5	PA1*	IOUDS	PORT A Bit 1 Input/Output	
						T40OUTB	O	Timer 40 Pulse Output	
						EC40	I	Timer 40 Event Count Input	
						T42INP	I	Timer 42 Capture/Force Input	
						SS10	I	SPI Slave Select Input	
						AN1	IA	A/D Converter Analog Input 1	
						CP0P0	IA	Comparator 0 Positive Input	
						SEG19	OA	LCD Segment Signal Output	
16	12	8	8	24	6	PA2*	IOUDS	PORT A Bit 2 Input/Output	
						T41OUTA	O	Timer 41 Pulse Output	
						T41INP	I	Timer 41 Capture/Force Input	
						TXD10	O	UART Data Output	
						MOSI10	I/O	SPI Master Output, Slave Input	
						AN2	IA	A/D Converter Analog Input 2	
						CP1OUT	OA	Comparator 1 Output	
						CP1N0	IA	Comparator 1 Negative Input	
						SEG18	OA	LCD Segment Signal Output	
17	13	9	9	25	7	PA3*	IOUDS	PORT A Bit 3 Input/Output	
						T41OUTB	O	Timer 41 Pulse Output	
						EC41	I	Timer 41 Event Count Input	
						RXD10	I	UART Data Input	
						MISO10	I/O	SPI Master Input, Slave Output	
						ADTRG	I	A/D Converter Trigger Input	
						AN3	IA	A/D Converter Analog Input 3	
						CP1P0	IA	Comparator 1 Positive Input	
						SEG17	OA	LCD Segment Signal Output	
18	-	-	-	-	-	VSS	P	Ground	
19	-	-	-	-	-	VDD	P	Power	
20	14	10	10	26	8	PA4*	IOUDS	PORT A Bit 4 Input/Output	
						T43INP	I	Timer 43 Capture/Force Input	
						SCK10	I/O	SPI Clock Input/Output	
						SS1	I	SPI Slave Select Input	
						AN4	IA	A/D Converter Analog Input 4	
						CP0N1	IA	Comparator 0 Negative Input	
						CP1N1	IA	Comparator 1 Negative Input	

Table 3. Pin Description (continued)

Pin number						Pin name	Type	Description	Remark
LQFP-64	LQFP-48	LQFP-32	QFN-32	TSSOP-28	QFN-24				
21	15	11	11	27	9	PA5*	IOUDS	PORT A Bit 5 Input/Output	
						T40OUTA	O	Timer 40 Pulse Output	
						T40INP	I	Timer 40 Capture/Force Input	
						SCK1	I/O	SPI Clock Input/Output	
						AN5	IA	A/D Converter Analog Input 5	
						CP0N2	IA	Comparator 0 Negative Input	
						CP1N2	IA	Comparator 1 Negative Input	
22	16	12	12	28	10	PA6*	IOUDS	PORT A Bit 6 Input/Output	
						T43OUTA	O	Timer 43 Pulse Output	
						T43INP	I	Timer 43 Capture/Force Input	
						MISO1	I/O	SPI Master Input, Slave Output	
						AN6	IA	A/D Converter Analog Input 6	
						CP0OUT	OA	Comparator 0 Output	
						SEG16	OA	LCD Segment Signal Output	
23	17	13	13	1	11	PA7*	IOUDS	PORT A Bit 7 Input/Output	
						T43OUTB	O	Timer 43 Pulse Output	
						EC43	I	Timer 43 Event Count Input	
						MOSI1	I/O	SPI Master Output, Slave Input	
						AN7	IA	A/D Converter Analog Input 7	
						CP1OUT	OA	Comparator 1 Output	
						CP1P1	IA	Comparator 1 Positive Input	
						SEG15	OA	LCD Segment Signal Output	
24	-	-	-	-	-	PA8*	IOUDS	PORT A Bit 8 Input/Output	
						LPTXD	O	LPUART Data Output	
						AN8	IA	A/D Converter Analog Input 8	
						SEG14	OA	LCD Segment Signal Output	
25	-	-	-	-	-	PA9*	IOUDS	PORT A Bit 9 Input/Output	
						LPRXD	I	LPUART Data Input	
						AN9	IA	A/D Converter Analog Input 9	
						SEG13	OA	LCD Segment Signal Output	
26	18	14	14	-	-	PB0*	IOUDS	PORT B Bit 0 Input/Output	
						AN10	IA	A/D Converter Analog Input 10	
						TXD1	O	UART Data Output	
						SEG12	OA	LCD Segment Signal Output	
27	19	15	15	2	12	PB1*	IOUDS	PORT B Bit 1 Input/Output	
						LPDE	O	LPUART DE Signal Output	
						AN11	IA	A/D Converter Analog Input 11	
						RXD1	I	UART Data Input	
						SEG11	OA	LCD Segment Signal Output	
28	20	-	16	-	-	PB2*	IOUDS	PORT B Bit 2 Input/Output	
						T50OUT	O	Timer 50 Pulse Output	
						SEG10	OA	LCD Segment Signal Output	

Table 3. Pin Description (continued)

Pin number						Pin name	Type	Description	Remark
LQFP-64	LQFP-48	LQFP-32	QFN-32	TSSOP-28	QFN-24				
29	21	-	-	-	-	PB3*	IOUDS	PORT B Bit 3 Input/Output	
						T41OUTA	O	Timer 41 Pulse Output	
						T41INP	I	Timer 41 Capture/Force Input	
						SCK0	I/O	SPI Clock Input/Output	
						LPTXD	O	LPUART Data Output	
						SCL1	I/O	I2C Clock Input/Output	
						ADTRG	I	A/D Converter Trigger Input	
						SEG9	OA	LCD Segment Signal Output	
30	22	-	-	-	-	PB4*	IOUDS	PORT B Bit 4 Input/Output	
						T41OUTB	O	Timer 41 Pulse Output	
						EC41	I	Timer 41 Event Count Input	
						LPRXD	I	LPUART Data Input	
						SDA1	I/O	I2C Data Input/Output	
						ADTRG	I	A/D Converter Trigger Input	
						SEG8	OA	LCD Segment Signal Output	
31	23	16	-	16	22	VSS	P	Ground	
32	24	17	17	17	23	VDD	P	Power	
33	25	-	-	3	-	PB5*	IOUDS	PORT B Bit 5 Input/Output	
						SS0	I	SPI Slave Select Input	
						LPDE	O	LPUART DE Signal Output	
						SEG7	OA	LCD Segment Signal Output	
34	26	-	-	4	13	PB6*	IOUDS	PORT B Bit 6 Input/Output	
						T42OUTA	O	Timer 42 Pulse Output	
						T42INP	I	Timer 42 Capture/Force Input	
						SCK0	I/O	SPI Clock Input/Output	
						SCL1	I/O	I2C Clock Input/Output	
						SEG6	OA	LCD Segment Signal Output	
35	27	-	-	5	14	PB7*	IOUDS	PORT B Bit 7 Input/Output	
						T42OUTB	O	Timer 42 Pulse Output	
						EC42	I	Timer 42 Event Count Input	
						RTCOUT	O	Real Time Clock Output	
						MISO0	I/O	SPI Master Input, Slave Output	
						LPDE	O	LPUART DE Signal Output	
						SDA1	I/O	I2C Data Input/Output	
						ADTRG	I	A/D Converter Trigger Input	
						SEG5	OA	LCD Segment Signal Output	
36	28	-	-	-	-	PB8*	IOUDS	PORT B Bit 8 Input/Output	
						MOSI0	I/O	SPI Master Output, Slave Input	
						SEG4	OA	LCD Segment Signal Output	
37	-	-	-	-	-	PB9*	IOUDS	PORT B Bit 9 Input/Output	
						T43OUTA	O	Timer 43 Pulse Output	
						T43INP	I	Timer 43 Capture/Force Input	
						SEG3	OA	LCD Segment Signal Output	

Table 3. Pin Description (continued)

Pin number						Pin name	Type	Description	Remark
LQFP-64	LQFP-48	LQFP-32	QFN-32	TSSOP-28	QFN-24				
38	-	-	-	-	-	PB10*	IOUDS	PORT B Bit 10 Input/Output	
						T43OUTB	O	Timer 43 Pulse Output	
						EC43	I	Timer 43 Event Count Input	
						SEG2	OA	LCD Segment Signal Output	
39	-	-	-	-	-	PB11*	IOUDS	PORT B Bit 11 Input/Output	
						T43INP	I	Timer 43 Capture/Force Input	
						SEG1	OA	LCD Segment Signal Output	
40	-	-	-	-	-	PB12*	IOUDS	PORT B Bit 12 Input/Output	
						T42INP	I	Timer 42 Capture/Force Input	
						SEG0	OA	LCD Segment Signal Output	
41	29	18	18	6	-	PC0*	IOUDS	PORT C Bit 0 Input/Output	
						CLKO	O	System Clock Output	
						SC0IN	I	Smartcard Detection Input	
						COM0	OA	LCD Common Signal Output	
42	30	19	19	7	15	PC1*	IOUDS	PORT C Bit 1 Input/Output	
						CLKO	O	System Clock Output	
						TXD0	O	UART Data Output	
						SC0PWR	O	Smartcard Power Control Output	
						COM1	OA	LCD Common Signal Output	
43	31	20	20	8	16	PC2*	IOUDS	PORT C Bit 2 Input/Output	
						RXD0	I	UART Data Input	
						SC0CLK	O	Smartcard Clock Output	
						COM2	OA	LCD Common Signal Output	
44	32	21	21	-	-	PC3*	IOUDS	PORT C Bit 3 Input/Output	
						MISO1	I/O	SPI Master Input, Slave Output	
						SC0RXD	I	SC0's UART Data Input	
						SC0RST	O	Smartcard Reset Output	
						CP0OUT	OA	Comparator 0 Output	
45	33	22	22	-	-	PC4*	IOUDS	PORT C Bit 4 Input/Output	
						MOSI1	I/O	SPI Master Output, Slave Input	
						SC0TXD	O	SC0's UART Data Output	
						SC0DATA	I/O	Smartcard Data Input/Output	
						CP1OUT	OA	Comparator 1 Output	
46	34	23	23	9	17	PC5	IOUDS	PORT C Bit 5 Input/Output	
						SWDIO*	I/O	SWD Data Input/Output	Pull-up
47	35	-	-	-	-	VSS	P	Ground	
48	36	-	-	-	-	VDD	P	VDD	
49	37	24	24	10	18	PC6	IOUDS	PORT C Bit 6 Input/Output	
						TXD10	O	UART Data Output	
						MOSI10	I/O	SPI Master Output, Slave Input	
						SC0TXD	O	SC0's UART Data Output	
						SC0DATA	I/O	Smartcard Data Input/Output	
						SWCLK*	I	SWD Clock Input	Pull-down

Table 3. Pin Description (continued)

Pin number						Pin name	Type	Description	Remark
LQFP-64	LQFP-48	LQFP-32	QFN-32	TSSOP-28	QFN-24				
50	38	25	25	11	-	PC7*	IOUDS	PORT C Bit 7 Input/Output	
						T40OUTA	O	Timer 40 Pulse Output	
						T40INP	I	Timer 40 Capture/Force Input	
						RXD10	I	UART Data Input	
						MISO10	I/O	SPI Master Input, Slave Output	
						SC0RXD	I	SC0's UART Data Input	
						SC0RST	O	Smartcard Reset Output	
						SS1	I	SPI Slave Select Input	
						SEG24	OA	LCD Segment Signal Output	
51	-	-	-	-	-	PC8*	IOUDS	PORT C Bit 8 Input/Output	
						SCK10	I/O	SPI Clock Input/Output	
						SC0CLK	O	Smartcard Clock Output	
						LPTXD	O	LPUART Data Output	
						COM4	OA	LCD Common Signal Output	
						SEG25	OA	LCD Segment Signal Output	
52	-	-	-	-	-	PC9*	IOUDS	PORT C Bit 9 Input/Output	
						SS10	I	SPI Slave Select Input	
						SC0PWR	O	Smartcard Power Control Output	
						LPRXD	I	LPUART Data Input	
						COM5	OA	LCD Common Signal Output	
						SEG26	OA	LCD Segment Signal Output	
53	-	-	-	-	-	PC10*	IOUDS	PORT C Bit 10 Input/Output	
						TXD1	O	UART Data Output	
						SC0IN	I	Smartcard Detection Input	
						COM6	OA	LCD Common Signal Output	
						SEG27	OA	LCD Segment Signal Output	
54	-	-	-	-	-	PC11*	IOUDS	PORT C Bit 11 Input/Output	
						RXD1	I	UART Data Input	
						LPDE	O	LPUART DE Signal Output	
						COM7	OA	LCD Common Signal Output	
						SEG28	OA	LCD Segment Signal Output	
55	39	26	26	12	-	PD0*	IOUDS	PORT D Bit 0 Input/Output	
						T40OUTB	O	Timer 40 Pulse Output	
						EC40	I	Timer 40 Event Count Input	
						SC1CLK	O	Smartcard Clock Output	
						SCK1	I/O	SPI Clock Input/Output	
						CP1N3	IA	Comparator 1 Negative Input	
						SEG29	OA	LCD Segment Signal Output	

Table 3. Pin Description (continued)

Pin number						Pin name	Type	Description	Remark
LQFP-64	LQFP-48	LQFP-32	QFN-32	TSSOP-28	QFN-24				
56	40	27	27	-	-	PD1*	IOUDS	PORT D Bit 1 Input/Output	5V tolerant I/O (The internal pull-up resistor must be disabled to use 5V I/O) VDD ≥ 2.0V when CP1P2, CP1P3, CP1P4, and CP1P5
						T43OUTA	O	Timer 43 Pulse Output	
						T43INP	I	Timer 43 Capture/Force Input	
						SC1RXD	I	SC1's UART Data Input	
						SC1RST	O	Smartcard Reset Output	
						MISO1	I/O	SPI Master Input, Slave Output	
						CP1P2	IA	Comparator 1 Positive Input	
						SEG30	OA	LCD Segment Signal Output	
57	41	28	28	-	-	PD2*	IOUDS	PORT D Bit 2 Input/Output	
						EC50	I	Timer 50 Event Count Input	
						T43OUTB	O	Timer 43 Pulse Output	
						EC43	I	Timer 43 Event Count Input	
						SC1TXD	O	SC1's UART Data Output	
						SC1DATA	I/O	Smartcard Data Input/Output	
						MOSI1	I/O	SPI Master Output, Slave Input	
						CP1P3	IA	Comparator 1 Positive Input	
						SEG31	OA	LCD Segment Signal Output	
58	42	29	29	13	19	PD3*	IOUDS	PORT D Bit 3 Input/Output	
						SCL0	I/O	I2C Clock Input/Output	
						TXD0	O	UART Data Output	
						SC1IN	I	Smartcard Detection Input	
						CP1P4	IA	Comparator 1 Positive Input	
						VLC0	IA/OA	LCD Bias Voltage Input/Output	
59	43	30	30	14	20	PD4*	IOUDS	PORT D Bit 4 Input/Output	
						T50INP	I	Timer 50 Capture/Clear Input	
						SDA0	I/O	I2C Data Input/Output	
						RXD0	I	UART Data Input	
						SC1PWR	O	Smartcard Power Control Output	
						CP1P5	IA	Comparator 1 Positive Input	
60	44	31	31	15	21	PD5	IOUDS	PORT D Bit 5 Input/Output	
						BOOT*	I	Boot Mode Selection Input	Pull-up
61	45	-	32	-	-	PD6*	IOUDS	PORT D Bit 6 Input/Output	
						SCL0	I/O	I2C Clock Input/Output	
						SEG32	OA	LCD Segment Signal Output	
62	46	-	-	-	-	PD7*	IOUDS	PORT D Bit 7 Input/Output	
						SS0	I	SPI Slave Select Input	
						SDA0	I/O	I2C Data Input/Output	
						COM3	OA	LCD Common Signal Output	
63	47	32	33	-	-	VSS	P	Ground	
64	48	-	-	-	-	VDD	P	VDD	

NOTES:

1. *Notation: I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
2. (*) Selected pin function after reset condition
3. Pin order may be changed with revision notice.

3 System and memory overview

Main system and memory of A31L12x series consist of the followings:

- ARM® Cortex® -M0+ core
- Five channels of DMA
- Internal SRAM
- Internal Flash memory
- AHB (Advanced High Performance Bus) and APB (Advanced Peripheral Bus)

3.1 Cortex®-M0+ core

The Cortex-M0+ processor is the most energy-efficient ARM processor available. It builds on the very successful Cortex-M0+ processor, retaining full instruction set and tool compatibility, while further reducing energy consumption and increasing performance. Technical reference manual “DDI 0484C” from ARM provides detail information of Cortex-M0+.

3.2 Interrupt controller

The Cortex-M0+ process has embedded an interrupt controller named NVIC (Nested Vector Interrupt Controller). A31L12x has additional interrupt control block for controlling 32 interrupt sources generated by internal peripherals.

To use interrupts from internal peripherals, both the NVIC and the interrupt control block must be configured properly. This document describes only the peripheral interrupt controller. For more information about NVIC inside the Cortex-M0+ processor, please refer to the technical reference manual “ARM DDI 0484C” in ARM technical document site.

Table 4. Interrupt Vector Map

Priority	Vector Address	Interrupt Source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Exception
-13	0x0000_000C	Hard Fault Exception

Table 4. Interrupt Vector Map (continued)

Priority	Vector Address	Interrupt Source
-12	0x0000_0010	Reserved
-11	0x0000_0014	
-10	0x0000_0018	
-9	0x0000_001C	
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	SVCall Exception
-4	0x0000_0030	Reserved
-3	0x0000_0034	
-2	0x0000_0038	PenSV Exception
-1	0x0000_003C	SysTick Exception
0	0x0000_0040	LVI Interrupt
1	0x0000_0044	WUT Interrupt
2	0x0000_0048	WDT Interrupt
3	0x0000_004C	EINT0 Interrupt
4	0x0000_0050	EINT1 Interrupt
5	0x0000_0054	EINT2 Interrupt
6	0x0000_0058	EINT3 Interrupt
7	0x0000_005C	TIMER40 Interrupt
8	0x0000_0060	TIMER41 Interrupt
9	0x0000_0064	TIMER42 Interrupt
10	0x0000_0068	I2C0 Interrupt
11	0x0000_006C	USART10 Interrupt
12	0x0000_0070	SPI0 Interrupt
13	0x0000_0074	SPI1 Interrupt
14	0x0000_0078	I2C1 Interrupt

Table 4. Interrupt Vector Map (continued)

Priority	Vector Address	Interrupt Source
15	0x0000_007C	TIMER50 Interrupt
16	0x0000_0080	SC0 Interrupt
17	0x0000_0084	SC1 Interrupt
18	0x0000_0088	ADC Interrupt
19	0x0000_008C	UART0 Interrupt
20	0x0000_0090	UART1 Interrupt
21	0x0000_0094	TIMER43 Interrupt
22	0x0000_0098	CMP 0/1 Interrupt
23	0x0000_009C	DMACH0 Interrupt
24	0x0000_00A0	DMACH1 Interrupt
25	0x0000_00A4	LPUART Interrupt
26	0x0000_00A8	Reserved
27	0x0000_00AC	
28	0x0000_00B0	RTCC Interrupt
29	0x0000_00B4	DMACH2 Interrupt
30	0x0000_00B8	DMACH3 Interrupt
31	0x0000_00BC	DMACH4 Interrupt

3.3 Boot mode

Boot mode pins

A31L12x series has a Boot mode to program the internal flash memory. The Boot mode will be activated by setting a BOOT pin to “Low” level at reset timing (Normal operation mode is “High” level).

The Boot mode supports either UART boot or SPI boot. For the UART boot, TXD10/RXD10 ports are used. For the SPI boot, MOSI10/MISO10/SCK10/SS10 ports are used.

Table 5 introduces pins used in the Boot mode.

Table 5. Boot Mode Pin List

Block	Pin Name	Direction	Description
SYSTEM	nRESET	I	Reset Input signal
	BOOT/PD5	I	'0' to enter Boot mode
UART mode of USART10	RXD10/PA3	I	UART Boot Receive Data
	TXD10/PA2	O	UART Boot Transmit Data
SPI mode of USART10	SS10/PA1	I	SPI Boot Slave Input
	SCK10/PA4	I	SPI Boot Clock Input
	MISO10/PA3	I	SPI Boot Data Input with function exchange
	MOSI10/PA2	O	SPI Boot Data Output with function exchange

Boot mode connection

A user can design target boards using any of Boot mode ports – UART or SPI mode of USART10. Examples of connection diagrams in the Boot mode are introduced in figures 6 and 7.

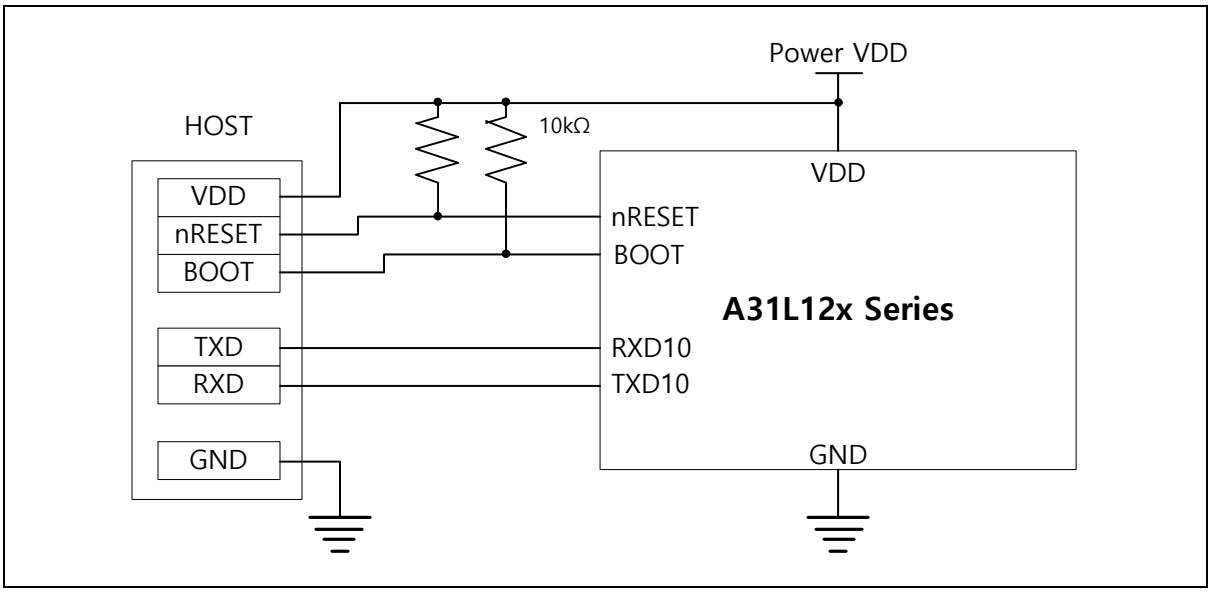


Figure 8. Connection Diagram of UART Boot

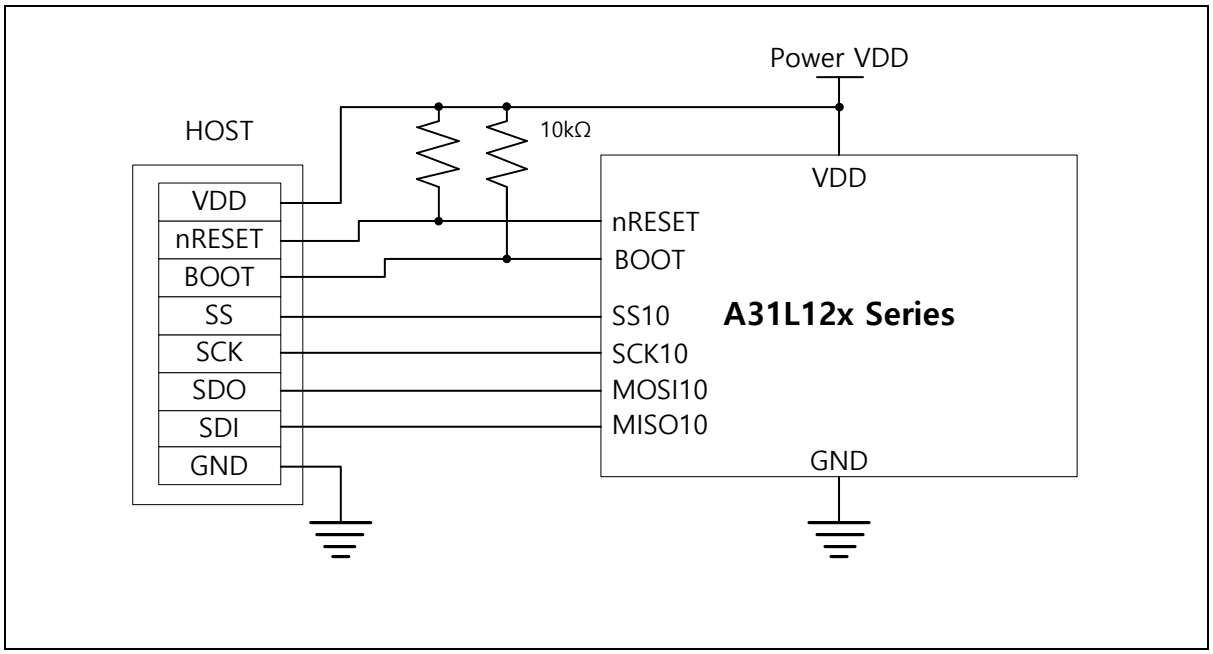


Figure 9. Connection Diagram of SPI Boot

3.4 SWD debug mode and E-PGM+ connection

Connections for SWD debugger interface or E-PGM+ is described in figure 8.

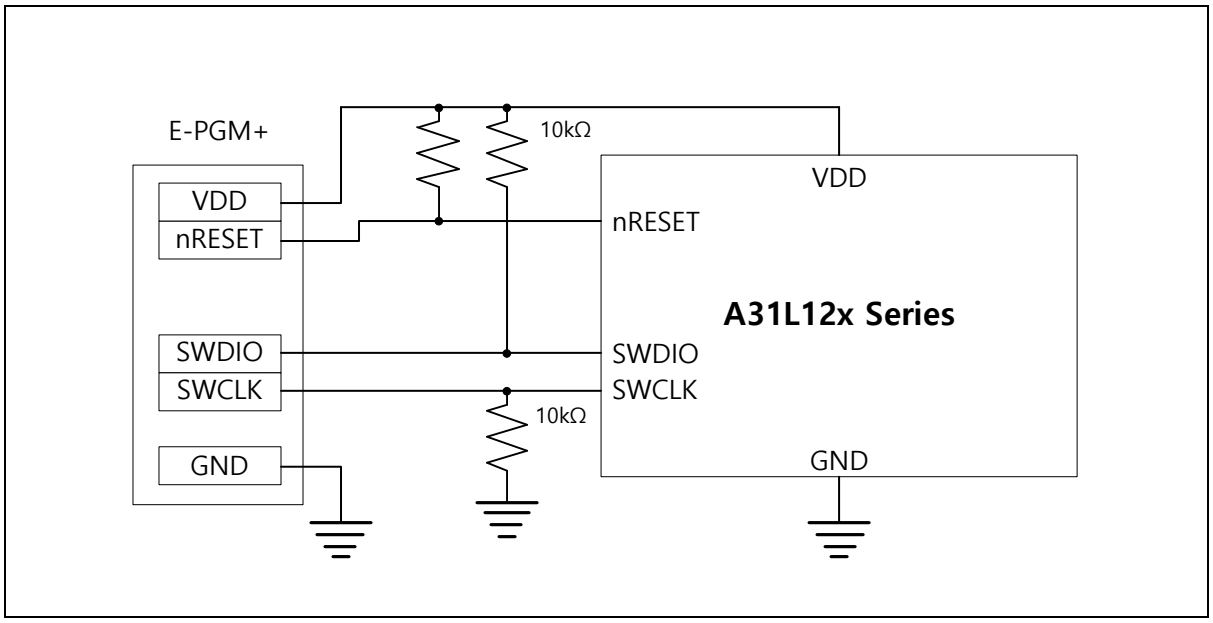


Figure 10. Connection between A31L12x Series and E-PGM+ using SWD Debugger Interface

3.5 Memory organization

3.5.1 Memory map

Figure 9 shows addressable memory space in memory map.

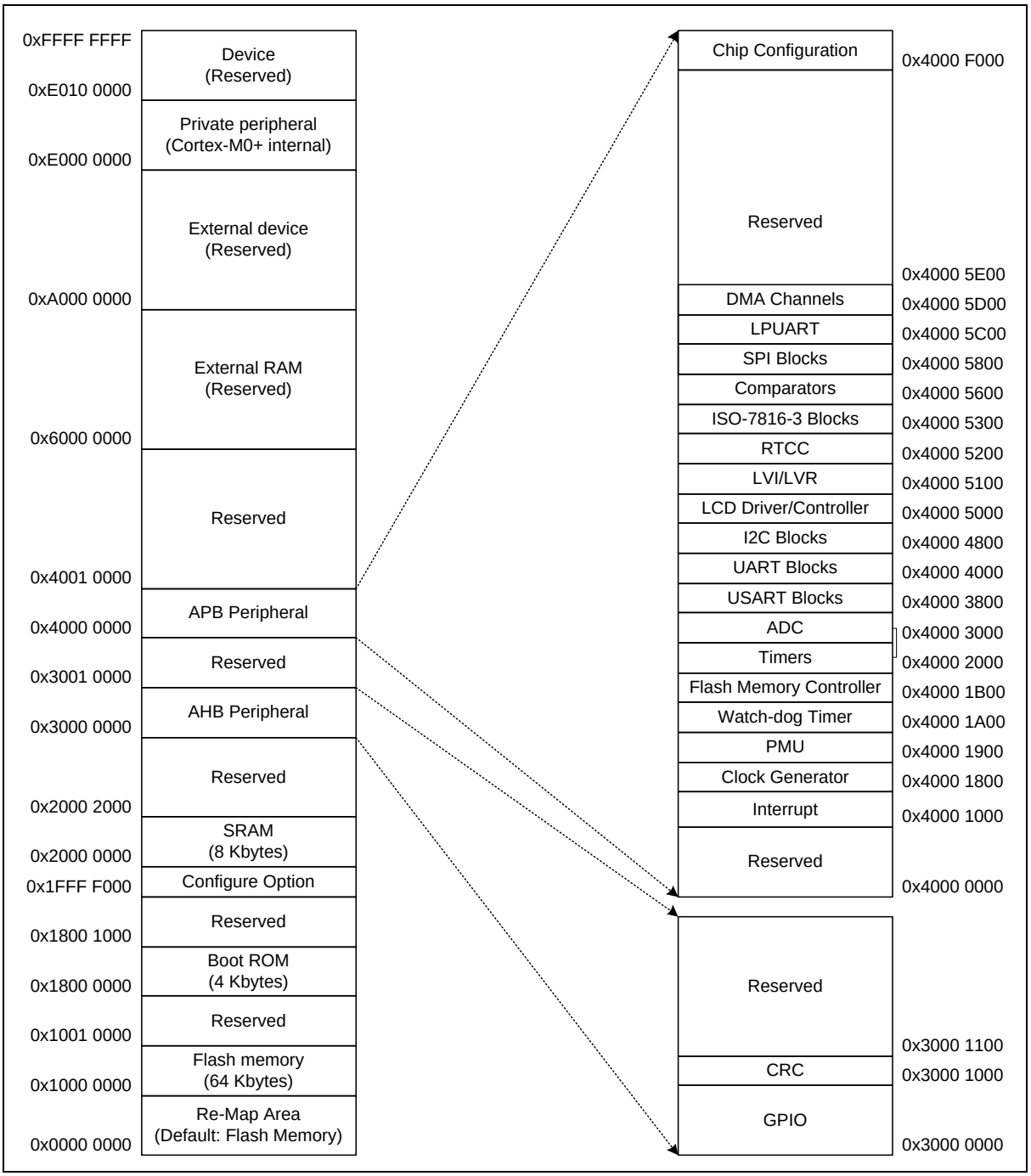


Figure 11. Main Memory Map

3.5.2 Internal SRAM

A31L12x series has a block of 0-wait on-chip SRAM. Its size is 8KB, and its base address is 0x2000_0000. The SRAM's memory area is mainly for data memory and stack memory. It is possible to locate code area in the SRAM memory for fast operation or for flash erase or program operation for self-program.

This device does not support memory remapping. So jump and return is required to process the code in SRAM memory area.

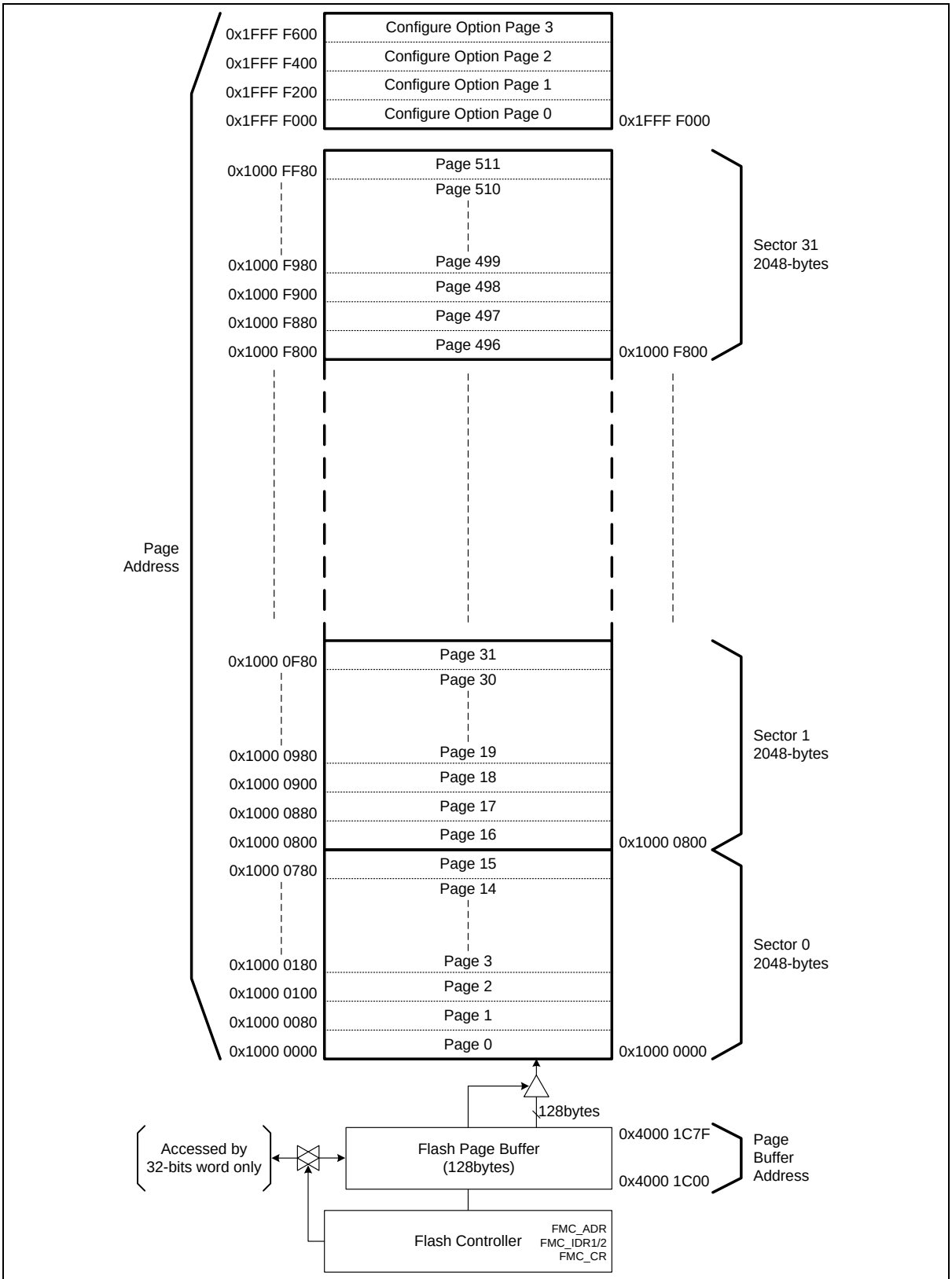
3.5.3 Flash memory

A31L12x series has an internal flash memory as shown in the followings:

- 64 or 32KB Flash code memory
- 32-bit read data bus width
- 128-byte page size
- Page erase and bulk erase available
- 128-byte unit program

Table 6. Internal Flash Memory Specification

Item	Description
Size	64KB
Start address	0x1000_0000
End address	0x1000_FFFF
Page size	128-byte
Total page count	512 pages
PGM unit	128-byte
Erase unit	128-byte or bulk



NOTES:

1. If any instruction other than 32-bit is used to write data to the buffer, wrong data will be written.
2. Each configure option page0/1/2/3 has 128bytes respectively.

Figure 12. Internal Flash Memory Block Diagram

3.5.4 Configure option area

Configuration option area of A31L12x series is used for system related trimming values, user option, and user data. The configure option area consists of four pages in the flash memory, which can be erased and written by the flash memory controller. This area can be read by any instruction.

The four pages of the configuration option area are listed in the followings:

- Page 0: System related trimming values and 128-bit unique device ID registers
- Page 1: User option for read protection, watchdog timer, and LVR voltage level configurations
- Page 2: User data 0 area
- Page 3: User data 1 area

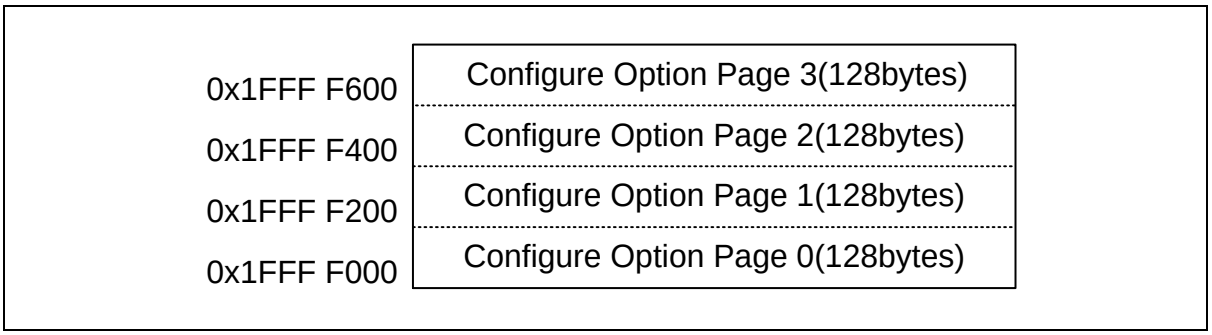


Figure 13. Configure Option Area Structure

Configuration option page

Base address of the configuration option area ranges from 0x1FFF_F000 to 0x1FFF_F600. The area map is shown in Table 7.

Table 7. Configuration Option Area Map

Page	NAME	ADDRESS	DESCRIPTION
0	**-**	0x1FFF_F000 to 0x1FFF_F04F 0x1FFF_F060 to 0x1FFF_F07F	System Trimming Values
	CONF_MF1CNFIG	0x1FFF_F050	Manufacture Information 1 for 128-bit unique ID
	CONF_MF2CNFIG	0x1FFF_F054	Manufacture Information 2 for 128-bit unique ID
	CONF_MF3CNFIG	0x1FFF_F058	Manufacture Information 3 for 128-bit unique ID
	CONF_MF4CNFIG	0x1FFF_F05C	Manufacture Information 4 for 128-bit unique ID
1	**CONF_RPCNFIG**	0x1FFF_F200	Configuration for Read Protection
	CONF_WDTCNFIG	0x1FFF_F20C	Configuration for Watch-Dog Timer
	CONF_LVRCNFIG	0x1FFF_F210	Configuration for Low Voltage Reset
	CONF_CNFIGWTP1	0x1FFF_F214	Erase/Write Protection for Configure Option Page 1/2/3
	CONF_FMWTP1	0x1FFF_F240	Erase/Write Protection for Flash Memory
2	**-**	0x1FFF_F400 to 0x1FFF_F47F	User Data Area 0
3	**-**	0x1FFF_F600 to 0x1FFF_F67F	User Data Area 1

4 SCU (System Control Unit)

A31L12x series has a built-in intelligent power control block, which manages analog blocks and operating modes. Internal reset and clock signals are controlled by SCU block to maintain optimized system performance and power dissipation.

4.1 SCU block diagram

Figure 14 shows the SCU block diagram.

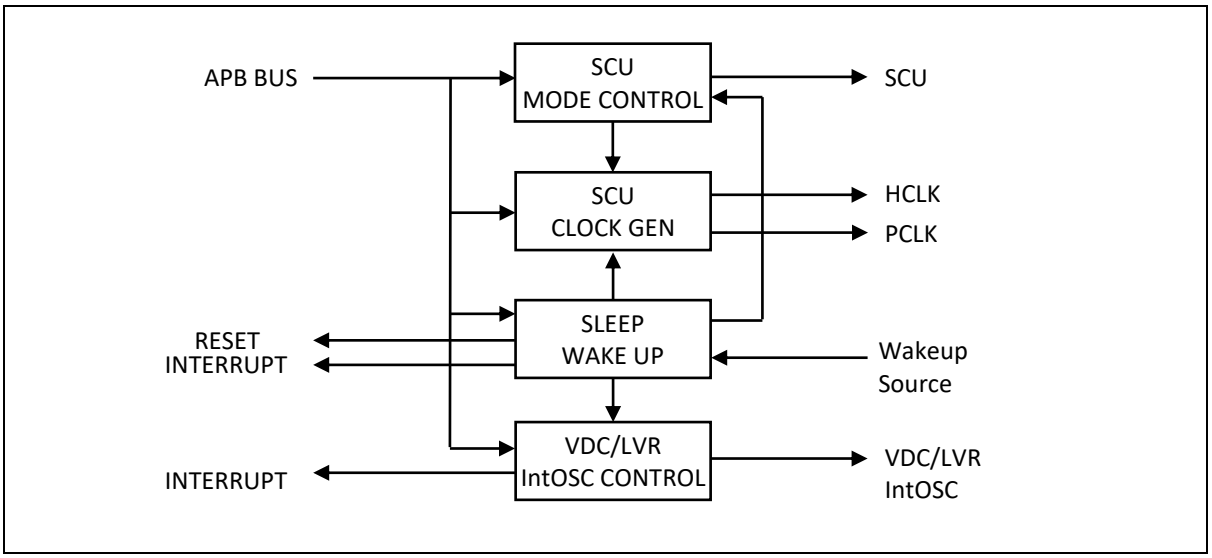


Figure 14. SCU Block Diagram

4.2 Clock system

A31L12x series has two main operating clocks. One is HCLK, which supplies the clock to the CPU and AHB bus system. The other one is PCLK, which supplies the clock to the peripheral systems.

Users can control the clock system variation by software. Figure 15 shows the clock system of A31L12x series and Table 8 shows the descriptions for clock sources.

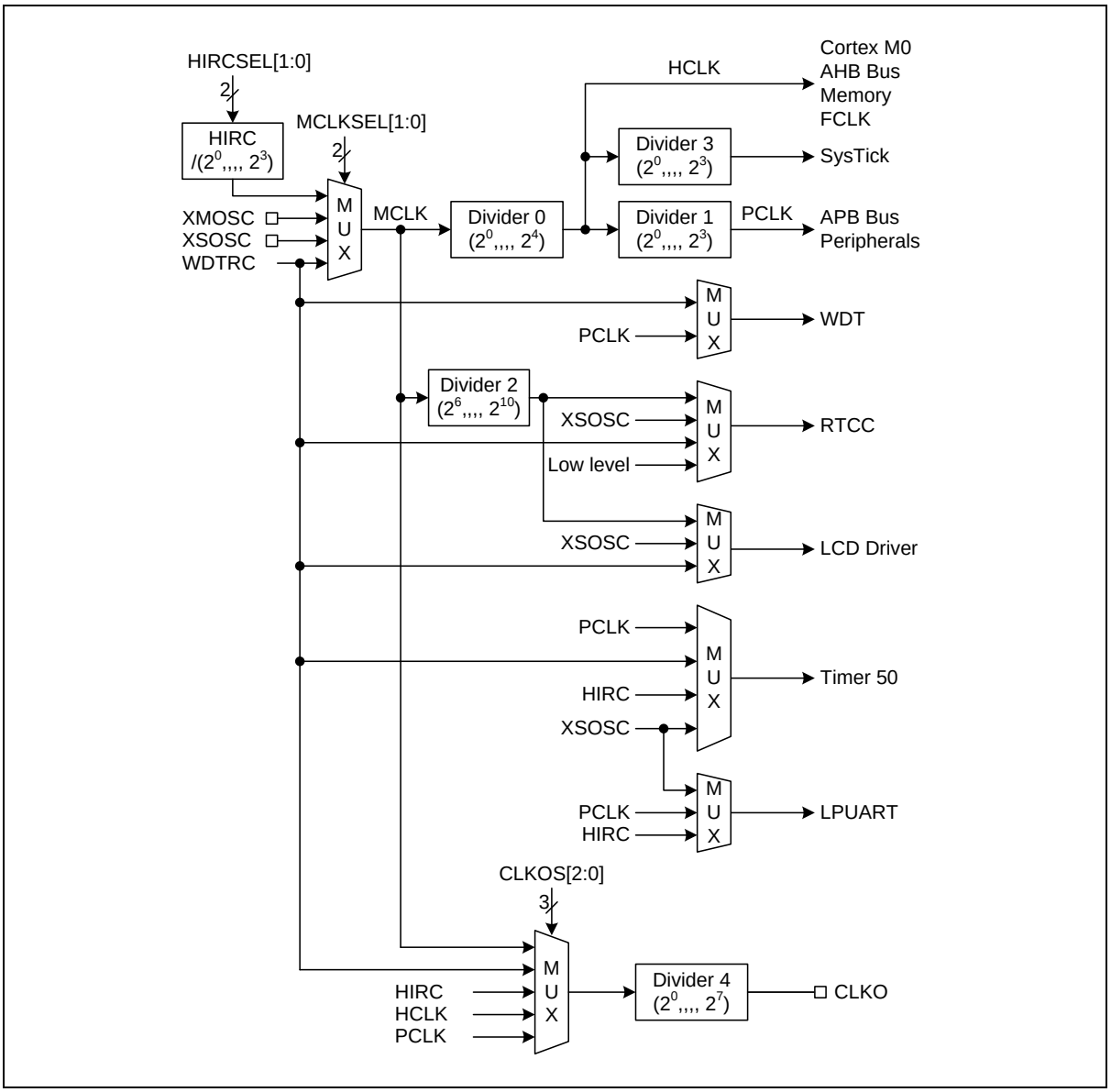


Figure 15. Clock Source Configuration

Each mux to switch clock source has a glitch-free circuit. So a clock can be switched without glitch risks. When you change the clock mux control, be sure both clock sources are alive. If either is not alive, clock change operation stops and system will shut down and not recover.

Table 8. Clock Sources

Clock name	Mnemonic	Frequency	Description
Main OSC	XMOSC	• X-TAL (2MHz to 16MHz) • External Clock (2MHz to 32MHz)	• External Main Crystal OSC • External Main Clock
Sub OSC	XSOSC	X-TAL (32.768kHz)	External Sub Crystal OSC
Internal RC OSC	HIRC	2MHz to 32MHz	High Frequency Internal RC OSC
WDT RC OSC	WDTRC	40kHz	Watchdog Timer RC OSC

4.2.1 HCLK clock domain

HCLK clock feeds the clock to the CPU and AHB bus. Cortex-M0+ CPU requires 2 clocks, FCLK and HCLK. FCLK is a free running clock and is always running except during power down mode. HCLK can be stopped during sleep mode.

The HCLK clock operates the BUS system and memory systems. Max BUS operating clock speed is 32MHz. HCLK frequency should be limited to a frequency of 32MHz or lower.

4.2.2 Miscellaneous clock domain

Various clock sources are required for each functional block. The SCU provides clock source selectivity with dedicated pre-scaler for each functional block. The clock selection mux does not support glitch-free function, so the clock is unpredictable during clock selection. Figure 14 shows the configurations for miscellaneous clocks.

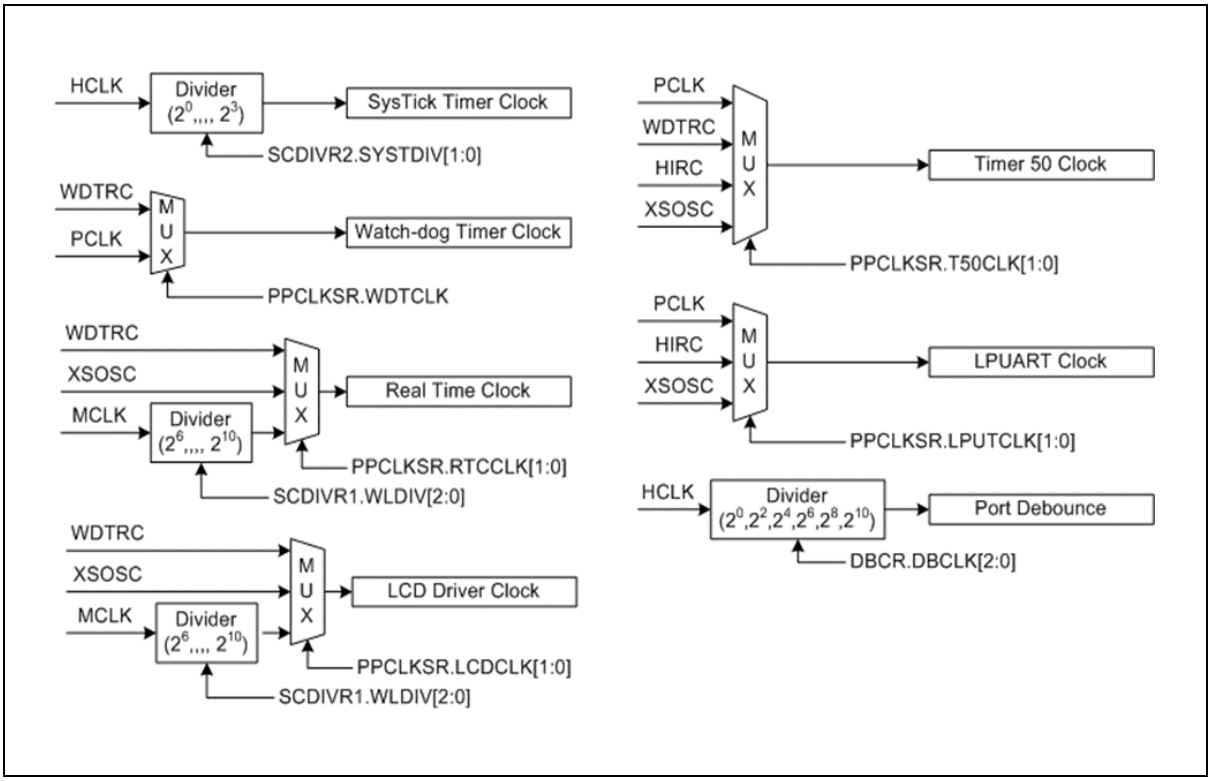


Figure 16. Miscellaneous Clock Configuration

4.2.3 PCLK clock domain

PCLK is the master clock for all the peripherals except for the CRC generator and ports. It can shut down during power down mode. Each peripheral clock is generated by SCU_PPCLKEN1 and SCU_PPCLKEN2 register set. Figure 13 illustrates the PCLK clock distributions. The peripherals are

not accessible even by reading its registers until each PCLK clock of each block is enabled.

4.2.4 Clock configuration procedure

After power on the device, a default system clock is generated by HIRC (2MHz) clock. The HIRC is enabled by default during power up sequence. Other clock sources are enabled by user controls and configuration options with a system clock.

XMOSC and XSOSC clocks are enabled by XMOSCEN and XSOSCEN bits of SCU_CLKSRCR register respectively. Before enabling XMOSC and XSOSC blocks, the pin mux configuration should be set for XIN/XOUT and SXIN/SXOUT functions. PE2/PE3 and PE0/PE1 pins are shared by XMOSC's XIN/XOUT function and XSOSC's SXIN/SXOUT function – PE_MOD and PE_AFSR1 registers should be configured properly.

After enabling the XMOSC and XSOSC blocks, a user can check stability of crystal oscillation through a clock monitoring control register, SCU_CMONCR. It takes more than 1ms to ensure stable crystal oscillation before changing the system clock.

Figure 17 shows an example flow chart to configure the system clock to XMOSC and XSOSC clock.

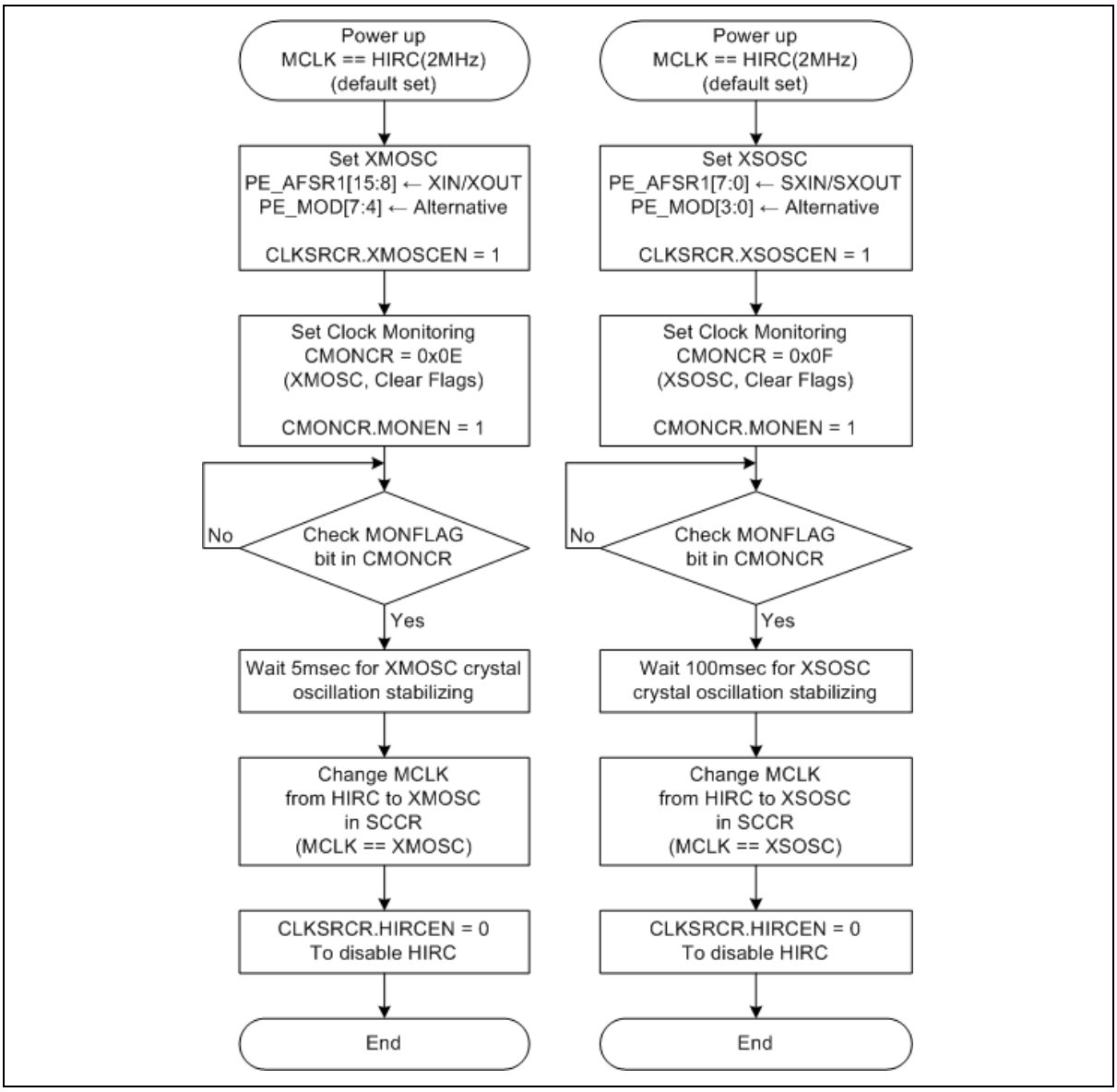


Figure 17. Clock Configuration Procedure

4.3 Reset

A31L12x series has two system resets. One is the cold reset by POR, which is effective during power up or down sequence. The other is the warm reset, generated by several reset sources. The reset event makes the device to turn back to its initial state.

The cold reset has only one reset source, which is POR, while the warm reset has several reset sources as shown below:

- nRESET pin
- WDT reset
- LVR reset
- MON reset
- S/W reset
- CPU request reset

4.3.1 Cold reset

The cold reset is one of important feature of the A31L12x series when it powers up. This characteristic will globally affect the system boot.

Internal VDC is enabled when VDD power is turned on. Internal VDD level slope follows the External VDD power slope. Internal POR trigger level is at 1.1V of the internal VDC voltage. At this time, boot operation begins.

Internal RC clock turns on and counts 4ms for internal VDC level to stabilize. At this time, external VDD voltage level should be bigger than initial LVR level (1.50V). After 4ms of counting, the CPU reset is released and operation begins.

Figure 18 shows waveform of power up sequence and internal reset.

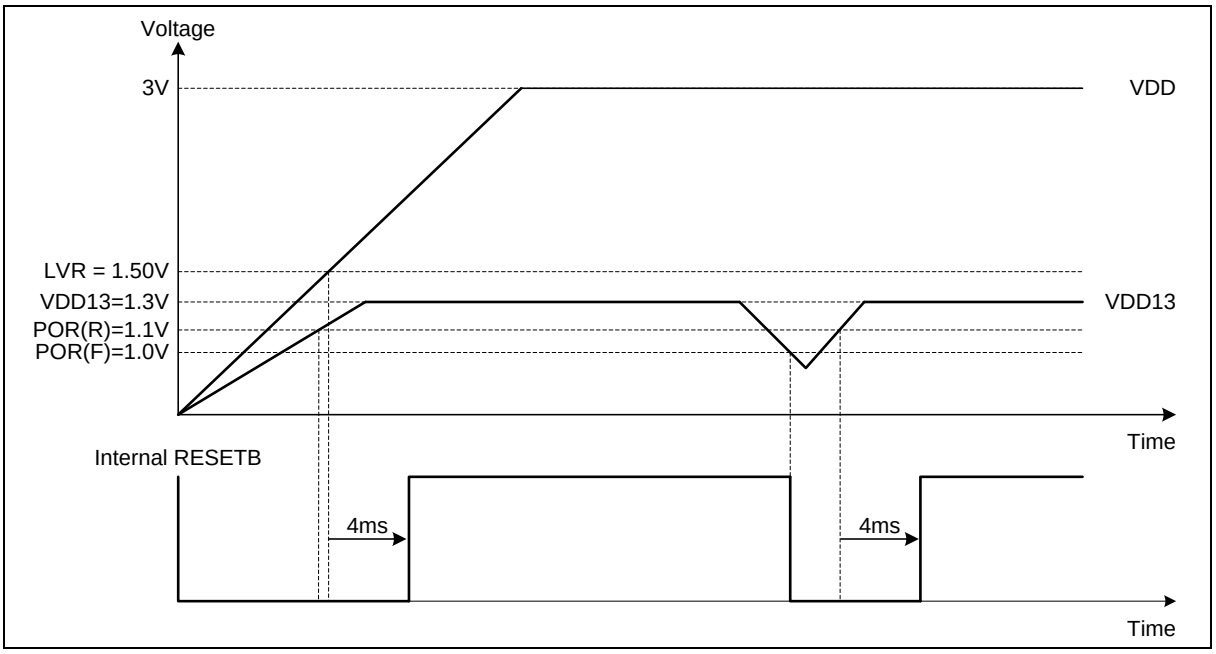


Figure 18. Power-up POR Sequence

A register SCU_RSTSSR shows the POR reset status. The last reset comes from the POR. SCU_RSTSSR.PORSTA is set to '1'. After power on, this bit is always '1' if the bit is not cleared by S/W. If abnormal internal voltage drop is detected during normal operation, the system will be reset and this bit also will be set to '1'.

When the cold reset is applied, the entire device returns to its initial state.

4.3.2 Warm reset

The warm reset event has several reset sources and some parts of the device return to their initial states when the warm reset takes place.

The warm reset status appears in a register SCU_RSTSSR. A reset for each peripheral block is controlled by a register SCU_PPRST. The reset can be masked independently.

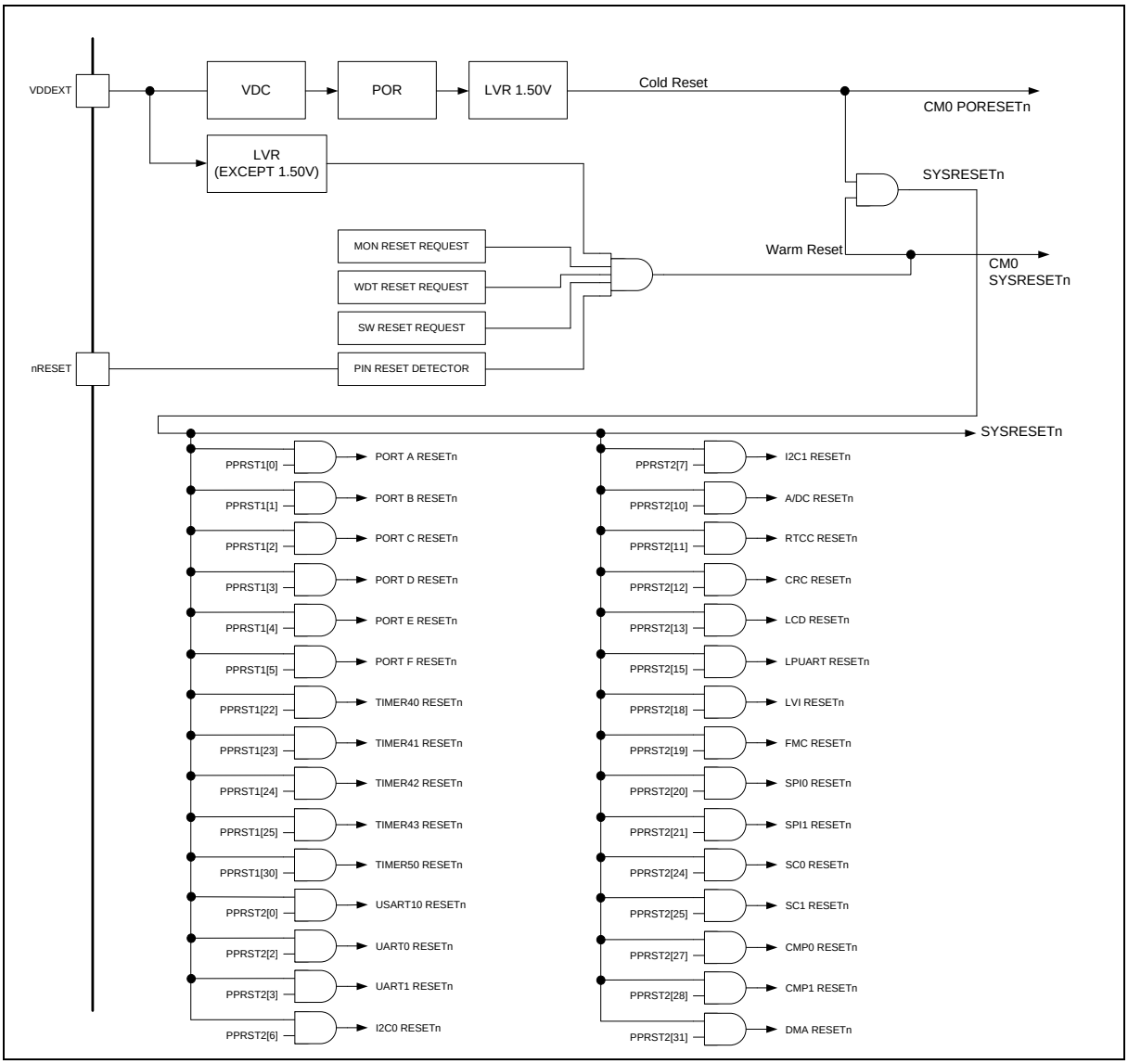


Figure 19. Reset Configuration

4.3.3 LVR reset

The LVR voltage level is set by a low voltage reset configuration register (CONF_LVRCNFIG) in the configuration option page 1.

LVR reset status appears in a register SCU_RSTSSR. The reset for LVR is controlled by a register SCU_LVRCR. The register is cleared to “0x00” on POR reset.

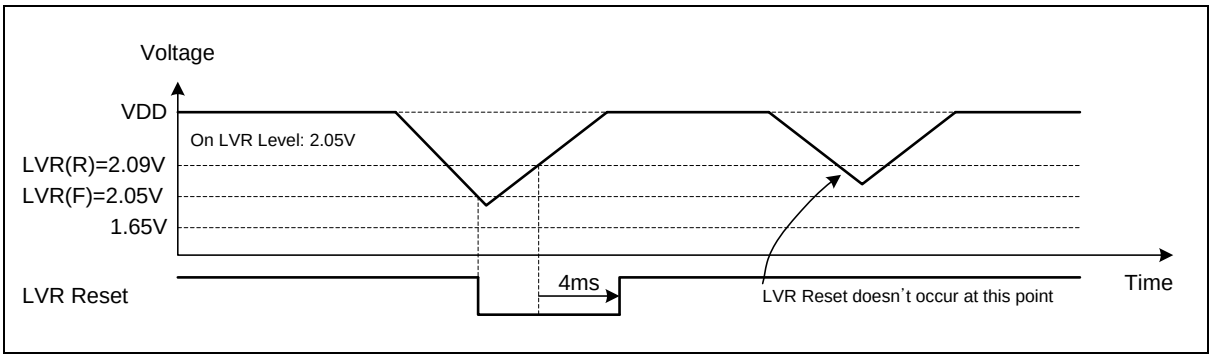


Figure 20. LVR Reset Timing Diagram

4.4 Operation mode

INIT mode is the initial state of the device when reset. At RUN mode, the chip runs at its max CPU performance with a high-speed clock system. At SLEEP and DEEP SLEEP mode, the chip runs at a low power consumption mode. The system saves power by halting the processor core and unused peripherals.

Figure 21 shows the operation mode transition diagram.

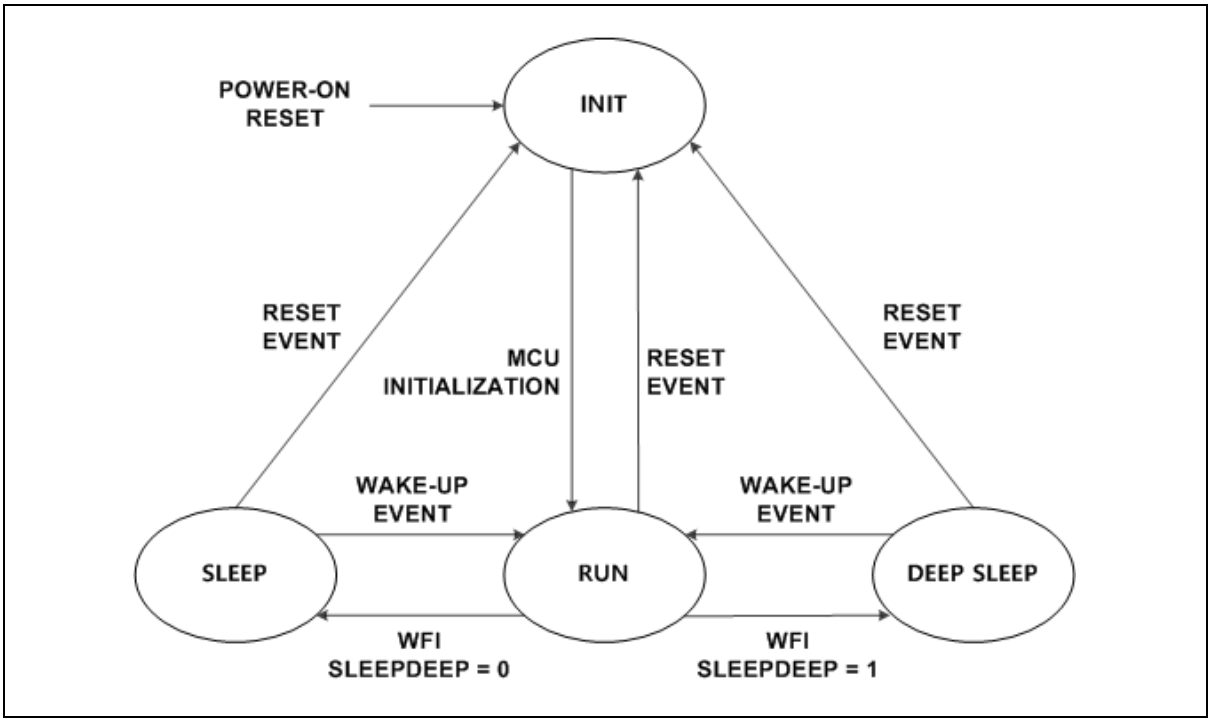


Figure 21. Operating Mode

4.4.1 Run mode

This mode is to operate CPU core and peripheral hardware with a high-speed clock. The device enters in the INIT state after reset, and then enters in the RUN mode.

4.4.2 Sleep mode

The device stops only CPU in this mode. Each peripheral function turns on by a function enable bit and a clock enable bit of the register SCU_PPCLKEN.

4.4.3 Deep sleep mode

The device stops not only CPU but also a selected system clock (MCLK) in this mode. RTCC with sub clock and watchdog timer with WDTRC still operate in this mode.

4.5 Pins for SCU

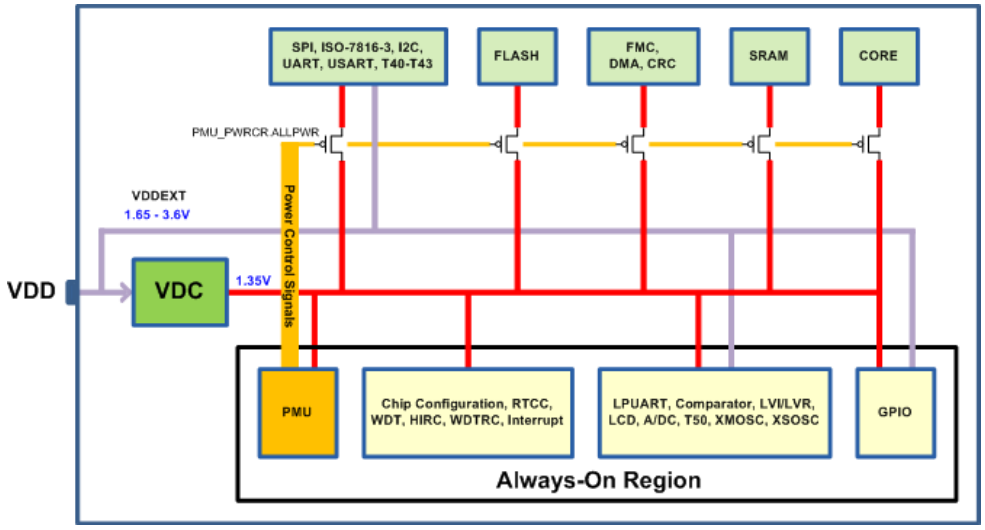
Table 9. Pins and External Signals for SCU

PIN NAME	TYPE	DESCRIPTION
nRESET	I	External Reset Input
XIN/XOUT	OSC	External Crystal Oscillator for Main Clock
SXIN/SXOUT	OSC	External Crystal Oscillator for Sub Clock
CLKO	O	Clock Output Monitoring Signal

5 PMU

A31L12x series has a built-in PMU (Power Management Unit), which manages the internal power supply of system control and peripheral parts and a wake-up time from sleep and deep sleep modes. This PMU has 32-bytes backup registers to retain data during deep sleep mode with power shut-off of system and peripherals except always-on region.

5.1 PMU block diagram



NOTE: The 6 “NOP Instruction” should follow immediately after WFI or WFE Instruction’.

Figure 22. PMU Block Diagram

6 PCU and GPIO

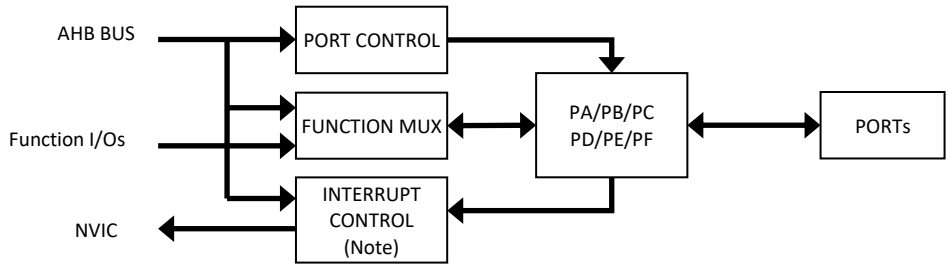
PCU (Port Control Unit) configures and controls external I/Os as shown below:

- It configures direction of an external signal of each pin.
- It sets Interrupt trigger mode for each pin.
- The PCU sets internal pull-up/down register control and open drain control.

Most pins, except for dedicated function pins, can be used as GPIO (General Purpose I/O) ports. GPIO block controls the GPIO as shown below:

- Output signal level (H/L) select
- External interrupt interface
- Pull-up/down enable or disable

6.1 PCU and GPIO block diagrams



NOTE: Refer to the Chapter 3.2 Interrupt Controller.

Figure 23. PCU Block Diagram

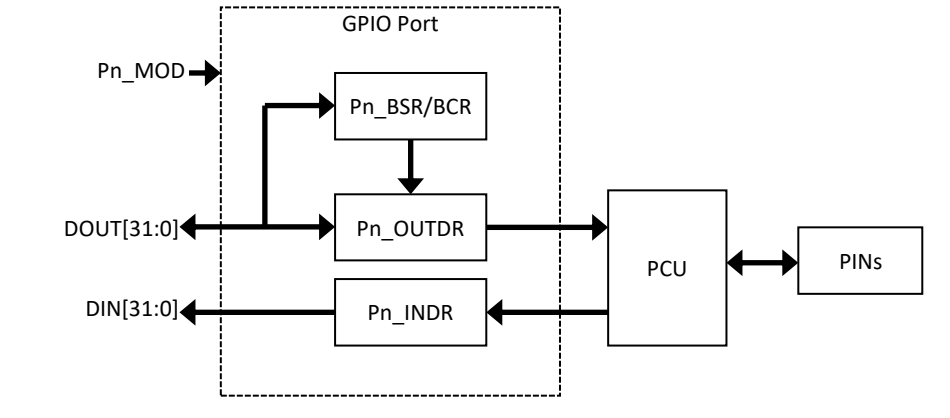


Figure 24. GPIO Block Diagram

6.2 I/O port block diagram

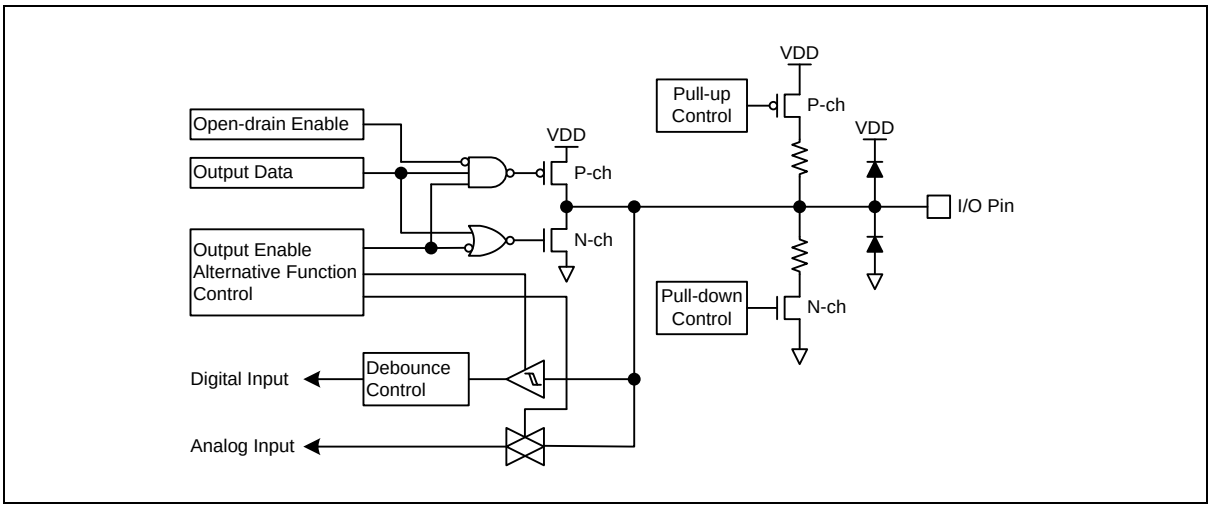


Figure 25. I/O Port Block Diagram (General Purpose I/O Pins)

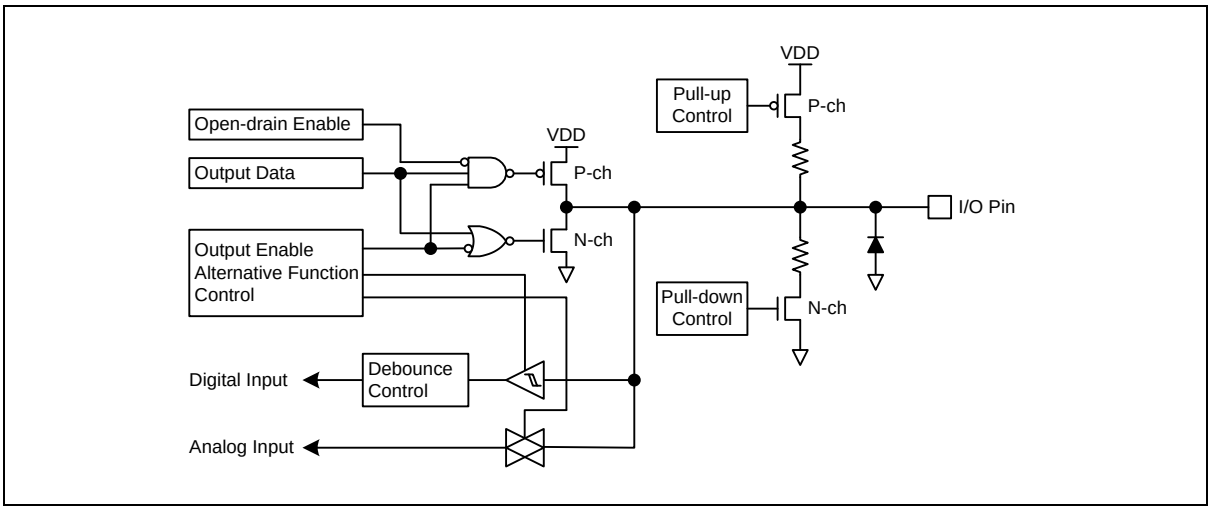


Figure 26. I/O Port Block Diagram (5V Tolerant I/O pins)

6.3 Pin multiplexing

GPIO pins support alternative functions. Table 10 shows pin multiplexing information.

Table 10. GPIO Alternative Functions

PORT	PIN	FUNCTION							
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA	0	T40OUTA	T40INP	–	–	AN0	CP0N0	CP0OUT	–
	1	T40OUTB	EC40	T42INP	SS10	AN1	CP0P0	–	SEG19
	2	T41OUTA	T41INP	TXD10	MOSI10	AN2	CP1N0	CP1OUT	SEG18
	3	T41OUTB	EC41	RXD10	MISO10	AN3	CP1P0	ADTRG	SEG17
	4	–	T43INP	SS1	SCK10	AN4	CP0N1	CP1N1	–
	5	T40OUTA	T40INP	–	SCK1	AN5	CP0N2	CP1N2	–
	6	T43OUTA	T43INP	–	MISO1	AN6	–	CP0OUT	SEG16
	7	T43OUTB	EC43	–	MOSI1	AN7	CP1P1	CP1OUT	SEG15
	8	–	–	LPTXD	–	AN8	–	–	SEG14
	9	–	–	LPRXD	–	AN9	–	–	SEG13
PB	0	–	–	TXD1	–	AN10	–	–	SEG12
	1	–	–	RXD1	–	AN11	LPDE	–	SEG11
	2	T50OUT	–	–	–	–	–	–	SEG10
	3	T41OUTA	T41INP	LPTXD	SCK0	SCL1	–	ADTRG	SEG9
	4	T41OUTB	EC41	LPRXD	–	SDA1	–	ADTRG	SEG8
	5	–	–	–	SS0	–	LPDE	–	SEG7
	6	T42OUTA	T42INP	–	SCK0	SCL1	–	–	SEG6
	7	T42OUTB	EC42	RTCOUT	MISO0	SDA1	LPDE	ADTRG	SEG5
	8	–	–	–	MOSI0	–	–	–	SEG4
	9	T43OUTA	T43INP	–	–	–	–	–	SEG3
	10	T43OUTB	EC43	–	–	–	–	–	SEG2
	11	T43INP	–	–	–	–	–	–	SEG1
	12	T42INP	–	–	–	–	–	–	SEG0

Table 10. GPIO Alternative Functions (continued)

PORT	PIN	FUNCTION							
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC	0	CLKO	–	–	–	SC0IN	–	–	COM0
	1	CLKO	–	TXD0	–	SC0PWR	–	–	COM1
	2	–	–	RXD0	–	SC0CLK	–	–	COM2
	3	–	–	–	MISO1	SC0RST	SC0RXD	CP0OUT	–
	4	–	–	–	MOSI1	SC0DATA	SC0TXD	CP1OUT	–
	5	SWDIO	–	–	–	–	–	–	–
	6	SWCLK	–	TXD10	MOSI10	SC0DATA	SC0TXD	–	–
	7	T40OUTA	T40INP	RXD10	MISO10	SC0RST	SC0RXD	SS1	SEG24
	8	–	–	LPTXD	SCK10	SC0CLK	–	–	COM4/ SEG25
	9	–	–	LPRXD	SS10	SC0PWR	–	–	COM5/ SEG26
	10	–	–	TXD1	–	SC0IN	–	–	COM6/ SEG27
	11	–	–	RXD1	–	–	LPDE	–	COM7/ SEG28
PD	0	T40OUTB	EC40	–	SCK1	SC1CLK	CP1N3	–	SEG29
	1	T43OUTA	T43INP	–	MISO1	SC1RST	SC1RXD	CP1P2	SEG30
	2	T43OUTB	EC43	EC50	MOSI1	SC1DATA	SC1TXD	CP1P3	SEG31
	3	–	–	TXD0	–	SC1IN	SCL0	CP1P4	VLC0
	4	–	T50INP	RXD0	–	SC1PWR	SDA0	CP1P5	–
	5	BOOT	–	–	–	–	–	–	–
	6	–	–	–	–	SCL0	–	–	SEG32
	7	–	–	–	SS0	SDA0	–	–	COM3
PE	0	SXIN	–	–	–	–	–	–	–
	1	SXOUT	–	–	–	–	–	–	–
	2	XIN	–	–	–	–	–	–	–
	3	XOUT	–	–	–	–	–	–	–
	4	RTCOUT	–	–	–	–	–	–	–

Table 10. GPIO Alternative Functions (continued)

PORT	PIN	FUNCTION							
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF	0	–	EC50	–		AN12	–	–	SEG23
	1	T50OUT	–	–	–	AN13	–	–	SEG22
	2	–	T50INP	–	MISO0	AN14	–	–	SEG21
	3	–	–	–	MOSI0	AN15	–	–	SEG20

NOTES:

1. The PC8 – PC11 are automatically configured as common or segment signal according to the duty of the LCD control register when the pins are selected as alternative functions for common/segment.
2. The SWCLK and SWDIO pins shouldn't be changed as other alternative functions by software during the pins are connected with debugger host.
3. The VDD should be greater than or equal to 2.0V if CP1P2, CP1P3, CP1P4, and CP1P5 are used as comparator pins for alternative function.

7 WDT

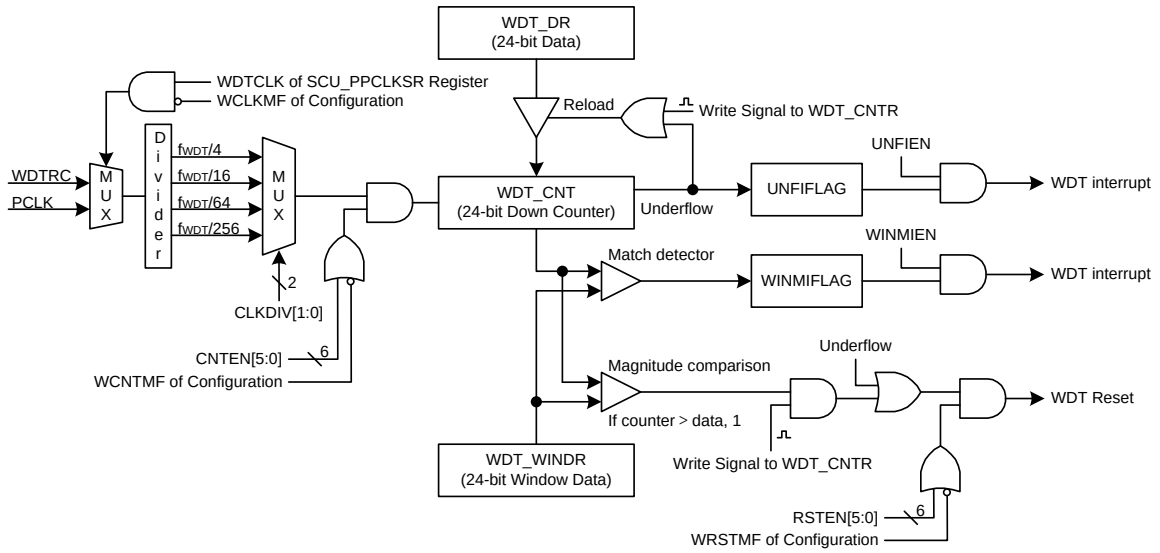
WDT (Watchdog Timer) rapidly detects CPU malfunctions such as endless loops caused by noise and recovers the CPU to the normal state. WDT signal for malfunction detection can be used as either a CPU reset or an interrupt request.

When the WDT is not being used for malfunction detection, it can be used as a timer to generate interrupts at fixed intervals. When WDT_CNT value reaches WDT_WINDR value, a watchdog interrupt can be generated. The underflow time of the WDT can be set by WDT_DR. If an underflow occurs, an internal reset may be generated. The WDT operates at 40KHz which is the embedded RC oscillator's clock.

The WDT operations are listed in the followings:

- 24-bit down counter (WDT_CNT)
- Select reset or periodic interrupt
- Count clock selection
- Watchdog overflow output signal
- Includes Counter Window function

7.1 WDT block diagram



NOTE: When a reload signal is generated, the WDT_DR value is reloaded to WDT_CNT register, after 1-clock delay, with the clock selected by the CLKDIV bits.

Figure 27. WDT Block Diagram

8 RTCC

RTCC (Real Timer Clock and Calendar) has a function for RTC (Real Time Clock) and calendar operations. Internal structure of the RTCC is implemented with the clock source select circuit, second/minute/hour/day/week/month/year counter circuits, alarm circuit, output select circuit, and error correction circuit.

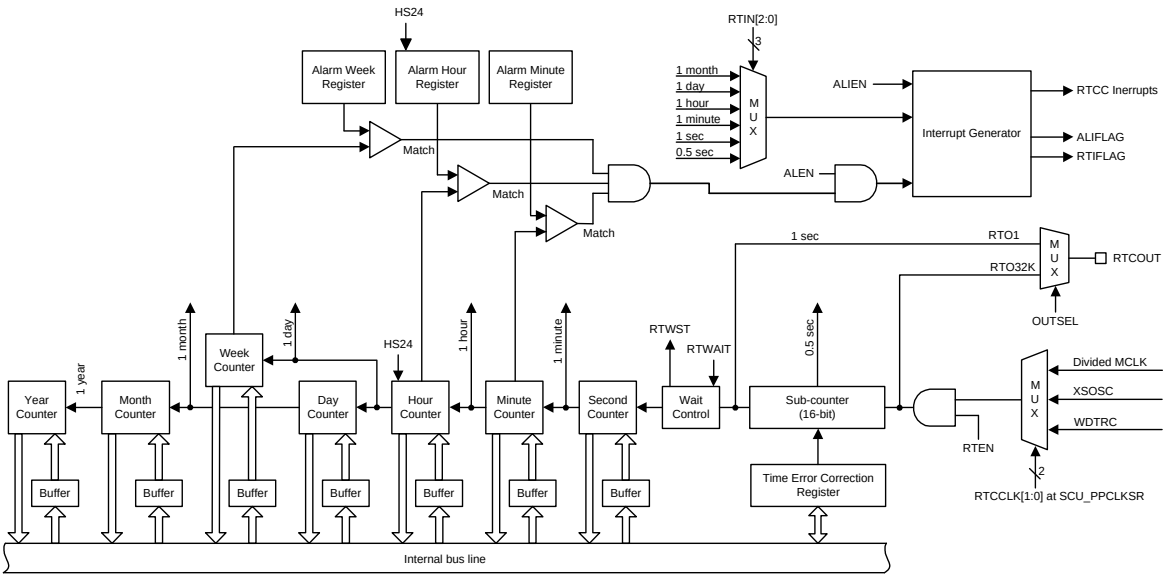
The RTCC is an independent BCD counter. The RTCC circuitry and the related control bits are not reset by a system reset other than POR.

Main operations of the RTCC are introduced in the following list:

- Calendar with 0.5 seconds, seconds, minutes, hours, day, week, month, and year up to 2099
- Time error correction function
- Alarm function with interrupt
- Wake-up possible from deep sleep mode

8.1 RTCC block diagram

Figure 28 shows a block diagram of the RTCC block.



NOTE: Time in the block diagram is based on 32.768 kHz.

Figure 28. RTCC Block Diagram

9 Timer counter 40/41/42/43 and Timer counter 50

9.1 Timer counter 40/41/42/43

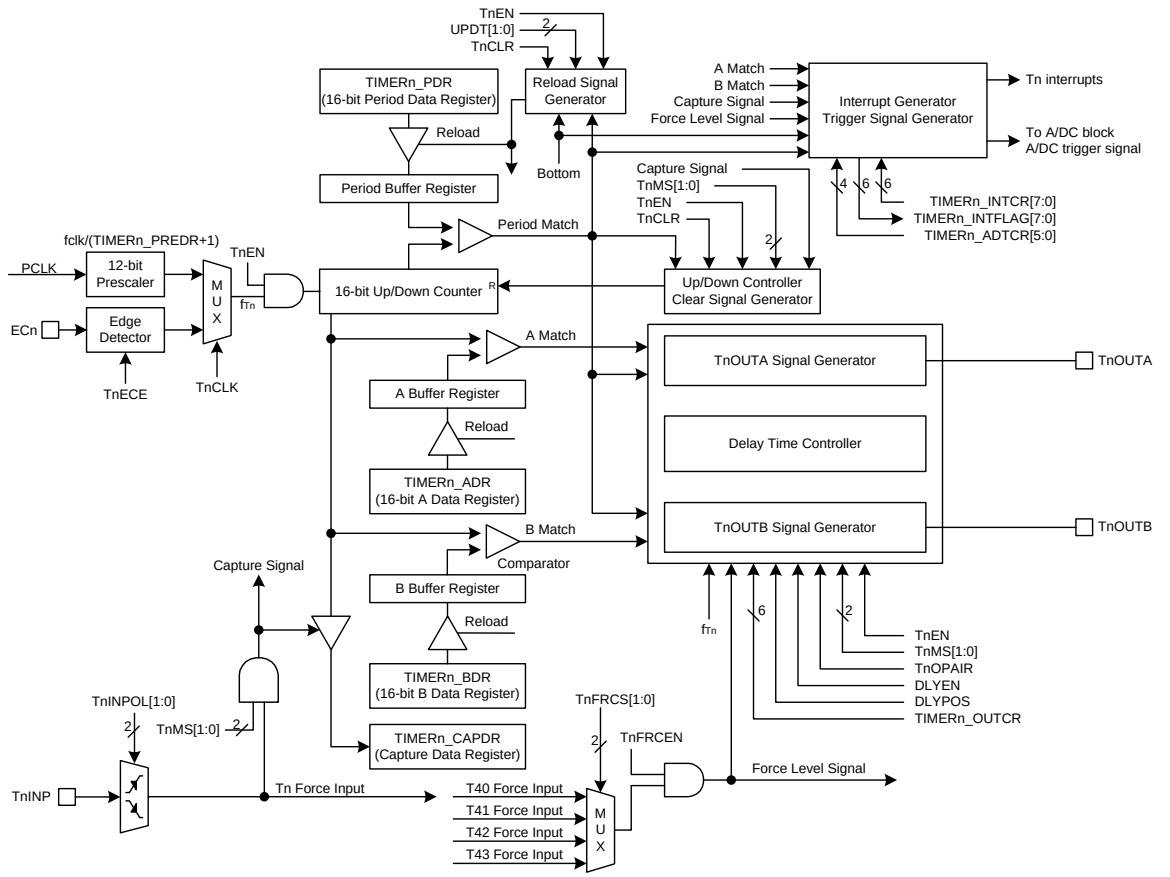
Each of Timer counter 40/41/42/43 is a 16-bit general purpose timer with two outputs. It has an independent 16-bit counter and a dedicated prescaler that feeds counting clock. It supports periodic timer, PWM pulse, one-shot and capture mode.

Main purpose of this timer is to work as a periodical tick timer or to provide a wake-up source. The operations of Timer counter 40/41/42/43 are listed in the followings:

- 12-bit prescaler and 16-bit up-counter
- Interval timer, One-shot timer, Back-to-back, and Capture mode
- Counter sharing function to connect each other
- Synchronous start and clear function

9.1.1 Timer counter 40/41/42/43 block diagram

Figure 29 shows the block diagram of a timer block unit.



NOTES:

1. Period/A/B match interrupts except for bottom can occur in the interval mode.
2. Period match interrupt only can occur in the capture mode.
3. 16-bit up/down counter in the capture mode is cleared to “0000H” after the counter value is loaded to the TIMERn_CAPDR register at a valid edge.
4. TnEN bit is automatically cleared to logic “0b” after one pulse is generated at a one-shot interval mode.
5. After the TnEN bit is set, the counting of TIMERn_CNT may be delayed 2 clocks or more.
6. High/low width of ECn clock should be longer than PCLK clock period.

Figure 29. Timer Counter 40/41/42/43 Block Diagram (n = 40, 41, 42, and 43)

9.1.2 Pins for Timer counter 40/41/42/43

Table 11. Pins and External Signals for Timer Counter 40/41/42/43 (n = 40, 41, 42, and 43)

PIN NAME	TYPE	DESCRIPTION
ECn	I	External clock input
TnINP	I	Capture or force input
TnOUTA	O	Timer A output
TnOUTB	O	Timer B output

9.2 Timer counter 50

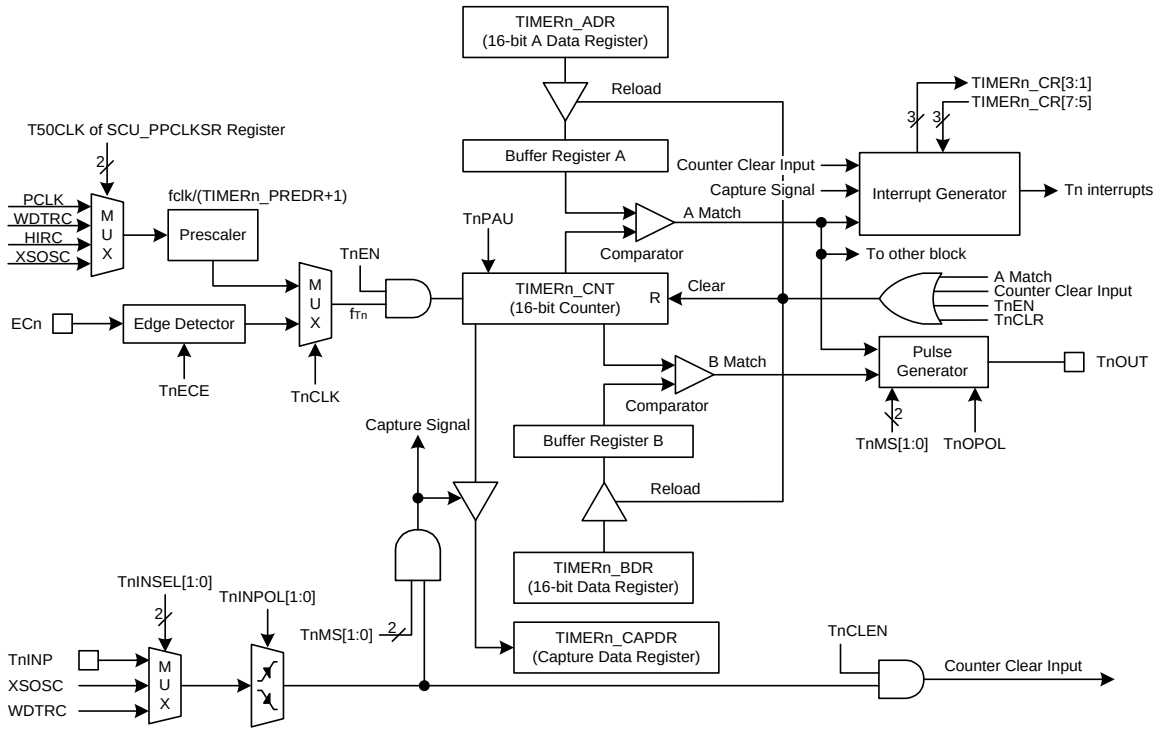
A timer block includes a single channel 16-bit general purpose timer. This timer has an independent 16-bit counter and a dedicated prescaler that feeds counting clock. It supports periodic timer, PWM pulse, one-shot timer and capture mode.

Additional free-run timer is optionally provided. Main purpose of this timer is to work as a periodical tick timer or to provide a wake-up source. The Timer counter 50 features the followings:

- 16-bit up-counter and 8-bit prescaler
- Interval timer, One-shot timer, PWM pulse, and Capture mode
- Synchronous start and clear function
- Low power operation with WDTRC or XSOSC

9.2.1 Timer counter 50 block diagram

Figure 30 shows the block diagram of a timer block unit.



NOTES:

1. TnEN is automatically cleared to logic '0' after one pulse is generated in PPG one-shot interval mode.
2. After TnEN bit is set, counting of TIMERn_CNT may be delayed by 2 clocks or more.
3. Counter clear input can control wake-up from Sleep mode by suppressing A-match interrupt.
4. High/low width of ECn clock should be longer than PCLK clock period.
5. The capture and counter clear input interrupts cannot be used as a wake-up source in DEEP SLEEP mode. That is, these interrupts will not be generated in DEEP SLEEP mode.

Figure 30. Timer Counter 50 Block Diagram (n = 50)

9.2.2 Pins for Timer counter 50

Table 12. Pins and External Signals for Timer Counter 50 (n = 50)

PIN NAME	TYPE	DESCRIPTION
ECn	I	External clock input
TnINP	I	Capture/Clear input
TnOUT	O	PWM/one-shot output

10 High speed 12-bit ADC

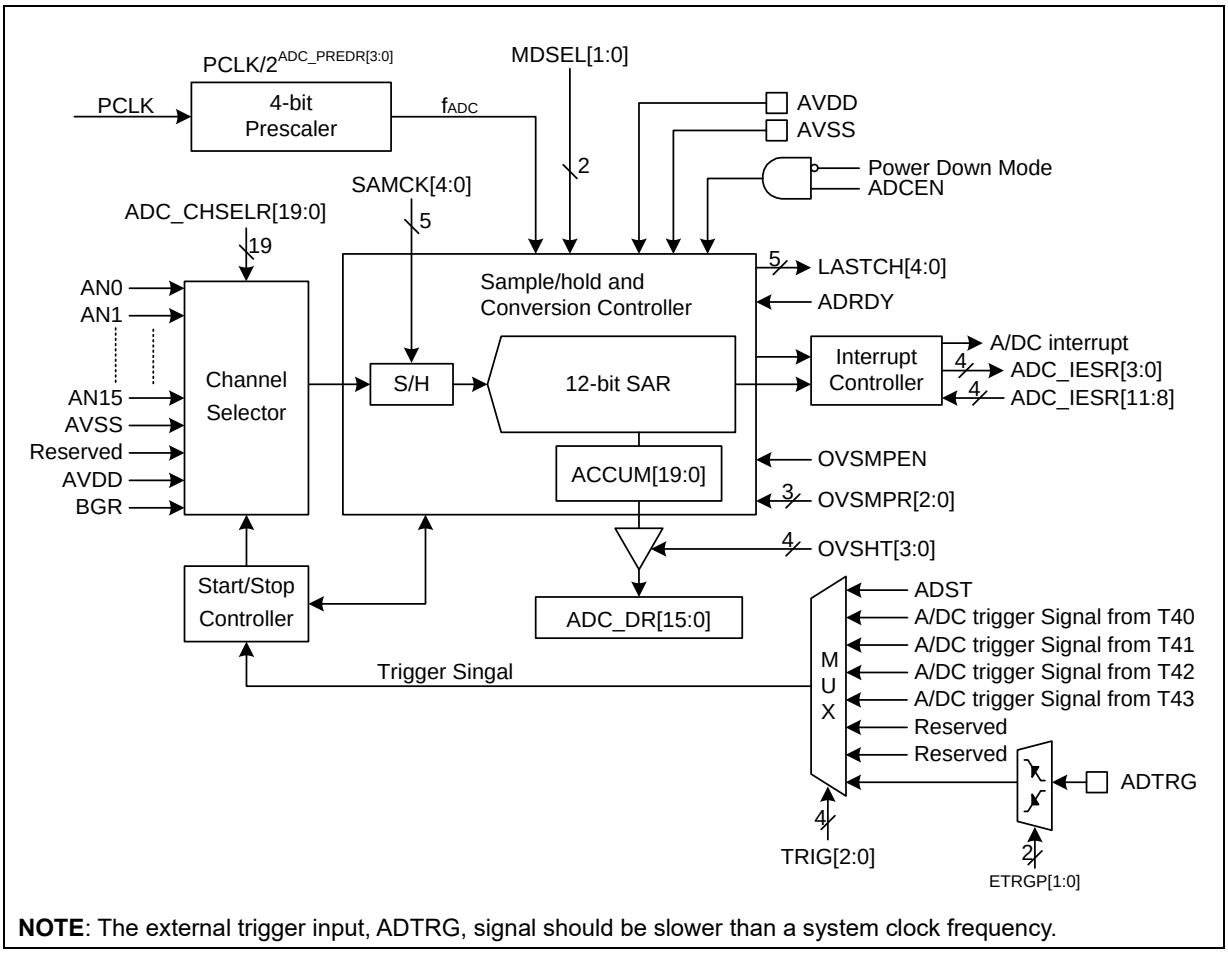
ADC (Analog-to-Digital Converter) of A31L12x series allows conversion of an analog input signal to a corresponding 12-bit digital value. Its A/D module has sixteen analog inputs as shown in Figure 31. Output of the multiplexer is the input into the converter, which generates the result through successive approximation.

The A/D module has seven registers such as a control register (ADC_CR), a data register (ADC_DR), a prescaler data register (ADC_PREDR), an oversampling control register (ADC_OVSCR), an interrupt enable and status register (ADC_IESR), a sampling time register (ADC_SAMR), and a channel selection register (ADC_CHSELR). The A/D module supports single, sequential, and continuous conversion modes. Main features of the ADC are listed in the followings:

- 16-channel of analog inputs
- S/W (ADST), Timer trigger (T40/41/42/43 ADC trigger signal), and external trigger support
- Conversion time: Up to 1us with 12 clocks + at least 4 sample/hold clocks
- 4-bit Prescaler and 16-bit data registers
- Up to 256 over sampling
- Single, sequential, and continuous conversion mode

10.1 12-bit ADC block diagram

Figure 31 shows a block diagram of an ADC block.



NOTE: The external trigger input, ADTRG, signal should be slower than a system clock frequency.

Figure 31. 12-bit ADC Block Diagram

10.2 Pins for 12-bit ADC

Table 13. Pins and External Signals for 12-bit ADC

PIN NAME	TYPE	DESCRIPTION
AN0	A	ADC Input 0
AN1	A	ADC Input 1
AN2	A	ADC Input 2
AN3	A	ADC Input 3
AN4	A	ADC Input 4
AN5	A	ADC Input 5
AN6	A	ADC Input 6
AN7	A	ADC Input 7
AN8	A	ADC Input 8
AN9	A	ADC Input 9
AN10	A	ADC Input 10
AN11	A	ADC Input 11
AN12	A	ADC Input 12
AN13	A	ADC Input 13
AN14	A	ADC Input 14
AN15	A	ADC Input 15
AVSS	AP	Analog GND
AVDD	AP	Analog Power

NOTE: Where A=Analog, AP= Analog Power

11 Comparator 0/1

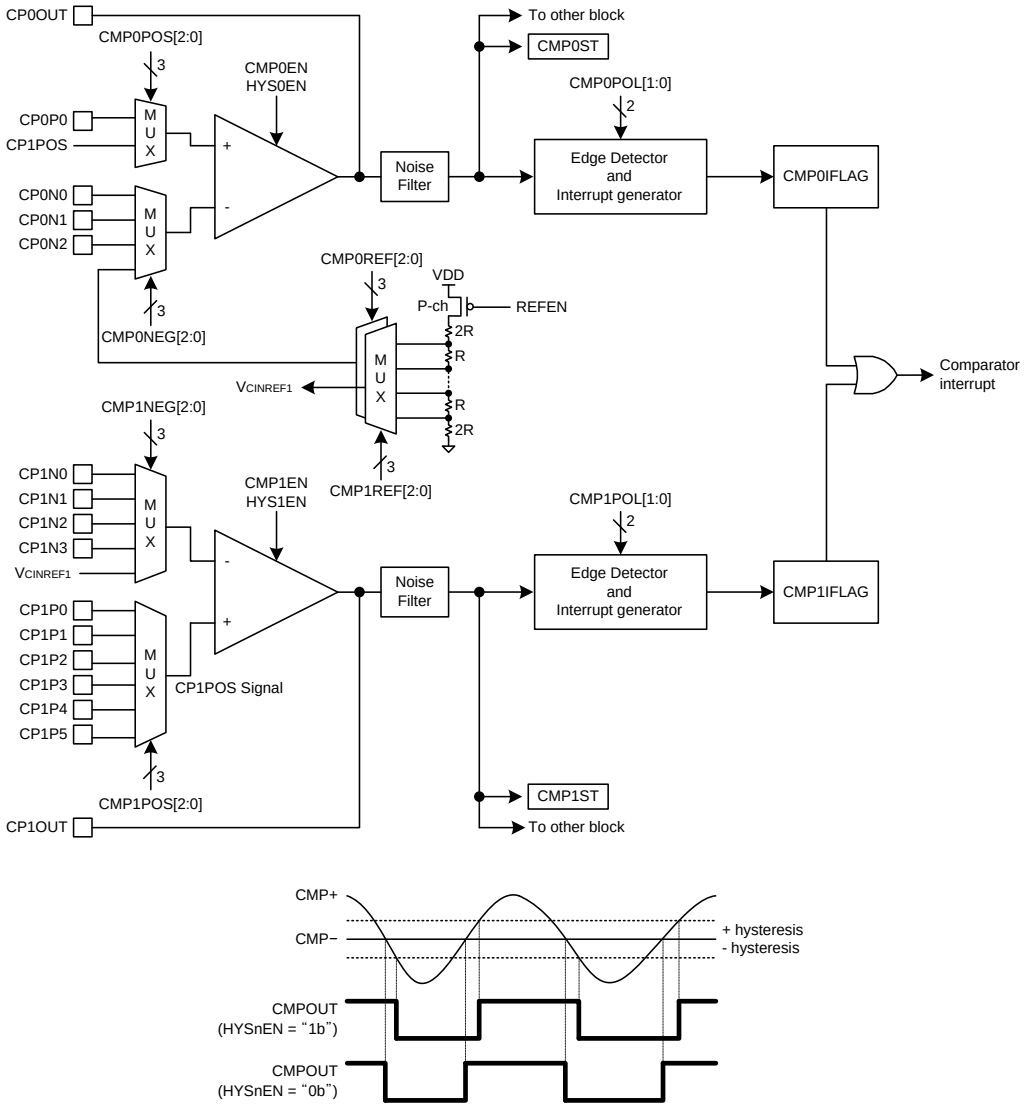
A31L12x series includes two comparator modules. Each comparator module has three registers such as a control register (CMP_CR), a status register (CMP_SR), and a reference control register (CMP_RCR). The comparator module has an internal reference circuit too.

The comparator module features the followings:

- External analog inputs
- Hysteresis function
- Low and fast speed selectable
- Wake-up possible from deep sleep mode

11.1 Comparator 0/1 block diagram

Figure 32 shows a block diagram of the comparator block.



NOTE: VDD should be greater than or equal to 2.0V if CP1P2, CP1P3, CP1P4, and CP1P5 are used as comparator pins for alternative functions.

Figure 32. Comparator 0/1 Block Diagram

11.2 Pins for Comparator 0/1

Table 14. Pins and External Signals for Comparator 0/1

PIN NAME	TYPE	DESCRIPTION
CP0P0	A	Comparator 0 positive input
CP0N0	A	Comparator 0 negative input
CP0N1	A	Comparator 0 negative input
CP0N2	A	Comparator 0 negative input
CP0OUT	A	Comparator 0 output
CP1P0	A	Comparator 1 positive input
CP1P1	A	Comparator 1 positive input
CP1P2	A	Comparator 1 positive input
CP1P3	A	Comparator 1 positive input
CP1P4	A	Comparator 1 positive input
CP1P5	A	Comparator 1 positive input
CP1N0	A	Comparator 1 negative input
CP1N1	A	Comparator 1 negative input
CP1N2	A	Comparator 1 negative input
CP1N3	A	Comparator 1 negative input
CP1OUT	A	Comparator 1 output

12 USART 10, UART 0/1, and LPUART

12.1 USART 10

USART (Universal Synchronous and Asynchronous serial Receiver and Transmitter) is a highly flexible serial communication device. The USART of A31L12x series features the followings:

- Full Duplex Operation. (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Baud Rate Generator
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits
- Odd or Even Parity Generation, and Parity Check Supported by Hardware.
- Supports Receive Character Detection and Receive Time Out Function
- Data OverRun Detection
- Framing Error Detection
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion
- Double Speed Asynchronous communication mode
- Up to 16MHz data transfer for SPI

12.1.1 USART 10 block diagram

Figure 33 shows a block diagram of the UART block.

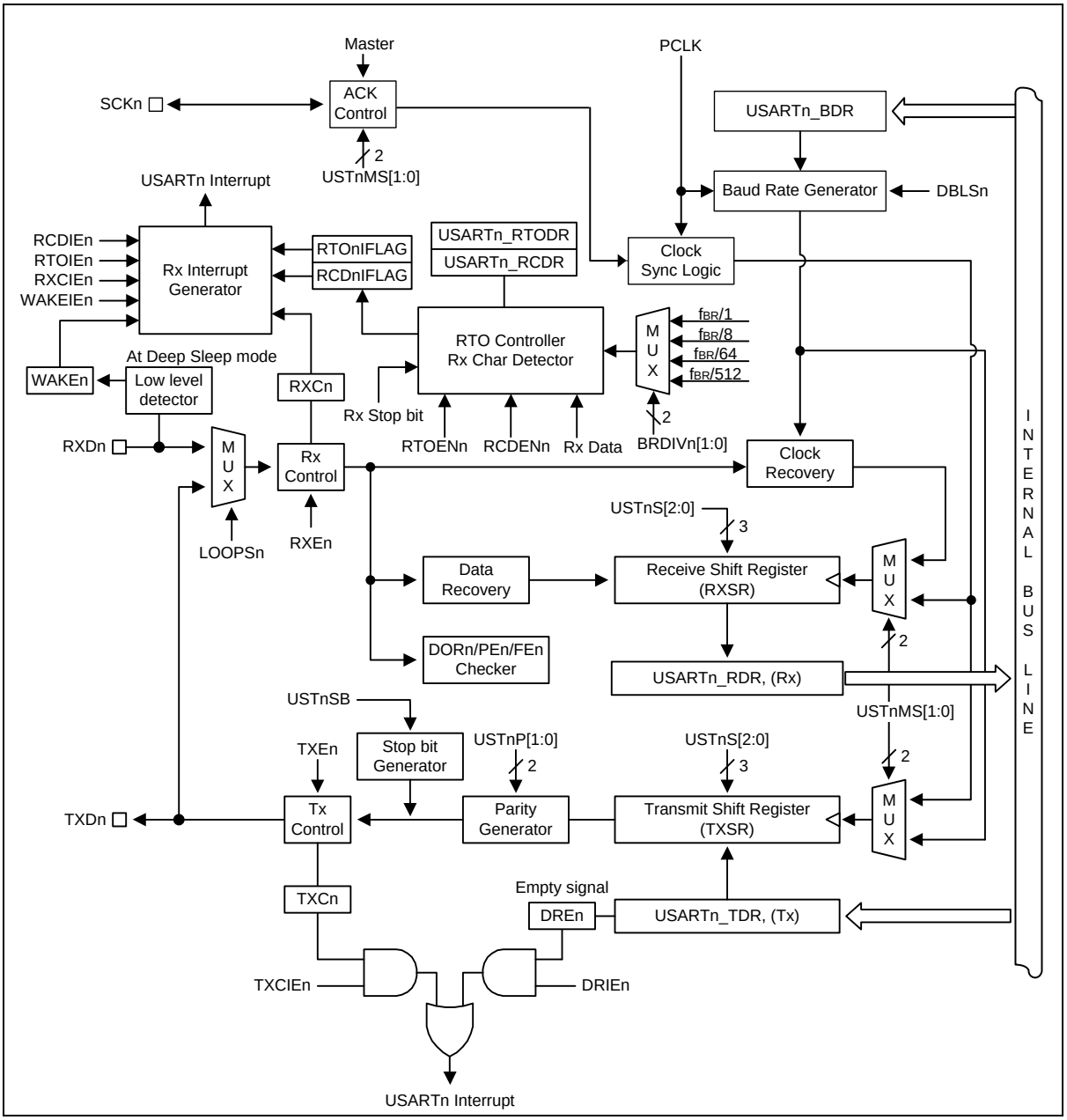
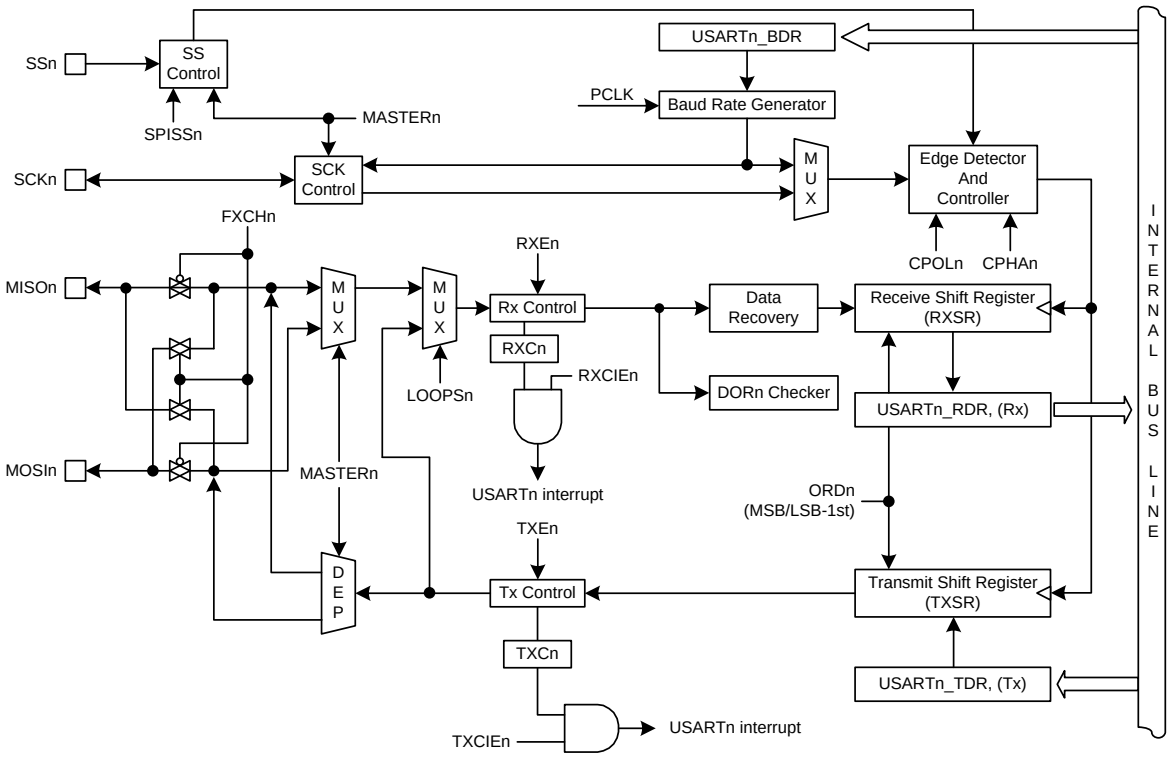


Figure 33. UART Block Diagram of USART (n = 10)

Figure 34 shows a block diagram of the SPI block.



NOTES:

1. The clock frequency of SCKn should be less than or equal to PCLK/2.
2. When DMA is used, the interval of data to be received requires at least 32 clock of PCLK.

Figure 34. SPIn Block Diagram of USART (n = 10)

12.1.2 Pins for USART 10

Table 15. Pins and External Signals for USART 10

PIN NAME	TYPE	DESCRIPTION
TXDn	O	UART Channel n transmit output
RXDn	I	UART Channel n receive input
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data (Master output, Slave input)
MISOn	I/O	SPIn Serial data (Master input, Slave output)

12.2 UART 0/1

There are built-in 2-channel of UART modules (Universal Asynchronous Receiver/Transmitter) in A31L12x series. UART operation status including error status can be read from a status register.

A baud rate generator, which generates proper baud rate, exists for each UART channel. This baud rate generator can divide PCLK from 1 to 65536. Then, baud rate is generated using a 1:16 clock and an 8-bit precision clock tuning function.

The UART 0/1 of A31L12x series features the followings:

- Compatible with 16450
- Configurable standard asynchronous control bit (start, stop, and parity)
- Programmable 16-bit fractional baud generator
- Programmable serial communication
- 5-, 6-, 7- or 8- bit data transfer
- Even, odd, or no-parity bit insertion and detection
- 1-, 1.5- or 2-stop bit-insertion and detection
- 16-bit baud rate generation with 8-bit fraction control
- Hardware inter-frame delay function
- Stop bit error detection
- Detail status register

12.2.1 UART 0/1 block diagram

Figure 35 shows a block diagram of the UART block.

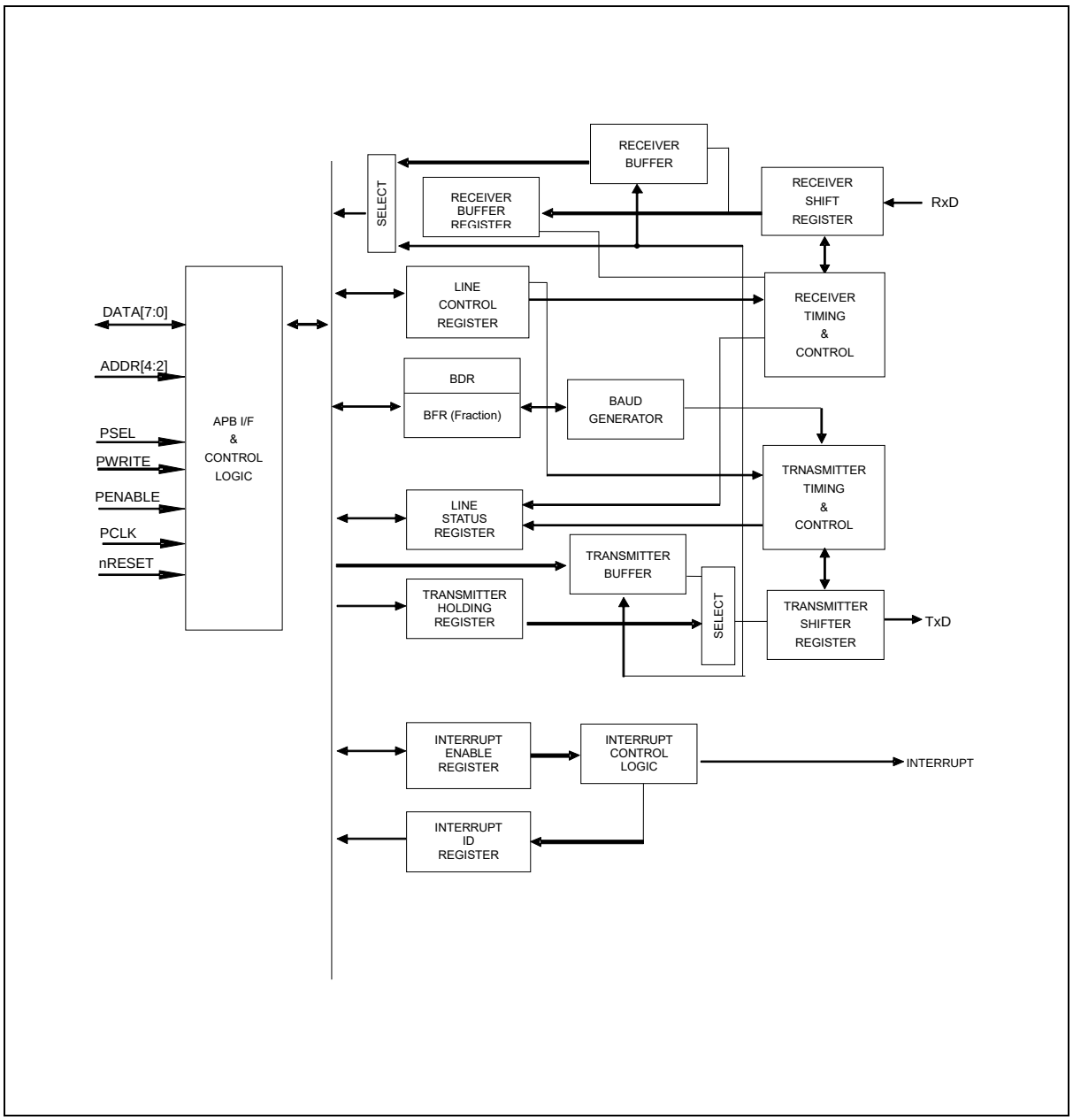


Figure 35. UART 0/1 Block Diagram

12.2.2 Pins for UART 0/1

Table 16. Pins and External Signals for UART 0/1

PIN NAME	TYPE	DESCRIPTION
TXDn	O	UART Channel n transmit output
RXDn	I	UART Channel n receive input

12.3 LPUART

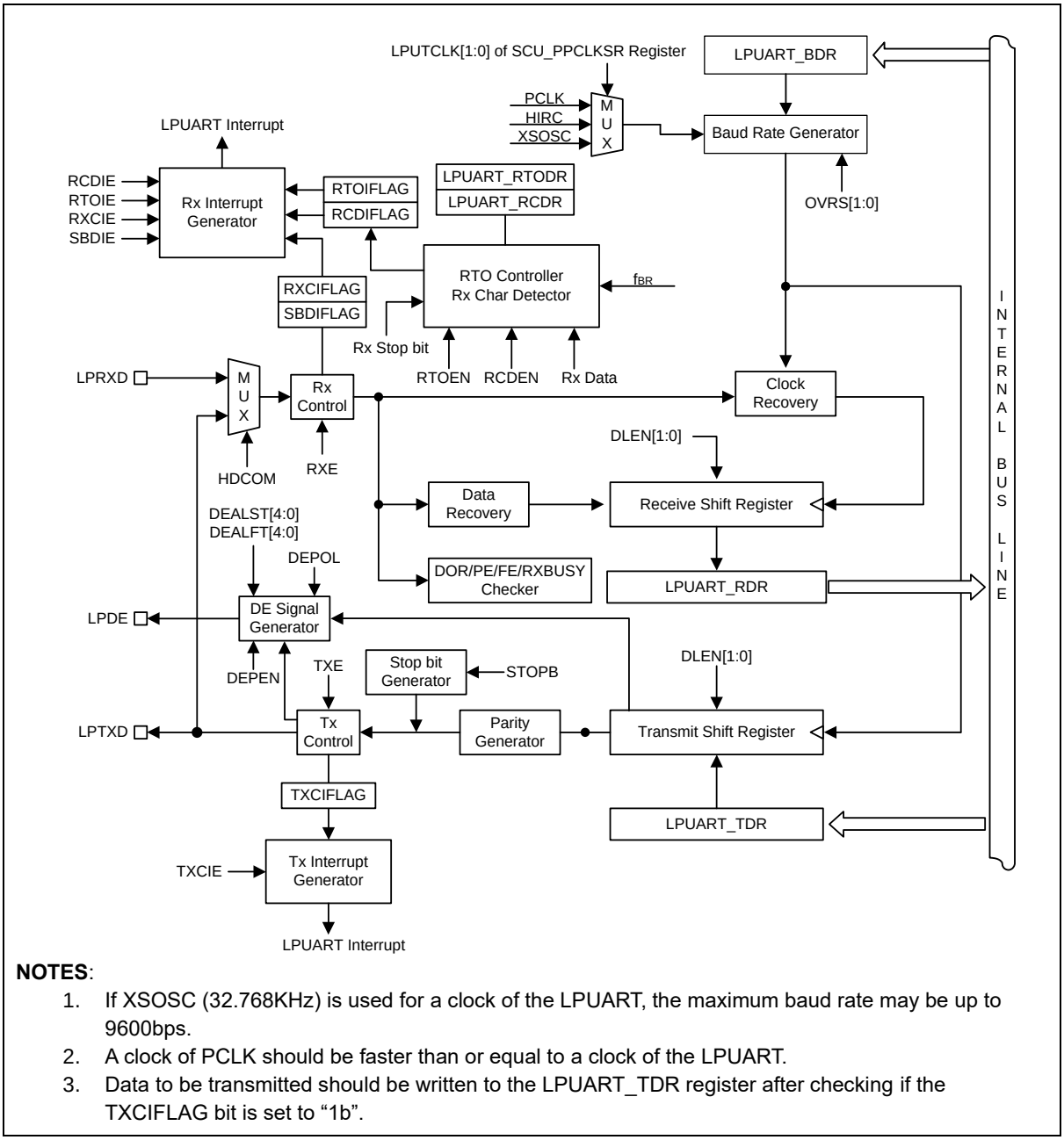
There is a built-in 1-channel of low power UART module (Universal Asynchronous Receiver/Transmitter) in A31L12x series. This LPUART (Low Power UART) supports asynchronous serial communication up to 9600bps in Deep sleep mode with 32.768KHz sub-oscillator. It also supports 1-wire half-duplex communication.

The LPUART of A31L12x series features the followings:

- Full-Duplex and Half-Duplex Operations
- Baud Rate Generator
- Supports Serial Frames with 5,6,7, or 8 Data bits and 1 or 2 Stop bits
- Odd or Even Parity Generation, and Parity Check Supported by Hardware
- Supports Receive Character Detection and Receive Time Out Function
- Baud Rate Compensation Function
- Supports up to 9600pbs with 32.768KHz sub-oscillator
- Data OverRun Detection
- Framing Error Detection
- Double Speed Asynchronous Communication Mode

12.3.1 LPUART block diagram

Figure 36 shows a block diagram of the LPUART block.



NOTES:

1. If XSOSC (32.768KHz) is used for a clock of the LPUART, the maximum baud rate may be up to 9600bps.
2. A clock of PCLK should be faster than or equal to a clock of the LPUART.
3. Data to be transmitted should be written to the LPUART_TDR register after checking if the TXCIFLAG bit is set to “1b”.

Figure 36. LPUART Block Diagram

12.3.2 Pins for LPUART

Table 17. Pins and External Signals for LPUART

PIN NAME	TYPE	DESCRIPTION
LPTXD	O	Low Power UART transmit output
LPRXD	I	Low Power UART receive input
LPDE	O	Low Power UART DE signal output

13 I2C 0/1, SPI 0/1, and smartcard 0/1 interface

13.1 I2C 0/1 interface

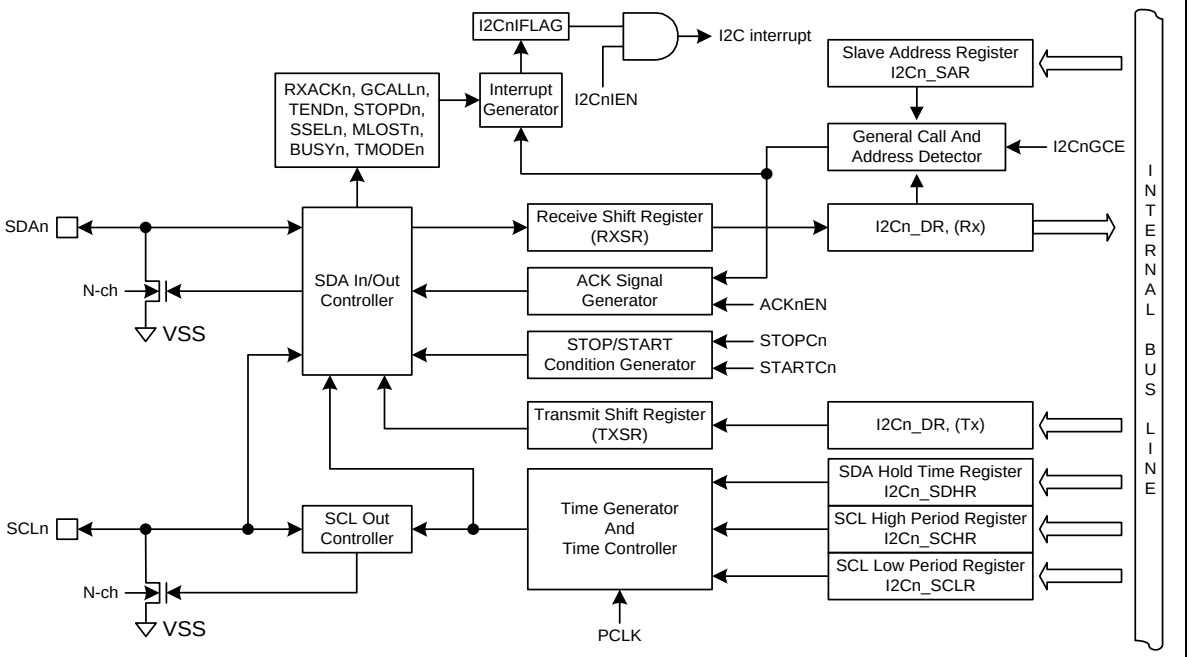
I2C is one of industrial standard serial communication protocols, which uses 2 bus lines, Serial Data Line (SDAn) and a Serial Clock Line (SCLn), to exchange data. Because both SDAn and SCLn lines are open-drain output, each line needs a pull-up resistor (n = 0 and 1).

The I2C interface 0/1 of A31L12x series features the followings:

- Compatible with I2C bus standard
- Multi-master operation
- Up to 1MHz data transfer read speed
- 7-bit address
- Support two slave addresses
- Both master and slave operation
- Bus busy detection

13.1.1 I2C 0/1 block diagram

Figure 37 shows a block diagram of the I2C block.



NOTE: When the corresponding port of I2C is a sub-function for SCLn/SDAn pin, the SCLn/SDAn pins are automatically set as N-channel open-drain outputs and the input latch is read when reading the pins. The corresponding pull-up resistor is determined by the control register.

Figure 37. I2C Block Diagram (n = 0 and 1)

13.1.2 Pins for I2C 0/1

Table 18. Pins and External Signals for I2C (n = 0 and 1)

PIN NAME	TYPE	DESCRIPTION
SCLn	I/O	I2C channel n Serial clock bus line (open-drain)
SDAn	I/O	I2C channel n Serial data bus line (open-drain)

13.2 SPI 0/1 interface

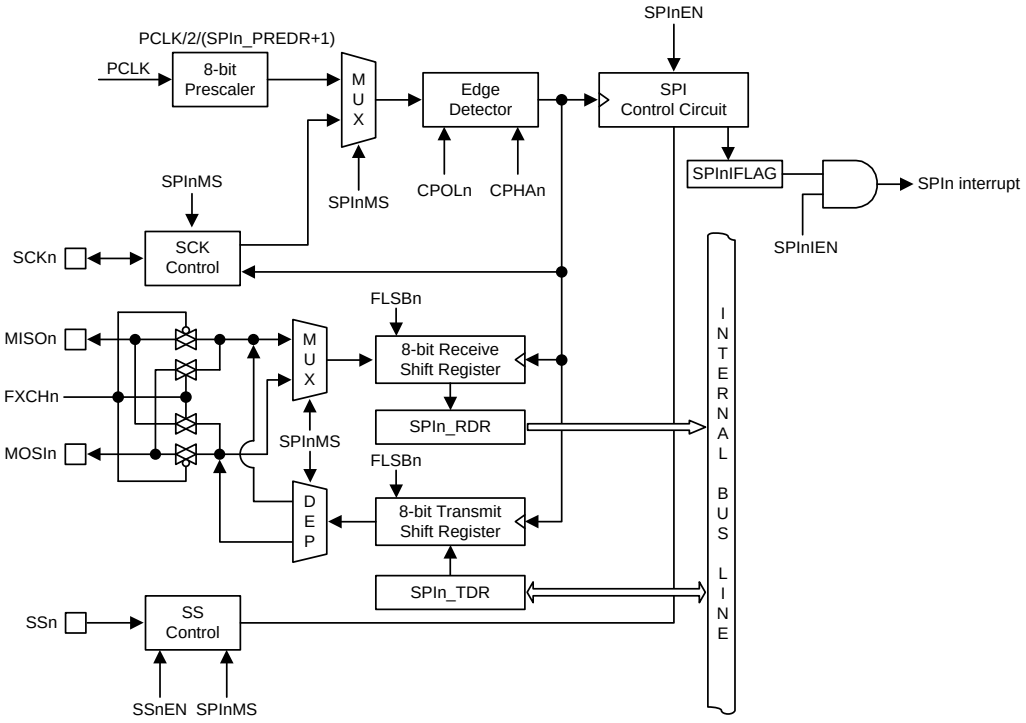
SPI interface allows synchronous serial data transfer between external serial devices. It can do full-duplex communication by using 4-wires (MOSIn, MISOn, SCKn, SSn) and support master/slave mode. In addition, the SPI can select serial clock (SCKn) polarity and whether LSB first data transfer or MSB first data transfer.

The SPI 0/1 of A31L12x series features the followings:

- Supports master and slave mode
- Clock polarity selectable
- Up to 16MHz data transfer
- Exchangeable MOSIn and MISOn function

13.2.1 SPI 0/1 block diagram

Figure 38 shows a block diagram of the SPI block.



NOTES:

1. Clock frequency of SCKn should be less than or equal to PCLK/2.
2. Interrupts of SPIn occur only when one byte transmission/receiving finishes. So, status (SPInMS and SSnHIGH) bits should be checked by s/w.
3. When DMA is used, interval between data-receiving requires at least 32 clock of PCLK.

Figure 38. SPI Block Diagram (n = 0 and 1)

13.2.2 Pins for SPI 0/1

Table 19. Pins and External Signals for SPI (n = 0 and 1)

PIN NAME	TYPE	DESCRIPTION
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data (Master output, Slave input)
MISOn	I/O	SPIn Serial data (Master input, Slave output)

13.3 Smartcard interface 0/1

A smartcard interface block of A31L12x series is based on ISO/IEC 7816-3 standard. It supports UART mode to communicate with others.

This smartcard interface block has thirteen registers such as control registers (SCn_CR1, SCn_CR2, SCn_CR3), receive data register (SCn_RDR), transmit data register (SCn_TDR), baud-rate data register (SCn_BDR), and so on.

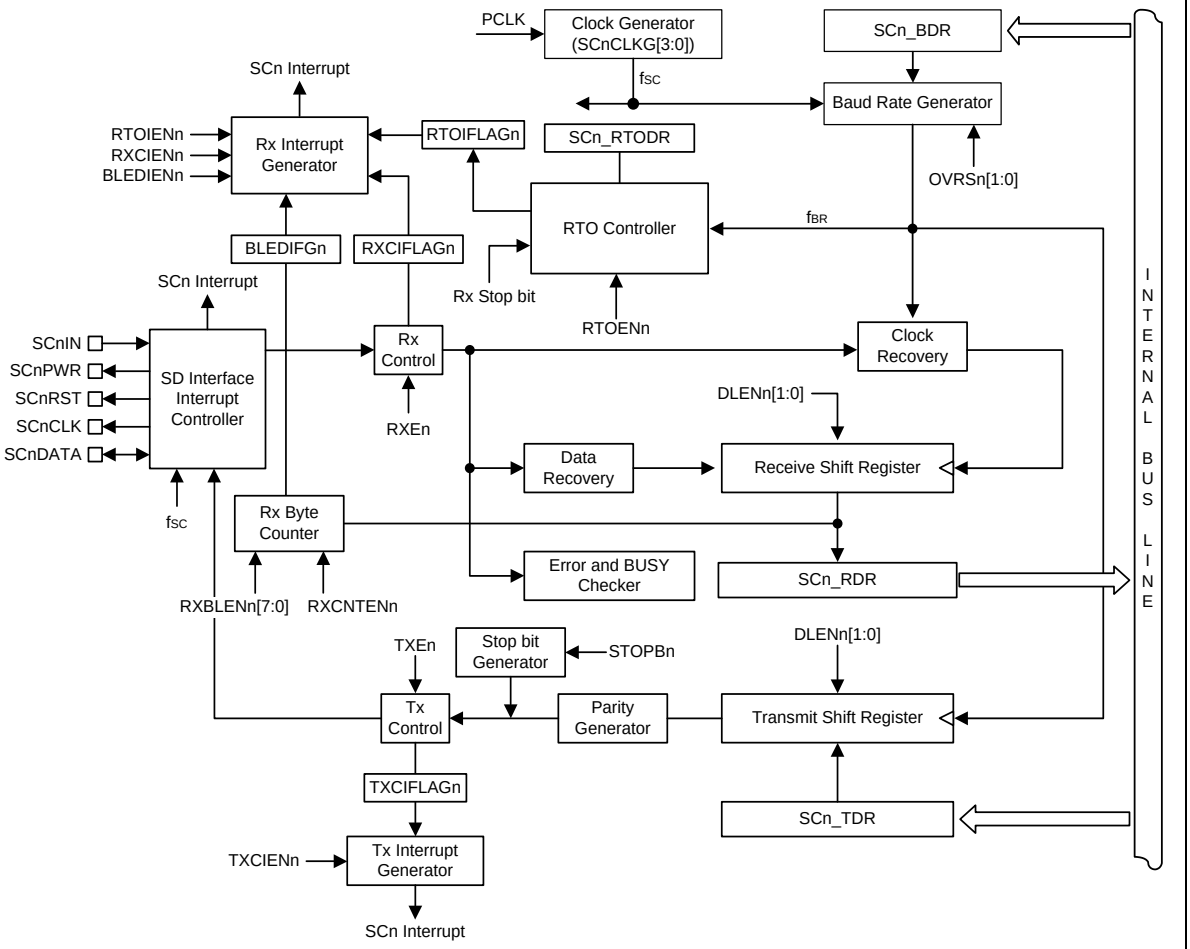
The smartcard interface 0/1 of A31L12x series features the followings:

- ISO-7816-3 T = 0, T = 1 compliant

- Supports DMA transfer
- Programmable guard time
- Supports auto activation sequence
- Supports auto warm reset sequence
- Supports auto deactivation sequence
- Supports auto convention detection sequence
- Baud rate compensation function
- Selectable UART mode
- Full duplex asynchronous operation
- Programmable baud-rate generation
- Selectable even, odd, or no parity bit generation and detection
- Selectable 1 or 2 stop bit generation
- Programmable data delay time after stop bit

13.3.1 Smartcard interface 0/1 block diagram

Figure 39 shows a block diagram of the Smartcard interface block.



NOTE: After checking that the TXCIFLAGn bit is set to '1', write the data to be sent to the SCn_TDR register.

Figure 39. Smartcard Interface Block Diagram (n = 0 and 1)

13.3.2 Pins for Smartcard interface 0/1

Table 20. Pins and External Signals for Smartcard Interface (n = 0 and 1)

PIN NAME	TYPE	DESCRIPTION
SCnPWR	O	Smartcard power control output
SCnDATA	I/O	Smartcard data input/output
SCnRST	O	Smartcard reset output
SCnCLK	O	Smartcard clock output
SCnIN	I	Smartcard detection input
SCnTXD	O	SCn's UART data output
SCnRXD	I	SCn's UART data input

14 LCD driver

LCD driver of A31L12x series includes an LCD control register (LCD_CR) and an LCD bias and contrast control register (LCD_BCCR). LCLK[1:0] of the LCD_CR determines frequency of COM signal scanning each segment output. A RESET clears the LCD_CR, and sets the LCD_BCCR to logic '0'.

LCD display can continue its operation even during Sleep mode and Deep sleep mode if it uses a selected clock for LCD driver.

A clock and duty of the LCD driver is initialized by hardware whenever a value is written to the control register. So, it is recommended not to rewrite the LCD_CR frequently.

14.1 LCD driver block diagram

Figure 40 shows a block diagram of the LCD driver block.

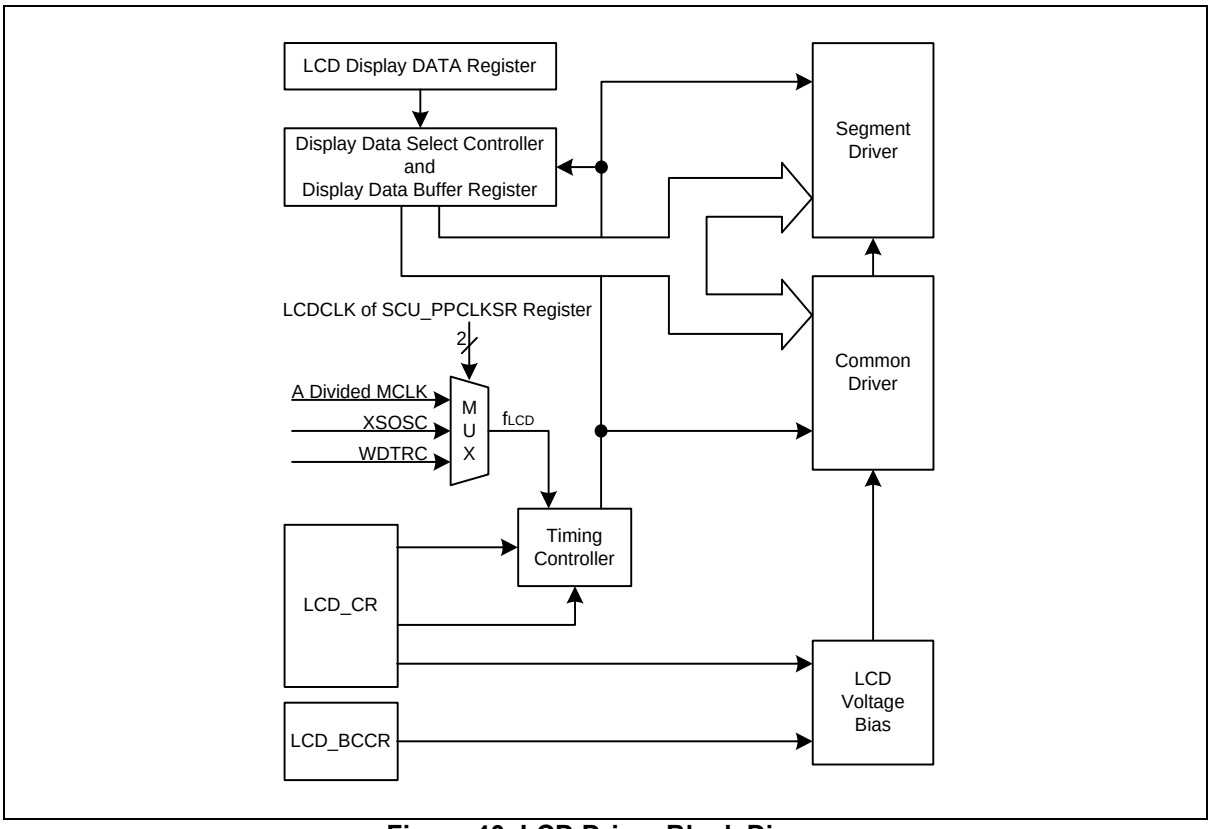


Figure 40. LCD Driver Block Diagram

14.2 Pins for LCD driver

Table 21. Pins and External Signals for LCD Driver

PIN NAME	TYPE	DESCRIPTION
COM0 - COM7	O	LCD common signal outputs
SEG0 - SEG32	O	LCD segment signal outputs
VLC0	I/O	LCD bias voltage input/output

15 CRC and checksum

A CRC (cyclic redundancy check) generator is used to obtain 8/16/32-bit CRC code of Flash ROM and any data stream.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of functional safety standards, they offer means of verifying Flash memory's integrity.

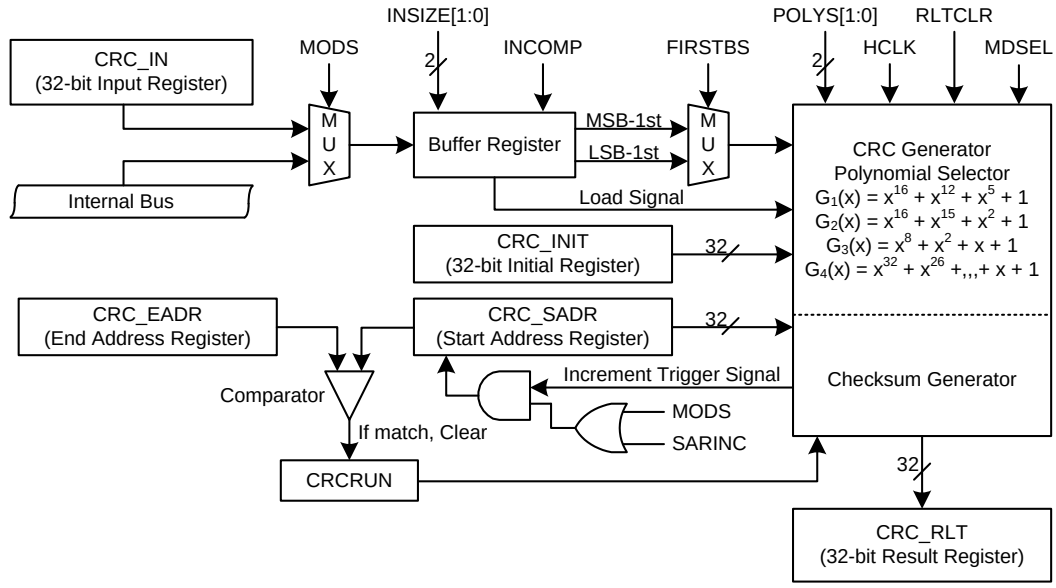
The CRC generator helps computing the signature of the software during runtime, comparing with a reference signature.

A CRC generator of A31L12x series has following features:

- Auto CRC and User CRC Mode
- Supports CRC-CCITT ($G_1(x) = x^{16} + x^{12} + x^5 + 1$)
- Supports CRC-16 ($G_2(x) = x^{16} + x^{15} + x^2 + 1$)
- Supports CRC-8 ($G_3(x) = x^8 + x^2 + x + 1$)
- Supports CRC-32 ($G_4(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$)
- CRC and Checksum mode
- CRC/Checksum Start Address Auto Increment (User mode only)

15.1 CRC and checksum block diagram

Figure 41 shows a block diagram of the CRC and checksum interface block.



NOTES:

1. The operation is finished after calculating from the CRC_SADR to the CRC_EADR on auto mode or SARINC=1.
2. The CRC_SADR and CRC_EADR are the same value after completion.
3. End address (CRC_EADR) must be greater than start address (CRC_SADR).
4. The end address must be at least 0x7C from the start address in “Auto mode”.
5. The CRC_SADR/CRC_EADR in “Auto mode” should have any value in flash memory area (0x10000000 to 0x1000FFFF).
6. CPU will be held at “Auto mode” if the CPU is in the flash memory, and global interrupts should be disabled by software.
7. HCLK frequency should be less than or equal to 20MHz in “Auto mode” by CRC_CR.MODS bit.
8. During the Auto mode running, the CRC_CR register can’t be written and the CRC_RLT register can’t be read.

Figure 41. CRC and Checksum Block Diagram

16 DMA controller

DMA (Direct Memory Access) controller transfers data without s/w assert. The DMA has 5 channels, and the DMA controller has four registers such as a control register (DMACHn_CR), a peripheral address register (DMACHn_PAR), a memory address register (DMACHn_MAR), and an interrupt enable and status register (DMACHn_IESR).

The DMA controller of A31L12x series features the followings:

- Supports 5 channels
- Supports 8/16/32-bit data size
- Transfer memory to peripheral
- Transfer peripheral to memory

16.1 DMA controller block diagram

Figure 42 shows a block diagram of the DMA controller block.

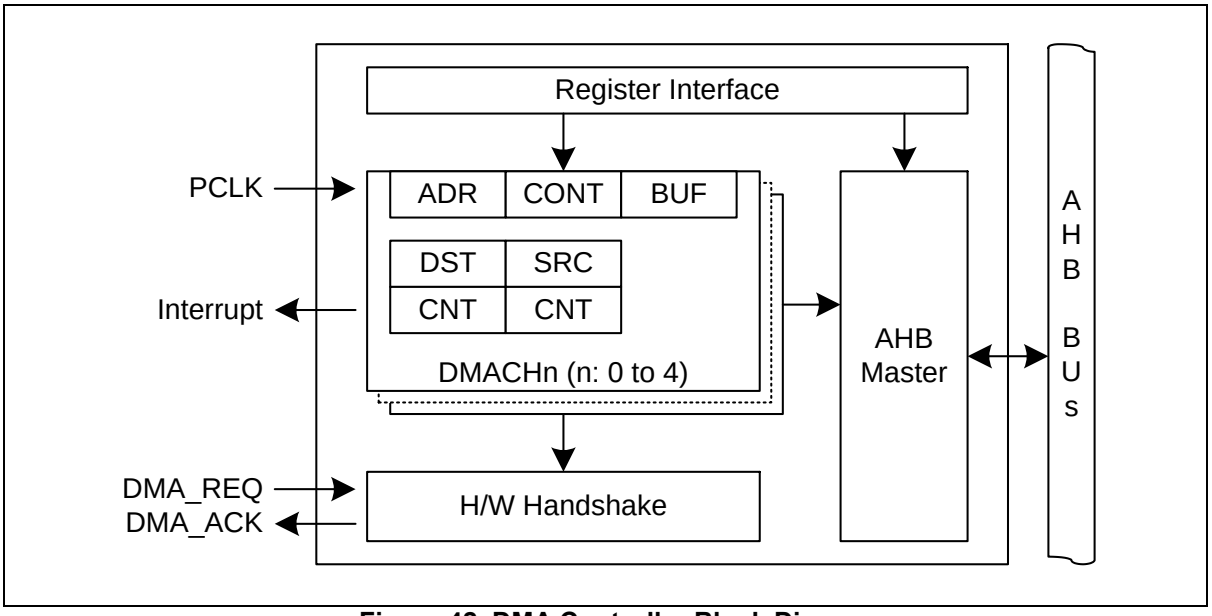


Figure 42. DMA Controller Block Diagram

17 Electrical characteristics

Unless otherwise specified, test conditions for DC characteristics are as shown in the followings:

- T_A = - 40 °C to +85°C(Commercial grade) or T_A = - 40 °C to + 105°C(Industrial grade)
- VDD = 1.65V to 3.6V

NOTES:

1. Refer to Figure 62. A31L12x Series Numbering Nomenclature for device part number by Commercial and Industrial grade.

17.1 Absolute maximum ratings

Absolute maximum ratings are limiting values of operating and environmental conditions, which should not be exceeded under the worst possible conditions.

Table 22. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	VDD	-0.3 to +4.0	V	–
Normal pin	V_I	-0.3 to VDD +0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 to VDD +0.3	V	
	I_{OH}	-15	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	ΣI_{OH}	-60	mA	Maximum current (ΣI_{OH})
	I_{OL}	20	mA	Maximum current sunk by (I_{OL} per I/O pin)
	ΣI_{OL}	80	mA	Maximum current (ΣI_{OL})
5V tolerant pin	VI	-0.3 to +6.0	V	Voltage on any pin with respect to VSS
Total power dissipation	P_T	300	mW	–
Storage temperature	T_{STG}	-65 to +150	°C	–

17.2 Recommended operating conditions

Table 23. Recommended Operating Conditions

Parameter	Symbol	Conditions			Min	Max	Units
Operating voltage	VDD	fx = 32 to 38KHz	Sub Clock		1.65	3.6	V
		fx = 2.0 to 4.2MHz	Main Clock	Ceramic	2.2	3.6	
		fx = 2.0 to 16MHz		Crystal	2.7	3.6	
		fx = 2.0 to 32MHz	External Clock		3.0	3.6	
		fx = 40KHz	Internal RC		1.65	3.6	
		fx = 2.5 to 32MHz			1.65	3.6	
Input voltage	V_{IN}	Normal Pin			-0.3	VDD+0.3	V
		5V tolerance Pins, PD[4:1]	2.0V ≤ VDD ≤ 3.6V		-0.3	5.5	
			1.65V ≤ VDD < 2.0V		-0.3	5.0	
Operating temperature	T_{OPR}	VDD = 1.65 to 3.6V (Commercial grade)			-40	85	°C
		VDD = 1.65 to 3.6V (Industrial grade)			-40	105	

17.3 ADC characteristics

Table 24. ADC Characteristics

(TA = 25℃)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Resolution	–	–		–	12	–	bit
Integral non-linearity	INL	AVDD=1.8V – 3.6V		–	–	±6	LSB
Differential non-linearity	DNL			–	–	±1	
Zero offset error	ZOE			–	–	±5	
Full scale error	FSE			–	–	±5	
Integral non-linearity	INL	AVDD=1.65V – 3.6V		–	–	±6	LSB
Differential non-linearity	DNL			–	–	±1.5	
Conversion time	t_{CONV}	AVDD=2.7V – 3.6V		1	–	–	µs
		AVDD=1.8V – 3.6V		2	–	–	
		AVDD=1.65V – 3.6V		2	4	–	
Analog input voltage	V_{AN}	–		VSS	–	AVDD	V
Analog voltage	AVDD	–		VDD-0.3	VDD	VDD+0.3	V
ADC stabilization time	t_{STAB}	–		–	–	16	$1/f_{ADC}$
Band gap reference buffer voltage	V_{ADCBUF}	–		900	950	1000	mV
ADC input leakage current	I_{AN}	AVDD=3.0V		–	–	2	µA
ADC current	I_{ADC}	Enable	AVDD=3.0V, f_{ADC}=16MHz	–	400	800	µA
		Disable		–	–	10	nA

NOTES:

1. Zero offset error is a difference between 0x000 and the converted output for zero input voltage (VSS).
2. Full scale error is a difference between 0xFFF and the converted output for top input voltage (VDD).

17.4 Power-on reset characteristics

Table 25. Power-on Reset Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reset release level	V_{POR}	–	–	1.2	–	V
Hysteresis	△V	–	–	0.1	–	V
VDD voltage rising time	t_R	0.2V to 2.0V	0.05	–	100	V/ms
POR current	I_{POR}	–	–	21	40	nA

17.5 Comparator characteristics

Table 26. Comparator Characteristics

(TA = 25℃)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input offset voltage	VOF	VDD=3.0V, VIN=1/2VDD		–	±4	±20	mV
Operating voltage	VDD	All comparator pins except below		1.65	–	3.6	V
		CP1P2, CP1P3, CP1P4, CP1P5		2.0	–	3.6	
Startup time	t_{START}	Fast Speed		–	15	20	µs
		Slow Speed		–	20	25	
Propagation delay	t_{DELAY}	1.65V ≤ VDD ≤ 2.7V	Fast Speed	–	1.2	4	µs
		2.7V ≤ VDD ≤ 3.6V		–	0.8	2	
		1.65V ≤ VDD ≤ 2.7V	Slow Speed	–	2.5	6	
		2.7V ≤ VDD ≤ 3.6V		–	1.8	3.5	
Hysteresis	△V+	VDD=3.0V, VIN- = 1/2VDD, HYSnEN=1		5	10	20	mV
	△V-			-20	-10	-5	
Minimum input level	V_{INMIN}	HYSnEN=1		50	–	–	mVp-p
Reference resistors	R_{REF}	VDD=3.0V		21	30	39	KΩ
Comparator current	ICMP	Enable, fast speed	VDD=3.0V	–	3.5	5	µA
		Enable, slow speed		–	1.0	2	
		Disable		–	–	0.02	

17.6 Low voltage reset/ indicator characteristics

Table 27. Low Voltage Reset Characteristics

(TA = 25℃)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Detection level	V_{LVR} V_{LVI}	• LVR: All levels, • LVI: Other levels except 1.5V, • 1.50V level: Rising edge voltage, • Other levels: Falling edge voltage		–	1.50	1.64	V
				1.65	1.75	1.90	
				1.75	1.90	2.05	
				1.90	2.05	2.20	
				2.05	2.20	2.35	
				2.15	2.35	2.55	
				2.30	2.50	2.70	
				2.45	2.65	2.85	
Hysteresis	△V	–		–	40	150	mV
Minimum pulse width	t_{LVRW} t_{LVIW}	–		100	–	–	µs
LVR/LVI current	$I_{LVR/LVI}$	Enable, one of two	VDD = 3V	–	200	400	nA
		Enable, both		–	250	500	
		Disable		–	–	10	

17.7 High frequency internal RC oscillator characteristics

Table 28. High Frequency Internal RC Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{HIRC}	VDD = 1.65V to 3.6V	–	32	–	MHz
Accuracy	–	T_A = 0 °C to + 50 °C	–	–	±1.5	%
		T_A = -40 °C to +85 °C (commercial grade)	–	–	±3.5	
		T_A = -40 °C to +105 °C (industrial grade)	–	–	±4.5	
Clock duty ratio	T_{OD}	–	40	50	60	%
Stabilization time	t_{HFS}	–	–	–	2	µs
IRC current	I_{HIRC}	Enable	–	300	450	µA
		Disable	–	–	10	nA

17.8 Internal watchdog timer RC oscillator characteristics

Table 29. Internal Watchdog Timer RC Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{WDTRC}	–	34	40	46	KHz
Stabilization time	t_{WDTS}	–	–	–	100	µs
WDTRC current	I_{WDTRC}	Enable	–	450	650	nA
		Disable	–	–	10	

17.9 LCD voltage characteristics

Table 30. LCD Voltage Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
LCD voltage	VLC0	LCD contrast disabled, 1/4 bias		Typx0.95	VDD	Typx1.05	V
		LCD contrast enabled, 1/4 bias, No Panel load	VLCD[3:0]=0x00	Typx0.94	VDDx32/47	Typx1.06	V
			VLCD[3:0]=0x01		VDDx32/46		
			VLCD[3:0]=0x02		VDDx32/45		
			VLCD[3:0]=0x03		VDDx32/44		
			VLCD[3:0]=0x04		VDDx32/43		
			VLCD[3:0]=0x05		VDDx32/42		
			VLCD[3:0]=0x06		VDDx32/41		
			VLCD[3:0]=0x07		VDDx32/40		
			VLCD[3:0]=0x08		VDDx32/39		
			VLCD[3:0]=0x09		VDDx32/38		
			VLCD[3:0]=0x0A		VDDx32/37		
			VLCD[3:0]=0x0B		VDDx32/36		
			VLCD[3:0]=0x0C		VDDx32/35		
			VLCD[3:0]=0x0D		VDDx32/34		
			VLCD[3:0]=0x0E		VDDx32/33		
			VLCD[3:0]=0x0F		VDDx32/32		
LCD mid bias voltage NOTE	VLC1	• VDD = 2.7V to 3.6V • LCD clock = 0Hz • 1/4 bias, No panel load		Typ-0.2	3/4xVLC0	Typ+0.2	V
	VLC2			Typ-0.2	2/4xVLC0	Typ+0.2	
	VLC3			Typ-0.2	1/4xVLC0	Typ+0.2	
LCD driver output impedance	R_{LO}	VLCD=3V		–	5	10	kΩ
LCD bias dividing resistor	RLCD1	1/4 bias, T_A = 25°C		7	11	15	kΩ
	RLCD2			35	50	65	
	RLCD3			56	80	104	
	RLCD4			168	240	312	

NOTE: It is the middle output voltage when the VDD and the VLC0 node are connected.

17.10 DC electrical characteristics

Table 31. DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH}	All input pins, nRESET	0.8VDD	–	VDD	V
Input Low Voltage	V_{IL}	All input pins, nRESET	–	–	0.2VDD	V
Input hysteresis	△V	All input pins, nRESET, VDD=3V	100	200	–	mV
Output High Voltage	V_{OH}	VDD=3V, I_{OH} = – 10mA, T_A=25°C	VDD-1.0	–	–	V
Output Low Voltage	V_{OL}	VDD=3V, I_{OL} = 10mA, T_A=25°C	–	–	1.0	V
Input high leakage current	I_{IH}	All Input ports	–	–	1	µA
Input low leakage current	I_{IL}	All Input ports	– 1	–	–	µA
Pull-up resistor	R_{PU}	V_I=0V, T_A=25°C, VDD=3V All Input ports	25	50	100	kΩ
		V_I=0V, T_A=25°C, VDD=3V RESETB	150	250	400	
Pull-down resistor	R_{PD}	V_I=VDD, T_A=25°C, VDD=3V All Input ports	25	50	100	kΩ
OSC feedback resistor	R_{X1}	XIN=VDD, XOUT=VSS, T_A=25°C, VDD=3V	0.6	1.2	2.0	MΩ
	R_{X2}	T_A=25°C, VDD=3V	4.0	7.0	14.0	MΩ

17.11 Supply current characteristics

Table 32. Supply Current Characteristics

Parameter	Symbol	Conditions			Typ	Max	Units
Supply current	I_{DD1} (main run)	f_{HIRC} = 32MHz		VDD=3V, Code executed from flash	2.5	3.8	mA
		f_{HIRC} = 16MHz			1.6	2.4	
		f_{HIRC} = 8MHz	TA=85°C		1.1	1.6	
		f_{XIN} = 16MHz			1.5	2.3	
		f_{HIRC} = 32MHz		VDD=3V, Code executed from RAM, Flash power off	2.3	3.4	mA
		f_{HIRC} = 16MHz			1.4	2.1	
		f_{XIN} = 16MHz			1.4	2.1	
	I_{DD2} (main sleep)	f_{HIRC} = 32MHz		VDD=3V, Sleep in flash	1.3	2.0	mA
		f_{HIRC} = 16MHz			0.8	1.2	
		f_{XIN} = 16MHz			0.8	1.2	
		f_{HIRC} = 32MHz		VDD=3V, Sleep in RAM, Flash power off	1.3	2.0	mA
		f_{HIRC} = 16MHz			0.8	1.2	
		f_{XIN} = 16MHz			0.8	1.2	
	I_{DD3} (sub run)	f_{SUB} = 32.768KHz (C_L: 7pF), or f_{WDTRC} = 40KHz	T_A=25°C	VDD=3V Code executed from flash	12.0	20.0	uA
			T_A=85°C		18.0	30.0	
			T_A=105°C		30.0	50.0	
			T_A=25°C	VDD=3V, Code executed from RAM, Flash power off	9.0	15.0	uA
			T_A=85°C		15.0	35.0	
			T_A=105°C		22.0	55.0	
	I_{DD4} (sub sleep)	f_{SUB} = 32.768KHz (C_L: 7pF), or f_{WDTRC} = 40KHz	T_A=25°C	VDD=3V, Sleep in flash	2.0	5.0	uA
			T_A=85°C		6.0	18.0	
			T_A=105°C		12.0	30.0	
	I_{DD5} (deep sleep)	VDD=3V PMU_PWRCR.ALLPWR=0		T_A=25°C	0.65	1.5	uA
				T_A=85°C	4.5	9.0	
				T_A=105°C	11.0	25.0	
		VDD=3V PMU_PWRCR.ALLPWR=1		T_A=25°C	0.6	1.0	uA
				T_A=85°C	2.0	4.0	
				T_A=105°C	4.5	9.0	
		PMU_PWRCR.ALLPWR=0		VDD=3V, T_A=25°C, RTCC/f_{SUB} On	1.3	1.9	uA
		PMU_PWRCR.ALLPWR=1			1.2	1.7	

NOTES:

1. Where the f_{XIN} is an external main oscillator, the f_{SUB} is an external sub oscillator (ISET_I[2:0] = 0x5), the f_{HIRC} is a high frequency internal RC oscillator, and the fx is the selected system clock.
2. All supply current items don't include the current of an internal watch-dog timer RC (WDTRC) oscillator and a peripheral block except when explicitly mentioned.
3. All supply current items include the current of the power-on reset (POR) block.

17.12 AC characteristics

Table 33. AC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RESETB input low width	t_{RST}	VDD = 3 V	10	–	–	µs
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupts, VDD = 3 V	50	–	–	ns
External counter input high, low pulse width	t_{ECWH}, t_{ECWL}	VDD = 3 V All external counter input	1	–	–	$1/f_{PCLK}$
External counter transition time	t_{REC}, t_{FEC}	ECn, VDD = 3 V All external counter input	–	–	10	ns
I/O frequency	f_{IO1}	VDD = 3.0V, C_L = 30pF, All except f_{IO2}	–	–	10	MHz
	f_{IO2}	VDD = 2.7V, C_L = 30pF, SPI pins	–	–	16	

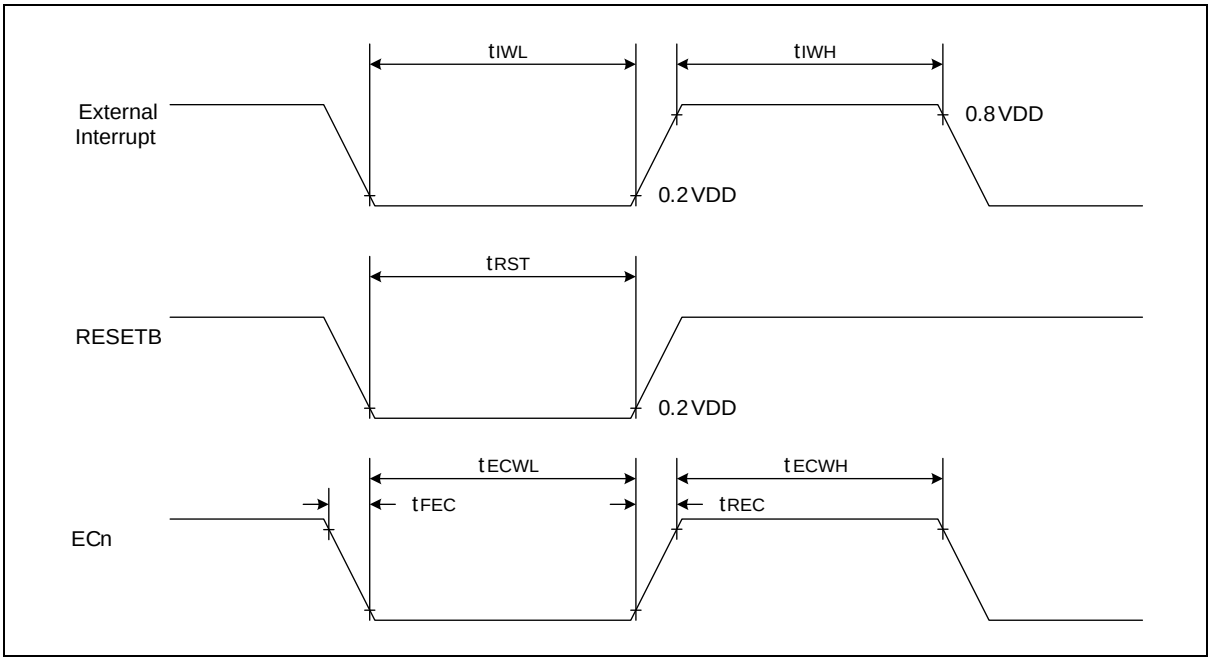


Figure 43. AC Timing

17.13 SPI characteristics

Table 34. SPI Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
SPI clock frequency	f_{SCK}	VDD ≥ 2.7V	Internal SCK source	–	–	16	MHz
			External SCK source				
	f_{SCK}	VDD ≥ 1.71V	Internal SCK source	–	–	12	
			External SCK source				
	f_{SCK}	VDD ≥ 1.65V	Internal SCK source	–	–	8	
			External SCK source				
Input/output clock high, low pulse width	t_{SCKH}, t_{SCKL}	Internal/External SCK source		0.8*Typ	t_{SCK}/2	1.2*Typ	ns
First output clock delay time	t_{FOD}	Internal/External SCK source, CPHA = 0		0.4*t_{SCK}	–	–	
Output clock delay time	t_{DS}	–		–	–	18	
Input setup time	t_{DIS}			13	–	–	
Input hold time	t_{DIH}			15	–	–	

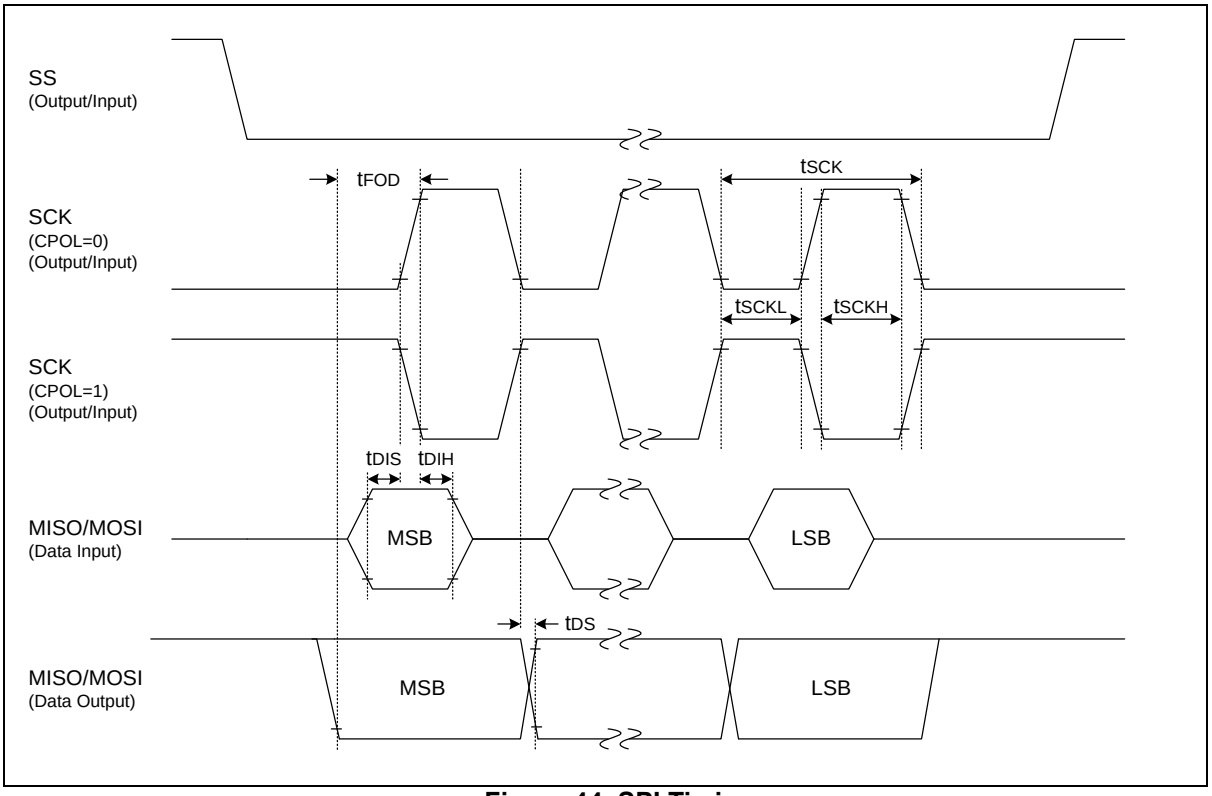


Figure 44. SPI Timing

17.14 I2C characteristics

Table 35. I2C Characteristics

Parameter	Symbol	Standard		Fast		Fast Plus		Units
		Min	Max	Min	Max	Min	Max	
I2C operating voltage	–	VDD ≥ 1.65V		VDD ≥ 2V		VDD ≥ 2.7V		_
Clock frequency	t_{SCL}	0	100	0	400	0	1000	KHz
Clock high pulse width	t_{SCLH}	4.0	–	0.6	–	0.26	–	µs
Clock low pulse width	t_{SCLL}	4.7	–	1.3	–	0.5	–	
Bus free time	t_{BF}	4.7	–	1.3	–	0.5	–	
Start condition setup time	t_{STSU}	4.7	–	0.6	–	0.26	–	
Start condition hold time	t_{STHD}	4.0	–	0.6	–	0.26	–	
Stop condition setup time	t_{SPSU}	4.0	–	0.6	–	0.26	–	
Stop condition hold time	t_{SPHD}	4.0	–	0.6	–	0.26	–	
Output Valid from Clock	t_{VD}	0	–	0	–	0	–	
Data input hold time	t_{DIH}	0	–	0	1.0	0	0.45	
Data input setup time	t_{DIS}	250	–	100	–	50	–	ns

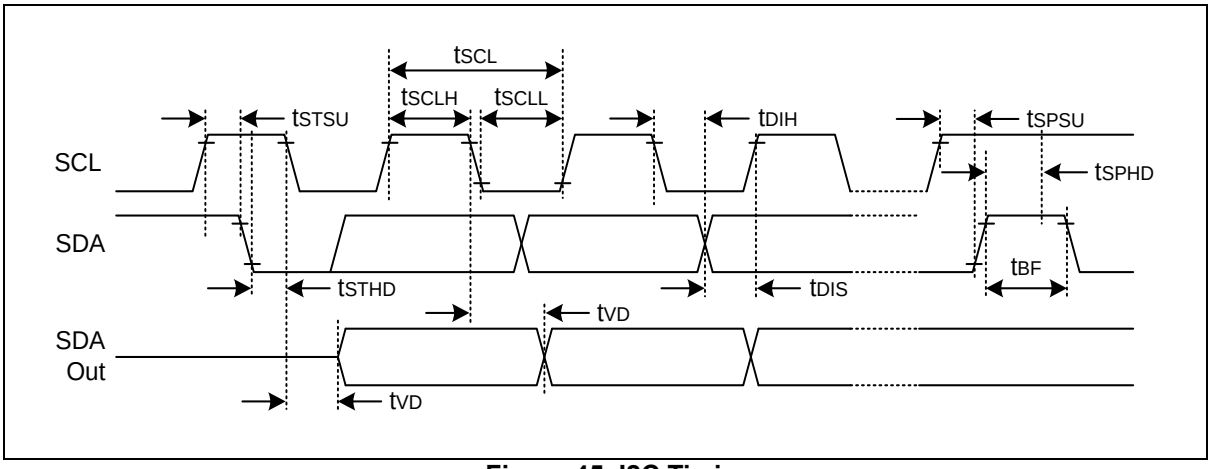


Figure 45. I2C Timing

17.15 UART timing characteristics

Table 36. UART Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Serial port clock cycle time	t_{SCK}	–	–	2000	KHz
Output data setup to clock rising edge	t_{S1}	t_{SCK} x 12/16	–	–	ns
Clock rising edge to input data valid	t_{S2}	–	–	t_{SCK} x 13/16	
Output data hold after clock rising edge	t_{H1}	–	–	50	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	t_{SCK} x 6/16	t_{SCK} x 8/16	t_{SCK} x 10/16	

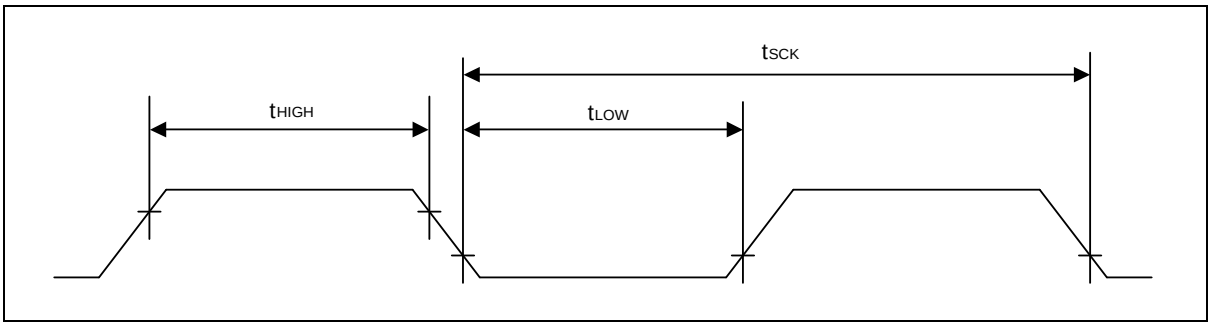


Figure 46. UART Timing Characteristics

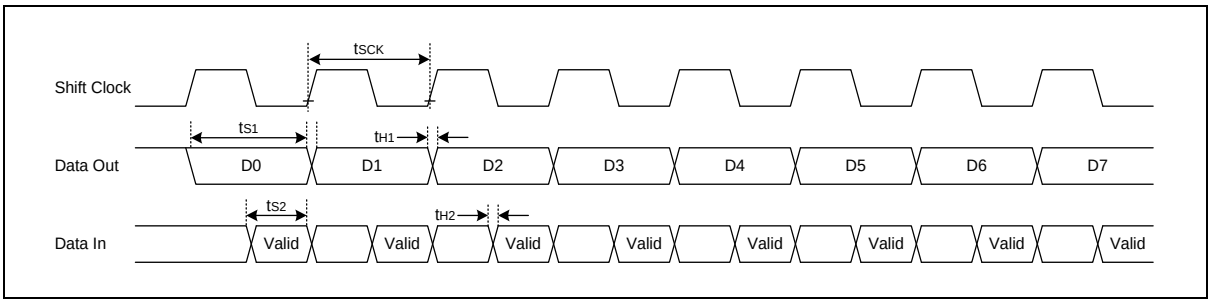


Figure 47. Timing Waveform of UART Module

17.16 Data retention voltage in Stop mode

Table 37. Data Retention Voltage in Stop Mode

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data retention supply voltage	V_{DDDR}	–	1.65	–	3.6	V
Data retention supply current	I_{DDDR}	• V_{DDDR} = 1.65V (T_A=25°C) • Deep sleep mode	–	–	1	µA

17.17 Internal flash characteristics

Table 38. Internal Flash Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Page write time	t_{FSW}	–		–	3.0	3.5	ms
Page erase time	t_{FSE}	–		–	3.0	3.5	
Chip erase time	t_{FCE}	–		–	3.0	3.5	
Flash program voltage	V_{PGM}	On erase/write		2.0	–	3.6	V
System clock frequency	f_{HCLK}	–		2.0	–	–	MHz
Endurance of Write/Erase	NF_{WE}	• Page 0 to 511 • Configure Option Page 1	T_A=25 °C, Page unit	10,000	–	–	Cycles
		Configure Option Page 2/3		100,000			
Retention time	t_{RT}			10	–	–	Years

17.18 Input/ output capacitance

Table 39. Input/ Output Capacitance

(VDD = 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input capacitance	C_{IN}	• f=1MHz • Unmeasured pins are connected VSS	–	–	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

17.19 Main oscillator characteristics

Table 40. Main Oscillator Characteristics

(VDD = 2.2V to 3.6V)

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Crystal	Main oscillation frequency	2.7 V to 3.6 V	2.0	–	16.0	MHz
Ceramic Oscillator	Main oscillation frequency	2.2 V to 3.6 V	2.0	–	4.2	
		2.7 V to 3.6 V	2.0	–	16.0	
External Clock	XIN input frequency	3.0 V to 3.6 V	2.0	–	32.0	MHz
	External Clock Duty Ratio	–	45	50	55	%

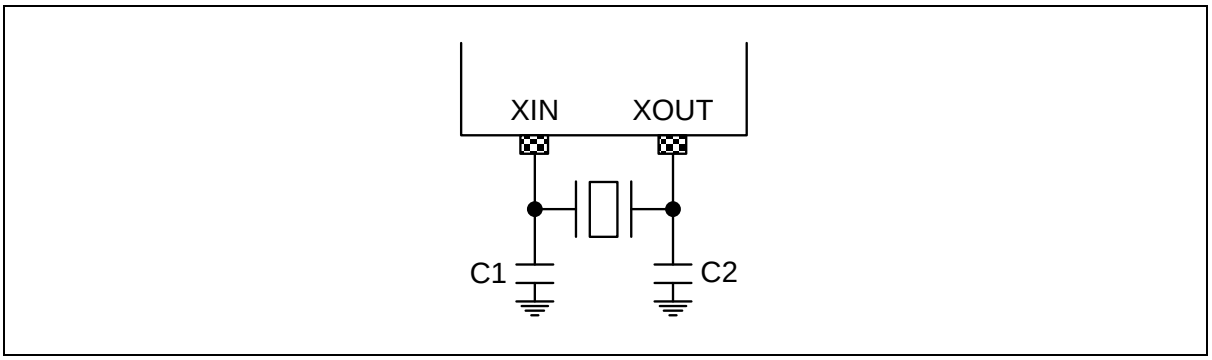


Figure 48. Crystal/Ceramic Oscillator

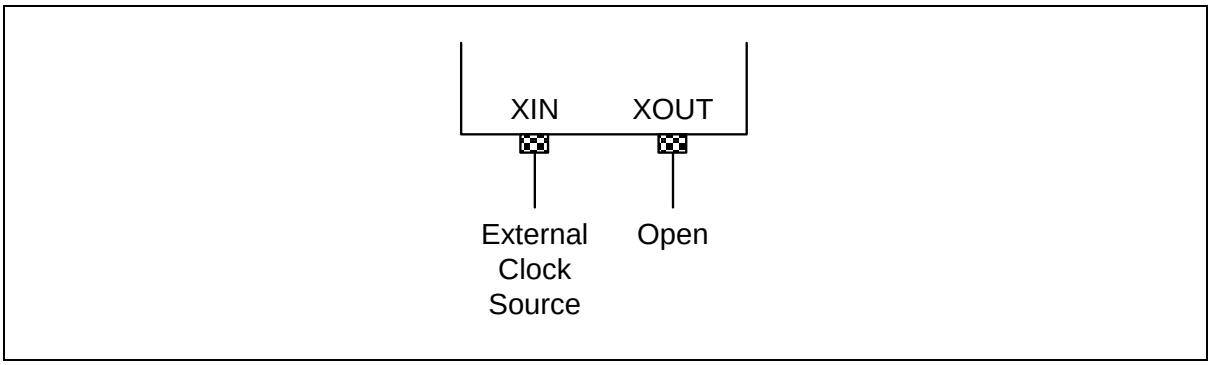


Figure 49. External Clock

17.20 Sub-oscillator characteristics

Table 41. Sub-oscillator Characteristics

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Crystal	Sub oscillation frequency	1.65 V to 3.6 V	32	32.768	38	kHz

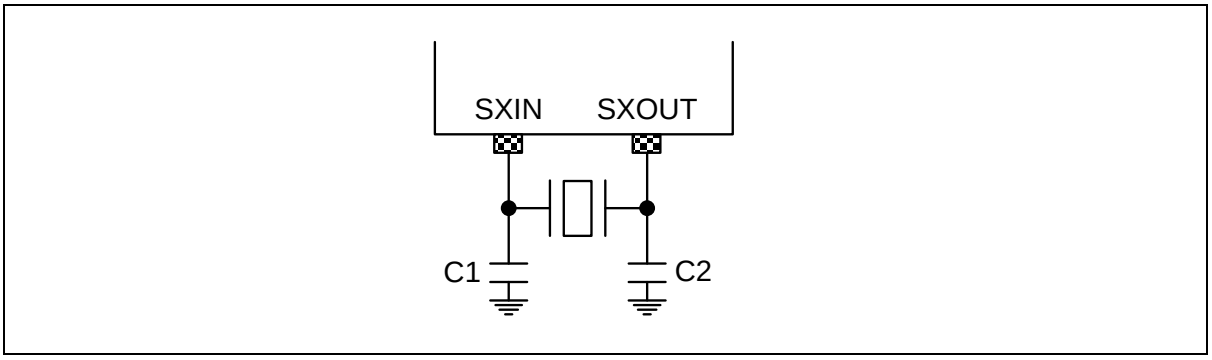


Figure 50. Crystal Oscillator

17.21 Main oscillation stabilization time

Table 42. Main Oscillation Stabilization Time

(VDD = 2.2V to 3.6V)

Oscillator	Conditions		Min	Typ	Max	Units
Crystal	• f_{XIN} ≥ 2 MHz	VDD = 2.7V to 3.6V	–	–	60	ms
Ceramic	• Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	VDD = 2.2V to 3.6V	–	–	10	
external clock	• f_{XIN} = 2.0 to 32 MHz • XIN input high and low width (t_{XL}, t_{XH})		12.5	–	250	ns

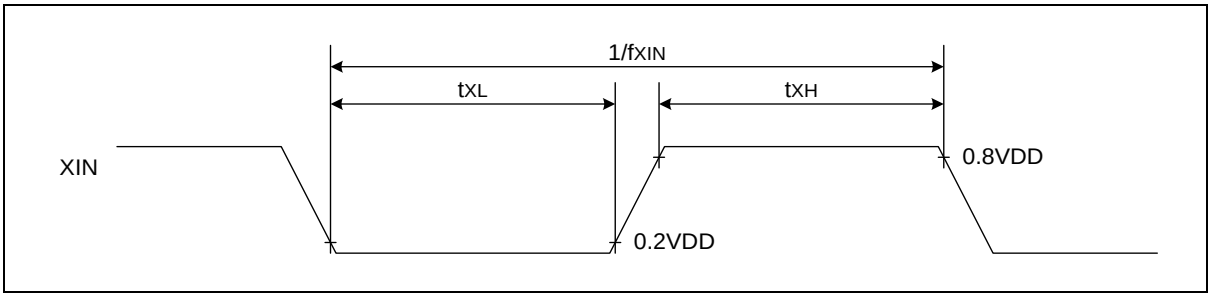


Figure 51. Clock Timing Measurement at XIN

17.22 Sub-oscillation stabilization time

Table 43. Sub-oscillation Stabilization Time

Oscillator	Conditions	Min	Typ.	Max	Units
Crystal	–	–	–	10	sec
	VDD=3V, T_A=25 °C, ISET_I[2:0] = 0x7	–	0.7	1.5	
External clock	SXIN input high and low width (t_{XL}, t_{XH})	5	–	15	µs

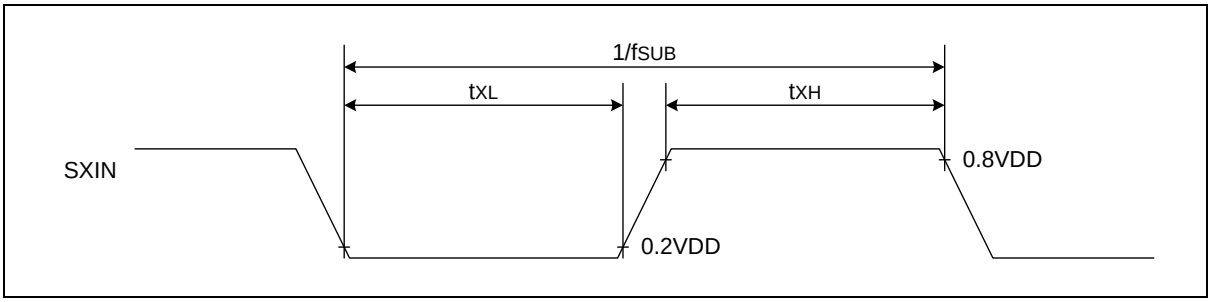


Figure 52. Clock Timing Measurement at SXIN

17.23 Operating voltage range

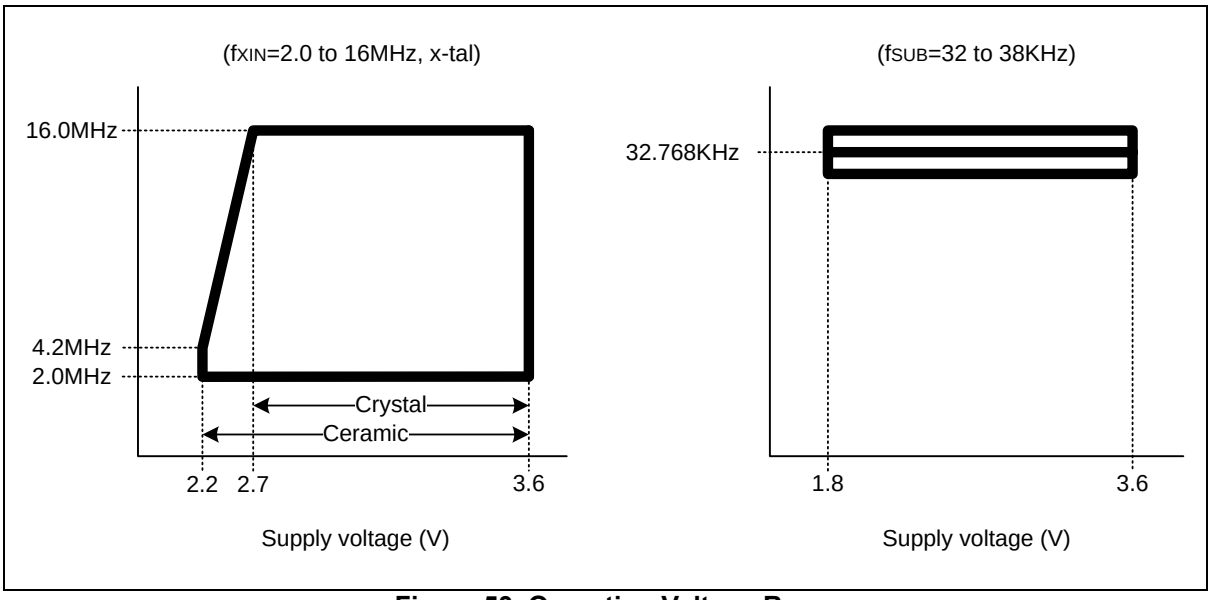


Figure 53. Operating Voltage Range

17.24 Recommended circuit and layout

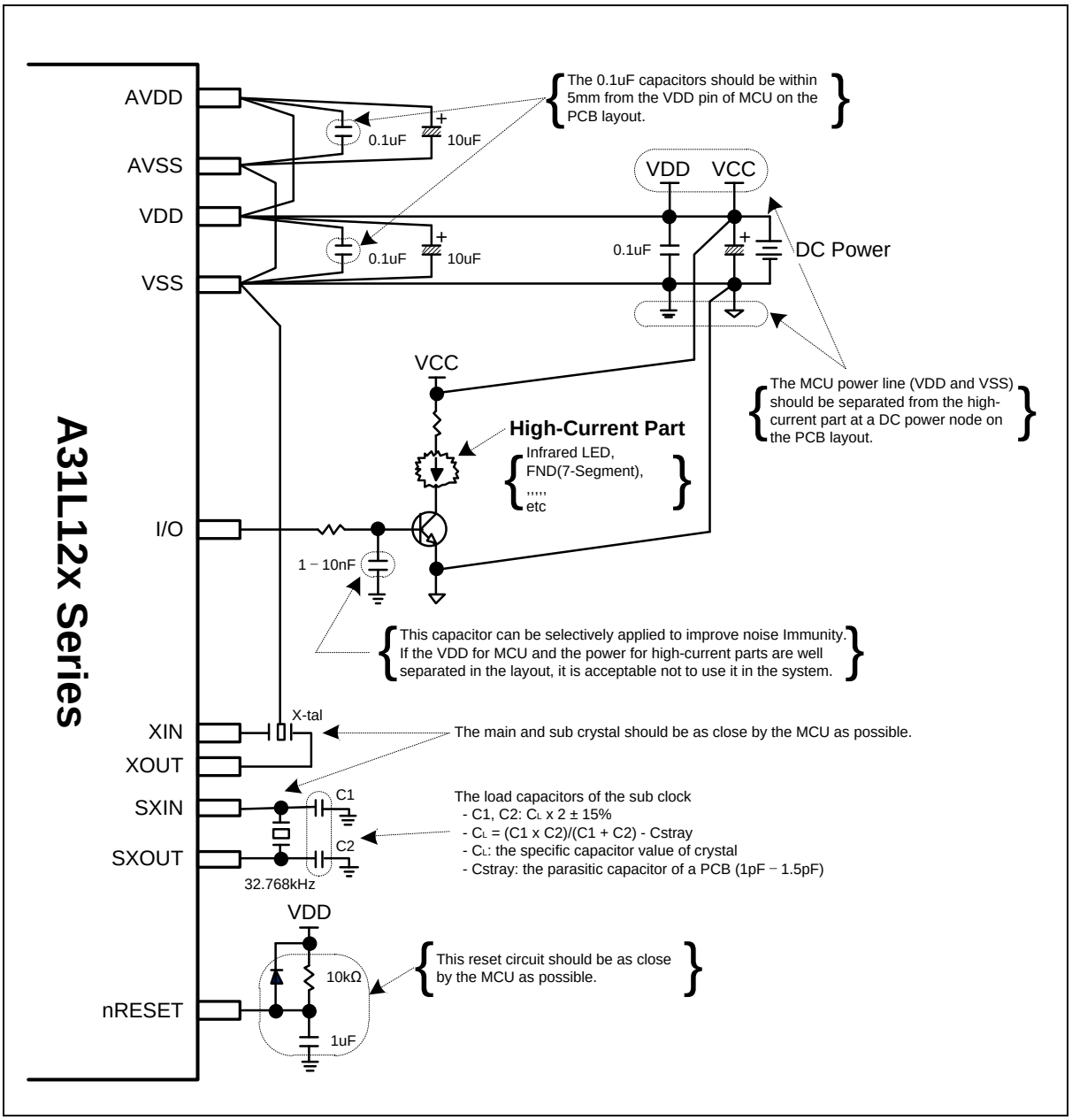
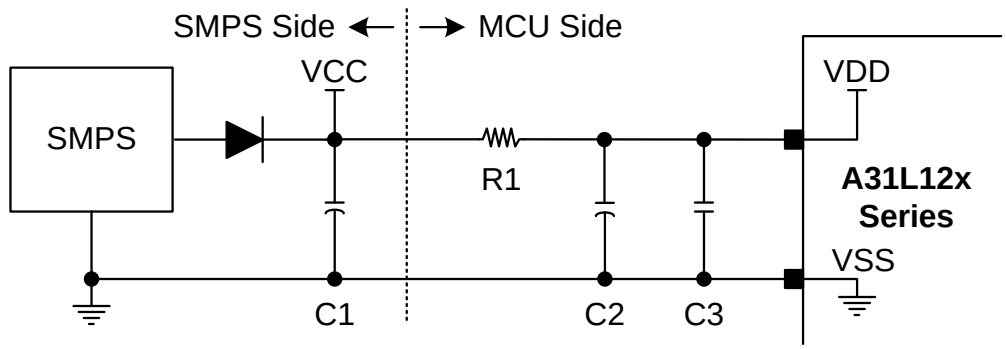


Figure 54. Recommended Circuit and Layout



NOTES:

1. Capacitor C1 is to flatten out the voltage of the SMPS power, VCC.
   - Recommended C1: 470uF/25V more
2. Resistor R1 and capacitor C2 are the RC filter for VDD and suppress the ripple of VCC.
   - Recommended R1: 10Ω - 20Ω
   - Recommended C2: 47uF/25V more
   - The R1 and C2 should be as close by the C3 as possible.
3. Capacitor C3 is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   - Recommended C3: ceramic capacitor 2.2uF more.
   - C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc.) when the SMPS supplies the VDD of MCU.

Figure 55. Recommended Circuit and Layout with SMPS Power

18 Package information

18.1 64 LQFP package information

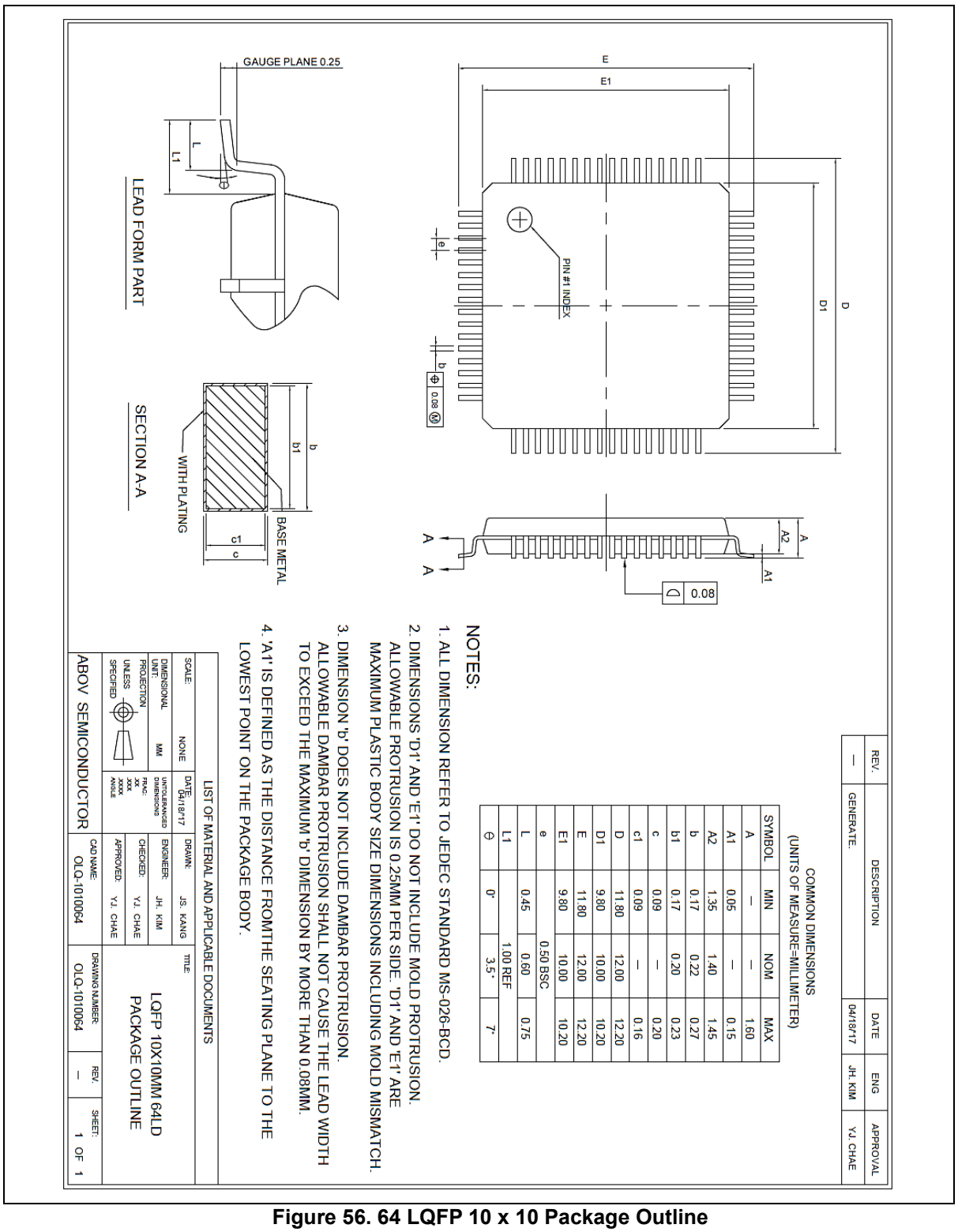
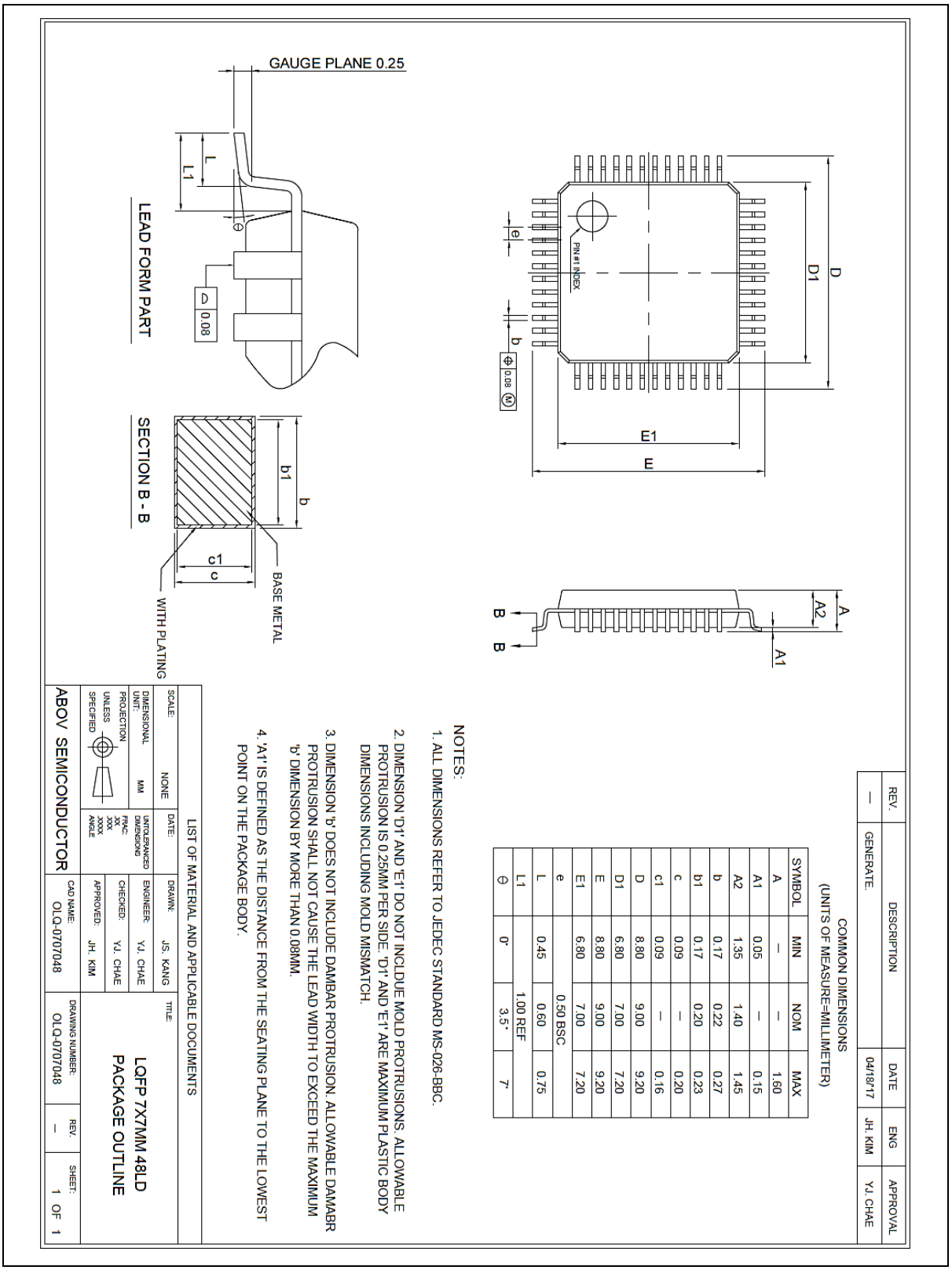


Figure 56. 64 LQFP 10 x 10 Package Outline

18.2 48 LQFP package information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BBC.
2. DIMENSION 'D1' AND 'E1' DO NOT INCLDUE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMABR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/18/17	JH. KIM	YJ. CHAE

SCALE: NONE	DATE:	DRAWN: JS. KANG	TITLE: LQFP 7X7MM 48LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: YJ. CHAE	
PROJECTION	FRAC: ± XX ± .XXX .XXXX ANGLE	CHECKED: YJ. CHAE	
UNLESS SPECIFIED		APPROVED: JH. KIM	
ABOV SEMICONDUCTOR	CAD NAME: OLQ-0707048	DRAWING NUMBER: OLQ-0707048	REV: —
			SHEET: 1 OF 1

Figure 57. 48 LQFP 07 x 07 Package Outline

18.3 32 LQFP package information

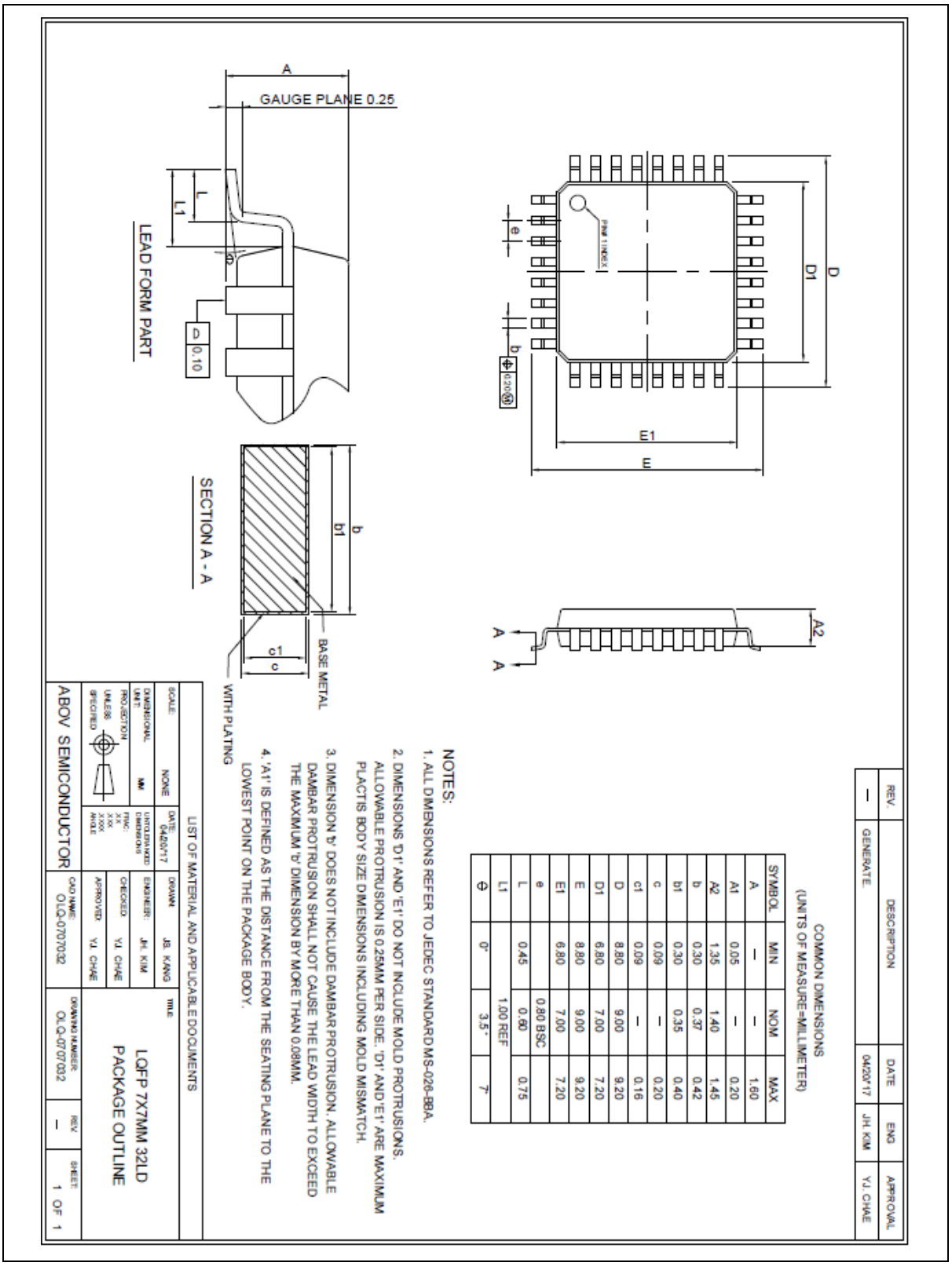


Figure 58. 32 LQFP 07 x 07 Package Outline

18.4 32 QFN package information

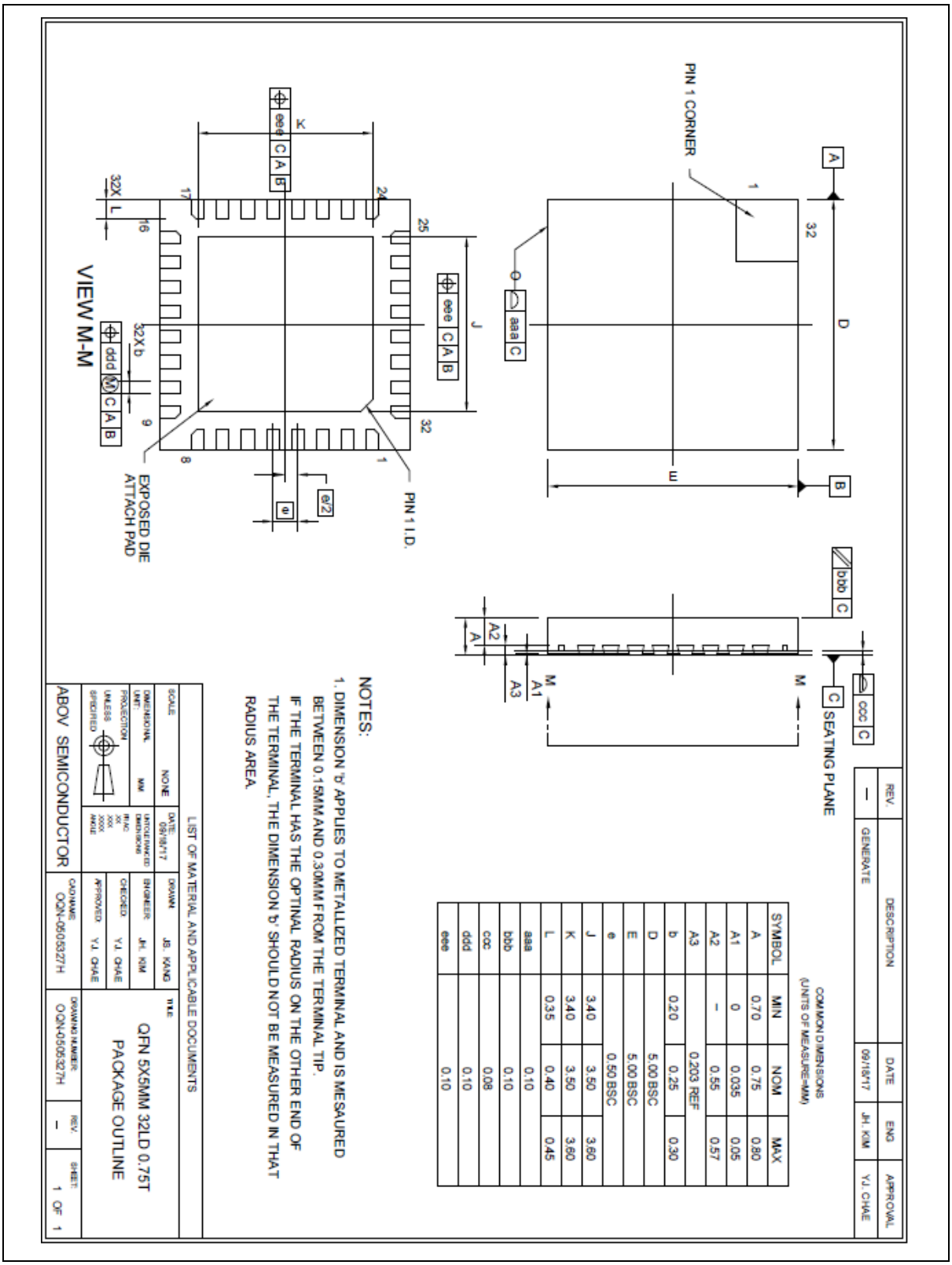


Figure 59. 32 QFN 05 x 05 Package Outline

18.5 28 TSSOP package information

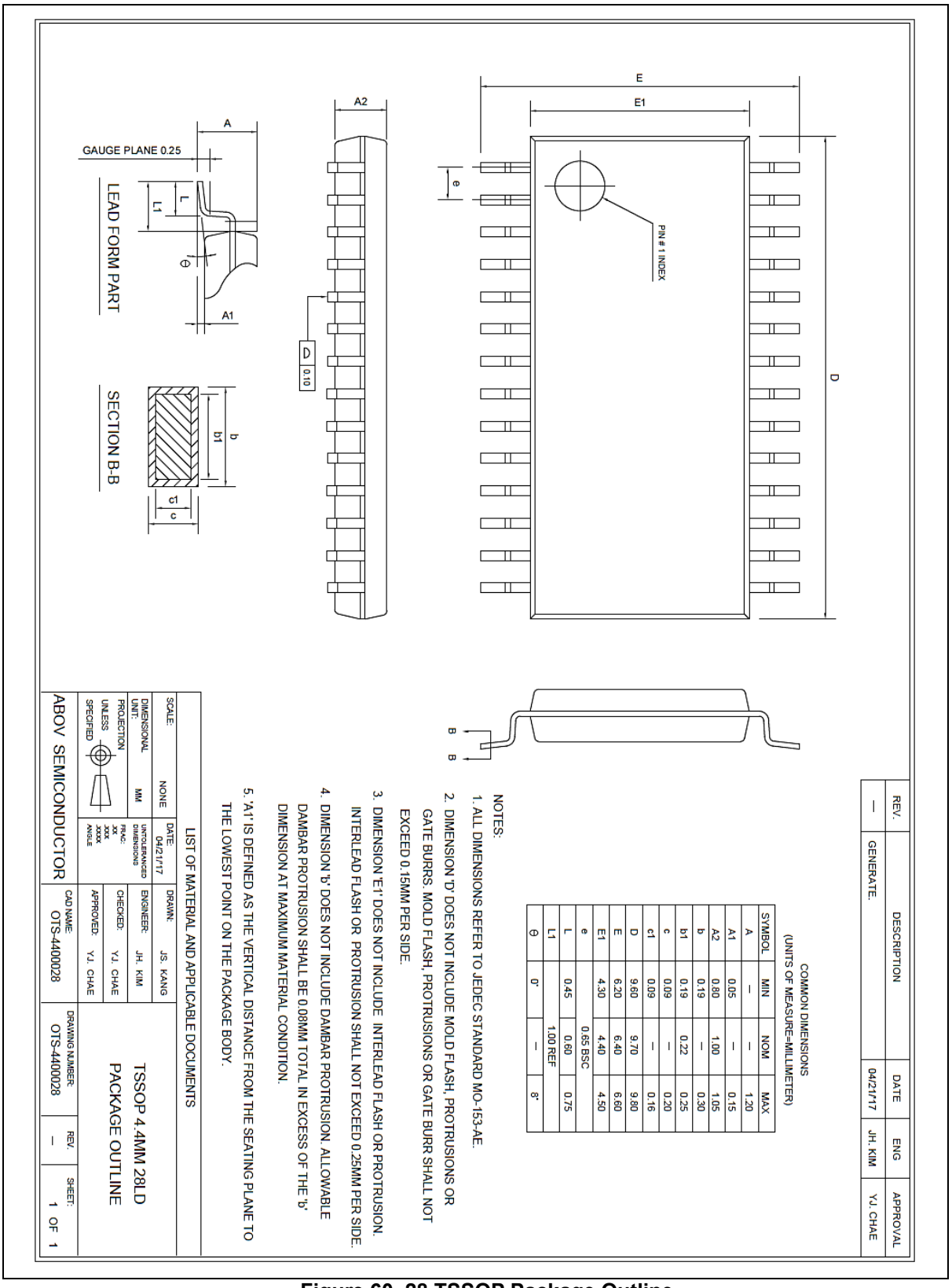


Figure 60. 28 TSSOP Package Outline

18.6 24 QFN package information

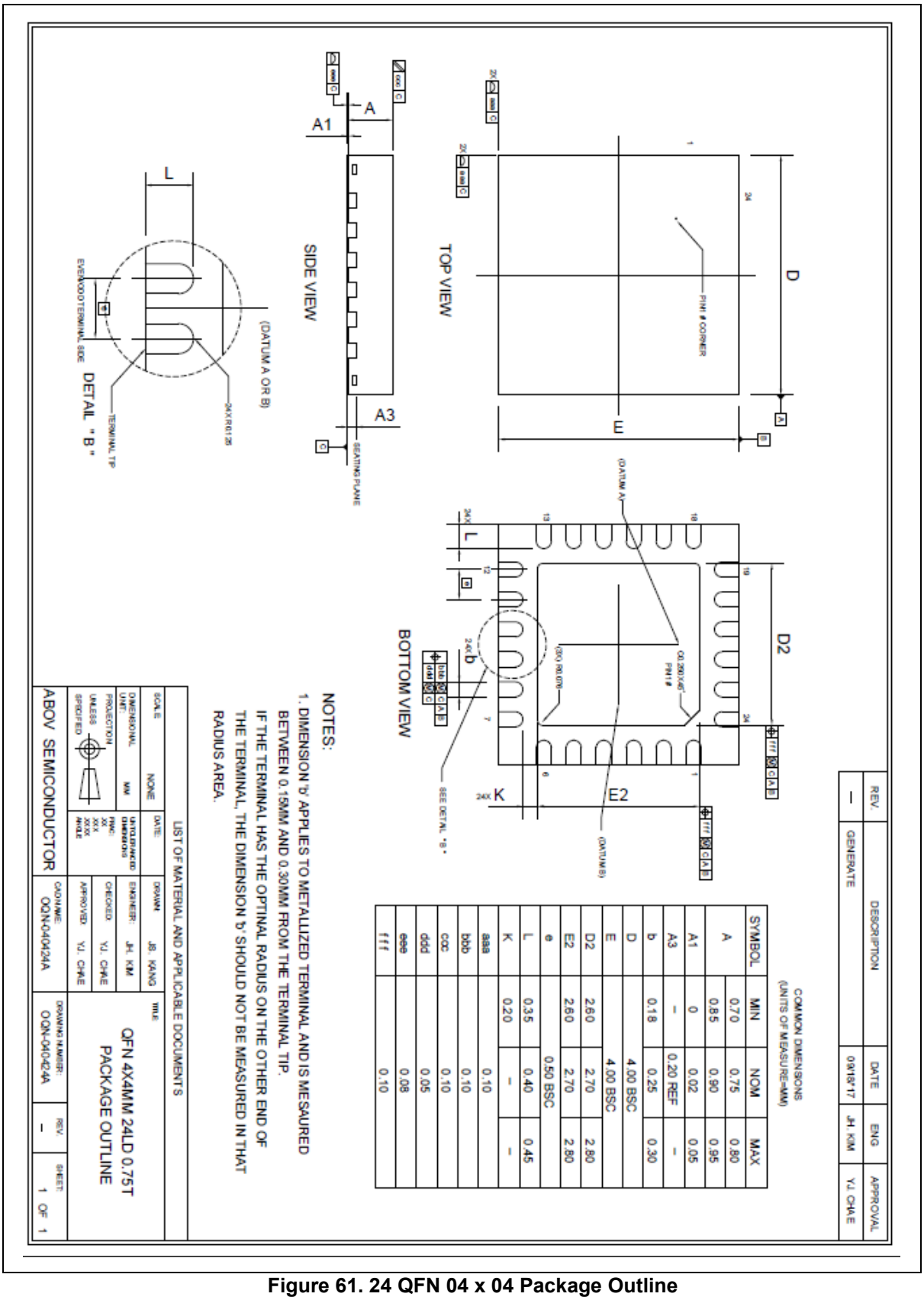


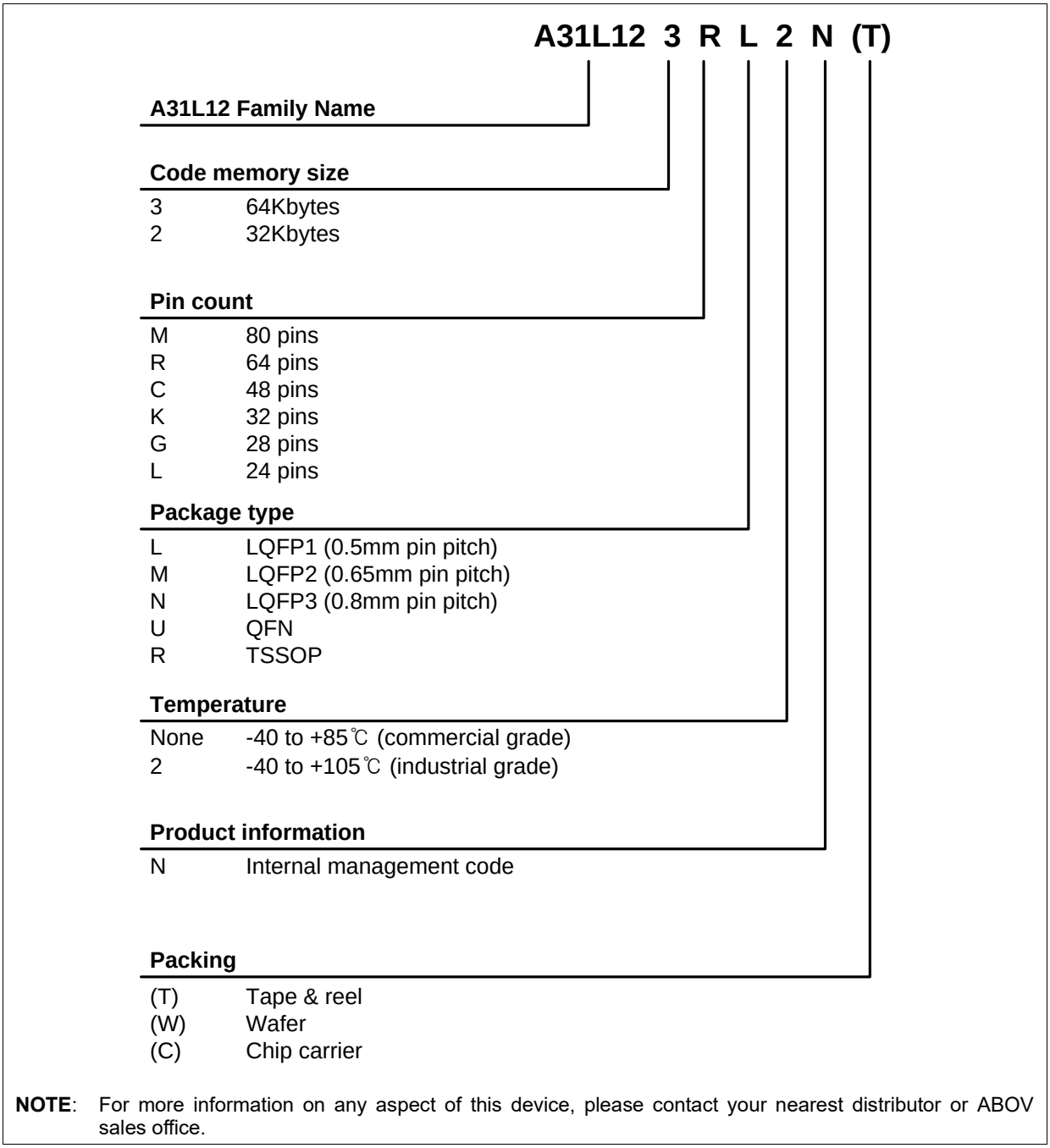
Figure 61. 24 QFN 04 x 04 Package Outline

19 Ordering information

Table 44. A31L12x Series Ordering Information

Part Number	Flash	SRAM	USART	UART	LPUART	SC	I2C	SPI	TIMER	ADC	I/O	Package
A31L123RL	64KB	8KB	1	2	1	2	2	2	5	16ch	52	64LQFP-1010
A31L123CL*	64KB	8KB	1	2	1	2	2	1	5	10ch	38	48LQFP-0707
A31L123KN*	64KB	8KB	1	2	0	2	1	1	5	10ch	26	32LQFP-0707
A31L123KU*	64KB	8KB	1	2	0	2	1	1	5	10ch	28	32QFN-0505
A31L123GR*	64KB	8KB	1	1	0	1	1	1	4	9ch	24	28TSSOP
A31L123LU*	64KB	8KB	1	1	0	0	1	1	4	9ch	20	24QFN
A31L122RL*	32KB	8KB	1	2	1	2	2	2	5	16ch	52	64LQFP-1010
A31L122CL*	32KB	8KB	1	2	1	2	2	1	5	10ch	38	48LQFP-0707
A31L122KN*	32KB	8KB	1	2	0	2	1	1	5	10ch	26	32LQFP-0707
A31L122KU*	32KB	8KB	1	2	0	2	1	1	5	10ch	28	32QFN-0505
A31L122GR*	32KB	8KB	1	1	0	1	1	1	4	9ch	24	28TSSOP
A31L122LU*	32KB	8KB	1	1	0	0	1	1	4	9ch	20	24QFN

* For available options or further information on the devices with "*" marks, please contact the ABOV Sales Office.



NOTE: For more information on any aspect of this device, please contact your nearest distributor or ABOV sales office.

Figure 62. A31L12x Series Numbering Nomenclature

Revision history

Date	Version	Description
Feb.4, 2020	1.00	1st creation
Jul.2, 2020	1.10	Add a IDD1 8MHz condition in chapter 17.11 Supply current characteristics.
Dec.1, 2020	1.20	Add a note about using WFI/WFE Instruction. Fix condition about sub OSC feedback resistor (RX2), "Chapter 17.10 DC electrical characteristics". Remove a item about "sub external clock", "Chapter 17.20 Sub-oscillator characteristics". Remove a 'XTFLSR register'. Add a note about disabling "clock monitoring function", "Chapter 5.6.19 SCU_CMONCR", clock monitoring control register in the user's manual. Add a note about USTnEN bit, "Chapter 14.3.2 USARTn_CR2", USARTn control register 2 in the user's manual. Add a note about SPInEN bit, "Chapter 18.3.1.1 SPIn_CR", SPIn control register in the user's manual.
Mar.2, 2021	1.21	Add contents about RTCC time error correction in the user's manual. Add a note about RXEn bit, "Chapter 19.3.1 SCn_CR1: SCn control register 1" in the user's manual. Add a note about TRERIFGn bit, "Chapter 22.2.2 DMACHn_IESR: DMA channel n interrupt enable and status register" in the user's manual. Add a note about ADATA bits, "Chapter 12.3.4 ADC_DR: A/D converter data register" in the user's manual. Typos modify.
Jul.5, 2022	1.22	Add a note about WUTIFLAG bit, "Chapter 5.6.10 SCU_WUTCR: wake-up timer control register" in the user's manual. Add a note about Timer 50's wake-up source, "Figure 28. Timer Counter 50 Block Diagram". Typos modify.
Oct.24, 2022	1.30	Change the document format.
Nov.18, 2022	1.40	Add TSSOP28, QFN24 Packages.
Dec.2, 2024	1.50	Updated the disclaimer.

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