A31xxxx Errata Sheet

Disabling clock monitoring

ET Rev. 2.01

Introduction

This errata sheet introduces a method to disable 'clock monitoring' function safely. If the 'clock monitoring' function is disabled in an inappropriate method, the MCU device may malfunction. It is important that the 'clock monitoring' function is disabled in the correct order.

This document describes the correct sequence of disabling the 'clock monitoring' function and introduces the example code corresponding to the sequence.

Table 1 summarizes the limitations.

Table 1. Limitation summary

Module	Limitations	
SCU	Depending on the procedure to disable the clock monitoring function, the MCU may malfunction.	

Table 2 shows the list of MCU devices to which this document applies.

Table 2. Device limitations

Reference product	Part name
A31G11x	A31G111GR, A31G111KN, A31G111KU, A31G111LU, A31G112CL, A31G112GR, A31G112KN, A31G112KU, A31G112KY, A31G112LU, A31G112SQ
A31G12x	A31G122ML, A31G122MM, A31G122RL, A31G122RM, A31G123CL, A31G123ML, A31G123MM, A31G123RL, A31G123RM, A31G123RN, A31G123SQ
-	A31R713CL, A31R713ML, A31R713RT
A31L12x	A31L122CL, A31L122KN, A31L122KU, A31L122RL, A31L123CL, A31L123KN, A31L123KU, A31L123RL

Contents A31xxxx Errata Sheet

Contents

Intro	ductio'	n	1
1. Disabl		ling clock monitoring	
		Description of limitation	
	1.2	Workaround	4
Rev	ision h	istory	5



A31xxxx Errata Sheet List of tables

List of tables

Table 1. Limitation summary	•
Table 2. Device limitations	•
Table 3. The sequence of disabling clock monitoring	4



1. Disabling clock monitoring

1.1 Description of limitation

The 'clock monitoring' function is disabled by default. Users want to enable or disable the 'clock monitoring' function depending on the individual applications, and they may change the settings.

If the 'clock monitoring' function is enabled by setting the MACTS[1:0] bits to '10', disabling this function by writing '0b' to the MONEN bit in SCU CMONCR register may cause the device to malfunction.

1.2 Workaround

It is recommended to clear the MACTS[1:0] bits in SCU_CMONCR register to '00', before disabling the 'clock monitoring' function.

Table 3 describes the procedure for disabling the 'clock monitoring' function.

Table 3. Sequence of disabling clock monitoring

Step	Description	
1	Clear the MACTS[1:0] bits in SCU_CMONCR register to '00'.	
	No action by the 'clock monitoring' function	
	- Flags will be set/cleared on condition.	
2	Clear the MONEN bit in SCU_CMONCR register to '0'.	
	- The 'clock monitoring' function is disabled.	

The example code shown below disables the 'clock monitoring' function sequentially:

```
SCUCG->CMONCR_b.MACTS = 0;  // 1. Clear MACTS bits
SCUCG->CMONCR_b.MONEN = 0;  // 2. Disable clock monitoring function
```

- 1. It clears the MACTS bits in SCU_CMONCR register to '00b'.
- 2. It disables the 'clock monitoring' function.



A31xxxx Errata Sheet Revision history

Revision history

Revision	Date	Notes
1.00	Nov. 27, 2020	Initial release
2.00	Apr. 14, 2023	Made major changes due to standardization of content structure and document template. Changed the file name (From 'ERRATA_A31G11x_A31G12x_A31R713_A31L12x_ENG_201127').
2.01	Dec. 2, 2024	Updated the disclaimer.



Important notice A31xxxx Errata Sheet

Korea

Regional Office, Seoul R&D, Marketing & Sales 8th Fl., 330, Yeongdong-daero, Gangnam-gu, Seoul, 06177, Korea

Tel: +82-2-2193-2200 Fax: +82-2-508-6903 www.abovsemi.com

Domestic Sales Manager

Tel: +82-2-2193-2206 Fax: +82-2-508-6903 Email: <u>sales_kr@abov.co.kr</u> HQ, Ochang

R&D, QA, and Test Center 93, Gangni 1-gil, Ochang-eup, Cheongwon-gun, Chungcheongbuk-do,28126, Korea

Tel: +82-43-219-5200 Fax: +82-43-217-3534 www.abovsemi.com

Global Sales Manager Tel: +82-2-2193-2281 Fax: +82-2-508-6903 Email: sales gl@abov.co.kr China Sales Manager
Tel: +86-755-8287-2205
Fax: +86-755-8287-2204
Email: sales cn@abov.co.kr

ABOV Disclaimer

IMPORTANT NOTICE - PLEASE READ CAREFULLY

ABOV Semiconductor ("ABOV") reserves the right to make changes, corrections, enhancements, modifications, and improvements to ABOV products and/or to this document at any time without notice. ABOV DOES NOT GIVE WARRANTIES AS TO THE ACCURACY OR COMPLETENESS OF THE INFORMATION INCLUDED HEREIN. Purchasers should obtain the latest relevant information of ABOV products before placing orders. Purchasers are entirely responsible for the choice, selection, and use of ABOV products and ABOV assumes no liability for application assistance or the design of purchasers' products. NO LICENSE, EXPRESS OR IMPLIED, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY ABOV HEREIN. ABOV DISCLAIMES ALL EXPRESS AND IMPLIED WARRANTIES AND SHALL NOT BE RESPONSIBLE OR LIABLE FOR ANY INJURES OR DAMAGES RELATED TO USE OF ABOV PRODUCTS IN SUCH UNAUTHORIZED APPLICATIONS. ABOV and the ABOV logo are trademarks of ABOV. For additional information about ABOV trademarks, please refer to https://www.abov.co.kr/en/about/corporate identity.php. All other product or service names are the property of their respective owners. Information in this document supersedes and replaces the information previously supplied in any former versions of this document.

© 2020 ABOV Semiconductor - All rights reserved

