A31L12x

How to Wake up with LPUART

Application Note

Version 1.02

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1 Introduction

A31L12x microcontroller has a low power universal asynchronous receiver transmitter (LPUART) that can properly receive data even when the MCU is in deep sleep mode. The LPUART can wake up the MCU from deep sleep mode only when XSOSC is selected for the LPUART clock and the system clock is configured to HIRC or XMOSC. If the system clock is XMOSC, users need to pay attention to the stabilization time of the XMOSC.

Wake-up sources of the LPUART are as follows:

- Receive character detection: when the data in the LPUART_RCDR register matches the data received without error.
- Start bit detection: when a start bit is detected in deep sleep mode.
- Receive data register not empty: when there is data received.

In this document, users can learn how to wake up the A31L12x from deep sleep mode through the A31L12x's LPUART. Example code is presented to help users understand.

2 How to Wake up from Deep Sleep Mode

To use the LPUART as a wake-up source, corresponding register bits must be set as below:

- SCU_PPCLKSR.LPUTCLK[1:0] = “10b”: It selects the XSOSC (32.768kHz) as the LPUART clock.
- LPUART_CR1.OVRS[1:0] = “10b”: It selects no oversampling (Only 1 sampling).
- LPUART_CR1.WAKEN = “1b”: It enables wake-up function in deep sleep mode. This bit must be set to “1b” just before entering deep sleep mode and be cleared to “0b” immediately after the wake-up.

2.1 Wake-up Method 1 by Receive Character Detection

The receive character detection function is activated by setting the LPUART_CR2.RCDEN bit to “1b”. The low power UART block has the receive character detection data register, LPUART_RCDR, to detect whether a specific character such as an address has been entered.

The LPUART_IFSR.RCDIFLAG bit is set to “1b” when a character in the LPUART_RCDR register matches a character received without errors in frame and parity. This flag can be used as an interrupt source and as a wake-up source in deep sleep mode.

If the system clock is XMOSC, sufficient x-tal stabilization time before the next reception must be given.

Figure 1 shows an example timing diagram of the wake-up by receive character detection.

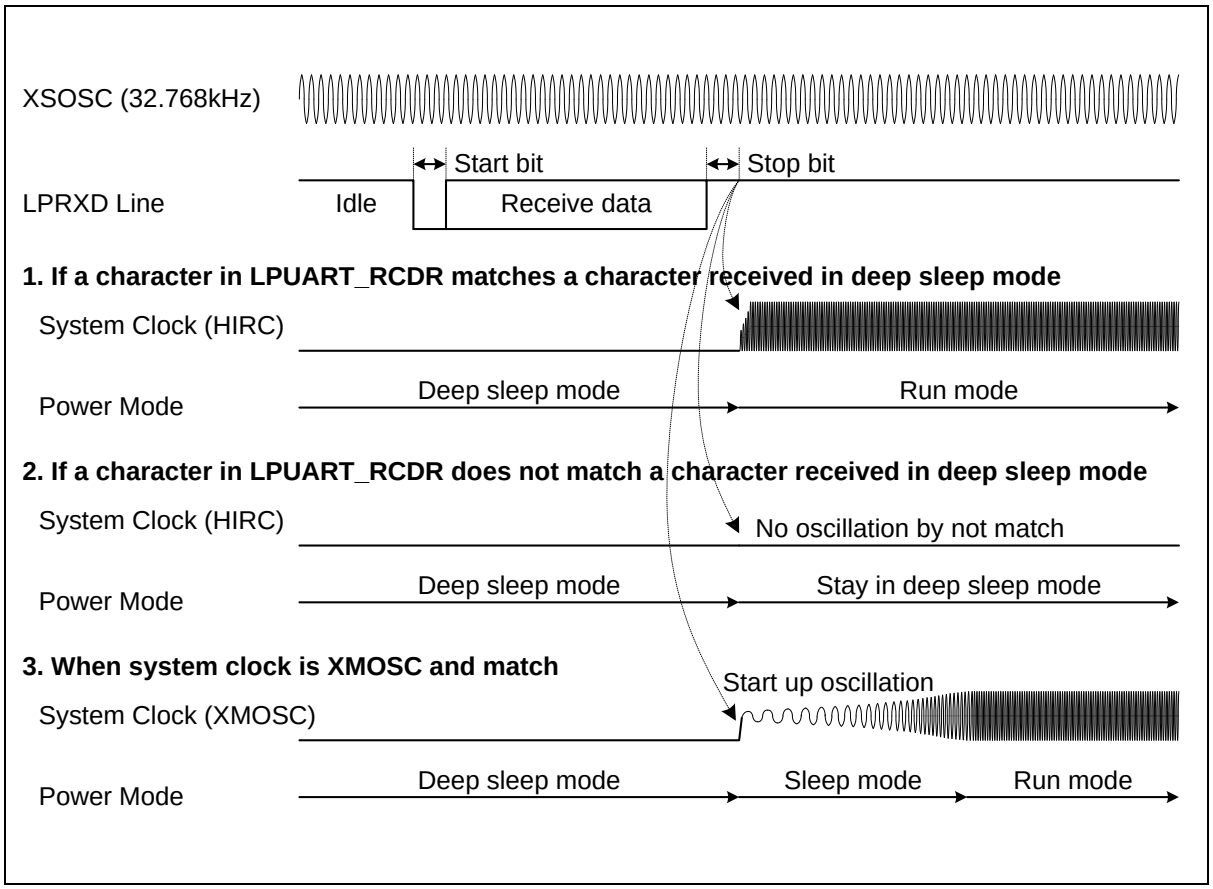

Figure 1. Wake-up by Receive Character Detection

2.2 Wake-up Method 2 by Start Bit Detection

The LPUART_IFSR.SBDIFLAG bit is set to “1b” when a valid start bit is detected in deep sleep mode. This flag can be used as a wake-up source only in deep sleep mode.

Figure 2 shows an example timing diagram of the wake-up by start bit detection in deep sleep mode.

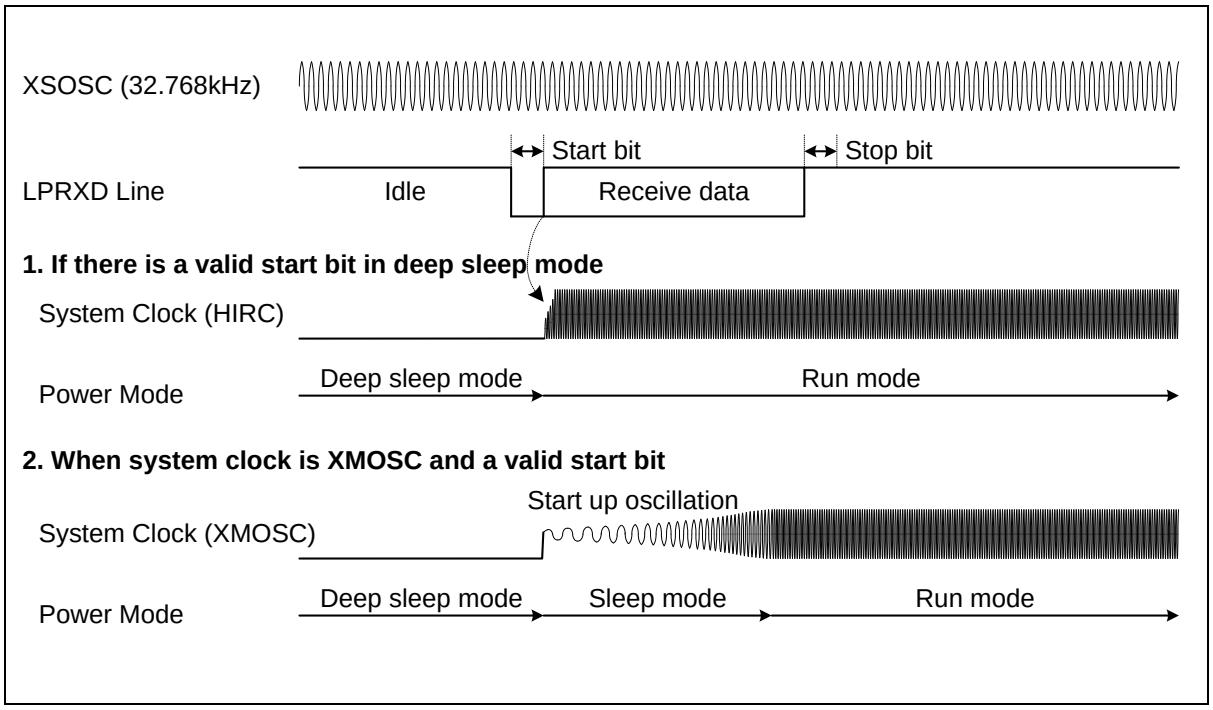

Figure 2. Wake-up by Valid Start Bit Detection

2.3 Wake-up Method 3 by Arbitrary Data Received

The LPUART_IFSR.RXCIFLAG bit is set to “1b” when new data is received while the receive data register is empty. This flag can be used as a wake-up source in deep sleep mode.

Figure 3 shows an example timing diagram of the wake-up by arbitrary data in deep sleep mode.

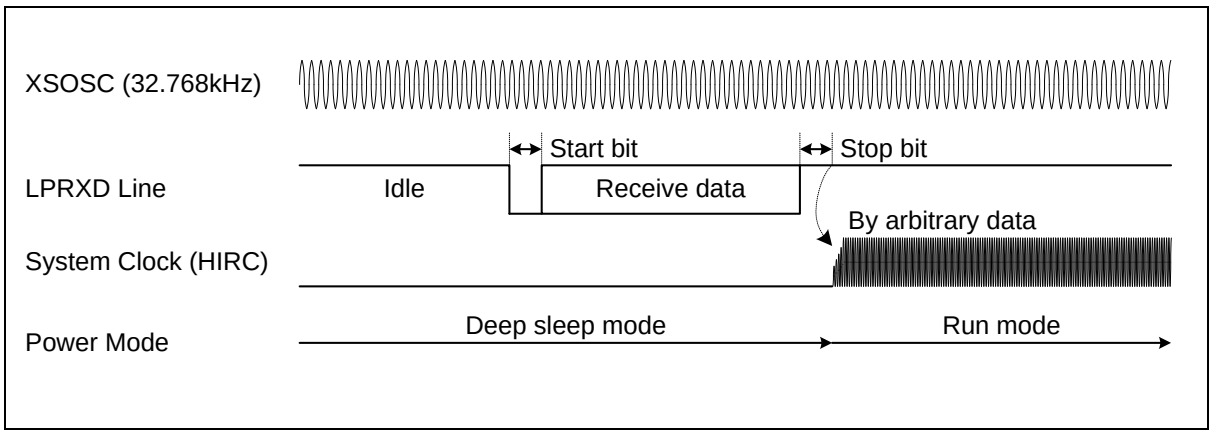

Figure 3. Wake-up by Arbitrary Data Received

3 Baud Rate and Compensation

The LPUART has a baud rate generation register (LPUART_BDR) and a baud rate compensation register (LPUART_BCMP). When the XSOSC (32.768kHz) is used as an LPUART clock source, the baud rate can be up to 9600 bps.

3.1 LPUART Baud Rate Generation Register

Table 1 describes the low power UART baud rate generation register (LPUART_BDR).

Table 1. Description of LPUART Baud Rate Generation Register

LPUART_BDR Address: 0x4000_5C20

Bits	[31:16]	[15:0]
Name	Reserved	BDATA
Reset Value	0x0000	0xFFFF

15 0	BDATA	These bits are used to generate baud rate. 16 oversampling: • Baud Rate = fLPUART/{16 x (BDATA[15:0] +1)} • BDATA[15:0] range: 0x0 to 0xFFFF 8 oversampling: • Baud Rate = fLPUART/{8 x (BDATA[15:0] +1)} • BDATA[15:0] range: 0x0 to 0xFFFF No oversampling: This can be used with XSOSC (32.768kHz). • Baud Rate = fLPUART/(BDATA[15:0] +1) • BDATA[15:0] range: 0x2 to 0xFFFF • If this register is 0x0002 on the no oversampling, the LPUART_BCMP[15] bit (BCMPS) shouldn't be set to "1b" for minus compensation.

The following formula calculates the LPUART_BDR value with conditions of no over sampling and f_{LPUART} = 32.768kHz.

LPUART_BDR: f_{LPUART} ÷ ("Baud Rate" x Sampling) – 1 = 32768 ÷ (9600 x 1) -1 ≒ 2.41333

Since the calculation result is 2.41333, the LPUART_BDR value is 2. That is, sampling is performed at the midpoint every 3 f_{LPUART} clocks from a falling edge. The sampling proceeds every 3 clocks as the LPUART_BDR value is 2, but the data of the LPRXD line should be sampled every 3.4 clocks. The received data is different from the actual data due to the difference of 0.4 sampling clock.

Figure 4 shows an example of sampling point error on no over sampling.

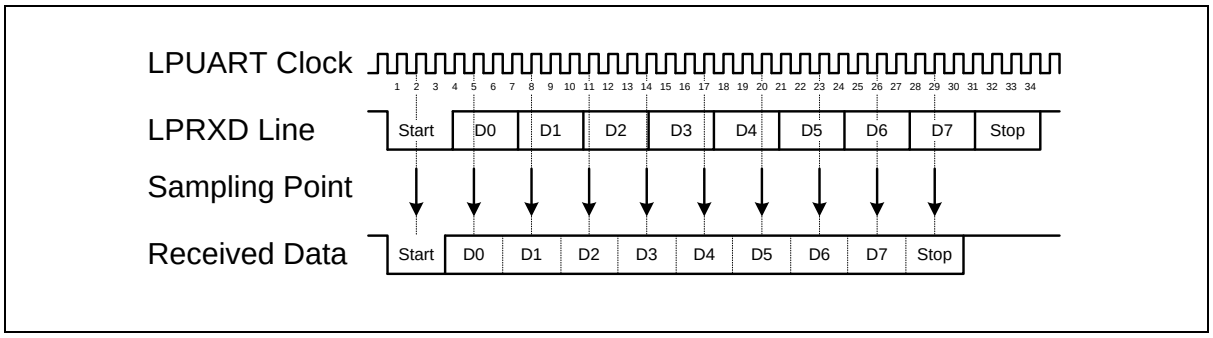

Figure 4. Sampling Point Error on Only 1 Sampling

So, to receive data without error, users need to compensate 0.4 clock. The next section explains how to compensate baud rate clock.

3.2 LPUART Baud Rate Compensation Register

Table 2 describes the low power UART baud rate compensation register (LPUART_BCMP).

Table 2. Description of LPUART Baud Rate Compensation Register

LPUART_BCMP Address: 0x4000_5C24

Bits	[31:16]	[15]	[14:9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	Reserved	BCMPS	Reserved	BCMP8	BCMP7	BCMP6	BCMP5	BCMP4	BCMP3	BCMP2	BCMP1	BCMP0
Reset Value	0x0000	0	0x00	0	0	0	0	0	0	0	0	0

15	BCMPS	Baud Rate Compensation Sign. 0 ➔ Plus 1 clock for compensation 1 ➔ Minus 1 clock for compensation
x	BCMPx	Baud Rate Compensation bits. x: 0 to 8. 0 ➔ No compensation 1 ➔ Clock compensation with sign bit (BCMPS)

The baud rate clock can be adjusted by adding or subtracting 1 LPUART clock using the LPUART_BCMP register. The BCMPS is a sign bit, and if its value is “0b”, 1 LPUART clock is added when sampling the corresponding bit. If the BCMPS is “1b”, the baud rate is subtracted.

The BCMP8 is for parity bit and the BCMP[7:0] bits are for data[7:0].

Table 3 shows an example of baud rate compensation when the LPUART clock is 32.768kHz and baud rate is 9600 bps.

Table 3. Example Baud Rate Compensation

Rx/Tx bit	BCMPx bit	Clock Error before compensation	Compensation bit	Final Clock Error
Start	–	-0.413	x	-0.413
D0	bit 0	-0.827	1	-0.827 + 1 = 0.173
D1	Bit 1	-0.240	0	-0.240
D2	Bit 2	-0.653	1	-0.653 + 1 = 0.347
D3	Bit 3	-0.067	0	-0.067
D4	Bit 4	-0.480	0	-0.480
D5	Bit 5	-0.893	1	-0.893 + 1 = 0.107
D6	Bit 6	-0.307	0	-0.307
D7	Bit 7	-0.720	1	-0.720 + 1 = 0.280
Parity	Bit 8	-0.133	0	-0.133

In the above table, the LPUART_BCMP.BCMPS bit is cleared to “0b” for plus compensation. The bit is calculated as follows, if the result is positive, it is plus compensation, and if it is negative, it is minus compensation.

“Required Sampling Clock” – “Set Sampling Clock” = 3.413 – 3 = 0.413

Refer to the 16.4.2 A31L12x User’s manual for an example of minus compensation.

Figure 5 shows an example timing diagram of compensation sampling point on no over sampling.

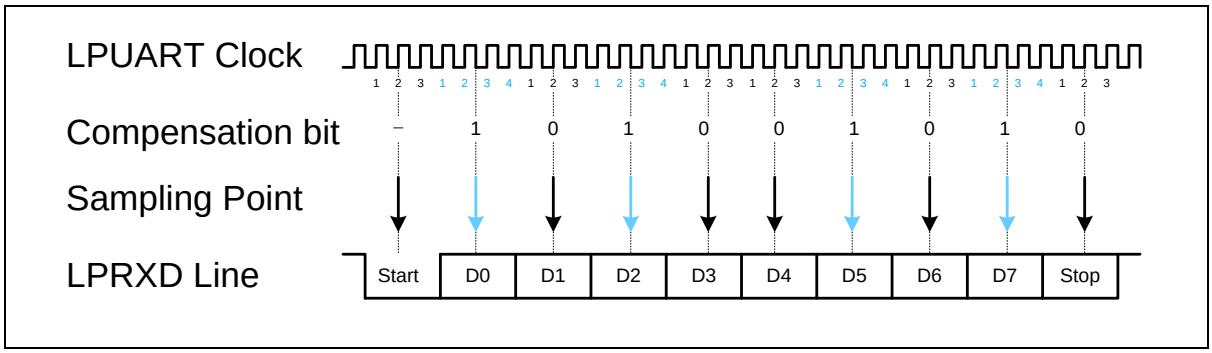

Figure 5. Compensation Sampling Point

As shown in the figure above, data can be received normally after compensating for the sampling point.

4 Programming Tips

Chapter 4 introduces programming tips for the wake-up by receive character detection. The following is a list that must be configured to use LPUART as a wake-up source in deep sleep mode. The others are the same as general UART usage.

1. The XSOSC (32.768kHz) should be on oscillation and be selected as the LPUART clock.
2. No oscillation must be selected by oversampling selection bit in the LPUART control register.

```
void SysInit(void) {
        ---------
        SCUCG→CLKSRCR = 0xA5070000|(SCUCG→CLKSRCR|1);  // Enable XSOSC
        SCUCG→PPCLKSR_b.LPUTCLK = 2;                   // LPUART clock: XSOSC
        ---------
}

void LPUARTInit(void) {
        ---------
        LPUART→CR1_b.OVRS = 2;          // No oversampling
        LPUART→BDR = 2;                 // 9,600bps at 32.768kHz, Up to 9,600bps
        LPUART→BCMP = 0x00A5;           // Compensation: plus 0.4clock
        LPUART→CR2_b = 1;               // To enable “Receive Char Detection” function
        ---------
}

void DeepSleep(void) {
        ---------
        LPUART→CR1_b.WAKEN = 1;             // To wake up by LPUART
        HAL_PWR_EnterPowerDownMode();       // Deep sleep mode
        LPUART→CR1_b.WAKEN = 0;             // After wake-up from deep sleep mode
        ---------
}
```

Figure 6. Programming Tip for Wake-up by Receive Character Detection

5 References

- A31L12x User's Manual
- A31L12x Datasheet
- Example Code

Revision History

Version	Date	Description
1.00	21. 3.16	Created first version
1.01	22. 10.28	Modify a font
1.02	24. 12.2	Updated the disclaimer.

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