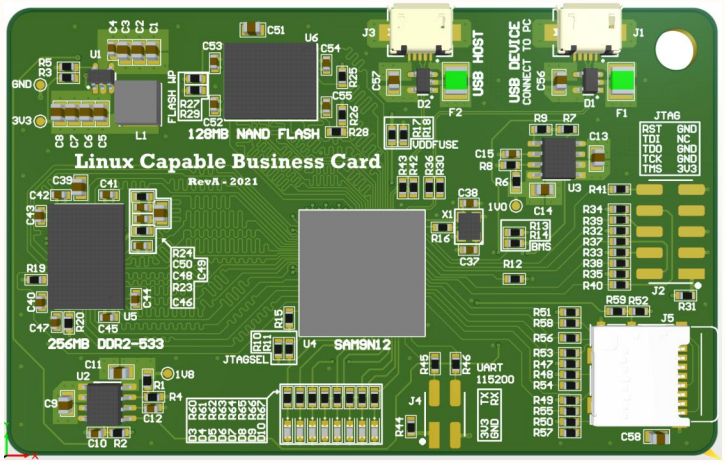
Linux Capable Business Card

Rev A 01/09/2021

TOP VIEW



BOTTOM VIEW

Page	Index
1	COVER PAGE
2	BLOCK DIAGRAM
3	POWER SUPPLIES
4	CPU POWER
5	CPU EBI INTERFACE
6	RAM DDR2
7	NAND FLASH
8	CONNECTORS
9	CPU GPIO

DESIGN CONSIDERATIONS

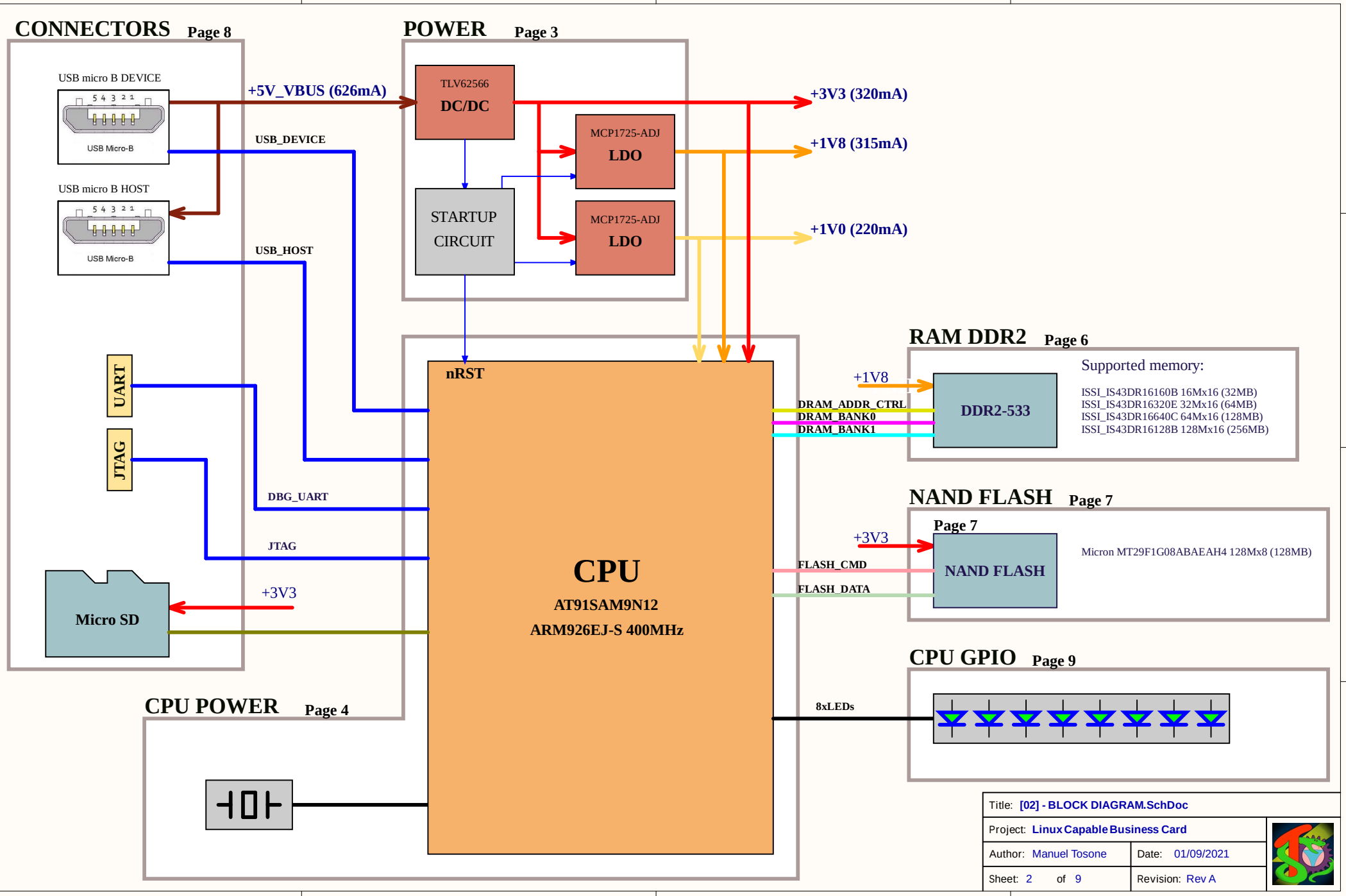
DESIGN NOTE:
Example text for informational design notes .

DEBUG NOTE:
Example text for debug notes.

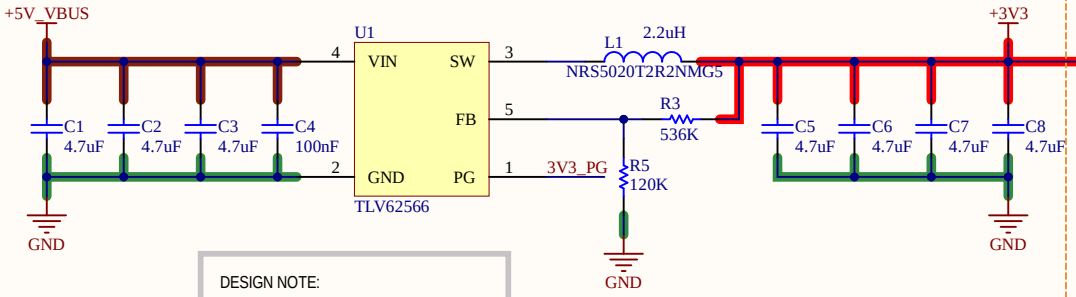
DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

Title: [01] - COVER PAGE.SchDoc	
Project: Linux Capable Business Card	
Author: Manuel Tosone	Date: 01/09/2021
Sheet: 1 of 9	Revision: Rev A


CONNECTORS Page 8
USB micro B DEVICE
USB Micro-B
USB micro B HOST
USB Micro-B
+5V_VBUS (626mA)
USB_DEVICE
USB_HOST
POWER Page 3
TLV62566
DC/DC
STARTUP
CIRCUIT
MCP1725-ADJ
LDO
MCP1725-ADJ
LDO
+3V3 (320mA)
+1V8 (315mA)
+1V0 (220mA)
UART
JTAG
Micro SD
+3V3
DBG_UART
JTAG
nRST
CPU
AT91SAM9N12
ARM926EJ-S 400MHz
RAM DDR2 Page 6
+1V8
DDR2-533
Supported memory:
ISSI_IS43DR16160B 16Mx16 (32MB)
ISSI_IS43DR16320E 32Mx16 (64MB)
ISSI_IS43DR16640C 64Mx16 (128MB)
ISSI_IS43DR16128B 128Mx16 (256MB)
DRAM_ADDR_CTRL
DRAM_BANK0
DRAM_BANK1
NAND FLASH Page 7
Page 7
+3V3
NAND FLASH
Micron MT29F1G08ABAEAH4 128Mx8 (128MB)
FLASH_CMD
FLASH_DATA
CPU GPIO Page 9
8xLEDs
CPU POWER Page 4
Title: [02] - BLOCK DIAGRAM.SchDoc
Project: Linux Capable Business Card
Author: Manuel Tosone
Date: 01/09/2021
Sheet: 2 of 9
Revision: Rev A

DC/DC +3V3



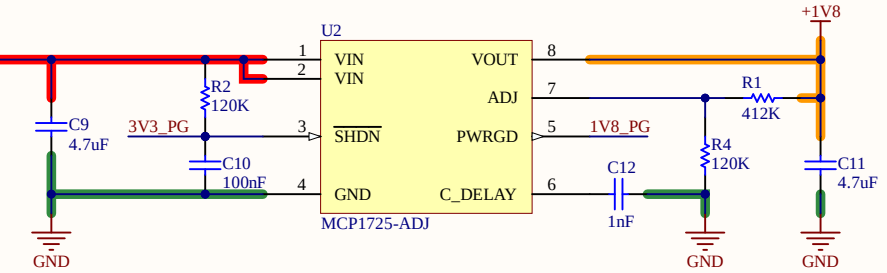
DESIGN NOTE:

Vout = 0.6 * (1+R202/R204) = 3.28V

DESIGN NOTE:

+3V3: Max current = 1.5A
Requred current = 915mA

LDO +1V8



DESIGN NOTE:

Vout = 0.41 * (1+R200/R203) = 1.82V

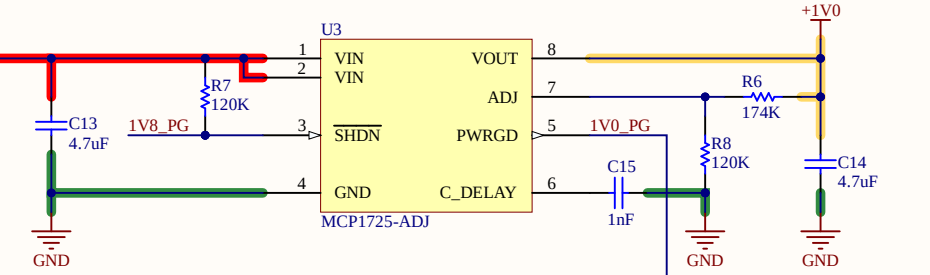
R201 and C209 introduce 7.2mS delay
delay = -R201*C209*ln(1-1.49/3.3)

DESIGN NOTE:

C211 introduces 3mS delay between 1V8 stable and PWRGD

delay = (C211 * 0.42)/0.14

LDO +1V0



DESIGN NOTE:

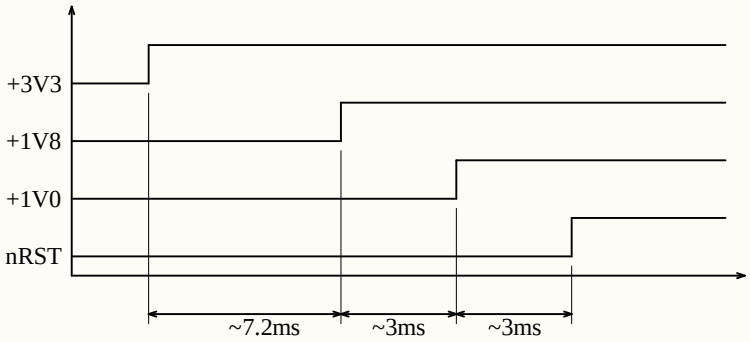
Vout = 0.41 * (1+R205/R207) = 1.00V

DESIGN NOTE:

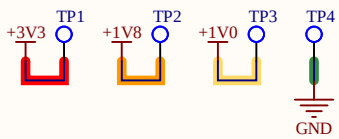
C214 introduces 3mS delay between 1V0 stable and PWRGD

delay = (C214 * 0.42)/0.14

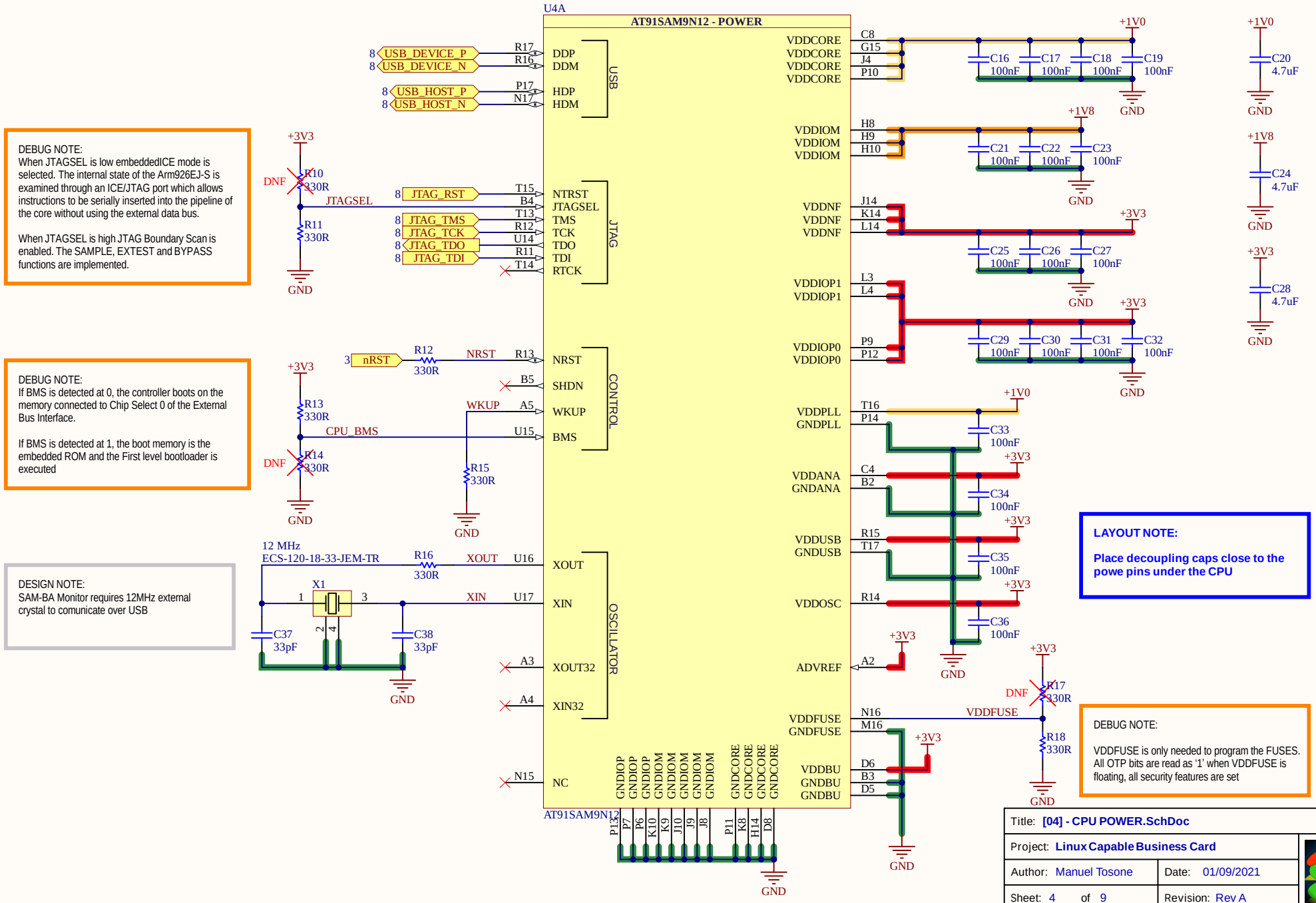
POWER-UP SEQUENCE

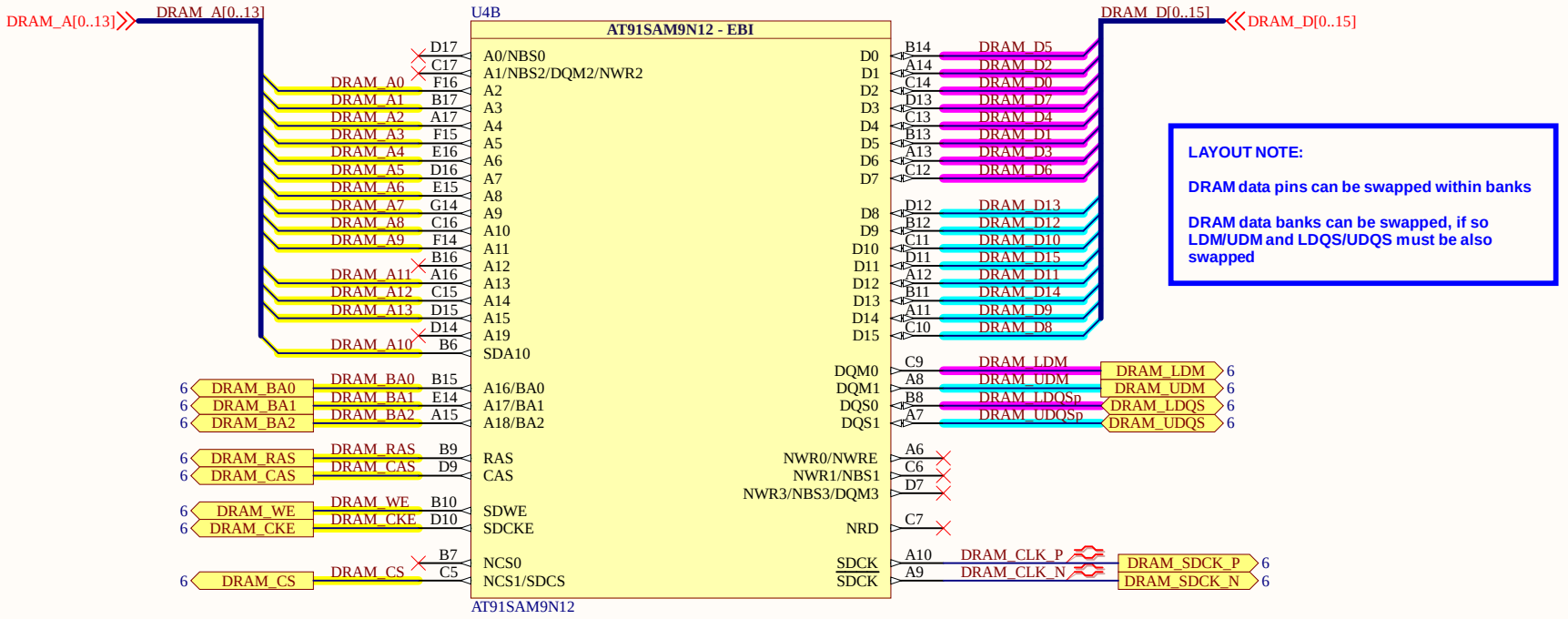


TEST POINTS

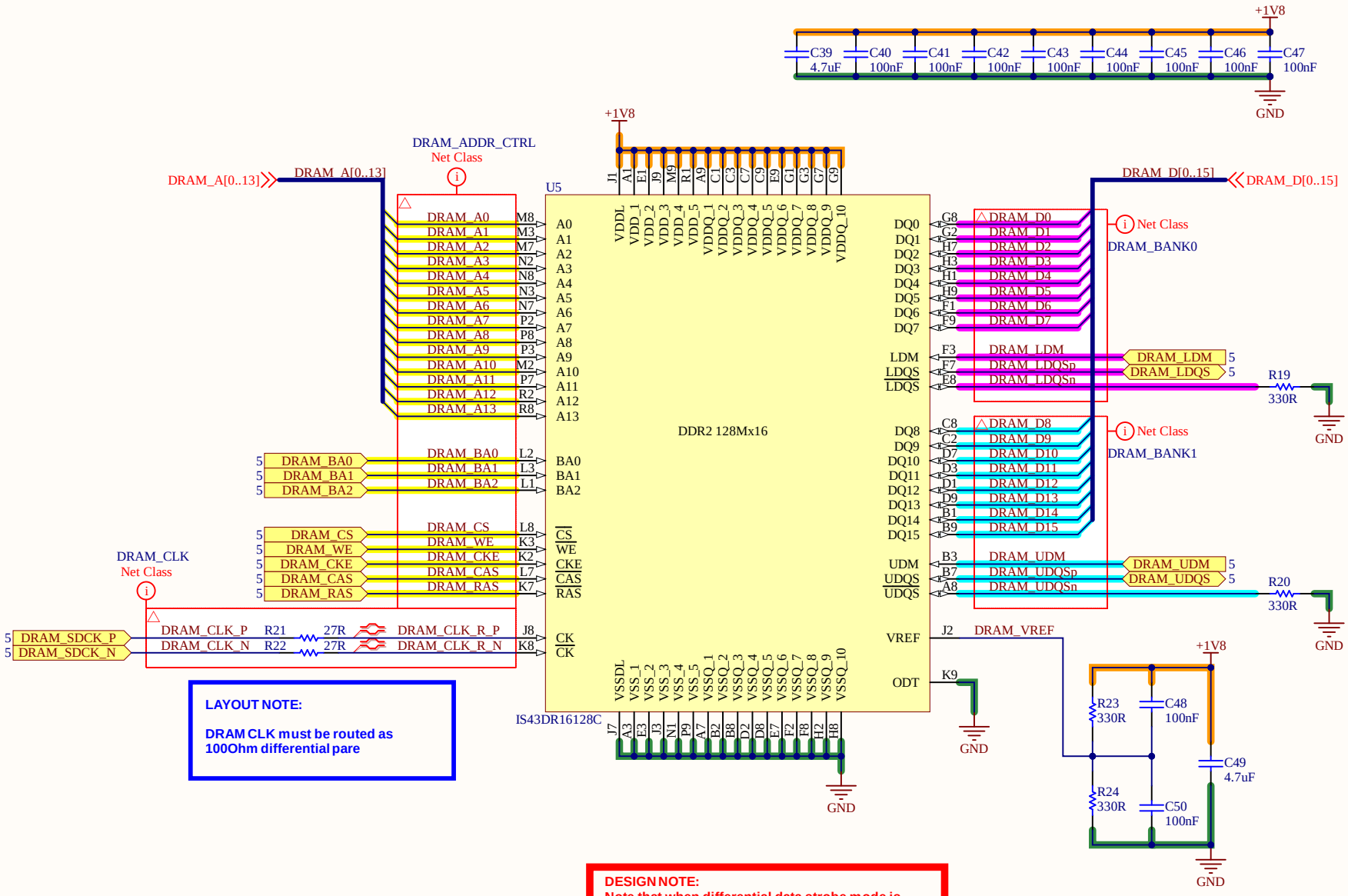


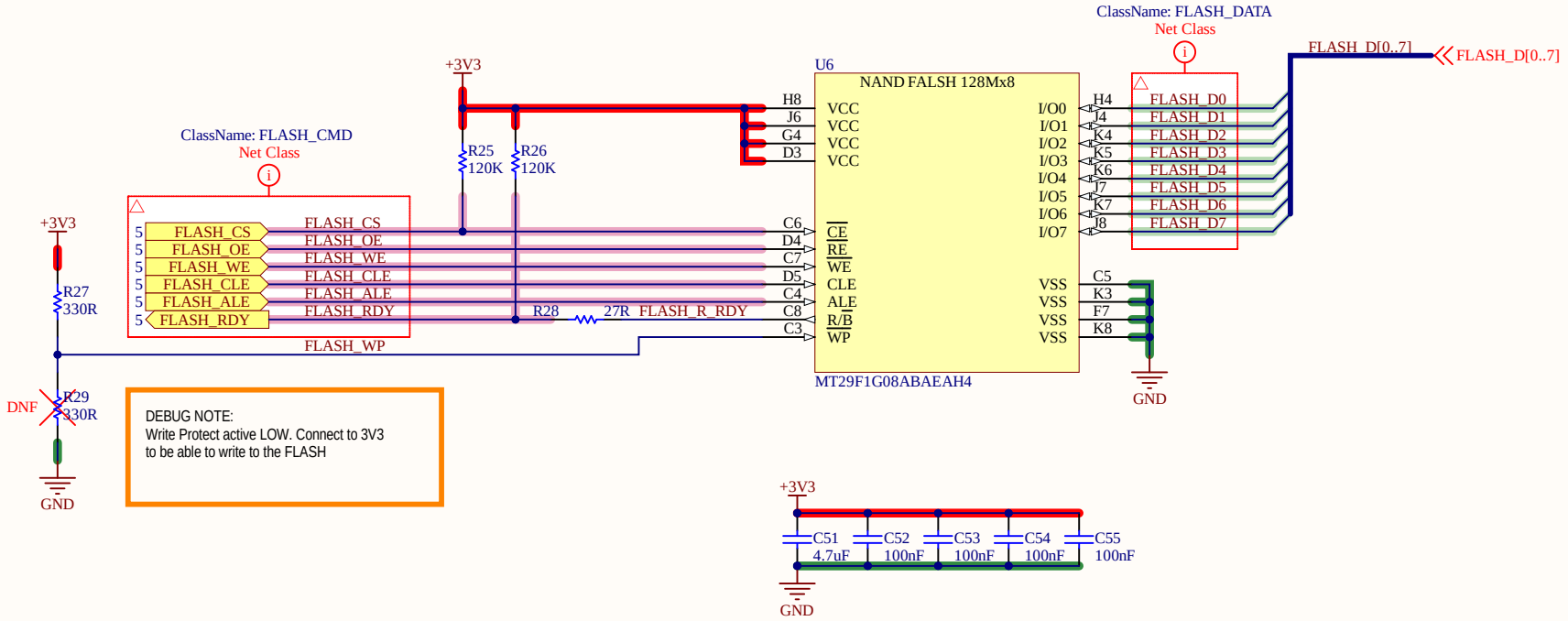
Title: [03] - POWER SUPPLIES.SchDoc	
Project: Linux Capable Business Card	
Author: Manuel Tosone	Date: 01/09/2021
Sheet: 3 of 9	Revision: Rev A


U4A
AT91SAM9N12 - POWER
USB
JTAG
CONTROL
OSCILLATOR
AT91SAM9N12
USB_DEVICE_P
USB_DEVICE_N
USB_HOST_P
USB_HOST_N
DDP
DDM
HDP
HDM
JTAG_RST
JTAG_TMS
JTAG_TCK
JTAG_TDO
JTAG_TDI
NTRST
JTAGSEL
TMS
TCK
TDO
TDI
RTCK
nRST
NRST
SHDN
WKUP
BMS
XOUT
XIN
XOUT32
XIN32
NC
VDDCORE
VDDIOM
VDDNF
VDDIOP1
VDDIOP0
VDDPLL
GNDPLL
VDDANA
GNDANA
VDDUSB
GNDUSB
VDDOSC
ADVREF
VDDFUSE
GNDFUSE
VDDBU
GNDBU
GNDIOP
GNDIOM
GNDCORE
+3V3
+1V8
+1V0
GND
DNF
JTAGSEL
CPU_BMS
12 MHz
ECS-120-18-33-JEM-TR
X1
C37
33pF
C38
33pF
VDDFUSE
DEBUG NOTE:
When JTAGSEL is low embeddedICE mode is selected. The internal state of the Arm926EJ-S is examined through an ICE/JTAG port which allows instructions to be serially inserted into the pipeline of the core without using the external data bus.
When JTAGSEL is high JTAG Boundary Scan is enabled. The SAMPLE, EXTEST and BYPASS functions are implemented.
DEBUG NOTE:
If BMS is detected at 0, the controller boots on the memory connected to Chip Select 0 of the External Bus Interface.
If BMS is detected at 1, the boot memory is the embedded ROM and the First level bootloader is executed
DESIGN NOTE:
SAM-BA Monitor requires 12MHz external crystal to comunicate over USB
LAYOUT NOTE:
Place decoupling caps close to the powe pins under the CPU
DEBUG NOTE:
VDDFUSE is only needed to program the FUSES. All OTP bits are read as '1' when VDDFUSE is floating, all security features are set
Title: [04] - CPU POWER.SchDoc
Project: Linux Capable Business Card
Author: Manuel Tosone
Date: 01/09/2021
Sheet: 4 of 9
Revision: Rev A

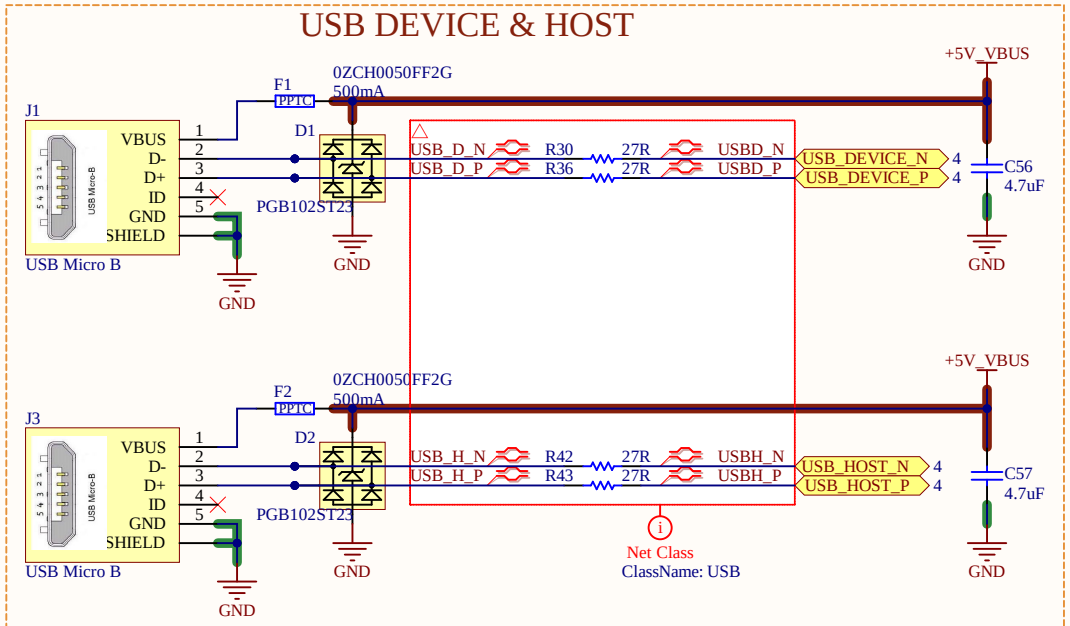


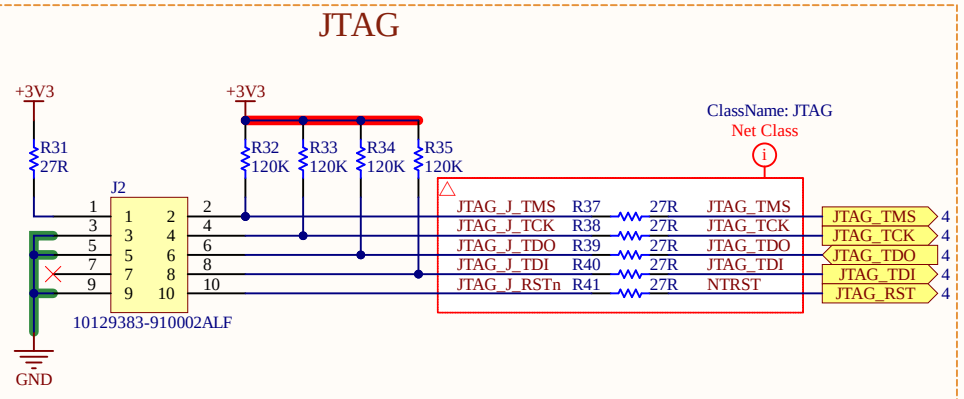
Title:	[05] - CPU EBI INTERFACE.SchDoc
Project:	Linux Capable Business Card
Author:	Manuel Tosone
Date:	01/09/2021
Sheet:	5 of 9
Revision:	Rev A

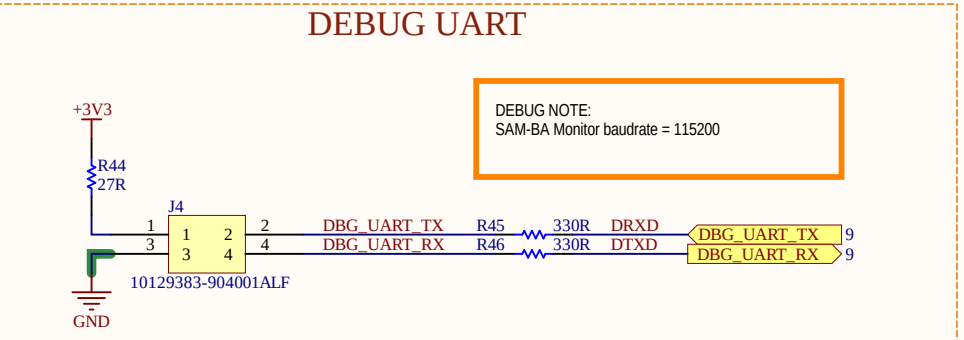

+1V8
C39 4.7uF
C40 100nF
C41 100nF
C42 100nF
C43 100nF
C44 100nF
C45 100nF
C46 100nF
C47 100nF
GND
DRAM_ADDR_CTRL
Net Class
DRAM_A[0..13]
DRAM_A[0..13]
U5
DRAM_A0 M8
DRAM_A1 M3
DRAM_A2 M7
DRAM_A3 N2
DRAM_A4 N8
DRAM_A5 N3
DRAM_A6 N7
DRAM_A7 P2
DRAM_A8 P8
DRAM_A9 P3
DRAM_A10 M2
DRAM_A11 P7
DRAM_A12 R2
DRAM_A13 R8
DRAM_BA0 L2
DRAM_BA1 L3
DRAM_BA2 L1
DRAM_CS L8
DRAM_WE K3
DRAM_CKE K2
DRAM_CAS L7
DRAM_RAS K7
DDR2 128Mx16
IS43DR16128C
DRAM_CLK
Net Class
DRAM_SDCK_P
DRAM_SDCK_N
DRAM_CLK_P R21 27R DRAM_CLK_R_P J8
DRAM_CLK_N R22 27R DRAM_CLK_R_N K8
LAYOUT NOTE:
DRAM CLK must be routed as 100Ohm differential pare
DRAM_D[0..15]
DRAM_D[0..15]
DRAM_D0 G8
DRAM_D1 G2
DRAM_D2 H7
DRAM_D3 H3
DRAM_D4 H1
DRAM_D5 H9
DRAM_D6 F1
DRAM_D7 F9
Net Class
DRAM_BANK0
DRAM_LDM F3
DRAM_LDQSp F7
DRAM_LDQSn E8
DRAM_LDM
DRAM_LDQS
R19 330R
GND
DRAM_D8 C8
DRAM_D9 C2
DRAM_D10 D7
DRAM_D11 D3
DRAM_D12 D1
DRAM_D13 D9
DRAM_D14 B1
DRAM_D15 B9
Net Class
DRAM_BANK1
DRAM_UDM B3
DRAM_UDQSp B7
DRAM_UDQSn A8
DRAM_UDM
DRAM_UDQS
R20 330R
GND
J2
DRAM_VREF
K9
GND
R23 330R
C48 100nF
C49 4.7uF
R24 330R
C50 100nF
GND
DESIGN NOTE:
Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, DQS, must be tied externally to VSS through a 20 Ω to 10 kΩ resistor to insure proper operation
Title: [06] - RAM DDR2.SchDoc
Project: Linux Capable Business Card
Author: Manuel Tosone
Date: 01/09/2021
Sheet: 6 of 9
Revision: Rev A

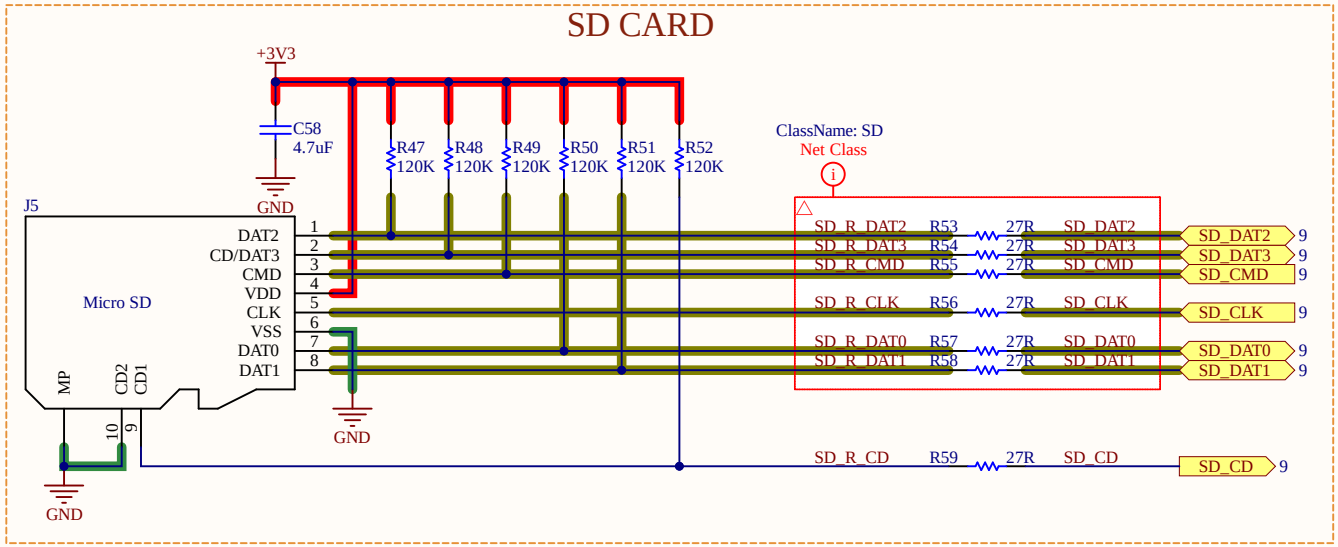


Title:	[07] - NAND FLASH.SchDoc
Project:	Linux Capable Business Card
Author:	Manuel Tosone
Date:	01/09/2021
Sheet:	7 of 9
Revision:	Rev A

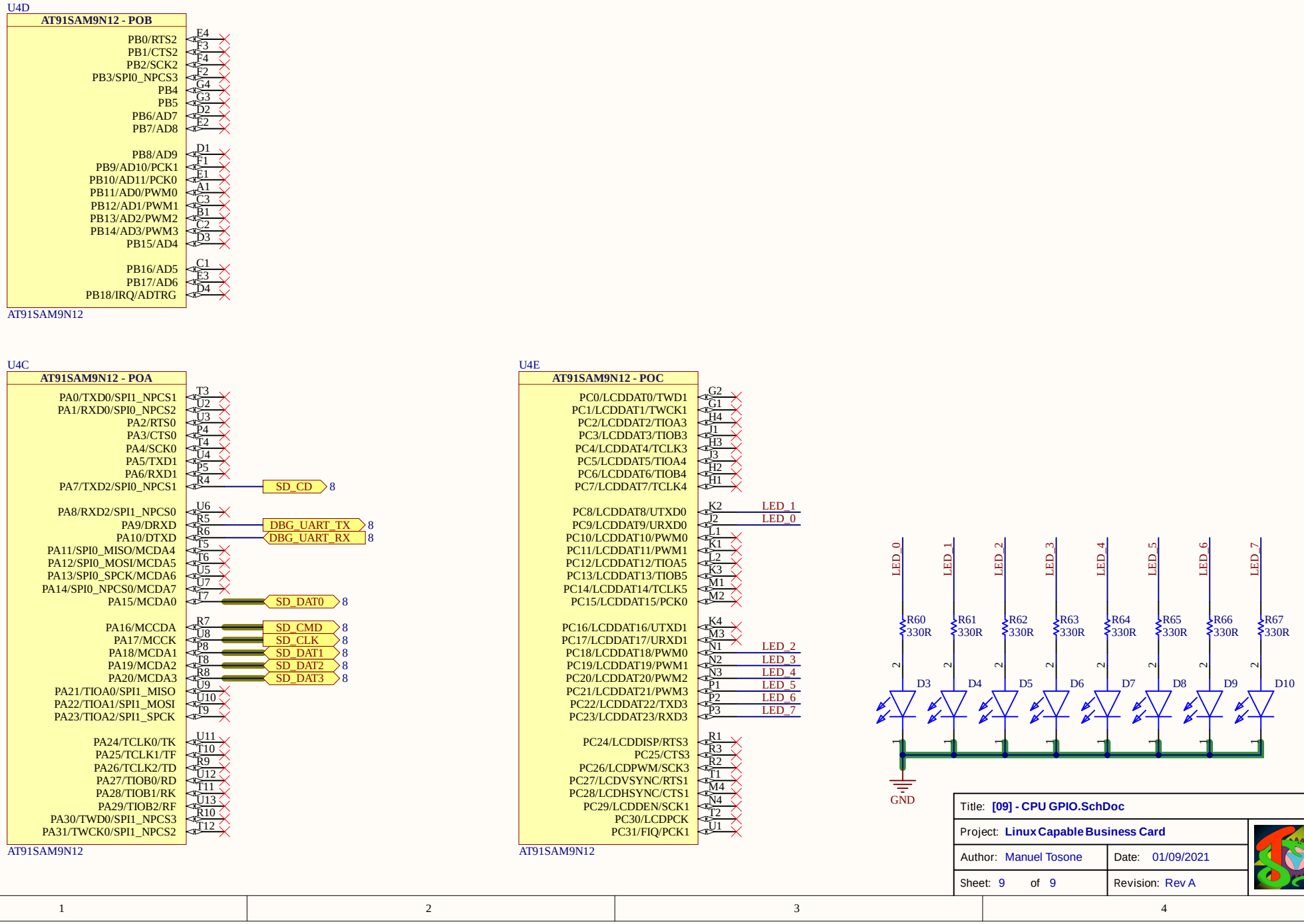








Title: [08] - CONNECTORS.SchDoc	
Project: Linux Capable Business Card	
Author: Manuel Tosone	Date: 01/09/2021
Sheet: 8 of 9	Revision: Rev A


U4D
AT91SAM9N12 - POB
PB0/RTS2 E4
PB1/CTS2 F3
PB2/SCK2 F4
PB3/SPI0_NPCS3 F2
PB4 G4
PB5 G3
PB6/AD7 D2
PB7/AD8 E2
PB8/AD9 D1
PB9/AD10/PCK1 F1
PB10/AD11/PCK0 E1
PB11/AD0/PWM0 A1
PB12/AD1/PWM1 C3
PB13/AD2/PWM2 B1
PB14/AD3/PWM3 C2
PB15/AD4 D3
PB16/AD5 C1
PB17/AD6 E3
PB18/IRQ/ADTRG D4
AT91SAM9N12
U4C
AT91SAM9N12 - POA
PA0/TXD0/SPI1_NPCS1 T3
PA1/RXD0/SPI0_NPCS2 U2
PA2/RTS0 U3
PA3/CTS0 P4
PA4/SCK0 T4
PA5/TXD1 U4
PA6/RXD1 P5
PA7/TXD2/SPI0_NPCS1 R4
SD_CD 8
PA8/RXD2/SPI1_NPCS0 U6
PA9/DRXD R5
DBG_UART_TX 8
PA10/DTXD R6
DBG_UART_RX 8
PA11/SPI0_MISO/MCDA4 T5
PA12/SPI0_MOSI/MCDA5 T6
PA13/SPI0_SPCK/MCDA6 U5
PA14/SPI0_NPCS0/MCDA7 U7
PA15/MCDA0 T7
SD_DAT0 8
PA16/MCCDA R7
PA17/MCCK U8
PA18/MCDA1 P8
PA19/MCDA2 T8
PA20/MCDA3 R8
SD_CMD 8
SD_CLK 8
SD_DAT1 8
SD_DAT2 8
SD_DAT3 8
PA21/TIOA0/SPI1_MISO U9
PA22/TIOA1/SPI1_MOSI U10
PA23/TIOA2/SPI1_SPCK T9
PA24/TCLK0/TK U11
PA25/TCLK1/TF T10
PA26/TCLK2/TD R9
PA27/TIOB0/RD U12
PA28/TIOB1/RK T11
PA29/TIOB2/RF U13
PA30/TWD0/SPI1_NPCS3 R10
PA31/TWCK0/SPI1_NPCS2 T12
AT91SAM9N12
U4E
AT91SAM9N12 - POC
PC0/LCDDAT0/TWD1 G2
PC1/LCDDAT1/TWCK1 G1
PC2/LCDDAT2/TIOA3 H4
PC3/LCDDAT3/TIOB3 J1
PC4/LCDDAT4/TCLK3 H3
PC5/LCDDAT5/TIOA4 J3
PC6/LCDDAT6/TIOB4 H2
PC7/LCDDAT7/TCLK4 H1
PC8/LCDDAT8/UTXD0 K2
PC9/LCDDAT9/URXD0 J2
LED_1
LED_0
PC10/LCDDAT10/PWM0 L1
PC11/LCDDAT11/PWM1 K1
PC12/LCDDAT12/TIOA5 L2
PC13/LCDDAT13/TIOB5 K3
PC14/LCDDAT14/TCLK5 M1
PC15/LCDDAT15/PCK0 M2
PC16/LCDDAT16/UTXD1 K4
PC17/LCDDAT17/URXD1 M3
PC18/LCDDAT18/PWM0 N1
PC19/LCDDAT19/PWM1 N2
PC20/LCDDAT20/PWM2 N3
PC21/LCDDAT21/PWM3 P1
PC22/LCDDAT22/TXD3 P2
PC23/LCDDAT23/RXD3 P3
LED_2
LED_3
LED_4
LED_5
LED_6
LED_7
PC24/LCDDISP/RTS3 R1
PC25/CTS3 R3
PC26/LCDPWM/SCK3 R2
PC27/LCDVSYNC/RTS1 T1
PC28/LCDHSYNC/CTS1 M4
PC29/LCDDEN/SCK1 N4
PC30/LCDPCK T2
PC31/FIQ/PCK1 U1
AT91SAM9N12
LED_0
LED_1
LED_2
LED_3
LED_4
LED_5
LED_6
LED_7
R60 330R
R61 330R
R62 330R
R63 330R
R64 330R
R65 330R
R66 330R
R67 330R
2
D3
D4
D5
D6
D7
D8
D9
D10
1
GND
Title: [09] - CPU GPIO.SchDoc
Project: Linux Capable Business Card
Author: Manuel Tosone
Date: 01/09/2021
Sheet: 9 of 9
Revision: Rev A