Decoupling capacitors: what size and how many?

Asked 11 years, 9 months ago Active 4 years, 7 months ago Viewed 70k times

78

Lots of chips nowadays require smoothing capacitors between VCC and GND for proper function. Given that my projects run at all sorts of different voltage and current levels, I was wondering if anyone had any rules of thumb for a) how many and b) what size capacitors should be used to ensure that power supply ripple doesn't affect my circuits?

40

power capacitor decoupling-capacitor

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edited Apr 3 '12 at 17:12

Brian Carlton

13.1k ●5 ●41 ●63

asked Apr 17 '10 at 9:14

jeremy

4,967 ●4 ●32 ●32

7 Smoothing capacitors are what you use in power supplies after rectifying, to get rid of most of the ripple. What you're talking about are decoupling capacitors. – stevenvh Apr 3 '12 at 14:25

I have a sorta related question (sorry for hijack) for could ceramic capacitors work just as well for decoupling caps? – user3073 Apr 3 '12 at 15:29

8 Answers

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You need to add a couple of more questions -- (c) what dielectric should I use and (d) where do I place the capacitor in my layout.

49

The amount and size varies by application. For power supply components the ESR (effective series resistance) is a critical component. For example the MC33269 LDO datasheet lists an ESR recommendation of 0.2Ohms to 10Ohms. There is a minimum amount of ESR required for stability.

For most logic ICs and op-amps I use a 0.1uF ceramic capacitor. I place the capacitor very close to the IC so that there is very short path from the capacitor leads to the ground. I use extensive ground and power planes to provide low impedance paths.

For power supply and high current components each application is different. I follow the manufacturer recommendations and place the capacitors very close to the IC.

For bulk filtering of power inputs coming into the board I will typically use a 10uF ceramic X7R capacitor. Again this varies with application.

Unless there is an minimum ESR requirement for stability or I need very large values of capacitance I will use either X7R or X5R dielectrics. Capacitance varies with voltage and temperature. Currently it is not difficult to get affordable 10uF ceramic capacitors. You do not need to over specify the voltage rating on ceramic capacitors. At the rated voltage the capacitance is within the tolerance range. Unless you increase the voltage above the dielectric breakdown you are only losing capacitance. Typically the dielectric strength is 2 to 3 times the rated voltage.

There is a very good application note about grounding and decoupling by Paul Brokaw called "An IC Amplifier User's Guide to Decoupling, Grounding,. and Making Things Go Right for a Change".

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edited Apr 25 '12 at 13:45
Community Bot
1

answered Apr 17 '10 at 11:58
jluciani
11.4k ● 1 ● 33 ● 54

17

I use the following rules of thumb for my digital circuits:

Each pair of power supplies pins should get its X7R ceramic 100nF capacitor. It should be as close as possible to the pins. Best is if the supply line passes by the capacitor first before it goes to the pin, but most of the time this is not necessary.

The capacitors at the ICs have nothing to do with ripple from the PSU. They are needed for *decoupling*, that is to satisfy fast changes in power supply current for the respective IC. The leads from the power supply to the IC are comparatively long and have some inductance, which prevents quick changes of the current. The power supply voltage at the IC may then get out of range and the IC can spuriously malfunction or in extreme cases become damaged.

Input and output of the voltage regulator should get a capacitor according to its data sheet, in particular with a correct equivalent series resistance (ESR) value. If you do it wrong the regulator may oscillate, especially for low dropout voltage regulators (LDOs).

For analog circuits X7R may not be the right material, because it has a relatively large piezoelectric effect. That is, mechanical vibrations can cause voltage changes and vice versa. C0G is better in that respect. Though this caveat mostly applies to signal paths.

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edited Jun 14 '17 at 19:35

Brian Carlton

13.1k ● 5 ● 41 ● 63

answered Apr 17 '10 at 15:27

starblue

6,332 ● 2 ● 20 ● 34

"The output of the power supply should typically get a 10µF capacitor. Check the data sheet of the voltage regulator data sheet for the required ESR value, if you do it wrong the regulator may oscillate." Is it to diminish the ripple of the PSU ? Can you explain how to do it "right" ? – MikeTeX Aug 19 '15 at 14:39

I edited the question somewhat, reflecting my understanding 5 years later. – starblue Aug 22 '15 at 7:13

It's the first time I hear about the piezoelectric effect, affecting capacitors! Thanks. – not2qubit Aug 13 '19 at 14:11

Here is the TDK document for singing caps. – not2qubit Aug 14 '19 at 8:08

13

Like I said in comment, you probably mean *decoupling capacitors*, not smoothing capacitors.

Decoupling capacitors' purpose is not to get rid of your power supply's ripple, but to catch glitches. An IC may need much extra current for a short time, for instance when thousands of transistors switch at the same time. The inductance of the PCB's traces may prevent that the power supply can deliver this that fast. So decoupling capacitors are used as local energy buffers to overcome this.

This means that it's not easy to calculate what value the capacitors should have. The value depends on the inductance of the PCB's traces and the current peaks your IC excerts on the power supply. Most engineers will place 100nF X7R capacitors *as close as possible* to the IC's power pins. One capacitor per power pin. A good IC pinout will have a ground pin next to each power pin, so you can keep the loop as short as possible.

For low-power ICs 10nF capacitors may be sufficient and may be preferred over the 100nF because of their lower internal inductance. For this reason you also find 10nF parallel to the 100nF. In this case the smaller capacitor should be closest to the pins.

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answered Apr 3 '12 at 14:41

stevenvh

142k ● 20 ● 443 ● 658

1 As shown in another answer [electronics.stackexchange.com/questions/25280/..., the lower value cap *in the same package size* doesn't have very much lower inductance. But if you go to a smaller package to get lower inductance, you might be forced to use a smaller capacitance value to get the WV you want. – The Photon Apr 3 '12 at 16:34

1 Just a few years ago, 0.1 uF in 0402 was still somewhat exotic, high-priced, and low-reliability. In those days, an 0402 at 0.01 uF paralleled with a 0.1 uF in 0603 was a very common configuration. Now 0.1 uF in 0402, as several answers have recommended, is mature technology and a widely-used standard for

decoupling logic circuits. – The Photon Apr 3 '12 at 16:37

2 Also, I'd add to your list of things to consider when choosing the capacitor: What's the frequency range of the transient currents drawn by the chip being decoupled; and how sensitive is that chip and others in the circuit to voltage ripple. – The Photon Apr 3 '12 at 16:41

10

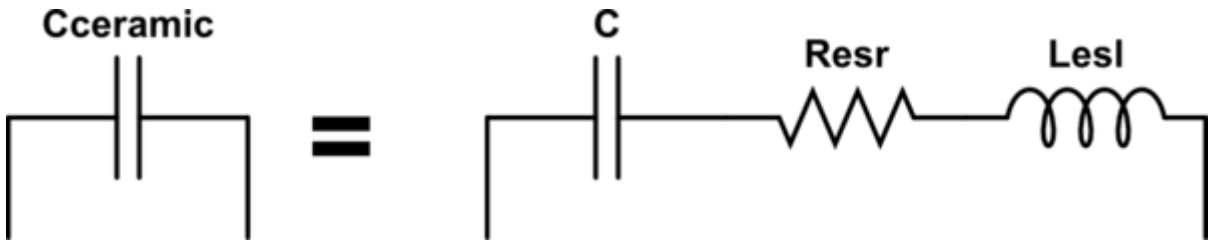
Capacitors made of X7R (and even more so Y5V) have huge capacity/voltage dependence. You can check this yourself at the excellent Murata products online characteristics browser (Simsurfing) at ttp://ds.murata.co.jp/software/simsurfing/en-us/

The ceramic capacitor voltage dependence is striking. It is normal for X7R capacitor to have no more then 30% of rated capacity at rated voltage. For example - 10uF Murata capacitor GRM21BR61C106KE15 (0805 package, X5R) rated for 16V will give you only 2.3uF capacity with 12V DC applied at 25C temperature. Y5V is much worse in this respect.

In order to obtain close to 10uF capacity you have to use 25V rated GRM32DR71E106K (1210 case, X7R) which gives 7.5uF under same conditions.

Other then DC voltage (and temperature) dependencies, Real "ceramic chip capacitor" have strong frequency dependence when acting as power decoupling shunts. Murata's site provides |Z|, R and X frequency dependencies graphs for their capacitors, browsing these gives you an insight into actual performance of the part we call "capacitor" at different frequencies.

Real ceramic capacitor can be modeled by an ideal capacitor (C) connected in series with internal resistance (Resr) and inductance (Lesl). There is also R-isolation in parallel with C, but unless you go over capacitor's rated voltage it is unimportant for power decoupling applications.



simulate this circuit – Schematic created using CircuitLab

Thus chip ceramic capacitors will act as capacitors only up to a certain frequency (self resonant for the serial LC contour which real capacitor is in fact), above which they start to act as inductors. This frequency Fres is equal to sqrt(1/LC) and is determined by both the ceramics composition and capacitor geometry - generally smaller packages have higher Fres Also, capacitors have a purely resistive component (Resr) which results mostly from the losses in the ceramic and determines the minimum impedance the capacitor can provide. It is usually in the mili-Ohms range.

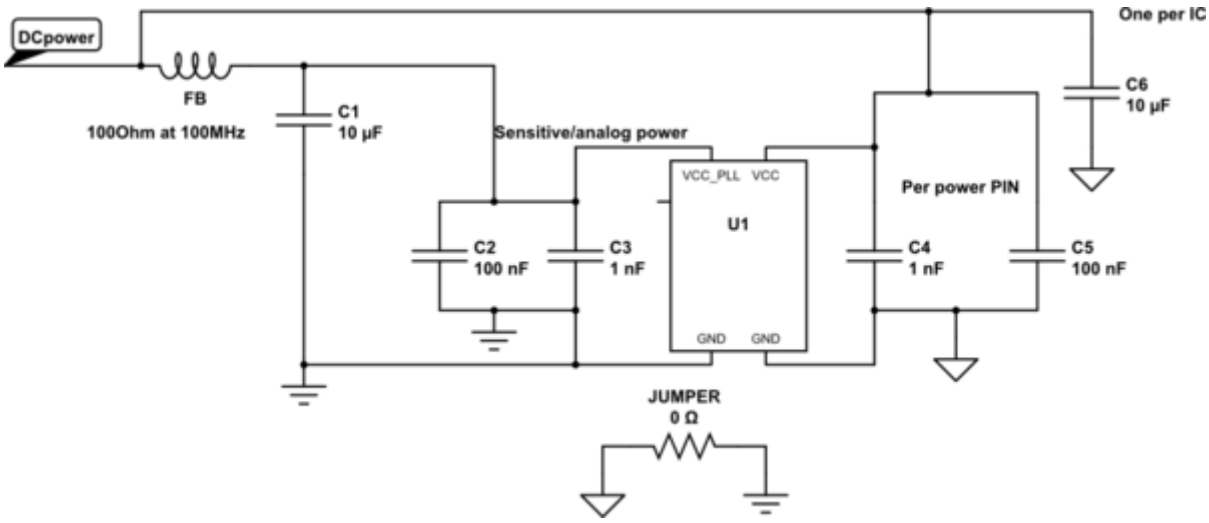
In practice for good decoupling I use 3 types of capacitors.

Higher capacity about 10uF in 1210 or 1208 package per integrated circuit, that covers 10KHz

Higher capacity about 10uF in 1210 or 1206 package per integrated circuit, that covers 10KHz to 10MHz with less then 10-15 mili-Ohm shunt for power line noise.

Then per every IC power pin I put two capacitors - one 100nF in 0806 package covering 1MHz to 40MHz with 20 mili-Ohm shunt, and one 1nF in 0603 package, covering 80MHz to 400MHz with 30 mili-ohm shunt. This more or less covers 10KHz to 400MHz range for filtering out power line noise.

For sensitive power circuits (like PLL digital and especially analog power) I put ferrite beads (again, Murata has characteristics browser for those) rated 100 to 300 Ohms at 100Mhz. It's also a good idea to separate grounds between sensitive and regular power circuits. Thus overall outline of IC power plan looks like this, with 10uF C6 per IC package, and 1nF/100nF C4/C5 per each power pin:



simulate this circuit

Speaking about routing and placement - power and ground is routed to capacitors first, only at capacitors we connect to power and ground planes through vias. 1nF capacitors are placed closer to IC pins. Capacitors have to be placed as close to power pins as possible, no further then 1mm trace length from capacitor pad to IC pad.

Vias and even short traces on PCB pose a significant inductance for the frequencies and capacitance we're dealing with. For example, 0.5mm diameter via in 1.5mm thick PCB has 1.1nH inductance from top to bottom layer. For 1nF capacitor that results in Fres equal to only 15MHz. Thus, connecting a capacitor through via makes 1nF capacitor low Resr unusable at frequencies above 15MHz. In fact 1.1nH reactance at 100MHz is as much as 0.7 Ohm.

Trace of 1mm length 0.2mm width, 0.35mm above power plane will have comparable inductance of 0.4nH - which again makes capacitors less efficient, thus trying to limit capacitors trace length to a fraction of a mm and making them as wide as possible makes a lot

of sense.

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edited Aug 18 '15 at 10:04

answered Aug 18 '15 at 9:52

vleo

201 ● 2 ● 5

How to separate grounds in single PCB? Add another PSU? From what I heard even if two PSU is used (e.g. one to power motor, another for IC), then it is recommended to make grounds common. – Ivan Balashov Feb 8 '16 at 10:27

You make separate PCB sub planes for power and analog grounds, join then through a single jumper - like the one on the picture above (JUMPER 0 Ohm). Same sub planes separation for analog and digital power. Feed analog power through ferrite bead, as shown on the picture above (FB). Route analog wires only above analog planes, and ditital wires - only above digital planes (power and ground). This assumes at least 4 layers PCB normally. Ideally, route wires above ground layer. – vleo Feb 26 '16 at 17:00

1 This is really one of the best answers I've seen on this topic. Thank you. – not2qubit Aug 13 '19 at 14:14

I think the plane separation with jumper will be ok because you mention keeping analog and digital signals above their planes, but i think it's worth being very explicit about this because if you route some of the digital signals over the analog ground it could be bad (all return currents are going to have to flow through that jumper). Here's a great discussion of this. In any event I think keeping the digital/signal routing isolated is more important than separating ground planes. – MattHusz Mar 23 '20 at 7:39

7

If you're using big electrolytics to smooth out a power supply, don't forget to add small ceramic caps in parallel for the high frequencies. Electrolytic caps actually look like inductors at high frequencies.

- http://www.boostbuck.com/BypassingaCapacitor.html
- http://www.amccaps.com/leaded-capacitors/switch-mode-ceramic-capacitors/impedance-vs-frequency.html
- http://enjeti.tamu.edu/conf-papers/electrolytic-cap-pwm-asd.pdf

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edited Apr 17 '10 at 14:18

answered Apr 17 '10 at 14:04

endolith

27.6k ● 21 ● 109 ● 172

What kind of frequency range is "high frequencies"? – bean May 23 '15 at 19:25

4

If it's not a very demanding circuit, scatter some 100nF X7R caps around. If you don't have power planes, keep them close to a pair of device pins, directly across them ideally.

If your circuit is drawing a lot of power, at high frequencies, you need to *design* your power distribution system (PDS). Xilinx have a reasonable introduction to this. There's also lots of discussion on si-list.

Next question is "what are good rules of thumb to decide if my circuit is demanding enough to be beyond rules of thumb for decoupling design?" :)

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edited Nov 4 '16 at 13:50

answered Apr 3 '12 at 16:32

Martin Thompson

8,199 ● 1 ● 21 ● 43

2

A smoothing capacitor should be placed, as you stated, in the circuit in case of current spikes caused by load changes. When placing a smoothing capacitor, place it as close to the IC pin as you can. A value of 47uf to about 100uf should be sufficient.

Check out:

http://www.learningaboutelectronics.com/Articles/How-to-connect-a-voltage-regulator-in-a-circuit

for some info on clarifying different capacitor usages in circuits.

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answered Apr 3 '12 at 14:16

David

21 ● 1

1 The location of 47 uF-100 uF caps are much less important than the lower value ones. – Brian Carlton Jun 14 '17 at 19:36

Interesting link, the caps used with the 7805 in the above-cited article are non-polarized, whereas in the Art of Electronics the (same capacitance) caps are both polairzed. I would be very grateful if someone could call one way or the other. I'm inclined to go with AoE, of course. – Hektor Jul 30 '21 at 18:43

2

The reservoir or smoothing capacitor value is a product of the maximum current required by the circuit, and the recovery time of the regulator under load... (no regulator reacts instantly)...

In circuit where the current demands are constant, 10uF - 22uF should suffice...

For circuits where current demands fluctuate rapidly, a capacitor value in the hundreds of uF may be required...

In a recent build with a 3.3 volt supply and sudden demand for 250mA, a capacitor value of 470uF was required to maintain stability...

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answered Nov 10 '14 at 23:33

Mike

21 ● 1