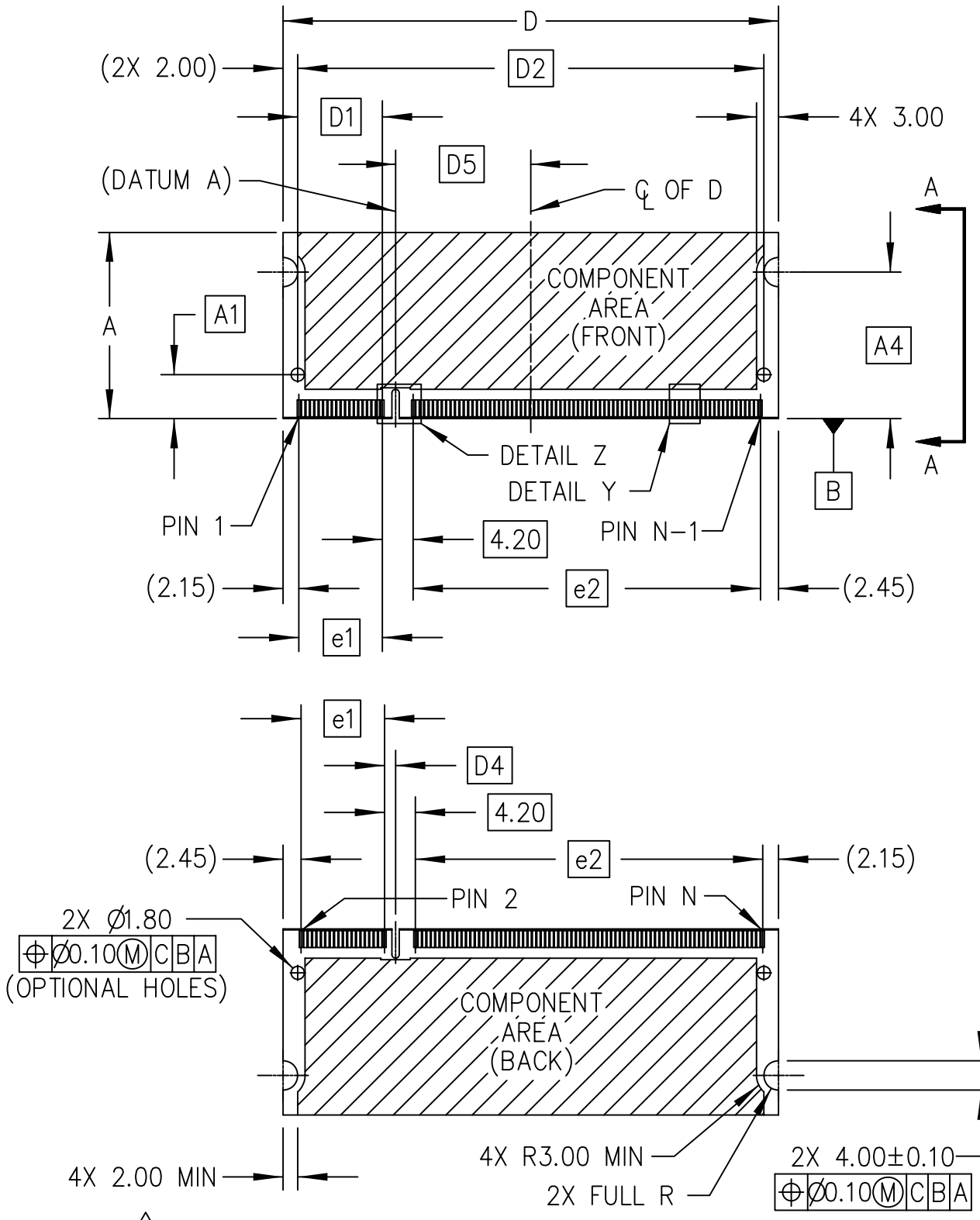

PATENT ISSUES 12

JEDEC SOLID STATE PRODUCT OUTLINE	THIS REGISTERED OUTLINE HAS BEEN PREPARED AND PUBLISHED BY THE JEDEC JC–11 COMMITTEE AND REFLECTS A PRODUCT WITH ANTICIPATED USE IN THE ELECTRONICS INDUSTRY. CHANGES ARE LIKELY TO OCCUR.

TITLE:	PACKAGE DESIGNATOR:	ISSUE:	DATE:	ITEM NO.	PAGE:
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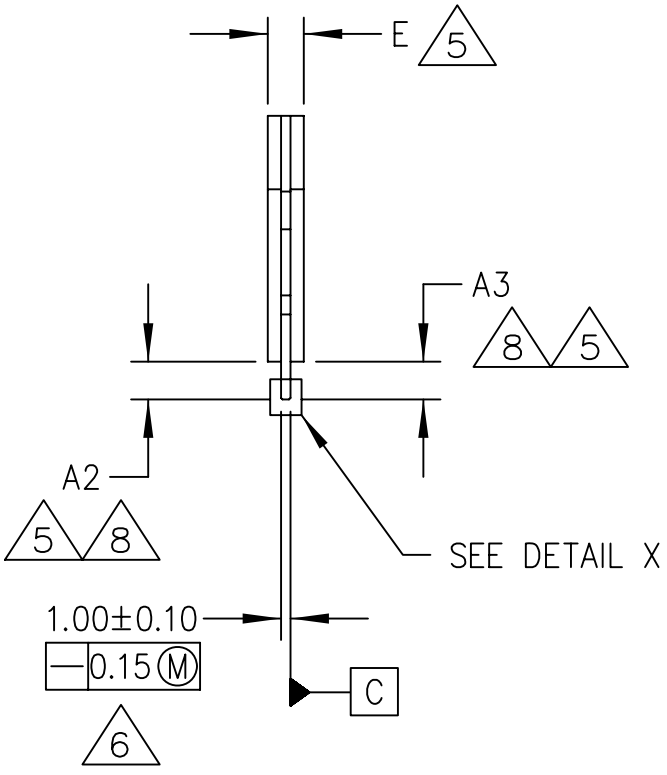
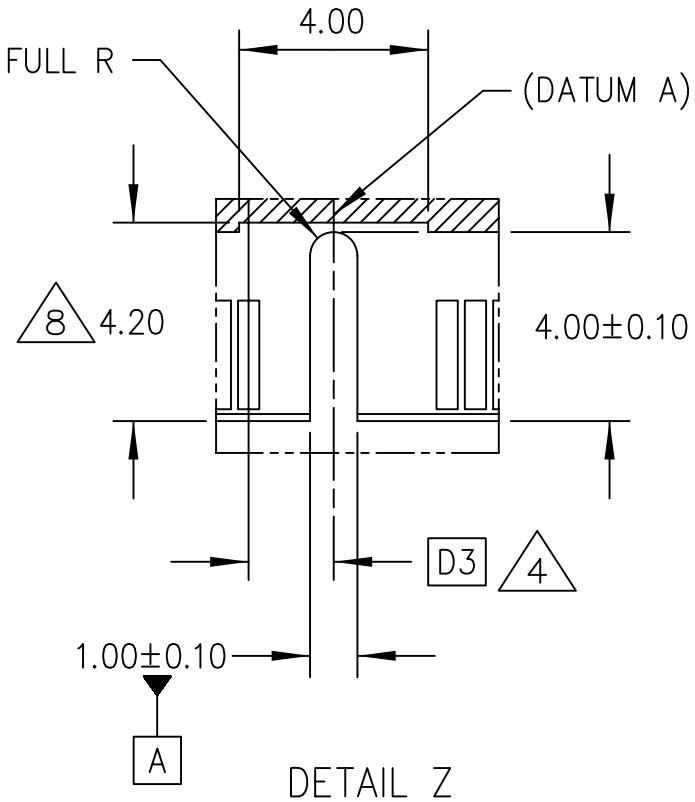
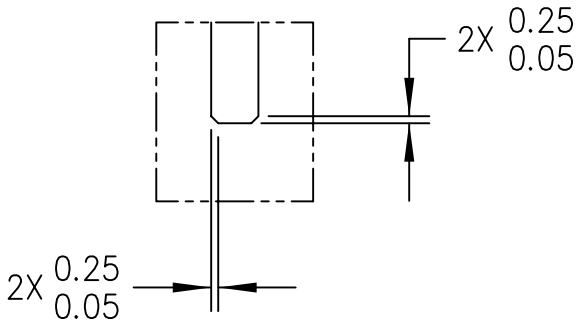


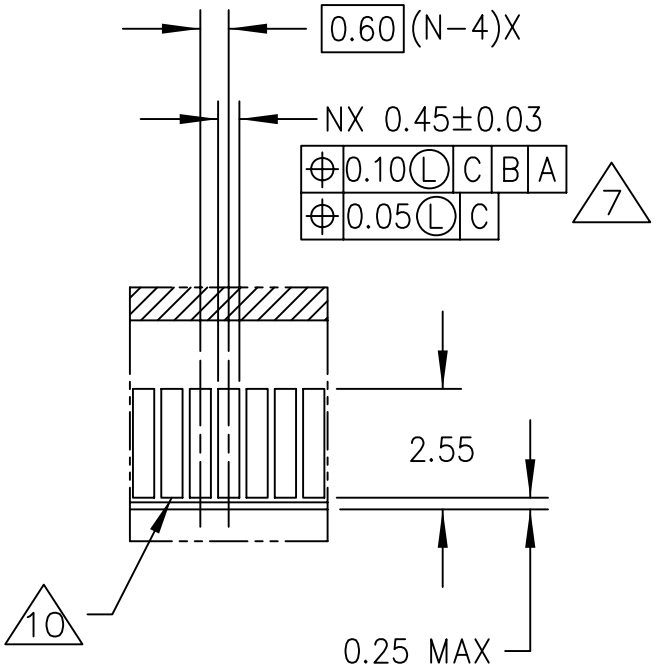
VIEW A–A



DETAIL Z



DETAIL X
(OPTIONAL)
11



DETAIL Y

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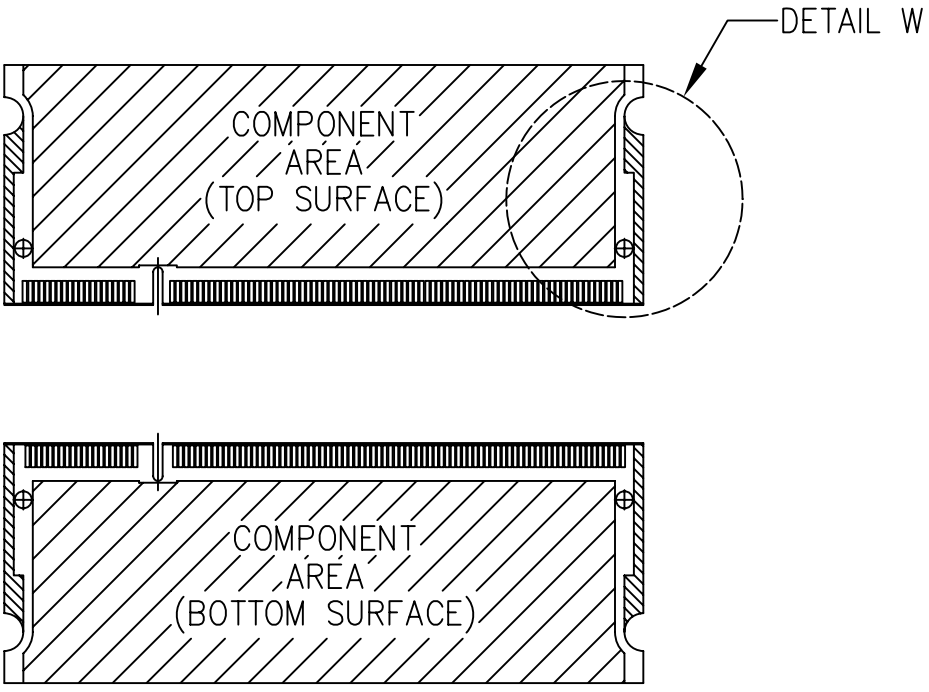
COMMON DIMENSION TABLE				
SYMBOL	MIN	NOM	MAX	NOTES
A1	6.00 BASIC			
A2	4.00	--	--	5,8
A3	4.00	--	--	5,8
A4	20.00 BASIC			
D	67.45	67.60	67.75	
D1	11.55 BASIC			
D2	63.60 BASIC			
E	--	--	3.80	5
e1	11.40 BASIC			
e2	47.40 BASIC			
N	200			
ISSUE	A			
REF	14-043			
NOTES	1,2,3			

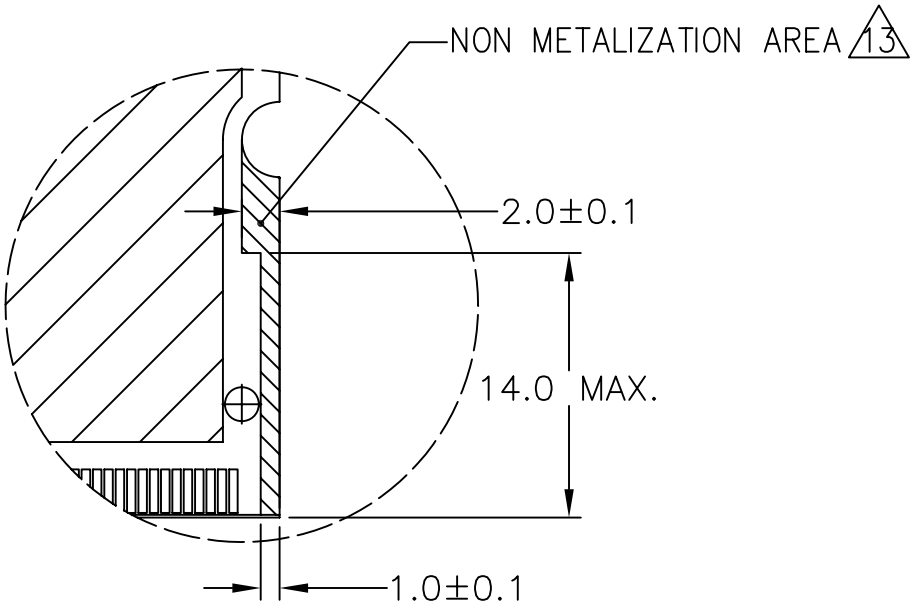
SDRAM VARIATIONS							
	AA			AB			
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX	NOTES
A	25.25	25.40	25.55	25.25	25.40	25.55	
D3	1.80 BASIC			2.70 BASIC			4
D4	1.50 BASIC			2.40 BASIC			
D5	18.45 BASIC			17.55 BASIC			
ISSUE	A						
REF	14-043						
NOTES	1,2,3						

SDRAM VARIATIONS							
	BA			BB			
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX	NOTES
A	31.60	31.75	31.90	31.60	31.75	31.90	
D3	1.80 BASIC			2.70 BASIC			4
D4	1.50 BASIC			2.40 BASIC			
D5	18.45 BASIC			17.55 BASIC			
ISSUE	A						
REF	14-043						
NOTES	1,2,3						

SDRAM VARIATIONS							
	CA			CB			
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX	NOTES
A	29.85	30.00	30.15	29.85	30.00	30.15	
D3	1.80 BASIC			2.70 BASIC			4
D4	1.50 BASIC			2.40 BASIC			
D5	18.45 BASIC			17.55 BASIC			
ISSUE	B						
REF	14-059						
NOTES	1,2,3						

NON–METALIZATION DEFINITION OUTER LAYERS





DETAIL W (4 PLACES)

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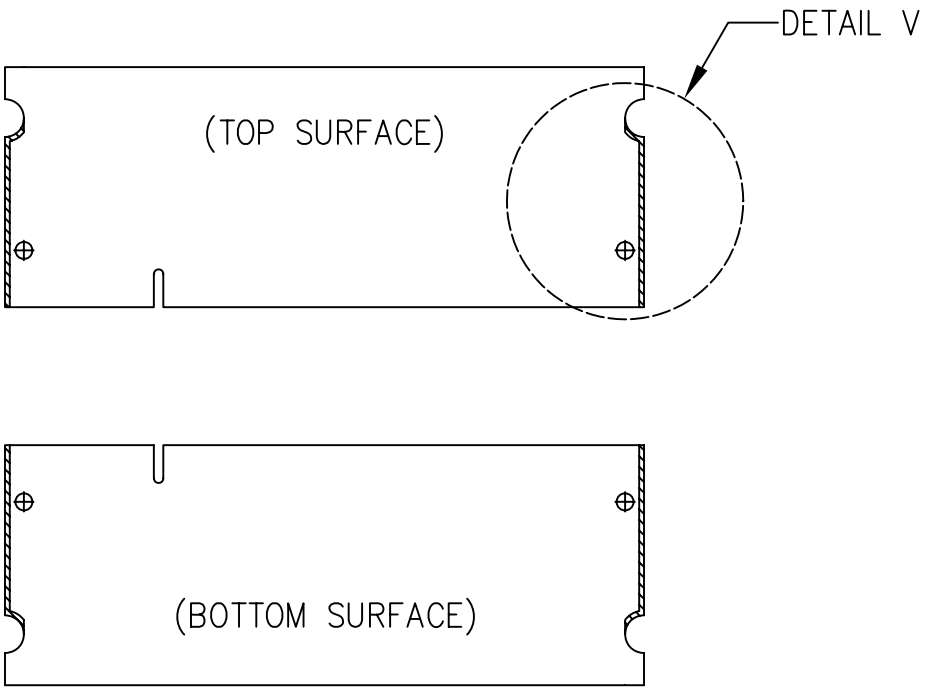
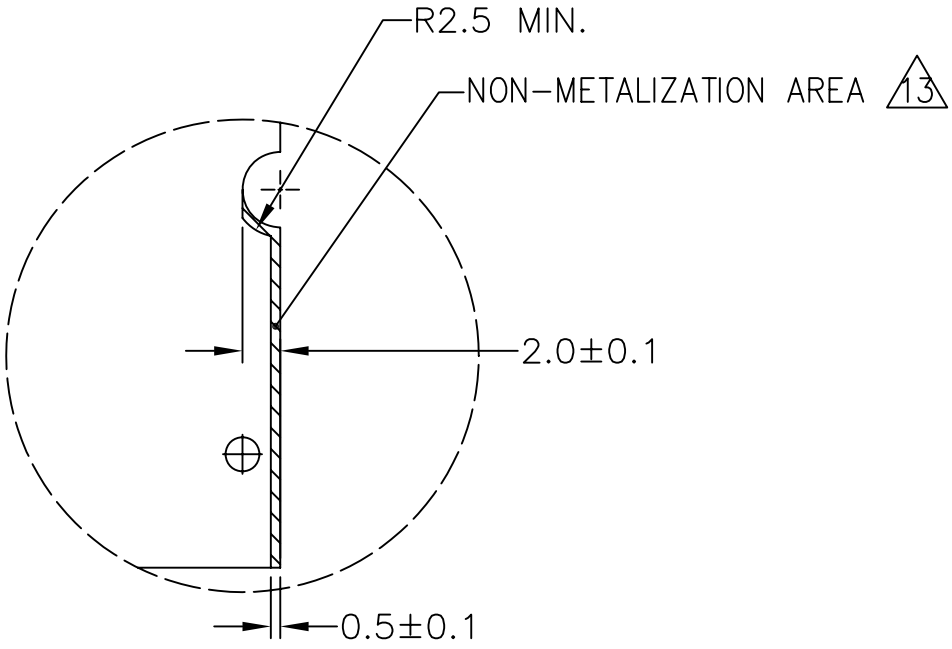
NON-METALIZATION DEFINITION ALL INNER LAYERS





DETAIL V (4 PLACES)

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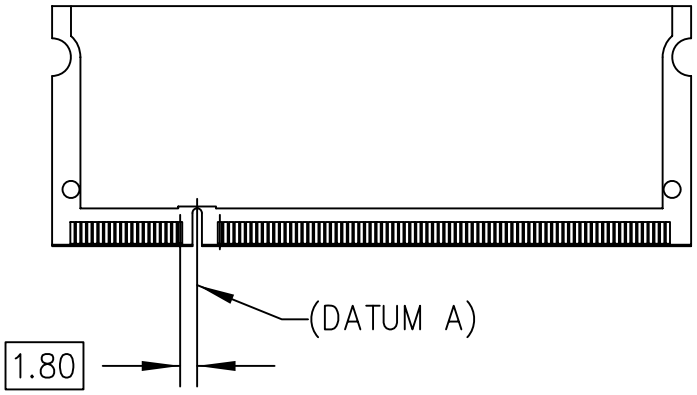
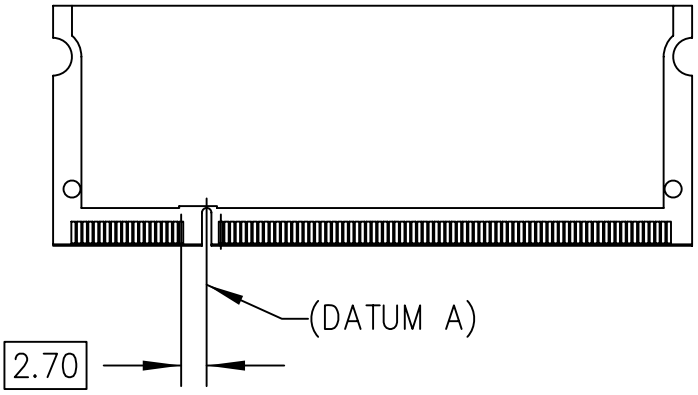
MECHANICAL KEYING:
(FRONT VIEWS)

POWER SUPPLY ⚠9	⚠4
2.5 V	
1.8 V	

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994.

2. TOLERANCES ON ALL DIMENSIONS ±0.15 UNLESS OTHERWISE SPECIFIED.

3. ALL DIMENSIONS ARE IN MM.

4 APPLICATION NOTE:
VARYING THE POSITION OF THE NOTCH IDENTIFIES THE OPERATIONAL VOLTAGE: 2.5 VOLT (XA), 1.8 VOLT (XB).

5 DIMENSIONS APPLICABLE WHEN COMPONENTS MOUNTED ON BOTH SIDES.

6 CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.

7 APPLICATION NOTE:
RECOMMENDED PLATING FOR CONTACT PADS ARE:
1) PREFERABLE PLATING: ELECTROLYTIC GOLD PLATING 0.76 MICROMETERS MINIMUM OVER ELECTROLYTIC Ni 2.00 MICROMETERS MINIMUM.
2) ALTERNATIVE PLATING: GOLD PLATING 0.05 – 0.75 MICROMETERS OVER Ni 2.00 MICROMETERS MINIMUM MUST USE AN ELECTRONIC CONTACT GRADE CORROSIVE BARRIER LUBRICANT.

8 BORDER OF COMPONENT AREA.

9 THE JC–45.3 COMMITTEE CONTROLS THE INFORMATION IN THIS COLUMN. IT IS SHOWN HERE FOR REFERENCE ONLY, AND IS SUBJECT TO CHANGE.

10 APPLICATION NOTE:
EDGE OF CONTACT PADS SHALL BE FREE OF BURRS AND EXTERNAL TIE BARS.

11 THE ADDITION OF THIS BEVEL IS A FABRICATION OPTION AND IS NOT REQUIRED. THE BEVEL AIDS THE INSERTION OF THE MODULE INTO THE CONNECTOR. THE BEVEL IS NOT TO HIT THE PLATED CONTACTS.

12 PATENT CLAIM:
IT HAS BEEN STATED THAT U.S. PATENT NO. 5,227,664 (HELD BY HITACHI) MAY BE RELATED TO CERTAIN IMPLEMENTATIONS OF THIS PACKAGE OUTLINE.

NOTES:

13. 'METALIZATION' IS DEFINED AS ANY METAL SURFACE THAT HAS A RETURN PATH TO POWER SUPPLY OR GROUND, THROUGH A COMPONENT OR CONDUCTIVE PLANE VCC OR VDD, BLIND OR PLATED THROUGH HOLE (PTH), AS WELL AS NARROW OR WIDE TRACES. ANY SURFACE METALS SUCH AS CONNECTOR PIN IDENTIFICATION, PCB VENDER CODE, ETC. THAT DO NOT HAVE A METALS AS A RETURN PATH ARE ACCEPTABLE.
'NON-METALIZATION' IS DEFINED AS THE OPPOSITE TO 'METALIZATION' AND DOES NOT INCLUDE ANY METAL OR CONDUCTIVE ELEMENTS THAT MAY CAUSE ELECTRICAL SHORT CIRCUIT.
HOWEVER, ANY SURFACE METALS SUCH AS CONNECTOR PIN IDENTIFICATION, PCB VENDOR NAME OR CODE, ETC. THAT DOES NOT HAVE CONDUCTIVE RETURN PATH TO VCC OR VDD IS ACCEPTABLE.

Change Record

If the changes involves any words added or deleted (excluding deletion of accidentally repeated words), the change is included. Punctuation chages may or may not be included.

Initial Issue: A	Date:	Item:

Revision History:

Issue: E	Date: Nov 06	Item: 11.14-106E

Location	Change from:	Change to:
Page 1	PIN N/2	PIN N-1

Location	Change from:	Change to:

Location	Change from:	Change to:

JEDEC SOLID STATE PRODUCT OUTLINES	THIS *REGISTERED OUTLINE* HAS BEEN PREPARED BY THE JEDEC JC-11 COMMITTEE AND REFLECTS A PRODUCT WITH ANTICIPATED USAGE IN THE ELECTRONICS INDUSTRY; CHANGES ARE LIKELY TO OCCUR.

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