Fundamentals of HBM, MM, and CDM Tests

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STORY

The primary ESD tests are the human-body model (HBM), the machine model (MM), and the charged-device model (CDM).

There are many established models that test the reliability of semiconductor devices against an ESD event to insure effectiveness and reliability. The primary ESD tests are the human-body model (HBM), the machine model (MM), and the charged-device model (CDM) (Figure1).

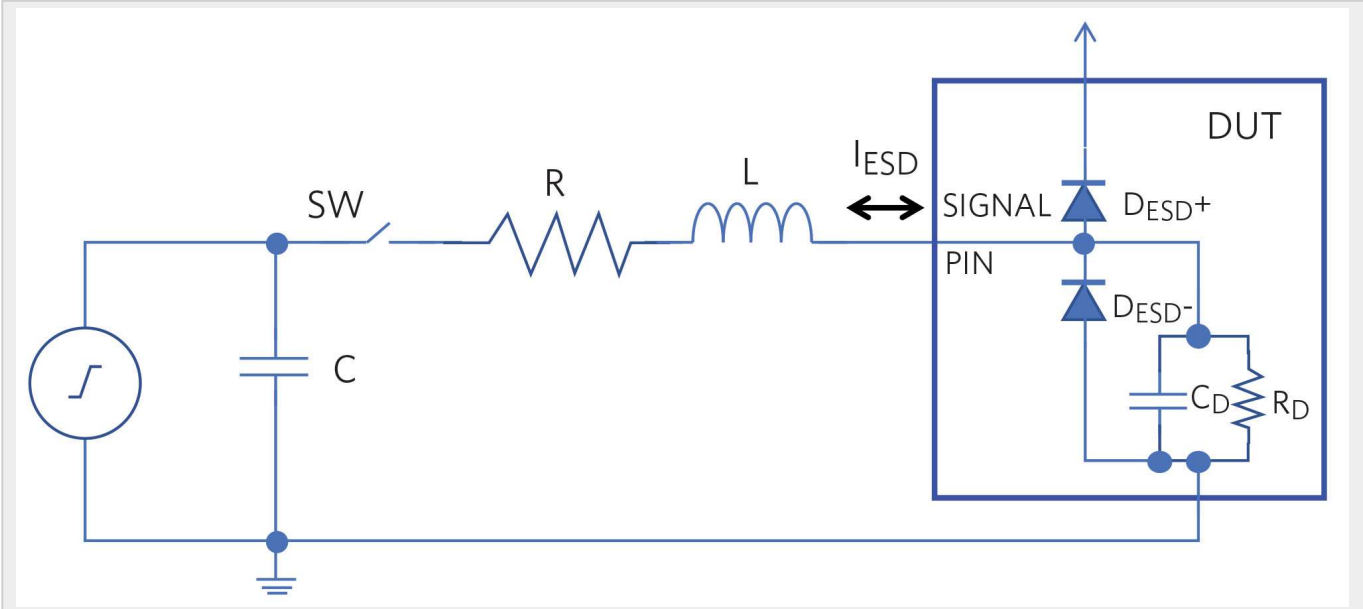

Figure 1. ESD model for HBM, MM, and CDM tests.

The JEDEC standards ensure ESD test effectiveness and reliability. The test configuration (Figure 1) for these three tests has five elements: V_{ESD}, C, SW, R, and L. The input V_{ESD} voltage charges the capacitor C before the closure of the switch (SW). With the closing of SW, the ESD fixture's output impedance (R and L) sends the V_{ESD} signal, which converts to a current (I_{ESD}) into the device-under-test (DUT). The now ESD current flows through the DUT's ESD diodes; D_{ESD+} and D_{ESD-}. If either or both ESD diodes fail or are missing, the current (I_{ESD}) from this ESD event will find another path, which many times catastrophically goes further into the DUT circuitry.

Equation 1 represents the mathematical transfer function for the Figure 1 test circuit.

$$0 = \frac{d^2(i)}{dt^2} + \frac{R}{L} \times \frac{di}{dt} + \frac{1}{L \times C} \times i \quad \text{Eq. 1}$$

This configuration causes a momentary ESD event to occur at the Signal pin juncture to emulate one of the three ESD test signal events. The DUT Signal pin is either an input or output device pin. For these three ESD tests, the values of V_{ESD}, C, R, and L components vary to accomplish realistic ESD events (Table 1).

Table 1. ESD Events of HBM, MM, CDM

ESD Model		R	L	C	V_{ESD}
Human Body Model	HBM	1.5 kΩ	750 nH	100 pF	≥ 2kV
Machine Model	MM	20 Ω	750 nH	200 pF	100 – 200 V
Charged Device Model	CDM	20 Ω	5 nH	2 – 10 pF	200V – 1kV

In Table 1, these three models boil down to a series RLC circuit plus a pulse generator, but the circuit values and pulse characteristics differ between the models. However, all three tests produce a short, well-defined ESD pulse that results in current (I_{ESD}) levels comparable to those experienced during an actual ESD event.

The human-body model (HBM) characterizes an electronic device's susceptibility to electrostatic discharge (ESD) damage. The human body model is a model that simulates a human being's ESD path from the finger through a device-under-test (DUT) and then to ground. The ESD supply voltage (V_{ESD}) charges the capacitor in the test circuit. The standard HBM test includes a supply voltage of ±2 kV, a high-value resistance at 1 to 10 M?, and a capacitance of 100 pF.

The intention of the Machine Model (MM) is to create an HBM test with more severity. The charge capacitor (C) is intentionally larger (200 pF), and the charge source resistance is a very low value; 0 to 10Ω. This low-value resistor allows the ESD source to supply even higher currents than the HBM model. Although the intention of this model is to characterize machine ESD events associated with the end-user electronic assembly, it is not intended to embody the handlers used in semiconductor final testing and handling.

The Charge Device Model (CDM) can be a replacement test for a one-time popularly applied MM. This CDM test simulates the charge accumulated by an IC package or piece of manufacturing equipment as a device is processed through the final production operations. In the manufacturing process, opportunities to create static electricity exist within the device handling equipment. This is where IC devices slide down anti-static tubes or test handlers that build up a charge.

The current (I_{ESD}) injected into the DUT generates heat. The magnitude of the generated heat depends on the peak ESD pulse voltage, the capacitance, and DUT resistance. In HBM testing, IC failure modes typically manifest themselves as gate-oxide, contact spike, and junction damage.

ESD Test Comparison

The similar rise times of these three tests are about 10 ns, but the total duration of the HBM and MM tests exceed the CDM model by approximately 200 ns (Figure 2).

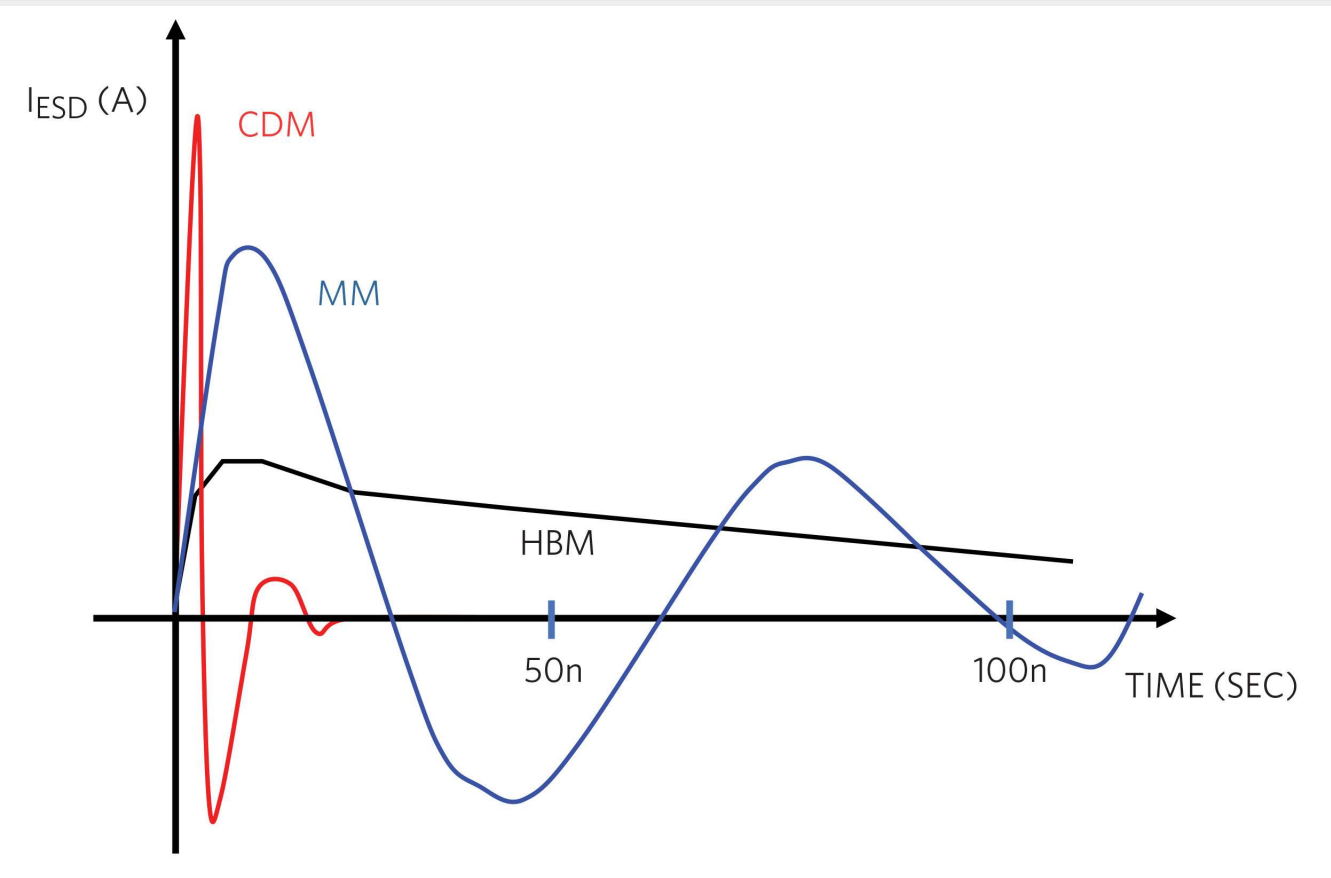

Figure 2. The CDM, MM, and HBM ESD current versus time tests.

Figure 2 shows the current (I_{ESD}) waveform characteristics for HBM, MM, and CDM ESD tests. Usually, the stress level of the HBM ESD test is approximately 10 times higher than the MM ESD test condition. Also, the protection voltage level for HBM tests typically is 2 kV, while for MM tests, it is 200 V and for CDM tests, it is 500 V. There is no correlation between CDM, HBM, or MM. Therefore, HBM and CDM tests are commonly used for ESD protection circuit tests. The longer duration of I_{ESD} causes an increase in the overheating of the on-chip ESD structures. HBM and MM test failures usually show up in the gate oxide or as junction damage.

Tables 2, 3, and 4 show the HBM, CDM, and MM ESD immunity classifications.

Table 2. ESD Immunity Classification for HBM

CLASS	Voltage Range
1	<250 V (fails for ESD pulse of 250 V)
1A	250 V to <500 V (passes 250 V and fails 500 V)
1B	500 V to <1000 V (passes 500 V and fails 1000 V)
1C	1000 V to <2000 V (passes 1000 V and fails 2000 V)
2	2000 V to <4000 V (passes 2000 V and fails 4000 V)
3A	4000 V to <8000 V (passes 4000 V and fails 8000 V)
3B	≥8000 V (passes 8000 V or above)

Table 3. ESD Immunity Classification for CDM

CLASS	Voltage Range
C1	<125 V (fails for ESD pulse of 125 V)
C2	125 V to <250 V (passes 125 V and fails 250 V)
C3	250 V to <500 V (passes 250 V and fails 500 V)
C4	500 V to <1000 V (passes 500 V and fails 1000 V)
C5	1000 V to <1500 V (passes 1000 V and fails 1500 V)
C6	1500 V to <2000 V (passes 1500 V and fails 2000 V)
C7	2000 V (passes 2000 V)

Table 4. ESD Immunity Classification for MM

CLASS	Voltage Range
M1	<100 V (fails for ESD pulse of 100 V)
M2	100 V to <200 V (passes 100 V and fails 200 V)
M3	200 V to <400 V (passes 200 V and fails 400 V)
M4	≥400 V (passes 400 V or above)

References

HFTA-16.0: ESD Protection for Bipolar Integrated Circuits

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