# Power Bus Decoupling Guidelines for Printed Circuit Boards with Closely Spaced Power Distribution Planes

**Applicable to:**

Multi-layer boards with power distribution planes spaced ~0.5 mm or less apart

## General Guidelines

- Multi-layer boards generally employ two types of decoupling capacitor. Large-valued "bulk" capacitors help to minimize the impedance of the power bus at low frequencies (e.g. below a few hundred kHz). Smaller "high-frequency" capacitors reduce the power bus impedance at higher frequencies (e.g. up to ~ 100 MHz on boards with closely spaced planes). At even higher frequencies, the power bus impedance is determined by the planes themselves.
- Boards typically have one or two large electrolytic bulk decoupling capacitors or they may employ half a dozen or more bulk decoupling capacitors in smaller packages. Either approach is effective and this decision is normally made based on size, cost and board-area constraints.
- The total value of the bulk decoupling is determined by the transient power requirements of the active devices on the board. Generally, the total bulk decoupling capacitance is 1 - 10 times the total high-frequency decoupling capacitance connected to the power bus.
- The high-frequency capacitors are often called "local" decoupling capacitors, but this is a misnomer. When the power and ground planes are closely spaced, all capacitors mounted on the surface of the board are "global" (i.e. they respond to changes in the voltage on the power planes due to all active device switching and do not favor one device over another). The inductance of their connection to the power distribution planes is far more critical than their nominal capacitance. Generally, smaller package sizes can be connected to the planes with a lower inductance than larger packages. Therefore, high-frequency decoupling capacitors should generally be as small (physically) as possible. The vias connecting these capacitors to the planes should be located as close to one another as possible.
- Choose the largest nominal capacitance available in a given package size. However, do not use capacitors that have a nominal capacitance less than the parallel plate capacitance that naturally occurs between the power and power-return planes [$C=\varepsilon A/d$]. A board made with FR-4 material containing one pair of power distribution planes spaced 0.25 mm (10 mils) apart has an interplane capacitance of approximately 16 pF/cm$^2$.
- The location of the decoupling capacitors is not critical because their performance is dominated by the inductance of their connection to the planes. At the frequencies where they are effective, they can be located anywhere within the general vicinity of the active devices [1].
- The maximum frequency at which the capacitors will be effective is proportional to the square root of the number of capacitors [1]. Therefore, high-speed circuit boards often have many high-frequency decoupling capacitors for every active device on the board.
- Connection inductance is determined by the loop area formed by the capacitor body, mounting pads, traces and vias (See: Estimating the connection inductance of a decoupling capacitor. (http://www.cvel.clemson.edu/emc/tutorials/estimating-L01/estimating-L01.html))

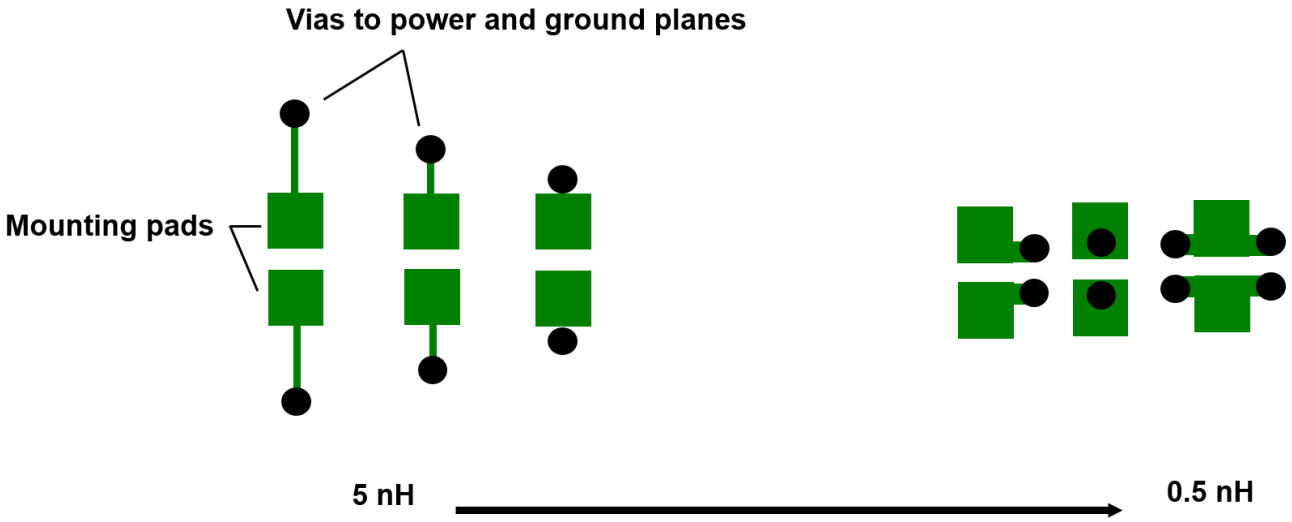
### To minimize connection inductance:

- Never use traces! Locate the vias adjacent to the mounting pads and near each other.
- If there is no room for the via adjacent to the pad, then move the whole capacitor. Capacitor location is not so important, but connection inductance is critical.

- Four vias (instead of two) can cut the connection inductance nearly in half when the via diameter is small relative to the mounting pad width.
- Mount all of the high-frequency decoupling capacitors on the face of the board nearest to the planes. Connection inductance is nearly proportional to the distance from the planes.
- Do not let high-frequency decoupling capacitors share a via with an active device.

# Examples

The figure below shows various examples of high-frequency decoupling capacitor connections to boards with closely spaced power distribution planes. Connections with lower inductance will be more effective at higher frequencies.




# References

[1] T. H. Hubing, J. L. Drewniak, T. P. Van Doren, and D. Hockanson, "Power bus decoupling on multilayer printed circuit boards (http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=385878&isnumber=8741&punumber=15&k2dockey=385878@ieeejrns&query=%28%28power+bus+decoupling+on+multilayer+printed+circuit+boards%29%3Cin%3Emetadata%29&pos=0)," *IEEE Trans. on Electromagnetic Compatibility*, vol. 37, no. 2, May 1995, pp. 155-166.

[2] M. Xu, T. Hubing, J. Chen, T. Van Doren, J. Drewniak and R. DuBroff, “Power-bus decoupling with embedded capacitance in printed circuit board design (http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=1180390&isnumber=26506&punumber=15&k2dockey=1180390@ieeejrns&query=%28%28decoupling+with+embedded+capacitance+in+printed+circuit+board+%29%3Cin%3Eti+%29&pos=0&access=no),”*IEEE Trans. on Electromagnetic Compatibility*, vol. 45, no. 1, Feb. 2003, pp. 22-30.

---



Back to Top