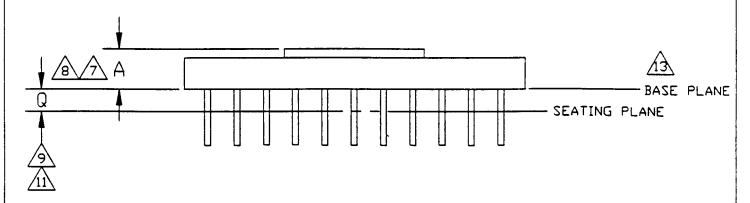


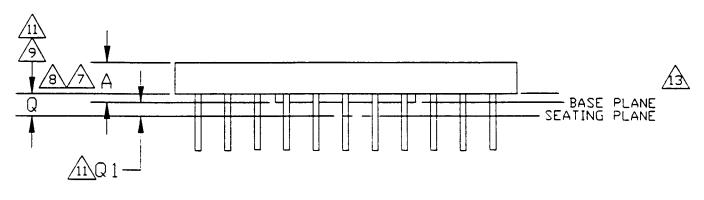
JEDEC SOLID STATE PRODUC OUTLINE	PIN GRID ARRAY FAMILY 100 INCH PITCH (LARGE DUTLINE) S-CPGA-P	ISSUE B	DATE JUNE 1993	M0-067	SHEET 1 of 8
			1993		

## FIGURE 2

CAVITY UP



CAVITY DOWN



3-Crua-r 2 1773	JEDEC SOLID STATE PRODUCT OUTLINE	PIN GRID ARRAY FAMILY ISSUE 100 INCH PITCH (LARGE OUTLINE) S-CPGA-P B	DATE JUNE 1993	M0-067	SHEET 2 of 8
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	MIN	NOM	MAX	Ť E	MIN	NOM	MAX	N	MIN	NOM	MAX	N - E	MIN	NOM	MAX	Ĭ E
D	.940	.960	.980	18	1.040		1.080	18	1.140	1.160	1.180	18		1.260	i	18
E	.940	.960	.980	18	1.040	1.060	1.080	18	1.140	1.160	1.180	18	1.240	1.260	1.280	18
M		9		4		10		4		11		4		12		4
N			81	5			100	5			121	5		<b>-</b>	144	5
Q	.045		.075	11	.045		.075	11	.045		.075	11	.045		.075	11
Q1	.025			11	.025			11	.025			11	.025			11
S		.000		21		.050		21		.000		21		.050		21
NOTE		1,2,3,6,9	,14,17													
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D	1.340	1.360	1.380	18	1.440	1.460	1.480	18	1.540	1.560	1.580	18	1.640	1.660	1.680	18
Ε	1.340	1.360	1.380	18	1.440	1.460	1.480	18	1.540	1.560	1.580	18	1.640	1.660	1.680	18
М		13		. 4		14		4		15		4		16		4
N	<b>-</b>		169	5			196	5			225	5			256	5
Q	.045		.075	11	.045		.075	11	.045		.075	11	.045		.075	11
Q1	.025			11	.025			11	.025			11	.025			11
S		.000		21		.050		21		.000		21		.050		21
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D	1.740	1.760	1.780	18	1.840	1.860	1.880	18	1.940	1,960	1.980	18	2.040	2.060	2.080	18
E		1.760		18	1.840			18	1.940	ł		1		2.060	2.080	18
M		17		4		1.000		4		19		4		20		4
N			289	5	<b>-</b>		324	5			361	5			400	5
Q	.045		.075	11	.045		.075	11	.045		.075	11	.045		.075	11
Q1	.025			11	.025			11	.025			11	.025			11
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JEDEC PIN GRID ARRAY FAMILY ISSUE DATE SOLID STATE PRODUCT .100 INCH PITCH (LARGE DUTLINE) - JUNE MO-OF								~ <del>~</del>		EET						
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D	2.440	2.460	2.480	18	3.040	3.060	3.080	18	3.840	3.860	3.880	18	4.440	4.460	4.480	18
E	2.440	2.460	2.480	18	3.040	3.060	3.080	18	3.840	3.860	3.880	18	4.440	4.460	4.480	18
M		24		4		30		4		38		4		44		4
N			576	5			900	5			1444	5			1936	5
Q	.045		.075	11	.045		.075	11	.045	<b></b>	.075	11	.045		.075	11
Q1	.025			11	.025			11	.025			11	.025			11
S		.050		21		.050		21		.050		21		.050		21
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D E	.940 .940	.960 .960	.980 .980	18 18	1.040 1.040		1.080 1.080	18 18	1.140 1.140	1.160 1.160	1.180 1.180	18 18	1	1.260 1.260	1	18 18
М		9		4		10		4		11		4		12		4
N			81	5			100	5			121	5			144	5
Q	.000		.000	11	.000		.000	11	.000		.000	11	.000		.000	11
Q1	.000		.000	11	.000		.000	11	.000	- <b></b>	.000	11	.000		.000	11
S		.000		21		.050		21		.000		21		.050		21
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<u> </u>	MIN	NDM	MAX	T E	MIN	NOM	MAX	E	MIN	NOM	MAX	τ Ε	MIN	NDM	MAX	Ē
D	1.340	1.360	1.380	18	1.440	1.460	1.480	18	1.540	1.560	1.580	18	1.640	1.660	1.680	18
E	1.340	1.360	1.380	18	1.440	1.460	1.480	18	1.540	1.560	1.580	18	1.640	1.660	1.680	18
M		13		4		14		4		15		4		16		4
N			169	5			196	5			225	5			256	5 /
Q	.000		.000	11	.000		.000	11	.000		.000	11	.000		.000	11
Q1	.000		.000	11	.000		.000	11	.000		.000	11	.000		.000	11
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L	MIN	NOM	MAX	Ε	MIN	NDM	MAX	T E	MIN	NOM	MAX	E	MIN	NDM	MAX	Ť E
D	1.740	1.760	1.780	18	1.840	1.860	1.880	18	1.940	1.960	1.980	18	2.040	2.060	2.080	18
E	1.740	1.760	1.780	18	1.840	1.860	1.880	18	1.940		1.980	18	2.040	2.060	2.080	18
M		17		4		18		4		19		4		20		4
N			289	5			324	5			361	5			400	5
Q	.000		.000	11	.000		.000	11	.000		.000	11	.000		.000	11
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L	MIN	NDM	MAX	0 T E	MIN	NDM	MAX	<u>-</u> ۲	MIN	NDM	MAX	T E	MIN	NDM	MAX	T E
D	2.440	2.460	2.480	18	3.040	3.060	3.080	18	3.840	3.860	3.880	18	4.440	4.460	4.480	18
E	2.440	2.460	2.480	18	3.040	3.060	3.080	18	3.840	3.860	3.880	18	4.440	4.460	4.480	18
M		24		4		30		4		38		4		44		4
N			576	5			900	5			1444	5			1936	5
Q	.000		.000	11	.000		.000	11	.000		.000	11	.000		.000	11
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L		C TINC			S	-CPGA-	<u>r</u>				1993	L				

	NOTES:					
1		Tolerancing per ANS	I Y14.5	M-1982.		,
2	Refer to appli	cable symbol list.				,
3		ion designation per		TANDARD	PROCEDURES AND	D
4		ber SPP-010, JESD 95	-1.			
4 5		the pin matrix size. the maximum allowabl	a numba	n of n:	n.c	
6		2 matrix sizes shown				
$\overline{A}$		includes the package				/ UD
		n configurations. (				у ар
<u> </u>		does not include hear				ures.
Δ		variations AA-AT mus				
د کے	_	major dimension of			•	
$\wedge$		are no standoffs on				
10	For variations	AA-AT, the seating p	olane is	s define	ed by the stand	loff
	surface facing	away from the ceram	c body	(outer	standoff surfo	ice).
$\wedge$	method of appl	BA-BT the seating pication and thereby	lane is	detine for no	a by the user	
<u>/1 i\</u>	Dimension "Q"	is measured from the	ceramic	c body <sup>-</sup>	to the outer st	and-
	off surface an	d is applicable to be	oth cav	ity up (	and cavity down	
		. Dimension "Q1" is r				
$\wedge$	only. (See Fig	ce and is applicable	to the	Cavity	down configure	tion
		be on .100 inch grid				
<i>,</i> ,		ne of pin to package		ace for	both cavity up	o and
$\overline{\wedge}$	down configura	tions. (See Figure 2	2, Pg. a	2)	, ,	
$\frac{14}{\lambda}$	See APPLICATIO	N NOTE.				
15	Pin tips shoul	d have a radius or cl	namfer.	See Al	PPLICATION NOTE	- - •
		allows a 750 microin		ck coat	ing for solder	
		See APPLICATION NOTE				
1/	here must be	some type of Al corne	er iden:	tificat = antin	ion on both top	o and
	of notches In	s of the package. ID pins, metallized man	rype i	or othe	nal and may col r features. The	1515i 2
$\wedge$		on each surface may 1				•
<u> 18</u>	There must be	.020 inch minimum spo	acing be	etween :	any two metal	
/ \		e package surface.				
		and "E" do not includ				า
		y not extend more the			•	
		ges of the package bo tection or identifico		nave c	namters for	
/ \	•	defines the maximum		or the	n:n brozo pode	
/\					prii bruze puus	•
·		d with respect to -	und	<u>- b - </u> ]	•	
22	All dimensions	are in INCHES.				
	JEDEC	PIN GRID ARRAY FAMILY	ISSUE	DATE		SHEET
2UL1I	STATE PRODUCT OUTLINE	.100 INCH PITCH (LARGE DUTLINE) S-CPGA-P	В	JUNE 1993	M0-067	7 of 8
			<u> </u>			L

## APPLICATION NOTES:

- A. For applications where a PGA package is used in a socket, the following requirements may apply:
  - a. Pin tips must have a radius or chamfer.
  - b. Minimum pin length (dimension "L") must be .120".
  - c. Maximum pin diameter including finish should be .020".
- B. For military applications the pin length (dimension "L") range may be restricted to .120"/.140".
- C. All variations are suitable for single and multichip applications.

JEDEC SOLID STATE PRODUCT OUTLINE	PIN GRID ARRAY FAMILY .100 INCH PITCH (LARGE DUTLINE)	ISSUE R	DATE JUNE	MD-067	SHEET 8 of 8
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