Tips for Optimal High Speed SPI Layout Routing

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If you have spent any time in the city you have probably ridden the bus at least once. True, it does not offer the freedom of driving your own vehicle, but it also does not require you to hunt aimlessly for a place to park once you arrive at your final destination. If you have ridden the bus a lot, like me, then you probably have also experienced when the buses get out of sync and you miss your connection. This asynchronous bus routing always happens at a bad time and you wind up late for work or an important appointment.

Asynchronous data transfer can also be a major problem for communicating between a microcontroller and peripherals. Although, this can be addressed by constantly sending start and stop bits with each transmission unit, this is not

efficient. A better approach is synchronous data transmission using a serial peripheral interface or SPI. For your SPI to be most effective, there are considerations aside from timing that must be considered. Let's take a look at how to optimize high speed SPI layout routing. But, first let's clearly define the SPI layout.

What is the High Speed SPI Layout?

Today, most electronic devices and systems are considered to be "smart" to some degree. In this context, smart means the system consists of a microcontroller, essentially a small computer on an IC chip, that can control how and when data or information is sent to or received from external components or devices. These external devices or components are referred to as peripherals. Peripherals are classified as one of three types based on their data transfer relationship with the microcontroller, as listed below:

Types of Peripherals

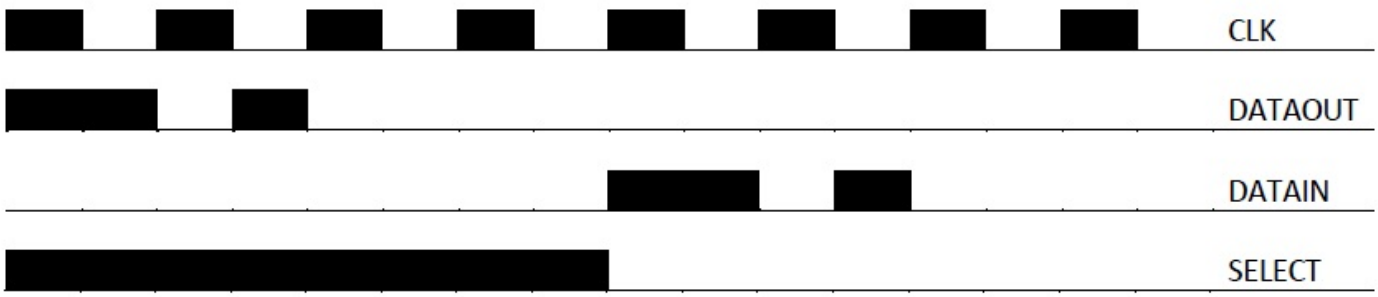
Peripheral Type	Common Components or Devices
Input device	Sends data or information to the microcontroller; such as a ROM module.
Output device	Receives data or information from the microcontroller; such as a LED display.
Input/Output device	Sends data or information to and receives data or information from the microcontroller; such as an SD memory card.

A microcontroller and its peripherals may be mounted on the same IC. In this case, routing is internal and not a design activity. However, when peripherals are external to the microcontroller IC, whether on the same PCB or interconnected via a cable, trace routing is necessary. This is where the SPI layout comes into play.

The serial parallel interface or SPI layout can be defined as the routing of traces between a microcontroller and a peripheral component or device. The layout includes separate data lines, a clock line and a control or select line.

In most cases, communication between microcontroller and peripherals is high-speed. Generally, high speed is taken to mean above 50MHz; however, high speed on a PCB is when the signal begins to be affected by reflections on the transmission line. A more accurate determination is obtained by dividing the signal propagation time for the trace length by the signal rise or fall time. If this ratio is greater 1.0, then **your trace is in the high speed domain**.

In the figure below, an example of the relationship between signals for a high speed SPI layout are shown.



High speed SPI signal plots

As shown, your layout for each peripheral typically includes the following:

CLK: this ensures synchronization between the devices.

DATAOUT: for data transfer from the microcontroller.

DATAIN: for data transfer to microcontroller.

SELECT: this is for activating/deactivating the peripheral.

In contrast to the unidirectional data transfer shown above, some layouts utilize a single bidirectional data line; however, the clock and select lines are still separate. When routing the SPI layout, good trace routing guidelines should be applied; however, there are additional considerations that must be addressed to optimize your layout for manufacturing and operation.

How to Optimize Your High Speed SPI Layout

Fast, reliable communication between the microcontroller and peripheral(s) is the motivation for opting to implement an SPI layout as opposed to slower and sometimes redundant asynchronous data transfer methods. Although, the scheme itself inherently contributes to the advantages of SPI over this alternative, there are disadvantages that can be improved to achieve the best or an optimal high speed SPI layout. One major disadvantage is the need for multiple lines, which can mean more space on your board and present trace routing challenges. However, there are tips, as listed below, that can help you address these issues.

High Speed SPI Layout Routing Tips:

Tip 1: Keep all SPI layout traces as short as possible

The need for multiple lines between the microcontroller and peripheral makes component mounting more of an issue and they should be placed as close together as possible to minimize trace lengths.

Tip 2: Keep all SPI layout traces the same length

Your **SPI traces are not differential pairs**; however, treating them as such is advantageous for your SPI layout design. In particular, having data transfer lines of the same length, copper weight and impedance are recommended.

Tip 3: Use a constant impedance on all traces

For high frequency transmission, consistent impedance is critical for the best signal integrity. This may be the **common 50 Ω impedance** used for many connectors for board interconnection or some other fixed impedance calculated specifically for your board.

Tip 4: Select materials to aid signal integrity

For most board designs, the often used FR-4 is sufficient. For high speed design, your **material selection** is more important as the dielectric constant will impact impedances and signal propagation.

By applying the tips above, you can create the best high speed SPI layout for your design. For manufacturability and operational reliability these design choices must adhere to your contract manufacturer's (CM's) DFM rules and guidelines, as well.

When routing your SPI layout, it is a distinct advantage to have an innovative and comprehensive PCB design software tool at your disposal. There is no better option than Cadence's flagship Allegro software package, which includes the ability to route and analyze your traces in 3-D, as shown below.

3D Trace routing analysis

With this and other **PCB design and analysis capabilities** you can create your optimal SPI layout quickly. And using in-design **visual feedback and controlled trace automation**you can be assured that your design is manufacturable.

If you're looking to learn more about how Cadence has the solution for you, **talk to us and our team of experts**.