

## **VARIATIONS** ALL DIMENSIONS SHOWN IN INCHES



SYM	AA			NO	
SYMBOL	MIN	NOM	MAX	0 T E	
Α	.060	.070	.080		
b	.022	.025	.028		
Ь1	.006	.014	.022	2	
b2	.030			7	
D	.665	.675	.685	4	
D1 E					
	.340	.350	.360	4	
е					
h		5			
L	.045	.050	.055		
L1	.080	.090	.100		
L2	.003	.009	.015	2	
N		6			
N1		9			
N2		9			
N3		9			
N4		9			
NOTE	1, 3	. 8			
REF	10-3				
ISSUE	Α				

## NOTES:

- 1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
- 2. Metallized castellations shall be connected to Plane 1 terminals. 🖄 Index Area: An identification mark shall be located adjacent to pin one within the shaded area shown. Plane 1 terminal identification may be an extension of the length of the metallized terminal which shall not be wider than the b dimension.



1 The cover shall not extend beyond the edges of the body.  $\overline{ rac{ }{ ext{ } ext{ } ext{ } ext{ }} }$  The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option.

- 6. N indicates total number of terminal positions.
- 7. Unless otherwise specified, a minimum clearance of .015 inch shall be maintained between all metallized features (e.g., lid, castellation, terminals, thermal pads, etc.).
- 8. Solder finish is optional with a maximum allowable thickness of .007 inch. Measurement of dimensions A, b1, and L2 may be made prior to solder application.
- 5 For terminal identification purposes only. Terminals between N1 and N2, and between N3 and N4 are omitted if values for, N1, N2, N3 and N4 are listed on the table.

JEDEC SOLID STATE PRODUCT OUTLINE	TITLE: R-CDCC-N LEADLESS SMALL OUTLINE	ISSUE:	DATE:		SHEET:
	CERAMIC CHIP CARRIER .350" BODY, .050" PITCH	A	JUNE 1993	MO-144	2 OF 2