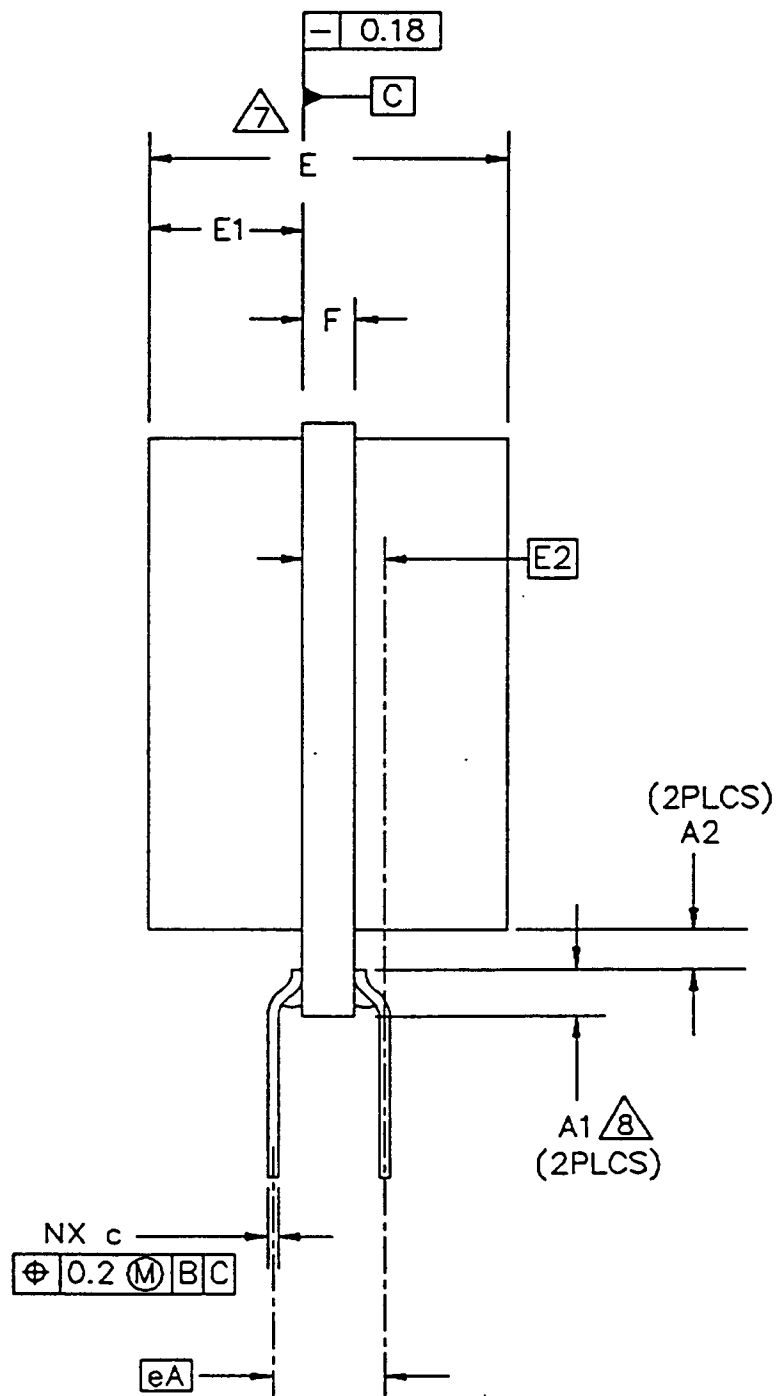


|  |  |             |               |        |                 |
|--|--|-------------|---------------|--------|-----------------|
| JEDEC<br>SOLID STATE PRODUCT<br>OUTLINE  | THIS REGISTERED OUTLINE HAS BEEN PREPARED BY THE JEDEC<br>JC-11 COMMITTEE AND REFLECTS A PRODUCT WITH ANTICIPATED USAGE<br>IN THE ELECTRONICS INDUSTRY; CHANGES ARE LIKELY TO OCCUR. |             |               |        |                 |
| TITLE:<br>72 PIN STAGGERED DUAL INLINE<br>MODULE (SDIM) FAMILY 1.27 LEAD CENTERS | JESD - 30 DESIGNATOR   | ISSUE:<br>A | DATE:<br>8/96 | MO-185 | SHEET<br>1 OF 3 |







VIEW A-A

|   |   |                    |                       |               |                         |
|---|---|--------------------|-----------------------|---------------|-------------------------|
| <p>JEDEC<br/>SOLID STATE PRODUCT<br/>OUTLINE</p>  | <p>THIS REGISTERED OUTLINE HAS BEEN PREPARED BY THE JEDEC<br/>JC-11 COMMITTEE AND REFLECTS A PRODUCT WITH ANTICIPATED USA<br/>IN THE ELECTRONICS INDUSTRY; CHANGES ARE LIKELY TO OCCUR.</p> |                    |                       |               |                         |
| <p>TITLE:<br/>72 PIN STAGGERED DUAL INLINE<br/>MODULE (SDIM) FAMILY 1.27 LEAD CENTERS</p> | <p>JESD - 30 DESIGNATOR</p>   | <p>ISSUE<br/>A</p> | <p>DATE:<br/>8/96</p> | <p>MO-185</p> | <p>SHEET<br/>2 OF 3</p> |

| SYMBOL | VARIATIONS (ALL DIMENSIONS SHOWN IN MILLIMETERS) |       |       | NOTE |
|--------|--|-------|-------|------|
|        | AA   |       |       |      |
|        | MIN  | NOM   | MAX   |      |
| A      | 14.35  | 14.50 | 14.65 |      |
| A1     | 1.25   | 1.90  | 2.25  |      |
| A2     | 0.65   |       |       | 7    |
| b      | .35  |       | .55   |      |
| c      | .15  |       | .35   |      |
| b1     | .35  | .45   | .50   |      |
| c1     | .15  | .25   | .30   |      |
| D      | 97.50  | 97.65 | 97.80 |      |
| E      |  |       | 8.90  |      |
| E1     |  |       | 3.55  |      |
| E2     | 1.85 BSC.  |       |       |      |
| e1     | 2.54 BSC.  |       |       |      |
| e2     | 1.27 BSC.  |       |       |      |
| e3     | 91.44 REF.                                       |       |       |      |
| e4     | 3.175 BSC.                                       |       |       |      |
| e5     | 6.35 BSC.  |       |       |      |
| eA     | 2.55 BSC.  |       |       |      |
| F      | 1.00   | 1.15  | 1.30  |      |
| G      | .60  | 1.90  | 3.15  |      |
| G1     | .60  | 1.90  | 3.15  |      |
| L      | 3.15   | 3.80  | 4.45  |      |
| N      | 72 PINS  |       |       | 4    |
| NOTE   | 1, 2, 3  |       |       |      |
| REF.   | 14-022   |       |       |      |
| ISSUE  | A  |       |       |      |

NOTES:

1. REFER TO APPLICABLE SYMBOL LIST.
  2. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M - 1994.
  3. ALL DIMENSIONS ARE IN mm.
  4. N IS MAXIMUM QUANTITY OF LEAD POSITIONS.
-  PIN 1 IDENTIFIER MUST BE LOCATED IN THIS AREA.  
 PIN NUMBERING: ODD NUMBERED PINS LOCATED ON BACK SIDE AND EVEN NUMBERED PINS LOCATED ON FRONT SIDE.  
 DIMENSIONS APPLICABLE WHEN COMPONENTS MOUNTED ON BOTH SIDES.  
 DIMENSION A1 IS MEASURED FROM PANEL BOTTOM

|  |  |  |            |               |                 |
|--|--|--|------------|---------------|-----------------|
| JEDEC<br>SOLID STATE PRODUCT<br>OUTLINE  |  | THIS REGISTERED OUTLINE HAS BEEN PREPARED BY THE JEDEC JC-11 COMMITTEE AND REFLECTS A PRODUCT WITH ANTICIPATED USAGE IN THE ELECTRONICS INDUSTRY; CHANGES ARE LIKELY TO OCCUR. |            |               |                 |
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