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1 PURPOSE

This specification details the minimum requirements for the fabrication of all printed circuit boards (PCB's) delivered to any division of Plexus. It also defines the criteria for acceptability of those PCB's. All Specifications outlined in this document are requirements, unless otherwise stated.

2 SCOPE

This specification is applicable to all PCB suppliers that quote, manufacture and supply printed circuit boards for any division of Plexus. In the event of a conflict between this specification and any other applicable document, section 3. ORDER OF DOCUMENT PRECEDENCE shall apply.

3 ORDER OF DOCUMENT PRECEDENCE

In case of conflict between the requirements of the procurement document(s), the text described in this document, including references cited herein and those defined in any other applicable document, the following order of precedence shall apply:

- Purchase Order including applicable Q-Codes
- PCB Fabrication Drawing
- Plexus Customer Specification
- Plexus PCB Fabrication Specification G9000-3 (This document)
- The latest version of the following Specifications where applicable:

IPC-A-600	Acceptability of Printed Circuit Boards
IPC-4101	Specification for Base Materials for Rigid and Multilayer Printed Boards
IPC-6011	Generic Performance Specification for Printed Boards
IPC-6012	Qualification and Performance Specification for Rigid Printed Boards
IPC-T50M	Terms and Definitions for Interconnecting and Packaging Electronic Circuits
IPC-7711	Rework, Modification and Repair of Electronic Assemblies
J-STD-003	Solderability Tests for Printed Boards
J-STD-033	IPC/JEDEC Standard for Handling, Packing, Shipping, and use of Moisture/Reflow Sensitive Surface-Mount Devices
IPC-4552	Performance Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Boards
IPC-6013	Qualification and Performance Specification for Flex and Rigid Flex Printed Boards
IPC-6018	Microwave End Product Board Inspection and Test
IPC-SM-840	Qualification and Performance of Polymer Coating (Solder Mask)
IPC-1601	Printed Board Handling and Storage
IPC-TM-650	Test Methods Manual
J-STD-020	Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices
UL-94	Test for Flammability of Plastic Materials
UL-796	Printed Wiring Boards
5501	Plexus Materials Specification – Supplier Requirements for Compliance to RoHS

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4 ACRONYMS, TERMS & DEFINITIONS

in “	Inch
Mil	1/1000 inch
µin	Micro Inch
mm	Millimeter
µm	Micron
C&S	Coverage and Solderable as per J-STD-003
HASL	Hot Air Solder Level
LFHASL	Lead Free Hot Air Solder Level
IPC	Association Connecting Electronics Industries
MOT	Manufacturing Operating Temperature
MTO	Made to Order
OSP	Organic Solder Preservative
PCB	Printed Circuit Board
TDR	Time Domain Reflectometry
Tg.	Glass Transition Temperature
Td.	Decomposition Temperature
UL	Underwriter’s Laboratories
SMOBC	Solder mask Over Bare Copper
Supplier	Company which is fabricating the PCB’s

5 SUPPLIER RESPONSIBILITY

During the quotation stage and prior to accepting an order, it is the responsibility of the PCB supplier to:

- Ensure they can meet all requirements of this specification
- Inspect all artwork/CAD data and documentation released from Plexus, prior to manufacturing
- Ensure the electronic data is sufficient to define and auto-create all applicable features
- Inform Plexus of any requirements within this specification that cannot be met or that greatly affect cost and or schedule prior to fabrication of the PCB
- Submit copies of any post processed Gerber data including Stencil files for record retention if available

6 PRODUCT / PROCESS CHANGE

Supplier shall obtain written approval from Plexus prior to making any modifications to the supplied product (PCB’s) or to the manufacturing process used to fabricate the PCB’s. This requirement is not limited to form, fit or function and includes changes to:

- Layout, construction and design
- Base material, Pre-preg (type, style, manufacturer, grade)
- Artwork
- Netlists
- Machining (routing, profile, blanking, drill diameters)
- Processing chemistry
- Applied chemistry (Solder mask, Legend, Carbon etc.)
- Manufacturing location (Including subcontracting of part processes)

6 months advance change notification is required and the change shall not be implemented until formal change approval has been granted in writing from Plexus following the Plexus PCN procedure.

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7 VENDOR UL REQUIREMENTS

The PCB supplier shall be UL registered and hold valid UL listing status for each of the technologies being produced. The product (PCB's) shall also be manufactured such that they meet the detailed requirements highlighted in the following sections of this document.

- Section 11.1.7 Flame Class
- Section 11.1.8 Manufacturing Operating Temperature (MOT)
- Section 11.9 Supplier ID Markings

UL Listing implies recognition of the PCB manufacturing process as well as recognition of the PCB materials.

8 PERFORMANCE CLASS

This specification establishes the general performance requirements of PCB's. Based on the IPC-6010 Board Performance documents series and unless otherwise stated within this document the default performance class to be adhered to shall be **CLASS 2**

9 ROHS / WEEE DIRECTIVES

Any PCB specified as RoHS or Lead-Free shall comply with the RoHS directive 2011/65/EU and WEEE directive 2012/19/EU and as defined in Plexus Material Specification #5501.

10 ARTWORK ENHANCEMENTS

Supplier may enhance or modify the supplied or generated artwork in order to increase internal process efficiency, to enable more capable manufacturing or to follow best manufacturing practices in the following instances only:

10.1 TEAR DROPPING OF PADS

Supplier may enhance the supplied artwork by modifying or "tear dropping" the through-hole pads on any circuit layer which does not meet the supplier's manufacturing capabilities. The minimum space defined by the fabrication drawing shall be maintained. Solder mask on the teardrop portion of the pad is acceptable.

10.2 RoHS/PB-Free / ImmAg

If a PCB is specified as RoHS/Lead-free Assembly compliant, or if Immersion Silver (ImmAg) is the specified surface finish, teardrops are required on all external layer exposed PTH pads. The teardrop shape shall extend beyond or under solder mask.

10.3 COPPER THIEVING/ROBBING/HATCHING

PCB breakaway areas are non-functional and as such the Supplier may alter the layer plots to add or remove copper as long as the modifications:

- Do not affect any TDR test coupons
- Maintain a minimum clearance of 0.1" from any designated bar code area
- Maintain a 0.1" radius clearance from fiducial targets, on all layers

It is not allowed to add any copper thieving, dot robbing or cross hatching to any circuit areas without formal written approval from Plexus buyer. Layer plots and or modified Gerber data must be provided prior to requesting approval utilizing the suppliers EQ/TQ process.

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10.4 NON-FUNCTIONAL INNER-LAYER PAD REMOVAL

Non-functional inner layer pads are the plated through-hole pads, on each inner layer, not attached to a signal trace or copper plane. Formal written approval must be received prior to making such changes. Supplier shall identify, document and request change permission via their EQ/TQ process.

10.5 SILKSCREEN CLIPPING

Clipping of silkscreen, up to 0.008" maximum from pads/lands, shall be performed on supplied silkscreen data to provide adequate legibility and clearance from exposed PCB copper.

11 FINISHED PCB REQUIREMENTS**11.1 BASE MATERIAL**

Base materials, herein also referred to as pre-preg or laminate shall comply with IPC-4101 **Specification for Base Materials for Rigid and Multilayer Printed Boards**. Laminates and pre-pregs shall be manufactured from FR-4 Glass Epoxy; the following reinforcement styles shall be used:

- E-Style Glass
- S-Style Glass
- Aramid
- Quartz

11.1.1 BASE MATERIAL PROPERTIES – STANDARD PRODUCTS

Standard Products are defined as any conventional (Non-HDI) PCB constructed with <8 layers, which are < 2.0mm/78mil thick and which are drilled with a minimum hole diameter $\geq 0.3\text{mm}/12\text{mil}$.

- Glass Transition Temperature (T_g) = $150^\circ\text{C} \pm 5^\circ\text{C}$
- Decomposition Temperature (T_d) $\geq 325^\circ\text{C}$
- Time to Delamination T-288 ≥ 5 minutes
- Coefficient of Thermal Expansion (CTE) Z-axis ($50^\circ\text{C} - 260^\circ\text{C}$) $\leq 3.5\%$
- Max. Moisture Absorption level $\geq 0.5\text{mm}$ (t) = 0.5% wt.

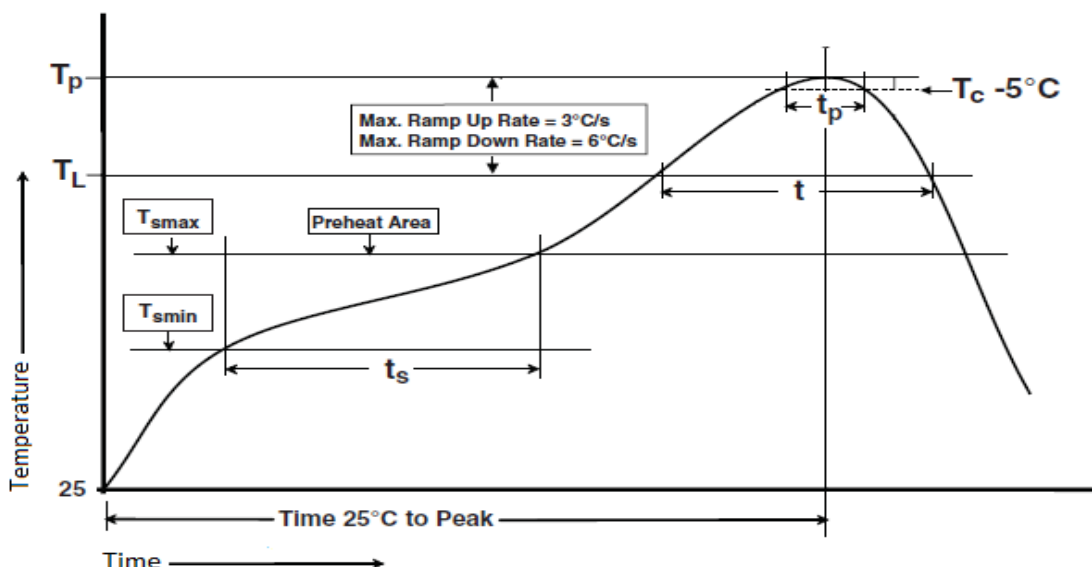
11.1.2 BASE MATERIAL PROPERTIES – ADVANCED PRODUCTS

Advanced Products are defined as any PCB constructed with ≥ 8 layers, or which $\geq 2.0\text{mm}/78\text{mil}$ thick or which are drilled with a minimum hole diameter $< 0.3\text{mm}/12\text{mil}$. Advanced Product classification will also apply to any design containing a BGA, CGA, or Copper layer $> 4\text{oz}$, $140\mu\text{m}$

- Glass Transition Temperature (T_g) = $170^\circ\text{C} \pm 5^\circ\text{C}$
- Decomposition Temperature (T_d) $\geq 340^\circ\text{C}$
- Time to Delamination T-288 ≥ 5 minutes
- Coefficient of Thermal Expansion (CTE) Z-axis ($50^\circ\text{C} - 260^\circ\text{C}$) $\leq 3.0\%$
- Moisture Absorption level $\geq 0.5\text{mm}$ 0.5% wt. max

11.1.3 BASE MATERIAL PROPERTIES - IR REFLOW CYCLES (Sn-Pb and Pb-Free)

Unless otherwise specified, finished printed circuit boards are required to withstand six (6) cycles of IR reflow at either the Sn-Pb or Pb-free soldering process profile as specified in IPC/JEDEC J-STD-020E and as depicted below:



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Min (T _{smin})	100 °C	150 °C
Temperature Max (T _{smax})	150 °C	200 °C
Time (t _s) from (T _{smin} to T _{smax})	60 -120 seconds	60 -120 seconds
Ramp-up rate (T _L to T _p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T _L)	183 °C	217 °C
Time (t _L) maintained above (T _L)	120 - 150 seconds	120 - 150 seconds
Time (t _p) within 5 C of the specified classification temperature (T _c)	20 seconds	30 seconds
Ramp-down rate (T _p to T _L)	6 °C/second max	6 °C/second max
Time 25 C to peak temperature	6 minutes max	8 minutes max

11.1.4 BASE MATERIAL PROPERTIES – METAL PLANES/CORES

Internal or external metal planes and/or metal core substrate shall conform to IPC-6012 with the following exception for Copper-Invar-Copper (CIC)

CIC shall be 0.006” thick with a 12.5% - 75% - 12.5% Copper – Invar – Copper construction.

11.1.5 BASE MATERIAL PROPERTIES – COPPER FOILS

Copper foil shall be Type E3 HTE conforming to IPC-4562. Resin coated RCC foil shall conform to IPC-4563

11.1.6 MINIMUM DIELECTRIC THICKNESS

Unless otherwise specified, the minimum dielectric thickness shall be 0.0035" (0.09mm). In instances where thin laminates are specified <0.0035" then preference shall be given to low profile coppers

11.1.7 FLAME CLASS

Unless otherwise specified and verifiable through the UL Recognized Component Directory, Rigid PCB's <13.0mm thick shall conform to UL 94 **"Standard for Tests for Flammability of Plastic Materials for Parts in Devices and Appliances"** and achieve the minimum classification of V-0. In addition to UL94 V-0 requirements Rigid PCB' shall also conform to UL 796. Flex and Flex Rigid PCB's shall conform to UL 796F.

11.1.8 MAXIMUM OPERATING TEMPERATURE (MOT)

Minimum UL Recognition = 130°C MOT.

11.2 CONSTRUCTION

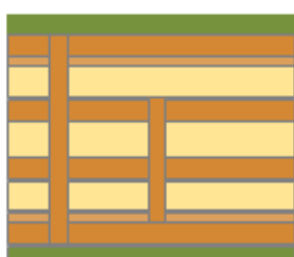
The PCB fabrication drawing and/or supplied data shall be referenced to determine the PCB layer stack-up details. If not provided or if a free build is specified then the supplier may propose their own construction as long as the following criteria is met:

- Construction must be symmetrical and balanced
- Multilayer builds start with maximum possible core thickness
- All FR4 laminates and pre-preg used is of NEMA grade with UV Blocking
- Teflon laminates shall be used for High Frequency applications
- Final construction shall be approved by Plexus

11.2.1 EXAMPLE CONSTRUCTIONS

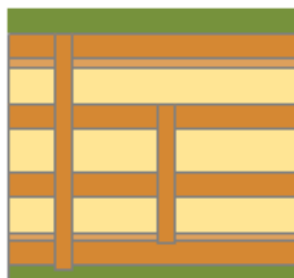
The following pictures are examples of symmetrical builds, please note that 7628 pre-pregs while acceptable are seldom used due to the High Glass Low Resin content. MIL values are rounded up:

4 Layer 1.0mm/39.37 Mil (t)



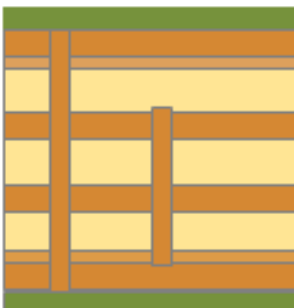
	Micron	Mil
Soldermask - Green Matte	25	1
Plated Cu	25	1
Base or Foil	18	0.69
7628HR Pre-Preg	224	8.8
Base or Foil	35	1.38
0.36 Tg 150 1oz Core	360	14
Base or Foil	35	1.38
7628HR Pre-Preg	224	8.8
Base or Foil	18	0.69
Plated Cu	25	1
Soldermask - Green Matte	25	1

4 Layer 1.2mm/47.24 Mil (t)



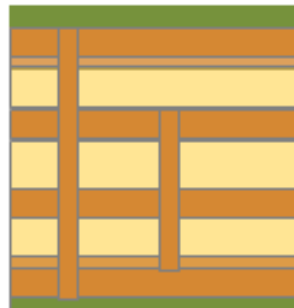
	Micron	Mil
Soldermask - Green Matte	25	1
Plated Cu	25	1
Base or Foil	18	0.69
7628SP Pre-Preg	190	7.5
Base or Foil	35	1.38
0.61mm Tg 150 1oz Core	610	24
Base or Foil	35	1.38
7628SP Pre-Preg	190	7.5
Base or Foil	18	0.69
Plated Cu	25	1
Soldermask - Green Matte	25	1

4 Layer 1.5mm/59 Mil (t)



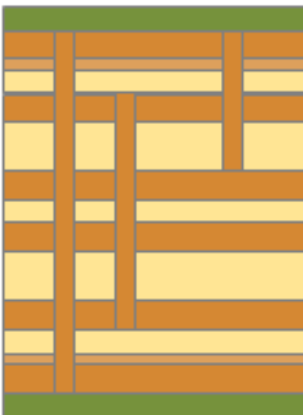
	Micron	Mil
Soldermask - Green Matte	25	1
Plated Cu	25	1
Base or Foil	18	0.69
7628SP Pre-Preg	178	7
Base or Foil	35	1.38
1mm Tg 150 1oz Core	1000	40
Base or Foil	35	1.38
7628SP Pre-Preg	178	7
Base or Foil	18	0.69
Plated Cu	25	1
Soldermask - Green Matte	25	1

4 Layer 1.6mm/63.0 Mil (t)

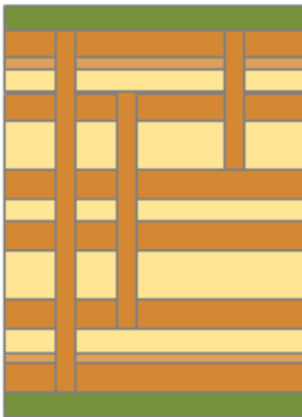


	Micron	Mil
Soldermask - Green Matte	25	1
Plated Cu	25	1
Base or Foil	18	0.69
2116LG Pre-Preg	109	4.3
Base or Foil	35	1.38
1.2mm Tg150 1oz Core	1200	47
Base or Foil	35	1.38
2116LG Pre-Preg	109	4.3
Base or Foil	18	0.69
Plated Cu	25	1
Soldermask - Green Matte	25	1

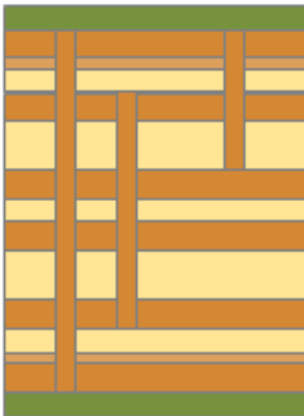
6 Layer 1.0mm/39.37Mil (t)

	Micron	Mil
		
Soldermask - Green Matte	25	1
Plated Cu	25	1
Base or Foil	18	0.69
1080LG Pre-Preg	76	3
Base or Foil	35	1.38
0.2mm Tg150 1oz Core	191	7.5
Base or Foil	35	1.38
7628SP Pre-Preg	190	7.5
Base or Foil	35	1.38
0.2mm Tg150 1oz Core	191	7.5
Base or Foil	35	1.38
1080LG Pre-Preg	76	3
Base or Foil	18	0.69
Plated Cu	25	1
Soldermask - Green Matte	25	1

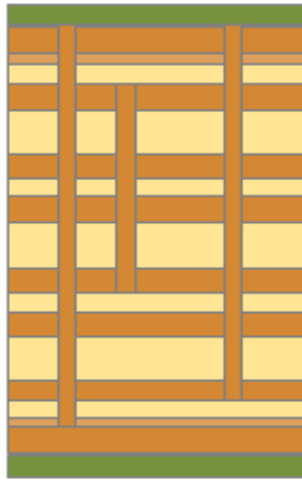
6 Layer 1.2mm/47.24Mil (t)

	Micron	Mil
		
Soldermask - Green Matte	25	1
Plated Cu	25	1
Base or Foil	18	0.69
7628LG Pre-Preg	178	7
Base or Foil	35	1.38
0.2mm Tg150 1oz Core	191	7.5
Base or Foil	35	1.38
7628LG Pre-Preg	178	7
Base or Foil	35	1.38
0.2mm Tg150 1oz Core	191	7.5
Base or Foil	35	1.38
7628LG Pre-Preg	178	7
Base or Foil	18	0.69
Plated Cu	25	1
Soldermask - Green Matte	25	1

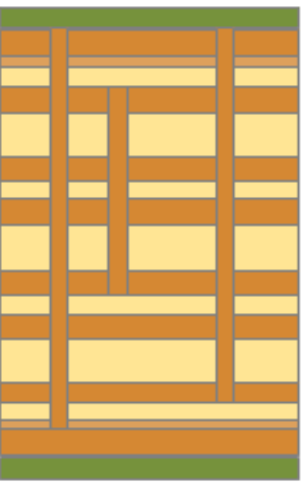
6 Layer 1.6mm/63 Mil (t)

	Micron	Mil
		
Soldermask - Green Matte	25	1
Plated Cu	25	1
Base or Foil	18	0.69
7628LG Pre-Preg	178	7
Base or Foil	35	1.38
0.36mm Tg150 1oz Core	360	14
Base or Foil	35	1.38
7628LG Pre-Preg	178	7
Base or Foil	35	1.38
0.36mm Tg150 1oz Core	360	14
Base or Foil	35	1.38
7628LG Pre-Preg	178	7
Base or Foil	18	0.69
Plated Cu	25	1
Soldermask - Green Matte	25	1

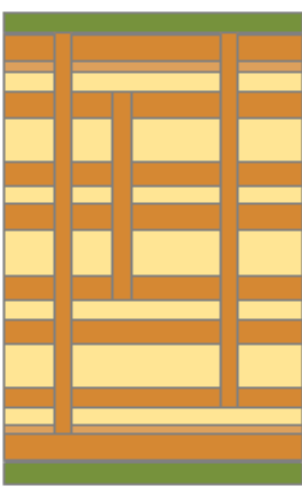
8 Layer 1.0mm/39.37Mil (t)

	Micron	Mil
		
Soldermask - Green Matte	25	1
Plated Cu	25	1
Base or Foil	18	0.69
1080LG Pre-Preg	76	3
Base or Foil	35	1.38
0.18mm Tg170 1oz Core	177	4.5
Base or Foil	35	1.38
1080LG Pre-Preg	76	3
Base or Foil	35	1.38
0.18mm Tg170 1oz Core	177	4.5
Base or Foil	35	1.38
1080LG Pre-Preg	76	3
Base or Foil	35	1.38
0.18mm Tg170 1oz Core	177	4.5
Base or Foil	35	1.38
1080LG Pre-Preg	76	3
Base or Foil	18	0.69
Plated Cu	25	1
Soldermask - Green Matte	25	1

8 Layer 1.2mm/47.24Mil (t)

	Micron	Mil
		
Soldermask - Green Matte	25	1
Plated Cu	25	1
Base or Foil	18	0.69
1080LG Pre-Preg	76	3
Base or Foil	35	1.38
0.19mm Tg170 1oz Core	191	7.5
Base or Foil	35	1.38
1080LG Pre-Preg	76	3
Base or Foil	35	1.38
0.19mm Tg170 1oz Core	191	7.5
Base or Foil	35	1.38
1080LG Pre-Preg	76	3
Base or Foil	35	1.38
0.19mm Tg170 1oz Core	191	7.5
Base or Foil	35	1.38
1080LG Pre-Preg	76	3
Base or Foil	18	0.69
Plated Cu	25	1
Soldermask - Green Matte	25	1

8 Layer 1.6mm /63.0Mil (t)

	Micron	Mil
		
Soldermask - Green Matte	25	1
Plated Cu	25	1
Base or Foil	18	0.69
1080LG Pre-Preg	178	7
Base or Foil	35	1.38
0.19mm Tg170 1oz Core	191	7.5
Base or Foil	35	1.38
1080LG Pre-Preg	178	7
Base or Foil	35	1.38
0.19mm Tg170 1oz Core	191	7.5
Base or Foil	35	1.38
1080LG Pre-Preg	178	7
Base or Foil	35	1.38
0.19mm Tg170 1oz Core	191	7.5
Base or Foil	35	1.38
1080LG Pre-Preg	178	7
Base or Foil	18	0.69
Plated Cu	25	1
Soldermask - Green Matte	25	1

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11.3 GENERAL PCB CONDITIONS

DESCRIPTION	Standard/Value/Method	Tolerance/Specification	Notes
Board Thickness	<1.0mm for example: 0.4, 0.5, 0.6, 0.8 > 1.0mm for example: 1.0, 1.2, 1.4, 1.6, 2.0mm	+/- 0.1mm +/- 10%	Measurement to be taken SMOBC, if gold edge contacts are present then measure center of contact area.
Warp / Bow & Twist	IPC-TM-650 2.4.22	0.75% of diagonal	Bow correction not permitted
Board Edge Requirements	Visual Acceptance	IPC-A-600	
Layer – Layer Registration	Measurement	+/- 0.005"	Alignment of patterns.
Datum Hole to PCB Edge	Measurement	+/- 0.010"	
Datum to Routed Slot	Measurement	+/- 0.010"	
Datum to V-Score Location	Measurement	+/- 0.010"	
Radius Outline Corners	Measurement	≥ 0.508mm	
Datum Hole to Drilled Hole	Measurement	+/-0.004"	
Material Utilization (Array)	85% Minimum		Multi up PCB arrays must achieve a minimum of 85% material utilization
Material Tg. Tolerance	Tg 150, Tg170, Tg180	+/- 5° C	

11.4 CONDUCTORS

11.4.1 Finished Conductor Width & Spacing

Any combination of edge roughness, nicks, pinholes, scratches, etc. **shall not** reduce the conductor width or the conductor space by more than 20% or 0.002", whichever minimum value is less.



11.4.2 Minimum Internal Layer Foil & Plated Copper Thickness

If the internal conductor thickness is specified by foil weight, then the minimum conductor thickness including plated copper and after processing shall be in accordance with IPC-6012 and as depicted in the table below: Processing allowances as per IPC-4562 are allowed. When a minimum copper thickness is specified then the conductor shall meet or exceed that minimum amount.

Weight	Minimum Cu (IPC-4562 less 10%)		Minimum Final Finish after processing	
1/8 oz. 5.1µm	4.6µm	181µin	3.1µm	122µin
1/4 oz. 8.5µm	7.7µm	303µin	6.2µm	244µin
3/8 oz. 12.0µm	10.8µm	425µin	9.3µm	366µin
1/2 oz. 17.1µm	15.4µm	606µin	11.4µm	449µin
1 oz. 34.3µm	30.9µm	1217µin	24.9µm	980µin
2 oz. 68.6µm	61.7µm	2429µin	55.7µm	2193µin
3 oz. 102.9µm	92.6µm	3646µin	86.6µm	3409µin
4 oz. 137.2µm	123.5µm	4862µin	117.5µm	4626µin
> 4 oz. 137.2µm	IPC-4562 value less 10% reduction		6µm (236 µin) below min thickness of calculated 10% reduction of foil thickness in IPC-4562	

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11.4.3 Minimum External Surface Conductor Thickness

The minimum total copper thickness inclusive of foil and plating, after processing shall be in accordance with IPC-6012 and as depicted in the table below. When a minimum copper thickness is specified then the conductor shall meet or exceed that minimum amount.

Starting Copper Weight	Minimum Surface Conductor Thickness after Processing			
	Class 1 & 2		Class 3	
1/8 oz.	23.1µm	909µin	28.1µm	1106µin
1/4 oz.	26.2µm	1031µin	31.2µm	1228µin
3/8 oz.	29.3µm	1154µin	34.3µm	1350µin
1/2 oz.	33.4µm	1315µin	38.4µm	1512µin
1 oz.	47.9µm	1886µin	52.9µm	2083µin
2 oz.	78.7µm	3098µin	83.7µm	3295µin
3 oz.	108.6µm	4276µin	113.6µm	4472µin
4 oz.	139.5µm	5492µin	144.5µm	5689µin

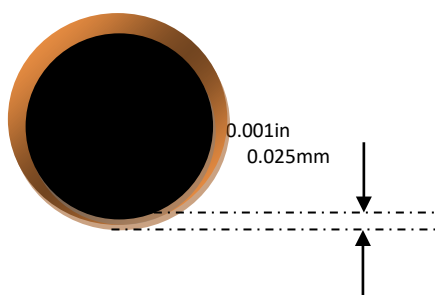
11.5 Hole Size, Hole Pattern and Feature Pattern Accuracy.

The hole size, hole size tolerance, hole pattern accuracy and feature location accuracy shall be as specified in the procurement document and shall be based on finished requirements after plating. Verification of hole size tolerance shall be conducted across all applicable hole sizes, sample measurement is allowed.

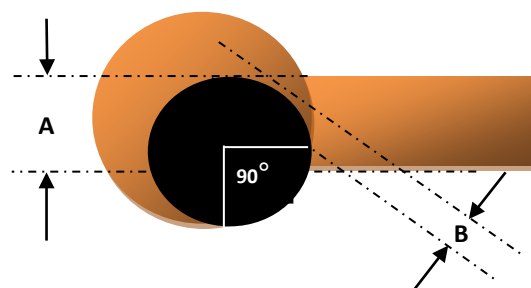
Nodules or rough plating **shall not** reduce the hole diameter below the minimum specified requirement.

11.5.1 Annular Ring and Breakout Class 1 & 2

Minimum Annular Land [MAL] External



Minimum Annual Land [MAL] Internal



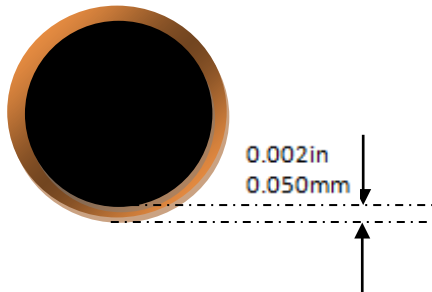
A = Minimum Conductor Width
B = Land/Conductor Junction

90° Breakout is allowed on internals providing that the land/conductor junction [B] is not reduced below the minimum conductor width.

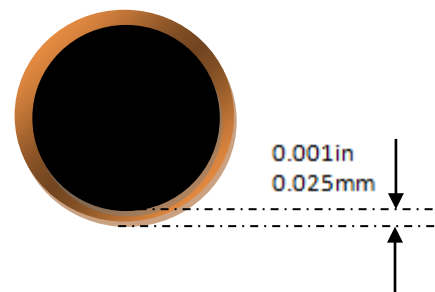
i.e. [A] must measure more than [B]

11.5.2 Annular Ring and Breakout Class 3

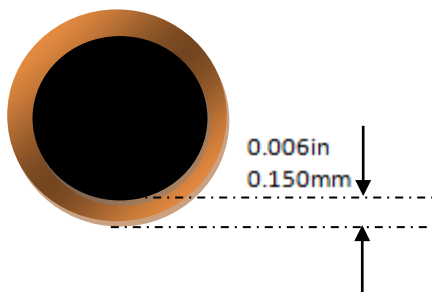
Minimum Annular Land [MAL] External



Minimum Annual Land [MAL] Internal



11.5.3 External Unsupported Holes Class 1 & 2 & 3



11.5.4 Rectangle and Oval Pads



Breakout is permitted on the long axis of oval and rectangular pads unless otherwise specified.

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11.5.5 Minimum Plating Requirements, Surface, Blind, Buried & Through Hole

All holes and vias shall meet the minimum Class 3 plating requirements specified in IPC-6012 and as tabulated below:

Copper – average	25.0µm	984µin
Thin areas	20.0µm	787µin
Wrap	12.0µm	472µin

Any hole less than 0.151mm [0.006in] in diameter and any blind via with an aspect ratio less than 1:1 shall be treated as a Microvia.

11.5.6 Minimum Plating Requirements, Surface, Blind & Buried, Microvias

Copper – average	12.0µm	472µin
Thin areas	10.0µm	394µin
Wrap	6.0µm	236µin

Microvias 0.006in Dia. or less shall contain 0.0004in absolute minimum plating as per IPC-6016.

11.5.7 Minimum Plating Requirements, Surface & Buried Via Cores

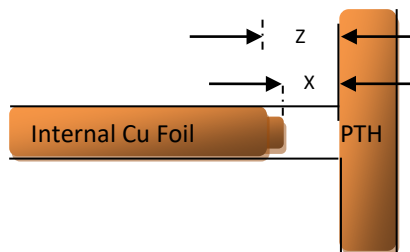
Copper – average	15.0µm	592µin
Thin areas	13.0µm	512µin
Wrap	7.0µm	276µin

11.5.8 Epoxy Smear Removal

Epoxy smear removal is required, prior to plating, for all plated through holes. No epoxy smear allowed in the hole wall when viewed by cross-section. Lateral resin removal **shall not** exceed 25.0µm [984µin]; random tears or drill gouges excluded

11.5.9 Negative Etchback

Unless otherwise specified, Negative Etchback **shall not** exceed 13µm [512µin] 'X' distance and 19.5µm [768µin] 'Z' distance as depicted below.



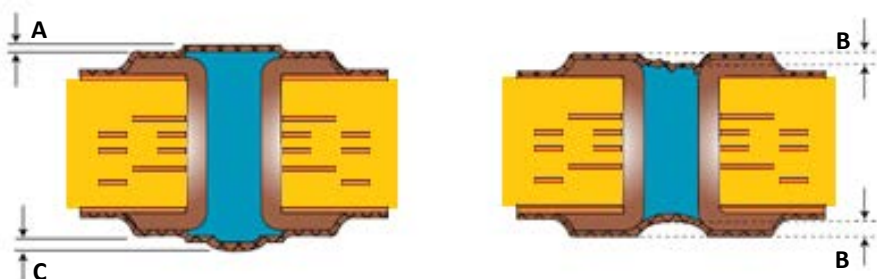
11.5.10 Filled Holes

Unless otherwise specified, holes requiring to be filled shall be filled with non-conductive epoxy materials supporting a CTE value similar to that of the laminate system in use. Conductive epoxies **shall not** be used without the express written permission of the Plexus commodity manager. The hole fill must be a minimum of 70% and any voids must be fully encapsulated. The fill material shall be planar with the surface with a maximum allowable protrusion of + 0.076mm as per IPC 6012

11.5.11 Copper Cap Plating of Filled Holes

If specified in the procurement document, Copper Cap Plating of filled holes (Resin, conductive and or non-conductive) shall be in accordance with IPC-6012 Class 2 requirements.

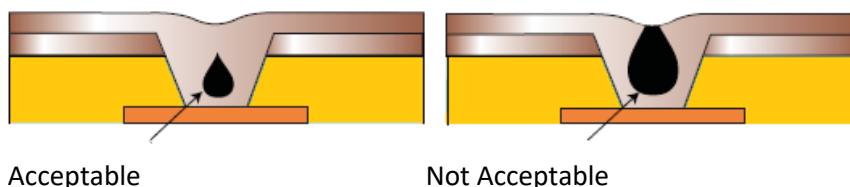
A: Copper Cap – Minimum Thickness	5.0µm	197µin
B: Filled via Depression (Dimple) – Max	127.0µm	5000µin
C: Filled via Protrusion (Bump) – Max	50.0µm	1970µin



Cap plating voids over resin filled holes are not allowed unless completely covered by solder mask.

11.5.12 Plated Copper Filled Microvias (Blind & Buried)

Microvias shall be completely filled with copper, voids are acceptable as long as they are completely encapsulated and do not exceed 25% of the viewable area as depicted below. The area adjacent to any plating void shall meet the minimum copper thickness requirement of 10.0µm [394µin].



11.6 SOLDER MASK

The qualification and conformance requirements of IPC-SM-840 shall apply with the following class designations.

Class 1 & 2:	IPC-SM-840 Class 'T'
Class 3:	IPC-SM-840 Class 'H'
Flex Class 1&2:	IPC-SM-840 Class 'FT'
Flex Class 3:	IPC-SM-840 Class 'FH'

11.6.1 Solder Mask Finish

Unless otherwise specified, the default solder mask color to be used shall be Green Matte, Satin LPI for conventional boards and LDISM for LDI boards. Other solder masks types and colors such as Red, Blue, Black, Gloss or Semi-gloss can be used only with express written permission.

11.6.2 Solder Mask Coverage

- Solder mask coverage shall be uniform and measure no less than 0.0004" in thickness and no more than 0.002" in thickness as measured over any conductor
- Metal conductors **shall not** be exposed in areas where solder mask is required
- Touch-up is not allowed in fine pitch area's defined by features 25mil or less
- Touch-up is allowed in other areas as long as a minimum 3mm pad – repair area is observed
- Misregistration of solder mask defined features **shall not** expose adjacent conductors or lands
- Solder mask registration shall be within +/- 0.003" of the respective outer circuit layer
- Solder mask is not allowed on pads unless specified by design

11.6.3 Solder Mask Encroachment of Vias

Via pads which contain a solder mask aperture smaller than the pad and larger than the finished hole diameter in the supplied data shall be partially covered with solder mask. The finished PCB shall meet the following requirements in regards to solder mask encroached vias:

- Solder mask shall encroach onto the pad 0.003" minimum from the entire outer circumference of the via pad
- Solder mask in the barrel of the via is not preferred, however it is acceptable if required to meet the 0.003" encroachment requirement

11.6.4 Solder Mask Coverage (Capping) of Vias

Via capping is not allowed with an Organic Solderability Protectant (OSP) surface finish. Via pads which contain no solder mask aperture in the supplied data shall meet the following requirements:

- Solder mask material must cover the pad and cap the hole, exposed metalized material is not allowed
- Solder mask material shall only cover the vias on the side of the PCB that contains no aperture
- Total combined thickness of primary solder mask and secondary cap **shall not** exceed 0.003"
- Capping material shall be similar in chemistry to the LPI solder mask
- Capping material **shall not** penetrate more than 75% of the hole being capped $\geq 70\%$ double side
- If the exposed copper density does not allow capping of vias (i.e. dogbone vias inside a 0.8mm BGA) tenting of the vias and allowing solder mask in the barrel is acceptable
- Solder mask via cap process must occur after the final copper cleaning process

11.6.5 Solder Mask Cure and Adhesion

Visual assessment of the cured solder mask shall show no signs of cracking, blistering, or delamination.

- Adhesion – the adhesion of the cured solder mask to the base material and conductors shall be tested to IPC-TM-650 method 2.4.28.1, the maximum percentage of lifted solder mask prior to and after exposure to solder is zero, 0%. 5% lifted solder mask is permitted over ENIG and 10% over melting metals such as LFHASL and Immersion Tin
- Adhesion – when subsequent solder mask coatings are applied such as double coating the adhesion between layers shall meet the same requirements as above.

11.6.6 Solder Mask Flammability

The flammability performance of the cured solder mask shall be determined in accordance with UL 94, the solder mask coating **shall not** raise the flammability rating 'V' or 'VTM'

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11.7 SURFACE FINISH

The table below provides the standard surface finish requirements for each finish that may be called out on the fabrication drawing. When Solder Mask Over Bare Copper (SMOBC) is specified, the surface finish should be applied to all solder mask exposed copper.

Surface Finish Requirements		
Description	Thickness	Specification
HASL - Hot Air Solder Level	C&S	J-STD-003
LFHASL - Lead Free Hot Air Solder Level	C&S	J-STD-003
OSP - Organic Solder Preservative	Solderable	J-STD-003
HTOSP - High Temperature Organic Solder Preservative	Solderable	J-STD-003
I-Ag - Immersion Silver	0.12-0.4µm / 5-16µin	IPC-4553
I-Sn - Immersion Tin	1µm/40µin	IPC-4554
ENIG - Electroless Nickel Immersion Gold	118µin /2.00µin **	IPC-4552
ENEPIG Electroless Palladium Immersion Gold	118µin /2.00µin/C&S	IPC-4552 J-STD-003
N - Nickel-Electroplate edge printed board connectors	98.4µin minimum	None
NB - Nickel – Electroplate as a barrier	51.2µin minimum	None
DIG - Direct Immersion Gold (Solderable Surface)	Solderable	J-STD-003
C - Bare Copper	AABUS	AABPS
TLU - Electrodeposited Tin-Lead Unfused	315µin minimum	J-STD-003
T - Electrodeposited Tin-Lead Fused	C&S	J-STD-003
G - Gold edge printed connectors and non solderable areas	31.5µin minimum	None
GS - Gold Electroplate on solderable areas	17.72µin minimum	None
GWB-1 - Gold Electroplate for areas to be wire bonded + Electrolytic nickel under gold (Minimum - Ultrasonic)	1.97µin 118µin	None
GWB-2 - Gold Electroplate for areas to be wire bonded + Electrolytic nickel under gold (Minimum - Thermosonic)	11.8µin 118µin	None
CB1 - Carbon Ink Pads	0.001in nominal	None

** Note, Plexus minimum Gold/Nickel thickness requirement of 118µin /2.00µin exceeds that of IPC 4552

11.7.1 Gold Edge Board Contacts and Contact Pads

All pads specified in the fabrication drawing as Gold Edge Contacts and Gold Contact Pads shall meet the following requirements unless otherwise stated in the fabrication drawing:

- Shall meet the plating requirements for (N) + (G) in the above table
- Shall not be covered by or contain solder mask residue
- Shall not exhibit evidence of delamination, burrs, solder, routing slivers, plating slivers or blisters.
- Shall not exhibit exposed nickel or copper except where exposed due to bevel cut on edge connectors
- Shall not contain scratches greater than 0.005" wide

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11.7.2 Electroless Nickel Immersion Gold (ENIG)

To ensure the highest coating durability rating possible as specified in J-STD-003, two features of an ENIG coated PCB or representative test coupon shall be micro-sectioned at a frequency determined by the supplier to ensure demonstrable compliance to IPC 4552 Hyper-Corrosion requirements. The determined frequency shall not exceed Five MTO's of the Nickel plating bath and must ensure compliance on a lot by lot basis of shipped product. The analysis of the sample shall be performed on a specimen which has not been etched. The sample shall contain two or more features in the mount, one of which shall be a PTH feature, the other an SMT pad. Analysis of the micro-section shall be performed using optical microscopy at a maximum reference magnification of 1000x ensuring that Nickel Hyper-Corrosion deposits conform to the acceptability criteria as defined in section 11.7.5

	Level 0	Level 1	Level 3	Level 2
Observation	Defect free ENIG deposit	- Number of Spike-Type Defects observed < 10 and All corrosion spike depths are $\leq 20\%$ of the nickel deposit thickness	- Number of Spike-Type and/or Spreader-Type Defects observed ≥ 10 and > 5 of the observed defects have a depth > 40% of the nickel deposit thickness or - Black Band-Type defect(s) present that extend to $\geq 30\%$ of the field of view	All other observations

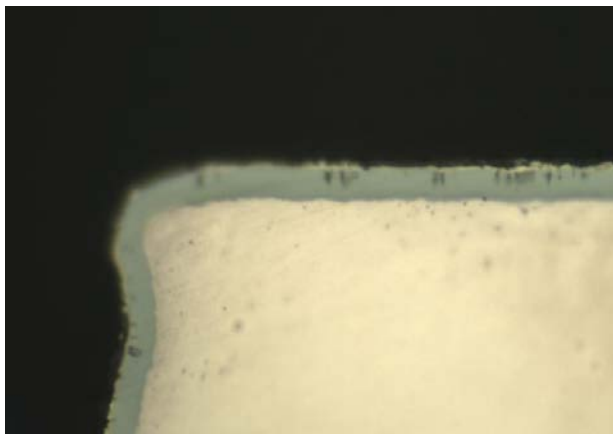
Note: A feature is defined as an observation location within a surface mount or fiducial pad or a PTH with associated annular rings plated with ENIG and evaluated in cross section. It may be within a test coupon or from an actual circuit.

Thickness measurements of both the Nickel and the Gold shall also be performed at a frequency which ensures compliance to IPC 4552, it is acceptable to use the encapsulated Hyper-Corrosion microsection above to perform the Nickel measurements but the Gold thickness measurement shall be performed using X-ray fluorescence (XRF) as per ISO-4527, Auto-Catalytic Nickel-Phosphorous Coatings; Specifications and Test Methods.

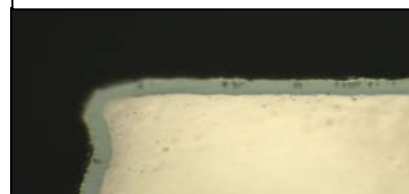
The acceptability of the ENIG coating shall be certified through the certificate of conformity and the polished micro-section and measurement results shall be retained for a period of 2 years by the supplier and made available upon request to Plexus.

11.7.3 Identification of Hyper-Corrosion Product

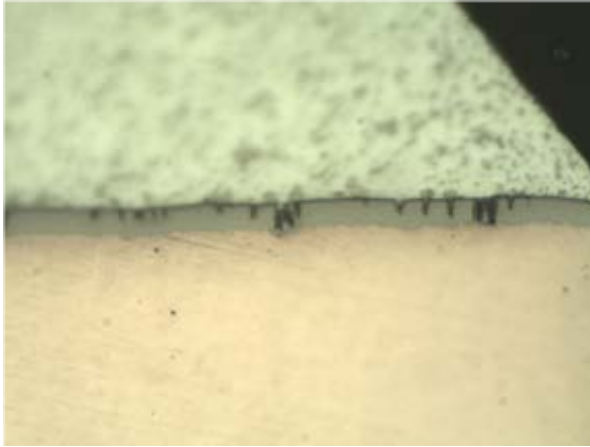
Nickel Spikes



A spike is a narrow, less than 2.5 microns wide, dark, isolated feature extending downwards from the electroless nickel surface into the electroless nickel deposit.



Spreader Defects

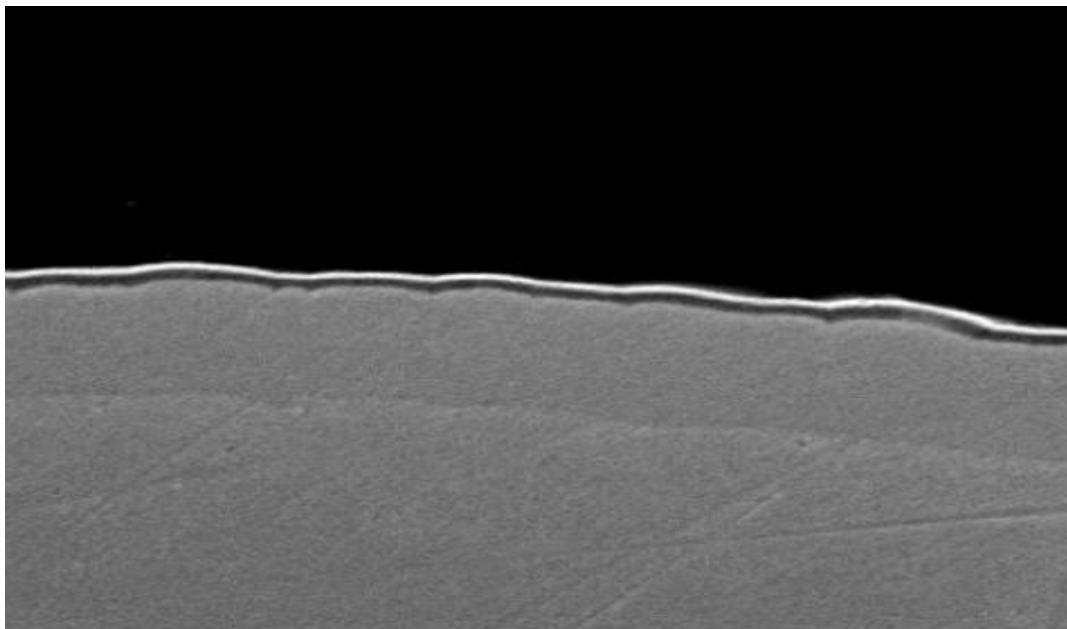


Spreader defects are a single, contiguous feature that is greater than 2.5 μm (100 μinch) in width extending from the electroless nickel / immersion gold interface into the nickel deposit.



Black Band Defects

Black band defects are a contiguous layer of corrosion that extends across the nickel surface for a minimum of 30% of the field of view at 1000X. Black band defects have several different appearances, with and without gold being visible, deep penetration into the nickel deposit in a jagged pattern or shallow in nature but to a uniform depth. The contiguous layer is what defines the black band, not the shape of the corrosion.



11.7.4 Measurement and Analysis

Samples for hyper-corrosion evaluation shall be in the as-plated condition. The samples shall be prepared in a cross section mount that has not been etched in any manner. The sample must contain two or more features in one or more cross-section mounts. While a feature may be a through hole with associated annular ring, it is also acceptable to micro-section a surface mount pad for the purpose of evaluation.

Inspection for hyper-corrosion of the feature selected above for the purposes of PCB acceptance shall use optical microscopy at a maximum of 1000X magnification.

Surface Mount Feature

If a surface mount feature is selected for evaluation then five locations on the feature must be observed.

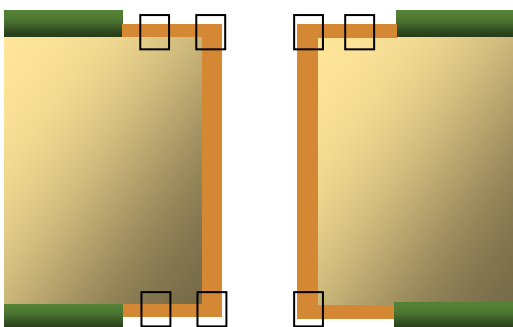


The level of Hyper-Corrosion at each location shall be recorded in a table and the product acceptance shall be determined based on the disposition criteria as specified in section 11.7.5

	Pad x	Level
sample ID xxxxxx	Location 1	
	Location 2	
	Location 3	
	Location 4	
	Location 5	

Through-Hole Feature with Annular Ring

If a through-hole feature is selected for evaluation then seven locations on the feature must be observed.



	PTH x	Level
sample ID xxxxxx	Location 1	
	Location 2	
	Location 3	
	Location 4	
	Location 5	
	Location 6	
	Location 7	

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11.7.5 Product Acceptance Criteria

Following evaluation of the micro-sections based on the recorded levels of Hyper-Corrosion, the product rating shall be established and the product dispositioned accordingly. Please note that when differing product ratings occur between the SMT feature and the PTH feature, the maximum product rating shall apply to the product being dispositioned.

PTH FEATURE	Sample 1	Sample 2	Sample 3	Sample 4
	level	level	level	level
Location 1	1	2	1	2
Location 2	1	1	1	2
Location 3	0	2	1	1
Location 4	2	1	2	2
Location 5	1	1	1	1
Location 6	3	1	1	1
Location 7	1	3	1	1

SMT PAD	Sample 1	Sample 2	Sample 3	Sample 4
	level	level	level	level
Location 1	3	2	1	2
Location 2	1	1	1	3
Location 3	1	1	2	1
Location 4	2	2	1	2
Location 5	1	1	1	1

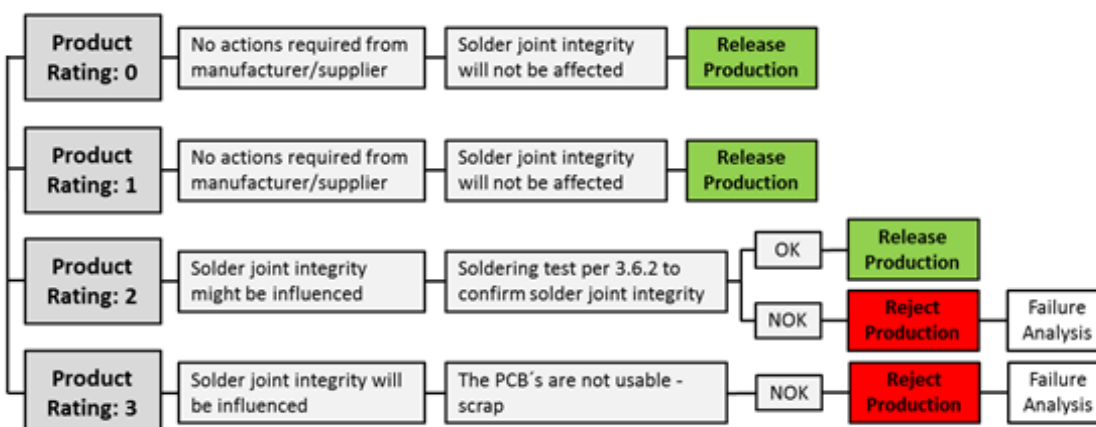
	Total	Total	Total	Total
Level 0	1	0	0	0
Level 1	4	4	6	4
Level 2	1	2	1	3
Level 3	1	1	0	0

	Total	Total	Total	Total
Level 0	0	0	0	0
Level 1	3	3	4	2
Level 2	1	2	1	2
Level 3	1	0	0	1

Product Rating	1	2	1	2
----------------	---	---	---	---

Product Rating	1	2	1	2
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Product Rating	Hyper-Corrosion Investigation	Disposition
0	Defect free ENIG deposit -zero evidence of hyper-corrosion	Target condition
1	≥60% of investigated locations show Level 0 or 1	Acceptable – This level of hyper-corrosion activity will not degrade solder joint integrity.
2	All other observations	AABUS – Will require extra analyses and testing to ensure acceptability.
3	≥40% of investigated locations show Level 3	Rejectable – This level of hyper-corrosion will degrade solder joint integrity.



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11.8 CARBON INK

All pads specified to have carbon ink coating are subject to the following conditions unless otherwise stated in the fabrication drawing:

- Resistivity: 30 ohms – 40 ohms per square
- Thickness: 0.001" nominal
- Carbon ink must be centered over copper contact pattern, no pinholes, no smears, and no exposed copper areas are allowed
- The carbon ink deposition must provide continuous coverage on top of the conductor pattern where it has to be applied. Coverage on the sidewall of the conductor pattern is not required
- Voids are permissible provided that they do not exceed 0.005" in any direction. A maximum of three voids per conductor is allowable
- Foreign inclusions are permissible in the carbon ink deposit provided they do not exceed 0.010" in any direction. A maximum of three inclusions per conductor is allowable
- Carbon ink shall be capable of withstanding the tape pull adhesion test as defined in IPC-SM-840, Test Method 2.4.28.1, with the basis of rejection being exposed copper. Surface residual carbon is sometimes removed from a carbon contact; this condition does not warrant rejection

11.8.1 Silkscreen / Legend

Silkscreen shall be white nonconductive epoxy ink.

11.8.2 Silkscreen / Legend Registration

- Registration shall be within +/- 0.006" of its respective outer circuit layers
- No ink is permissible on plated through hole pads and surface mount lands
- Minor skipping or smearing is acceptable as long as it does not affect legibility or solderability
- Clipping of silkscreen should be performed per Section 10.5

11.9 SUPPLIER ID MARKINGS

The markings indicated in the following subsections must be marked or etched in the location indicated in the fabrication drawing. If the fabrication drawing does not specify a location, the preferred location is on the secondary side in copper. The primary side should only be used when space is too limited on the secondary side. Multi-up arrays shall contain these markings on each PCB within the array. The actual location must always be approved by Plexus and shall be raised as an Engineering Query as part of the DFM process.

11.9.1 Supplier Logo

The UL recognized supplier logo must be added to the PCB with the UL type designation and/or markings that reflect the specified flame class and maximum operating temperature ratings.

11.9.2 Date Code

The date code shall consist of four numerals giving the year manufactured (YY) and work week (WW) – (e.g. 0628 stands for year 2006 – week 28).

11.9.3 Lot Code

The supplier is responsible to add a lot code and provide traceability to the work order.

11.9.4 3D Matrix or Barcode

If required and not specified, the supplier is responsible to request that Plexus identifies a suitable location for the placement of a laser ablated 3D Matrix or Barcode.

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11.10 CLEANLINESS

11.10.1 Ionic and Organic Contamination

Printed circuit boards shall be cleaned according to good industry practices to assure removal of oils, processing residues, contaminants, fingerprints, and other foreign material. Products shall be tested in accordance with IPC-TM-650 test methods, 2.3.25.0/1 ROSE or Modified (ROSE) extraction method and IPC-TM-650 2.3.28 Ion Chromatography Method.

The requirements of which are:

Internal Process Control at PCB fabricators facility

- TM-650 2.3.25.0/1 ROSE or Modified (ROSE) extraction method
 - Frequency 1 panel each batch or production lot/minimum 4 hourly
 - Process Stage – Pre-solder mask coat. **Maximum 0.40µg NaCl/cm² [2.6µg/in²]**
 - Process Stage – Final stage pre-pack. **Maximum 0.62µg NaCl/cm² [4.0 µg/in²]**
- TM-650 2.3.28 Ion Chromatography Test Method
 - Frequency 1 panel per Quarter *
 - Process Stage – Final stage pre-pack
 - Individual element specifications**
 - WOA – Only if requested ***

ANIONS	Max Limit	CATIONS	Max Limit	WOA ***	Max Limit
Bromide	<3µg/in ²	Ammonium	<2µg/in ²	Acetate	<2.5µg/in ²
Fluoride	<0.5µg/in ²	Calcium	<1µg/in ²	Phthalate	<3µg/in ²
Chloride	<2.5µg/in ²	Lithium	<0.5µg/in ²	Formate	<2.5µg/in ²
Nitrate	<2µg/in ²	Magnesium	<0.5µg/in ²	Glutamate	<3µg/in ²
Nitrite	<2µg/in ²	Potassium	<3µg/in ²	Melate	<3µg/in ²
Phosphate	<2µg/in ²	Sodium	<3µg/in ²	Methane Sulfate	<3µg/in ²
Sulfate	<3µg/in ²	Citrate	<0.5µg/in ²	Succinate	<3µg/in ²

* Note: Ion Chromatography results with individual element analysis shall be retained by the supplier for a period of 2 years and shall be made available to plexus upon request.

** Note: If averages are used from multiple samples to determine the individual element analysis, any single result shall be within 1.5x the specified maximum limit.

*** Note: WOA results are only required when specifically requested in writing from Plexus and are not required as part of your normal retention records.

11.10.2 Inclusions

Foreign particles entrapped in solder mask or legend shall be no larger than 0.005 inch in its largest dimension and shall not reduce the distance between conductive patterns by more than 20%.

11.11 ELECTRICAL TEST

11.11.1 Test Requirement

All PCB's must be 100% tested to IPC-9252A Level C requirements for both continuity and isolation. Indirect testing by signature comparison is not allowed. When utilizing Flying probe testing, adjacency testing shall be used with a minimum adjacency value of 1.27mm [0.05in]. Final PCB test data must be cross-referenced to the IPC-D-356 file, neutral file or to the provided netlist.

Testing Type	Specification/Limit
Resistive Continuity Testing	$\leq 10\Omega$
Resistive Isolation Testing	$\geq 10M\Omega$
Indirect Isolation & Continuity	Not Allowed
Adjacency Testing	1.27mm [0.050in] min

11.11.2 Evidence of PCB Test

Evidence of test performance required via permanent non-conductive stamp in contrasting color on the PCB. Edge marking of PCB's is allowed as an alternative to stamping unless otherwise specified. Stamp location to be agreed between plexus and Supplier. Supplier shall keep test records on file for a minimum of 1 year; records shall be available to Plexus upon request.

11.12 CONTROLLED IMPEDANCE

When controlled impedance traces are specified in the PCB fabrication drawing, the supplier must fabricate the PCB to match the impedance goals as defined in IPC-2141 so that they can be tested in accordance with IPC-TM-650 (2.5.5.7). Minor modifications to achieve target impedance are allowed, as long as they are within the limits of the fabrication drawing and this specification. Plexus must approve any changes beyond the specified limits.

11.12.1 Impedance Tolerance

The impedance tolerance $\geq 50\Omega$ shall be $\pm 10\%$ if not defined in the PCB fabrication drawing, when impedance is less than 50Ω then $\pm 5\Omega$ applies.

11.12.2 TDR Test Requirements

When controlled impedance is specified, the initial lot shall have 100% of the coupons tested by the supplier using Time Domain Base Reflectometry (TDR). Subsequent shipments shall be tested as per a sampling plan coordinated with Plexus.

11.12.3 TDR Test Coupon

TDR test coupon shall model the construction and trace characteristics of the PCB. If the PCB contains differential signals, the TDR test coupon shall model the differential signals on the same layers in addition to the single ended signals. A minimum of one TDR test coupon shall be provided in the manufacturing panel. Traceability between coupon and manufacturing panel shall be maintained and coupons shall be stored for a period of not less than 2 years.

11.12.4 Rework and Repair

Track welding is not allowed. Short repair on O/L is not allowed. Other rework and repair is allowed as long as the act of reprocessing or restoring the product to a state of compliance is through the use of original or equivalent processing, in such a manner that ensures full compliance with the original drawing and specification and has no detrimental effect on quality or reliability.

11.13 SOLDERABILITY REQUIREMENTS

All PCB's shall be fabricated in accordance with IPC-6012 and shall be evaluated for surface and PTH solderability utilizing the default test methods as referenced in J-STD-003. The default test methods that shall be used and which are recognized by Plexus are the Surface Mount Simulation and the Wave Solder Simulation test.

The Solder float test method shall not be used in substitution

12 REQUIREMENTS FOR EACH SHIPMENT OF PCB'S

12.1 PCB AGE CRITERIA

All PCB's which are greater than 6 months in age **shall not** be shipped without written approval from Plexus.

12.1.1 PCB Shelf Life

PCB Shelf life is based on the date of manufacture and not the date of receipt; the following table applies to all PCB's shipped to Plexus.

Surface Finish	Shelf Life from D.O.M
HASL (HAL)	12 Months
LF HASL (LFHAL)	12 Months
Immersion Silver	6 Months
Immersion Tin	6 Months
ENIG	12 Months
ENIG	12 Months
Palladium	12 Months
Hard Gold	12 Months
OSP	6 Months
Flux	6 Months
Bare Copper	6 Months

12.2 SOLDER SAMPLES

The first prototype, revision changed order or Q-code defined PCB's shall contain two solder sample PCB's. The solder sample boards do not need to be good boards. These can be boards with defects or boards that do not pass test. The outline of the solder sample shall be the same as the good PCB's with no additional cutout or drilled out areas. Each solder sample board shall be clearly marked with a permanent marker. The markings shall not go over any exposed copper pads. The solder sample PCB's shall be packaged separately from the good PCB's. The package shall also be clearly marked as Solder Samples.

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12.3 HANDLING/PACKAGING /STORAGE REQUIREMENTS

PCB's shipped to Plexus shall be suitably dry packaged, handled and stored such that the PCB's are protected from contamination, physical damage, solderability degradation, electrostatic discharge and moisture uptake. This specification deviates from and takes precedence over IPC/JEDEC J-STD-033C-1, J-STD-020, J-STD075, IPC-1601 requirements.

12.3.1 MSD Level

PLEXUS categorize PCB's as MSL Level 3 devices.

LEVEL	FLOOR LIFE ⁴		SOAK REQUIREMENTS ³				
			STANDARD		ACCELERATED EQUIVALENT ¹		
					eV 0.40-0.48	eV 0.30-0.39	CONDITION
	TIME	CONDITION	TIME (hours)	CONDITION	TIME (hours)	TIME (hours)	
1	Unlimited	≤30 °C/85% RH	168 +5/-0	85 °C/85% RH	NA	NA	NA
2	1 year	≤30 °C/60% RH	168 +5/-0	85 °C/60% RH	NA	NA	NA
2a	4 weeks	≤30 °C/60% RH	696 ² +5/-0	30 °C/60% RH	120 +1/-0	168 +1/-0	60 °C/60% RH
3	168 hours	≤30 °C/60% RH	192 ² +5/-0	30 °C/60% RH	40 +1/-0	52 +1/-0	60 °C/60% RH
4	72 hours	≤30 °C/60% RH	96 ² +2/-0	30 °C/60% RH	20 +0.5/-0	24 +0.5/-0	60 °C/60% RH
5	48 hours	≤30 °C/60% RH	72 ² +2/-0	30 °C/60% RH	15 +0.5/-0	20 +0.5/-0	60 °C/60% RH
5a	24 hours	≤30 °C/60% RH	48 ² +2/-0	30 °C/60% RH	10 +0.5/-0	13 +0.5/-0	60 °C/60% RH
6	Time on Label (TOL)	≤30 °C/60% RH	TOL	30 °C/60% RH	NA	NA	NA

12.3.2 Maximum Shipping Quantity per Pack

The maximum pack quantities specified below shall be adhered to at all times.

PCB Dimensions	Maximum Quantity /Pack
PCB Thickness >3.0mm	15 Arrays/Pack
PCB Area > 12inch	10 Arrays / Pack
PCB Area < 12 inch	25 Arrays / Pack

12.3.3 Interleaving of PCB's

To prevent damage caused by friction and potential oxidization of the solderable surfaces, all PCB's shall be interleaved using Sulfur free paper between each array and between the PCB and the packaging film as depicted in the table below:

Surface Finish	Required
LF-HASL	NO
HASL	NO
Immersion Silver	YES
Immersion Tin	YES
ENIG	YES
ENIPIG	YES
Hard Gold	YES
Bare Copper	YES
OSP	YES
Flux Coating	YES



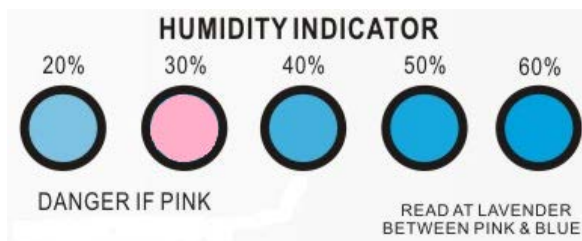
12.3.4 Corner Protection and Stiffeners

All 4 corners of the PCB stack shall be protected with Plastic or Sulfur free paper edges as depicted below, top and bottom FR4 stiffeners are also required when the PCB thickness is \leq than 0.5mm.



12.3.5 HIC and Desiccant

All PCB packages shall contain a 5 Spot Humidity Indicator Card showing incremental steps of 10% RH minimum plus a sulfur free desiccant bag. The HIC card and desiccant bag shall be placed on the side of the package and should never be placed directly on the surface of the PCB. The Desiccant bag should be of minimum dimension L x W of 2 inch x 2 inch (5g min) and be capable of protecting the PCB in a storage environment with elevated humidity levels up to 90% RH for 1 year.



Plexus may reject incoming packages which show evidence of humidity in excess of 30%.

12.3.6 Internal Packaging (Dry Pack)

All PCB's shipped to Plexus shall be shipped in a double wall dry pack consisting of an internal air evacuated ESD bag or air evacuated ESD pink wrap (Stage 1), and an outer wall consisting of air evacuated PE film (Stage 2) with a (Water Vapor Transmission Rate) $<$ than 0.002gm/100in²/24 hrs.

Stage 1: Air Evacuated ESD Bubble

Stage 2: Exterior Air Evacuated PE

Aluminum MBB's are not required



Aluminized Polyester bags while acceptable are not a requirement of this specification.

12.3.7 External Packaging and Additional Requirements

- The internal dry packs shall be sufficiently supported within the outer layer carton utilizing contaminant free packaging materials so as to protect the package and prevent movement
- The results of any TDR measurements associated with the shipping products shall be included
- TDR coupons are not required with the shipment unless specified or requested
- Each container or outer layer carton **shall not** exceed fifty (50) pounds in gross weight
- Shipments may contain mixed date and lot codes to aid manufacturing flexibility as long as they are segregated. The product date code, lot code and quantity must be clearly identified on the outer packaging and inner packaging labels. Mixed date and lot codes in the same dry pack are not allowed
- Reference to the Plexus Purchase Order should always be made to check for any additional quality requirements or Q-codes that may be necessary beyond this specification
- Each shipment shall contain a packing slip and certificate of compliance detailing the part number, EC level or revision, date code, lot code, quantity and purchase order number
- Each shipment of RoHS compliant PCB's shall be certified as such. A certificate of Analysis confirming compliance of the solder surface covering shall be included detailing the part number, EC level or revision, date code, lot code, quantity and purchase order number. The analytical results for the solder constituents shall be as defined by IPC-J-STD-006 (latest revision)
- All outer layer cartons shall be labelled up compliance detailing the part number, EC level or revision, date code, lot code, quantity and purchase order number

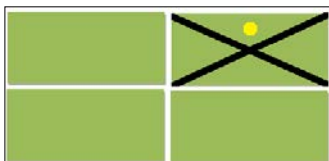
13.0 X-OUTS BAD BOARD (Multi-up Array)

Plexus understands that from time to time it may be advantageous to ship X-OUTS or Bad Boards as part of a controlled shipment, either to aid manufacturing flexibility or to ensure continuity of supply. High value arrays and or Flex/Rigid Flex designs having a high tendency to necessitate this requirement due to the inherent yield issues and the associated scrap costs.

The default rule is X-OUTS are **NOT** allowed and **shall not** be shipped to Plexus unless previously agreed in writing and documented as such on the specification and or purchase order.

When X-OUTS have been authorized or allowed then the following shall apply:

- Multi-up PCB arrays **shall not** contain X-OUTS when the batch size is less than 20 boards
- No more than 1 X-OUT is allowed in a 2up or 3up array configuration
- For 4up configurations and greater, no more than 25% of the total array shall contain X-OUTS
- The total number of X-OUT arrays in any one shipment **shall not** exceed 10% of the total quantity
- Arrays containing X-OUTS shall be segregated from those which do not and be clearly identified
- Arrays containing different X-OUT configurations shall be sorted and packaged in separate dry packs
- Quality records detailing the reason for X-OUTS shall be included with the shipment
- All X-OUT circuits must be clearly identified with a large black X in indelible marker and contain a bad board indicator in either yellow or white as depicted below:



REVISION HISTORY

REV	RELEASE DATE	ORIGINATOR	REASON FOR CHANGES
F	13 June 2014	Scott Ubl	CR58295 Section 3, Added text to more explicitly define the suppliers requirement for auto-creation of features as part of a CA
G	19 Oct 2015	Don Schmieder	CR64541 Section 9.3 updated to include description of HIC, combined with CR64721 Update packaging requirements to aid in better processing for manufacturing.
H	17 Aug 2016	Steve Bray	CR 69345 Complete and comprehensive rewrite of the whole document bringing it in line with the latest Industry best practice specification and revisions.
H.1	22 Sept 2016	Steve Bray	CR 70119 Add RIV, ISL & HGZ as applicable sites
I	2 Feb 2017	Steve Bray	CR71471 Various changes in document to reflect current or best practice.
J	24 May 2017	Steve Bray	CR 75130 Amended document in HIC Section based on ballot feedback relating IC quarterly testing.
K	26 Oct 2018	Steve Bray	CR 91190 Major Change to include Hyper-Corrosion measurement as well as Nickel/Gold thickness check in light of Major Black Pad incident. Also made some modifications to Shelf life section where I increased from 3-6 months, Preferred construction no longer recommends 7628 pre-preg as our goto low cost solution due to the Glass/Resin content. Ionic Contamination results have been reduced to quarterly and are now retained by the supplier, no longer require WOA's unless specifically requested.
L	07 Nov 2018	Steve Bray	CR 91336 Section 11, ENIG Hyper-Corrosion section amended based on an imminent change from the IPC 4552 committee. Added Definition for MTO. Updated Table of Contents.
L.1	10 Dec 2018	Steve Bray	CR 91561 Section 12.2, Removed ENIG Hyper-corrosion SHIP microsection requirement and removed the revision letter from references of IPC 4552. Some other minor edits to correct Type errors. IPC 6016 removed as now incorporated into latest revision of IPC 6012
L.2	28 Jun 2019	Steve Bray	CR# 92936. Referenced 11.5.7 disposition criteria in section 11.7.2 and changed formatting on the drawing in section 11.7.4.
L.3	03 Mar 2020	Daniela Jurcutiu	CR 96896 Section 11.9.2 Change date code format to bring it in line with latest updates in Supplier Quality Manual, with reference to ANSI Standard-10D.