



PATENT CLAIM $\triangle 5$

BOTTOM VIEW

JEDEC
SOLID STATE
PRODUCT OUTLINE

THIS **REGISTERED OUTLINE** HAS BEEN PREPARED BY THE JEDEC JC-11 COMMITTEE AND REFLECTS A PRODUCT WITH ANTICIPATED USAGE IN THE ELECTRONICS INDUSTRY; CHANGES ARE LIKELY TO OCCUR.

TITLE	PACKAGE DESIGNATOR	ISSUE	DATE	SHEET
CERAMIC NO LEAD CHIP CARRIER	R-CBCC-N3	A	01/01	1 OF 2
			TO-276	

VARIATIONS (ALL DIMENSIONS IN INCHES)												
SYMBOL	AA			NOTE	AB			NOTE	AC			NOTE
	RECTANGULAR				RECTANGULAR				RECTANGULAR			
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.112	.118	.124	2	.130	.136	.142	2	.130	.136	.142	2
A1	.010	.015	.020	2	.010	.015	.020	2	.010	.015	.020	2
b	.281	.286	.291	2	.370	.375	.380	2	.435	.440	.445	2
b1	.220	.225	.230	2	.410	.415	.420	2	.470	.475	.480	2
b2	.090	.095	.100	2	.135	.140	.145	2	.135	.140	.145	2
b3	.115	.120	.125	2	.152	.157	.162	2	.152	.157	.162	2
D	.395	.400	.405		.620	.625	.630		.685	.690	.695	
D1	.030	---	---		.030	---	---		.035	---	---	
E	.291	.296	.301		.445	.450	.455		.520	.525	.530	
e	.075 BSC				.105 BSC				.120 BSC			
Note	1, 3, 4, 5				1, 3, 4, 5				1, 3, 4, 5			
Ref.	10-408				10-408				10-408			
Issue	A				A				A			

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. SOLDER FINISH IS OPTIONAL. DIMENSIONS A, A1, b1, b2 AND b3 APPLIES TO A METALLIZED TERMINAL.
3. THE TERMINAL #1 IDENTIFIER MUST BE LOCATED WITHIN THE ZONE INDICATED. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL.
4. ALL DIMENSIONS ARE IN INCHES.
5. IT HAS BEEN STATED THAT U.S. PATENT NO. 5,111,277 (HELD BY OLIN AEGIS) MAY RELATE TO CERTAIN APPLICATIONS OF THIS PACKAGE OUTLINE.

JEDEC SOLID STATE PRODUCT OUTLINE	TITLE CERAMIC NO LEAD CHIP CARRIER	ISSUE A	DATE 01/01	TO-276	SHEET 2 OF 2
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