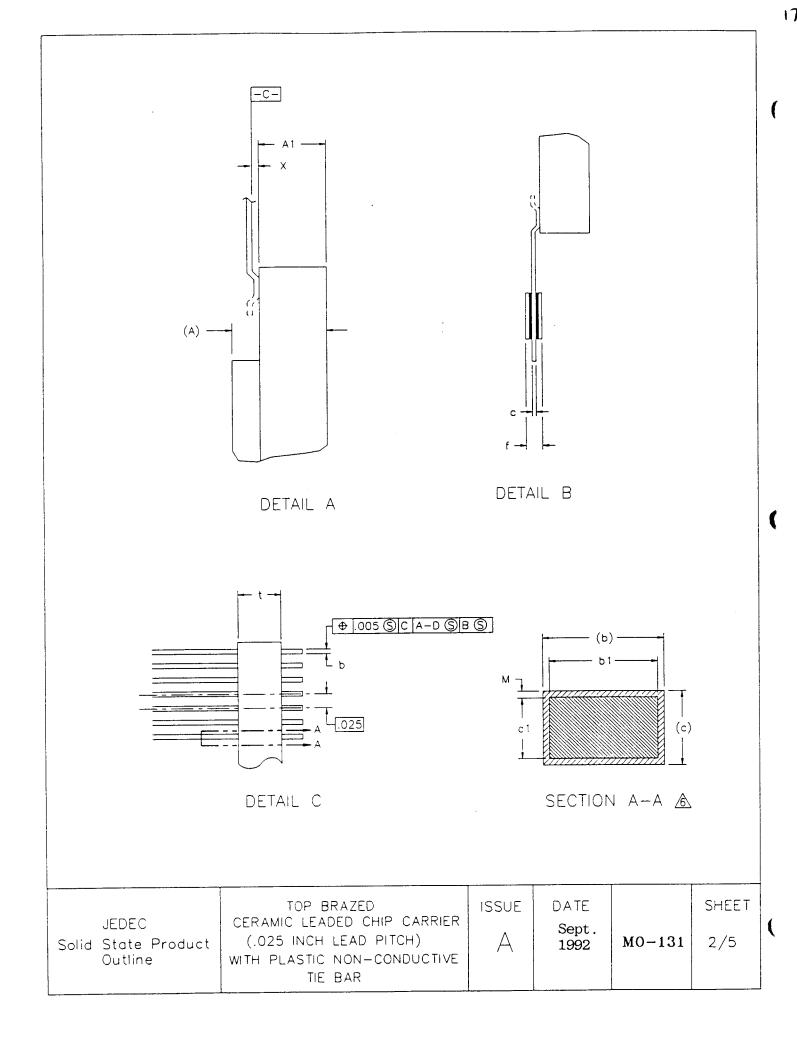
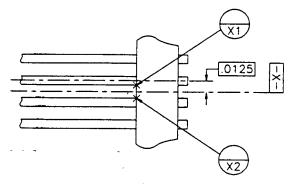


National Semiconductor has stated that U.S. Patent No. 4,796,080 may relate to a certain implementation of this package outline. The sponsor has not agreed with this statement.

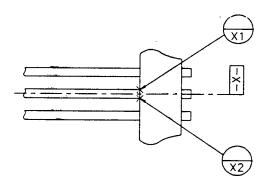
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JEDEC CERAMIC L Solid State Product (.025 IN Outline WITH PLAS	P BRAZED  LEADED CHIP CARRIER  CH LEAD PITCH)  TIC NON-CONDUCTIVE  TIE BAR	JE DATE Sept. 1992	MO-131	SHEET
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 $X = \begin{bmatrix} -A - \end{bmatrix}, \begin{bmatrix} -B - \end{bmatrix}$  OR  $\begin{bmatrix} -D - \end{bmatrix}$ EVEN LEAC SIDES



X = -A-, -B- OR -D-ODD LEAD SIDES

DETAIL "D"

JEDEC
Solid State Product Outline

TOP BRAZED
CERAMIC LEADED CHIP CARRIER
(.025 INCH LEAD PITCH)
WITH PLASTIC NON-CONDUCTIVE
TIE BAR

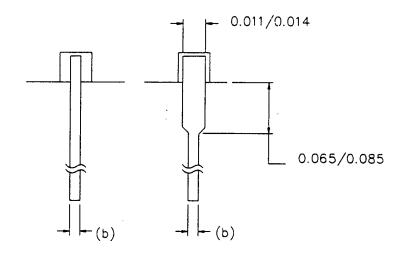
TOP BRAZED
CERAMIC LEADED CHIP CARRIER
A
Sept.
1992
M0-131
3/5

s			VARIA	4 TI(	DNS			
SYMBO		AA		OZ		AB		70Z
Į į	MIN.	NOM.	MAX.	ĬĔĪ	MIN.	NOM.	MAX.	Ī
Ā	_		0.130			-	0.140	
A1		_	0.105		_	_	0.105	
ь	0.006	0.008	0.010		0.006	0.008	0.010	
ь1	0.005	0.007	0.009	6	0.005	0.007	0.009	6
c	0.004	0.006	0.008		0.004	0.006	0.008	
c1	0.003	0.005	0.007 ·	6	0.003	0.005	0.007	6
D	0.935	0.950	0.965		1.035	1.050	1.065	
D2	1.510	1.520	1.530		1.710	1.720	1.730	
D3	-	_	1.540			-	1.740	
D4	0.820	0.830	0.840		0.895	- 0.905 -	0.915 -	
Ε	0.935	0.950	0.965		1.035	1.050	1.065	ļ
E2	1.510	1.520	1.530	1	1.710	1.720	1.730	<u> </u>
E3	-	-	1.540				1.740	-
E4	0.820	0.830	0.840	1	0.895	0.905	0.915	<del> </del>
f	0.015	0.035	0.045	<del> </del>	0.015	0.035	0.045	1
Х	0.002	0.008	0.014	$\downarrow \longrightarrow$	0.002	0.008	0.014	+
L1	0.190		_	+	0.190	_	0.0005	6
М			0.0005	6			0.0003	1 0
t	0.040	0.065	0.090		0.040	0.065	0.090	
N		132		3		144		3
NOTE	1,7							
REF	ITEM 10-2	290						
SSUE	A							
S			VΔR	ΙΔΤ	IONS			
Y	ļ		· V / \ \ \	T	10110	4.0		N
B		AC	•	] 6 [		AD	,	ŢÖ
SYMBOL	MIN.	NOM.	MAX.	N O T E	MIN.	NOM.	MAX.	NOTE
A		_	0.140	+		-	0.175	
A1		-	0.105		_	-	0.105	
b	0.006	0.008	0.010		0.006	0.008	0.010	
b1	0.005	0.007	0.009	6	0.005	0.007	0.009	6
С	0.004	0.006	0.008		0.004	0.006	0.008	
c1	0.003	0.005	0.007	6	0.003	0.005	0.007	6
D	1.335	1.350	1.365	1 -	1.510	1.525	1.540	
D2	1.900	1.910	1.920	1 1	2.210	2.220	2.230	
D3		_	1.930	1			2.240	
D4	1.220	1.230	1.240		1.395	1.405	1.415	
E	1.335	1.350	1.365		1.510	1.525	1.540	
E2	1.900	1.910	1.920		2.210	2.220	2.230	
E3		_	1.930			-	2.240	
E4	1.220	1.230	1.240		1.395	1.405	1.415	
f	0.015	0.035	0.045		0.015	0.035	0.045	
	0.002	0.008	0.014		0.002	0.008	0.014	
X		_	-		0.190	_		
	0.190	t		6	-	<b>-</b>	0.0005	6
X	0.190	<del> </del>	0.0005_					
X L1	<del></del>	0.065	0.0005	-	0.040	0.065	0.090	
X L1 M		- 0.065 196		3	0.040	0.065	0.090	3
L1 M					0.040		0.090	3

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JEDEC Solid State Product Outline	CERAMIC LEADED CHIP CARRIER  (.025 INCH LEAD PITCH)  WITH PLASTIC NON-CONDUCTIVE  TIE BAR	A	Sept. 1992	M0-131	4/5

## LEAD OPTIONS A

## OPTION. A OPTION B



## NOTES:

1. All dimensions are in inches.

Plastic tie bar corners with or without metal leadframe corners may be included in the "as is " shipped package.

- 3. Dimension N: Number of leads. For drawing clarity, not all leads are shown. Actual packages have a continuous array of leads.
- 4 Straight or step option.
  - 5 Plastic tie bar will not overhang lead tips.
- Dimensions b1 and c1 apply to base metal only.

  Dimension M applies to plating thickness.
- $\triangle$  Datum A-D and B- to be determined by datum points where leads contact the tie bar.
  - 8. Dimensioning and tolerancing per ANSI Y14.5M-1982.

TOP BRAZED  JEDEC CERAMIC LEADED CHIP CARRIER  Solid State Product (.025 INCH LEAD PITCH)  Outline WITH PLASTIC NON-CONDUCTIVE  TIE BAR	A	DATE Sept. 1992	MO-131	SHEET 5/5	-1
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