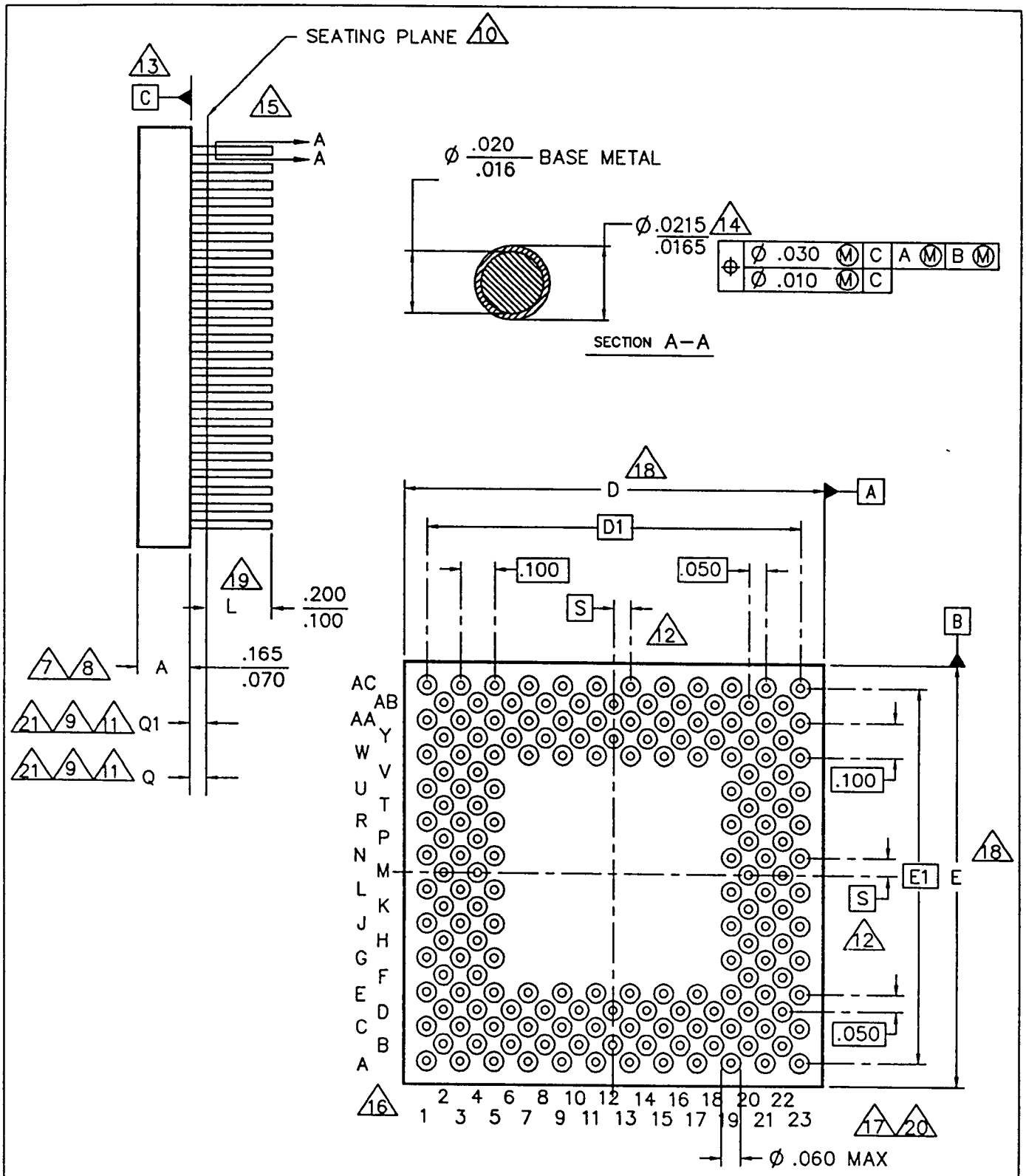

JEDEC SOLID STATE PRODUCT OUTLINES	THIS *REGISTERED OUTLINE* HAS BEEN PREPARED BY THE JEDEC JC-11 COMMITTEE AND REFLECTS A PRODUCT WITH ANTICIPATED USAGE IN THE ELECTRONICS INDUSTRY: CHANGES ARE LIKELY TO OCCUR.				
TITLE .100" CENTER STAGGERED PIN GRID ARRAY FAMILY (LARGE OUTLINE)	S-XPGA-P	ISSUE C	DATE 1/97	MO-128	SHEET 1/8

VARIATIONS

SYMBOL	AA			NOTE	AB			NOTE	AC			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
D	.940	.960	.980	18	1.040	1.060	1.080	18	1.140	1.160	1.180	18
D1		.800 BSC				.900 BSC				1.000 BSC		
E	.940	.960	.980	18	1.040	1.060	1.080	18	1.140	1.160	1.180	18
E1		.800 BSC				.900 BSC				1.000 BSC		
Q	.040	–	.075	9,11	.040	–	.075	9,11	.040	–	.075	9,11
Q1	.015	–	.075	9,11	.015	–	.075	9,11	.015	–	.075	9,11
M	–	17	–	4	–	19	–	4	–	21	–	4
N	–	–	145	5	–	–	181	5	–	–	221	5
S		.000 BSC				.050 BSC				.000 BSC		

VARIATIONS

SYMBOL	AD			NOTE	AE			NOTE	AF			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
D	1.240	1.260	1.280	18	1.340	1.360	1.380	18	1.440	1.460	1.480	18
D1		1.100 BSC				1.200 BSC				1.300 BSC		
E	1.240	1.260	1.280	18	1.340	1.360	1.380	18	1.440	1.460	1.480	18
E1		1.100 BSC				1.200 BSC				1.300 BSC		
Q	.040	–	.075	9,11	.040	–	.075	9,11	.040	–	.075	9,11
Q1	.015	–	.075	9,11	.015	–	.075	9,11	.015	–	.075	9,11
M	–	23	–	4	–	25	–	4	–	27	–	4
N	–	–	265	5	–	–	313	5	–	–	365	5
S		.050 BSC				.000 BSC				.050 BSC		

VARIATIONS

SYMBOL	AG			NOTE	AH			NOTE	AJ			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
D	1.540	1.560	1.580	18	1.640	1.660	1.680	18	1.740	1.760	1.780	18
D1		1.400 BSC				1.500 BSC				1.600 BSC		
E	1.540	1.560	1.580	18	1.640	1.660	1.680	18	1.740	1.760	1.780	18
E1		1.400 BSC				1.500 BSC				1.600 BSC		
Q	.040	–	.075	9,11	.040	–	.075	9,11	.040	–	.075	9,11
Q1	.015	–	.075	9,11	.015	–	.075	9,11	.015	–	.075	9,11
M	–	29	–	4	–	31	–	4	–	33	–	4
N	–	–	421	5	–	–	481	5	–	–	545	5
S		.000 BSC				.050 BSC				.000 BSC		

NOTE 1, 2, 3, 6, 9, 16, 20, 22

REF ITEM 10-291

ISSUE A

JEDEC Solid State Product Outline	S-XPGA-P .100" CENTER STAGGERED PIN GRID ARRAY FAMILY (LARGE OUTLINE)	ISSUE C	DATE 1/97	 MO-128	SHEET 2/8

VARIATIONS

SYMBOL	AK			NOTE	AL			NOTE	AM			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
D	1.840	1.860	1.880	18	1.940	1.960	1.980	18	2.040	2.060	2.080	18
D1		1.700 BSC				1.800 BSC				1.900 BSC		
E	1.840	1.860	1.880	18	1.940	1.960	1.980	18	2.040	2.060	2.080	18
E1		1.700 BSC				1.800 BSC				1.900 BSC		
Q	.040	–	.075	9,11	.040	–	.075	9,11	.040	–	075	9,11
Q1	.015	–	.075	9,11	.015	–	.075	9,11	.015	–	075	9,11
M	–	35	–	4	–	37	–	4	–	39	–	4
N	–	–	613	5	–	–	685	5	–	–	761	5
S		.050 BSC				.000 BSC				.050 BSC		

NOTE 1, 2, 3, 6, 9, 16, 20, 22

REF ITEM 10-291

SSUE B

VARIATIONS

SYMBOL	AN			NOTE	AP			NOTE	AQ			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
D	2.140	2.160	2.180	18	2.340	2.360	2.380	18	2.640	2.660	2.680	18
D1		2.000 BSC				2.200 BSC				2.500 BSC		
E	2.140	2.160	2.180	18	2.340	2.360	2.380	18	2.640	2.660	2.680	18
E1		2.000 BSC				2.200 BSC				2.500 BSC		
Q	.040	–	.075	9,11	.040	–	.075	9,11	.040	–	.075	9,11
Q1	.015	–	.075	9,11	.015	–	.075	9,11	.015	–	.075	9,11
M	–	41	–	4	–	45	–	4	–	51	–	4
N	–	–	841	5	–	–	1013	5	–	–	1301	5
S		.000 BSC				.000 BSC				.050 BSC		

NOTE 1, 2, 3, 6, 9, 16, 20, 22

REF ITEM 10-341

SSUE B

JEDEC Solid State Product Outline	S-XPGA-P .100" CENTER STAGGERED PIN GRID ARRAY FAMILY (LARGE OUTLINE)	ISSUE C	DATE 1/97	MO-128	SHEET 3/8

VARIATIONS

SYMBOL	BA			NOTE	BB			NOTE	BC			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
D	.940	.960	.980	18	1.040	1.060	1.080	18	1.140	1.160	1.180	18
D1		.800 BSC				.900 BSC				1.000 BSC		
E	.940	.960	.980	18	1.040	1.060	1.080	18	1.140	1.160	1.180	18
E1		.800 BSC				.900 BSC				1.000 BSC		
Q	0.0	–	0.0	21	0.0	–	0.0	21	0.0	–	0.0	21
Q1	0.0	–	0.0	21	0.0	–	0.0	21	0.0	–	0.0	21
M	–	17	–	4	–	19	–	4	–	21	–	4
N	–	–	145	5	–	–	181	5	–	–	221	5
S		.000 BSC				.050 BSC				.000 BSC		

VARIATIONS

SYMBOL	BD			NOTE	BE			NOTE	BF			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
D	1.240	1.260	1.280	18	1.340	1.360	1.380	18	1.440	1.460	1.480	18
D1		1.100 BSC				1.200 BSC				1.300 BSC		
E	1.240	1.260	1.280	18	1.340	1.360	1.380	18	1.440	1.460	1.480	18
E1		1.100 BSC				1.200 BSC				1.300 BSC		
Q	0.0	–	0.0	21	0.0	–	0.0	21	0.0	–	0.0	21
Q1	0.0	–	0.0	21	0.0	–	0.0	21	0.0	–	0.0	21
M	–	23	–	4	–	25	–	4	–	27	–	4
N	–	–	265	5	–	–	313	5	–	–	365	5
S		.050 BSC				.000 BSC				.050 BSC		

VARIATIONS

SYMBOL	BG			NOTE	BH			NOTE	BJ			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
D	1.540	1.560	1.580	18	1.640	1.660	1.680	18	1.740	1.760	1.780	18
D1		1.400 BSC				1.500 BSC				1.600 BSC		
E	1.540	1.560	1.580	18	1.640	1.660	1.680	18	1.740	1.760	1.780	18
E1		1.400 BSC				1.500 BSC				1.600 BSC		
Q	0.0	–	0.0	21	0.0	–	0.0	21	0.0	–	0.0	21
Q1	0.0	–	0.0	21	0.0	–	0.0	21	0.0	–	0.0	21
M	–	29	–	4	–	31	–	4	–	33	–	4
N	–	–	421	5	–	–	481	5	–	–	545	5
S		.000 BSC				.050 BSC				.000 BSC		

NOTE 1, 2, 3, 6, 9, 16, 20, 22

REF ITEM 10-341

ISSUE B

JEDEC Solid State Product Outline	S-XPGA-P .100" CENTER STAGGERED PIN GRID ARRAY FAMILY (LARGE OUTLINE)	ISSUE C	DATE 1/97	MO-128	SHEET 4/8

VARIATIONS

SYMBOL	BK			NOTE	BL			NOTE	BM			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
D	1.840	1.860	1.880	18	1.940	1.960	1.980	18	2.040	2.060	2.080	18
D1		1.700 BSC				1.800 BSC				1.900 BSC		
E	1.840	1.860	1.880	18	1.940	1.960	1.980	18	2.040	2.060	2.080	18
E1		1.700 BSC				1.800 BSC				1.900 BSC		
Q	0.0	–	0.0	21	0.0	–	0.0	21	0.0	–	0.0	21
Q1	0.0	–	0.0	21	0.0	–	0.0	21	0.0	–	0.0	21
M	–	35	–	4	–	37	–	4	–	39	–	4
N	–	–	613	5	–	–	685	5	–	–	761	5
S		.050 BSC				.000 BSC				.050 BSC		

VARIATIONS

SYMBOL	BN			NOTE	BP			NOTE	BQ			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
D	2.140	2.160	2.180	18	2.340	2.360	2.380	18	2.640	2.660	2.680	18
D1		2.000 BSC				2.200 BSC				2.500 BSC		
E	2.140	2.160	2.180	18	2.340	2.360	2.380	18	2.640	2.660	2.680	18
E1		2.000 BSC				2.200 BSC				2.500 BSC		
Q	0.0	–	0.0	21	0.0	–	0.0	21	0.0	–	0.0	21
Q1	0.0	–	0.0	21	0.0	–	0.0	21	0.0	–	0.0	21
M	–	41	–	4	–	45	–	4	–	51	–	4
N	–	–	841	5	–	–	1013	5	–	–	1301	5
S		.000 BSC				.000 BSC				.050 BSC		

NOTE 1, 2, 3, 6, 9, 16, 20, 22

REF ITEM 10-341

ISSUE B

JEDEC Solid State Product Outline	S-XPGA-P .100" CENTER STAGGERED PIN GRID ARRAY FAMILY (LARGE OUTLINE)	ISSUE C	DATE 1/97	MO-128	SHEET 5/8

NOTES:

1 DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

2 ALL DIMENSIONS IN INCHES.

3 TERMINAL POSITION DESIGNATION PER JEDEC PUBLICATION 95-1, SPP-010.

4 "M" REPRESENTS THE PIN MATRIX SIZE.

5 "N" REPRESENTS THE MAXIMUM ALLOWABLE NUMBER OF PINS.

6 23 x 23 MATRIX SIZES ARE SHOWN FOR ILLUSTRATION ONLY.

7 DIMENSION "A" INCLUDES THE PACKAGE BODY AND LID FOR BOTH CAVITY UP AND DOWN CONFIGURATIONS. (SEE REFERENCE DRAWING ON THE NEXT PAGE).

8 DIMENSION "A" DOES NOT INCLUDE INTEGRAL HEATSINK OR ATTACHED FEATURES.

9 STANDOFFS FOR VARIATIONS AA-AQ SHOULD BE LOCATED ON THE PIN MATRIX DIAGONALS.

10 THE SEATING PLANE IS THE OUTER STANDOFF SURFACE FACING AWAY FROM THE THE CERAMIC BODY FOR VARIATIONS AA-AQ. THE SEATING PLANE IS THE CERAMIC BODY SURFACE OR LID FOR VARIATIONS BA-BQ.

11 DIMENSION "Q" APPLIES TO CAVITY UP CONFIGURATION ONLY.
DIMENSION "Q1" APPLIES TO CAVITY DOWN CONFIGURATION ONLY.
(SEE REFERENCE DRAWING ON THE NEXT PAGE).

12 [S] IS MEASURED WITH RESPECT TO DATUM A AND DATUM B AND DEFINES THE POSITION OF THE CENTER PIN IN THE OUTER ROW, WHEN THERE IS AN ODD NUMBER OF PINS IN THE OUTER ROW, [S] = .000", WHEN AN EVEN NUMBER ARE USED, [S] = .050". ALL PINS IN A GIVEN ROW MUST BE ON A .100" GRID. ADJACENT ROWS OFFSET BY .050".

13 DATUM C IS THE PLANE OF PIN TO PACKAGE INTERFACE FOR BOTH CAVITY UP AND DOWN CONFIGURATIONS. (SEE REFERENCE DRAWING ON THE NEXT PAGE).

14 PIN DIAMETER INCLUDES SOLDER DIP OR CUSTOM FINISH.

15 PIN TIPS MAY REQUIRE A RADIUS OR CHAMFER WHEN USED WITH A SOCKET PER THE ATTACHED APPLICATIONS NOTE.

16 THERE MUST BE SOME TYPE OF A1 CORNER IDENTIFICATION ON BOTH TOP AND BOTTOM SURFACES OF THE PACKAGE. ID TYPE IS OPTIONAL AND MAY CONSIST OF NOTCHES, ID PINS, METALLIZED MARKINGS OR OTHER FEATURES. THE FEATURES USED ON EACH SURFACE MAY BE OF DIFFERING TYPES.

17 THERE MUST BE .010" MINIMUM SPACING BETWEEN ANY TWO METALLIZED FEATURES ON THE PACKAGE.

18 DIMENSION "D" AND "E" DO NOT INCLUDE CERAMIC PROTRUSIONS. SUCH PROTRUSIONS MAY NOT EXCEED MORE THAN .003" ON ANY SIDE. CORNERS OF THE PACKAGE BODY MAY HAVE CHAMFERS FOR MECHANICAL PROTECTION OR IDENTIFICATION.

19 IN SOME APPLICATIONS A HIGHER MINIMUM PIN LENGTH MAY BE REQUIRED PER THE ATTACHED APPLICATION NOTE.

20 THIS DIMENSION DEFINES THE MAXIMUM SIZE FOR THE BRAZE PADS, PINS MUST BE POSITIONED ENTIRELY ON THE BRAZE PADS.

21 THERE ARE NO STANDOFF PINS ON VARIATIONS BA THROUGH BQ.

22 THE PACKAGE DESIGNATOR DOES NOT SPECIFY A MATERIAL. THE MATERIAL IS THE MANUFACTURER'S OPTION. THIS REGISTRATION WAS ORIGINALLY DEVELOPED FOR CERAMIC DESIGNS.

JEDEC Solid State Product Outline	S-XPGA-P .100" CENTER STAGGERED PIN GRID ARRAY FAMILY (LARGE OUTLINE)	ISSUE	DATE		SHEET
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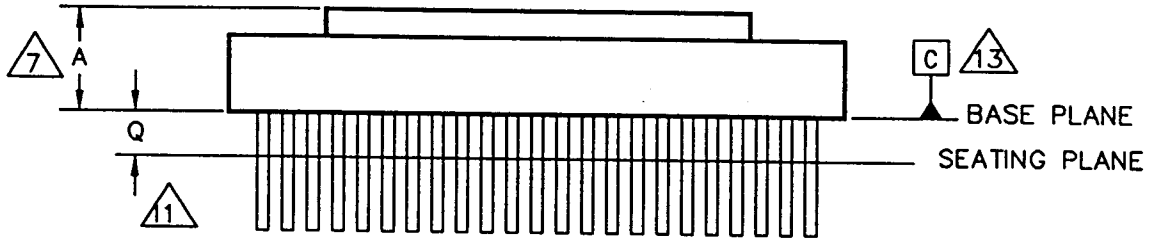
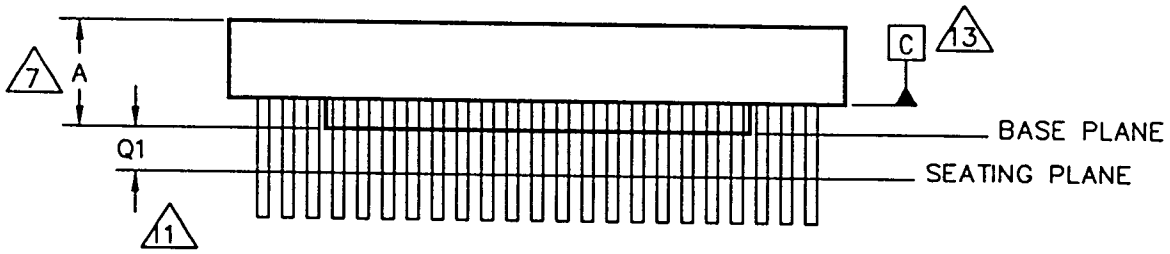
REFERENCE DRAWING

CAVITY UP



CAVITY DOWN



JEDEC Solid State Product Outline	S-XPGA-P .100" CENTER STAGGERED PIN GRID ARRAY FAMILY (LARGE OUTLINE)	ISSUE C	DATE 1/97	MO-128	SHEET 7/8

APPLICATION NOTES:

1. FOR APPLICATIONS WHERE A PGA PACKAGE IS USED IN A SOCKET.
   THE FOLLOWING REQUIREMENTS MAY APPLY.
   A. PIN TIPS MUST HAVE A RADIUS OR CHAMFER.
   B. STANDOFF HEIGHT MUST BE IN THE RANGE .055"/.045"
      FOR VARIATIONS AA–AQ.
   C. RECOMMENDED MINIMUM PIN LENGTH (DIMENSION "L") SHOULD BE .115".
   D. RECOMMENDED MAXIMUM PIN DIAMETER INCLUDING FINISH SHOULD BE .020".

2. FOR MILITARY APPLICATIONS THE PIN LENGTH (DIMENSION "L") RANGE
   MAY BE RESTRICTED TO .120"/.140".

3. ALL VARIATIONS ARE SUITABLE FOR SINGLE AND MULTICHIP APPLICATIONS.