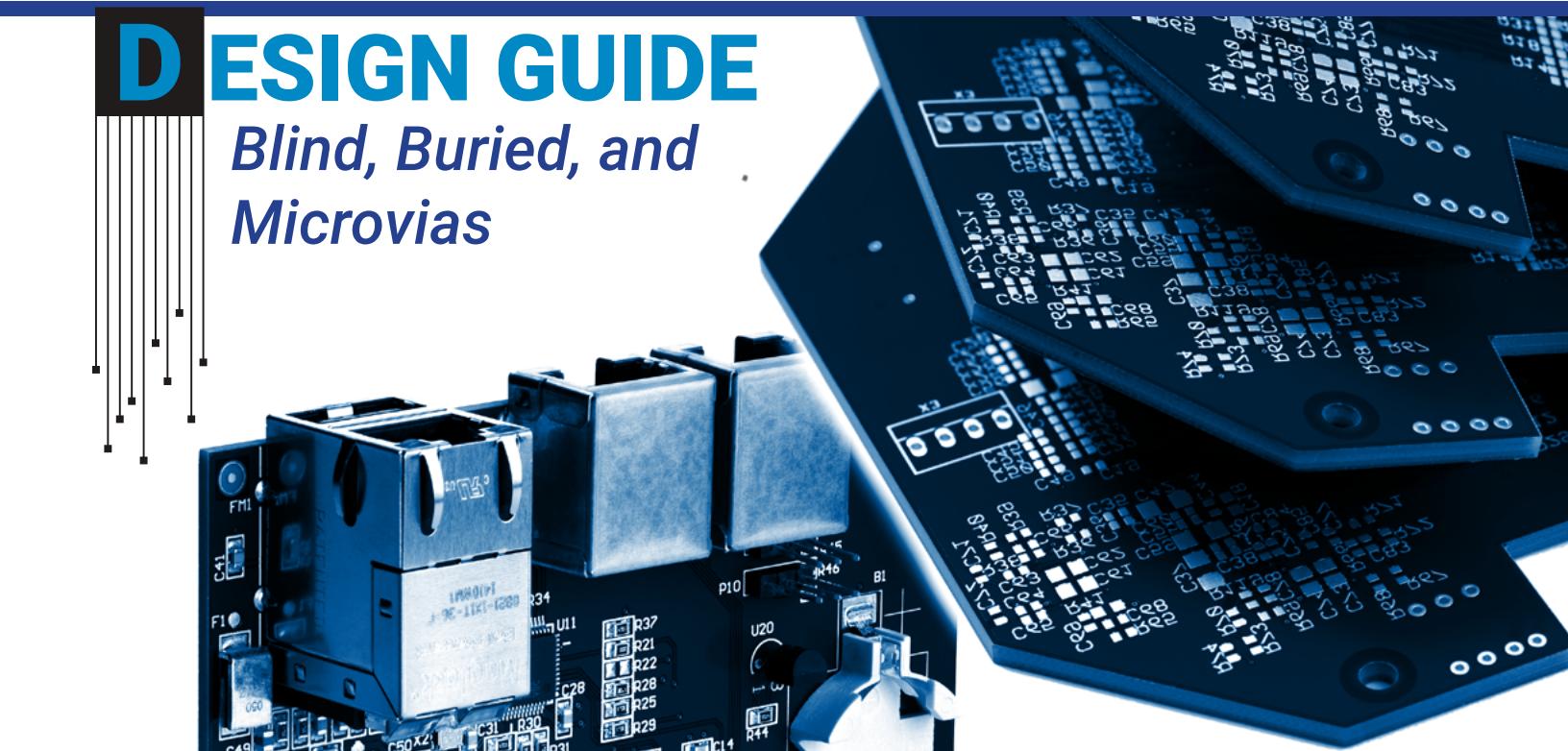


# HDI

## HIGH-DENSITY INTERCONNECT

### DESIGN GUIDE

*Blind, Buried, and  
Microvias*



# FOREWORD

Written by Happy Holden



Sierra Circuits has once again led the industry by introducing a comprehensive HDI Design Guide. This is characteristic of their support for printed circuit designers and electrical engineers. Like their excellent HDI Stackup Planner tool that is available on the Internet (an Industry FIRST), this design guide thoroughly explains the benefits of using high density interconnects, in this case, microvias.

I have never read in one place such a thoroughly researched design guide. There may be more complicated or more detailed HDI information available (like my HDI HANDBOOK-at 681 pages), but not in such an easy to read and understandable volume as this is. I hope you will use the advice presented here to successfully implement HDI in your boards and encourage others to download the design guide and use it also.

The "e-Book" format of this guide is also an important step towards making this book useful, not just for the present, but, also, into the future.

HDI is a fast-moving technology, and in some respects combines the elements of both "revolutionary" and "evolutionary" technology changes.

This format will allow the Editor, to update material as appropriate, keeping it fresh and pertinent at the leading edge of the technology.

Integrated circuit technology will continue to drive those devices into ever smaller and denser packages with increasing interconnection points. This will continue to make HDI technologies more and more "main stream," or standard printed circuit design, fabrication and assembly elements. Success in dealing with these issues will be critical to the success in the market place for electronic products. This e-Book will help the reader get the most out of HDI and make it work for you.

# Table of Contents

1. OVERVIEW	
1.1 What is HDI? .....	4
1.2 What is driving the increase preference for HDI PCBs? .....	8
1.3 The cost of HDI.....	9
1.4 What can go wrong?.....	11
2. THE KEY TO HDI PCB DESIGN SUCCESS	
2.1 The benefits of a planned approach.....	12
2.2 Choose the right PCB material.....	13
2.3 Have a plan for your PCB stack-up and microvia structure.....	17
2.3.1 HDI stack-up classes.....	18
2.3.2 Stacked vs staggered vias.....	22
2.4 Key considerations in your HDI PCB design strategy.....	24
3. SIGNAL INTEGRITY FOR HDI	
3.1 Signal quality of one net.....	27
3.2 Crosstalk noise.....	28
3.3 The constraints of controlled impedance.....	31
4. MANUFACTURING FOR HDI	
4.1 Layers and laminations.....	33
4.2 Mechanical vs laser drill.....	34
4.2.1 Laser drilled microvias.....	35
4.3 Hole fill process.....	35
4.4 Drill-to-copper.....	36
4.5 Landless via technology.....	37
4.6 Surface finishes.....	39
4.7 BGA breakout and fanout strategy.....	40
4.7.1 Example of how to breakout a .4mm BGA.....	41
4.7.2 Example of how to breakout a .5mm BGA.....	43
5. SIERRA CIRCUITS' CAPABILITIES	
5.1 Sierra Circuits' preferred materials.....	46
5.2 Sierra Circuit's HDI Stackup Planner online tool.....	47
5.3 HDI Stackup Planner tutorial.....	47
5.4 About Sierra Circuits.....	49

# 1. Overview

## 1.1 What is HDI?

### High-Density Interconnect

- HDI is characterized by its high density of components and routing interconnections.
- HDI uses microvias, blind and buried via/microvia techniques, as well as built-up PCB laminations.
- Microvias have an aspect ratio of less than 1:1.
- HDI design reduces the overall cost by decreasing the number of layers and size as compared to a standard technology PCB design.
- HDI offers a better electrical performance.

HDI stands for High-Density Interconnect. As the name suggests, an HDI PCB is characterized by its high density of components and routing interconnections that use the latest PCB technologies. An HDI design is by its very nature a high-performance design.

**HDI design uses the latest advances in the PCB interconnection technology.** Keeping in mind the latest state of the art PCB technology, we can define the HDI PCBs as those printed circuit boards that use some or all of these features: microvias, blind and buried via/microvia techniques, built-up PCB laminations and high-signal performance considerations.

## What is 'high-density'?

Happen Holden told us, "The definition may vary, but experienced designers usually consider 120-160 average pins per square inch to be 'high-density'. The amount of density (or complexity) of a printed circuit,  $W_d$ , as measured by the average length of traces per square inch of that board, including all signal layers. The metric is inches per square inch. The PWB density was derived by assuming an average of three electrical nodes per net and that the component lead was a node of a net. The result was an equation that says the PWB density is  $\beta$  times the square root of the parts per square inch times the average leads per part.  $\beta$  is 2.5 for the high analog/discrete region, 3.0 for the analog/digital region and 3.5 for the digital/ASIC region:

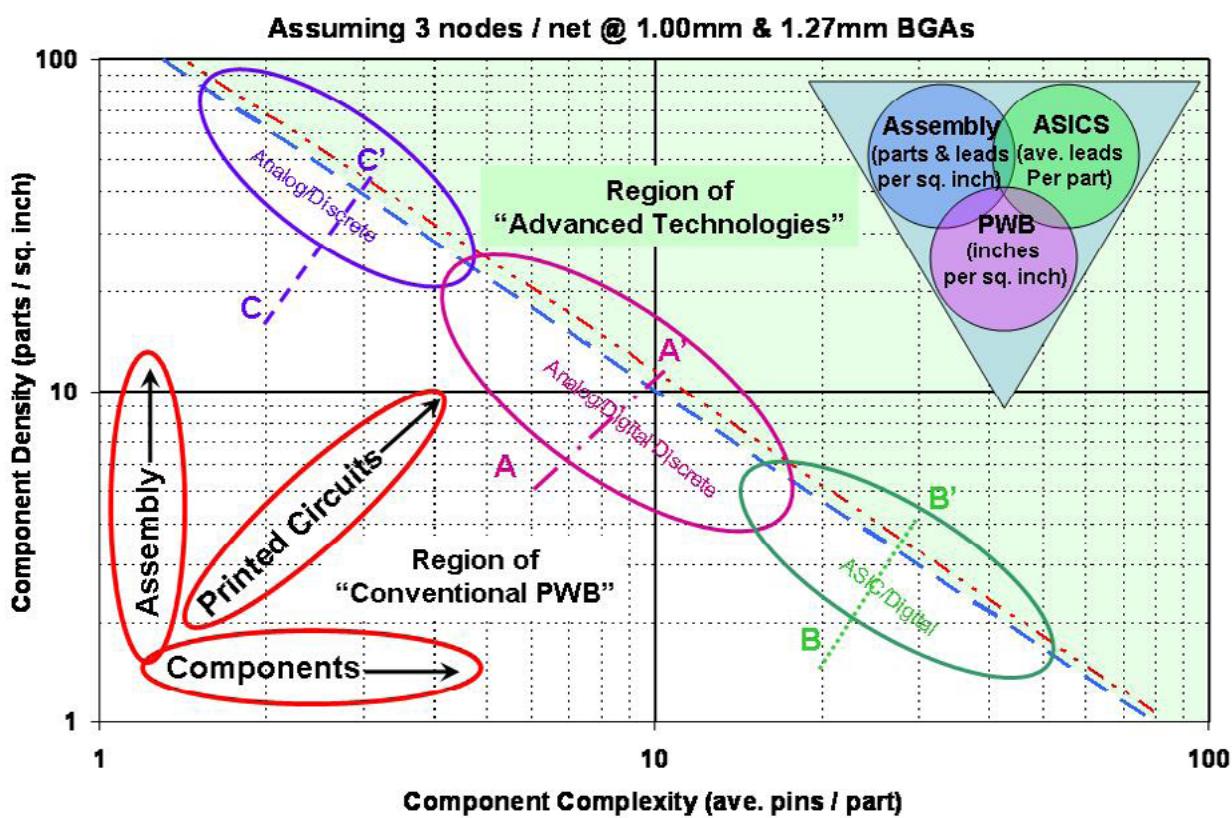
$$\begin{aligned} \text{PWB Density } (W_d) &= \beta \sqrt{([Cd]) \times (Cc)} \\ &= \beta \sqrt{[(\text{parts per sq.in.})] \times (\text{ave.leads per part})} \end{aligned}$$

Where:

$Cd$  = component density = ave. parts per sq. inch for a design

$Cc$  = component complexity = ave. leads per part

PWB Density ( $W_d$ ) =  $\beta \times Cc \times (Cd)^{.5}$



© Happy Holden

# 1

The table below shows the advantage of using HDI staggered microvias over through-holes in terms of cost and pin density:

THRU-HOLE VS. STAGGERED MICROVIA HDI: COST & PIN DENSITY														
ID	A		B		C		D		E		F		G	
Type	THRU-HOLE		1 BUILD-UP Blind		1 BUILD-UP Blind & Buried		1 BUILD-UP Blind & Buried		2 BUILD-UP Blind		2 BUILD-UP Blind & Buried		2 BUILD-UP Blind & Buried	
Stackup	N		1+N+1		1+bN+1		1+bN+1		2+N+2		2+bN+2		2+bN+2	
Micro Vias	none		L1-L2		L1-L2		skip via L1-L3 stagger L1-L2, L2-L3		stagger L1-L2, L2-L3		stagger L1-L2, L2-L3		stagger L1-L2, L2-L3	
Buried Vias	none		none		L2-L(N-1)		L2-L(N-1)		none		L2-L(N-1)		L3-L(N-2)	
Stackup & Via Models														
Signal Layers	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN
4L	0.6	20	0.8	40	1.1	40	1.3	40	1.4	135	--	--	--	--
6L	0.8	20	1.0	60	1.2	60	1.5	60	1.6	180	1.7	220	1.9	240
8L	1.0	30	1.2	100	1.5	100	1.7	100	1.9	240	2.1	240	2.3	300
10L	1.3	40	1.5	200	1.8	180	2.1	180	2.3	300	2.5	300	2.7	400
12L	1.7	60	1.9	210	2.3	220	2.6	220	3	350	3	500	3	500
14L	2.2	70	2.5	220	3	250	3	260	4	400	4	600	4	600
16L	3	80	3	260	4	300	4	300	5	500	5	800	5	800
18L	4	100	4	300	5	330	5	350	6	600	6	1000	7	1000
20L	5	105	5	360	6	380	7	400	8	700	8	1200	9	1200
22L	7	110	7	400	8	425	9	450	10	800	10	1300	11	1300
24L	9	125	9	460	10	480	11	500	12	1000	13	1400	14	1400
26L	11	130	11	500	13	550	14	600	15	1200	16	1500	17	1600
28L	13	135	14	540	16	620	17	700	18	1300	19	1600	29	1800
30L	16	140	17	580	18	690	20	800	21	1400	22	1650	23	2000
32L	18	145	19	620	21	770	23	900	24	1450	25	1700		
34L	21	150	22	660	24	900	26	1200	26	1500	27	1800		
36L	23	160	24	700	26	1000					30	2000		
38L	25	180	26	740	RCI = Relative Cost Index									
40L	26	200			DEN = Density: Pins/Square Inch									© Happy Holden 2006-2011

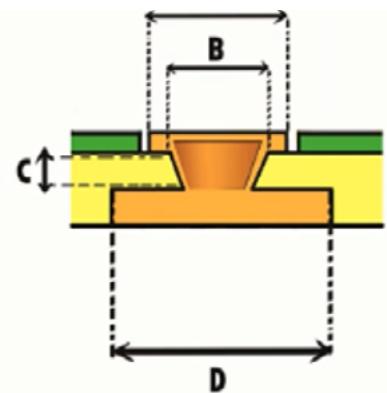
HDI became a thing in the 1990s as the consumer market started to ask for electronic products capable of supporting new features and capabilities – which means additional components and circuitry – while displaying smaller footprints and lower power consumption (typically measured in terms of battery life). HDI improved the way components were mounted and connected using the microvia technique. Until the late 1980s, most PCB manufacturers could only build through-holes that pass all the way through the board and have an aspect ratio (the ratio of the board thickness to the diameter of the drilled hole) from 6:1 to 20:1. Microvias have an aspect ratio of less than 1:1 and therefore perform with many times the thermal cycle life of the through-hole vias.

The chart below gives some aspect ratio guidelines:

## ASPECT RATIO OF LASER-DRILL MICROVIAS

- RATIO OF LASER MICROVIA = C/B:1
- MOST PRODUCTIVE AND COST-EFFECTIVE A/R IS .75:1 OR LESS

Microvia Hole Diameter	Maximum Dielectric Layer Thickness (mils)			
	A/R = 0.5	A/R = 0.75	A/R = 0.9	A/R = 1
6.00	3.0	4.50	5.40	6.00
5.00	2.5	3.75	4.50	5.00
4.00	2.0	3.00	3.60	4.00
3.00	1.5	2.25	2.70	3.00
2.00	1.0	1.50	1.80	2.00

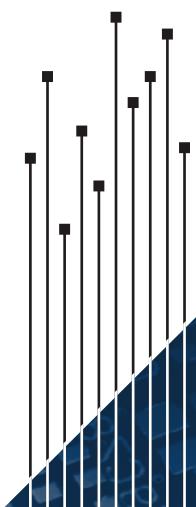


Microvias connect embedded capacitors and resistors within the layers of an HDI PCB. Reducing the distance and the mass of the conductive material improves electrical performance in compact, complex devices.

One of the key driving factors is to achieve more connections per area of the printed circuit board. This results in a more compact, dense, and lower layer count PCBs.

Not only does it make the PCBs smaller, lighter, and thinner; but HDI PCBs provide a much superior electrical performance, including:

- Better electrical performance and signal integrity
- Lower noise and crosstalk, and lower EMI/RFI
- Smaller size and weight
- **Cost optimization:** HDI design reduces the overall cost by decreasing the number of layers and size as compared to a standard technology PCB design for the same level of complexity.
- **Reduced design time:** HDI technology allows for more real estate on the board which results in faster signal routing during the layout design stage.
- **More reliable designs:** Studies conducted by IPC and other industry organizations have talked about superior reliability of small-blind vias over through-hole vias. This is due to the fact that the via aspect ratio is less than 1:1 compared to through-hole which has an aspect ratio greater than 6:1 that goes as high as 20:1.



# 1

## 1.2 What is driving the increase preference for HDI PCBs?

HDI provides a smarter solution.

- **HDI offers high-pin count and high-density device packages.**
- **HDI means smaller PCB sizes and a reduced number of PCB layers.**

HDI allows for dense component placement and more versatile routing in a PCB. The main benefit of HDI is that it reduces drill-to-copper. Using blind and buried vias allows designers to avoid denser areas of the board, which in turn means the denser circuitry is routed cleaner.

Compared with traditional PCBs, HDI PCBs have thinner trace widths and superior wiring density. They achieve these advantages through the use of technologies such as buried vias, blind vias, stacked, and staggered laser-drilled microvias.

Another note on microvias: Their extremely small pad size helps to boost channel routing width. Layer reduction is possible since through-holes may be replaced with microvias, allowing signal layers along with their corresponding reference planes to be eliminated. It's the PCB version of hitting two birds with one stone.

PCB designers also cite the following reasons for the increased adoption of HDI:

- **Complex and dense devices:** High-pin count and high-density device packages such as ball grid arrays (BGA), chip-scale packaging (CSP), wire-bond and flip chip BGAs, chip-on-board (COB), and system-in-package (SiP) are leading factors. When a complex and dense device has a large pin count and a very low pitch, it is almost impossible to design a PCB with a reasonable number of layers and/or thickness using standard PCB technology. The solution? HDI!
- **Compact PCBs:** As everything gets smaller, faster and cheaper at an ever increasing rate, the designers are faced with increasingly smaller PCB sizes and a reduced number of PCB layers. If one were to use conventional non-HDI designs, many would require a large number of PCB layers. HDI provides a smarter solution.
- **Integrating several PCBs into a single PCB:** With HDI, several existing PCBs can be integrated into a single high-density PCB in a more efficient manner.

• **Signal integrity discipline:** As PCBs have incorporated circuits that require higher speed signal transitions, faster rise/fall times, and higher clock rates, it requires even higher signal integrity levels and electrical performance. These require a high degree of signal integrity discipline to be implemented during the PCB design and manufacturing, which HDI provides. HDI inherently provides a better signal integrity performance than non-HDI because all the stray capacitances and inductances get reduced when using small vias. And because there are no stubs, the impedance of microvias is nearer to the traces impedance. The stray capacitance of a normal via is much higher, which causes greater discontinuity in impedance than a microvia does.

Try our free HDI Stackup Planner to estimate the cost of your design and see whether or not you need HDI.

### Making HDI work for you – The first step!

A good rule of thumb is to ask yourself, "Will HDI PCB technology solve a real problem and serve a real purpose in my design?" You should know exactly why you need HDI PCB technology in your PCB at the very beginning of the design process. We have provided some examples of when you should consider HDI PCB technology. Whatever your reasons, it is imperative that you are very

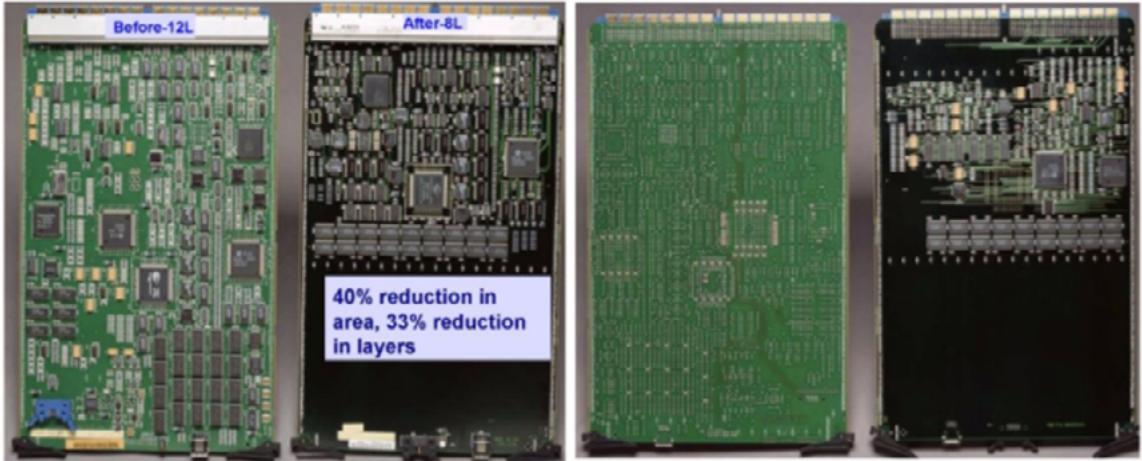
## 1.3 The cost of HDI

### What is the cost of a risky design?

- More laminations equal more cost.
- Yield is the paramount cost consideration.
- Your manufacturer might not get it right the first time.

It is true that more laminations equal more cost. However, when designing your board, you should keep in mind that adding layer after layer and making holes smaller and smaller as your circuit designs become more complex does not make any sense and will eventually cost you more. Over the years, Sierra Circuits has seen many PCB designers gambling on high via aspect ratios and tight hole-to-copper clearance instead of turning to a blind-and-buried via architecture, which would have been more effective. Why not choose to design your boards in an HDI manner, achieve 8-mil hole-to-copper clearances, instead of 4 mils, with through-hole aspect ratios that are 8:1, instead of 20:1, and use fewer layers?

# 1



*The benefit of HDI: The green PCB on the left is a conventional 12-layer through-hole controlled impedance design. The black PCB shows the benchmarked 8-layer HDI redesign, which saved 40% in surface area and 33% in layer depth with the same function. © Copyright 2001 Westwood Associates.*

HDI can make you save money when it comes to manufacturing. Once a job is quoted and accepted by a PCB shop, the fabricator has to deliver the number of boards requested, even if they push the edge of process tolerances. Let's say you ordered 10 twelve-layer boards with 3-mil drill-to-copper clearance. The manufacturer would probably have to produce 20 boards in order to just yield 10 that are acceptable. Perhaps the job would have to be run twice. And perhaps the temperature cycling would cause 8 out of these 10 good boards to short during use. The PCB shop would have to absorb the waste on this order but if you need another batch, you will be billed more to compensate for the loss on the previous batch. You could think of going to another PCB shop, but you know that it is unlikely that you would have time to start all over again. Inevitably, yield is the paramount cost consideration in PCBs.

Do not make the mistake to believe that you can keep adding layers, making everything smaller, and think that the manufacturer will find a way to produce your boards and get it right the first time. This is when you are supposed to think strategically and concentrate on yield from the beginning. If you focus on the lowest installed cost, at some level of circuit complexity, you will have to carefully assess the cost of HDI construction versus not using HDI.

Happy Holden revealed, "The thing we like to tell people is that an optimized HDI board can cost less than a through-hole board, and offer more reliability and higher electrical performance. But it does not happen by accident. It takes a lot of skill and experience. We hear, 'I don't use HDI because it costs too much.' It only costs too much because the designer has to learn how to take advantage of HDI. It can cost less or be the same, but it depends on the designer's education."

## “ Rick Hartley, Principal Engineer at RHartley Enterprises:

*The only disadvantage of HDI is a cost increase in the bare board. However that only happens when layer count is not reduced. With proper planning, cost of an HDI board can be the same or less than an all through-via board.*

## 1.4 What can go wrong?

Before designing begins, figure out if you require HDI, and how it will benefit you.

- Why do I need HDI?
- What materials should I use?
- Think about the testability of your board.

HDI as a forethought reduces your cost and gives you better electrical performance. HDI as an afterthought increases your cost.

HDI designs require upfront planning. We often see designs where laser drills and blind vias have been added at the last step. This is typical, because people do not necessarily want to design HDI. They are designing a finer chip or they are putting more parts together, and they get the board 80% - 90% completed and they are via starved. They have run out of places for vias. The only way to finish the design is to add hundreds of laser-drilled blind vias. That will certainly work, but that is the worst-case-scenario in terms of cost. You are paying for HDI but you are not fully benefiting from any of HDI's advantages. HDI really requires that you plan for HDI design far before you start to turn on the CAD system. In other words, what are my design rules? What are my materials? Do I require HDI? What are the reasons why I require HDI? Is it for higher wiring density? Better signal integrity and electrical performance? Smaller size?

**“ Steve Watt, Manager of PCB Engineering at Zuken:**

*Understand the rules of your manufacturer and how that correlates to the intent of your PCB design. Ensure that the DRCs that control your design tool are properly aligned with the above to create the most producible design possible and cut down on getting into a change loop with the manufacturer.*

HDI testability: How to ensure success on your first HDI design

As a designer, the testability of your board should always be taken into consideration. When you use blind and buried vias and you begin eliminating through-holes, testability is even more crucial. So have test pads for your critical nets.

Happy Holden advises that the first HDI board you should ever design should be a test vehicle, where you test the functionality and guarantee testability, reliability, signal integrity and power integrity.

# 2

## 2. The Key to HDI PCB Design Success



As a designer, the first step in the HDI design workflow is to determine whether or not you need HDI. You should have an idea by looking at your schematic and your target board. In doubt, use our [HDI Stackup Planner](#) in the Tools section on our website to find out. You can follow our tutorial in section 5.2.

Once you determine that you require HDI, you need to look at the stack-up. Don't use more than three sequential layers unless there is absolutely no other solution. We recommend that you use a good fanout strategy for complex ICs, like BGAs and QFNs – this will help you reduce the number of sequential laminations if you plan your fanout strategy properly. See our section 4.7.

Check whether or not you need controlled impedance. If the line length:  $l < \frac{\lambda_m}{6}$  (where  $\lambda_m$  is the rise-time of the highest frequency component in the signal), you have a shortline and it is not necessary to consider its transmission line effects, nor to design it as a controlled impedance line. But if the line length  $> \frac{\lambda_m}{6}$ , it then becomes necessary to consider the transmission line effects and to design such lines as controlled impedance lines. In this case, it is important that you understand the built-up layers copper characteristics to model the controlled impedance traces on these layers.

Built-up layers are like outer layers – they start with foil and get plated up. Stacked vias have outer plating step. Talk to your manufacturer to learn more.

### 2.1 The benefits of a planned approach

Plan ahead and avoid having to redesign from scratch.

- A planned approach will result in a design that performs as expected and is on budget.
- Planning ahead will speed up the design process.

There are no shortcuts when it comes to HDI design. High-density interconnect PCBs are more complex than standard PCBs. It is, therefore, very important that you plan out your HDI design process and other considerations well in advance. Warning: It is very difficult in HDI designs to implement major changes in the PCB structure as an afterthought!

At Sierra Circuits, we have often seen how designers new to HDI design end up redesigning from scratch after spending weeks on the first attempt. Often, their design becomes very expensive for fabrication.

A well thought out approach, on the other hand, results in a design that not only performs as expected, but is also on budget. Here are some key benefits to planning your HDI designs:

- **Avoid costly design iterations:** Once design strategies are made with a proper understanding of budget and manufacturing cycle time, you will be able to avoid costly design iterations. Your design will likely be more optimal in terms of electrical performance and you will have better control over the manufacturing. Our [HDI Stackup Planner](#) tool gives stack-ups as well as relative costs.

- **Optimal Design:** With a planned approach, even if you have had to add or reduce the number of signal layers, it will not leave you with a stack-up structure so constrained that the design never finishes, becomes suboptimal, or is difficult to manufacture. You will also have realistic expectations and avoid unpleasant surprises for all the important design determinants, such as the number of layers, lamination cycles, trace and space sizes, and via and pad sizes.

- **Faster:** Using a planned approach speeds up the design process significantly while also staying in budget. It is our hope that our planned approach will give you insight into whether using HDI design guidelines will reduce your layer count significantly, or if using HDI design is absolutely necessary. It will also allow you to compare your options right at the beginning.

Sierra Circuits has a team of stack-up designers who are available for you to discuss your trade-offs.

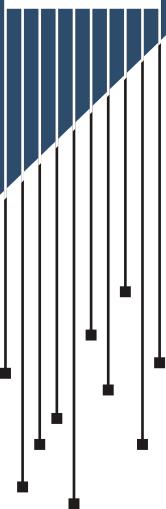
## 2.2 Choose the right PCB material

Will your material meet your temperature and electrical requirements?

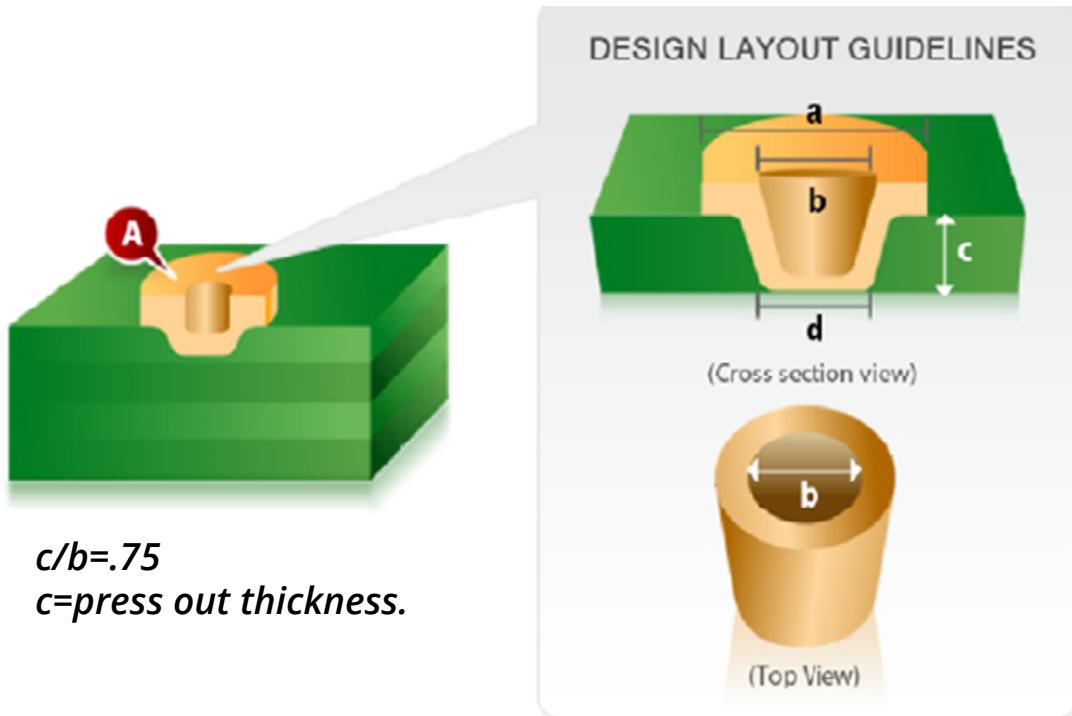
- Is your high-speed material suitable for sequential laminations?
- Materials will affect the electrical performance of the signal traces.
- The dielectric loss plays a vital role in material selection.

Material selection is, of course, important for all PCB designs. It is especially important for HDI PCB manufacturing because there are additional manufacturing constraints that play a role. The goal is always to select the right material for manufacturability that, at the same time, meets your temperature, and your electrical requirements. Also, make sure that your high-speed material is also suitable for your HDI design. There are many other factors that come into play when selecting the proper materials for your design.

# 2



Proper material selection is important for the layout design since materials will affect the electrical performance of the signal traces. The physical thickness of the material is important when considering the aspect ratio of the microvia to be plated. The current standard aspect ratio for a microvia is 0.75:1. (The microvia diameter should be larger than the height of the material it is penetrating to the next adjacent layer.)



The PCB manufacturer makes sure your materials come in required thickness to achieve .75 aspect ratio.

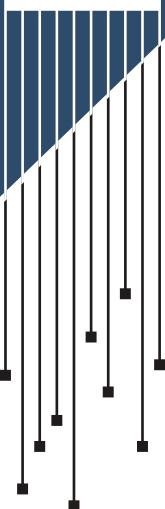
Other material considerations are the maximum withstand temperature, maximum frequency of signals and coefficients of thermal expansion (CTE). The maximum temperature here refers to that temperature which the PCB is required to withstand without affecting its mechanical integrity. It is usually expressed in degrees Celsius. The maximum frequency refers to the highest frequency that the electrical signals realized on the PCB are operating at. This is usually expressed in MHz or GHz. Our engineering staff will ask you the fastest rise/fall time during the circuit operation and help narrow down the selection of materials that would meet your requirements.

Along with these items, the dielectric constant of the material and the dielectric loss, or dissipation factor, will also play vital roles in material selection.

HDI TOPIC	PCB MATERIAL MAXIMUM TEMPERATURE
What Does it Mean?	The maximum temperature refers to the temperature which the PCB is required to withstand without affecting its mechanical integrity. It is usually expressed in Degrees Celsius.
Why is it Needed?	A PCB dielectric material, when subjected to higher temperatures, may become plastic or glassy. The useful operating temperature range is below the temperature where it starts degrading into a plastic material.
Where Can We Find it?	For a Quick Selection, refer to the "Sierra Quick Material Selection Guide", and the "Sierra PCB Material Information Sheet". They provide very detailed information on most of PCB materials and their properties.
How Do We Use it?	Choose a PCB material whose Tg (Glass transition temperature) is more than or equal to the maximum withstanding temperature required for the PCB. For example: If Top = 200 degC, choose a PCB material whose Tg $\geq$ 200 degC
Working Example:	If Top = 200 degC, choose a PCB material whose Tg $\geq$ 200 degC referring to the material sheet, the following materials were found to have a Tg of $\geq$ 200 degC <ul style="list-style-type: none"> <li>FR408HR              Tg=200</li> <li>N4000-13              Tg=210</li> <li>IS620                  Tg=220</li> <li>N9000-13              Tg=220</li> <li>N7000                  Tg=250</li> <li>RO4003/4350           Tg=270</li> </ul>
Additional Considerations: What Next?	For PCB material selection, another important consideration is the Highest Frequency at which the electrical circuit of the PCB will be operating at.

If you choose a high-speed material, make sure it is suitable for sequential laminations. When using high-speed materials like Rogers 3000, it is difficult to go through more than one lamination, it is very hard to predict the material movement and make the material really bond well. The material Sierra Circuits recommends for high-speed HDI is Megtron, Isola I-speed, etc.

# 2



When you are designing your stack-up for HDI, know where your cores are and know which ones are your prepreg layers so when you are doing your controlled impedance structure you have an idea of what the possible variation could be in the layer thickness – the distance of the dielectric from the signal layer to the reference plane. There is no harm in using sequential laminations as long as you understand the variations that could happen. If you pick the right material with less glass weave and more resin, you can have more predictability during press-out, which means better predictability in your impedance.

Try our free [Material Selector](#) in the Tools section on our website!

“

**Atar Mittal, General Manager at Sierra Circuits**

*Don't try to pick the materials that have been used for a long time because new materials are coming out that address any previous issues that the material may have had.*

*There is no necessity to go for very expensive materials because your application may not require it. There is a safety factor to take into account but not beyond a certain point. You have to be pragmatic about this.*

”

## Dielectric thickness of glass styles:

Dielectric thicknesses are dependent on prepreg glass styles and their press-out.

Glass Styles	Press Out Thicknesses vary from material to material		
	Nanya NP175	Isola 370HR	Nelco 4013
106	1.7	2	2
1080	2.8	3.1	3.1
2113	3.8	3.7	3.7
2216	4.1	4.9	4.8
7628	7.1	--	--

## 2.3 Have a plan for your PCB stack-up and microvia structure

The microvia structure affects the number of lamination cycles and therefore impacts the manufacturing process and cost.

- The best practice for a balanced structure is to have an even number of plane and signal layers.
- Know the process steps associated with the stack-up so you can control cost and yield.
- Should you use stacked or staggered microvias?

The total number of layers of your final HDI PCB is determined by BGA (or the highest pin count device), signals break-out, the number of signal layers, as well as the number of power and ground layers. The number of power and ground layers can be determined by taking into account the number of grounds, the number of different major voltages in the circuit, as well as signal integrity/controlled impedance requirements.

The sequence in which the layers are put together (signal, power, ground, etc.) is another factor that affects signal performance and allows for a balanced PCB structure. It is always good practice to order the layers in a balanced manner.

You should have the number of plane and signal layers both odd or both even (both even is the best for a balanced structure). They should also be symmetrically placed.

Manufacturability of HDI design primarily has to do with via structures.

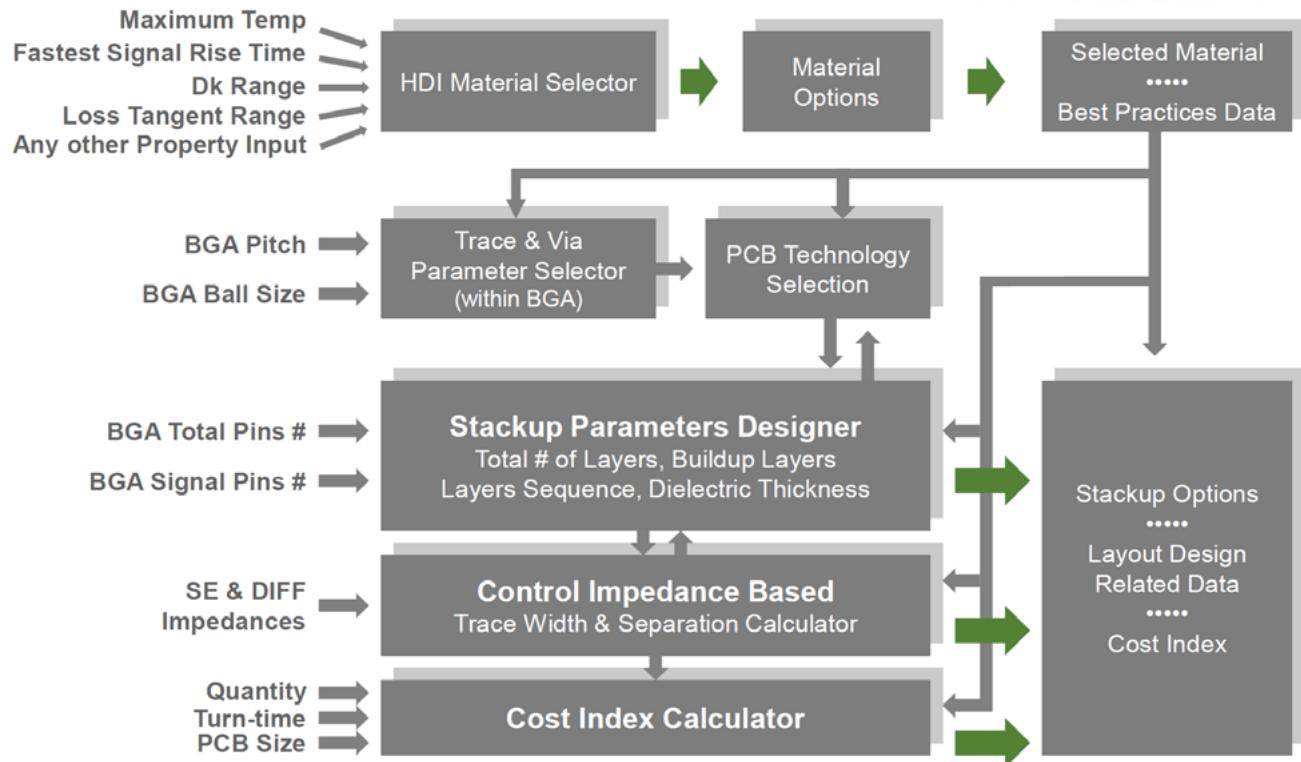
Microvia structures can have a big impact on the manufacturing process since they directly affect the number of lamination cycles. The more variations you have of layers where microvias start and stop at, the more number of sequential laminations are needed for the PCB manufacturing. Any layer on which a microvia starts or stops at requires a sub-construction, and each sub-construction will require an extra lamination cycle. (The lamination process is defined as pressing a set of copper layers with uncured dielectrics in between two adjacent copper layers under heat and pressure to form a multilayer PCB laminate).

### TIP:

Answer the following questions before you start working on your next project: Are you meeting the design guidelines for microvia aspect ratio? Are you stacking or staggering your microvias?

# 2

## HDI stack-up planning block diagram:



*Our HDI Stackup Planner tool was designed with this in mind.*

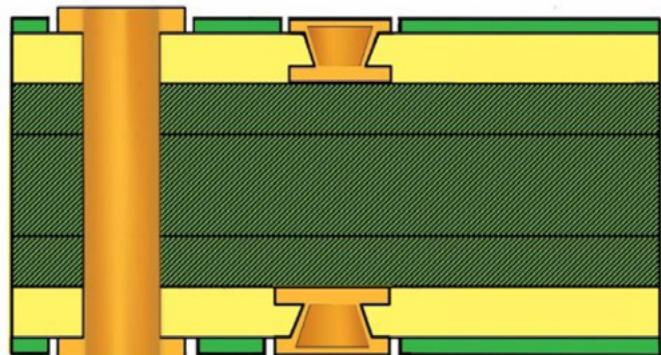
### Stack-up architecture:

In conventional multilayer boards, your design choices depend on the number of signal layers you require. HDI offers a larger variety of design choices. Choose from blind and buried, sequential build-up, or stacked and staggered, as well as many other design choices. Of course, HDI does not require complex architectures. One of the most common mistakes designers make is creating architectures that are unnecessarily complex.

### 2.3.1 HDI stack-up classes

There are different stack-up classes for HDI boards. The first option is a single lamination built using laser drills. This stack-up class is a no-brainer in terms of utilizing microvias in the least expensive way possible: Using only one lamination. When you use a laser drill, you benefit from a smaller pad and via size. This can help ease some of the design restrictions and reduce your design time.

#### 0-N-0 STACK-UP

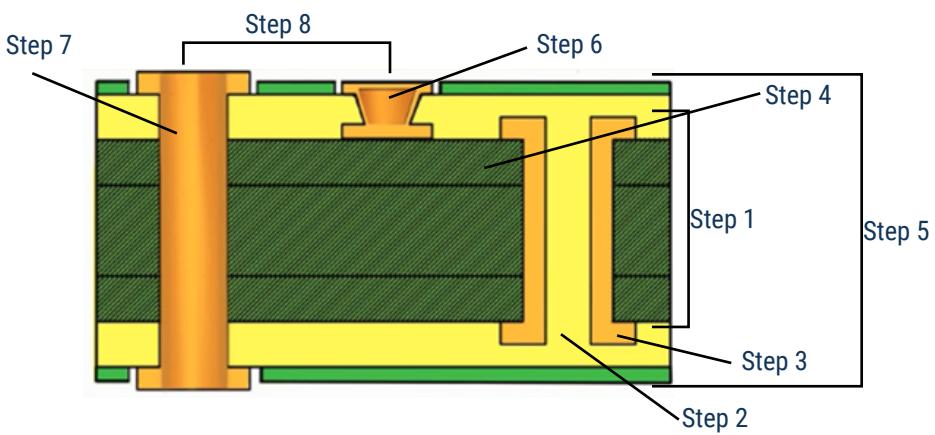


Going over the possible structures, it is important to know the process steps associated with the stack-up. Additional process steps mean more cost and more yield loss.

N represents the number of layers in the first or base lamination (or core lamination) and 0 tells that there is no sequential lamination steps and no extra dielectric and copper layers are added.

In this 1-N-1 type of stack-up, the '1' represents one sequential lamination on either side of the core. One sequential lamination adds two copper layers for a total of N+2 layers. This stack-up does not feature stacked vias. There is one extra lamination and no stacking of the vias. The buried via has been mechanically-drilled. There is no need to use a conductive fill for the via. It will naturally fill with the dielectric material. The second lamination adds the top and bottom layers. Then, we finish up with a final mechanical drill. The pcb manufacturer plans the right amount of prepreg between layer one and two so the resin flows into the buried via.

## 1-N-1 WITH LASER MICROVIAS AND MECHANICAL BURIED CORE VIA

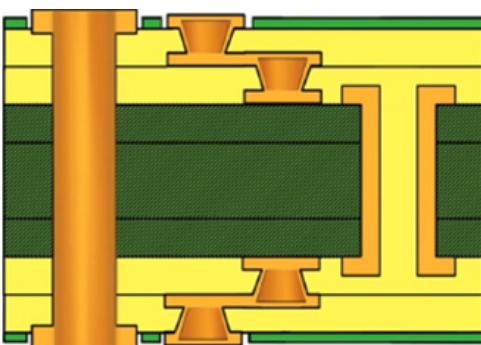


### TIP:

Consider whether you need a final mechanical drill. You can get the same connections with the laser drill and the buried mechanical. This saves an extra drill cycle and saves the manufacturer from dealing with the registration of the mechanical drill and the laser drill.

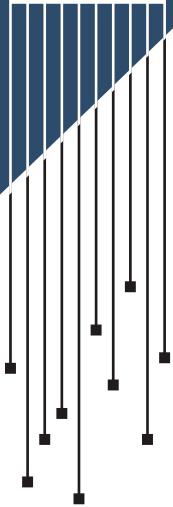
Building this next stack-up takes an additional two laminations for a total of three laminations:

## 2-N-2 WITH STAGGERED MICROVIAS AND BURIED CORE VIA



# 2

The manufacturing steps are as follows:



## 1-N-1

1. The core is laminated. (The core can be only two layers, so no lamination.)
2. The core is mechanically drilled.
3. The laser drilled vias are formed.
4. The mechanical drill is plated.
5. Layer two is imaged/etched.
6. The sequential lamination adds two additional layers.
7. (The mechanical drill is now a buried via.)
8. The laser drilled vias are formed.
9. The final through-hole via is formed.
10. The laser drill and the through-holes are plated.

## 2-N-2

1. The core is laminated. (The core can be only two layers, so no lamination.)
2. The core is mechanically drilled.
3. The laser drilled vias are formed.
4. The mechanical drill is plated.
5. Layer two is imaged/etched.
6. The sequential lamination adds two additional layers. (The mechanical drill is now a buried via.)
7. The laser drilled vias are formed.
8. Lamination of another 2 layers.
9. Laser drill.
10. Plating the laser drill.
11. Image and etch.
12. Back to lamination.

The manufacturer will be going back to the laser drill and plating process twice for the laser drills, once for the buried mechanical drill, and then a second time for the through-hole mechanical drills. Each lamination cycle can be done in one day. So with three laminations, this can only be done in three days. Plus an additional day for outer layer processing. Four days in total.

Here are some additional types of stack-ups:

- 0-N-0 with laser microvias

In this stack-up, the manufacturing steps are as follows:

1. The core is laminated.
2. The core is mechanically drilled.
3. The laser drilled vias are formed.

- 1-N-1 with microvia stacked on top of buried and filled core via

This stack-up is similar to the one above, except in this case there are also laser microvias stacked on top of buried core vias. This requires that the buried core vias should be filled and plated before adding the additional two layers. And the microvias need to be plated with copper and planarized flat.

- 2-N-2 with stacked microvias and buried core via

In a 2-N-2 stack-up, the '2' represents two sequential laminations.

As stated above, one sequential lamination adds two copper layers, so two sequential laminations add four copper layers for a total of N+4 layers. Again, there are no stacked vias.

A more complicated structure is called a 3-N-3. At this point, material selection becomes critical. Is your material robust enough to handle four lamination cycles, plus a reflow cycle in assembly, plus a possible rework that you might have afterwards?

Let's now talk about the cost.

SINGLE LAMINATION	
2 SUB CONSTRUCTION LAMINATIONS	
STAGGERED VIAS SEQUENTIAL LAMINATION UP TO 3 BUILD-UP LAYERS	
STACKED VIAS SEQUENTIAL LAMINATION UP TO 3 BUILD-UP LAYERS	

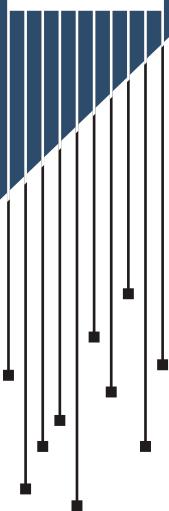
On the left of this chart, you have HDI stack-up classes, and on the right, you have the associated cost. The more sequential laminations, the higher the cost. The most expensive stack-up class is three sequential laminations. This includes microvias stacked on top of each other, which is necessary when you are breaking out of a tight pitch BGA, like .3 mm. Second in the stack-up class in terms of cost are using a non-conductive hole through process.

#### Getting design help from the PCB manufacturer: Too much of a good thing?

Leaning on your PCB fabricator too much has its pros and cons.

Most PCB fabricators have fleshed out their engineering support to be able to provide basic feedback on your HDI PCB layout. This is great information, but only up to a certain level. A PCB fabricator will seldom take into account your decision-making criteria when looking at your circuit schematics or BOM. If you want a strict review of your layout, there is no need to waste your time waiting for a response from the PCB fabricator's engineer. There are on-line web tools available that will provide this service quickly and with great detail. (Freedfm.com and BetterDFM.com)

# 2



When you are placing your vias, you need to know where they are going – what layer are they starting from and what layer are they stopping at? Knowing where your drilled holes are is the key to keeping your cost down. Think about the number of times the board has to go through mechanical and laser drill versus just going to laser drill. Most designers think they need mechanical drilling for the power of the pins of the BGA but this is not necessarily true. You do not want an HDI design where right at the center of the BGA there is a through-hole. A through-hole has to align with the laser drilled vias, which makes it harder to manufacture, you might have a lower yield, and you are just adding an extra through-hole process, which you probably did not need at first. The manufacturer has to align mechanical versus laser drilled holes.

“

**Rick Hartley, Principal Engineer at RHartley Enterprises:**

*When part of the power delivery system, they [vias] help create very low power bus impedance. Vias are one of the largest inductance features in power delivery, causing large  $Ldi/dt$  switching noise. HDI vias, especially when placed properly, have much lower inductance.*

*HDI vias create much less of the ‘Swiss Cheese’ effect in the planes, also helping to lower plane inductance. This also lowers switching noise in the power bus.*

*When placed on signal lines, they eliminate via stubs. Via stubs, at GHz frequencies, cause signal integrity issues.”*

”

## 2.3.2 Stacked vs staggered vias

Stacked vias essentially mean less process steps. The manufacturer does not have to fill the laser-drilled vias with copper because the second laser drill does not land on the first laser drill. Filling or plating a microvia shut usually happens in a special plating tank designed with chemistry that plates the laser-drilled microvia from the bottom of the via to the top of the via, until the hole is completely filled. Plating a laser-drilled microvia shut adds time and cost to the process and is only needed when you are stacking on an inner layer or if you have a via-in-pad on the outer layer. If the second laser-drilled via is staggered or offset, there is no need to copper plate shut. If you are staggering your laser-drilled microvias, it is important to know what spacing your manufacturer requires between the laser drills.

“

**Randy Clemons, PCB Designer CID+ at San Diego PCB:**

*A board with staggered vias is more difficult and time consuming to design. It is easier and faster to design a board using stacked vias. Good CAD tools have hot spot snap features, which simplify precise positioning stacked vias during the design process.*

”

# STAGGERED VS. STACKED MICROVIAS

## STAGGERED

- NO COPPER FILL REQUIRED
- NO EXTRA IMAGING STEP

## STACKED

- HOLE FILL REQUIRED
- PLANARIZATION REQUIRED
- EXTRA IMAGING STEP

What is the laser drill accuracy? It is very safe to assume it is +/- 1 mil accuracy. Usually, in a staggered microvia formation, the diameters of both operate and lower microvias are the same. The key parameter that decides whether the staggering is possible or not, without the lower microvia needing to be filled, is the dimension E, the vertical separation between the central access of the two microvias. For staggering to be viable, the value of E must be greater than the microvia diameter.

Sometimes, the space restrictions are so tight that your only option is a stacked via. Here are some precautions for stacked vias: Stacking on a buried mechanical drill is known to be a bad structure where failure can occur. We have seen cracks at this connection. We have not seen cracks on stacked laser-drilled microvias.

The final point is: If you have a buried via, it is better to offset your laser drills from the buried mechanical drills and then stack from that point onwards. This gives you the most reliable connection.

“

**Randy Clemons, PCB Designer CID+ at San Diego**

**PCB:**

*When choosing between staggered and stacked vias, there are fabrication processes and design costs, as well as reliability and signal integrity issues to consider. If the board is a low volume test board, like an IC test board which will be used to test millions of ICs, then signal integrity and reliability will be a priority. If the board is a consumable commercial product, then lower fabrication cost will be given a higher priority than design cost.*

”

# 3

## 2.4 Key considerations in your HDI PCB design strategy – a checklist

Via diameter, pad diameter, trace width and space, and aspect ratio.

- Think about the assembly process when deciding your BGA pad size.
- The trace width and via sizes will determine an optimum number of signal layers.
- Have your aspect ratios right for the plating process.

Take into account a complete view of the design before deciding the via and pad sizes you are implementing, so you don't paint yourself into a corner. The primary consideration at this point in the planning stage is routing density. Routing density is determined by the high-pin count fine pitch device on the board, for example, a BGA. BGA pin count and BGA pitch are both important parameters that affect routing density.

When you are deciding your BGA pad size, do take into account the assembly process and the PCB design rules that you are following. For example, pad to pad spacing and soldermask web are two critical design parameters. If you are choosing a via-in-pad approach, your BGA pad size needs to account for the size of the laser and mechanically drilled microvias while keeping the correct pad size required by the BGA assembly process.

The BGA pad size and the microvia size should be determined along with the trace width and spacing. Depending on the pitch of your BGA (say for example, 0.8 mm), the trace width and the via sizes will determine an optimum number of signal layers. At Sierra Circuits, we have created an HDI Design Planning Tool (with requisite algorithms) that assists our engineering staff in specifying an optimum via size, pad size, and trace width depending upon the desired number of signal layers.

You can see what an important role via sizes, pad sizes, and trace width and space play in the overall stack-up structure.

When you design an HDI board, make sure that you have your aspect ratios right for the plating process. To achieve acceptable copper plating, the plating solutions have to properly fill the hole. If the hole sizes are too small compared with the thickness of the PCB, you might get unsatisfactory plating.

# 3. Signal Integrity for HDI

“ Eric Bogatin, Signal Integrity Evangelist at Teledyne Lecroy:

In HDI boards, signal integrity issues are just as important to deal with as in traditional through-hole boards.”

By reducing the size and offering the opportunity for smaller current loops on critical nets, HDI improves signal integrity. HDI can indeed provide improvements and alternatives to issues like noise, crosstalk, and electro-magnetic interference (EMI). Because they are smaller, shorter, and have almost ten times less electrical parasitics than through-holes, microvias offer a decreased inductance and capacitance, which results in helping reduce switching and circuit noise, signal reflections, and crosstalk.

Carefully select your materials for HDI as they have an impact on the signal integrity performance.

In a paper entitled HDI's Beneficial Influence On High-Frequency Signal Integrity, Happy Holden explained that due to the physical structure of microvias, there is a reduction in switching noise. This is attributable to the decreased inductance and capacitance of the via as its physical size becomes smaller and shorter. A microvia will have nearly one-tenth the electrical parasitics of a through-hole. Another advantage of using microvia technology for creating interconnects is a reduction in signal reflections and crosstalk between traces. The corresponding increase in routability area also allows designers to place traces further apart to reduce crosstalk.

Four categories of noise describe the various effects:

1. **Signal quality** of one net and its return path (ringing due to reflections)
2. **Crosstalk** between two or more nets (noise pulses due to switching on neighboring lines)
3. **Switching noise** (noise on power and ground lines/planes)
4. **EMI**

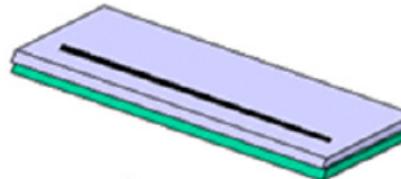
HDI Features	Signal Quality	Cross Talk	Switching Noise	EMI
Short interconnect lengths	x	x		
Low dielectric constant	x	x		
Small vias and small features	x		x	
Vias in pads			x	
Fine lines and thin dielectric		x	x	x
Support for fine-pitch components			x	x

# 3

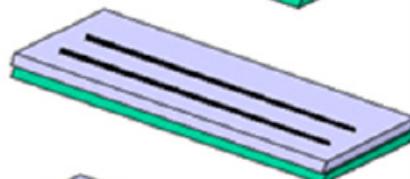
Each of the four categories named above has specific causes. By identifying the cause in each family of problems, design- and technology-based solutions can be identified and implemented.



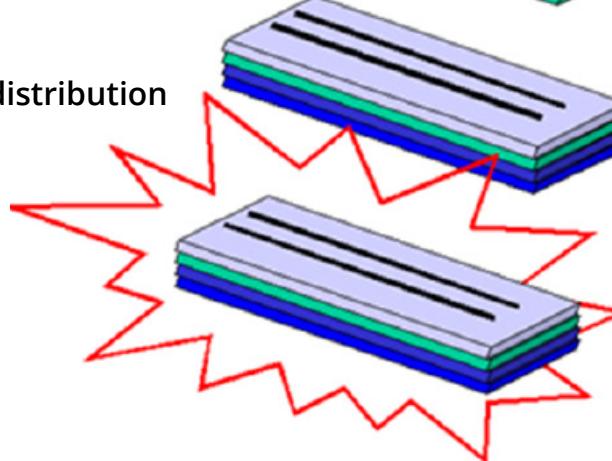
Signal quality of one net: reflections and distortions from impedance discontinuities in the signal or return path



Cross talk between multiple nets: with ideal return paths, and without (SSO)



Rail collapse in the power and ground distribution network



EMI from a component or the system

Noise can come from many sources in the board layout, such as:

- Changes in trace width
- Plane splits
- Cutouts in Power/Ground planes
- Via antipads
- Insufficient plane capabilities
- Excessive stubs, branched or bifurcated traces
- Component lead frames
- Improper impedance matching and termination networks
- Coupling between signals
- Varying loads and logic families

## 3.1 Signal quality of one net

A smaller substrate and improved signal integrity.

- 
- Shorter interconnect lengths, smaller vias, and thinner dielectrics of lower dielectric constant materials improve signal integrity.
  - The signal return path is just as important as the signal path.

HDI is a fabrication technology of miniaturization that has two main benefits: A smaller substrate and improved signal integrity. The smaller substrate is due to the shorter interconnect length, smaller vias, and thinner dielectrics of lower dielectric constant materials. These things also improve the signal integrity.

With HDI, devices can be brought so close together (both from a surface point of view and using the secondary or backside of the interconnect) that the signal may not need to use transmission lines. Interconnects with a time delay shorter than about 20 percent of the rise time of the signal may not need to use transmission lines. The interconnect length is given by:

$$\text{LENGTH} < 20\% \text{ of } (\text{rt} \times C) / Dk^{0.5}$$

Where:

rt = signal rise time in nsec

c = the speed of light in air~11.8 inches per nsec

Dk = dielectric constant of the material

The signal return path is just as important as the signal path, and exists whether you provided for it or not. The signal return path contributes to the inductance, capacitance, and resistance experienced by the signal. The signal return current will seek the path of minimum energy, which has the least impedance. For low frequencies, this path will have the least resistance; for high frequencies, the path will minimize the current loop. At higher frequencies, inductance dominates over resistance, so the return path follows the signal path even though it meets higher resistance.

The low dielectric constant results from the use of many new HDI materials. Many of these materials are not glass-reinforced and thus have lower dielectric constants than glass-reinforced laminates. Many of the dielectrics are liquid such as the high-Tg epoxy or polyimide, or the photodielectric resins (PDR). Some materials are thin, vacuum-laminated dielectrics with high thermo-plastics contents. However, all materials are uniformly thin — this contributes to reductions in wiring delays and reduction in noise. Several of these new materials and their electrical characteristics are shown in the table below.

# 3

Typical HDI Materials	Dielectric Constant	Dissipation Factor
ISOLA 370HR	3.92	0.015 - 0.025
Isola I-speed	3.63	0.0071
Isola I-Tera MT40	3.45	0.0031
Nelco N4800-20	3.76	0.0075
Nelco - 4000-13 (low Dk & loss)	3.9 - 3.7	0.009
NanYa CCL FR-4 NP170	4.3	0.01 - .016
Rogers R040003 (low Dk & loss)	3.4	0.0027
Rogers R04350 (low Dk & loss)	3.5	0.004

## 3.2 Crosstalk noise

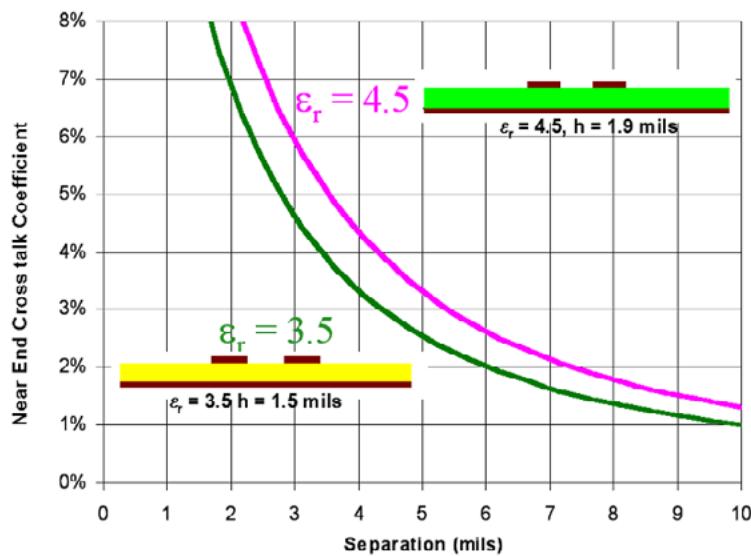
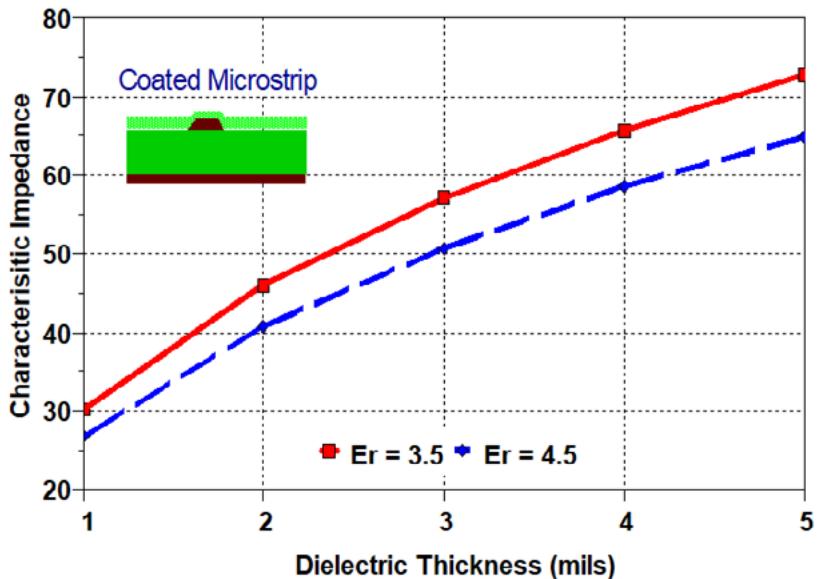
Crosstalk in HDI substrates is reduced by the shorter coupled lengths and by the lower dielectric constant by as much as 50 percent.

- Reduce crosstalk in HDI substrates by using lower Dk materials.
- The lower dielectric constant of the HDI material system may allow a board to shrink up to 28 percent.
- The thinner the distance to the reference plane, the lower the near-end cross-talk will be.

HDI miniaturization provides shorter interconnect lengths, and if the lower dielectric constant material is used, then crosstalk in HDI substrates is reduced. Eric Bogatin provides the following example: "A typical line-width in HDI technology is 3 mils (75 microns). The figure below shows the characteristic impedances of 3-mil-wide traces for various dielectric thicknesses."

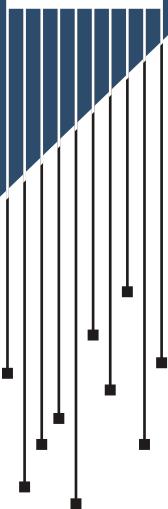
The dielectric thickness will be less for a lower dielectric constant. This means a lower dielectric constant material system will either result in less crosstalk for the same spacing, or the traces can be moved closer together and have the same amount of cross-talk."

Bogatin continues, "The variation in the near-end crosstalk coefficient with separation for two 50-ohm microstrip traces is shown [below]."



"In the two cases studied, the line-width was 3 mils, and the dielectric thickness was adjusted so that for the two different dielectric constants, the line impedance was the same. From these curves, it can be seen that if the routing pitch is crosstalk constrained, just the lower dielectric constant of the HDI material system may allow a board to shrink up to 28 percent.

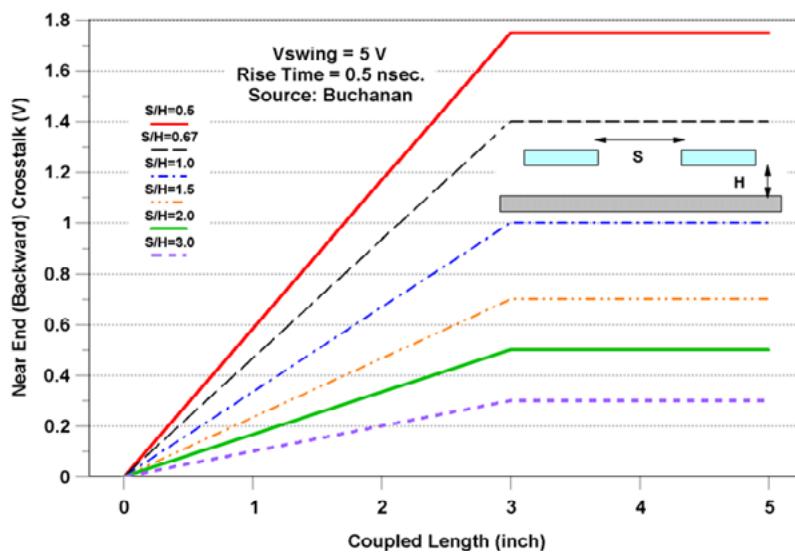
# 3



For coupled lengths less than the saturation length, the magnitude of the near-end voltage noise will scale with length. The saturation length will depend on the rise time. For a rise time of 1 nanosecond, the saturation length with an effective dielectric constant of 2.5 is about 7.6 inches, which would include many of the traces in a small card application. The relative coupled near-end noise would be given by:

$$\frac{V_{noise}}{V_{signal}} = \frac{\text{len coupled}}{\text{len sat}} K_b = \frac{\text{len coupled} \sqrt{\epsilon_r}}{\tau 12 \text{ in/nsec}} K_b$$

Crosstalk in HDI substrates is reduced by the shorter coupled lengths and by the lower dielectric constant by as much as 50 percent. Shorter trace lengths will radiate less, and traces with thinner dielectric will radiate less. The example below shows that the shorter the coupled length, the less the mutual inductance ( $L_m$ ), and the thinner the traces, the less the mutual capacitance ( $C_m$ ).



Moreover, the thinner the distance to the reference plane, the lower the near-end crosstalk will be, or the same crosstalk for a longer coupled length. With length reductions of 2x and dielectric thickness reductions of 2x over conventional boards, the radiated field from HDI signal loops might be reduced by as much as 4x, which is 12 dB.

“

### **Eric Bogatin, Signal Integrity Evangelist at Teledyne Lecroy:**

If the entire board is HDI, rather than just a few outer layer, controlling the return path can be a bigger challenge than in through-hole boards.

You have to pay attention to the same issues in HDI substrates:

1. Providing a continuous return path
2. Engineering controlled impedance interconnects
3. Routing in a linear, daisy chain path with minimal stub lengths
4. Managing reflection noise with terminations
5. Controlling via to via crosstalk by return path control
6. Using low inductance capacitors connected to the IC pins

In conjunction with a through-hole core, HDI interconnects can be incredibly valuable. ”

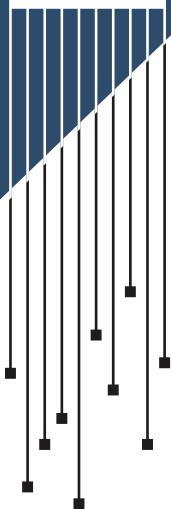
## 3.3 The constraints of controlled impedance

Know where to put your impedances.

- Make sure your manufacturer knows how to control the tolerance of a 3.5 or 3-mil trace.
- Use the correct thicknesses for the dielectrics between the signal layers and the reference planes.

Controlled impedance for HDI has some additional issues. HDI has thinner dielectrics than traditional boards, so if you are looking for a traditional 50-ohm single-ended or 100-ohm differential pair, the thinner dielectrics will require less wide traces. That is why it is possible to have a higher density of interconnections in an HDI board. You can design with 5-mil trace and space, but it is a lot better if you are using 3.5-mil trace and space, as that matches the 3 or 4-mil dielectrics on the build-up. As such, it is important that the fabricator knows how to control the tolerance of a 3.5 or 3-mil trace, in order to meet that characteristic impedance.

# 4



In order to get a higher impedance, you must have:

- Thinner traces
- Thicker dielectrics
- Less copper
- Lower dielectric constant ( $D_k$ )
- More space in between differential pairs

In order to get a lower impedance, you must have:

- Thicker traces
- Less dielectrics
- More copper
- Higher dielectric constant ( $D_k$ )
- Less space in between differential pairs

When you are trying to design appropriated trace widths for controlled impedance lines, it is important that you use the correct thicknesses for the dielectrics between the signal layers and the reference planes. The dielectric thickness to be taken is what is called the press-out thickness.

Another challenge in HDI technology is that you have to use the correct thickness of the copper layers in the built-up layers resulting from sequential lamination. Pay attention or things could go wrong.

The base thickness of the material is found on the material data sheets or is available from the laminate manufacturers. PCB manufacturers calculate the final press-out thicknesses that they expect from the prepreg, which depends on the amount of resin in the prepreg, the amount of the copper area percentage, and the thickness of the adjoining copper layers. PCB manufacturers calculate the copper area percentage from the CAD files that you sent. Therefore, they do not follow the generic thickness specified on the data sheets, they use the calculated press-out thicknesses for impedance modeling, which will change from design to design. This will require small adjustments in the trace widths and spacing of the controlled impedance traces. If they cannot meet the impedance requirement that you are looking for with the dielectric thicknesses or material types you have selected, they will suggest an alternative dielectric thickness or PCB material.

“ Randy Clemons, PCB Designer CID+ at San Diego PCB:

Maintaining a controlled impedance path from the signal source to the load destination is easier using stacked vias. Staggered vias create additional discontinuities and therefore may be less desirable to use in ultra high-speed designs, like 10 Gbit or higher.

”

# 4. Manufacturing for HDI

---

## 4.1 Layer and laminations

Think smart and reduce your cost.

- Have you planned your layer sequencing for reduced EMI?
- What is the total number of sequential laminations?
- And have you minimized your laminations?

When you are designing an HDI circuit board, there are many things to consider. The first thing you need to consider regarding the manufacturing process is the cost. What will make your HDI Board more expensive by accident? You want to avoid inadvertently increasing the cost of your HDI design by using a set of rules that are the easiest to manufacture. The first thing to understand is the number of laminations that your design requires because it will add to your cycle time and therefore cost. Understand how many sequential laminations you are designing for and then optimize. Try to get the least as possible.

In a traditional through-hole design, a lot of designers surround their signal layers with power and ground planes, but then they end up with a lot of layers. In HDI, this is a bad practice. Use mixed planes instead if there are signals that you need to protect with power and ground planes. In this manner, you are also shortening your signal path which inherently increases signal integrity and reduces crosstalk.

# 4

## 4.2 Mechanical vs laser drill

Drilling is the huge cost driver.

- The use of laser-drilled vias will decrease cost and cycle time.
- Define your laser drill size in proportion to the finished press-out thickness.

It is important to know what the pros and cons of mechanical versus laser drilling are. Let's start with the mechanical drilling. This chart shows the reasons why:

### DRILLING COST DRIVERS

- HOLE SIZE
- DRILL COST
- STACK HEIGHT
- FEED and SPEED
- PECKING
- EQUIPMENT SPEED REQUIRED
- YIELDS
- NUMBER OF DRILL FILES

SIZE	COST INDEX
4 MIL	7.0
6 MIL	3.5
8 MIL	2.5
10 MIL	1.2
12 MIL	1

To name a few, there is the cost of the drill bit, the time it takes to drill mechanical holes, and the quality of the drill. On the right side is the cost index. A 6-mil drill is much more expensive when compared to a 10-mil drill. What can make this process even more complex is the use of hybrid materials. For hybrid materials, each material requires a different drill cycle and plasma cycle. Bottom line, if you have the opportunity to reduce or eliminate mechanically-drilled vias and use laser-drilled microvias instead, you could save a tremendous direct cost for yield.

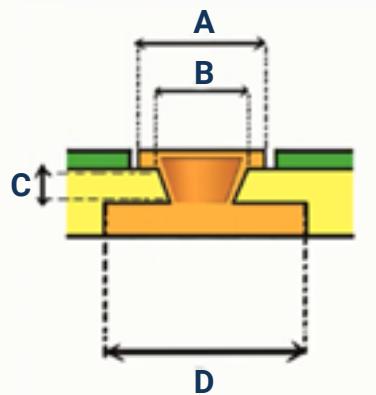
Strangely enough, designers typically seem to want to add more vias to protect their critical traces. However, to decrease cost and cycle time, instead of through-hole vias, use laser-drilled vias in your modeling. Laser-drilled vias do not add much cost. One laser drill costs the same as 10,000 laser drills.

#### 4.2.1 Laser drilled microvias

Here is the basic make-up of a laser-drilled microvia. The critical dimensions are the pad size, the laser drill size, and the press-out thickness of the dielectric. You must define your laser drill size in proportion to the finished press-out thickness in order to properly plate the via. Laser drill dimensions can get very small. But remember, they are only going from one layer to the next. Many fabricators can laser a 2-mil hole but plating the 2-mil hole becomes problematic because of the aspect ratio of the thickness due to the drill diameter of the hole.

### LASER-DRILLED MICROVIAS

A = LASER DRILL CAPTURE PAD (TOP PAD)  
B = DRILL DIAMETER OF LASER MICROVIA  
C = THICKNESS OF DIELECTRIC LAYER  
D = LASER DRILL TARGET PAD (BOTTOM PAD)



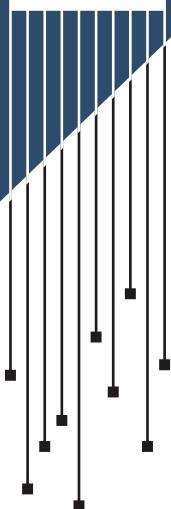
#### 4.3 Hole fill process

Conductive or non-conductive hole fill process?

- A hole fill is to help assembly form a good solder joint.

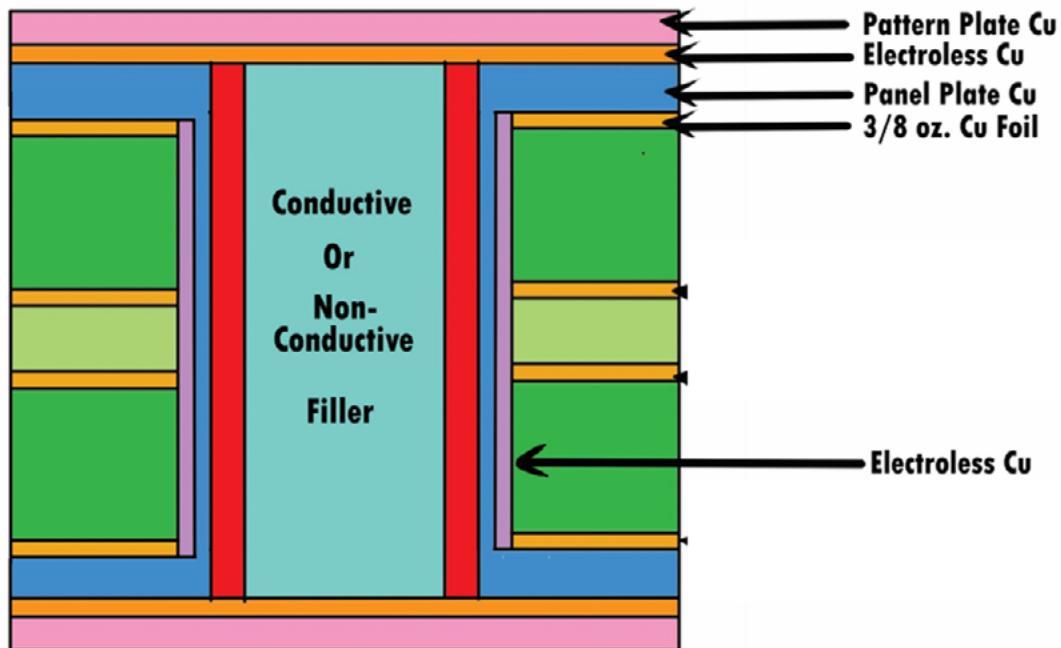
The next cost factor to consider is choosing between a conductive or non-conductive hole fill process. Do you have vias underneath a surface-mount component that is required to be filled and capped or plated over? It is costly because it requires two plating steps and two drill steps. We drill holes that will be filled separately from the regular through-holes on the board and any extra steps mean extra cost. In this case, the manufacturer is going back to the process twice, which costs in terms of time and dollars, drilling and plating.

4



The final objective of a hole fill is to help assembly form a good solder joint. And it works great for that. Just be aware of the added cost and time when it comes with this. If you have a choice between offset laser-drilled microvias and via-in-pads, I would choose the laser-drilled microvias over the mechanical drill.

Sierra Circuits can plate the laser drills and the through-hole mechanical drills at the same time. And not only is via-in-pad design another step in the process, it also challenges the manufacture registration system. If the via-in-pad is implemented with the through-hole mechanical drill instead of a laser drill, there is an extra step with a non-conductive fill process. Using a non-conductive fill is more expensive than plating the laser-drilled via shut.

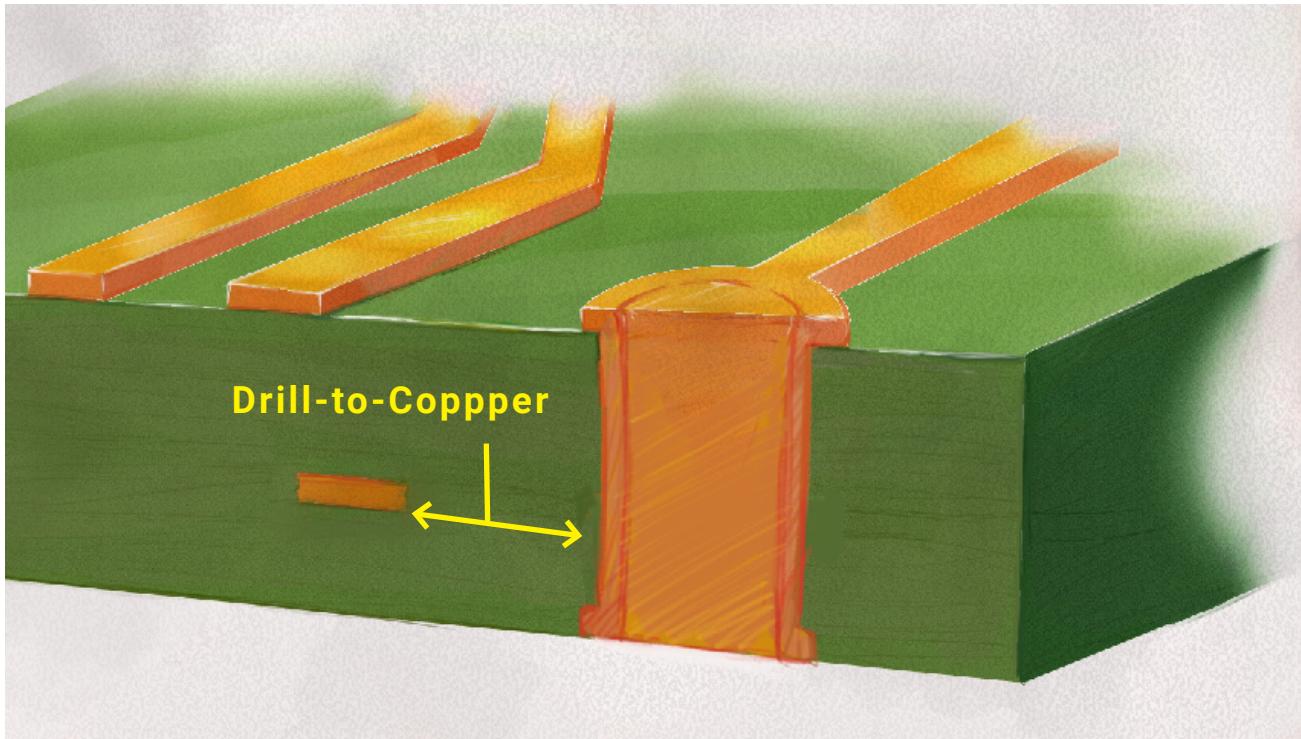


## 4.4 Drill-to-copper

Drill-to-copper only matters on inner layers. Drill to copper is the distance between the edge of your drilled hole and the next copper feature on your inner layers.

The software design tools do not check for drill-to-copper. If you provide enough annular ring, it does not mean that you cannot have any drill-to-copper issues. PCB materials move: When you laminate a core might shift one way and another core might shift another way. If this happens, it might hit the copper. Another possibility is that copper grows over time inside the circuit board along the glass weave of the dielectric – it is called CAF, which stands for conductive anodic filaments. The copper might grow enough to touch the hole and cause the board to be unreliable. CAF does not usually happen with laser drilling but it does with mechanical drilling.

If you use mechanical drills along with your laser drills, the first thing your manufacturer should check for is the registration of the mechanical drills to the laser drills, which means more spacing is needed for drill-to-copper. If you do not use mechanical drills, the yield will be higher. With laser drills, drill-to-copper is not a problem because the manufacturer can easily laser drilled vias more accurately than mechanically drilled vias.



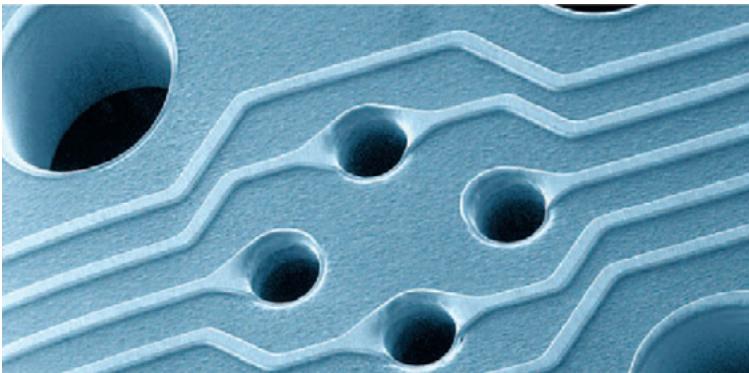
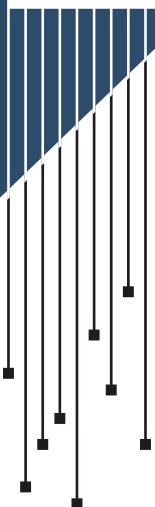
## 4.5 Landless via technology

Laser drilling makes it possible to have no pad at all!

- More space to route your traces.
- Landless via technology helps on noise reduction and signal integrity.

# 4

HDI is all about shrinking the design and pad sizes, which take a lot of space. The reason why designers tend to put big pads is because they want big annular rings to avoid breakouts. If you are allowed to breakout, you can minimize your annular ring and therefore have more space to route your traces. Laser drilling can reduce the annular ring because it is very accurate whether mechanical drilling might be a little off due to less control. In fact, it is even possible to not have any pad at all for laser drilling – this is what is called a landless via technology.



## Happy Holden's experience:

"Landless vias are a little known secret of some of the world's largest OEMs like IBM, Hewlett-Packard, NEC and Fujitsu.

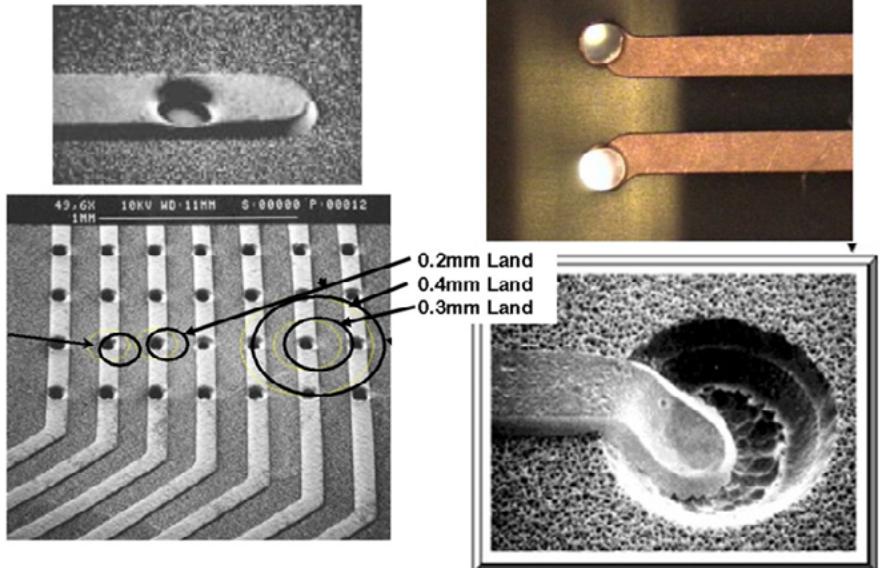
1. We used it a lot at Hewlett-Packard after learning it from our Japanese partner and testing the reliability. We found it to be at least 10 times more reliable than normal through-holes and 20 times more on high-aspect through-holes. So it is MUCH more reliable than normal through-holes and the same as landed microvias. But we are talking about surface vias (blind) not buried vias. This is shown in the PC Handbook, 7th ED pp-1307-Chapter on Via Reliability.

2. It provides for a much higher routing density on HDI boards 2X-4X, especially for bus routing where the vias can be 'invisible' (that is, the via is the same diameter as the trace width – either 100 microns, 75 microns or 50 microns).

3. It has nearly 1/10 the inductance of a through-hole, which helps on noise reduction and signal integrity.

4. To fabricate landless vias, no new processes or equipment are required, just changes to the artwork in tooling."

## Landless Is Now Practical!



## 4.6 Surface finishes

Choosing the right surface finish is critical in HDI.

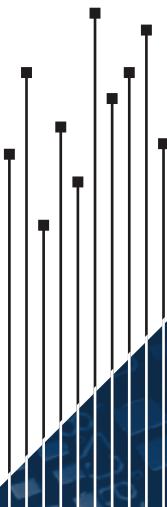
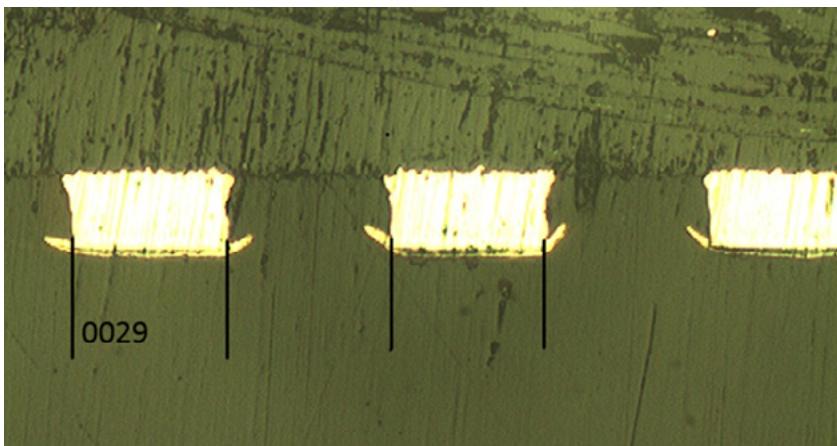
- When it comes to HDI, you should go with ENIG or ENEPIG.
- Get the typical thicknesses for immersion and soft gold.

Soft gold is used a lot for wire bonding – ENEPIG can also be a process for wire bonding. Make sure that you can get non-contaminated surface finishes. In a HDI board where the traces might be smaller, there is no reason to use HASL, which is very rough and not smooth enough to put on BGAs. HASL is a very aggressive process which weakens the strength of the copper. When a trace and space gets very tight, it is better to use ENIG or ENEPIG rather than a hard or soft gold which is electrolytic. You need to use an electrolytic-less gold. Do not use HAL because it is choppy. When you put the component down, it is not flat but tilting. So you cannot get a good connection. Do not ask for more gold than what is needed. When you put more gold, you have more yield loss on a PCB.

Standard thicknesses for surface finishes:

For immersion gold, the typical thickness is 0.05 - 0.23  $\mu\text{m}$  (2 - 9  $\mu\text{in}$ ) gold over 2.5 - 5.0  $\mu\text{m}$  (100 - 200  $\mu\text{in}$ ) electro-less nickel. This is not good for gold wire bonding and black pad.

For soft gold, the typical SMT thickness is 0.25 – 0.8  $\mu\text{m}$  (10 - 30  $\mu\text{in}$ ) gold over 2.5 – 8  $\mu\text{m}$  (100 - 300  $\mu\text{in}$ ) nickel. This is expensive but good for dual surface finish for fine pitch and wire bond surfaces, and overhang.



ENEPIG is considered a universal surface finish. It offers better shear strengths for SMT, high wire bond pull strengths for gold wire, and has a lower cost than soft gold.

# 4

## 4.7 BGA breakout and fanout strategy

BGAs have the highest density of I/O connections and array pins on a device, which is the most complex part of the layout.

- A good design practice is to do the layout part by part.
- Make sure that you will be able to fanout and connect all the pads under the BGA.
- Another good design practice is to draw short tracks.

BGA breakout means applying a fanout solution and routing traces from those fanouts to the perimeter of the device prior to general routing of the PCB.

Robert Feranec's fanout strategy:

"Be careful about drawing the connections all at once. It is a good design practice to do the layout part by part. If you have a BGA, the first goal is to go out of the BGA. Be sure that you can go out with all the pads and all the pins under the BGA. Do not fully route all the interfaces, but instead just route a little bit of track, and then stop routing to place vias, or draw the tracks for different parts just a little bit out of the BGA area. Make sure that you will be able to fanout and connect all the pads under the BGA. You can then start connecting all the interfaces.

If you only draw short tracks, it is very easy to delete them and redo parts of the layout under the BGA because you did not fully route the tracks. So you can just delete them and try to find a way to fanout all the pins. This practice is much easier and will save you a lot of time since you only have to deal with a small part of your layout. You want to avoid finding yourself in a difficult position once you have fully routed your BGA and you need to take out only one pin, for example. If that happened, you would have to deal with a lot of tracks just to be able to remove one signal.

There are some exceptions, like memories or high-speed interfaces. In this case, you can fully route the connections between the BGA and the memories or the high-speed interfaces before you finish the fanout of all the pads."

Watch [Robert Feranec's video on his YouTube channel! \(TIP #067\)](#)

## 4.7.1 Example of how to breakout a .4mm BGA

When planning out how to breakout (or route) a .4mm BGA, the overall size and the pin out of the part need to be thought through so the most cost efficient technology can be used. It is not just about the fact that the pads are .4mm apart and figuring out what are the numbers of widths and gaps that work.

When fanning out a .4mm BGA, the geometry does not work out so that you can route a trace between the pins. The traces and gaps are just too small to go down enough layers to get all the pins fanned out.

So with a .4mm BGA, blind and buried vias are required. The pins on the outside row in the BGA are routed on Layer 1, the pins on the next row in the BGA are routed on Layer 2 etc. The way the BGA is pinned out will determine how to route the BGA.

### Example of how to route a .4mm BGA:

This part is a standard .4mm BGA. The best way to fan it out is to use blind and buried vias and a multi-lamination fabrication.

Start off by adding a Layer 1 to Layer 2 blind via on all of the GND pins of the BGA. (This is a hole in the BGA pad that will tie that pin to the GND plane on Layer 2.) Now all of the GND pins are d routing described below.

### The routing plan:

Route the outside row or ring of pins (24 pins, row 1 and 7 and A and G) on the top side of the board, Layer 1. You may need to route out some of the GND pins on the outside row and not just add a 1 to 2 via in the BGA pad.

Add a Layer 1 to Layer 2 blind via to the next ring of pins (16 pins, row 2 and 6 and B and F), route this ring out on board Layer 2 – Layer 2 is a GND plane so these Layer 2 routes can only route out a short distance and then a standard top to bottom via is added. Do not cut off the GND plane with these short Layer 2 routes such that the GND plane is cut up and pins are not connected.

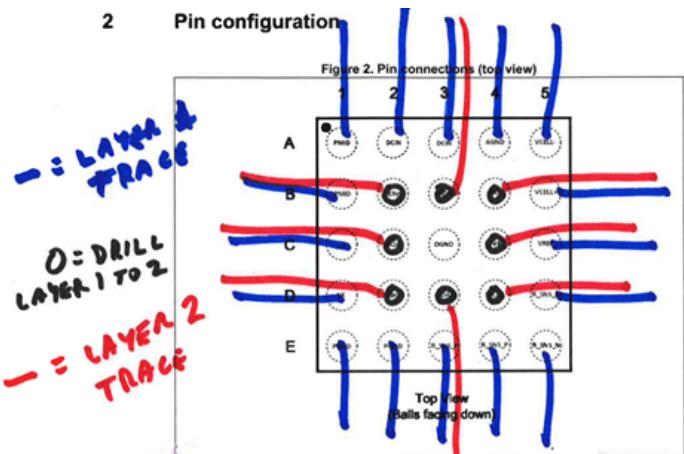


figure A

In this configuration above, the problem is what can you do with the GND pin? Drilling from Layer 2 to Layer 3 will cost more.

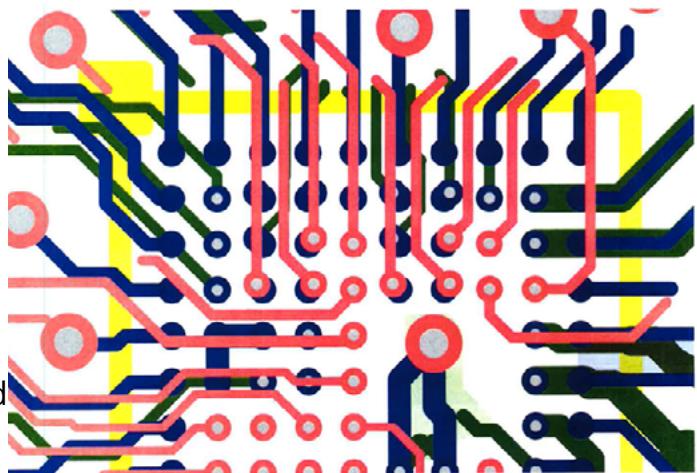
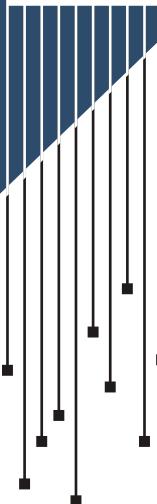


figure B

# 4

Then, on the next ring of pins (8 pins, row 3 and 5 and C and E), add a Layer 1 to Layer 2 blind via and a Layer 2 to Layer 3 buried via and route these nets out on board Layer 3.



The BGA pin in the very center of the chip will need to be worked out on Layer 2 or 3.

### Pad and drill sizes for .4mm BGA:

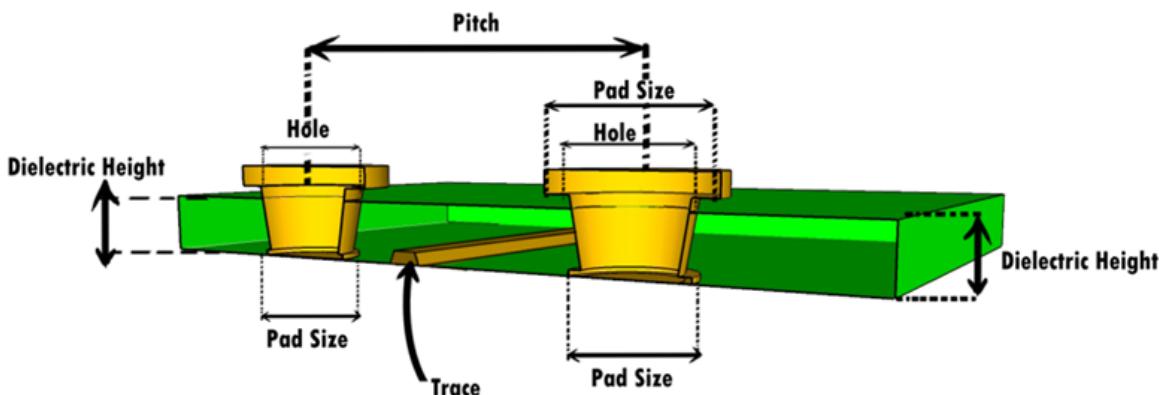
There will be no traces between pads on the top layer so the pads can be 10 mils and have a 5.7 gap between them. For the larger pad, let the manufacturer drill a 4 to 6-mil laser drill for the buried and blind vias. The distance between the board layers will determine the best drill size so they can plate the hole shut and make a flat pad for the BGA, etc.

### Sequential lamination:

Let's pretend that this is an 8-layer board.

Board Layers 2 through 7 will be laminated together. Then, a laser drill will be done from Layer 2 down to Layer 3: This is your 2 to 3 buried via. Note that a Layer 7 to 6 buried via could also be used, and a Layer 2 to 7 could be used; but the 2 to 7 needs to have bigger drill and pad.

<b>.4 mm Pitch</b>			
	<b>Drill Size</b>	<b>Pad Size</b>	<b>Trace</b>
<b>BGA Area MicroVia</b>	4 mil Drill	6.75 mil Pad	3 mils



Board Layers 1 and 8 will now be laminated to the board and a laser drill will be done from Layer 1 down to Layer 2 (Layer 10 to 9 if needed).

Then, the standard through via is drilled top to bottom – here again, bigger drill and pad are required.

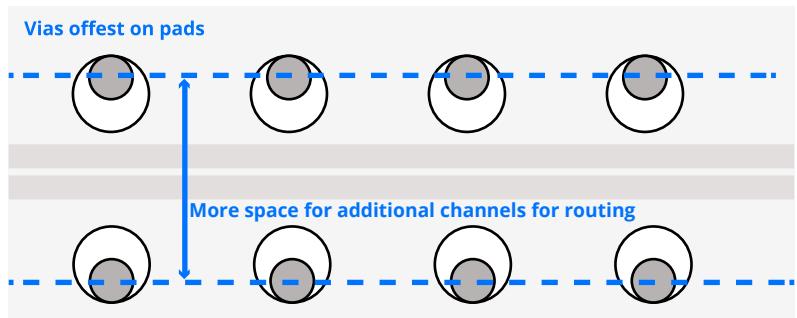
In your Gerber files, you have parts placed around the .4mm BGA. The fanning out and adding standard size vias and trace width and spacing will take up a lot of room around the BGA.

## Technology level for .4:

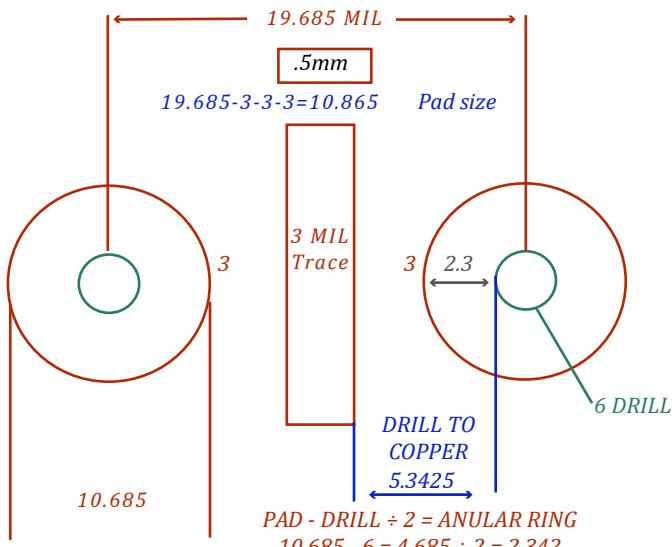
For BGA Pitch - 0.4	TECH I	TECH II
BGA area MicroVia Drill/Pad Dia in mils	6/12	4/6.75
BGA area BAse Core Via Drill/Pad Dia in mils	6/12	6/12
BGA Area Trace width and spacing Top Layer	5.00	5.00
BGA Area Trace width and spacing inner Buildup Layers	5.00	3.00
BGA Area Trace width and spacing inner Core Layers	5.00	5.00
BGA Area Trace width and spacing Bottom Layer	5.00	5.00
# of Traces bet BGA pads on : Top layer	0	0
# of Traces bet BGA vias on: Inner Buildup Layers	0	1
# of Traces bet BGA vias on : Inner Core Layers	0	0
# of Traces bet BGA vias on: Bottom Layer	0	0

**“ Ben Jordan, Director of Community Tools and Content at Altium:**

Laser drilled uVia-in-pads eliminate the need for via fill because they are small and very shallow compared to the pad. Offsetting the vias in row patterns will provide larger routing channels to allow inner pads to be easily escape-routed.

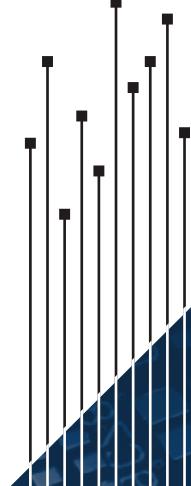


### 4.7.2 Example of how to breakout a .5mm BGA

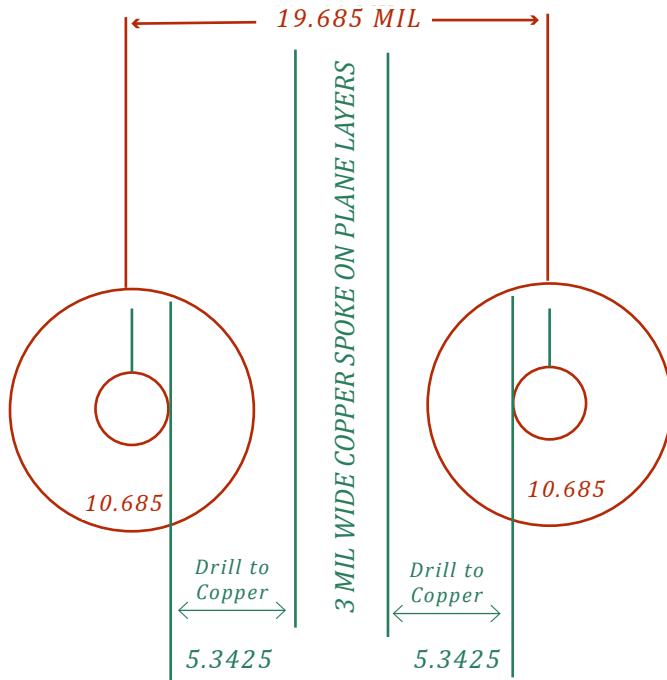
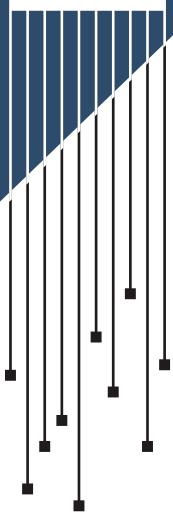


This example is from a board with pitch at .5mm (19.685 mils) and the minimum drill size is 6 mils. The minimum trace width needs to be 3 mils and the trace to pad spacing also needs to be 3 mils.

Take the BGA pitch minus the 3-mil trace minus the 3-mil trace to pad gap minus another 3-mil trace to pad gap and you have a pad diameter (or a pad size) of 10.685 mils.  
 $19.685 - 3 - 3 - 3 = 10.685$



# 4



Now take the pad size of 10.685 mils minus the 6-mil drill size divided by two and you have a 2.3425-mil annular ring on the pads.

$$10.685 - 6 / 2 = 2.3425$$

## On a plane layer:

If the via ties to the plane, it will be a solid tie (no thermal relief). If the via does not tie to the plane or to a signal trace on this layer, the pad on this layer can be removed. You can set up your design software to suppress unconnected pads and it will remove the pads on non-functional pins.

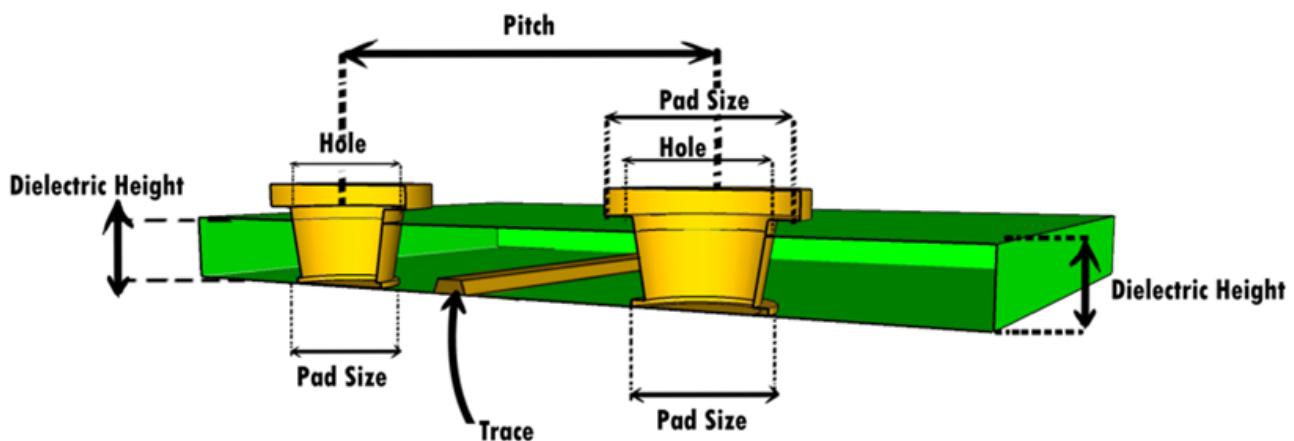
On a .5mm BGA, the copper spoke between the drills will be 3 mils wide. The distance from the edge of the drill to the edge of the 3-mil copper spoke between the drills is the drill-to-copper spacing. With the above sizes, the drill-to-copper will be 5.3425 mils. The drill-to-copper spacing required to manufacture the PCB changes due to many different factors. There is no set rule of thumb size for all boards.

This works if the board is 62 mils or less thick and does not have more than eight layers. The board thickness and the layer count have an increase in accumulative tolerances, which explains why fewer layers on a thinner board helps a lot.

Set up the footprint of the part with the via-in-pad- ie. a drill in the surface mount component pad of the BGA. The manufacturer might adjust the trace and space a little but can build the board with these numbers.

<b>.5 mm Pitch</b>			
	<b>Drill Size</b>	<b>Pad Size</b>	<b>Trace</b>
<b>BGA Area MicroVia</b>	6 mil Drill	10 mil Pad	3 mils

**Drill size:** 6 mils  
**Pads size:** 10.68 mils  
**Soldermask and solderpaste:** 10.68 mils  
**Trace width in the BGA area:** 3 mils  
**Trace to pad spacing in the BGA:** 3 mils



## Technology level for .5:

For BGA Pitch - 0.50mm			
	TECH I	TECH II	TECH III
BGA area MicroVia Drill/Pad Dia in mils	6/12	6/10	5/9
BGA area BAse Core Via Drill/Pad Dia in mils	8/14	7/14	6/12
BGA Area Trace width and spacing Top Layer	5.00	5.00	5.00
BGA Area Trace width and spacing inner Buildup Layers	5.00	3.00	3.50
BGA Area Trace width and spacing inner Core Layers	5.00	5.00	5.00
BGA Area Trace width and spacing Bottom Layer	5.00	5.00	3.50
# of Traces bet BGA pads on : Top layer	0	0	0
# of Traces bet BGA vias on: Inner Buildup Layers	0	1	1
# of Traces bet BGA vias on : Inner Core Layers	0	0	0

# 5

# 5. Sierra Circuits' Capabilities

## 5.1 Sierra Circuits' preferred materials

We have a list of approved materials that we like to use for HDI circuit boards.

For standard FR-4 lead free boards:

- Isola 370 HR
- Nan Ya NP-175F
- VENTEC
- Nan Ya NPG-170
- Nelco N4000-13SI
- Nelco N9000-13 RF

For standard polyimide boards:

- Isola P95
- Nelco N7000-ZHT

For advanced Teflon boards:

- Rogers RO3000 Series
- Rogers RT/DUROID Series
- Rogers ULTRALAM 2000

For advanced ceramic boards:

- Rogers RO4003
- Rogers RO4230
- Taconics RF-35A2
- Taconics RF-60

For standard Cyanate Ester boards:

- Nelco N8000

For standard ceramic boards:

- Rogers RO4350 F
- Rogers RO4350
- Rogers TTM 3, 4, 6, 10, 10i
- Taconics CER-10

For standard bond sheet boards:

- Hitachi 671N
- Rogers RO4450B, RO4450F

For standard flex boards:

- DuPont Pyralux AP
- DuPont Pyralux LF
- DuPont Pyralux FR

For advanced resistor boards:

- Rogers RO4003 / 4350 TICER TCR

For advanced thermal boards:

- Thermagon 88
- Laird IMPCB

To learn more about our via, drill, pad diameter capabilities, as well as our surface finishes, quality reports, etc., go to our [HDI capabilities](#) page.

## 5.2 Sierra Circuits' HDI Stackup Planner online tool

Get a cost effective, manufacturing-ready PCB stack-up in minutes using our free HDI Stackup Planner tool.

Sierra Circuits developed a unique online tool for electrical engineers and PCB layout designers that gives confidence to build HDI technology into their PCB boards. Design HDI layouts right the first time by getting a complete HDI PCB stack-up in minutes.

Highlights get a complete stack-up before the PCB layout starts:

- **Simple inputs, BIG outputs:** Provide the tool with information, like fastest signal rise/fall time of the devices used, maximum BGA pin count and minimum BGA pitch, and the tool will return complete HDI stack-up options.
- **Compare PCB stack-up options instantly:** Each HDI PCB stack-up option comes with complete information about dielectrics, copper weights, trace width and space and key manufacturing steps required. The Stackup Planner also provides a cost index based on complexity so the electrical engineer and the PCB designer can make informed decisions even before the layout begins.
- **Manufacturing-ready:** Have confidence that you are designing an HDI PCB stack-up that is manufacturing-ready. The tool has been built from an authority in HDI Manufacturing Technology and each HDI PCB stack-up has been tested for accuracy and high yield.
- **Save design iterations:** Instead of ending up with a less-than-optimal HDI design layout, the tool assists the HDI PCB designer to start in the right direction with a proven stack-up, pad sizes, and trace width and space.
- **Pricing and availability:** The online tool will be complimentary for a limited time. Please visit: [www.protoexpress.com/hdi](http://www.protoexpress.com/hdi)

## 5.3 HDI Stackup Planner tutorial

Using Sierra Circuits' free [HDI Stackup Planner](#) before you begin your layout design will ensure that your HDI PCB design will be manufacturable the very first time.

### Step 1: The Board Information

The first thing you have to do to use this tool is to fill out the board information. Fill out a **part number**, like 'Sierra Test' for example; a **revision number**, like 2; the **estimated size of the PCB**, like 4 inches by 4 inches; and then choose the **finished thickness** – you don't have to choose an exact thickness, the HDI Stackup Planner will try to find a thickness that comes close enough – like 0.062 inches, in this case.

# 5

Material Selection 										
Select	Material Name	Type	Application Area  	Tg°C  	DK  	DF  	Electrical Strength 	Cost Factor 	More details	
<input type="radio"/>	NP175	FR4 Family	Medium Speed & Loss	175	4.15	0.0160	1000	1.00	<button>View</button>	
<input type="radio"/>	370HR	FR4 Family	Medium Speed & Loss	180	4.00	0.0180	1350	1.05	<button>View</button>	
<input type="radio"/>	BT (N5000)	BT Epoxy	Microelectronic	185	3.60	0.0140	1200	1.20	<button>View</button>	
<input type="radio"/>	P95 Polyimide	Polyimide	Medium Speed & Loss	260	3.75	0.0180	1100	1.20	<button>View</button>	
<input type="radio"/>	N4000-13	Enhanced Epoxy	High Speed, Low Loss	210	3.50	0.0090	1200	1.20	<button>View</button>	
<input type="radio"/>	N4000-13EP	Enhanced Epoxy	High Speed, Low Loss	210	3.50	0.0090	1200	1.20	<button>View</button>	
<input type="radio"/>	I-Speed	FR-4 Family	High Speed, Low loss	180	3.63	0.0067	1741	1.20	<button>View</button>	

## Step 2: The Material Selection

In order to help you determine what sort of material will best suit your design needs, Sierra Circuits provides a list of 12 materials, with their most important properties, that you can compare. We chose these specific materials out of a whole list of PCB materials because they are suitable for HDI PCB manufacturing, and they almost cover the entire range of HDI applications.

For each material, you can see:

- The type
- The typical application areas
- The glass transition temperature (Tg)
- The dielectric constant (Dk) values
- The dissipation factor (Df) values
- The electrical strength
- The cost factor

We provide the cost factor to give you an idea of the relative cost of each material.

After selecting a material, you can click the "View" button to see a lot more characteristics from the data sheets.

## Step 3: The Stackup Design

Now that you have chosen the material, you can start the stack-up design. The first key design question is whether the outer layers of your final stack-up will be signal or plane. Almost every electrical engineer knows what the answer would be depending on their application and constraints.

[Continue reading on Sierra's blog: www.protoexpress.com/blog/hdi-stackup-planner-tutorial/](http://www.protoexpress.com/blog/hdi-stackup-planner-tutorial/)

## 5.4 About Sierra Circuits

At Sierra Circuits, our engineering staff has been trained on the topics discussed in this article and can analyze the design from a holistic point of view. Their analysis starts with determining the density of the most demanding component. Then, through a systematic set of questions and answers using our in-house HDI assistance design tool, we can recommend a set of stack-up recommendations that meet your cost, performance and timeline needs.

Sierra Circuits is a U.S. based manufacturer of HDI PCBs. Our specialty is quick turn, high technology and small to medium production of printed circuit boards. Our capabilities include laser microvias, blind and buried vias, fine lines and spaces, sequential lamination, via-in-pad technology. With our in-house YAG laser machines, we can laser drill 2-mil, or 50-micron microvias. Sierra Circuits has also pioneered fine line capability. With our laser direct imaging systems, we can provide consistent traces and spaces down to 35 microns in diameter. We also specialize in sequential build applications, using typical PCB materials like FR4, Polyimide, and RCC. We can provide up to 4 build-up layers on expedited lead times. Typical microvia structures include stacked microvias, buried microvias, staggered or stepped microvias.

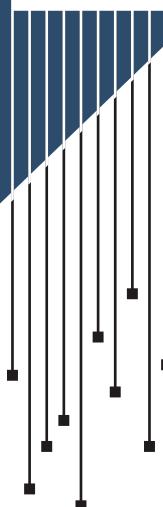
For our microelectronics PCBs and PCB substrates, we can provide build-up technology with fine lines and spaces down to 40 microns, high-temperature materials, like polyimide, stacked microvias, buried resistors, and multi-tiered cavity PCBs. We have provided microelectronic PCBs with fine pitch devices down to 200 microns, using 50-micron laser drilled via-in-pad technology and thin build-up materials. Our quality checks include surface cleanliness and wirebondability. Some examples of surface finish include OSP, ENIG, ENEPIG, Soft Gold.

Our engineering support provides valuable suggestions with their knowledge of high-speed designs, analog/digital, high-density PCB manufacturing design rules and design for assembly rules. Upload your data and receive a free consultation and review of your design. Services include system level design, schematic capture, PCB layout, and PCB/PCBA DFM.



# Thank you...

**...to all the great PCB experts who contributed to this HDI Design Guide!**



Before we even began to start writing this design guide, it was clear that we were going to need the best PCB experts to give us their best tips. This is exactly what they did and we personally want to thank each one of these PCB designers, engineers, influencers, etc. who took the time to answer our questions and help us make this HDI design guide come to life.

## **Randy Clemons, San Diego PCB**

Randy, ever since we've met you at Rick's San Diego workshop in February, you've always answered our questions whenever we needed your expertise. Thank you for helping us out every so often. We love your blog and we'd love to partner even more with you in the future!

## **Ben Jordan, Altium**

Ben, we've done so much with you in the past few years that it almost feels like you're part of the Sierra family! Thanks for always being there for us!

## **Robert Feranec, Fedevlel Academy**

Rob, it's always a pleasure to pick up your brain for designing tips. You're one of the greatest experts of our industry and we're honored to feature your advice in our design guide. Thank you!

## **Steve Watt, Zuken**

Steve, we met you last year at PCB West for an interview at our booth and here you are this year in our brand new HDI Design Guide. Let's plan something for 2019, shall we? But seriously, thank you for your valuable HDI recommendations!

## **Rick Hartley, RHartley Enterprises**

Rick, attending your Control of Noise, EMI and Signal Integrity in High-Speed Circuits workshop was a fantastic learning experience. From that day, we knew we would need to feature the EMI Jedi – as people call you; we swear we didn't come up with that nickname! – in our design guide. Thank you for helping us educate the designer community!

## **Eric Bogatin, Teledyne Lecroy**

Signal integrity and Eric Bogatin go hand in hand, don't they? Thank you Eric for contributing to this design guide. Our signal integrity section couldn't have been complete without your immense knowledge!

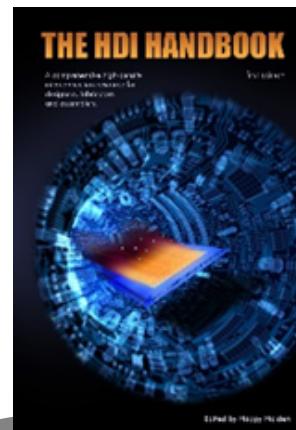
## **Happy Holden, Father of HDI**

And, of course, a huge thank you to you, Hap! Thanks for helping us with the content. Thanks for answering all of our questions and providing us great documentation to work with. Thanks for reviewing this design guide of 50+ pages in just 24 hours. Thanks for your wise foreword. Thanks for everything!

Because we couldn't cover the whole topic of HDI, you should download Happy's free 600-page HDI HANDBOOK at:

<http://hdihandbook.com/> (English)

<http://hdihandbook.cn/> (Simplified Chinese)



**Now we only have one question: Are you ready to contribute to our next design guide? ;)**

# Designer's Best Friend

---



Sierra Circuits, Inc.  
1108 West Evelyn Avenue  
Sunnyvale, CA 94086