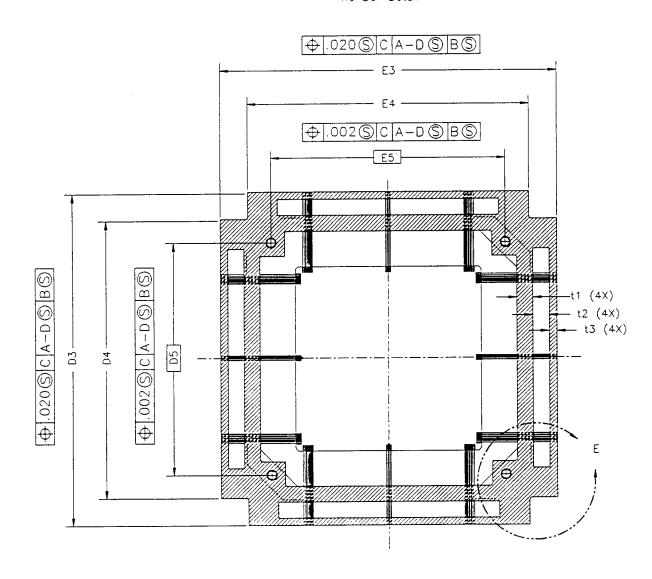


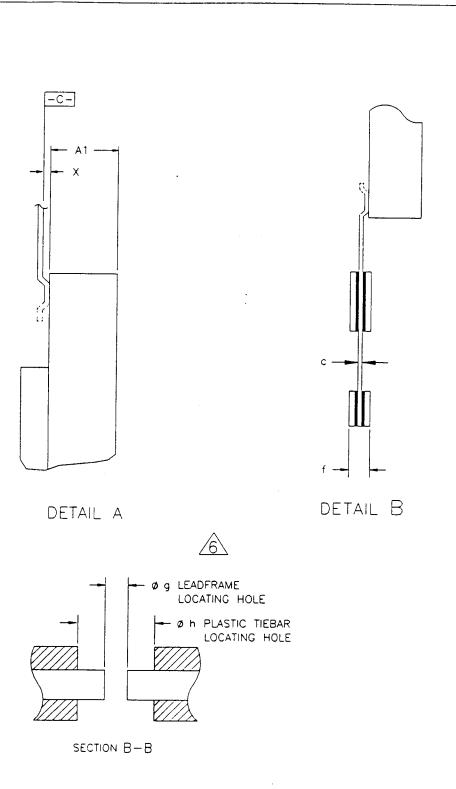
National Semiconductor has stated that U.S. Patent No. 4,796,080 may relate to a certain implementation of this package outline. The sponsor has not agreed with this statement.

JEDEC Solid State Product Outline	TOP BRAZED CERAMIC LEADED CHIP CARRIER (.015 INCH LEAD PITCH) WITH PLASTIC NON-CONDUCTIVE TIE BAR	issue A	DATE Sept. 1992	MO-130	SHEET	
---	---	------------	-----------------------	--------	-------	--

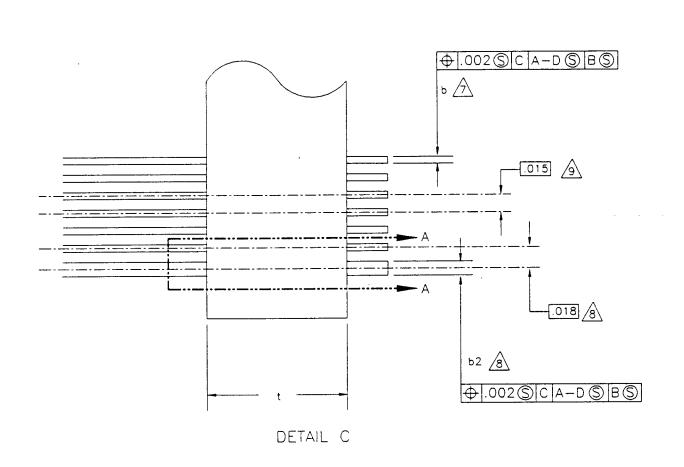


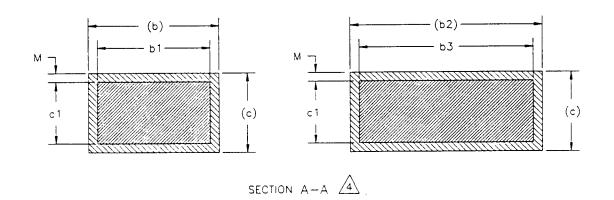


JEDEC Solid State Product Outline TOP BRAZED CERAMIC LEADED CHIP CARRIER (.015 INCH LEAD PITCH) WITH PLASTIC NON-CONDUCTIVE TIE BAR	issue A	DATE Sept. 1992	MO-130	SHEET 2/7	
--	------------	-----------------------	--------	--------------	--

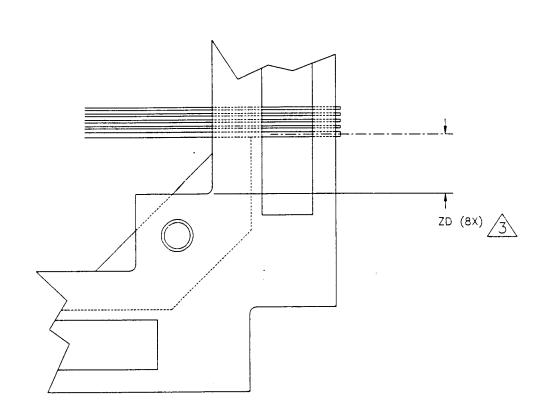


JEDEC	TOP BRAZED CERAMIC LEADED CHIP CARRIER	ISSUE	DATE		SHEET
Solid State Product Outline	(.015 INCH LEAD PITCH) WITH PLASTIC NON-CONDUCTIVE TIE BAR	A	Sept. 1992	MO-130	3/7

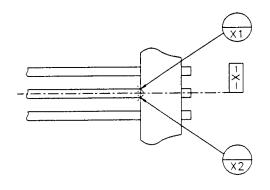




JEDEC Solid State Product Outline	TOP BRAZED CERAMIC LEADED CHIP CARRIER (.015 INCH LEAD PITCH) WITH PLASTIC NON-CONDUCTIVE TIE BAR	issue A	DATE Sept. 1992	MO-130	SHEET 4/7	
---	---	------------	-----------------------	--------	--------------	--



DETAIL E



 $X = \begin{bmatrix} -A - \end{bmatrix}, \begin{bmatrix} -B - \end{bmatrix}$ OR $\begin{bmatrix} -D - \end{bmatrix}$

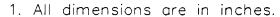
DETAIL D

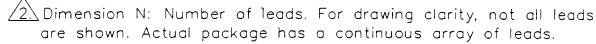
Solid State Product	TOP BRAZED CERAMIC LEADED CHIP CARRIER (.015 INCH LEAD PITCH) WITH PLASTIC NON—CONDUCTIVE TIE BAR	issue A	DATE Sept. 1992	MO-130	SHEET 5/7
---------------------	---	------------	-----------------------	--------	--------------

S	VA	ARIATIONS		
N≻≯BO		AA		70-m
0.7	MIN	NOM	MAX	Ē
Α		_	0.125	
A1	0.092	0.096	0.100	
Ь	0.005	0.006	0.007	
ь1	0.0044	0.0054	0.0064	4
b2	0.011	0.012	0.013	
ь3	0.0104	0.0114	0.0124	4
С	0.0025	0.003	0.004	
c1	0.0019	0.0024.	0.0034	4
D	1.380	1.390	1.400	
D2	1.910	1.920	1.930	
D3	2.505	2.510	2.515	
D4	2.095	2.100	2.105	
D5	1.748	1.750	1.752	
E	1.380	1.390	1.400	
E2	1.910	1.920	1.930	
E3	2.505	2.510	2.515	
E4	2.095	2.100	2.105	
E5	1.748	1.750	1.752	
f	0.015	0.025	0.045	
g	0.063	0.064	0.065	
h	0.072	0.074	0.076	
Χ	0.002	0.008	0.014	
L1	0.260	0.265	0.270	
М	_	-	0.0003	4
t1	0.115	0.120	0.125	
t2	0.115	0.120	0.125	
t3	0.050	0.055	0.060	
ZD	0.184	0.204	0.224	
N		340		2
NOTE	1 . 5			
REF	10-299			
ISSUE	Α			

JEDEC	TOP BRAZED CERAMIC LEADED CHIP CARRIER	ISSUE	DATE		SHEET
Solid State Product Outline	(.015 INCH LEAD PITCH) WITH PLASTIC NON—CONDUCTIVE TIE BAR	A	Sept. 1992	MO-130	6/7







3. Plastic tie bar will not overhang lead tips.

Dimension b1,b3 and c1 apply to base metal only. Dimension M applies to plating thickness.

5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

These holes are to be used for locating the package during tie bar attach, electrical testing, trim, form and excise operations.

 \nearrow Occurs on N-8 places. (width for all leads except corner leads).

8 Occurs on 8 corner leads.

 \bigcirc Occurs on N-12 places. (pitch for all leads except corner leads)

Datum A-D and -B- to be determined by datum points where leads contact the tie bar.

JEDEC Solid State Product Outline	TOP BRAZED CERAMIC LEADED CHIP CARRIER (.015 INCH LEAD PITCH) WITH PLASTIC NON-CONDUCTIVE TIF BAR	issue A	DATE Sept. 1992	MO-130	SHEET
	IIE BAR				