JTAG/SWD Interface

The ULINK*plus* supports an isolated JTAG/SWD interface using a low-cost 10-pin (0.05") connector.

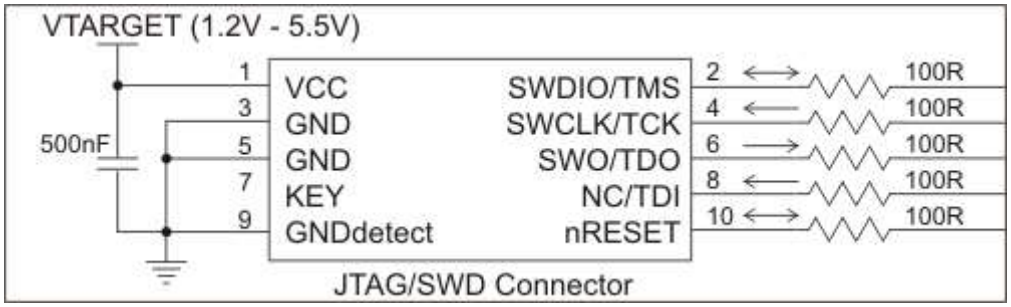
Technical characteristics

Interface	Description
JTAG/SWD	Voltage range: 1.2 V .. 5.5 V Clock speed: configurable up to 10 MHz SWO trace capturing: data rate up to 50 Mbit/s (UART/NRZ Mode) Isolation: 1 kV Supports hot-plugging to a running target

Interface Schematic

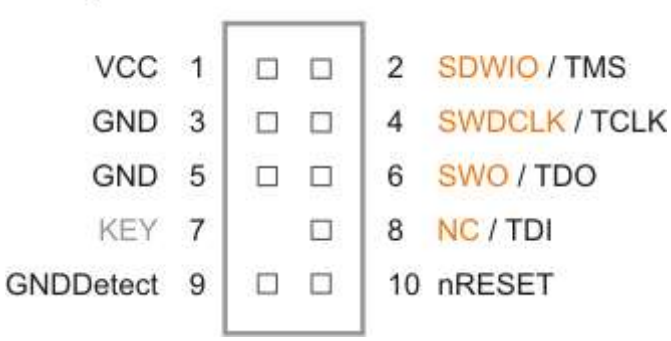
The target interface schematic shows the JTAG and Serial Wire interface circuits of ULINK*plus*. All pins are 1kV isolated and support hot-plugging while the target is running.

Use this schematic to help with board design, and for analyzing and debugging your target hardware.



JTAG/SWD Connector

The 10-pin, 0.05" JTAG/SWD connector offers ITM and DWT trace information. In SWD mode, two pins are used for debugging: one bi-directional pin (SWDIO) transfers the information and the second pin (SWDCLK) clocks the data. A third pin (SWO) delivers the trace data at minimum system cost. The Serial Wire and JTAG pins are shared.



Note

- KEY (position 7) has no pin and serves only as a key to properly orient the connector.
- VCC (pin 1) provides the supply voltage for the JTAG/SWD I/O driver and is required as ULINK*plus* has isolated connection.
- The 10-pin connector is a Samtec 10-pin: FTSH-105-01-L-DV-007-K connector with pin 7 removed. It's dimensions are: 0.25" x 0.188" (6.35mm x 4.78mm).

JTAG and Serial Wire Signals

Because the 10-pin **JTAG/SWD** connector supports both JTAG and Serial Wire signals, you can configure the debugger for either JTAG or Serial Wire mode to suit your Cortex device.

JTAG Signals

Signal	Connects to...
TMS	Test Mode State pin -- Use 100K Ohm pull-up resistor to VCC.
TDO	Test Data Out pin.
TDI	Test Data In pin -- Use 100K Ohm pull-up resistor to VCC.
TCLK	Test CLocK pin -- Use 100K Ohm pull-down resistor to GND.
VCC	Positive Supply Voltage -- Power supply for JTAG interface drivers.
GND	Digital ground.
RESET	RSTIN/ pin -- Connect this pin to the (active low) reset input of the target CPU.

Serial Wire Signals

The Serial Wire mode differs to JTAG debugging, because only two pins are used for the communication. A third pin can be used optionally to trace data. JTAG pins and SW pins are shared.

- **TCLK** is **SWCLK** (Serial Wire Clock)
- **TMS** is **SWDIO** (Serial Wire debug Data Input/Output)
- **TDO** is **SWO** (Serial Wire trace Output)

Signal	Connects to...
SWDIO	Data I/O pin -- Use 100K Ohm pull-up resistor to VCC.
SWO	Optional trace output pin.
SWCLK	Clock pin -- Use 100K Ohm pull-down resistor to GND.
VCC	Positive Supply Voltage -- Power supply for JTAG interface drivers.
GND	Digital ground.
RESET	RSTIN/ pin -- Connect this pin to the (active low) reset input of the target CPU.

Note

- Usually, devices do not include pull-up or pull-down resistors on JTAG nor SW pins. Resistors should be added externally onto the board. However, do not add resistors when the device includes them already.