



## PCB Layout

Some circuit designs are fabricated on tiny silicon wafers and others consist of various components connected by cables. However, the circuits that are often the center of an EMC engineer's attention are those that are laid out on fiberglass epoxy boards. Printed circuit boards similar to the one illustrated in Figure 1 can be found in nearly all electronic systems. Circuit *components* with metal pins are connected by copper *traces*. *Surface mount technology* (SMT) components are glued to the top and/or bottom of a board. *Pin-in-hole* components are held to the board by their pins, which extend through the board and are soldered to the traces on the opposite side.

Single-layer boards have all of the traces routed on one side of the board. Double-layer boards have traces on both sides. Many boards have several layers of copper traces separated by layers of fiberglass epoxy (or a similar dielectric). These are referred to as multi-layer boards. The number of layers is usually even. Four-layer boards are very common in low-cost products. Boards with dozens of layers are sometimes used to connect densely populated boards with high component pin counts.

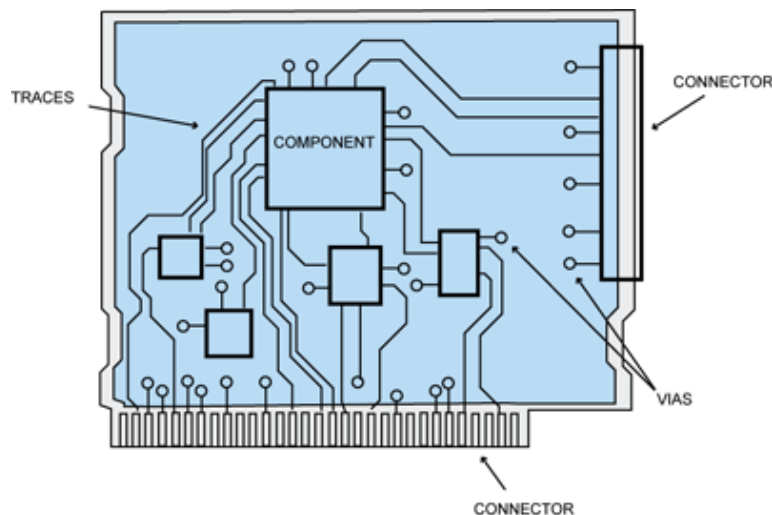


Figure 1: A printed circuit board.

Multi-layer boards usually have entire layers with solid copper planes dedicated to the distribution of power to the components on the board. These planes are usually named after the component pins they are connected to. For example, a copper plane connecting all of the  $V_{CC}$  components pins to the power supply is often called a  $V_{CC}$  plane.

The placement of components and the routing of traces usually play a crucial role in determining the electromagnetic compatibility of products employing printed circuit boards. Well laid out boards will not radiate significantly on their own and they do a good job of minimizing currents and fields that might couple noise to cables or other objects off the board. They also are configured to minimize opportunities for external currents or fields to couple interfering signals on to the board.

## Strategies for Laying Out Printed Circuit Boards

Most board designers employ a list of guidelines to help place components and route traces. For example, a typical guideline might be "minimize the length of all traces carrying a digital clock signal." Often, a designer is not familiar with the reason for the guideline or does not fully understand the consequences of violating the guideline for a particular application.

### Quiz Question

Suppose you're laying out a high-speed multi-layer printed circuit board and you need to route a trace carrying a high-frequency signal from a digital component to an analog amplifier. You want to minimize the chance of having an electromagnetic compatibility (EMC) problem, so you search the web for EMC design guidelines and you find three guidelines that seem to pertain to your situation:

1. minimize the length of high-speed traces;
2. always gap any solid planes between analog and digital circuits; and
3. never let a high-speed trace cross over a gap in the signal return plane.

You envision the three possible routing strategies illustrated in Figure 2. The first routing strategy routes the trace directly between the two components, but leaves the plane between them solid. The second routing strategy gaps the plane, but routes the trace over the gap. The third routing strategy routes the trace around the gap. Each of these alternatives violates one of the guidelines. Which is the best choice?

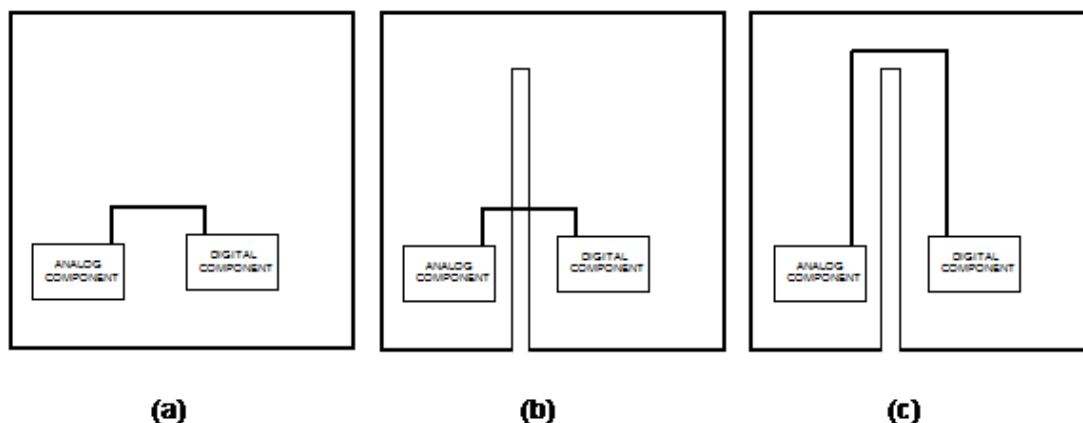


Figure 2: Which is the best trace routing alternative?

Is each alternative equally good because it satisfies 2 of 3 guidelines? Are they all bad because they all violate at least one guideline? These are the types of questions that circuit board designers are faced with every day. Making the right choice can be the difference between a board that meets all requirements and a board that has severe radiated emissions or susceptibility problems. In this case, one of the choices is much better than the other two. However before we reveal the correct answer, let's develop a strategy for evaluating printed circuit board layouts. With a proper strategy, the correct answer to this quiz question should become apparent.

In this tutorial, we will explore 4 steps that every EMC engineer should apply when laying out a printed circuit board or reviewing an existing board design. These steps are:

- Identify potential EMI sources and victims
- Identify critical current paths
- Identify potential antenna parts
- Explore possible coupling mechanisms.

By taking the steps outlined above first, component placement and trace routing decisions will become clearer. It should also be much more apparent which design guidelines are most important and which are not important at all for a specific design.

## Identifying Potential EMI Sources and Victims

A typical circuit board may have dozens, hundreds or even thousands of circuits. Each circuit is a potential source of energy that might eventually be coupled unintentionally to other circuits or devices. Each circuit is also a potential victim of unintentionally coupled noise. However, some circuits are much more likely than others to be a noise source and other circuits are much more likely to be victims. EMC engineers (and board designers) should be able to recognize those circuits that are potentially good sources and those that are potentially most susceptible. Circuits of particular interest are discussed below.

### Digital Clock Circuits

Synchronous digital circuits employ a system clock that must be sent to every active component (on or off the board) that needs to interpret the digital signal. Clock signals are constantly switching and have narrow band harmonics. They are often among the most energetic signals on a printed circuit board. For this reason, it is not uncommon to see narrow band radiated emission peaks at harmonics of the clock frequency, as illustrated in Figure 3.

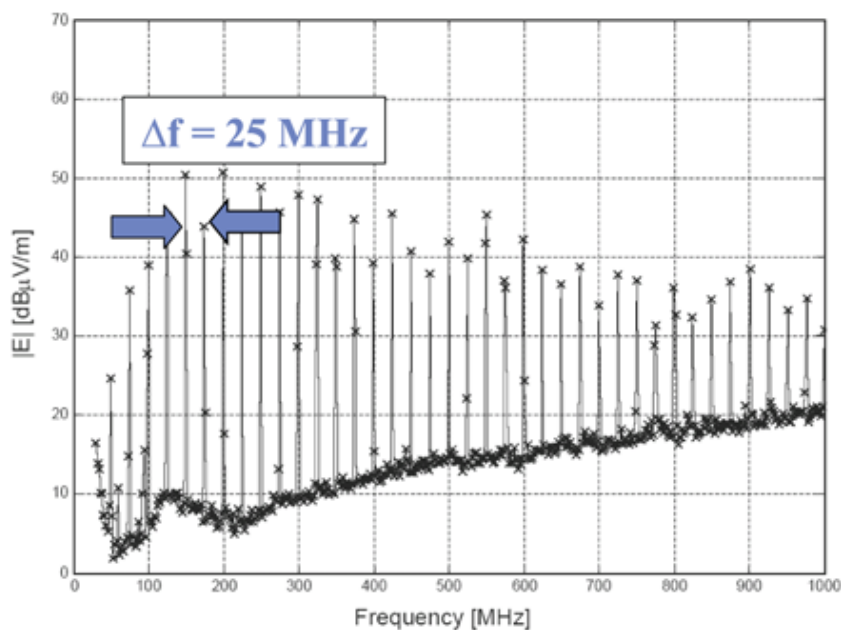


Figure 3: Radiated emissions from a product with a 25-MHz clock.

In this figure, the radiated emissions are clearly dominated by harmonics of the 25-MHz clock. The noise floor from 200 – 1000 MHz is the thermal noise of the spectrum analyzer used to make the measurement (corrected to reflect the antenna factor). In order to make this product compliant with the FCC or CISPR Class B radiated emission specification, the clock source amplitude would have to be decreased, the unintentional "antenna" made less efficient, or the source-antenna coupling path attenuated.

## Digital Signals

Most of the traces on a digital printed circuit board are carrying digital information rather than clock signals. Digital signals are not as periodic as clock signals, and their random nature results in noise that is more broadband. Digital signals that toggle more often can result in radiation similar to clock signals. An example of this would be the least significant bit on a microprocessor address bus, since stepping through consecutive addresses can cause this signal to toggle at the clock frequency. The exact form and strength of the radiation from digital signals depends on many factors including the software running and the encoding scheme employed. Generally, data signals are a less troublesome source than clock signals; however high-speed data can still produce significant amounts of noise.

## Power Switching Circuits

Switch-mode power supplies and DC-DC converters generate different voltages by switching the current into a transformer on and off rapidly. Typical switching frequencies are in the 10 - 100 kHz range. The spikes of current generated by this switching can couple noise to the power output and other devices on the board. Although this noise signal is relatively periodic (i.e. narrow band harmonics), it appears as broadband noise during a radiated emissions test because the distance between harmonic frequencies is lower than the resolution bandwidth of the measurement.

The small hump in the noise floor around 120 MHz in Figure 3 is due to power switching noise. In this product, the switching noise is negligible relative to the clock noise. However in other products the power switching noise can dominate, since only the upper harmonics of the switching noise fall in the frequency range where radiated emission are measured. Power switching noise can always be reduced by slowing down the transition time of the switching circuit. However, this reduces the efficiency of the power supply, so alternate methods are preferred. Possible solutions are discussed in the Conducted EMI tutorial.

## Analog Signals

Analog signals can be broadband or narrowband, high frequency or low frequency. If your board employs analog signals, it is a good idea to be familiar with what these signals look like in both the time and frequency domains. Narrowband, high-frequency analog signals can be particularly difficult to work with. Fortunately, since analog signals tend to be sensitive to low levels of noise, signal integrity concerns usually dictate that they are laid out in a manner that will minimize radiated emissions.

## DC Power Traces and Low-speed Digital Signals

Generally speaking, DC power and low-speed digital signals do not have enough power at radiated emission frequencies to be troublesome. Nevertheless, these traces are often the source of the most difficult radiated emissions problems. This is because the unintentional high frequency voltages and currents on these traces can be as great as or greater than the voltages and currents on high-speed traces.

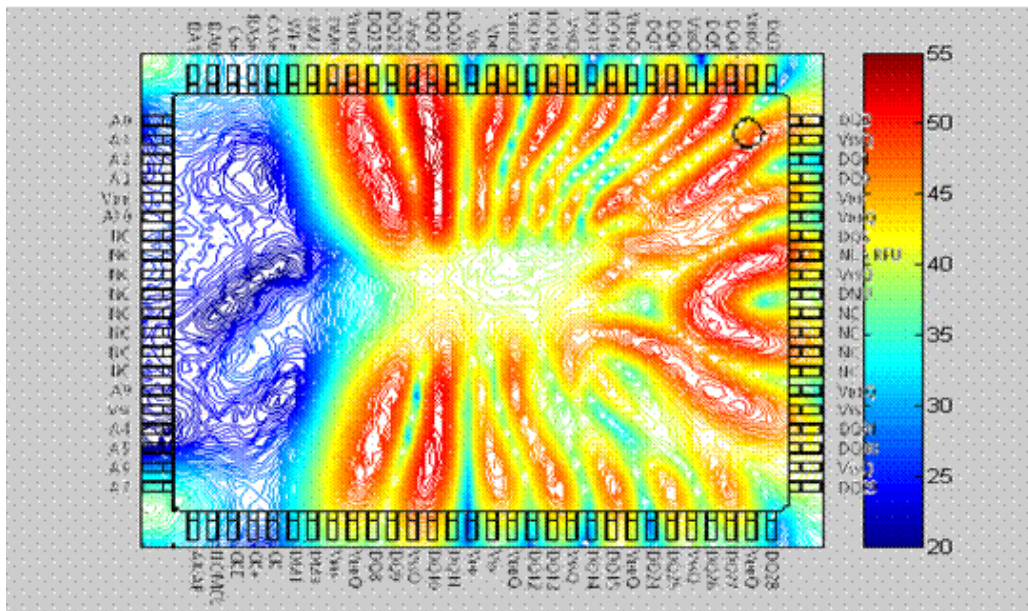


Figure 4: Near magnetic field above a packaged integrated circuit.

Figure 4 shows a map of the near magnetic field above a dynamic random access memory module commonly used in personal computers. The near magnetic field provides an indication of the currents flowing in the lead frame of the component package. The frequency of the measurement is the third harmonic of the clock frequency. Note that more current is being drawn from the DC power supply pins than is being drawn from the signal pins.

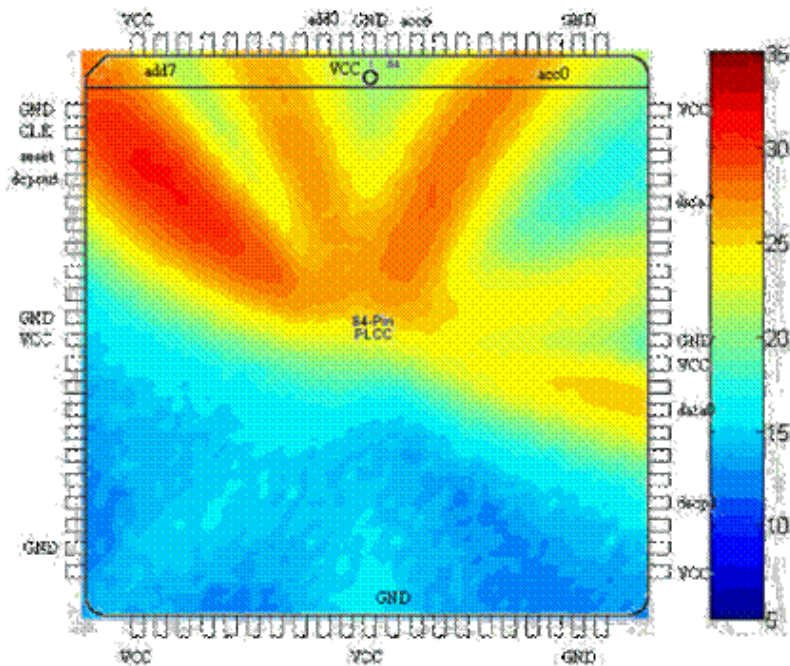


Figure 5: Near magnetic field above a microprocessor.

Figure 5 shows a similar plot of the near magnetic fields above a microprocessor implemented in a field programmable gate array (FPGA). In this figure, we see that the currents injected onto some of the low-speed address lines are nearly as strong as the currents in the clock signal.

How do high-frequency currents and voltages appear on low-frequency data lines? There are several ways that this can happen. Most have to do with the design and layout of the integrated circuits (ICs) connected to these traces. Some ICs do a good job of containing their internally generated noise and others do not. A poor design can put high-frequency voltage fluctuations on every input and output trace connected to the IC. Good designs can be relatively quiet.

When laying out a printed circuit board with an unfamiliar IC that is clocked internally at a high frequency, it is a good idea to treat every pin on that IC as if it were a high-frequency source with the same characteristics as the internal clock. Otherwise, the power or low-speed digital traces could be the most significant sources of radiated emissions.

## Identifying Current Paths

Perhaps the most important distinction between digital circuit designers and EMC engineers is that EMC (and signal integrity) engineers pay close attention to the currents flowing in a circuit as well as the voltages. This is a very important point. Most poor designs are the direct result of neglecting to consider where the signal currents were likely to flow.

Although this has already been discussed in a previous section, the subject of current path identification is so crucial to good printed circuit board design that it's worth reviewing the main concepts here. First and foremost,

## 1. Current flows in loops.

The same amount of current that flows out one side of a source must be drawn in from the other side. Also,

## 2. Current takes the path of least impedance.

At low (kHz and lower) frequencies, impedance is dominated by resistance, so current takes the path(s) of least resistance. At high (MHz and higher) frequencies, impedance is dominated by the inductance term so the current takes the path of least inductance.

Consider the circuit board layout illustrated in Figure 6. A 50-MHz signal propagates on a trace above a plane from Component A to Component B. We know that an equal amount of current must therefore flow from Component B to Component A. In this case we'll assume that this current exits the pin of Component B labeled GND and makes its way back to the pin of Component A labeled GND. Since a solid plane is provided and the ground pins of both components are close, it is tempting to conclude that the current takes the shortest path between them. However, we now know that this is not correct. High-frequency currents take the path of least inductance or the path of least loop area. The majority of the signal current returning on the plane therefore flows in a narrow path (Path 2) directly underneath the signal trace.

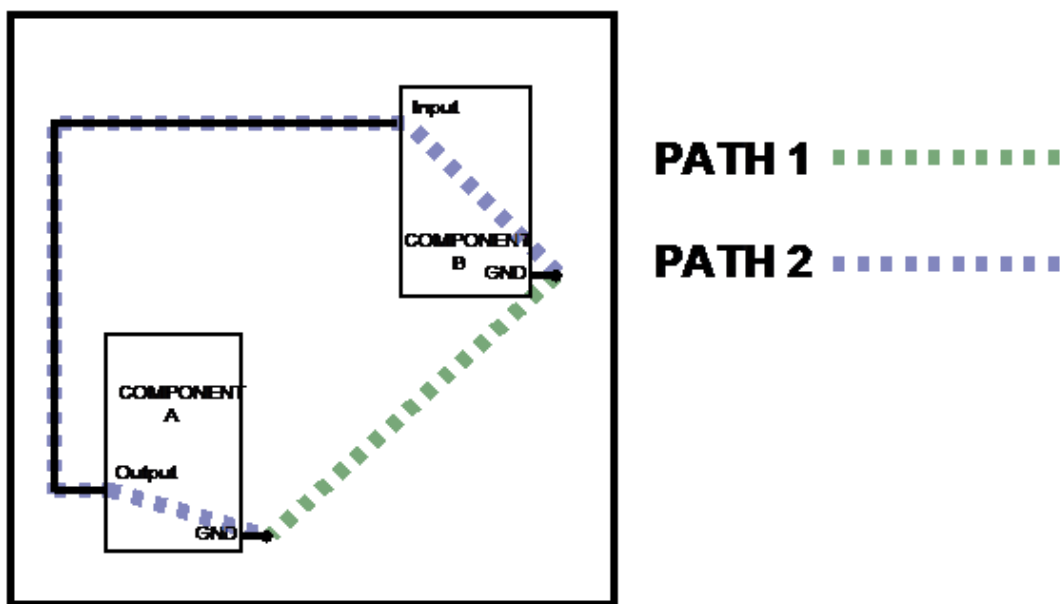


Figure 6: Which path does the signal return current take?

If the plane were to be gapped for any reason, as shown in Figure 7, a gap in position 2 would have little effect on the signal integrity or on radiated emissions. A gap in position 1 however, could result in significant problems. Current returning on the plane under the trace is forced to go around the gap. This significantly increases the signal loop area.

At low frequencies (generally kHz frequencies and below), the resistance of the planes tends to spread the current out so that current flowing between two distant points can cover most of the board as shown in Figure 8. On mixed signal boards, with low-frequency analog and digital components, this can create problems. Figure 9 illustrates how a well-placed gap in the ground plane can protect circuits located in a particular region of the board from low-frequency return currents flowing in the plane.

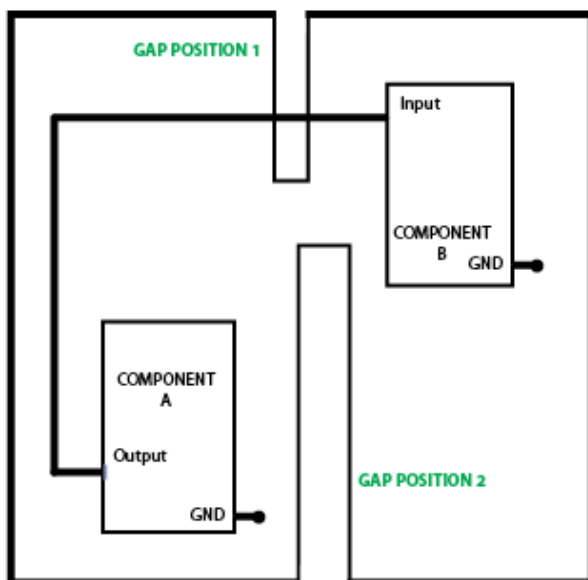




Figure 7: Which gap position affects the flow of the signal return current?

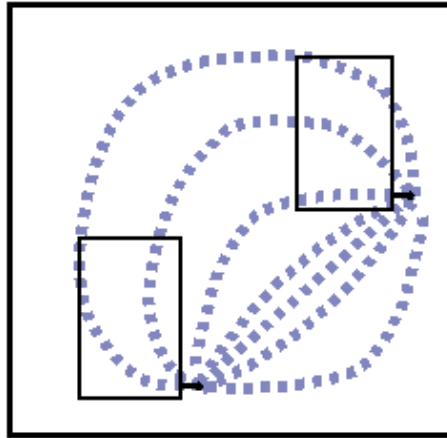


Figure 8: Low-frequency return current path

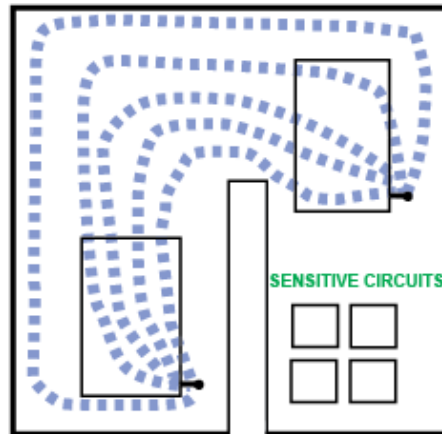


Figure 9: Low-frequency return current path with a gapped plane.

## Identifying Antennas

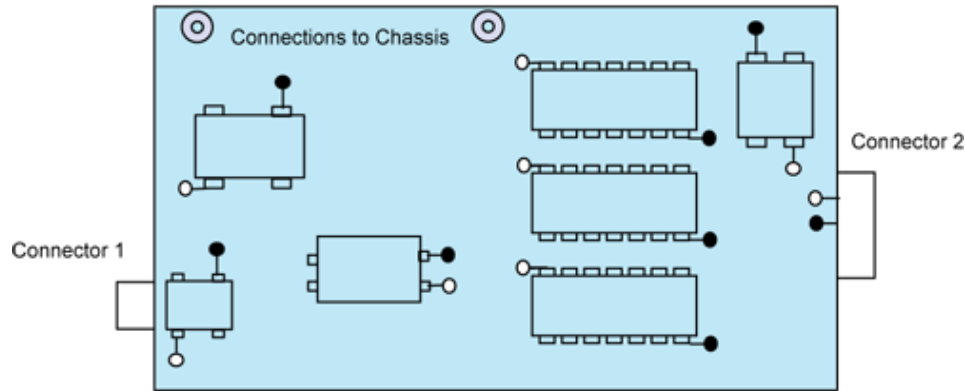
The section on electromagnetic radiation pointed out that there are basically 3 conditions that have to be met in order for most of the unintentional antennas that an EMC engineer encounters to radiate effectively:

1. The antenna must have two parts;
2. both parts must not be electrically small;
3. something must induce a voltage between the 2 parts.

Most printed circuit boards are electrically small at frequencies below about 100 MHz ( $\lambda > 3$  meters). This implies that any efficient antenna parts must be relatively large compared to most of the board components. Generally, at low frequencies the only viable antenna parts are the attached cables and/or a metallic chassis. If a printed circuit board is laid out in a manner that minimizes the possibility of inducing a voltage between any two of these possible antenna parts, then it is much less likely to have a radiated emission or radiated susceptibility problem.

Figure 10 shows two printed circuit board layouts. The connectors and chassis connections represent possible efficient antenna parts. Layout #2 is less likely to have radiated coupling problems below 100 MHz, because it is less likely to develop a significant voltage between any two conductors capable of serving as an efficient antenna. This was achieved simply by placing the two connectors on the same side of the board.

## LAYOUT #1



## LAYOUT #2

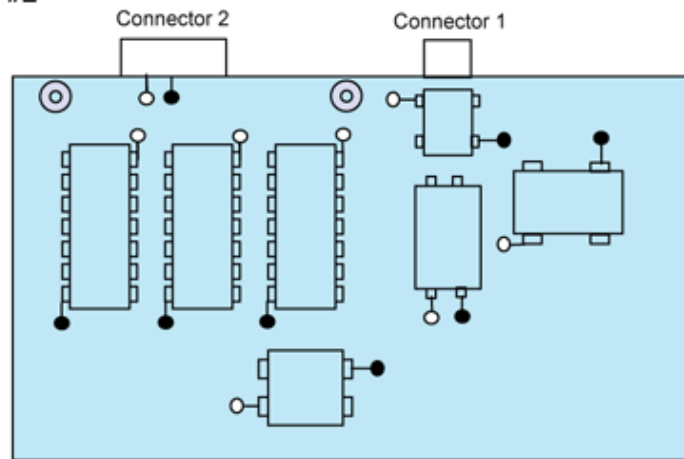


Figure 10. Two printed circuit board layouts.

At frequencies above 100 MHz, wavelengths are shorter and it becomes more likely that objects mounted on the board (or the board itself) can serve as efficient antenna parts. Nevertheless, even at frequencies up to several GHz, these antenna parts should be relatively easy to spot. For example, at 1 GHz the wavelength in free space is 30 cm. A quarter wavelength is 7.5 cm. Therefore an efficient antenna part will have to be at least several centimeters long and be driven relative to something that is just as large or larger. Recall that differential currents (currents whose return path is nearby) are relatively inefficient radiation sources. This means that a trace lying right beside or above its current return path is not a good antenna part. So if one half of our antenna is a metallic plane in the board, the other half must stick up and away from the plane. This helps to make these antenna parts readily identifiable even at relatively high frequencies. Table 1 lists common antenna parts found on printed circuit boards above and below 100 MHz.

Table 1: Printed Circuit Board Objects That May or May Not be Parts of a Good Antenna.

Good Antenna Parts		Poor Antenna Parts	
< 100 MHz	> 100 MHz	< 100 MHz	> 100 MHz
cables	heatsinks		
	power planes	microstrip or stripline traces	microstrip or stripline traces
	tall components	anything that is not big	
	seams in shielding enclosures		

## Identifying Coupling Mechanisms

Once we have identified the potential sources or victims and the potential antennas, good board layout is simply a matter of minimizing the coupling between the two. Earlier, we learned that there are only 4 categories of possible electromagnetic coupling mechanisms:

- Conducted coupling,
- Electric field coupling
- Magnetic field coupling
- Radiation.

Since we're talking about coupling between a source and its antenna on the same printed circuit board, we are not likely to have radiation coupling. Therefore, there are only three coupling mechanisms that we need to consider. Conducted coupling will only occur if the source we have identified directly drives one good antenna part relative to another. An example of conducted coupling would be a signal trace that was long enough to be an efficient antenna part driven relative to signal return plane but not routed over that plane. In this case, the source would be the signal source and the antenna would be the trace-plane pair. Clearly, high-frequency signals driven directly onto traces or other conductors need to be returned to their source on other conductors that are nearby to avoid radiated emissions due to direct conducted coupling between the source and the antenna.

Conducted coupling tends to be easy to spot once the source and the antenna parts have been identified. The field coupling mechanisms however, tend to be less obvious. In order to make field coupling a little more intuitive, it is convenient to think of electric field coupling as coupling that is proportional to the source voltage (*voltage driven*) and magnetic field coupling as coupling that is proportional to the source current (*current driven*).

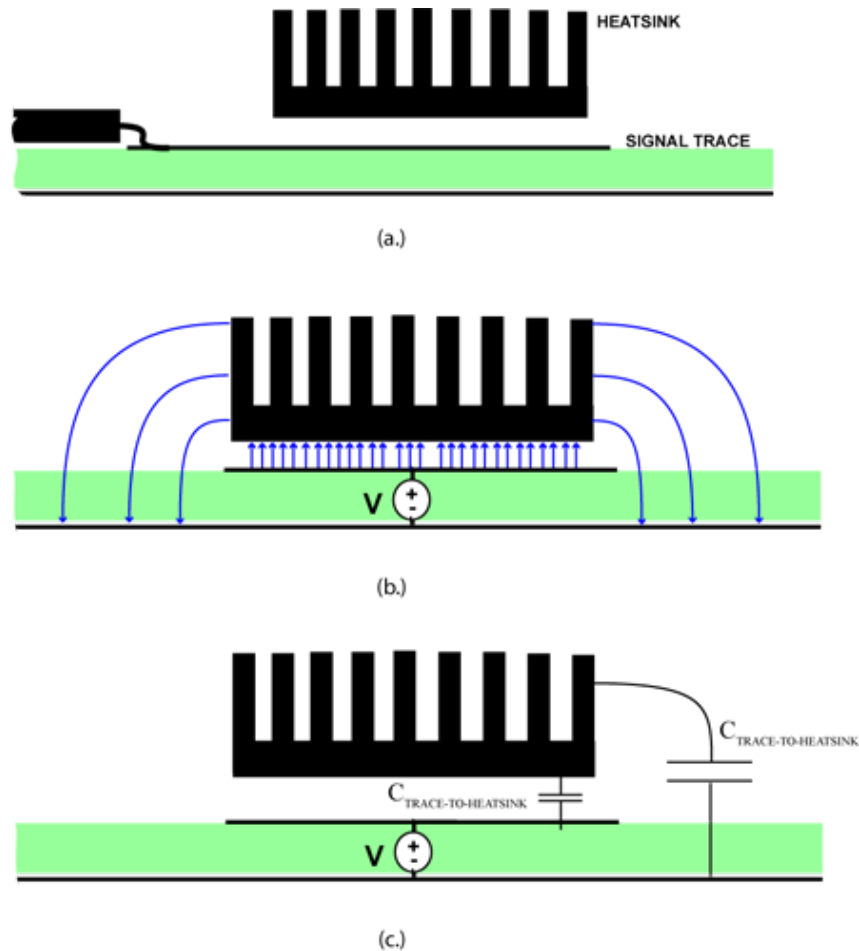


Figure 11: Printed circuit board trace coupling to a heatsink.

## Voltage-Driven Coupling

An example of voltage-driven coupling that results in radiated emissions is illustrated in Figure 11(a), which shows a signal trace routed beneath a heatsink. If the heatsink is not electrically small, it is potentially an effective antenna part. The board's metal planes are another potential antenna part. The trace does not connect directly to the heatsink, so there is no conducted coupling path. However, the voltage on the trace can drive the heatsink relative to the board because electric field lines between the trace and board are intercepted by the heatsink, as illustrated in Figure 11(b). This electric field coupling can be represented by capacitances as indicated in Figure 11(c). The voltage induced on the heatsink relative to the board is given by,

$$\begin{aligned}
 V_{\text{HEATSINK}} &= V_{\text{SIGNAL}} \frac{Z_{\text{HEATSINK-TO-BOARD}}}{Z_{\text{TRACE-TO-HEATSINK}} + Z_{\text{HEATSINK-TO-BOARD}}} \\
 &= V_{\text{SIGNAL}} \frac{C_{\text{TRACE-TO-HEATSINK}}}{C_{\text{TRACE-TO-HEATSINK}} + C_{\text{HEATSINK-TO-BOARD}}}
 \end{aligned}$$

Usually, board designers avoid routing high-speed signal traces directly under large heatsinks. Another more common example of voltage-driven coupling is illustrated in Figure 12. An active component is sandwiched between a printed circuit board and a heatsink. Again, neither the board nor the heatsink is electrically small at the frequency of interest. The average voltage on the component is not equal to the voltage on the board due to the fact that the component is drawing high-frequency current through a finite connection inductance, as indicated in Figure 12(a). This voltage drives the surface of the component relative to the surface of



the board as indicated by the model in Figure 12(b). There is no direct connection between the heatsink and the source, so we cannot have conducted coupling. However, the capacitance between the surface of the component and the heatsink provides an indirect (electric-field) connection.

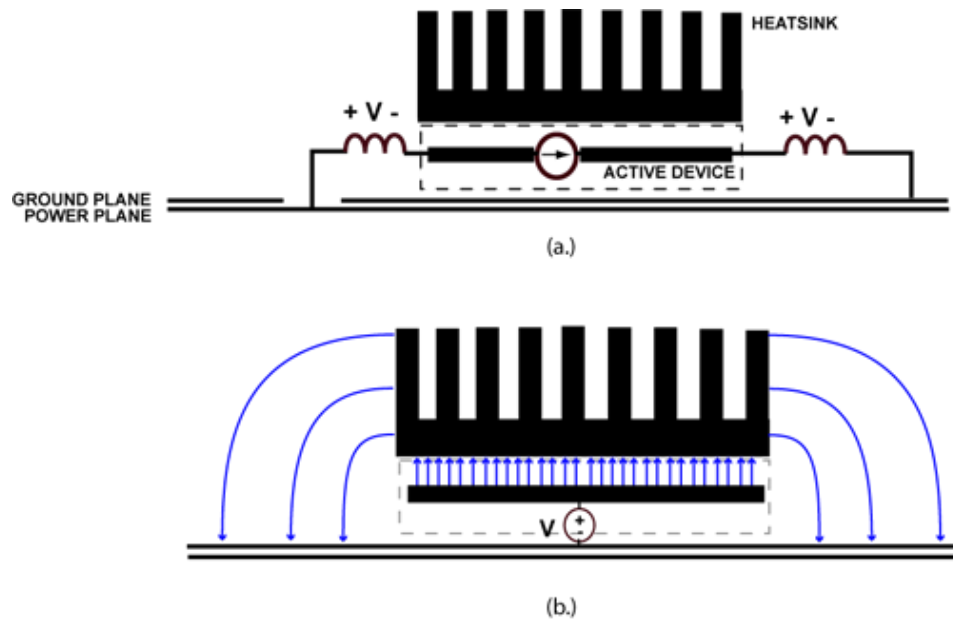


Figure 12: Component voltage driving a heatsink relative to a circuit board.

Note that in this case, it was a current driving an inductance that created the source voltage. In other words, there was a magnetic field involved in the coupling process. Nevertheless, the field coupling the component to the antenna is an electric field and the radiated emissions are proportional to the component's voltage relative to the board. Therefore, we still refer to this as voltage-driven coupling.

## Current-Driven Coupling

When the coupling between the source and antenna is due to a magnetic field and proportional to the signal current, it is referred to as *current-driven* coupling. Circuit designers often think of signals in terms of voltages and therefore are less likely to inadvertently drive a good antenna with a signal voltage. However, if they neglect to consider where the currents are flowing, there is a good chance that their design may drive two good antenna parts with a magnetic field.

A very common example of current-driven coupling is illustrated in Figure 13. An otherwise well-designed board has connectors attached to each side. We'll assume for now that the cables are perfectly shielded and the cable shields are connected to the "ground" plane on the circuit board. A circuit consisting of a single microstrip trace driven at one end and terminated at the other end is located between the two connectors.

We already know that microstrip traces are not efficient radiated emission sources, so the only possible antenna parts in this design are the two cable shields, and they are both "grounded". We expect the two antenna parts to be at the same potential, because they are connected to each other with a wide copper plane. However, remember that an important requirement for a "ground" conductor is that it not carry intentional power or signal currents.

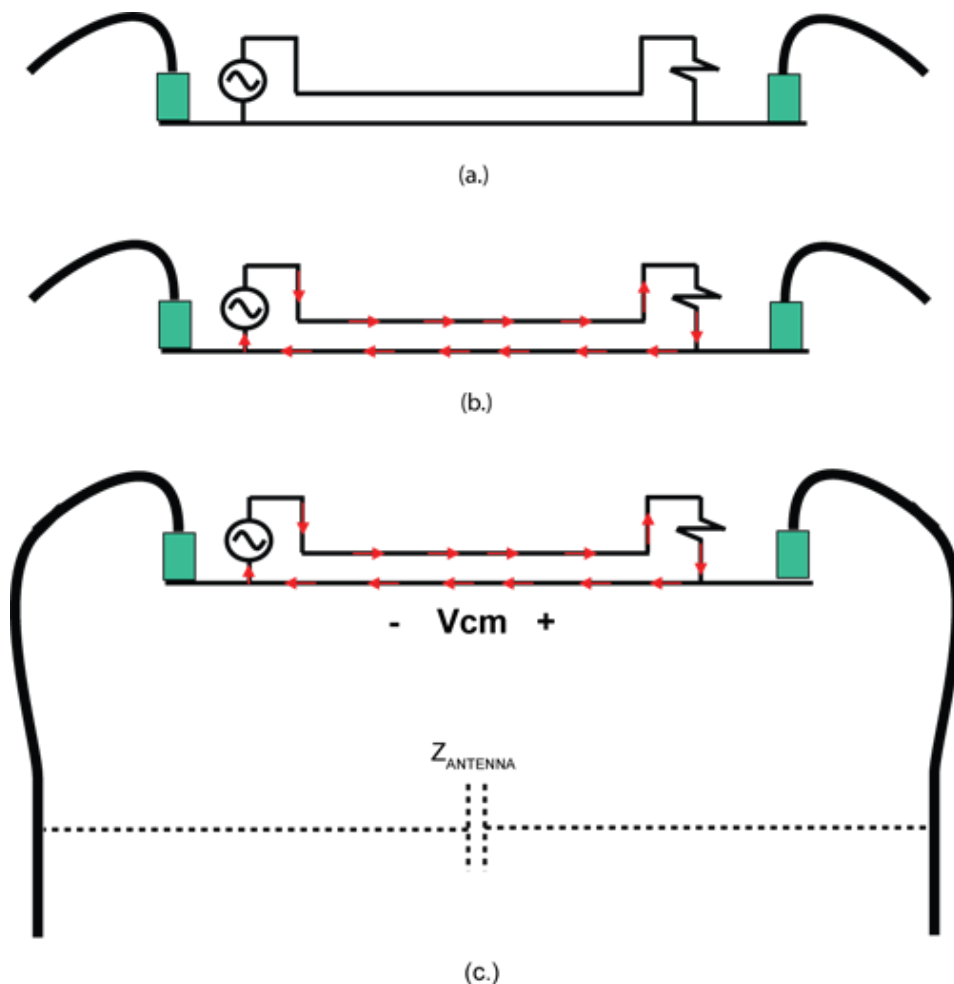


Figure 13: Example of current-driven coupling on a circuit board.

As indicated in Figure 13(b), the "ground" plane in this design does carry signal currents. In fact, the current flowing in the plane generates a magnetic flux that wraps around the plane. If we view the two cables as parts of an antenna and represent the antenna current path by an antenna impedance, illustrated in Figure 13(c), it becomes apparent that the currents flowing in the microstrip trace circuit induce a voltage across the plane that drives one cable relative to the other.

While it is true that the voltages induced across the plane are generally a few orders of magnitude lower than the signal voltages, a few millivolts of noise on an efficient antenna is sufficient to exceed FCC and CISPR radiated emissions requirements. In fact, when high-speed digital components are located between connectors on a board in an unshielded product, it is very difficult to meet radiated emissions requirements. On the other hand when two connectors are located next to each other, it is unlikely that magnetic fields will induce enough voltage between them to cause a problem.

## Direct Coupling to I/O

Although, strictly speaking, it is not an independent coupling mechanism, a common problem that occurs with printed circuit board layouts is coupling from noise sources directly to traces capable of carrying that noise off the board. An example of this is illustrated in Figure 14. A moderately high-speed trace is routed alongside another trace that attaches to a connector. Voltages and/or currents coupled from one trace to the other (via electric or magnetic fields) can be propagated down the I/O trace and off the board. In the example shown in the figure, the two antenna parts could either be the I/O cable driven relative to the board or one wire in the I/O cable driven relative to the other.

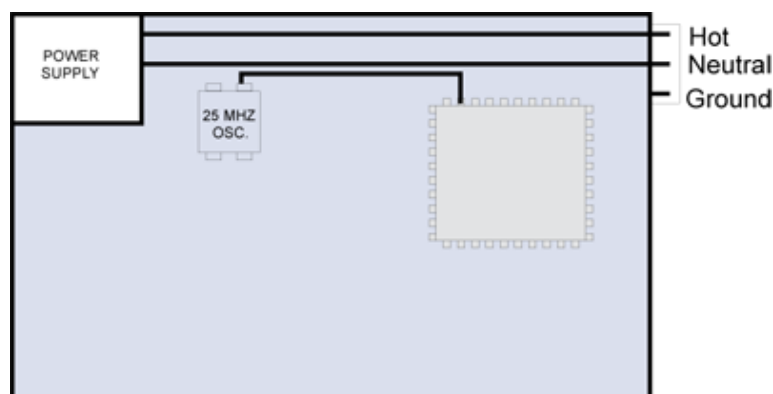


Figure 14: A possible coupling problem.

You might think that this is a rare problem, because it is fairly obvious once you see it. However, on a board with hundreds or thousands of traces laid out by an autorouter, this situation arises more often than it should. If your autorouter can't check for I/O traces that are routed in the vicinity of high-speed traces, then it should be done manually. The same also applies to I/O traces routed in the vicinity of traces connected to vulnerable inputs, since the easiest way for radiated noise to get onto a board is through the I/O.

## Printed Circuit Board Design Guidelines

As indicated earlier in these notes, many board designers employ a list of guidelines to help place components and route traces. Now that we know a little more about noise sources, antennas and coupling mechanisms on printed circuit boards, we can take a closer look at some of these design guidelines and understand why and when they are important. Below is a list of 16 EMC design guidelines for printed circuit boards along with a short justification for each.

*1. The lengths of traces carrying high-speed digital signals or clocks should be minimized.*

High-speed digital signals and clocks are often the strongest noise sources. The longer these traces are, the more opportunities there will be to couple energy away from these traces. Remember also, that loop area is generally more important than trace length. Make sure that there is a good high-frequency current return path very near each trace.

*2. The lengths of traces attached directly to connectors (I/O traces) should be minimized.*

Traces attached directly to connectors are likely paths for energy to be coupled on or off the board.

*3. Signals with high-frequency content should not be routed beneath components used for board I/O.*

Traces routed under a component can capacitively or inductively couple energy to that component.

*4. All connectors should be located on one edge or on one corner of a board.*

Connectors represent the most efficient antenna parts in most designs. Locating them on the same edge of the board makes it much easier to control the common-mode voltage that may drive one connector relative to another.

*5. No high-speed circuitry should be located between I/O connectors.*

Even if two connectors are on the same edge of the board, high-speed circuitry located between them can induce enough common-mode voltage to drive one connector relative to the other resulting in significant radiated emissions.

*6. Critical signal or clock traces should be buried between power/ground planes.*

Routing a trace on a layer between two solid planes does an excellent job of containing the fields from these traces and prevents unwanted coupling.

*7. Select active digital components that have maximum acceptable off-chip transition times.*

If the transition times of a digital waveform are faster than they need to be, the power in the upper harmonics can be much higher than necessary. If the transition times of the logic employed are faster than they need to be, they can usually be slowed using series resistors or ferrites.

*8. All off-board communication from a single device should be routed through the same connector.*

Many components (especially large VLSI devices) generate a significant amount of common-mode noise between different I/O pins. If one of these devices is connected to more than one connector, this common-mode noise will potentially drive a good antenna. (The device will also be more susceptible to radiated noise brought in on this antenna. )

*9. High-speed (or susceptible) traces should be routed at least 2X from the board edge, where X is the distance between the trace and its return current path.*

The electric and magnetic field lines associated with traces very near the edge of a board are less well contained. Crosstalk and coupling to and from antennas tends to be greater from these traces.

*10. Differential signal trace pairs should be routed together and maintain the same distance from any solid planes.*

Differential signals are less susceptible to noise and less likely to generate radiated emissions if they are balanced (i.e. they have the same length and maintain the same impedance relative to other conductors).

*11. All power (e.g. voltage) planes that are referenced to the same power return (e.g. ground) plane, should be routed on the same layer.*

If, for example, a board employs three voltages 3.3 volts, 3.3 volts analog and 1.0 volt; then it is generally desirable to minimize the high-frequency coupling between these planes. Putting the voltage planes on the same layer will ensure that there is no overlap. It will also help to promote an efficient layout, since the active devices are unlikely to require two different voltages at any one position on the board.

*12. The separation between any two power planes on a given layer should be at least 3 mm.*

If two planes get too close to each other on the same layer, significant high-frequency coupling may occur. Under adverse conditions, arcing or shorts may also be a problem if the planes are too closely spaced.

*13. On a board with power and ground planes, no traces should be used to connect to power or ground. Connections should be made using a via adjacent to the power or ground pad of the component.*

Traces on a connection to a plane located on a different layer take up space and add inductance to the connection. If high-frequency impedance is an issue (as it is with power bus decoupling connections), this inductance can significantly degrade the performance of the connection.

*14. If the design has more than one ground plane layer, then any connection to ground at a given position should be made to all of the ground layers at that position.*

The overall guiding principle here is that high-frequency currents will take the most beneficial (lowest inductance) path if allowed to. Don't try to direct the flow of these currents by only connecting to specific planes.

*15. There should be no gaps or slots in the ground plane.*

It's usually best to have a solid ground (signal return) plane and a layer devoted to this plane. Any additional power or signal current returns that must be DC isolated from the ground plane should be routed on layers other than the layer devoted to the ground plane.

*16. All power or ground conductors on the board that make contact with (or couple to) the chassis, cables or other good "antenna parts" should be bonded together at high frequencies.*

Unanticipated voltages between different conductors both nominally called "ground" are a primary source of radiated emission and susceptibility problems.

In addition to the 16 guidelines above, board designers often employ guidelines that are specific to their industry. For example, "Clock generation circuits employing phase-locked loops should have their own isolated power derived from the board's power through a #1234 ferrite bead. " These guidelines based on experience can be invaluable to the knowledgeable board designer. However, these same guidelines applied to other designs with no concept of where they came from or why they work can result in wasted effort and non-functional boards. It is very important to understand the basic physics behind each and every guideline being applied.

It is also important to identify the potential noise sources, antennas and coupling paths with every single design you evaluate. The best design won't be the one that complies with the most guidelines. The best design is the one that meets all of the specifications with the lowest cost and highest reliability.

## Putting it All Together

So we have a list of design guidelines and a basic understanding of why and when they are important. Let's try applying them to the quiz question presented earlier that asked which of the board layouts in Figure 2 is the best.

Hopefully, you can quickly eliminate option (b), the design with a trace crossing over a gap in the return plane. Option (a) employs the shortest trace and therefore is the best option provided that the gap in the ground plane is truly unnecessary. If there is a low-frequency common-impedance coupling problem that makes the gap unavoidable, then option (c) is nearly as good as option (a) in terms of the routing of that one trace. Remember that the length of a microstrip signal trace is not nearly as important as its overall loop area.

## Example 1: A Simple One-Layer Board Layout

Harvey invents a device that keeps a record of the telephone calls made from his phone. The design is relatively simple and is shown in Figure 15. However, when it is hooked up to the phone line, radiation from the device interferes with his TV reception.

*Redesign Harvey's board in order to reduce the radiated EMI. You may move components and/or add components, but you must use a single-sided board.*

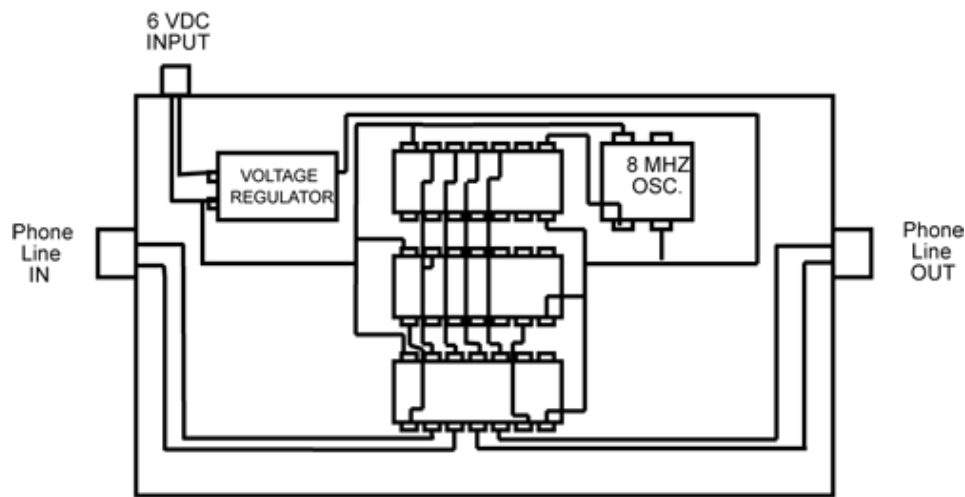


Figure 15: Harvey's Circuit.

We should begin by identifying the potential sources and antennas. Certainly, the 8-MHz clock signal is a potential source and so are the data lines. This device may also put significant noise on the power traces. Potential antenna parts are the three connectors. Nothing else on this board is large enough to be an efficient radiation source.

When we start to rearrange the components, we should try to put all of the antenna parts (i.e. the connectors) on one side of the board. We should also reorient the components to minimize the length of the traces. Finally, we should fill the empty space on the board with ground and make sure that each signal trace has a nearby return path.

One solution to this problem is shown in Figure 16. Try to trace the path of the 8-MHz signal current in the layout of Figure 15 compared to the same path in Figure 16. This current flows out the clock output pin of the oscillator, into the clock input pin of the upper IC, out the ground pin of the upper IC, and into the ground pin of the oscillator. This loop area is significantly smaller in the Figure 16 layout. Also note that no high-frequency current returns on the portion of the plane between any two connectors in the Figure 16 layout.

The design in Figure 15 is unlikely to meet a radiation emissions specification and therefore cannot be marketed or sold. The design in Figure 16 should meet virtually any country's radiated emissions specification without the need for any shielding or high-cost components. Note that we could have provided pads for mounting filter components on the phone lines if we felt that might be necessary.

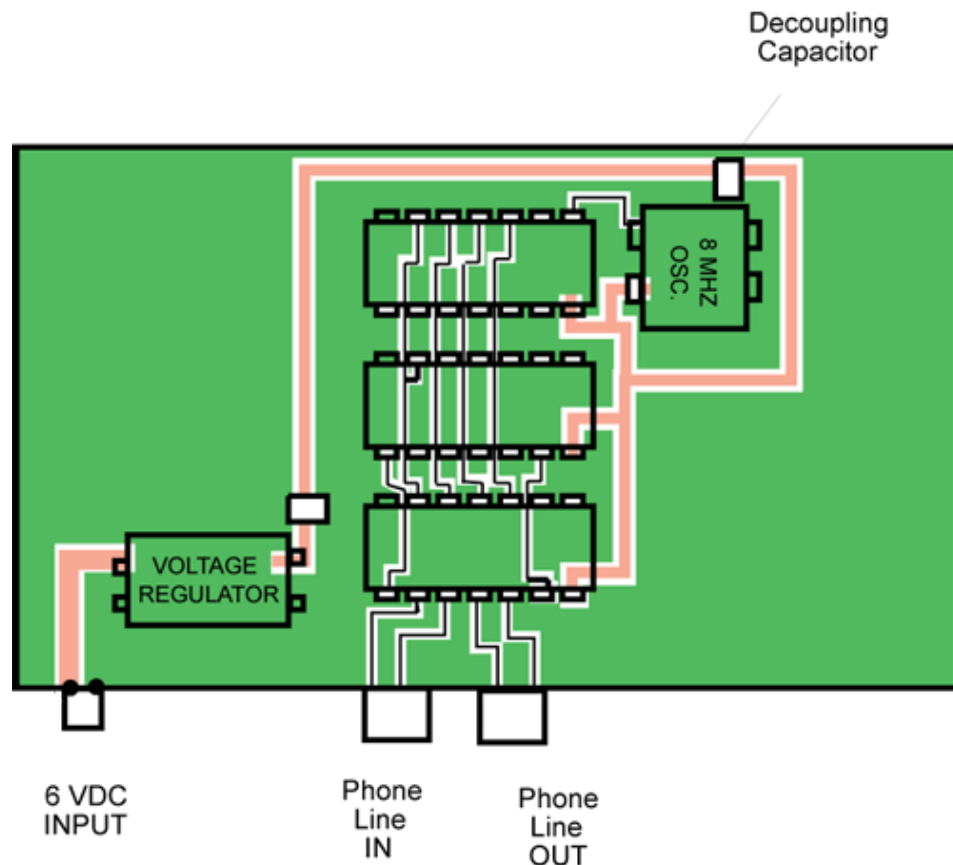


Figure 16: A better layout.

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