How to Select a MOSFET for Logic Circuits or Gate Design

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Field-effect transistors of the MOS (Metal-Oxide-Semiconductor) variety, or MOSFETs, are the semiconductor of choice for common high voltage and high current, voltage-driven switching applications. They have become much more popular than their current-driven predecessor, the BJT (Bipolar Junction Transistor). On the opposite end of switching spectrum, logic level MOSFETs prevail in the construction of processors and other small-signal devices due largely to their greater efficiency and high-speed switching capability.

The inner workings of the MOSFET are a clear departure from the BJT in terms of configuration but still use N and P junctions with enrichment or depletion channels where the conductivity occurs. For an explanation of the construction and operation of MOSFETs in general, review Digi-Key Electronics' article on the eewiki.

There are many microcontroller breadboard or PCB projects out there that specify TTL logic using BJT transistors such as the popular 2N3904 (NPN) or 2N3906 (PNP). They indeed perform nicely with or without prebiasing the base but are less efficient and in some cases have a slower response time than their CMOS counterparts.

Whether using 3.3 V or 5 V logic, there are threshold values between these voltages and ground that determine what is logically high or low. There is also a need for a range of voltages between high and low that act as a buffer, often referred to as an "illegal" region, that ensures the tipping point between a solid high and a solid low is not too abrupt which could result in unpredictable output (Figure 1).

Parameters to consider when selecting a logic level N-channel MOSFET

Gate-Source Threshold Voltage - Vgs(th)(min) and Vgs(th)(max): Gate voltage at or below the minimum threshold value turns the MOSFET off. Common minimum gate voltages for 5 V logic may fall between 0.5 V and 1 V. Gate voltages above the maximum threshold value turn the MOSFET on. Gate threshold voltages between the minimum and maximum could turn the MOSFET on or off and must be avoided. Notice how the minimum and maximum values roughly coincide with the illegal region in Figure 1.

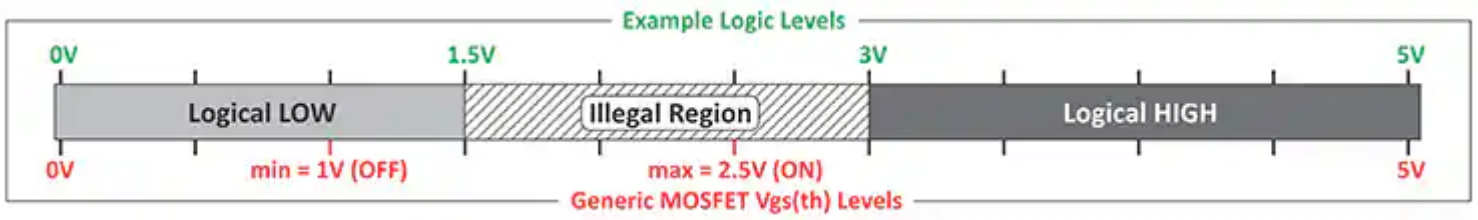

Figure 1

Drain-Source ON Resistance - Rds(on): When turned on, there is resistance between the drain and source that decreases as the gate-source voltage or Vgs increases. Choose a MOSFET whose lowest Rds(on) values occur at or near the ideal logic high voltage value and do not decrease substantially with higher Vgs values. See Figure 2.

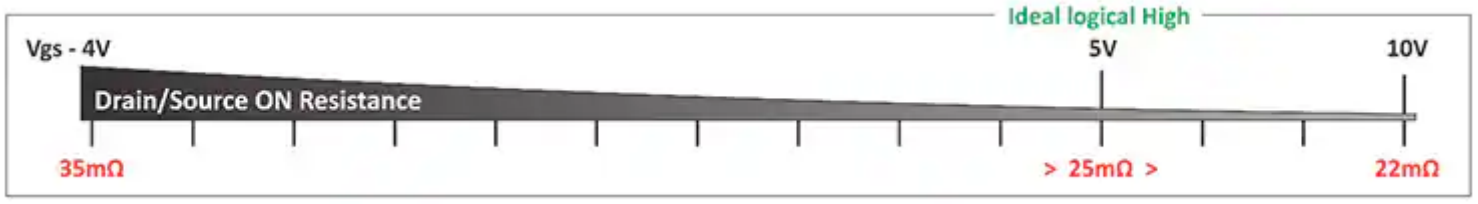

Figure 2

Example: According to its datasheet, an Infineon IRLZ44 MOSFET has 25 mOhms of drain-source resistance at 5 V, 35 mOhms at 4 V and 22 mOhms at 10 V. At 5 V, its Rds(on) value is only 3 mOhms higher than the value at 10 V but is 10 mOhms lower than the Rds(on) value at 4 V making it a good choice with respect to Rds(on).

Input Capacitance - Ciss: The combination of the gate, oxide layer, and the body connection of a MOSFET act as a small capacitor that begins charging when voltage is present at the gate. It takes time to charge which results in an ON-state delay. Choose a MOSFET with the lowest input capacitance possible to avoid long delays and to minimize in-rush current which can be very high initially but lessens as the capacitor charges. Ideally, the ON-state delay is extremely short but may create enough surge to damage an I/O pin that has limited current sourcing capacity.

A current limiting resistor between the pin and gate prevents excessive I/O pin current draw.

When using a MOSFET connected directly to a microcontroller output pin, the MOSFET gate should be pulled either high or low as needed using an external resistor to prevent floating gate logic and unwanted output from the MOSFET during MCU startups and resets.

The above parameters are a basic start to selecting a MOSFET for logic circuits or gate designs that may be fine-tuned with additional consideration for heat dissipation and other performance parameters. Don’t be afraid to give MOSFETs a try in your next project design.

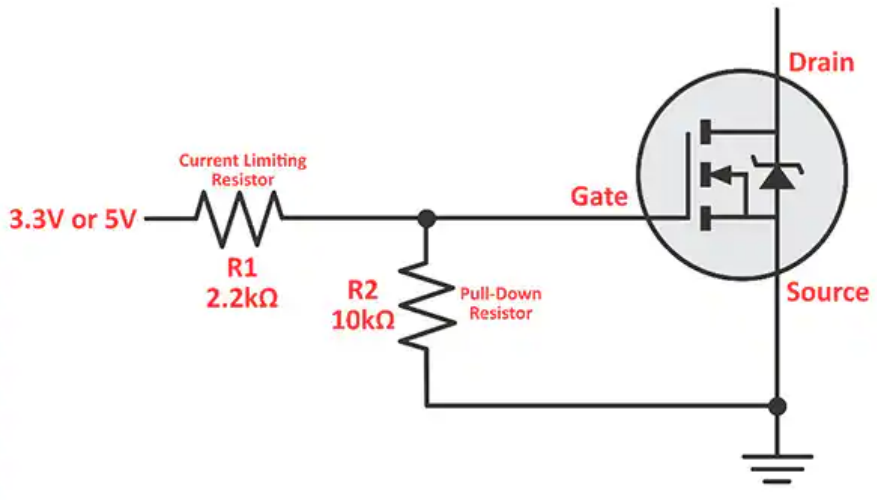

Figure 3