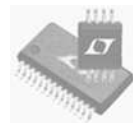


# LTspice IV

## Intermediate Lab Class Volume 3

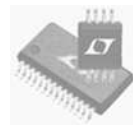
***Presented by:***  
***Mats Hellberg***  
*Linear Technology FAE*

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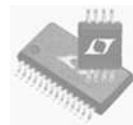


# Topics

1. *Creating a Schematic Symbol*
2. *Gain & Phase Analysis*
3. *Modeling MOSFETs*
4. *Modeling Coil Saturation*



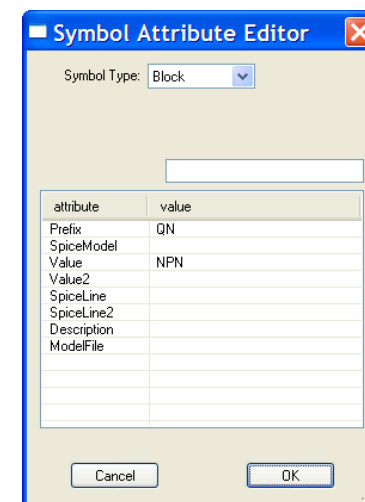
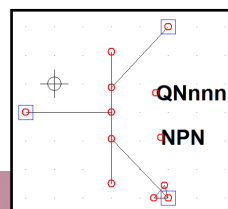
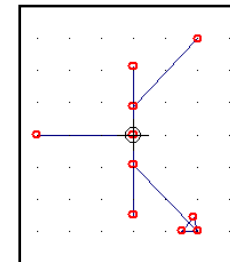
# Creating a Schematic Symbol



# Creating a Schematic Symbol

## Creating a NPN Transistor Schematic Symbol

1. Open up LTspice
2. File pull down menu ---> New Symbol
3. Draw pull down menu ---> Line. Draft an NPN symbol.
4. Edit pull down menu ---> Add Pin/Port. These are the actual electrical connections for B (base), C (collector), E (emitter). Netlist order for the pins: C = 1, B = 2, E = 3.
5. Edit pull down menu ---> Attributes ---> Edit Attributes (to add attributes). See the screen shot here ----->
6. Edit pull down menu ---> Attributes ---> Attribute Window (for attribute visibility) to make QN and NPN visible for the symbol





# Creating a Schematic Symbol

*Creating a NPN Transistor Schematic Symbol (continued.....)*

- 7. Save the schematic symbol as “My\_NPN.asy” in the same folder as the simulation file titled “NPN Schematic Symbol Import.asc”**
- 8. Open up the simulation file titled “NPN Schematic Symbol Import.asc” and follow the instructions in the simulation file.**



# Gain & Phase Analysis

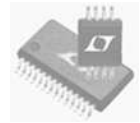
**How Do I Do Stability Analysis Of Switching Power Supplies In LTspice?**



# LTC3412A Example

- ❖ 5 Vin to 2.5 Vout @ 2.0 A
- ❖ DC652A Demoboard

# LTC3412A Example



## Simulation Command

Set simulation time to be as long as one period of the lowest frequency analyzed in the .step command plus the time to steady state.

Save data only after steady state is reached.

Limit maximum step size for proper measurement.

`.tran 0 11m 1m 0.5u startup`  
Must limit maximum step size for proper gain/phase to 0.5us in Simulation Command.

## .Step Directive

Choose Frequency Range.

Choose points/Decade  
Avoid too many points

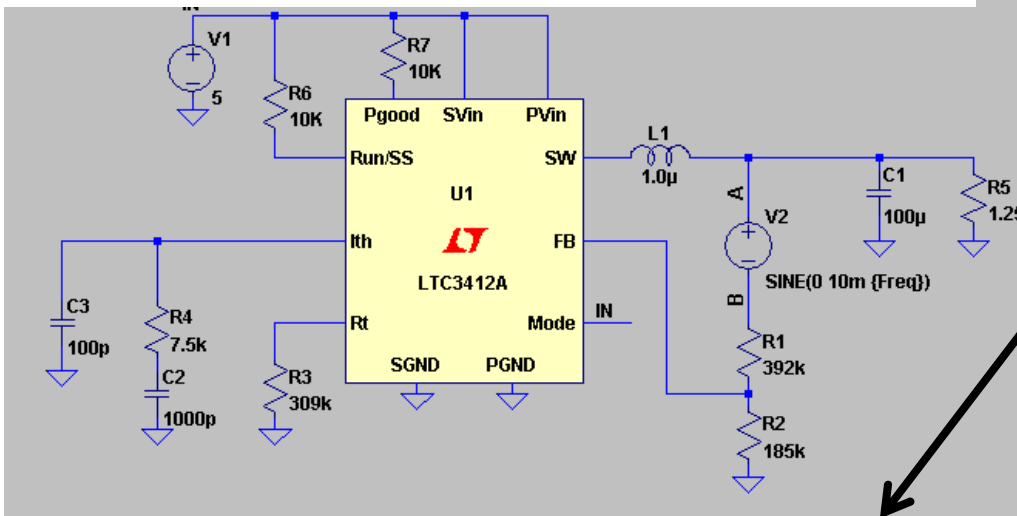
`.step dec param Freq 100 1Meg 3`

`.save V(a) V(b)`

```
.option plotwinsize=0 numdgt=15
.measure Aavg avg V(a)
.measure Bavg avg V(b)
.measure Are avg (V(a)-Aavg)*cos(360*time*Freq)
.measure Aim avg -(V(a)-Aavg)*sin(360*time*Freq)
.measure Bre avg (V(b)-Bavg)*cos(360*time*Freq)
.measure Bim avg -(V(b)-Bavg)*sin(360*time*Freq)
.measure GainMag param 20*log10(hypot(Are,Aim) / hypot(Bre,Bim))
.measure GainPhi param mod(atan2(Aim, Are) - atan2(Bim, Bre)+180,360)-180
```

## .Save Directive

Limited data saved.  
Helps with Memory.

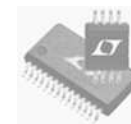




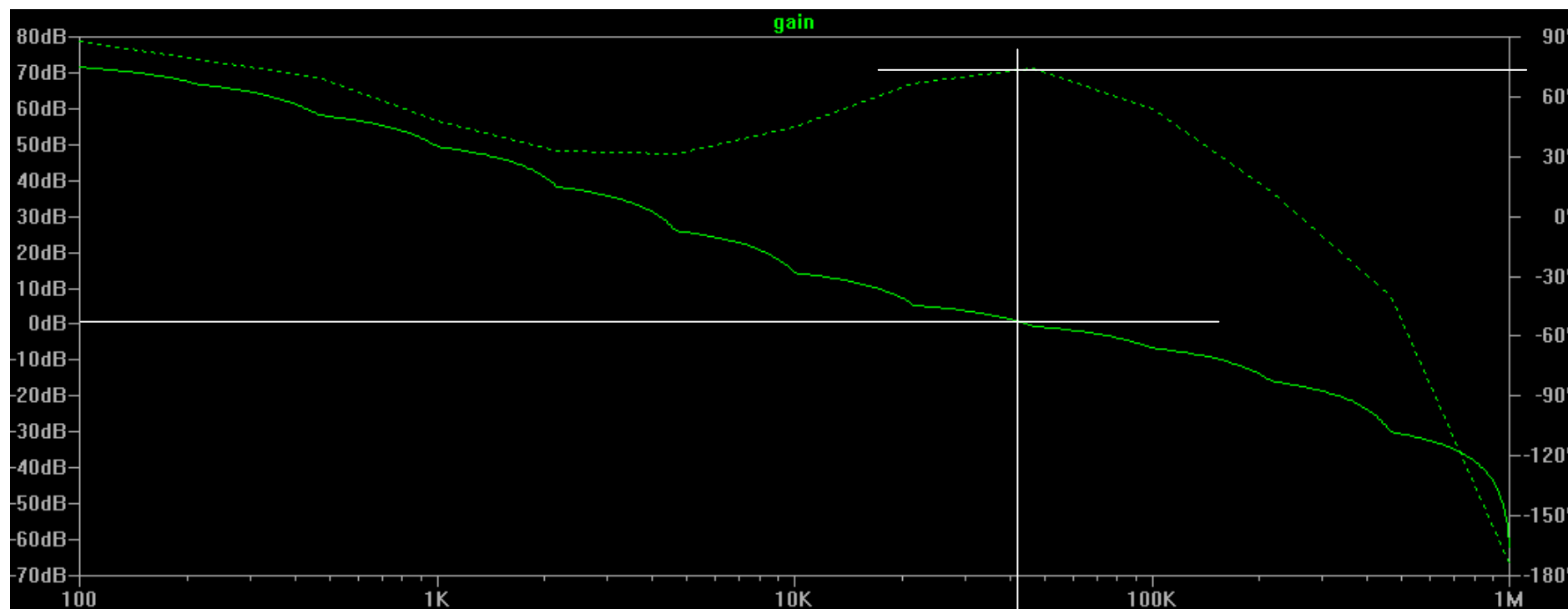


# Run Simulation, Then.....

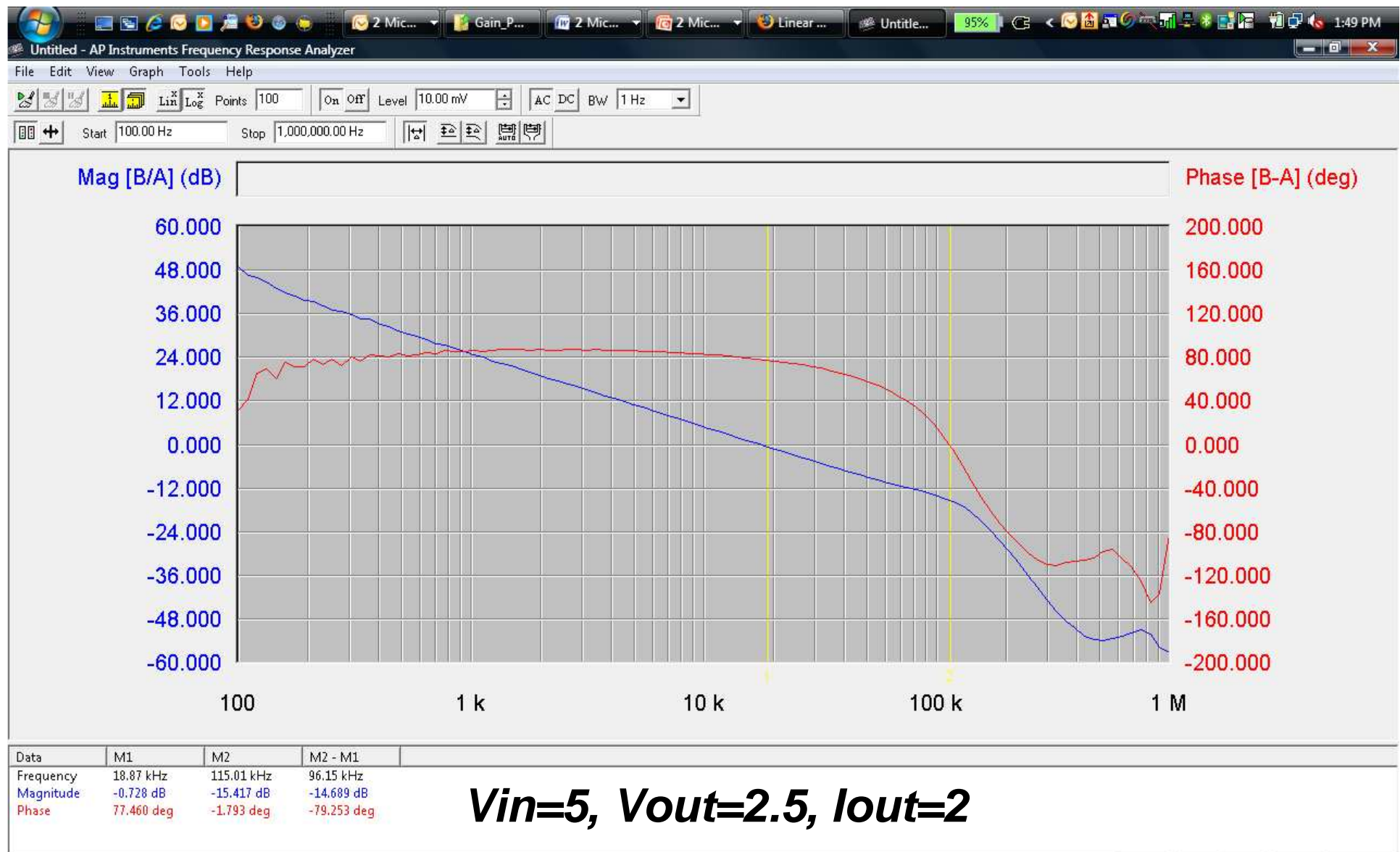
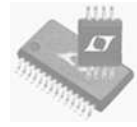
- After simulation is complete, from the "View" menu, select 'Spice Error Log'
  
- Right click anywhere in new window
  - Select 'Plot .step'ed .meas data'
  - Select 'Yes' in the next dialog box
  
- Right click anywhere in next window
  - Select 'Add Trace'
  - Select 'gain' and press 'OK'



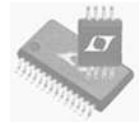
# Simulation Results – Long Run 30 Minute Run Time



# Actual Measured Data



# Simulation Speed Up Tips



## Simulation Command

If frequency range in .step command is narrowed, then the total simulation time can be reduced to one period of the lowest frequency plus the time it takes to get to steady state.

`.tran 0 11m 1m 0.5u startup`  
Must limit maximum step size for proper gain/phase to 0.5us in Simulation Command.

## .Step Directive

Choose Narrow Frequency Range.

```
.step dec param Freq 100 1Meg 3
.save V(a) V(b)

.option plotwinsize=0 numdgt=15
.measure Aavg avg V(a)
.measure Bavg avg V(b)
.measure Are avg (V(a)-Aavg)*cos(360*time*Freq)
.measure Aim avg -(V(a)-Aavg)*sin(360*time*Freq)
.measure Bre avg (V(b)-Bavg)*cos(360*time*Freq)
.measure Bim avg -(V(b)-Bavg)*sin(360*time*Freq)
.measure GainMag param 20*log10(hypot(Are,Aim) / hypot(Bre,Bim))
.measure GainPhi param mod(atan2(Aim,Are) - atan2(Bim,Bre)+180,360)-180
```

## Speed UP Summary

1. Change .tran directive to ".tran 0 2m 1m 0.5u startup
2. Change .step directive to ".step dec param Freq 1k 1Meg 3

The frequency of interest is changed from 100-1Meg Hz to 1K-1Meg Hz



```

.step dec param Freq 1k 1Meg 3

.save V(a) V(b) V(c) V(d) V(e) V(f)

.option plotwinsize=0 numdgt=15

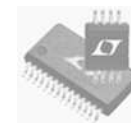
.measure Aavg avg V(a)
.measure Bavg avg V(b)
.measure Are avg (V(a)-Aavg)*cos(360*time*Freq)
.measure Aim avg -(V(a)-Aavg)*sin(360*time*Freq)
.measure Bre avg (V(b)-Bavg)*cos(360*time*Freq)
.measure Bim avg -(V(b)-Bavg)*sin(360*time*Freq)
.measure Gain1Mag param 20*log10(hypot(Are,Aim) / hypot(Bre,Bim))
.measure Gain1Phi param mod(atan2(Aim, Are) - atan2(Bim, Bre)+180,360)-180

.measure Cavg avg V(c)
.measure Davg avg V(d)
.measure Cre avg (V(c)-Cavg)*cos(360*time*Freq)
.measure Cim avg -(V(c)-Cavg)*sin(360*time*Freq)
.measure Dre avg (V(d)-Davg)*cos(360*time*Freq)
.measure Dim avg -(V(d)-Davg)*sin(360*time*Freq)
.measure Gain2Mag param 20*log10(hypot(Cre,Cim) / hypot(Dre,Dim))
.measure Gain2Phi param mod(atan2(Cim, Cre) - atan2(Dim, Dre)+180,360)-180

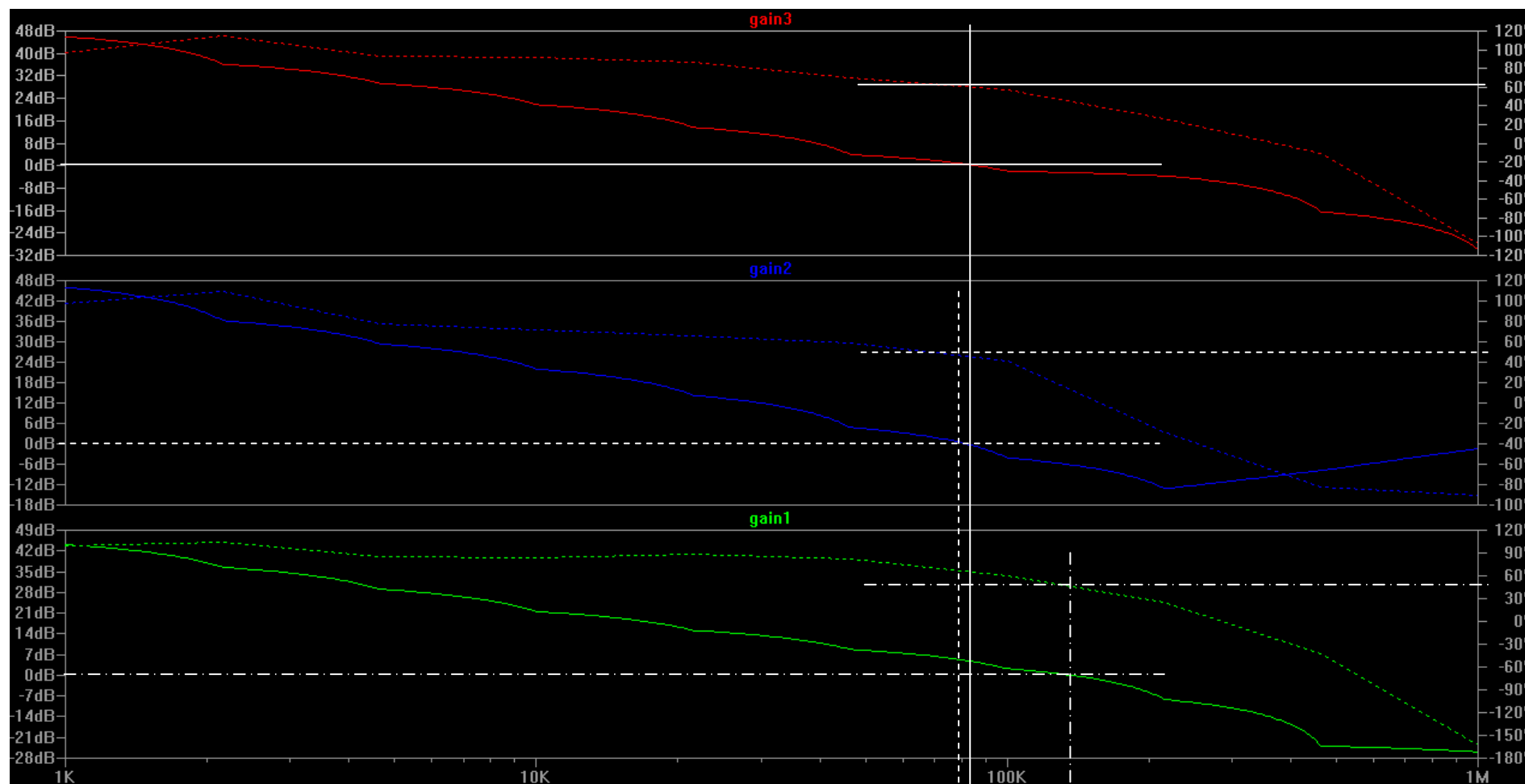
.measure Eavg avg V(e)
.measure Favg avg V(f)
.measure Ere avg (V(e)-Eavg)*cos(360*time*Freq)
.measure Eim avg -(V(e)-Eavg)*sin(360*time*Freq)
.measure Fre avg (V(f)-Favg)*cos(360*time*Freq)
.measure Fim avg -(V(f)-Favg)*sin(360*time*Freq)
.measure Gain3Mag param 20*log10(hypot(Ere,Eim) / hypot(Fre,Fim))
.measure Gain3Phi param mod(atan2(Eim, Ere) - atan2(Fim, Fre)+180,360)-180

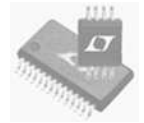
.tran 0 2m 1m 0.5u startup

```



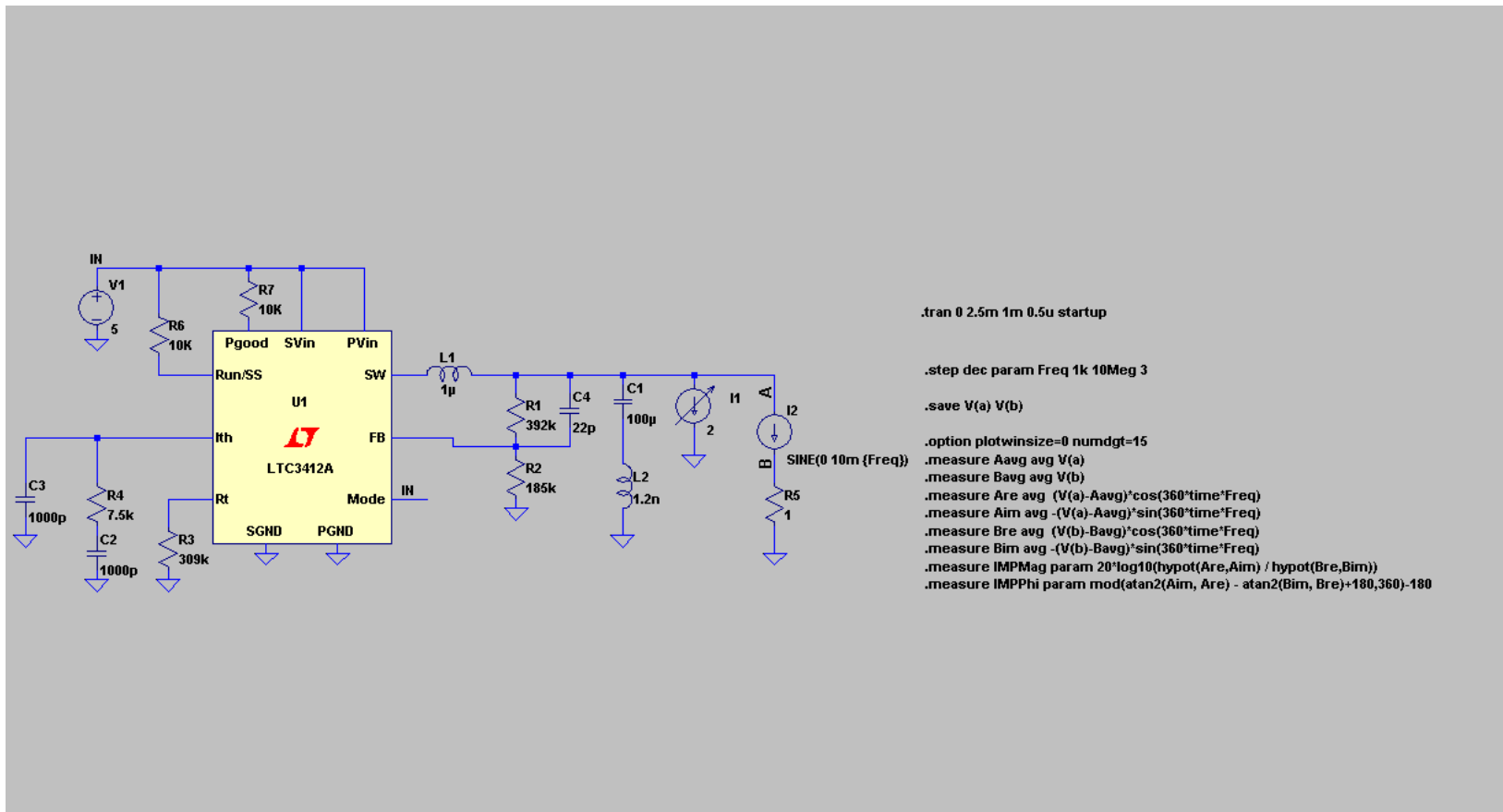
# Multi Output Converter Results



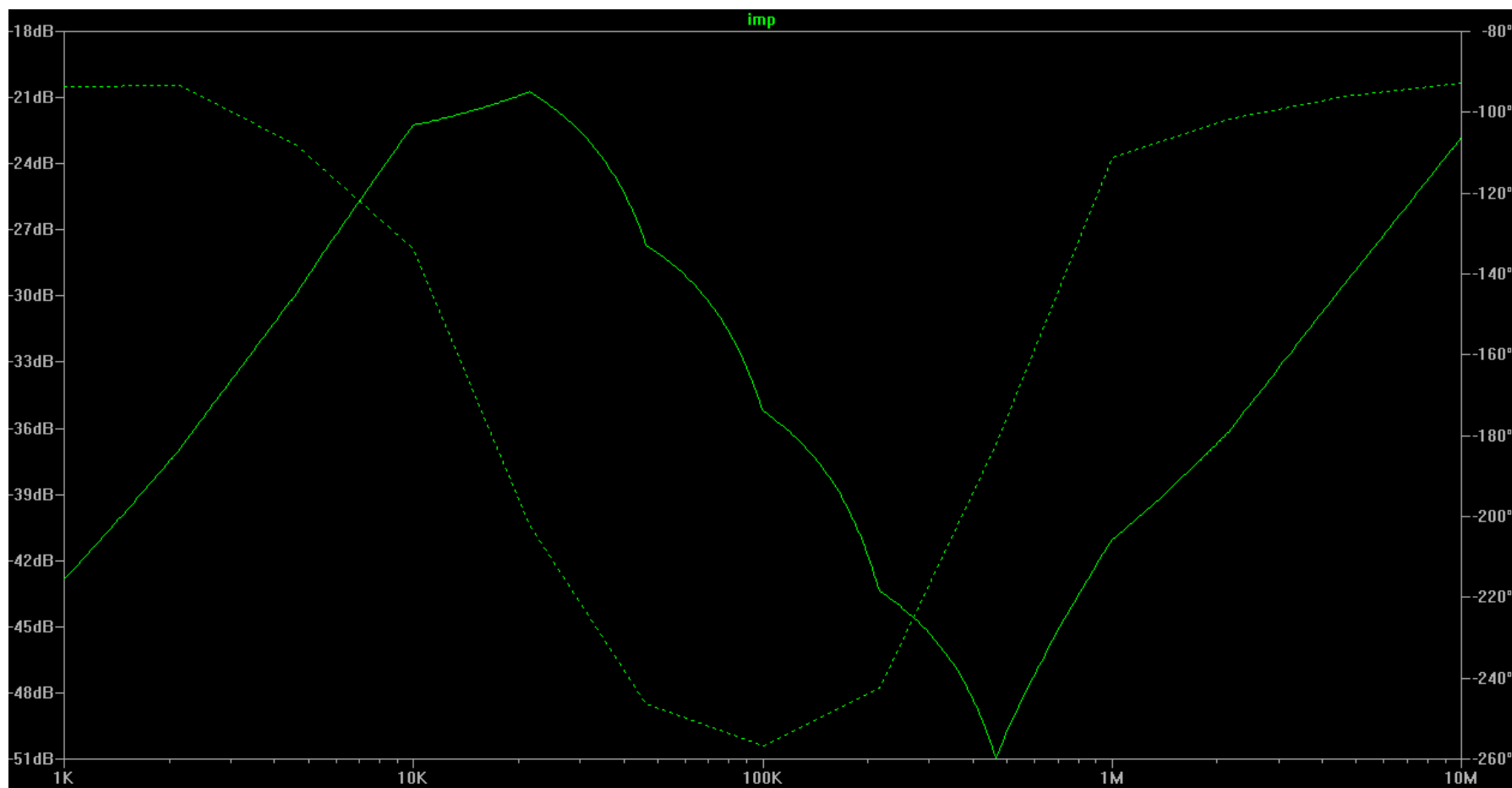
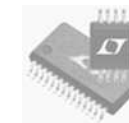


# Output Impepdance

*The same methodology can be applied to measure output impedance*



# Output Impedance Results







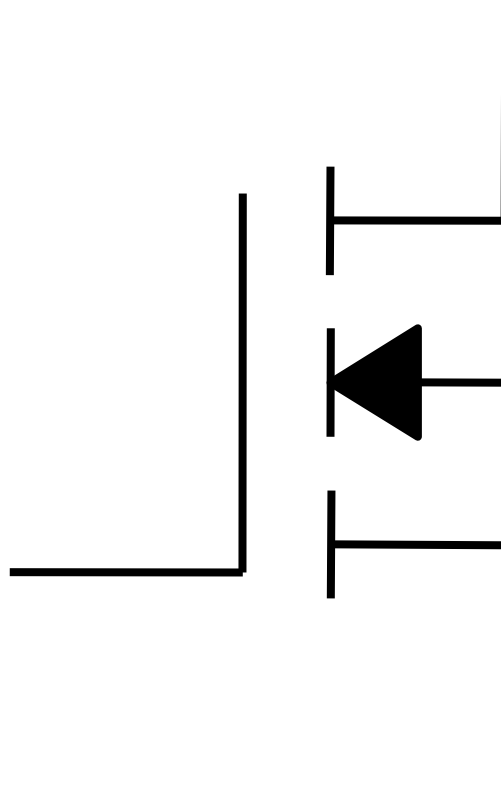
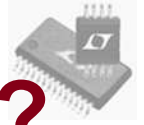
# Conclusion

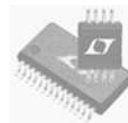
- 1. Possible to do small signal analysis of switching systems within Ltspice**
- 2. Not limited to one output**
- 3. Multiple inputs also possible. However, do not daisy chain DC-DC converters. The injected signal of the upstream converter interacts with the downstream converter.**
- 4. Multioutput supplies consume a lot of memory. Sample data should be over a limited frequency range.**



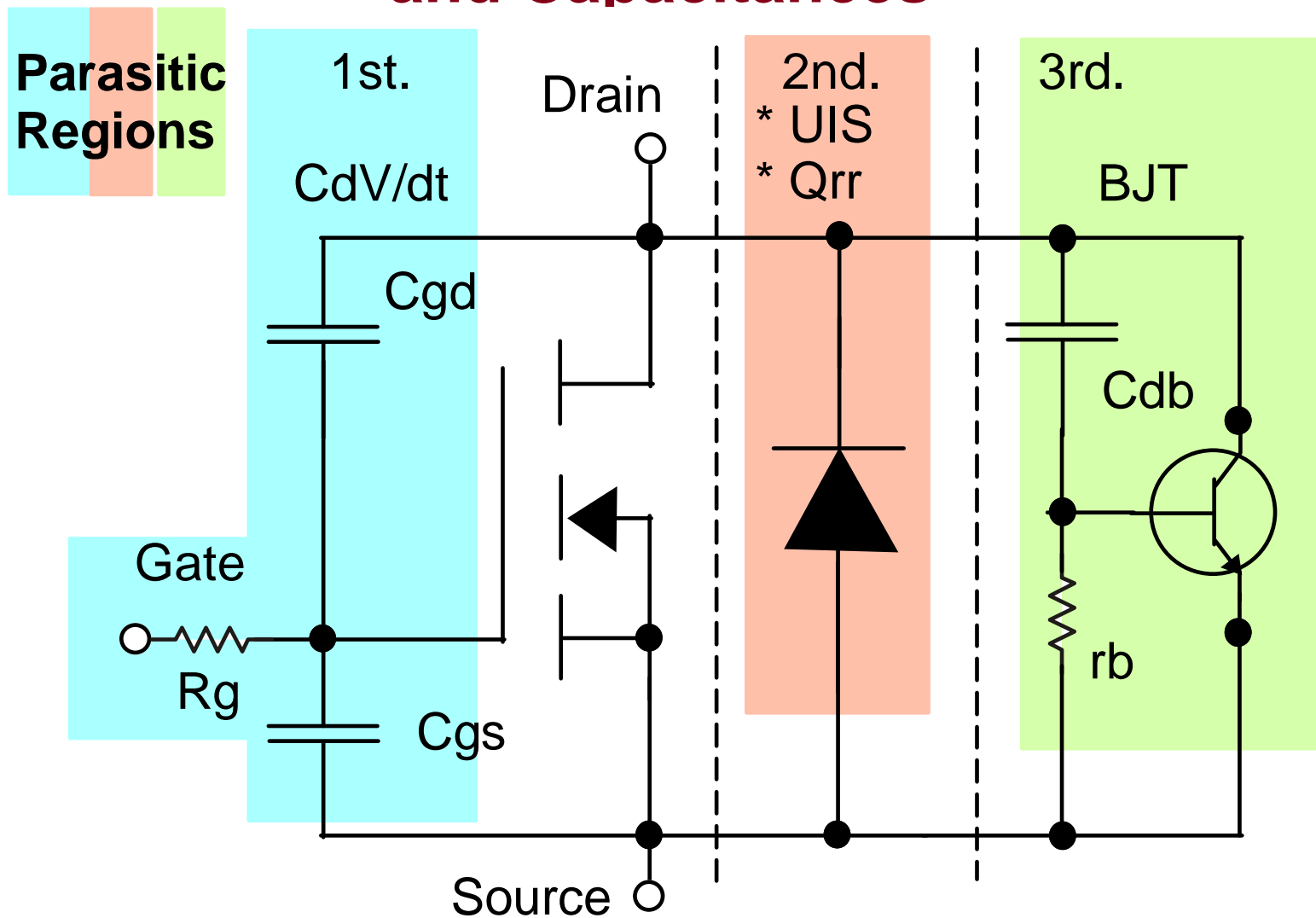
# Modeling MOSFETs

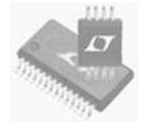
# A MOSFET is a Simple Device, Right?



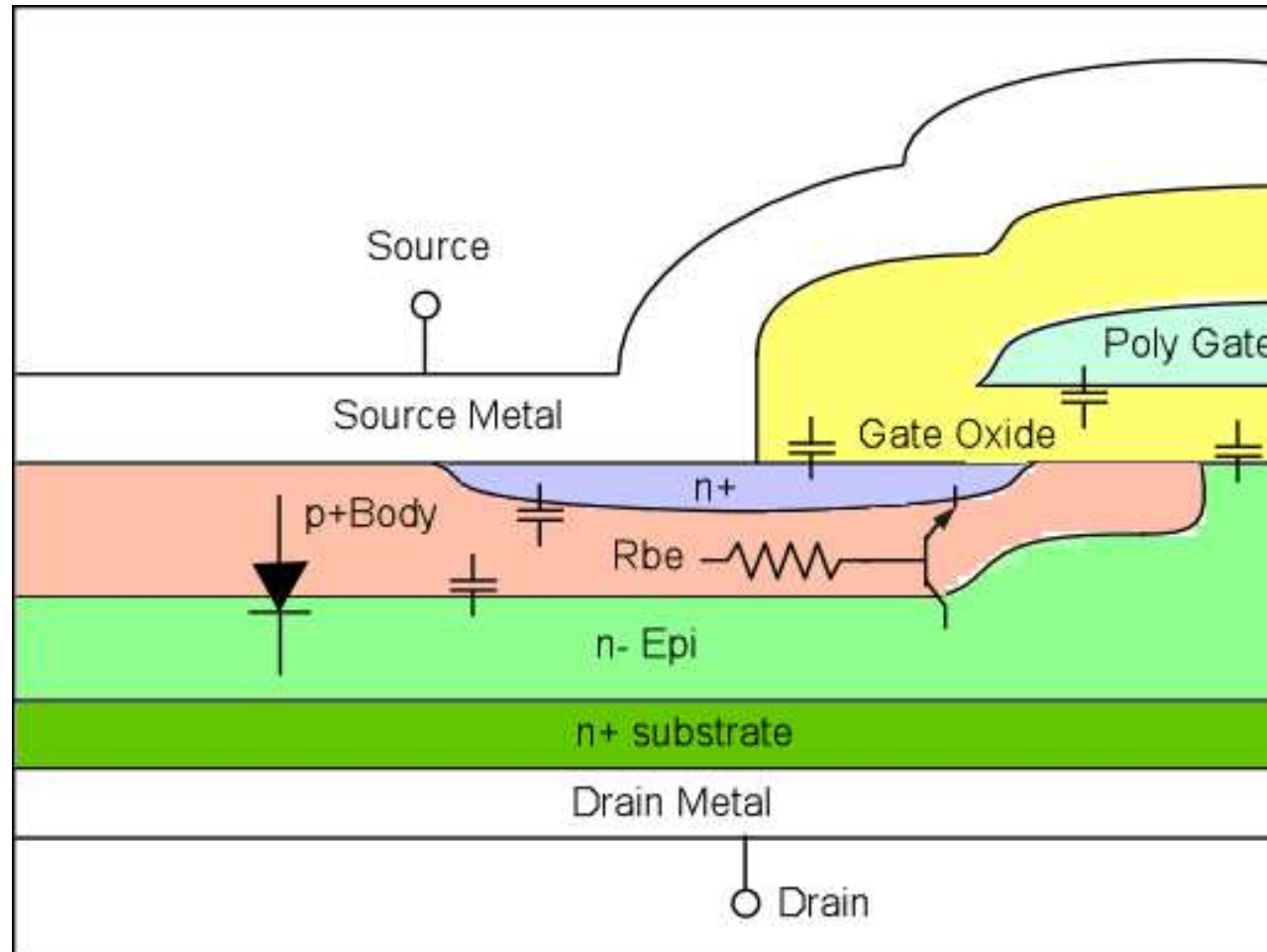


# Power MOSFET with Parasitic BJT, Diode and Capacitances





# Power MOSFET Cross Section

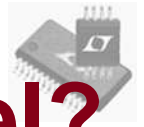




# LTspice VDMOS Model

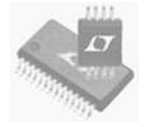
- ❖ Traditional Models are complex and slow, building elaborate subcircuits to duplicate behavior
- ❖ LTspice MOSFET Model is a new intrinsic model
  - ❖ Speed
  - ❖ Convergence
  - ❖ Simplicity
- ❖ DC Model is the same as a Level 1 Pspice model
- ❖ AC Model is based on:
  - ❖ Gate to source capacitance is constant
  - ❖ Gate to drain capacitance follows an empirical curve based on hyperbolic tangent whose min and max point is based on:
    - ❖ MOSFET off,  $V_{gd}$  is negative,  $C_{gd}$  is at minimum
    - ❖ MOSFET on,  $V_{gd}$  is positive,  $C_{gd}$  is at maximum

***Search, “M. MOSFET” in LTspice help section for further details***



# What do I need to make my own model?

- ❖ Datasheet of MOSFET
- ❖ Pspice model file

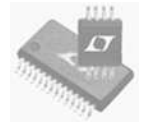


# Explanation of Terms

- ❖  $R_g$  – Gate ohmic resistance
- ❖  $R_d$  – Drain ohmic resistance.
- ❖  $R_s$  – Source ohmic resistance.
- ❖  $V_{to}$  – Zero-bias threshold voltage.
- ❖  $K_p$  – Transconductance.
- ❖  $C_{gdmax}$  – Maximum gate to drain capacitance.
- ❖  $C_{gdmin}$  – Minimum gate to drain capacitance.
- ❖  $C_{gs}$  – Gate to source capacitance.
- ❖  $C_{jo}$  – Parasitic diode capacitance.
- ❖  $I_s$  - Parasitic diode saturation current.
- ❖  $R_b$  – Body diode resistance.

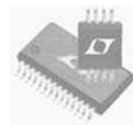
*Search, “M. MOSFET” in LTspice help section for further details*





# Example – IRF7456 MOSFET

- ❖ What is needed?
  - ❖ Spice Model provided by the vendor.
  - ❖ Datasheet provided by the vendor.
- ❖ Open LTspice. If you use Vista, you must run LTspice as the administrator.
- ❖ From the File tab, select 'Open'
- ❖ C: Program Files
  - ❖ LTC folder
    - ❖ LTspiceIV
      - ❖ Lib
        - ❖ CMP
        - ❖ Standard.mos



# Example – IRF7456 MOSFET

Go to Text File and Datasheet

***Warning!!!!***

***Do not trust the vendor spice model  
to be correct***



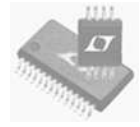
# Comments about the Spice Model

*All parameters should be in the Level 1 section*

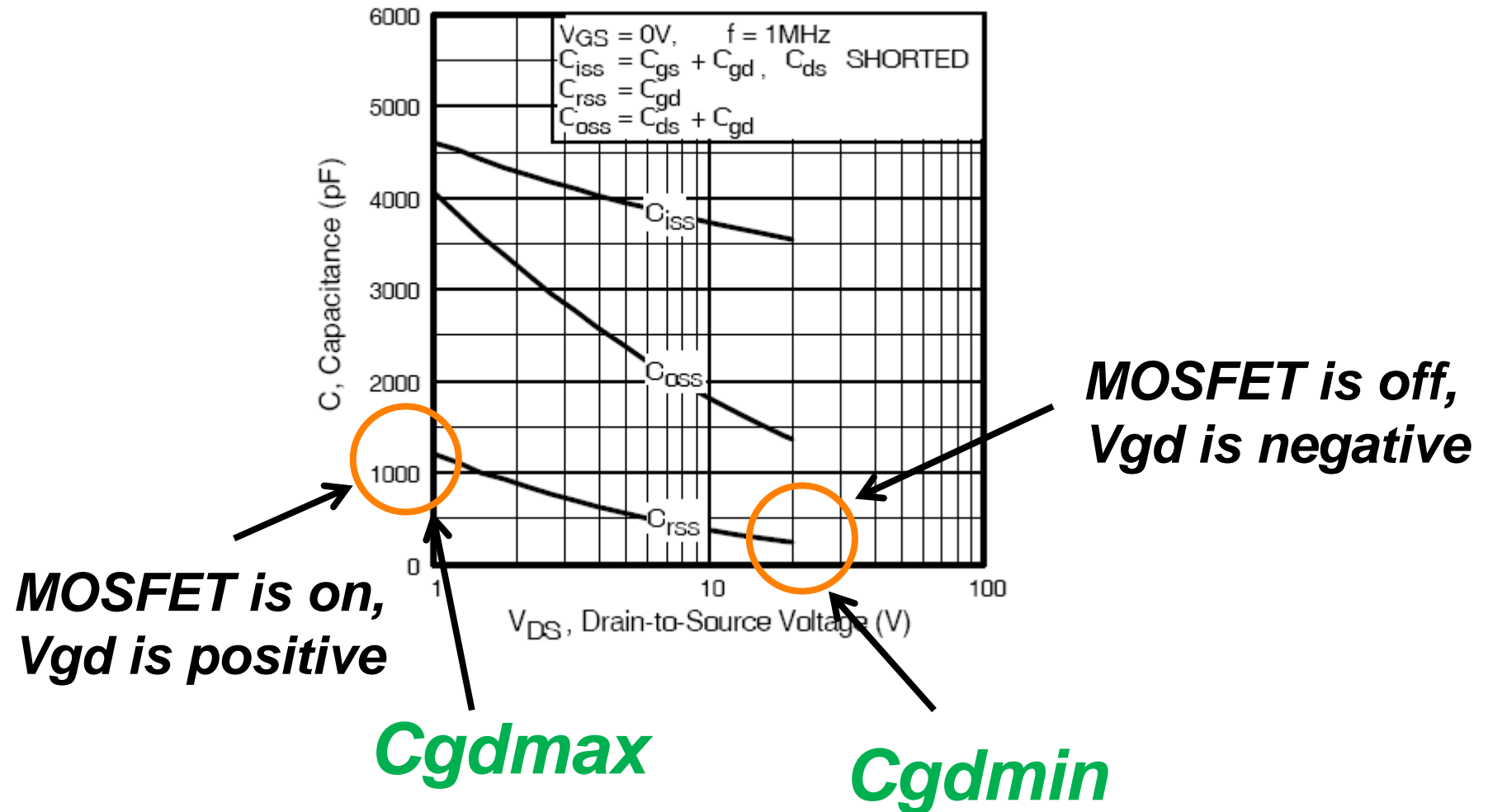
**Gate threshold  
and  
Gate capacitance  
do not match the  
datasheet**

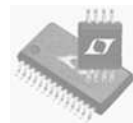
```
.MODEL M1 NMOS LEVEL=1 IS=1e-32
+VTO=2.07545 LAMBDA=0.0453657 KP=119.186
+CGSO=3.37108e-05 CGDO=1.97763e-09
RS 8 3 0.0001
D1 3 1 MD
.MODEL MD D IS=1.87521e-13 RS=0.013756 N=1.919559 BV=20
+IBV=0.00025 EG=1 XTI=1 TT=0
+CJO=3.98952e-09 VJ=0.635683 M=0.361988 FC=0.5
RDS 3 1 1e+06
RD 9 1 0.002047
RG 2 7 1.73819
D2 4 5 MD1
```

**Diode resistance is  
within the diode subcirc**



# IRF7456 Gate to Drain Capacitance





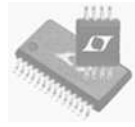
# IRF7456 Model

***Always compare  
spice model to  
datasheet.  
Sometimes the  
numbers in the  
spice model don't  
pass the 'common  
sense test'.***

Term	Value	Source
Rg	1.74	Spice Model
Rd	0.0001	Spice Model
Rs	0.0027	Spice Model
Vto	1.3	Data Sheet Electrical Table
Kp	119	Spice Model
Cgdmax	1200 e-12	Data Sheet Curve
Cgdmin	250 e-12	Data Sheet Curve
Cgs	3.37e-9	Data Sheet Electrical Table
Cjo	3.99e-9	Spice Model
Is	1.87e-13	Spice Model
Rb	0.013	Spice Model



# Add New Model Within LTSpice



```
LTSpice IV - [standard]
File Edit View Tools Window Help

.model1 HUFA76413DK8T UDMOS(Rg=3 Uto=2.2 Rd=22.4m Rs=16.8m Rb=28m Kp=50 Cgdmax=.6n Cgdmin=.1n Cgs=.6n Cjo=.2n Is=36p mfg=Fairchild Vds=60 Ron=56m Qg=18n)
.model1 IRF1302 UDMOS(Rg=3 Uto=4 Rd=1.6m Rs=1.2m Rb=2m Kp=50 Cgdmax=5n Cgdmin=1n Cgs=2n Cjo=1n Is=160p mfg=International_Rectifier Vds=20 Ron=4m Qg=80n)
.model1 IRF1312S UDMOS(Rg=3 Rd=4m Rs=3m Uto=5.25 Kp=70 Cgdmax=3.7n Cgdmin=.47n Cgs=6.2n Cjo=1.86n Is=186p Rb=5m mfg=International_Rectifier Vds=80 Ron=10m Qg=120n)
.model1 IRF1405 UDMOS(Rg=3 Uto=3.5 Rd=2m Rs=1.5m Rb=3m Kp=50 Cgdmax=5n Cgdmin=1n Cgs=4n Cjo=1.3n Is=100p mfg=International_Rectifier Vds=55 Ron=5m Qg=120n)
.model1 IRF1503S UDMOS(Rg=3 Uto=3.9 Rd=1.3m Rs=1m Rb=2m Kp=103.4 Cgdmax=3n Cgdmin=.9n Cgs=6n Cjo=1.5n Is=150p mfg=International_Rectifier Vds=30 Ron=3.3m Qg=120n)
.model1 IRF3717 UDMOS(Rg=3 Uto=2.45 Rd=1.8m Rs=1.3m Rb=2m Kp=100 Cgdmax=1.3n Cgdmin=.33n Cgs=2.2n Cjo=.66n Is=44p mfg=International_Rectifier Vds=20 Ron=4.4m Qg=120n)
.model1 IRF6607 UDMOS(Rg=3 Rd=1.5m Rs=1.1m Uto=2 lambda=.15 Kp=50 Cgdmax=2n Cgdmin=.5n Cgs=5.3n Cjo=1n Is=100p Rb=1.9m mfg=International_Rectifier Vds=30 Ron=2.7m Qg=120n)
.model1 IRF6609 UDMOS(Rg=3 Uto=2.6 Rd=.8m Rs=.6m Rb=1m Kp=106 Cgdmax=1.8n Cgdmin=.86n Cgs=5.1n Cjo=.92n Is=92p mfg=International_Rectifier Vds=20 Ron=2m Qg=120n)
.model1 IRF6618 UDMOS(Rg=3 Rd=1.1m Rs=.8m Uto=2.2 lambda=.05 Kp=50 Cgdmax=1.8n Cgdmin=.16n Cgs=4.5n Cjo=.92n Is=92p Rb=1.4m mfg=International_Rectifier Vds=20 Ron=2.7m Qg=120n)
.model1 IRF6620 UDMOS(Rg=3 Uto=2.5 Rd=1.1m Rs=.8m Rb=1m Kp=104.6 Cgdmax=1.5n Cgdmin=.6n Cgs=3n Cjo=.56n Is=56p mfg=International_Rectifier Vds=20 Ron=2.7m Qg=120n)
.model1 IRF6623 UDMOS(Rg=3 Uto=2.35 Rd=2.3m Rs=1.7m Rb=3m Kp=98.6 Cgdmax=.5n Cgdmin=.2n Cgs=1.4n Cjo=.22n Is=22p mfg=International_Rectifier Vds=20 Ron=5.7m Qg=120n)
.model1 IRF6635 UDMOS(Rg=3 Uto=1.8 Rd=.5m Rs=.1m Rb=1m Kp=45 lambda=.05 Cgdmax=3n Cgdmin=.6n Cgs=6n Cjo=1.5n Is=150p mfg=International_Rectifier Vds=30 Ron=1.8m Qg=120n)
.model1 IRF6691 UDMOS(Rg=3 Uto=2.5 Rd=.7m Rs=.5m Rb=1m Kp=106.4 Cgdmax=1.9n Cgdmin=.7n Cgs=6.1n Cjo=.94n Is=94p mfg=International_Rectifier Vds=20 Ron=1.8m Qg=120n)
.model1 IRF7201 UDMOS(Rg=3 Rs=12m Rd=5m Uto=2.64 Kp=26 Cgdmax=650p Cgdmin=135p Cgs=620p Cjo=620p a=1.5 Is=2.4p Rb=11m N=1.07 mfg=International_Rectifier Vds=20 Ron=1.8m Qg=120n)
.model1 IRF7204 UDMOS(pchan Rg=3 Rd=24m Rs=18m Uto=-1 Kp=15 Cgdmax=1n Cgdmin=.13n Cgs=1.7n Cjo=.5n Is=50p Rb=30m mfg=International_Rectifier Vds=-20 Ron=60m Qg=120n)
.model1 IRF7205 UDMOS(pchan Rg=3 Rd=28m Rs=21m Uto=-1 Kp=10 Cgdmax=1.1n Cgdmin=.14n Cgs=1.8n Cjo=.54n Is=54p Rb=35m mfg=International_Rectifier Vds=-30 Ron=70m Qg=120n)
.model1 IRF7207 UDMOS(pchan Rg=3 Rd=32m Rs=24m Uto=-1 Kp=8 Cgdmax=.6n Cgdmin=.08n Cgs=1n Cjo=.3n Is=30p Rb=40m mfg=International_Rectifier Vds=-20 Ron=80m Qg=120n)
.model1 IRF7210 UDMOS(pchan Rg=3 Rd=2m Rs=1.5m Uto=-1 Kp=100 Cgdmax=8.5n Cgdmin=1.06n Cgs=14.1n Cjo=4.24n Is=424p Rb=2.5m mfg=International_Rectifier Vds=-12 Ron=1.8m Qg=120n)
.model1 IRF7220 UDMOS(pchan Rg=3 Rd=4.8m Rs=3.6m Uto=-.75 Kp=86 Cgdmax=1.5n Cgdmin=4.25n Cgs=7n Cjo=1n Is=168p Rb=6m mfg=International_Rectifier Vds=-12 Ron=1.8m Qg=120n)
.model1 IRF7233 UDMOS(pchan Rg=3 Rd=8m Rs=6m Uto=-1 Kp=70 Cgdmax=2n Cgdmin=.25n Cgs=3.3n Cjo=.98n Is=98p Rb=10m mfg=International_Rectifier Vds=-12 Ron=20m Qg=120n)
.model1 IRF7303 UDMOS(Rg=3 Rs=30m Rd=10m Uto=2.3 Kp=15 Cgdmax=880p Cgdmin=10p Cgs=500p Cjo=500p a=1.5 Is=39p Rb=66m N=1.24 Vds=30 Ron=50m Qg=25n mfg=International_Rectifier Vds=30 Ron=13m Qg=120n)
.model1 IRF7335 UDMOS(Rg=3 Uto=1.9 Rd=5.2m Rs=3.9m Rb=7m Kp=84 Cgdmax=.7n Cgdmin=.2n Cgs=1.5n Cjo=.26n Is=26p mfg=International_Rectifier Vds=30 Ron=13m Qg=120n)
.model1 IRF7343M UDMOS(Rg=3 Rd=20m Rs=15m Uto=1 Kp=10 Cgdmax=1.4n Cgdmin=.18n Cgs=.8n Cjo=.72n Is=72p Rb=25m mfg=International_Rectifier Vds=55 Ron=50m Qg=30n)
.model1 IRF7343P UDMOS(pchan Rg=3 Rd=42m Rs=31m Uto=-1 Kp=1 Cgdmax=1.5n Cgdmin=.19n Cgs=.83n Cjo=.76n Is=76p Rb=52m mfg=International_Rectifier Vds=-55 Ron=1.8m Qg=120n)
.model1 IRF7401 UDMOS(Rg=3 Rd=8.8m Rs=6.6m Uto=2 Kp=66 Cgdmax=1.6n Cgdmin=.2n Cgs=2.7n Cjo=.8n Is=80p Rb=11m mfg=International_Rectifier Vds=20 Ron=22m Qg=40n)
.model1 IRF7403 UDMOS(Rg=3 Rd=8.8m Rs=6.6m Uto=2 Kp=66 Cgdmax=1.7n Cgdmin=.21n Cgs=2.8n Cjo=.84n Is=84p Rb=11m mfg=International_Rectifier Vds=30 Ron=22m Qg=40n)
.model1 IRF7404 UDMOS(pchan Rg=3 Rd=16m Rs=12m Uto=-1 Kp=30 Cgdmax=1.6n Cgdmin=.2n Cgs=2.7n Cjo=.8n Is=80p Rb=20m mfg=International_Rectifier Vds=-20 Ron=40n)
.model1 IRF7406 UDMOS(pchan Rg=3 Rd=18m Rs=13.5m Uto=-1 Kp=20 Cgdmax=1.4n Cgdmin=.18n Cgs=2.4n Cjo=.72n Is=72p Rb=22.5m mfg=International_Rectifier Vds=-30 Ron=40n)
.model1 IRF7413 UDMOS(Rg=3 Rd=4.4m Rs=3.3m Uto=2 Kp=88 Cgdmax=1.4n Cgdmin=.17n Cgs=2.3n Cjo=.68n Is=68p Rb=5.5m mfg=International_Rectifier Vds=30 Ron=11m Qg=120n)
.model1 IRF7413A UDMOS(Rg=3 Rd=5.4m Rs=4.1m Uto=2 Kp=83 Cgdmax=2.1n Cgdmin=.26n Cgs=3.5n Cjo=1.04n Is=104p Rb=6.8m mfg=International_Rectifier Vds=30 Ron=13.5m Qg=120n)
.model1 IRF7455 UDMOS(Rg=3 Rd=3m Rs=2.3m Uto=2 Kp=95 Cgdmax=1.5n Cgdmin=.19n Cgs=2.5n Cjo=.74n Is=74p Rb=3.8m mfg=International_Rectifier Vds=30 Ron=7.5m Qg=120n)
.model1 IRF7456 UDMOS(Rg=1.74 Rd=0.1m Rs=2.7m Uto=1.3 Kp=119 Cgdmax=1.2n Cgdmin=.25n Cgs=3.33n Cjo=3.99n Is=0.18p Rb=13m mfg=International_Rectifier Vds=20 Ron=1.8m Qg=120n)
.model1 IRF7468 UDMOS(Rg=3 Rd=6.4m Rs=4.8m Uto=1.8 Kp=40 Cgdmax=.9n Cgdmin=.12n Cgs=1.5n Cjo=.46n Is=46p Rb=8m mfg=International_Rectifier Vds=40 Ron=16m Qg=120n)
.model1 IRF7805 UDMOS(Rg=3 Rd=4.4m Rs=3.3m Uto=2 Kp=88 Cgdmax=1.2n Cgdmin=.16n Cgs=2.1n Cjo=.62n Is=62p Rb=5.5m mfg=International_Rectifier Vds=30 Ron=11m Qg=120n)
.model1 IRF7807 UDMOS(Rg=3 Rd=10m Rs=7.5m Uto=2 Kp=60 Cgdmax=.7n Cgdmin=.09n Cgs=1.1n Cjo=.34n Is=34p Rb=12.5m mfg=International_Rectifier Vds=30 Ron=25m Qg=120n)
.model1 IRF7809A UDMOS(Rg=3 Rd=3.4m Rs=2.6m Uto=2 Kp=93 Cgdmax=2.4n Cgdmin=.31n Cgs=4.1n Cjo=1.22n Is=122p Rb=4.3m mfg=International_Rectifier Vds=30 Ron=8.5m Qg=120n)
.model1 IRF7811 UDMOS(Rg=3 Rd=3.4m Rs=2.6m Uto=2 Kp=93 Cgdmax=.8n Cgdmin=.1n Cgs=1.3n Cjo=.38n Is=38p Rb=4.3m mfg=International_Rectifier Vds=30 Ron=8.5m Qg=120n)
.model1 IRF7811AU UDMOS(Rg=3 Rd=4.4m Rs=3.3m Uto=2 Kp=88 Cgdmax=.7n Cgdmin=.09n Cgs=1.1n Cjo=.34n Is=34p Rb=5.5m mfg=International_Rectifier Vds=30 Ron=11m Qg=120n)
.model1 IRF7822 UDMOS(Rg=3 Rd=2m Rs=1.5m Uto=2 Kp=100 Cgdmax=1.8n Cgdmin=.22n Cgs=2.9n Cjo=.88n Is=88p Rb=2.5m mfg=International_Rectifier Vds=30 Ron=5m Qg=120n)
.model1 IRF7831 UDMOS(Rg=3 Uto=2.35 Rd=1.4m Rs=1.1m Rb=2m Kp=102.8 Cgdmax=1.6n Cgdmin=.16n Cgs=2.7n Cjo=.8n Is=80p mfg=International_Rectifier Vds=30 Ron=3.6m Qg=120n)
.model1 IRF7832 UDMOS(Rg=3 Rd=1.6m Rs=1.2m Uto=2.2 Kp=112 Cgdmax=2.4n Cgdmin=.17n Cgs=4.3n Cjo=.68n Is=68p Rb=2m mfg=International_Rectifier Vds=30 Ron=4m Qg=120n)
.model1 IRF9410 UDMOS(Rg=3 Rd=12m Rs=9m Uto=2 Kp=50 Cgdmax=.7n Cgdmin=.09n Cgs=1.2n Cjo=.36n Is=36p Rb=15m mfg=International_Rectifier Vds=30 Ron=30m Qg=18n)
.model1 IRF9224S_L UDMOS(pchan Rg=3 Uto=-3.5 Rd=112m Rs=84m Rb=140m Kp=200 Cgdmax=.2n Cgdmin=.08n Cgs=1n Cjo=.1n Is=38p mfg=International_Rectifier Vds=-60 Ron=1.8m Qg=120n)
.model1 IRFL014 UDMOS(Rg=3 Uto=3.5 Rd=80m Rs=20m Rb=100m Kp=2 lambda=.01 Cgdmax=.5n Cgdmin=.07n Cgs=.25n Cjo=.1n Is=22p mfg=International_Rectifier Vds=60 Ron=1.8m Qg=120n)
```

Ready

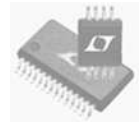
# Completing the Model



- ❖ **Must save file, quit LTspice and then reopen to access the new model.**
- ❖ **Sometimes, not all data is in Pspice file. You will need to pull more data from the datasheet.**



# Rdson Model Validation



$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown voltage temp. Coefficient	—	0.024	—	V/ $^{\circ}$ C	Reference to 25 $^{\circ}$ C, $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.0047	0.0065	$\Omega$	$V_{GS} = 10\text{V}, I_D = 16\text{A}$ ③
		—	0.0057	0.0075		$V_{GS} = 4.5\text{V}, I_D = 13\text{A}$ ③
		—	0.011	0.020		$V_{GS} = 2.8\text{V}, I_D = 3.5\text{A}$ ③

SPICE Error Log: C:\Users\Chris Gass\Training\LTSPICE\MOSFETs\...

```

Circuit: * C:\Users\Chris Gass\Training\LTSPICE\MO
.step v=2.7
Direct Newton iteration for .op point succeeded.
.step v=4.5
.step v=10

Measurement: rdson1
step      v(drain)/i(i1)    at
1         0.00891485      0.075
2         0.00544378      0.075
3         0.00376779      0.075

Measurement: rdson2
step      v(drain)/i(i1)    at
1         0.00915504      0.55
2         0.0054707        0.55
3         0.00377061      0.55

Measurement: rdson3
step      v(drain)/i(i1)    at
1         0.0092556        0.7
2         0.00548204      0.7
3         0.00377178      0.7
        
```

Gate: V1 {V}

Drain: I1, PWL(0 0 1 20)

M1: IRF7456

.tran 0 1 100m

**2.8 Vgs**

**4.5 Vgs**

**10 Vgs**

**Each .measure command corresponds to a distinct Rdson test. Make sure the current and Vgs in the .measure command match the tests on the electrical table.**

```

.measure Rdson1 find V(drain)/I(I1) when I(I1)=3.5; 2.8 Vgs test
.measure Rdson2 find V(drain)/I(I1) when I(I1)=13; 4.5 Vgs test
.measure Rdson3 find V(drain)/I(I1) when I(I1)=16; 10 Vgs test
        
```



# Switching Speed Model Validation

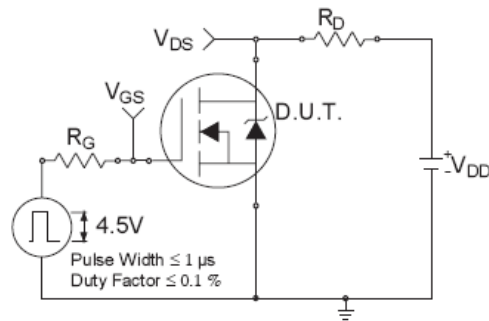
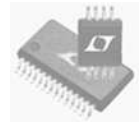


Fig 10a. Switching Time Test Circuit

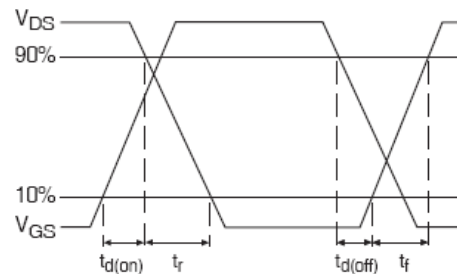
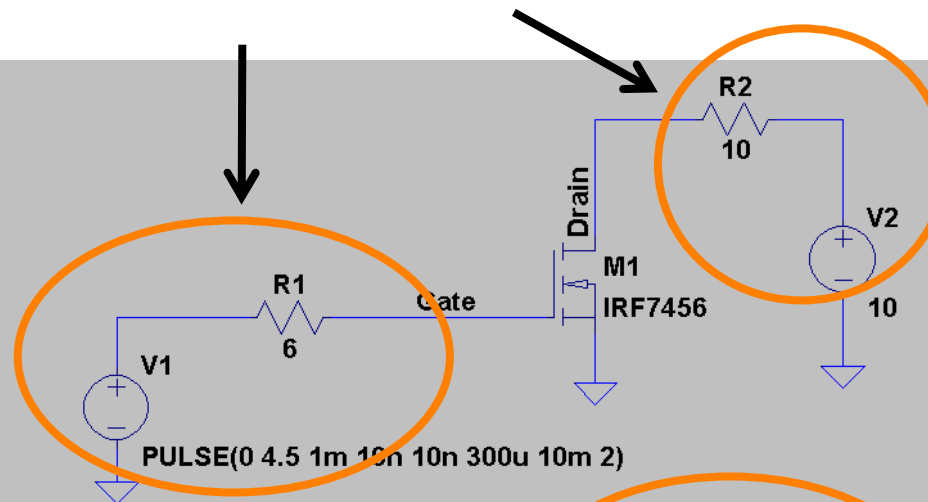


Fig 10b. Switching Time Waveforms

*V<sub>in</sub>, drain resistance, gate drive voltage, and gate resistance will be defined in the datasheet.*



.measure t1 find time when V(Gate)=0.45 rise=1  
 .measure t2 find time when V(Drain)=9 fall=1  
 .measure t3 find time when V(Drain)=1 fall=1  
 .measure t4 find time when V(Gate)=4.05 fall=1  
 .measure t5 find time when V(Drain)=1 rise=1  
 .measure t6 find time when V(Drain)=9 rise=1

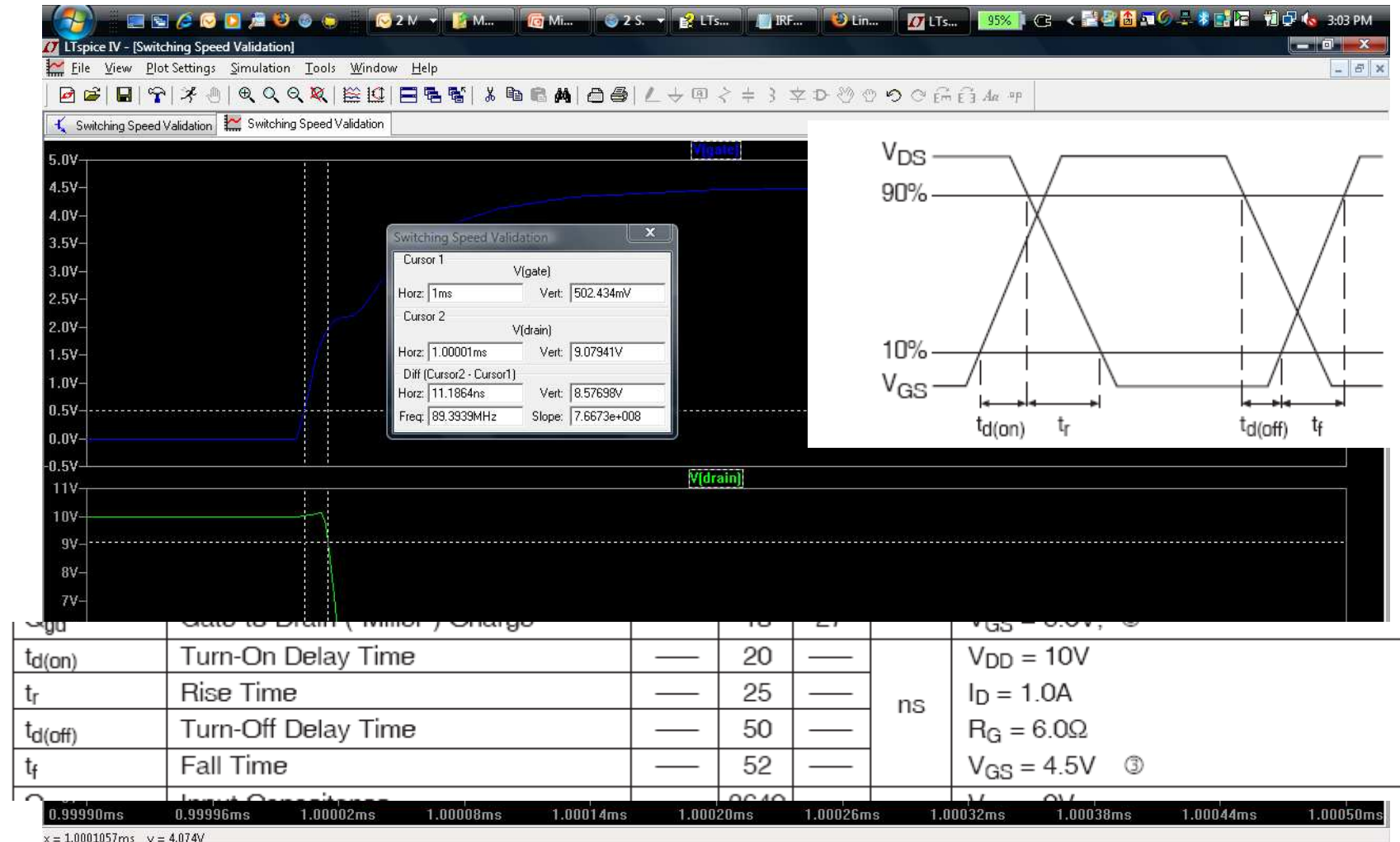
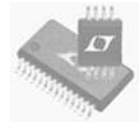
.measure tdon param t2-t1  
 .measure trise param t3-t2  
 .measure tdoff param t5-t4  
 .measure tfall param t6-t5

.tran 15m

*V(Gate) and V(Drain) voltage thresholds correspond to 10% and 90% values.*

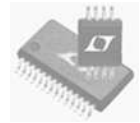
# Switching Speed Model Validation

## Turn On Delay

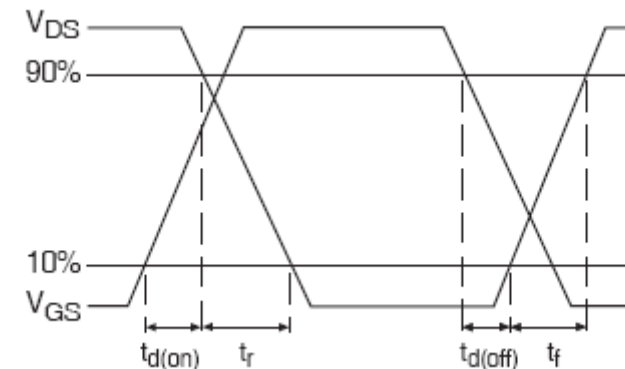
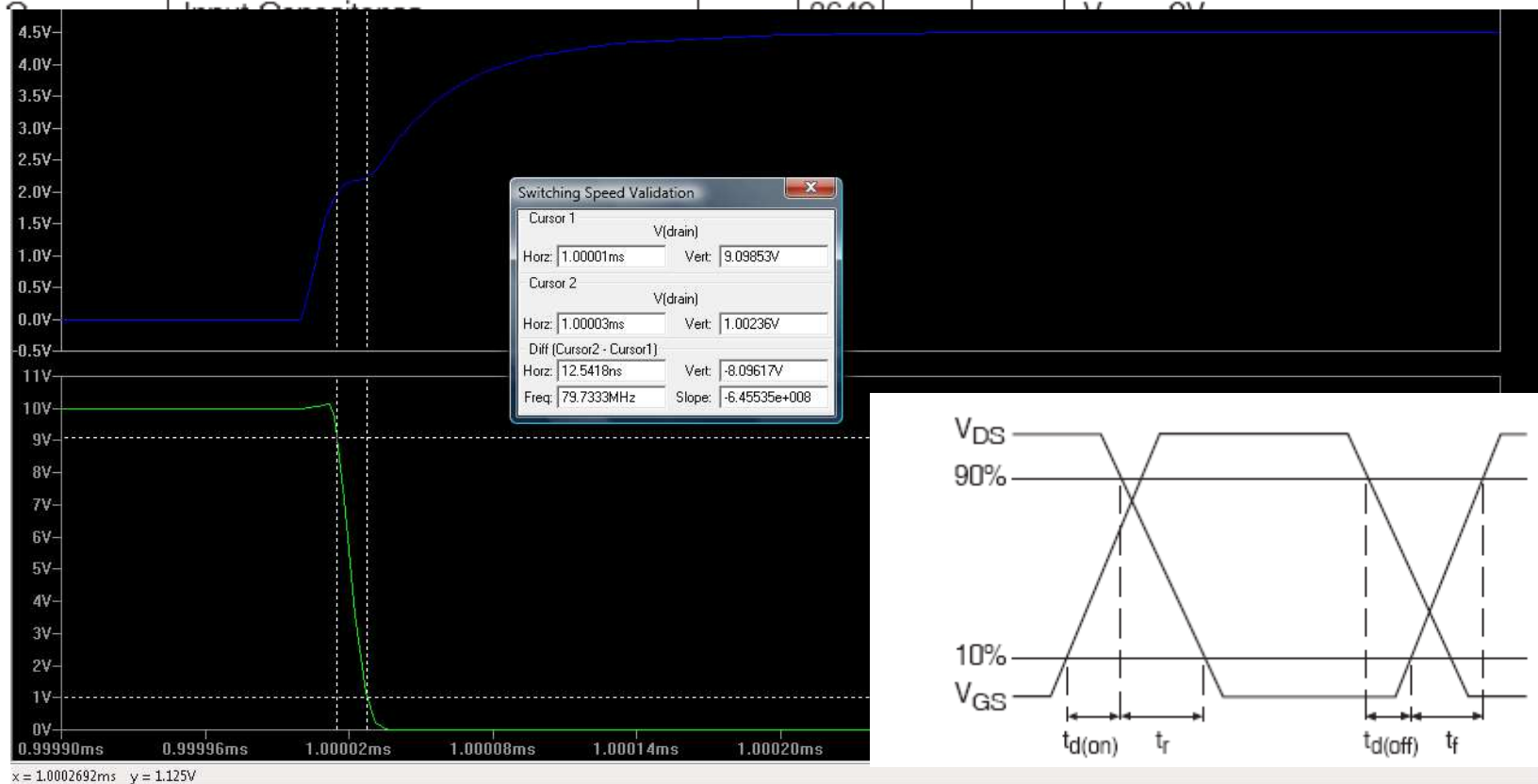


# Switching Speed Model Validation

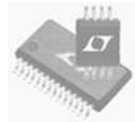
## Rise Time



Symbol	Parameter Name	Unit	Value	Notes
$t_{d(on)}$	Turn-On Delay Time	ns	20	$V_{GS} = 4.5V$ $V_{DD} = 10V$ $I_D = 1.0A$ $R_G = 6.0\Omega$ $V_{GS} = 4.5V$ ③
$t_r$	Rise Time	ns	25	
$t_{d(off)}$	Turn-Off Delay Time	ns	50	
$t_f$	Fall Time	ns	52	



# Switching Speed Model Validation



Symbol	Parameter Name	Value	Unit	Notes
$t_{d(on)}$	Turn-On Delay Time	20	ns	
$t_r$	Rise Time	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	50	ns	
$t_f$	Fall Time	52	ns	

$V_{DD} = 10V$   
 $I_D = 1.0A$   
 $R_G = 6.0\Omega$   
 $V_{GS} = 4.5V$  ③

SPICE Error Log: C:\Users\Chris Gass\Training\LTSPICE\MOSFETs\Sw...

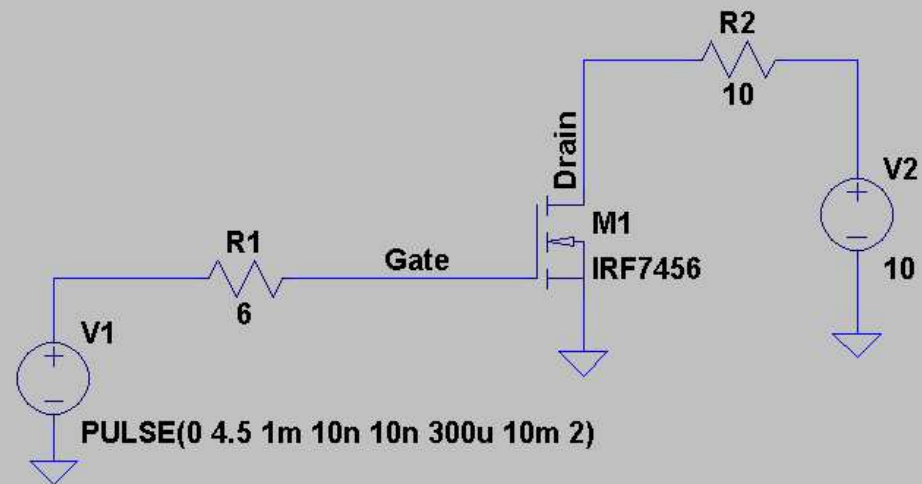
Circuit: \* C:\Users\Chris Gass\Training\LTSPICE\MOSFETs\Sw...

Direct Newton iteration for .op point succeeded

t1: time=0.001 at 0.001  
 t2: time=0.00100002 at 0.00100002  
 t3: time=0.00100003 at 0.00100003  
 t4: time=0.00130001 at 0.00130001  
 t5: time=0.00130006 at 0.00130006  
 t6: time=0.00130011 at 0.00130011  
 tdon: t2-t1=1.16482e-008  
 trise: t3-t2=1.23854e-008  
 tdoff: t5-t4=4.63506e-008  
 tfall: t6-t5=5.27265e-008

Date: Wed Jul 01 18:47:36 2009  
 Total elapsed time: 0.041 seconds.

tnom = 27  
 temp = 27  
 method = modified trap  
 totiter = 2577  
 traniter = 2572  
 tranpoints = 1177  
 accept = 1165  
 rejected = 12



.measure t1 find time when V(Gate)=0.45 rise=1  
 .measure t2 find time when V(Drain)=9 fall=1  
 .measure t3 find time when V(Drain)=1 fall=1  
 .measure t4 find time when V(Gate)=4.05 fall=1  
 .measure t5 find time when V(Drain)=1 rise=1  
 .measure t6 find time when V(Drain)=9 rise=1

.measure tdon param t2-t1  
 .measure trise param t3-t2  
 .measure tdoff param t5-t4  
 .measure tfall param t6-t5

.tran 15m

Ready



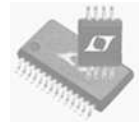
# Conclusions

- ❖ **Creating your own model takes a little time**
- ❖ **Requires a spice model and datasheet from the manufacturer**
- ❖ **Must use common sense as you review the information provided**
- ❖ **Review performance of new device. Some iteration may be required.**

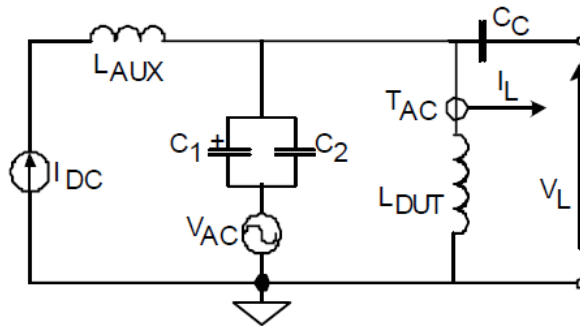


# Modeling Coil Saturation

# Modeling Coil Saturation



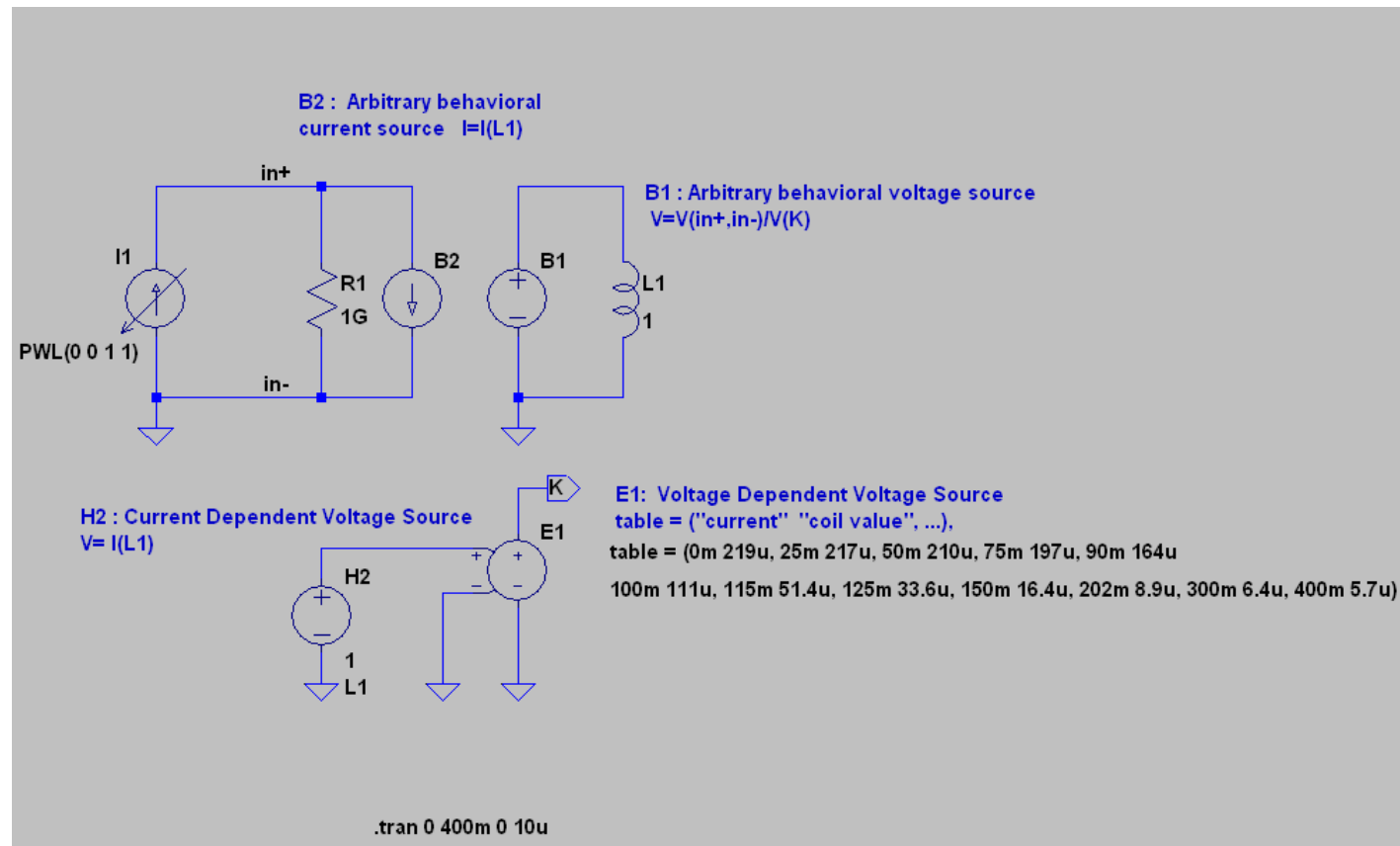
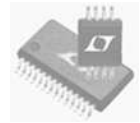
- ❖ First, characterize the saturation curve of the physical coil in the lab



**Nota : you can use a RLC meter if available!**

- ❖ Use “Voltage Dependent Voltage Source” or “Voltage Dependent Current Source” in order to model the coil saturation curve using the look up table capability of these behavioral sources
- ❖ A look-up table is used to specify the transfer function. The table is a list of pairs of numbers. The second value of the pair is the output voltage when the control voltage is equal to the first value of that pair. The output is linearly interpolated when the control voltage is between specified points. If the control voltage is beyond the range of the look-up table, the output voltage is extrapolated as a constant voltage of the last point of the look-up table.

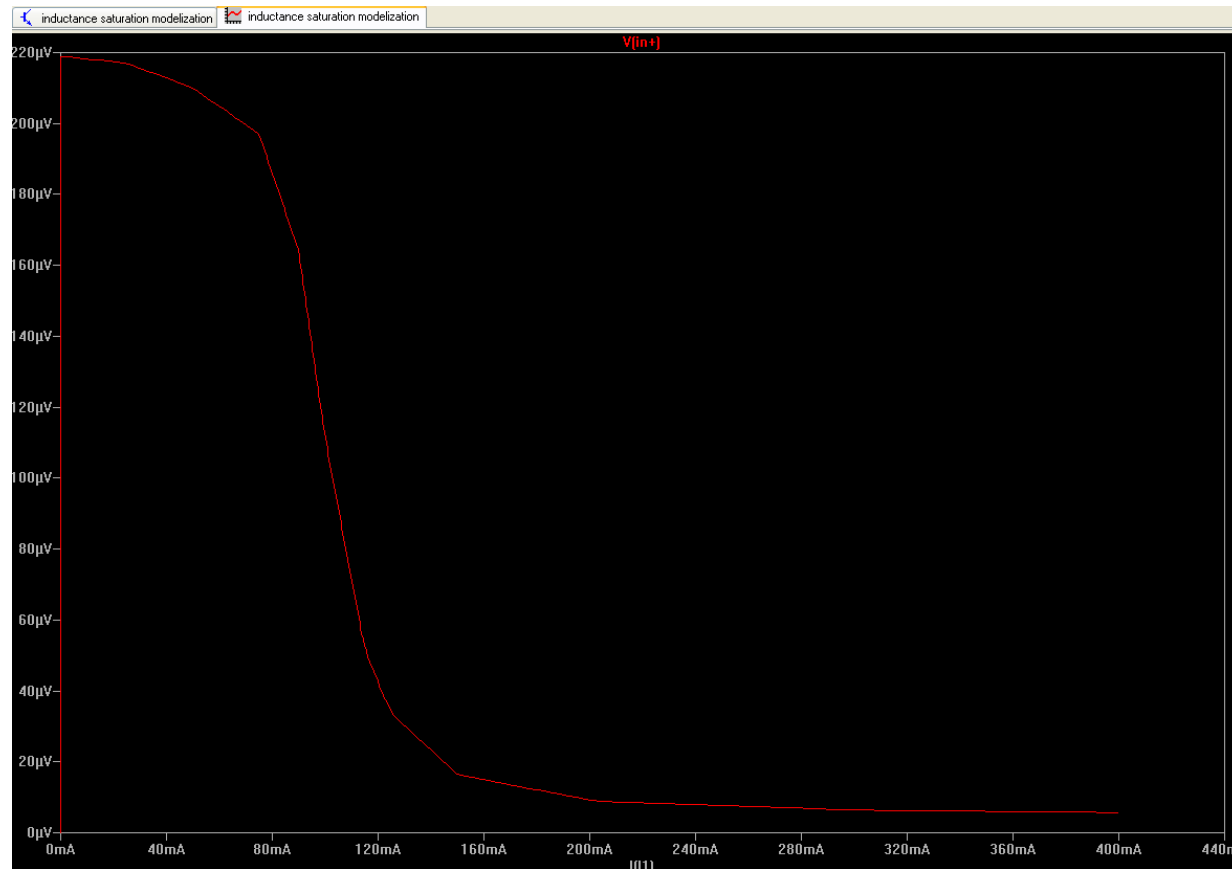
# Modeling Coil Saturation





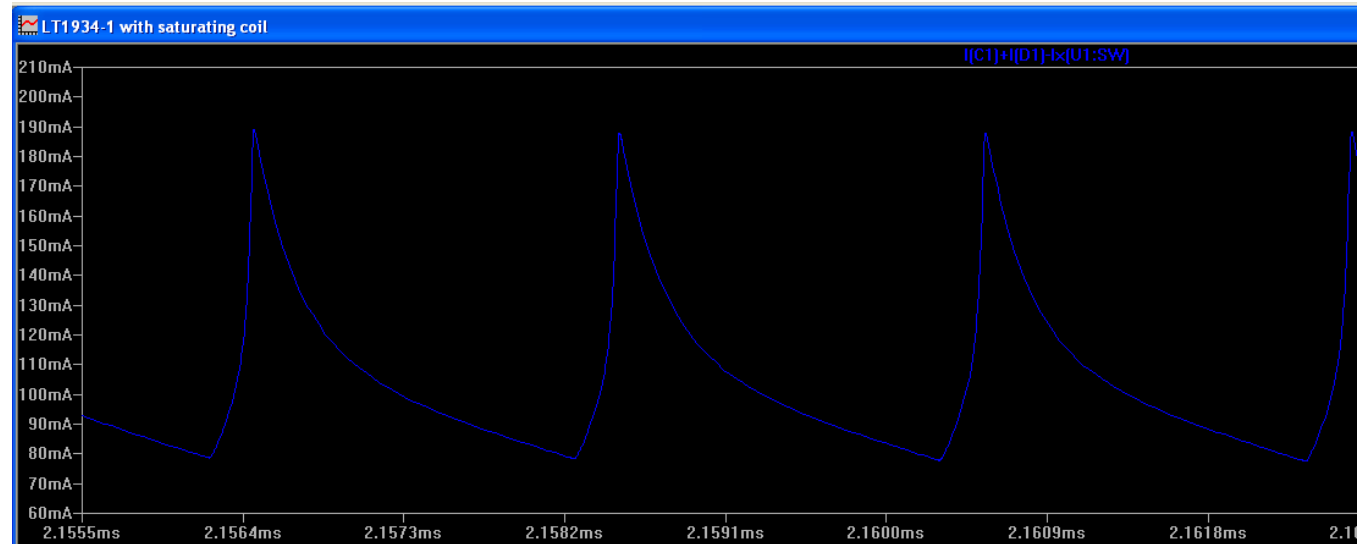
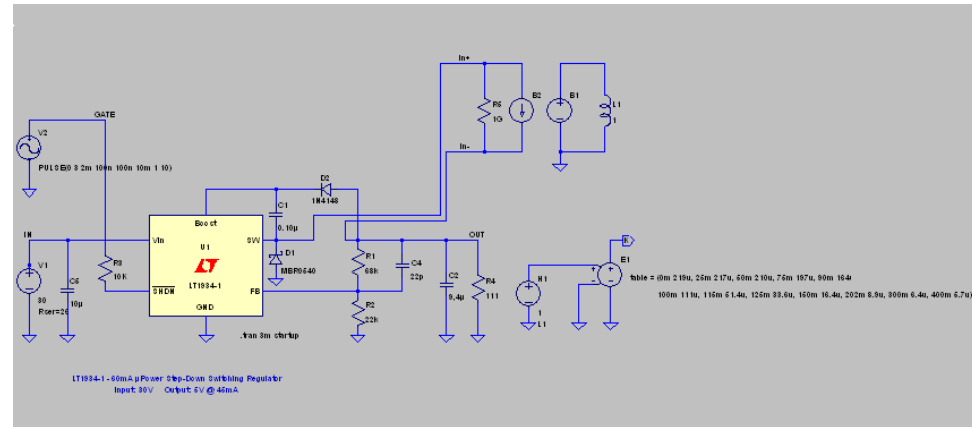


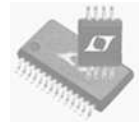
# Modeling Coil Saturation



***Plotting  $V(in+)$  vs.  $I(I1)$  to check the model !***

# Modeling Coil Saturation





# Variable Capacitor vs. Voltage ...

