LTspice IV
Intermediate Lab Class Volume 3

Presented by:
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Linear Technology FAE

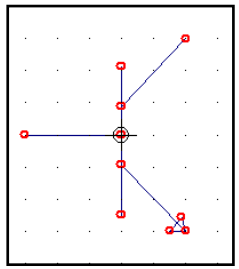
Topics

1. *Creating a Schematic Symbol*
2. *Gain & Phase Analysis*
3. *Modeling MOSFETs*
4. *Modeling Coil Saturation*

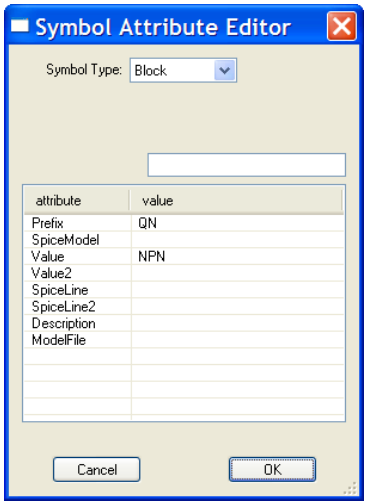
Creating a Schematic Symbol

Creating a Schematic Symbol

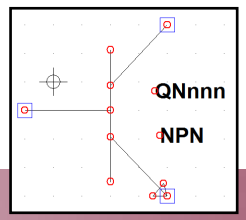
Creating a NPN Transistor Schematic Symbol



1. *Open up LTspice*
2. *File pull down menu ---> New Symbol*
3. *Draw pull down menu ---> Line. Draft an NPN symbol.*
4. *Edit pull down menu ---> Add Pin/Port. These are the actual electrical connections for B (base), C (collector), E (emitter). Netlist order for the pins: C = 1, B = 2, E = 3.*
5. *Edit pull down menu ---> Attributes ---> Edit Attributes (to add attributes). See the screen shot here ---------->*



6. *Edit pull down menu ---> Attributes ---> Attribute Window (for attribute visibility) to make QN and NPN visible for the symbol*



Creating a Schematic Symbol

Creating a NPN Transistor Schematic Symbol (continued…..)

7. ***Save the schematic symbol as "My_NPN.asy" in the same folder as the simulation file titled "NPN Schematic Symbol Import.asc"***
8. ***Open up the simulation file titled "NPN Schematic Symbol Import.asc" and follow the instructions in the simulation file.***

Gain & Phase Analysis

How Do I Do Stability Analysis Of Switching Power Supplies In LTspice?

LTC3412A Example

- 5 Vin to 2.5 Vout @ 2.0 A
- DC652A Demoboard

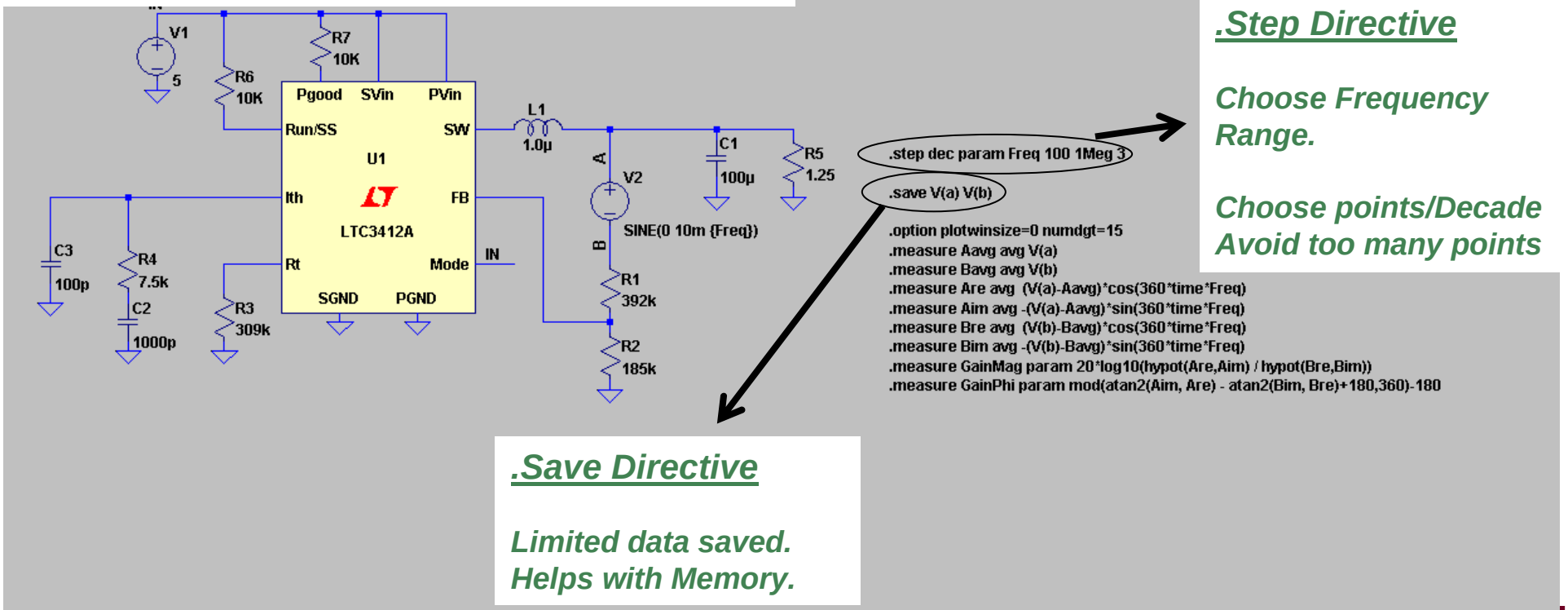
LTC3412A Example

Simulation Command

Set simulation time to be as long as one period of the lowest frequency analyzed in the .step command plus the time to steady state.

Save data only after steady state is reached.

Limit maximum step size for proper measurement.



.Step Directive

Choose Frequency Range.

Choose points/Decade
Avoid too many points

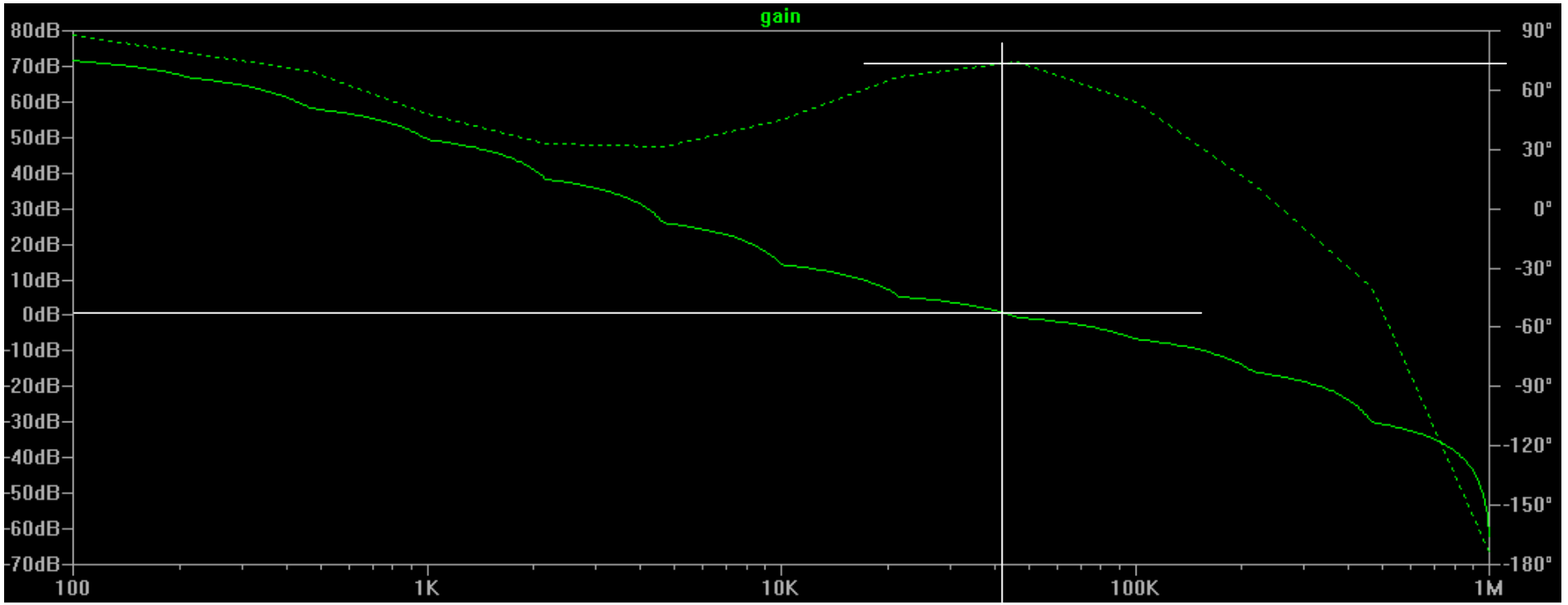
.Save Directive

Limited data saved.
Helps with Memory.

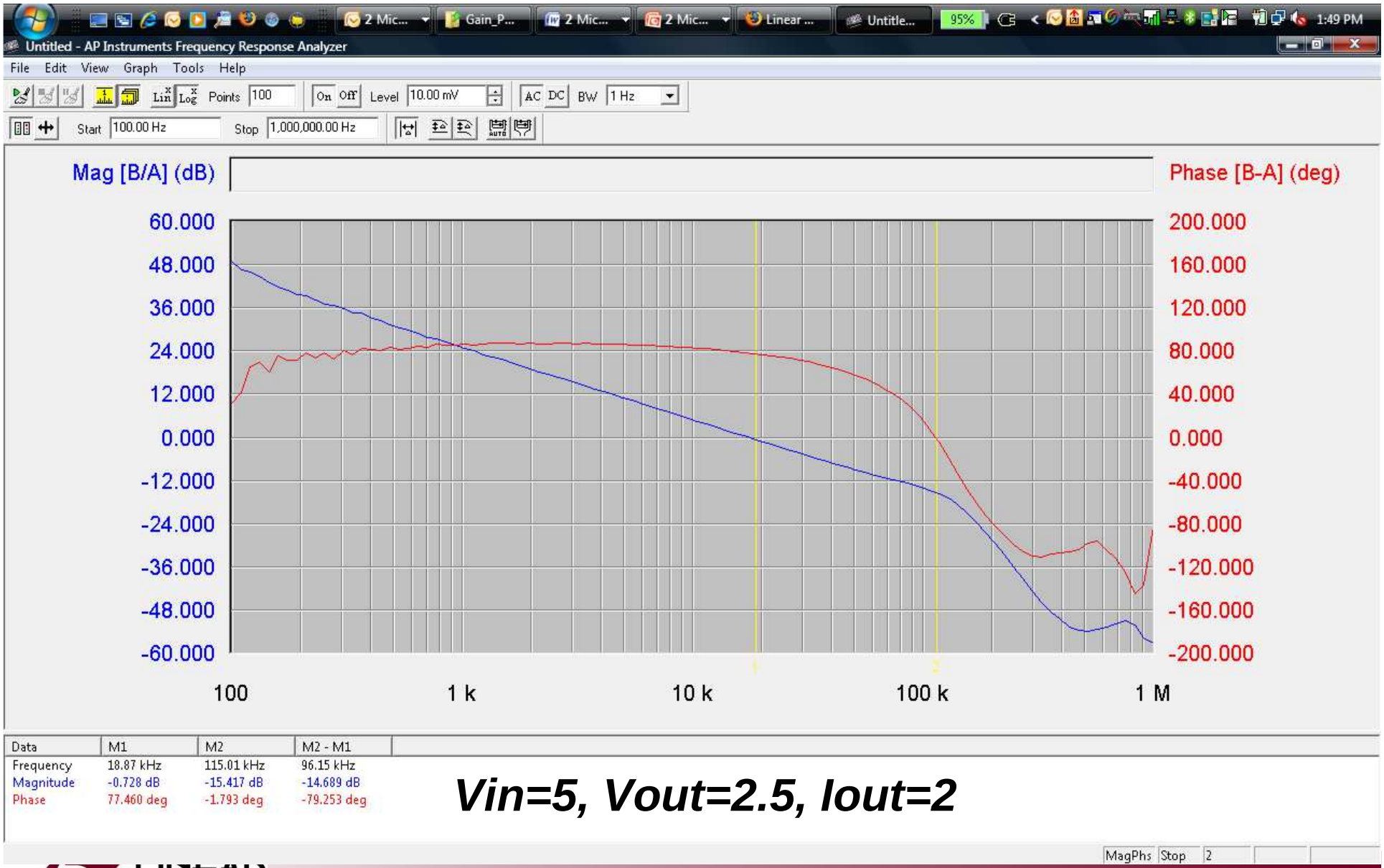
Run Simulation, Then…..

- After simulation is complete, from the "View" menu, select 'Spice Error Log'
  - Right click anywhere in new window
    - Select 'Plot .step'ed .meas data‘
      - Select 'Yes' in the next dialog box
  - Right click anywhere in next window
    - Select 'Add Trace'
      - Select 'gain' and press 'OK’

Simulation Results – Long Run
30 Minute Run Time



Actual Measured Data

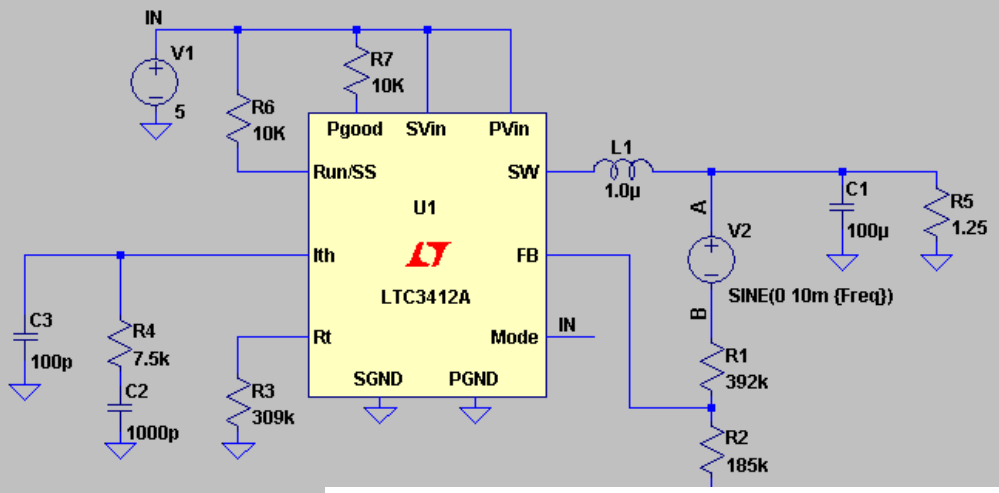


Vin=5, Vout=2.5, Iout=2

Simulation Speed Up Tips

Simulation Command

If frequency range in .step command is narrowed, then the total simulation time can be reduced to one period of the lowest frequency plus the time it takes to get to steady state.



.tran 0 11m 1m 0.5u startup

Must limit maximum step size for proper gain/phase to 0.5us in Simulation Command.

.step dec param Freq 100 1Meg 3

.save V(a) V(b)

.option plotwinsize=0 numdgt=15
.measure Aavg avg V(a)
.measure Bavg avg V(b)
.measure Are avg (V(a)-Aavg)*cos(360*time*Freq)
.measure Aim avg -(V(a)-Aavg)*sin(360*time*Freq)
.measure Bre avg (V(b)-Bavg)*cos(360*time*Freq)
.measure Bim avg -(V(b)-Bavg)*sin(360*time*Freq)
.measure GainMag param 20*log10(hypot(Are,Aim) / hypot(Bre,Bim))
.measure GainPhi param mod(atan2(Aim, Are) - atan2(Bim, Bre)+180,360)-180

.Step Directive

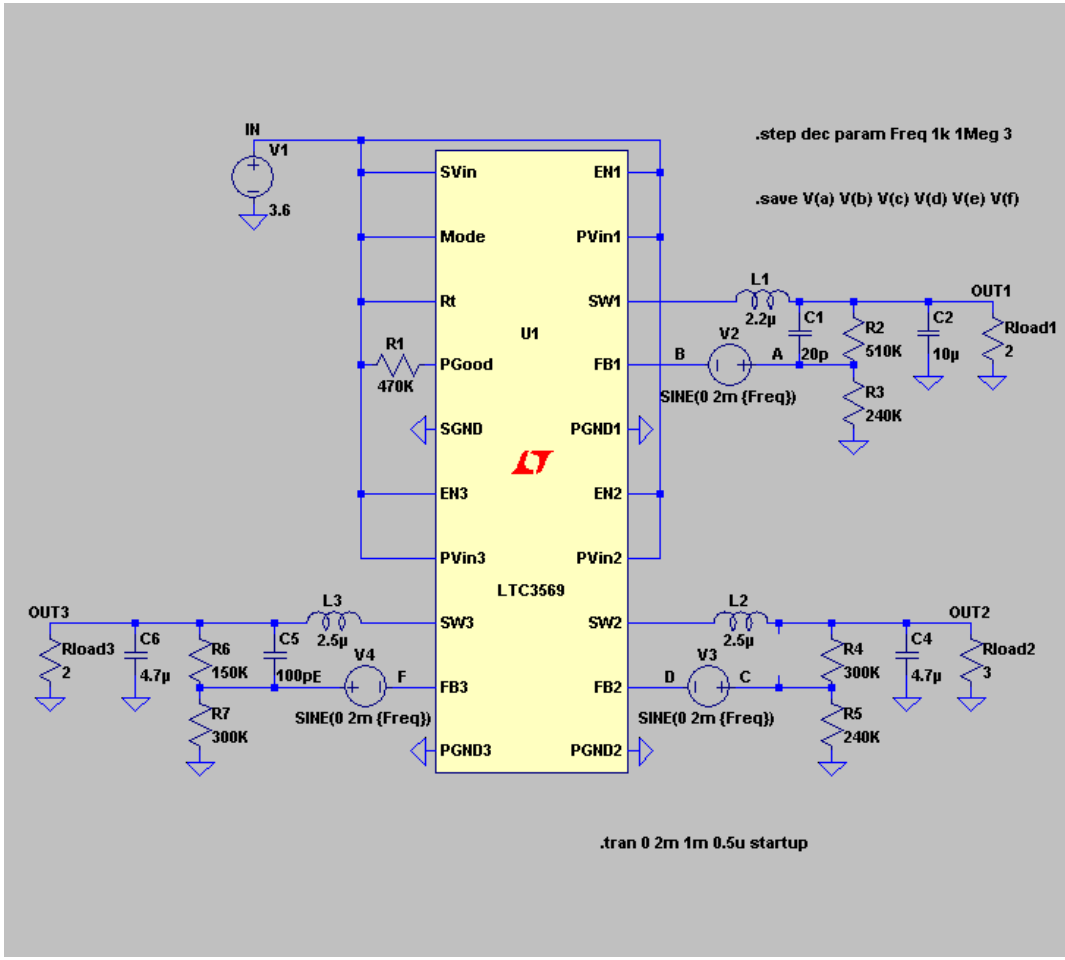
Choose Narrow Frequency Range.

Speed UP Summary

1.Change .tran directive to ".tran 0 2m 1m 0.5u startup
2.Change .step directive to ".step dec param Freq 1k 1Meg 3

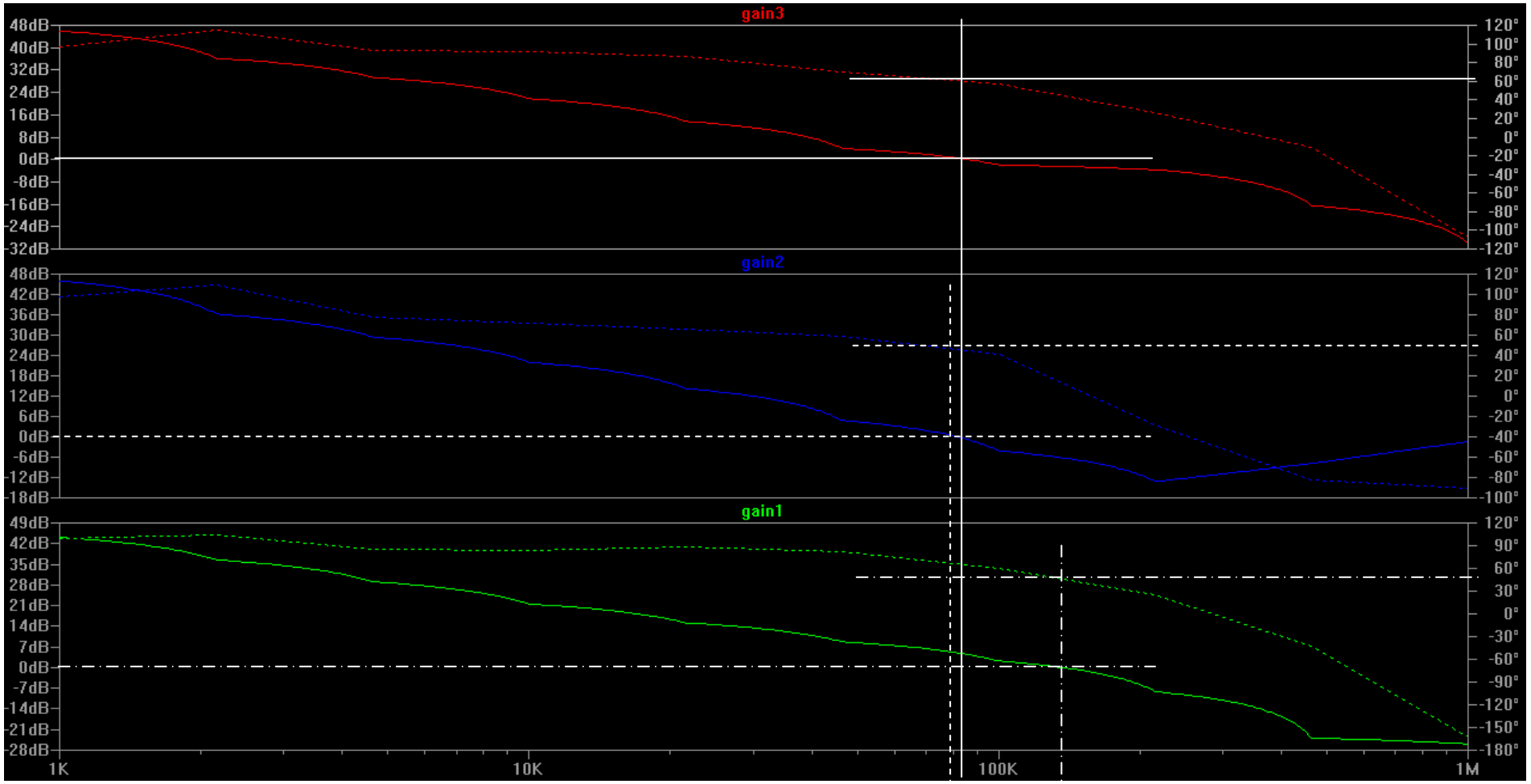
The frequency of interest is changed from 100-1Meg Hz to 1K-1Meg Hz

Multi Output DC-DC Converter



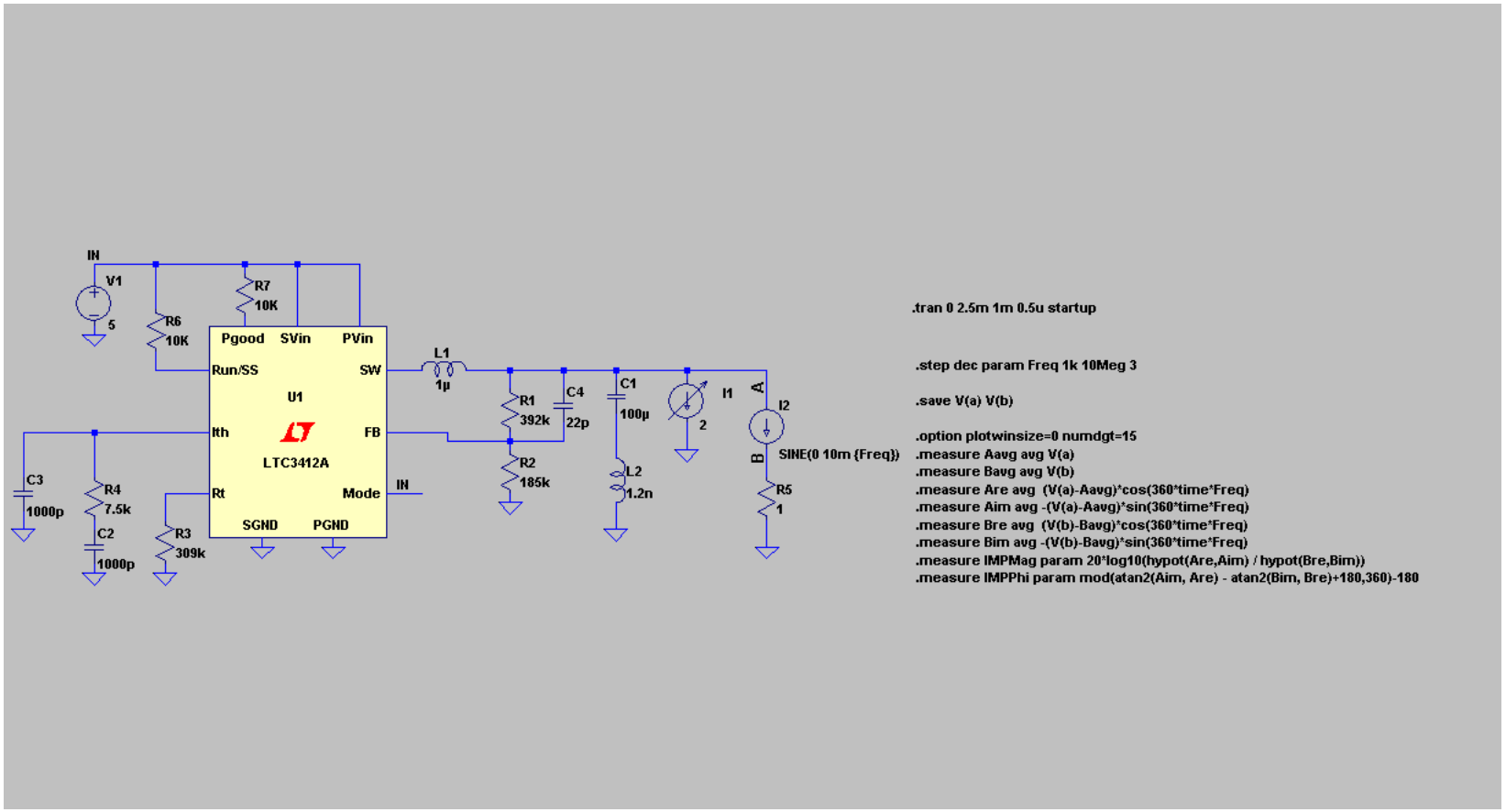

```
.option plotwinsize=0   numdgt=15

.measure Aavg avg V(a)
.measure Bavg avg V(b)
.measure Are avg  (V(a)-Aavg)*cos(360*time*Freq)
.measure Aim avg -(V(a)-Aavg)*sin(360*time*Freq)
.measure Bre avg  (V(b)-Bavg)*cos(360*time*Freq)
.measure Bim avg -(V(b)-Bavg)*sin(360*time*Freq)
.measure Gain1Mag param 20*log10(hypot(Are,Aim) / hypot(Bre,Bim))
.measure Gain1Phi param mod(atan2(Aim, Are) - atan2(Bim, Bre)+180,360)-180

.measure Cavg avg V(c)
.measure Davg avg V(d)
.measure Cre avg  (V(c)-Cavg)*cos(360*time*Freq)
.measure Cim avg -(V(c)-Cavg)*sin(360*time*Freq)
.measure Dre avg  (V(d)-Davg)*cos(360*time*Freq)
.measure Dim avg -(V(d)-Davg)*sin(360*time*Freq)
.measure Gain2Mag param 20*log10(hypot(Cre,Cim) / hypot(Dre,Dim))
.measure Gain2Phi param mod(atan2(Cim, Cre) - atan2(Dim, Dre)+180,360)-180

.measure Eavg avg V(e)
.measure Favg avg V(f)
.measure Ere avg  (V(e)-Eavg)*cos(360*time*Freq)
.measure Eim avg -(V(e)-Eavg)*sin(360*time*Freq)
.measure Fre avg  (V(f)-Favg)*cos(360*time*Freq)
.measure Fim avg -(V(f)-Favg)*sin(360*time*Freq)
.measure Gain3Mag param 20*log10(hypot(Ere,Eim) / hypot(Dre,Dim))
.measure Gain3Phi param mod(atan2(Eim, Ere) - atan2(Fim, Fre)+180,360)-180
```

Multi Output Converter Results

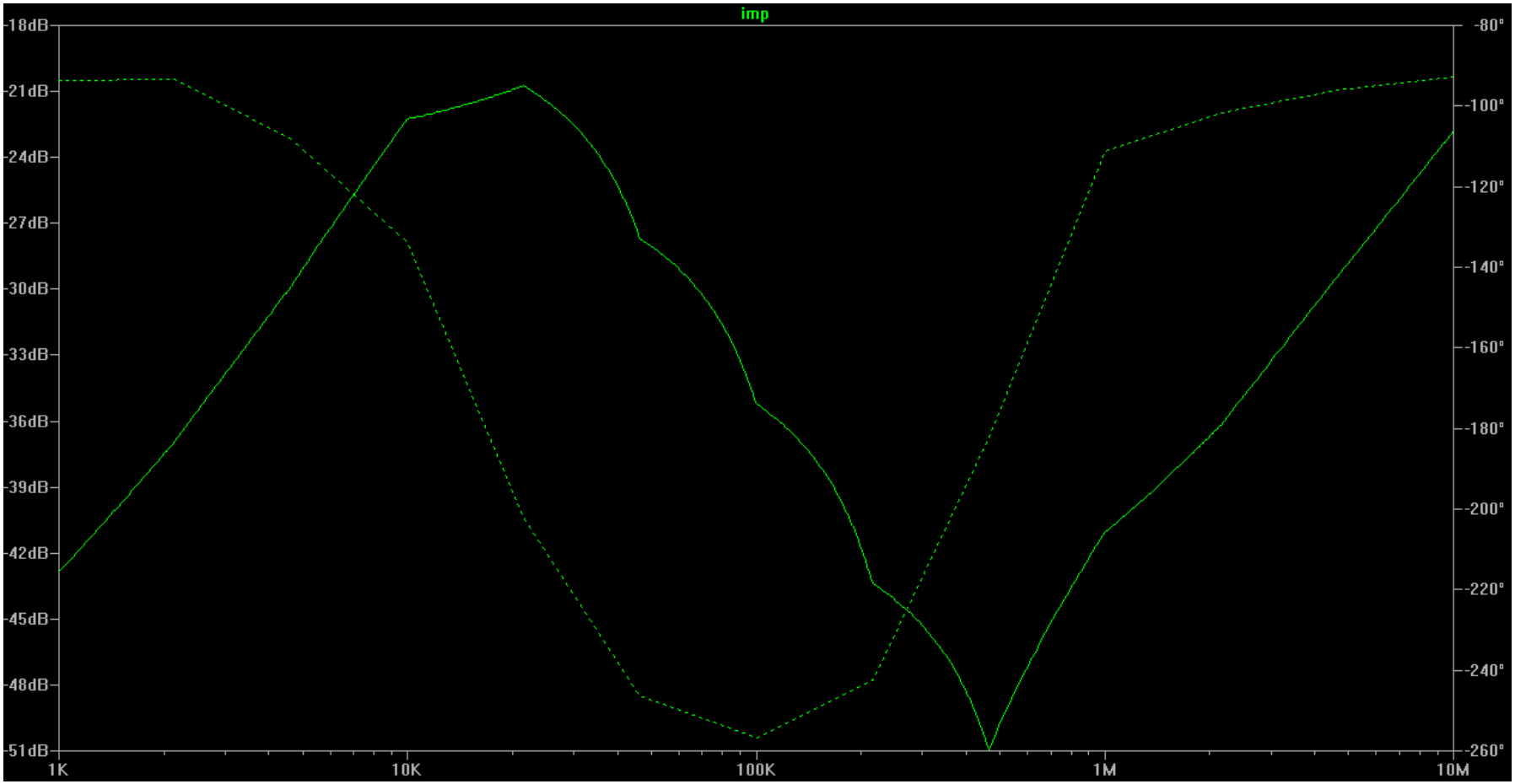


Output Imepedance

The same methodology can be applied to measure output impedance



Output Impedance Results

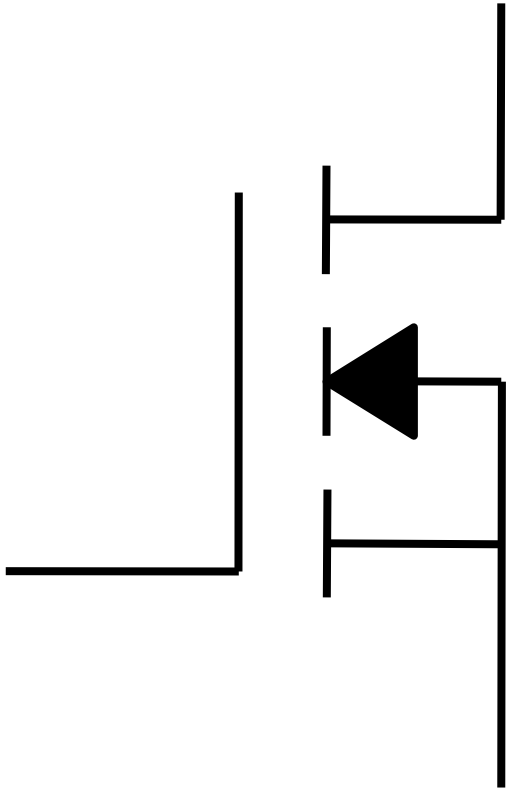


Conclusion

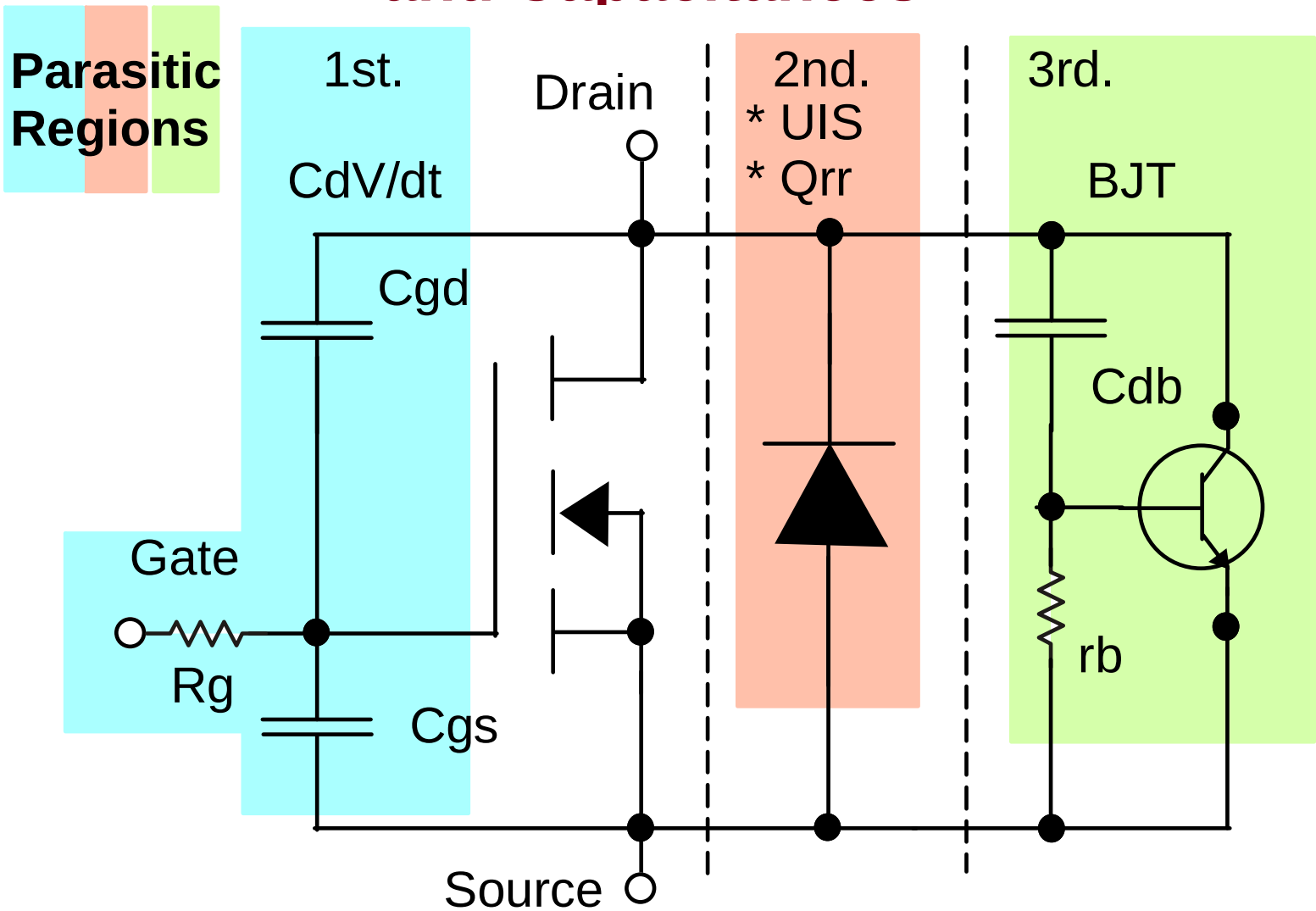
1. **Possible to do small signal analysis of switching systems within Ltspice**
2. **Not limited to one output**
3. **Multiple inputs also possible. However, do not daisy chain DC-DC converters. The injected signal of the upstream converter interacts with the downstream converter.**
4. **Multioutput supplies consume a lot of memory. Sample data should be over a limited frequency range.**

Modeling MOSFETs

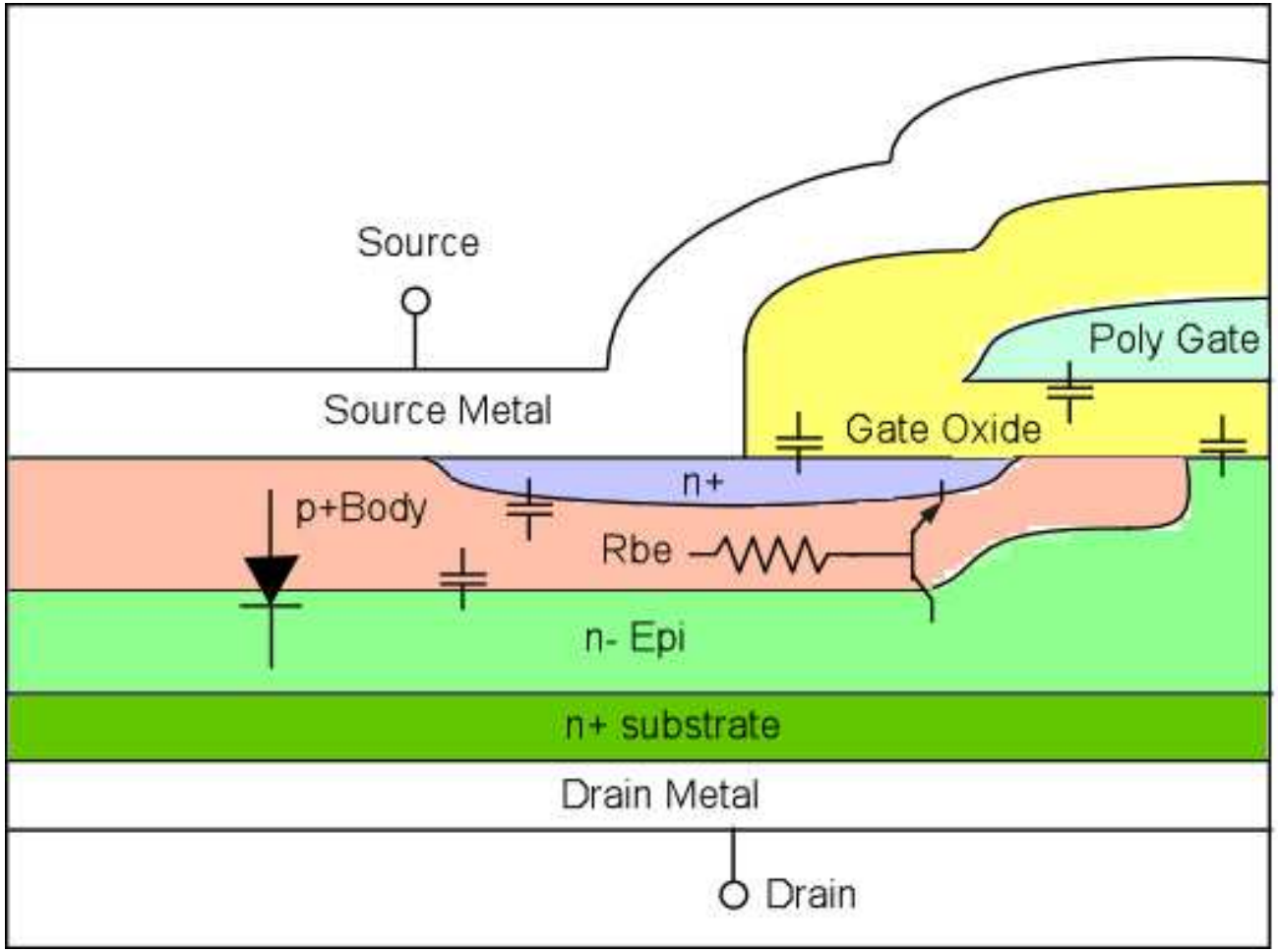
A MOSFET is a Simple Device, Right?



Power MOSFET with Parasitic BJT, Diode and Capacitances



Power MOSFET Cross Section



LTspice VDMOS Model

- Traditional Models are complex and slow, building elaborate subcircuits to duplicate behavior
- LTspice MOSFET Model is a new intrinsic model
  - Speed
  - Convergence
  - Simplicity
- DC Model is the same as a Level 1 Pspice model
- AC Model is based on:
  - Gate to source capacitance is constant
  - Gate to drain capacitance follows an empirical curve based on hyperbolic tangent whose min and max point is based on:
    - MOSFET off, Vgd is negative, Cgd is at minimum
    - MOSFET on, Vgd is positive, Cgd is at maximum

Search, "M. MOSFET" in LTspice help section for further details

What do I need to make my own model?

- Datasheet of MOSFET
- Pspice model file

Explanation of Terms

- Rg – Gate ohmic resistance
- Rd – Drain ohmic resistance.
- Rs – Source ohmic resistance.
- Vto – Zero-bias threshold voltage.
- Kp – Transconductance.
- Cgdmax – Maximum gate to drain capacitance.
- Cgdmin – Minimum gate to drain capacitance.
- Cgs – Gate to source capacitance.
- Cjo – Parasitic diode capacitance.
- Is - Parasitic diode saturation current.
- Rb – Body diode resistance.

Search, "M. MOSFET" in LTspice help section for further details

Example – IRF7456 MOSFET

- What is needed?
  - Spice Model provided by the vendor.
  - Datasheet provided by the vendor.

- Open LTspice. If you use Vista, you must run LTspice as the administrator.

- From the File tab, select ‘Open’
- C: Program Files
  - LTC folder
    - LTspiceIV
      - Lib
        - CMP
        - Standard.mos

Example – IRF7456 MOSFET

Go to Text File and Datasheet

Warning!!!!

Do not trust the vendor spice model to be correct

Comments about the Spice Model

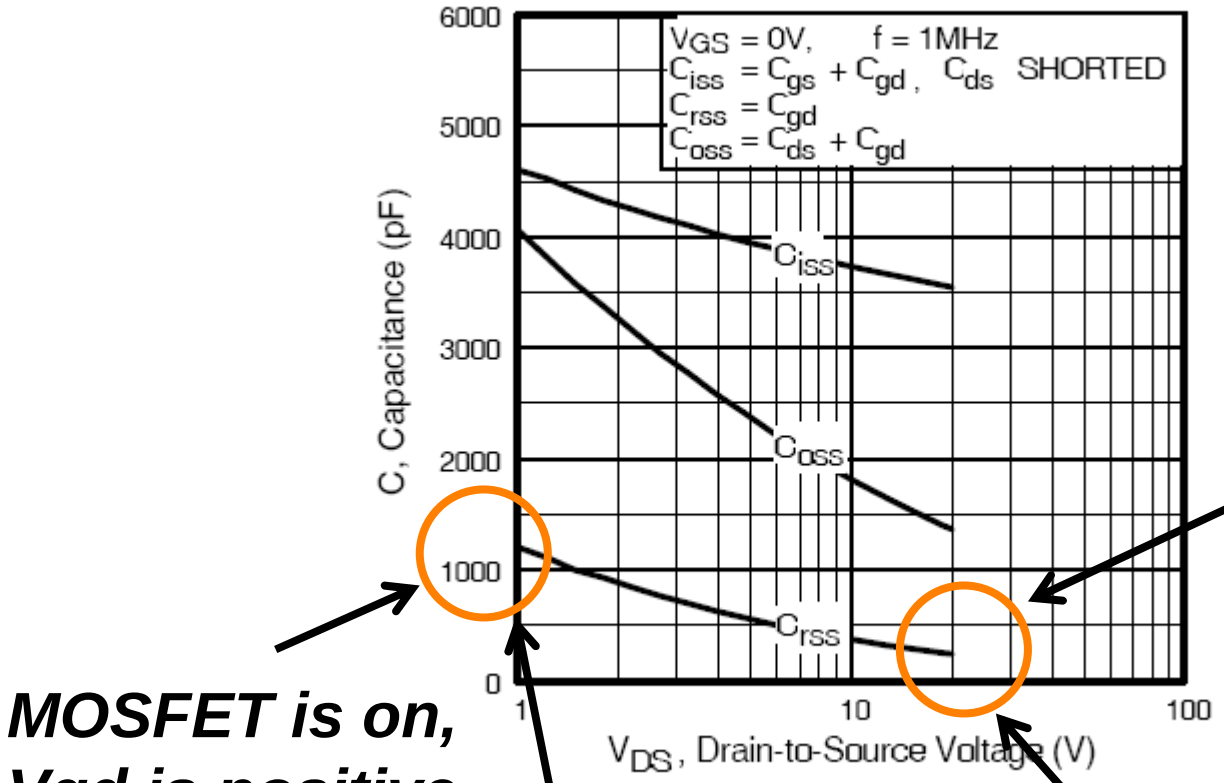
All parameters should be in the Level 1 section

Gate threshold and Gate capacitance do not match the datasheet

```
.MODEL MM NMOS LEVEL=1 IS=1e-32
+VTO=2.07545 LAMBDA=0.0453657 KP=119.186
+CGSO=3.37108e-05 CGDO=1.97763e-09
RS 8 3 0.0001
D1 3 1 MD
.MODEL MD D IS=1.87521e-13 RS=0.013756 N=0.919559 BV=20
+IBV=0.00025 EG=1 XTI=1 TT=0
+CJO=3.98952e-09 VJ=0.635683 M=0.361988 FC=0.5
RDS 3 1 1e+06
RD 9 1 0.002047
RG 2 7 1.73819
D2 4 5 MD1
```

Diode resistance is within the diode subcirc

IRF7456 Gate to Drain Capacitance



MOSFET is off, Vgd is negative

MOSFET is on, Vgd is positive

Cgdmax

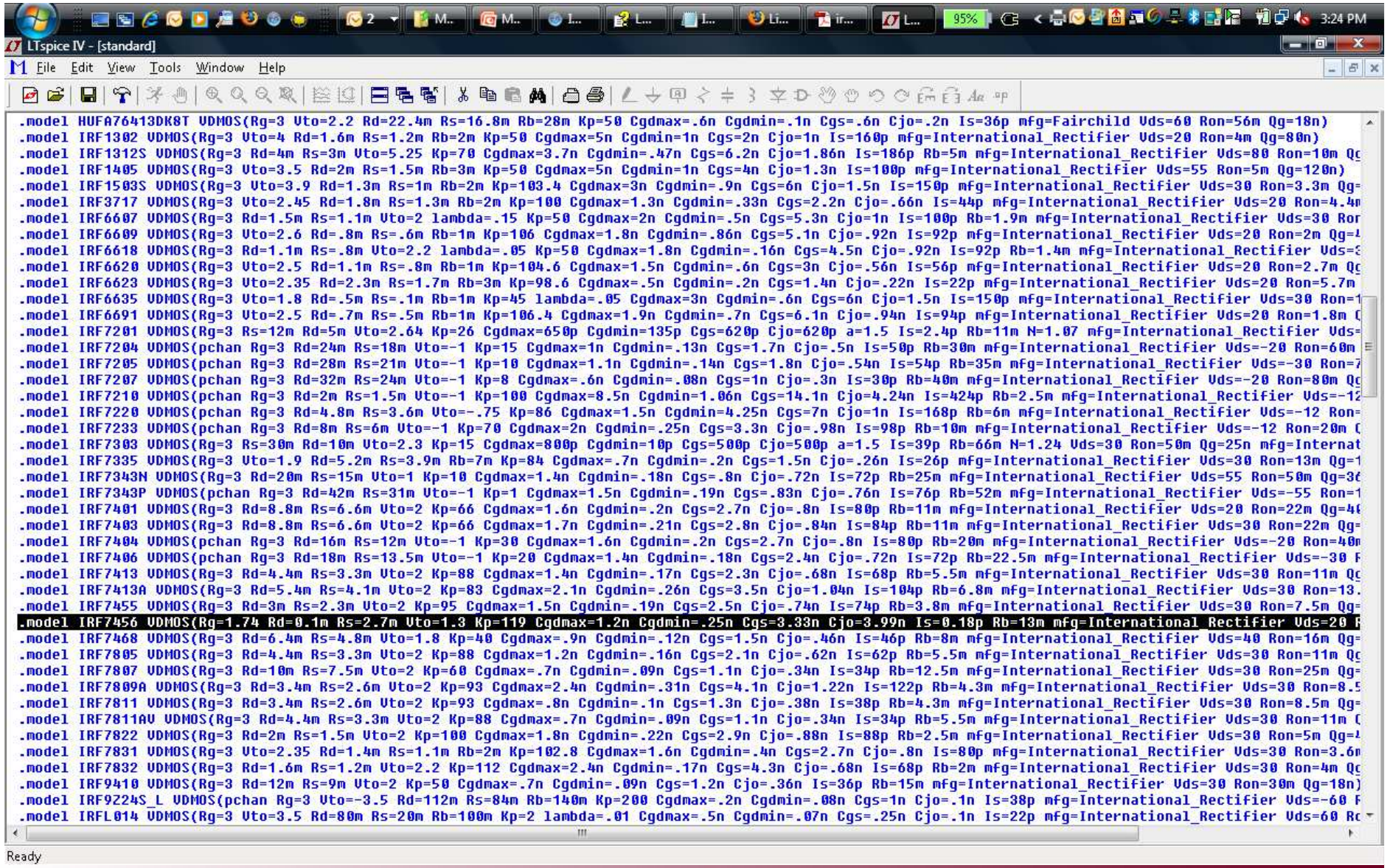
Cgdmin

IRF7456 Model

Always compare spice model to datasheet. Sometimes the numbers in the spice model don't pass the 'common sense test'.

Term	Value	Source
Rg	1.74	Spice Model
Rd	0.0001	Spice Model
Rs	0.0027	Spice Model
Vto	1.3	Data Sheet Electrical Table
Kp	119	Spice Model
Cgdmax	1200 e-12	Data Sheet Curve
Cgdmin	250 e-12	Data Sheet Curve
Cgs	3.37e-9	Data Sheet Electrical Table
Cjo	3.99e-9	Spice Model
Is	1.87e-13	Spice Model
Rb	0.013	Spice Model

Add New Model Within LTSpice



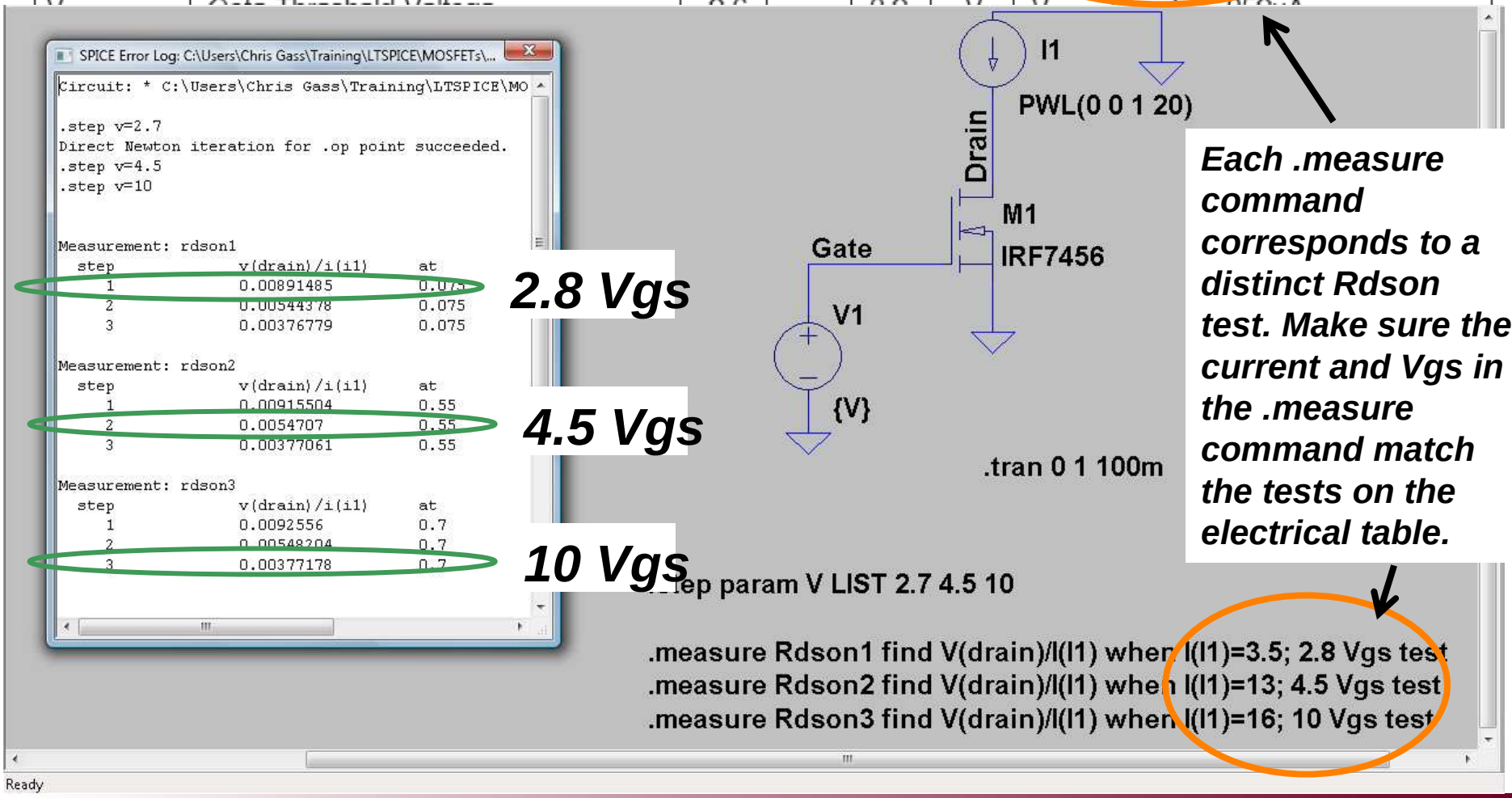
Completing the Model

- Must save file, quit LTspice and then reopen to access the new model.

- Sometimes, not all data is in Pspice file. You will need to pull more data from the datasheet.

Rdson Model Validation

$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.024	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.0047	0.0065	Ω	V_{GS} = 10V, I_D = 16A ②
		—	0.0057	0.0075		V_{GS} = 4.5V, I_D = 13A ③
		—	0.011	0.020		V_{GS} = 2.8V, I_D = 3.5A ③



Switching Speed Model Validation

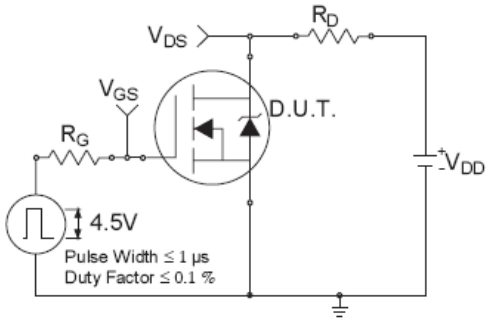


Fig 10a. Switching Time Test Circuit

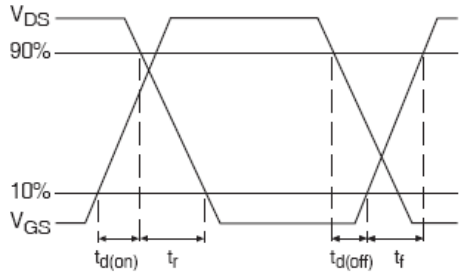
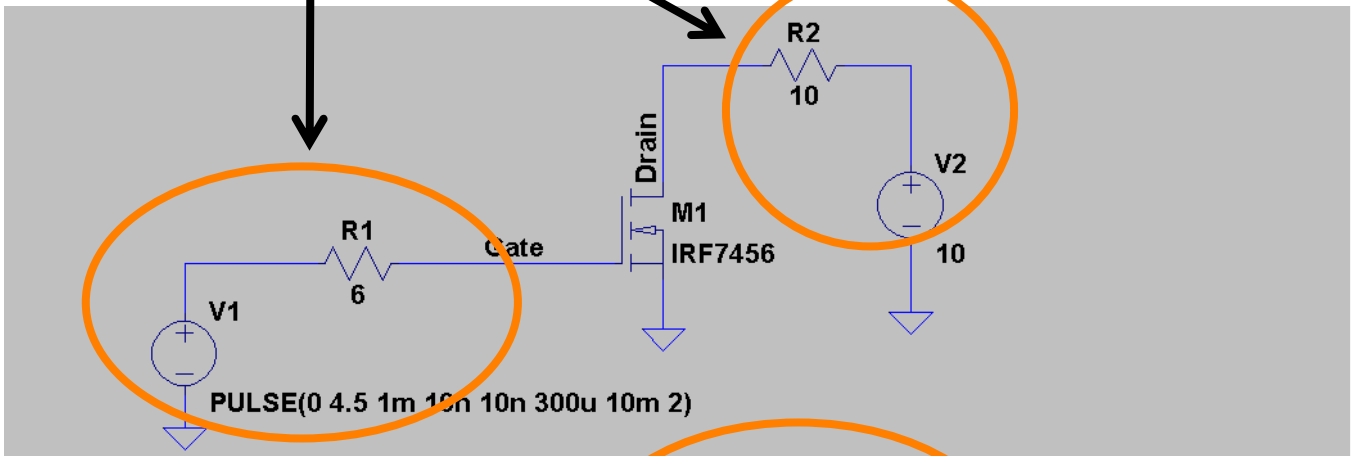


Fig 10b. Switching Time Waveforms

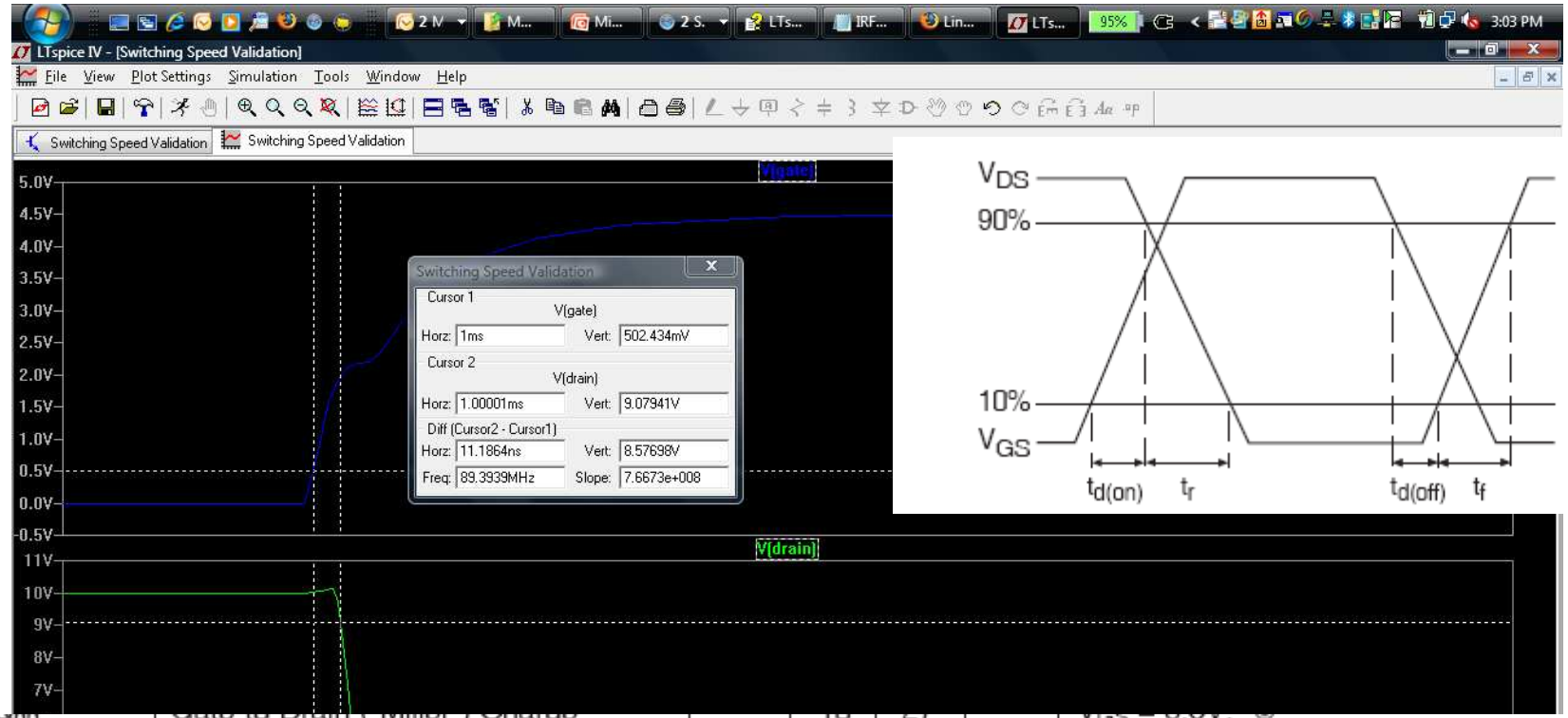
Vin, drain resistance, gate drive voltage, and gate resistance will be defined in the datasheet.




```
.measure t1 find time when V(Gate)=0.45 rise=1
.measure t2 find time when V(Drain)=9 fall=1
.measure t3 find time when V(Drain)=1 fall=1
.measure t4 find time when V(Gate)=4.05 fall=1
.measure t5 find time when V(Drain)=1 rise=1
.measure t6 find time when V(Drain)=9 rise=1

.measure tdon param t2-t1
.measure trise param t3-t2
.tran 15m      .measure tdoff param t5-t4
.measure tfall param t6-t5
```

V(Gate) and V(Drain) voltage thresholds corespond to 10% and 90% values.

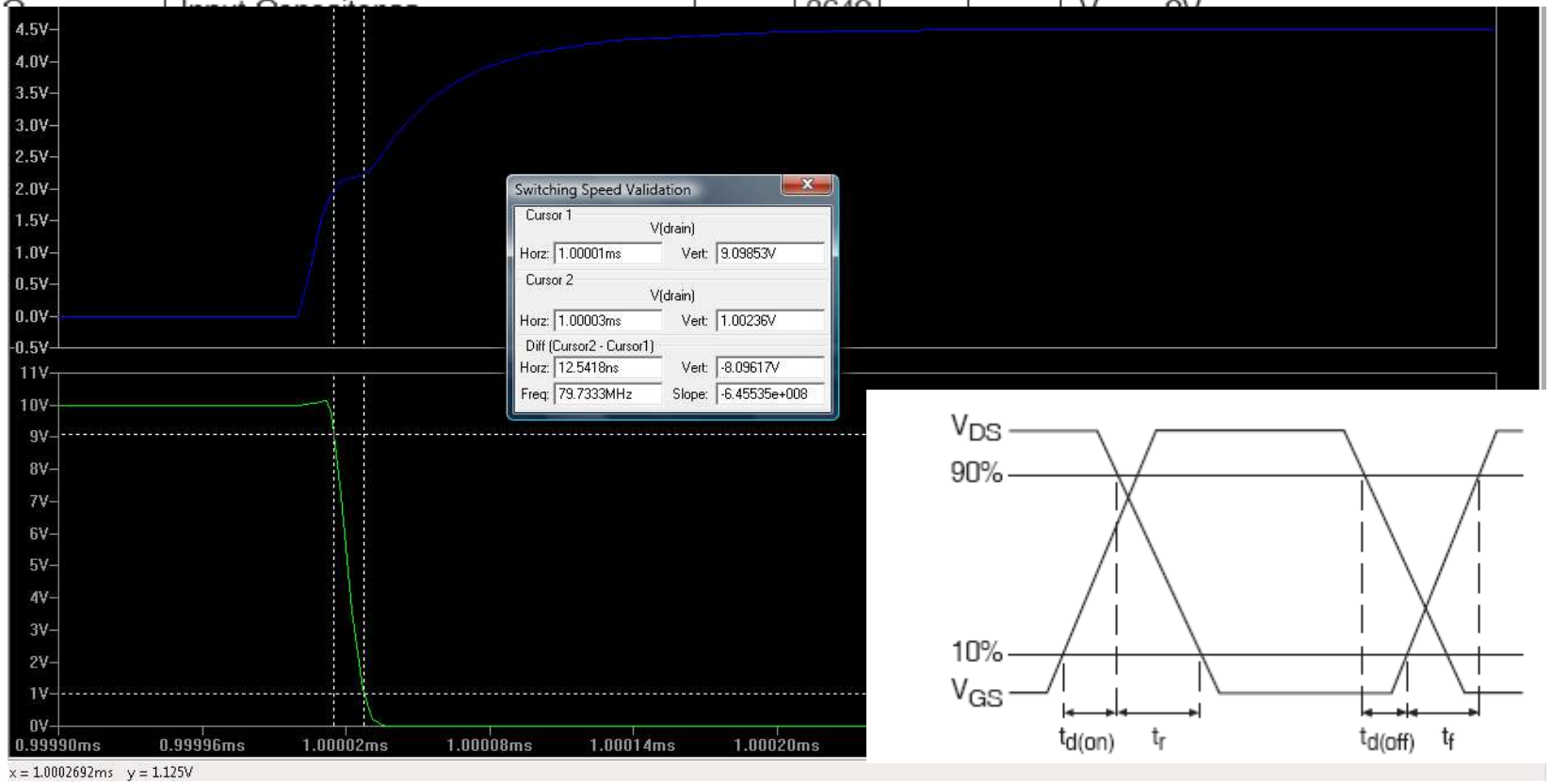
Switching Speed Model Validation
Turn On Delay



$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	V_{DD} = 10V
t_r	Rise Time	—	25	—		I_D = 1.0A
$t_{d(off)}$	Turn-Off Delay Time	—	50	—		R_G = 6.0Ω
t_f	Fall Time	—	52	—		V_{GS} = 4.5V ③

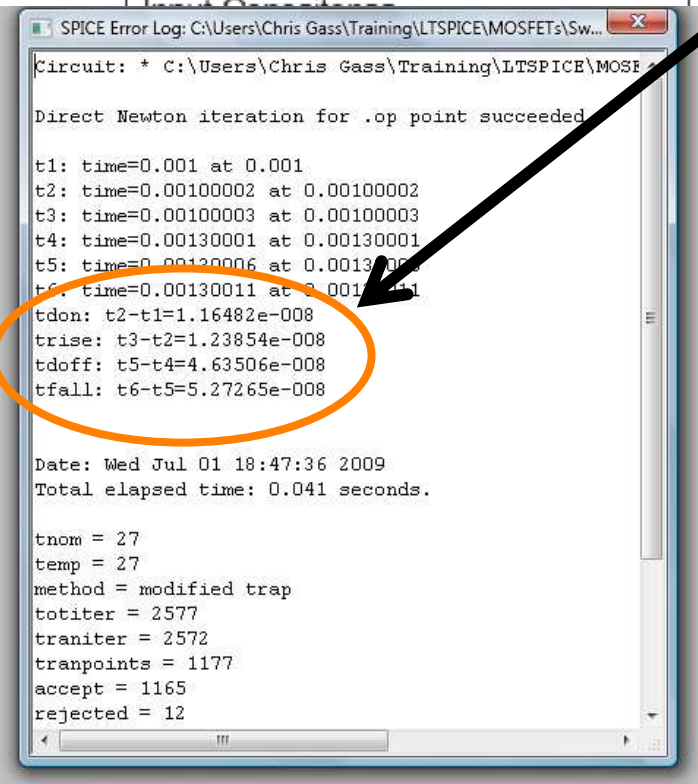
Switching Speed Model Validation
Rise Time

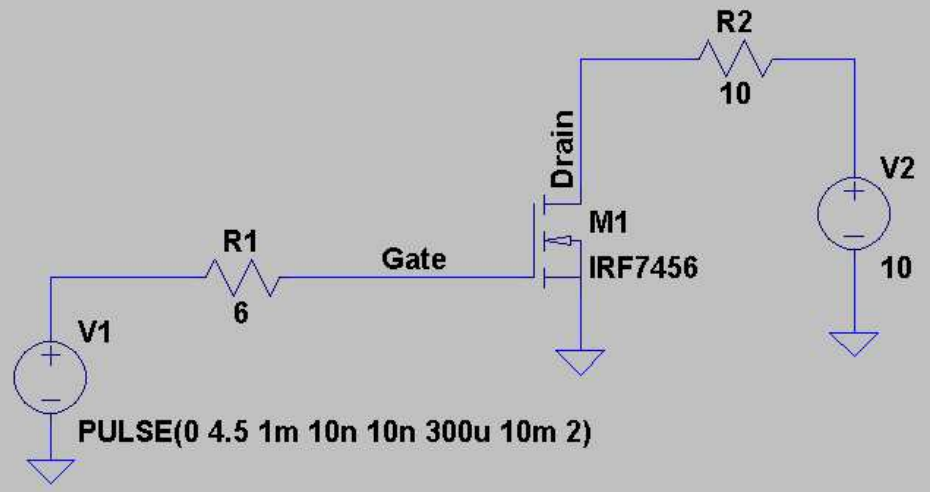
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	V_{DD} = 10V
t_r	Rise Time	—	25	—		I_D = 1.0A
$t_{d(off)}$	Turn-Off Delay Time	—	50	—		R_G = 6.0Ω
t_f	Fall Time	—	52	—		V_{GS} = 4.5V ③



Switching Speed Model Validation

$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	V_{DD} = 10V
t_r	Rise Time	—	25	—		I_D = 1.0A
$t_{d(off)}$	Turn-Off Delay Time	—	50	—		R_G = 6.0Ω
t_f	Fall Time	—	52	—		V_{GS} = 4.5V ③





.measure t1 find time when V(Gate)=0.45 rise=1
.measure t2 find time when V(Drain)=9 fall=1
.measure t3 find time when V(Drain)=1 fall=1
.measure t4 find time when V(Gate)=4.05 fall=1
.measure t5 find time when V(Drain)=1 rise=1
.measure t6 find time when V(Drain)=9 rise=1

.tran 15m

.measure tdon param t2-t1
.measure trise param t3-t2
.measure tdoff param t5-t4
.measure tfall param t6-t5

Ready

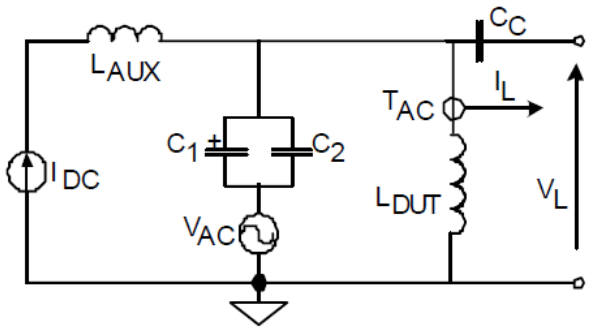
Conclusions

- Creating your own model takes a little time
- Requires a spice model and datasheet from the manufacturer
- Must use common sense as you review the information provided
- Review performance of new device. Some iteration may be required.

Modeling Coil Saturation

Modeling Coil Saturation

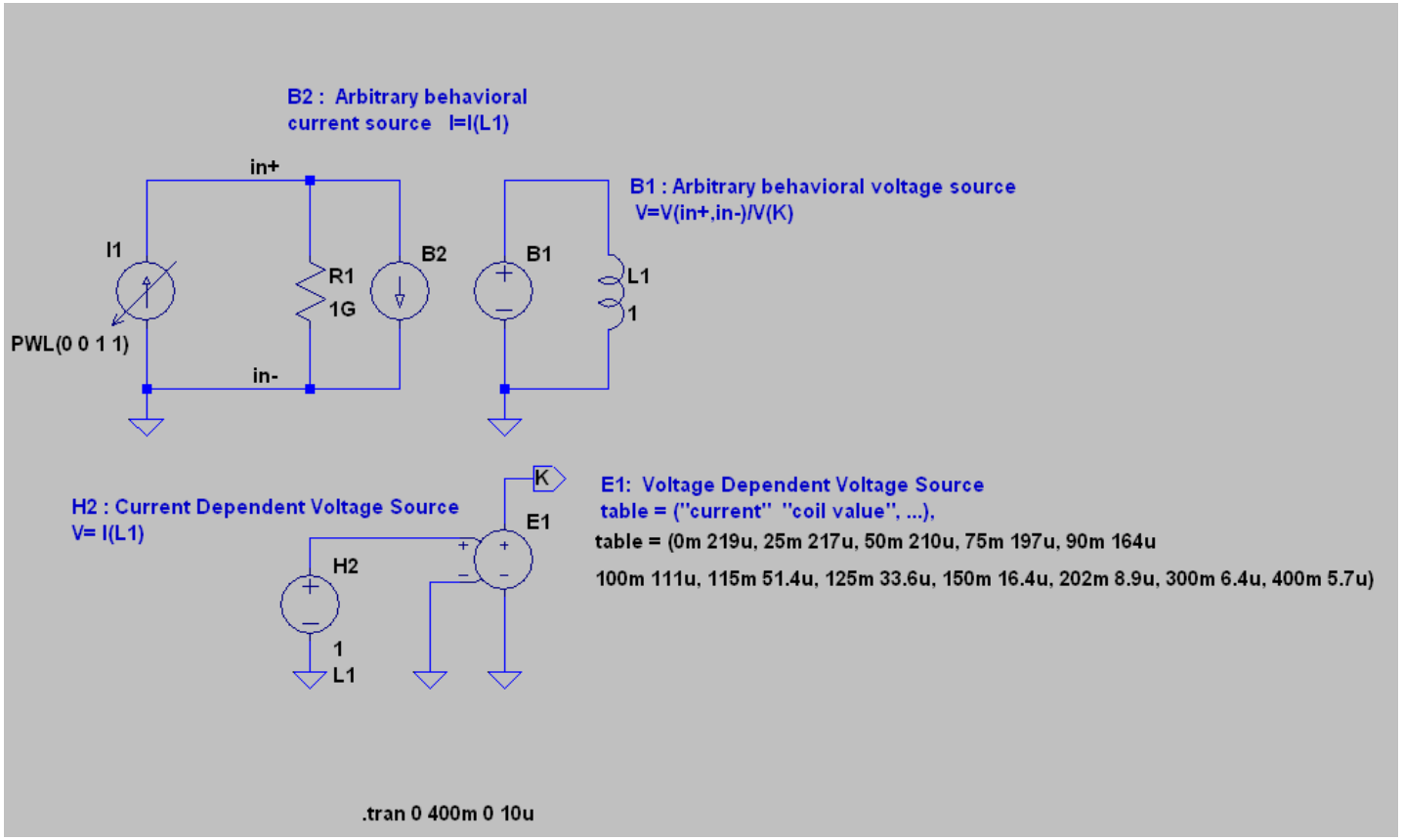
- First, characterize the saturation curve of the physical coil in the lab



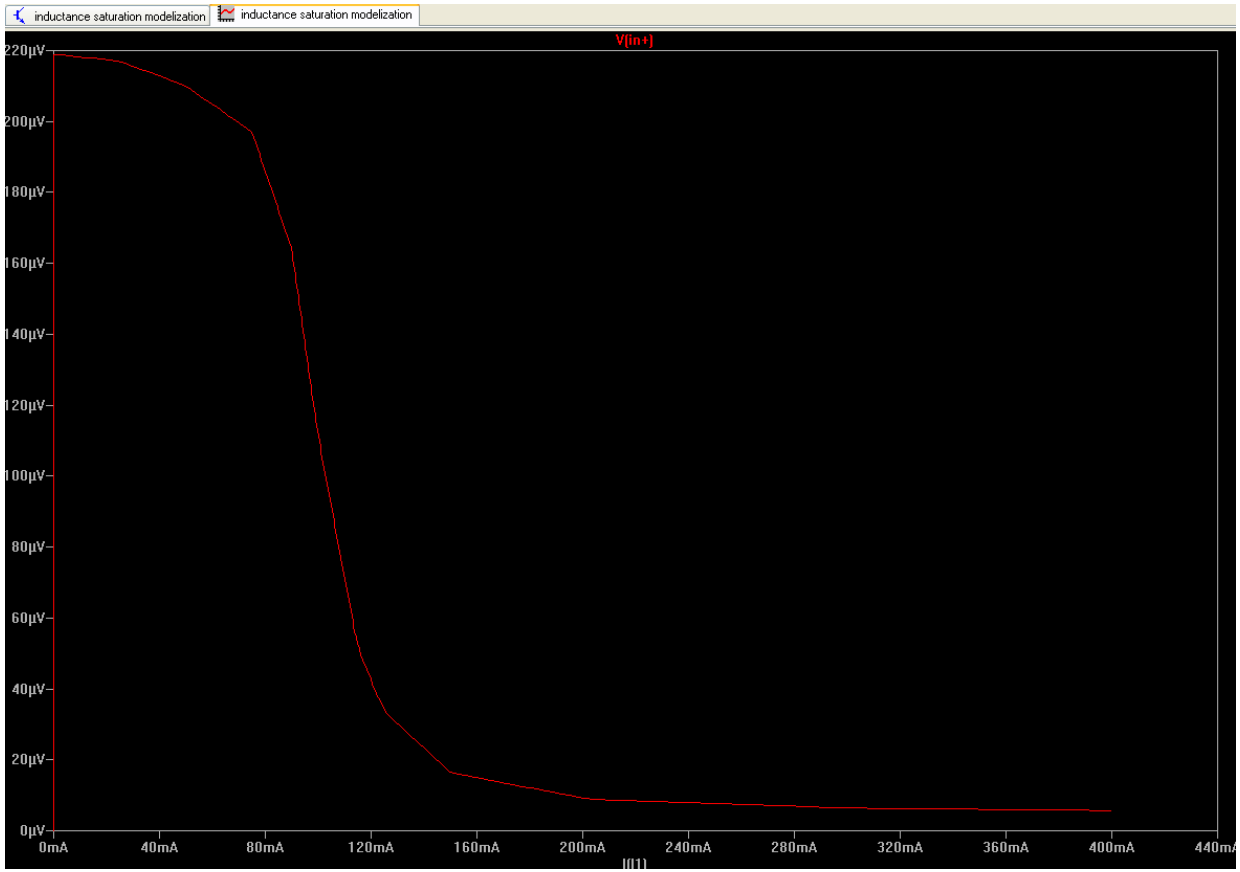
Nota : you can use a RLC meter if available!

- Use “Voltage Dependent Voltage Source” or “Voltage Dependent Current Source” in order to model the coil saturation curve using the look up table capability of these behavioral sources
- A look-up table is used to specify the transfer function. The table is a list of pairs of numbers. The second value of the pair is the output voltage when the control voltage is equal to the first value of that pair. The output is linearly interpolated when the control voltage is between specified points. If the control voltage is beyond the range of the look-up table, the output voltage is extrapolated as a constant voltage of the last point of the look-up table.

Modeling Coil Saturation

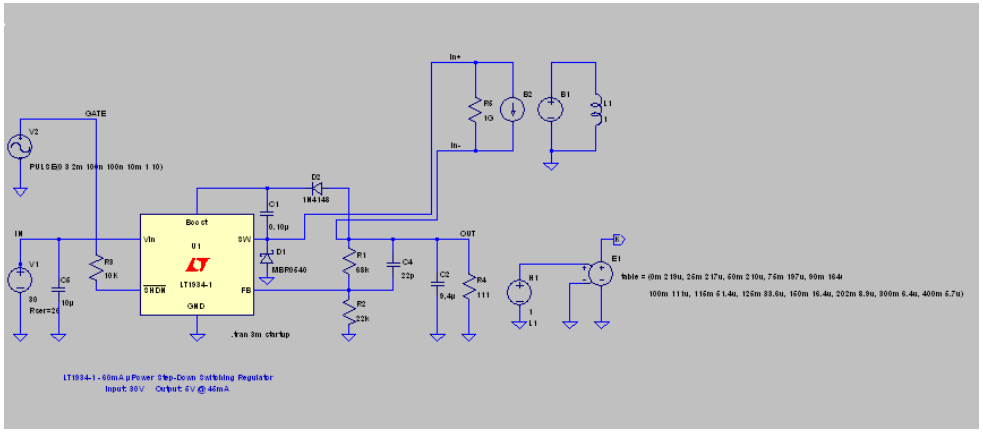


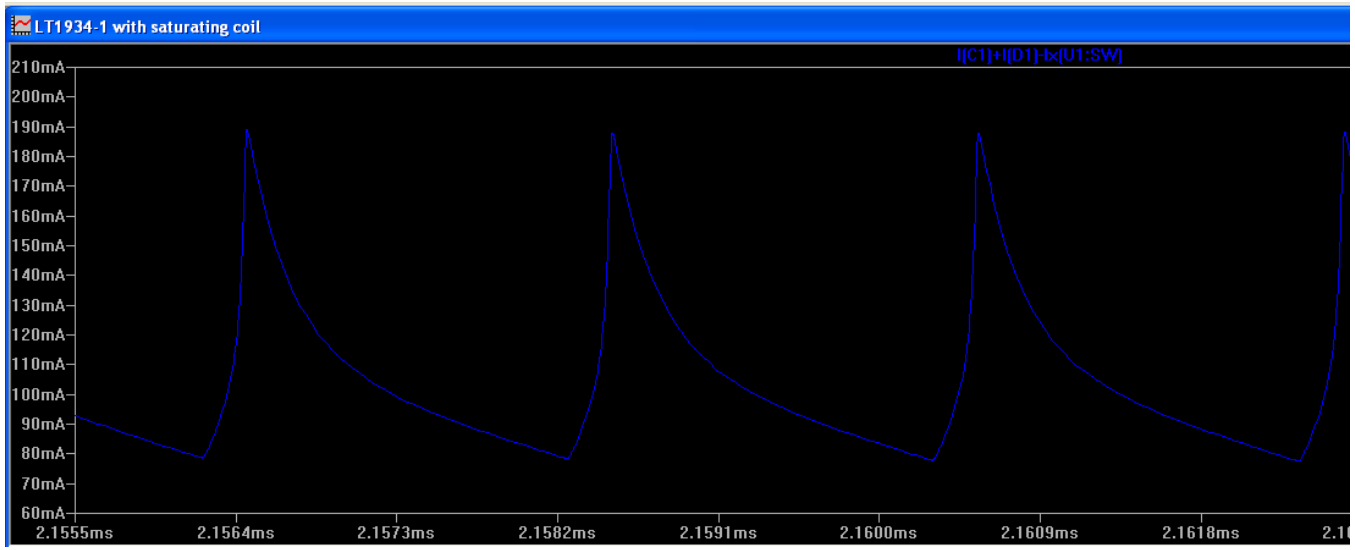
Modeling Coil Saturation



Plotting V(in+) vs. I(I1) to check the model !

Modeling Coil Saturation





Variable Capacitor vs. Voltage ...