Housekeeping and PCB Design: Let's Draw Some Parallels

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A year-long wave of home improvement is sweeping across my neighborhood; quite likely, yours too. People are doing yard projects and discarding clutter as we find ourselves at home more. Cleaning up my act includes buying a pressure washer and some accessories. Before I pointed the high-pressure stream at my walls and walkways, I wanted to learn all I could first.

One of the things I learned is that using an extra length of high-pressure hose along with an extended wand will keep the job going because I'm not having to move the machine as often. The other part of the deal is that the extra length reduces the maximum water pressure that the unit can deliver.

The 2500 PSI from the pump is like the voltage. The 1.5 gallons of water per minute through the high-pressure hose is the current. Together, they multiply out to the wattage that determines the actual cleaning power once we account for pressure drop through the whole system.

There are parameters for the minimum pressure and maximum temperature of the incoming water so the compressor has a long life. A tight bend in any of the hoses is to be avoided. You also have to be aware of the surface being cleaned and use the correct tip in order to regulate the out-going water pressure. Be careful about where you point that thing!

Just like that, our printed circuit boards also trade convenience for performance when it comes to the length of the transmission lines. The additional trace length is lossy. Not only that, but the signal is also likely to degrade over the longer trace because there are more attack surfaces where a noise generator can couple onto the signal. We have to work within the available geometry while leaving us with endless options.

Air gaps and Copper Thickness are Interrelated

That got me thinking about the other trade-offs we have to manage when it comes to designing a PCB. The one that comes to mind first is that boards that see a lot of current will benefit from having thick layers of copper to handle the power. Meanwhile, we also like to use narrow traces and pack them together to escape from the inner regions of the larger devices.

It becomes a balancing act to get the right stack-up that allows some fine-pitch connections along with some high current applications. The **design rules for this type of set-up will allow for small air-gaps on signal layers** while others have a more generous spacing rule set to supply power.

Those two things do not make good neighbors so we need other layers to act as a barrier. Adding layers add cost so we have to make the most of the layers we have available. There are cases where the fine-pitch rules only apply in a localized area. Once free of the connector or processor, a more conservative set of rules will apply. Dialing in this process is a balancing act.

What About Component Placement?

We know that small form factors are preferred. That's where those highly integrated circuits come in. A "do-it-all" system on a chip (SOC) will actually have hundreds of passive parts and perhaps, dozens of additional integrated circuits to actually create a system. Most of those additional circuits want to be as close as possible to the SOC.

All of the memory and high speed links want a seat at the table. There may be enough power supplies required to warrant a special power management integrated circuit or PMIC for short. Of course, any analog lines should be short and straight out of the SOC. Why are none of these functions on the SOC in the first place?

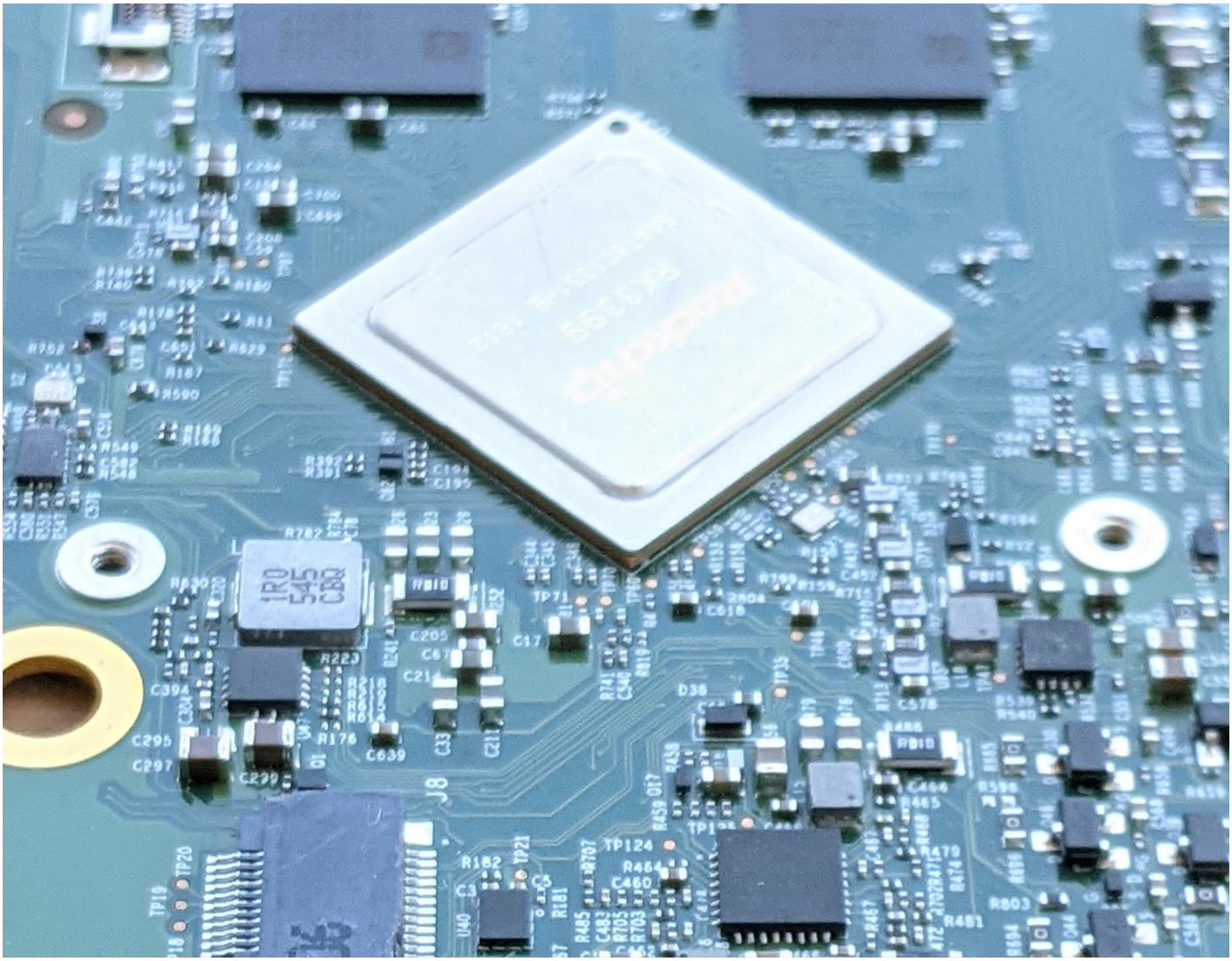

Figure 1. Image Credit: Author - Six-Layer Boards may cost less but some routing space will have to be allocated to the outer layers.

It comes down to chip architecture. Memory cells are huge relative to the virtually invisible transistor gates that make up most of the real estate of the SOC. Analog is a different beast that is good at picking up any noise. Which leads to the power supply silicon. That stuff has to live in its own package simply because it’s such a noise maker by design.

Nevertheless, the area around a computing device is a hot commodity. I mean that in the literal sense. The more space you can put around it the better. That files in the face of the requirement for a small form factor. We want to have our parts close together and separated at the same time.

All of these competing factors lead to strategic clustering, typically breaking things down by their voltage with secondary emphasis on their routing. We also take thermal and electromagnetic interference into account during the balancing act of PCB component placement. If we can spread things out a bit further, then we can increase our test access. Meanwhile, it would be nice if we could compress the whole board to make room for a bigger battery in a smaller enclosure than last year’s product.

Trade-Offs in Routing a Printed Circuit Board

So, routing is a function of the placement which is a function of several factors as mentioned above. Some of those factors are in direct competition with each other. The overlapping nuances are hard to predict even with the best simulations. Perfection is out of reach so what we’re looking for is good enough. If it functions reliably for as long as the warranty lasts, then we’ve done our jobs.

Given a long enough runway, we could theoretically approach a perfect memory bus that uses the minimum of meanders and a minimum of space while maintaining optimum separation for all of the various connections. The timing budget could be set to a vanishingly small amount of allowable skew. The thing is that time is nearly always in short supply so we need all of the latitude that the signals can handle.

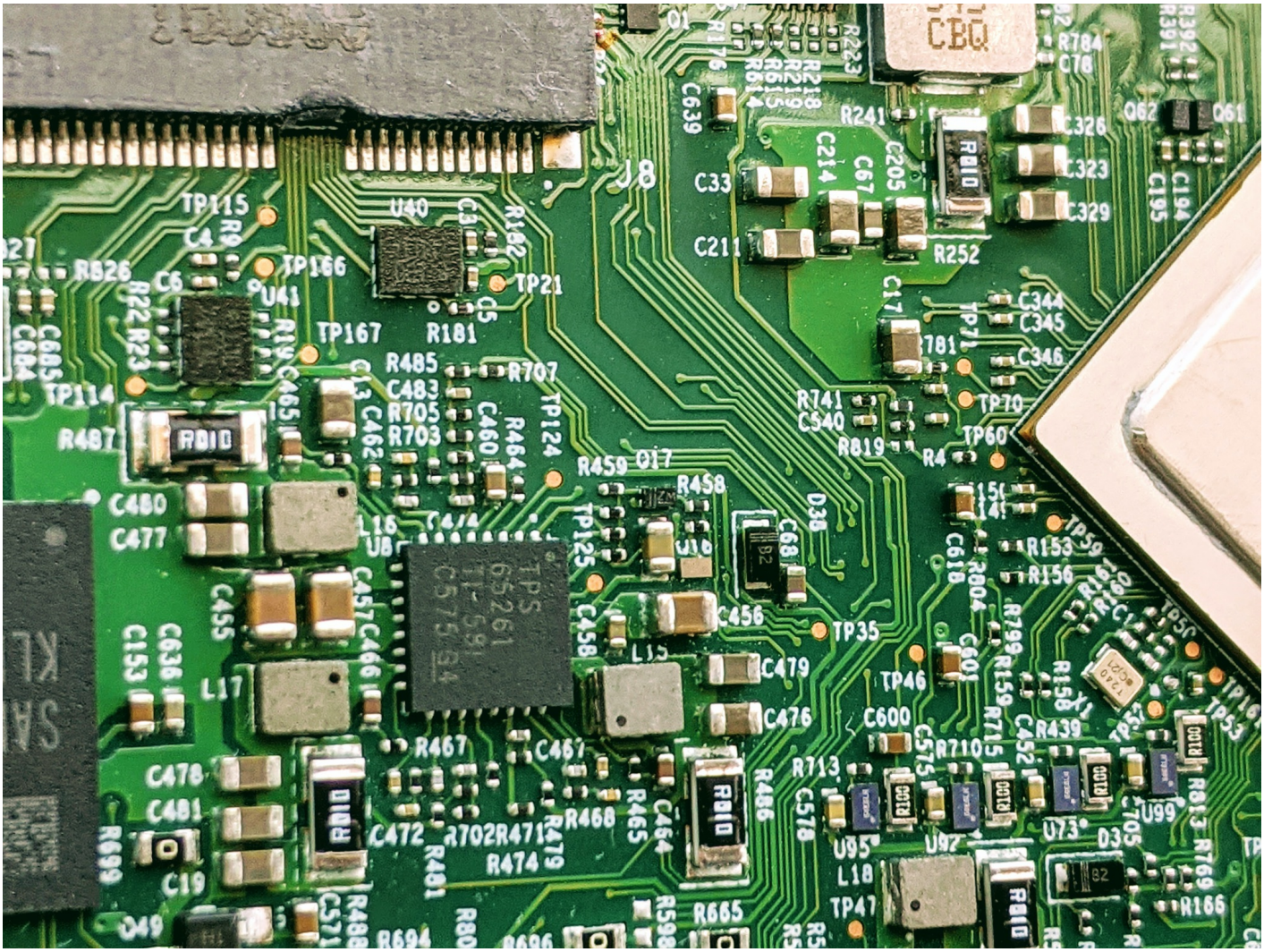

Figure 2. Image Credit: Author: Using outer layers for routing may not require as many vias but the traces are exposed which eats into the placement area.

It seems to be impossible to make everyone happy. By everyone, I include not just the in-house team but also each vendor who supplies a reference design built around their chip as if it were going to be the only thing on the board. The Marketing team would like it ready for CIS or back-to-school, maybe some other date. Now, the customer wants samples next week. How do we juggle all of these competing interests?

You know where this is going. The board designer incorporates every requirement to the extent that the time and space is available. The first revision comes out and we learn about problems that nobody could have imagined. Late nights lead to breakthroughs that almost always lead to solutions involving more parts on the next iteration of the board.

Your job becomes an all-out effort to make those new parts look like they were always meant to be there in terms of both **placement and routing**. It's not so much about looking good. The elegance is in performing. Seeing that kind of beauty takes a trained eye. You can't power-wash your way to a clean layout. It quite often requires a compromise.