

# Diagram

**GPIO(PMOD X 4)**

**AUDIO**

**AD/DA**

**CAMERA**

**POWER**

**7-SEG DISPLAY x 6**

**HDMI**

**BUTTON X7**

**SWITCH x 8**

**LED X 8**

**USB PHY x2**

**I2C EEPROM**

**ALTERA**

**TFT LCD**

**USB 2 UART**

**USB (MS & KBD)**

**SRAM (256K X2)**

**ETHERNET(1G)**

**FPGA & RISC-V JTAG**

**OSC\_50M, 32.768K**

**FLASH**

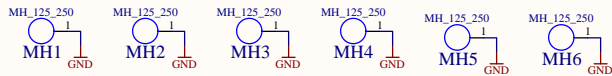
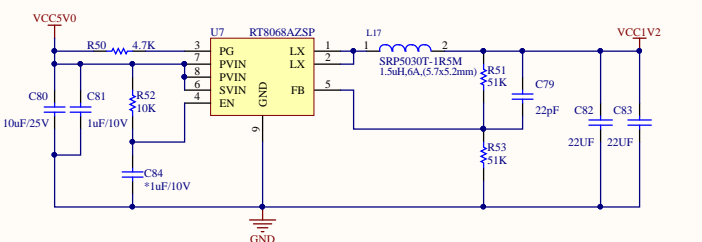
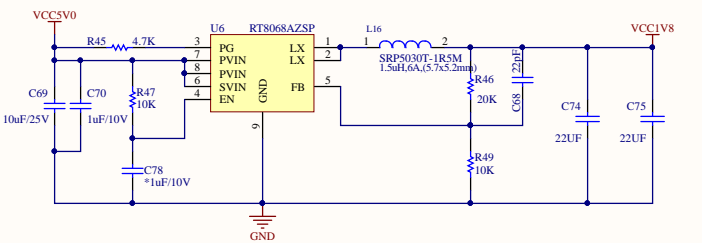
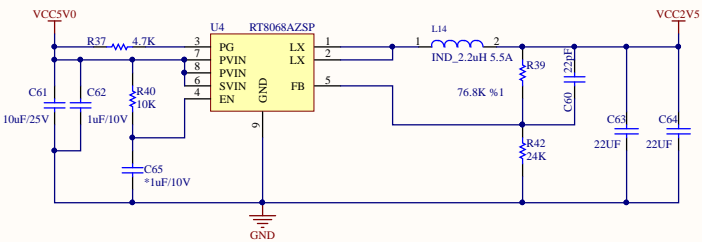
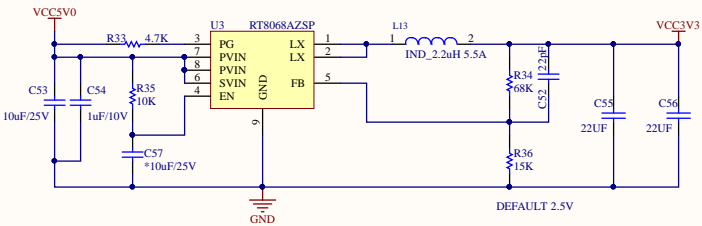
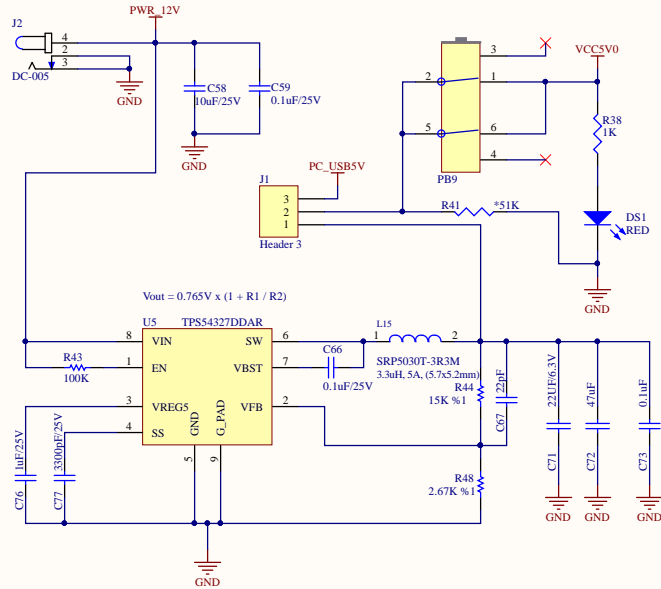
**CYCLONE 10 LP**

## IIC Addressing

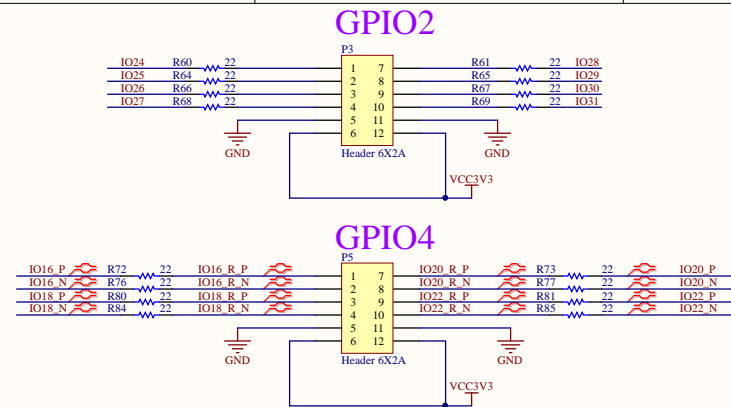
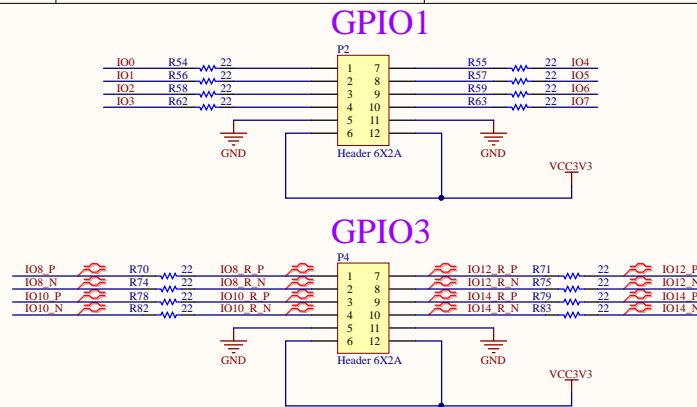
8'B1001000X	PCF8591T
8'B0111001X	HDMI
8'B1010100X	IIC EEPROM
8'B0011010X	WM8978

Company: FII		Title: DIAGRAM		of PRA040	
Date: 2019-07-20	Time 3:21:57 PM		Engineer: RJ WG		Size: A4
Revision: V3.0		Sheet 1 of 21			

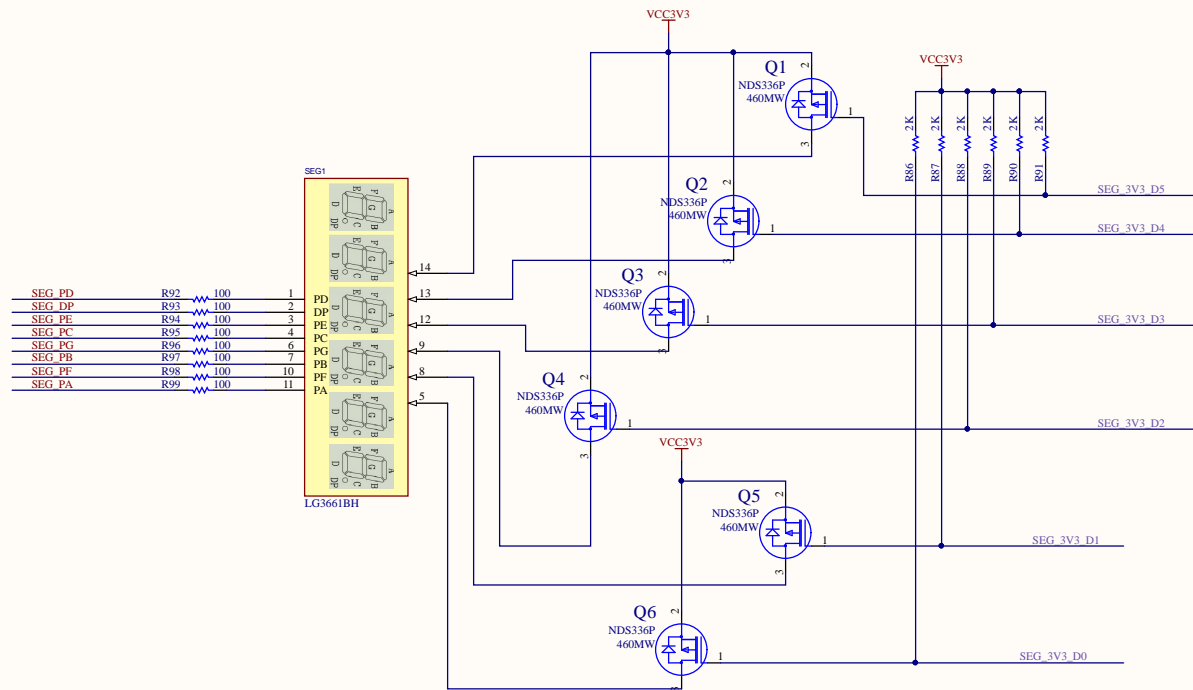
Power



## GPIO

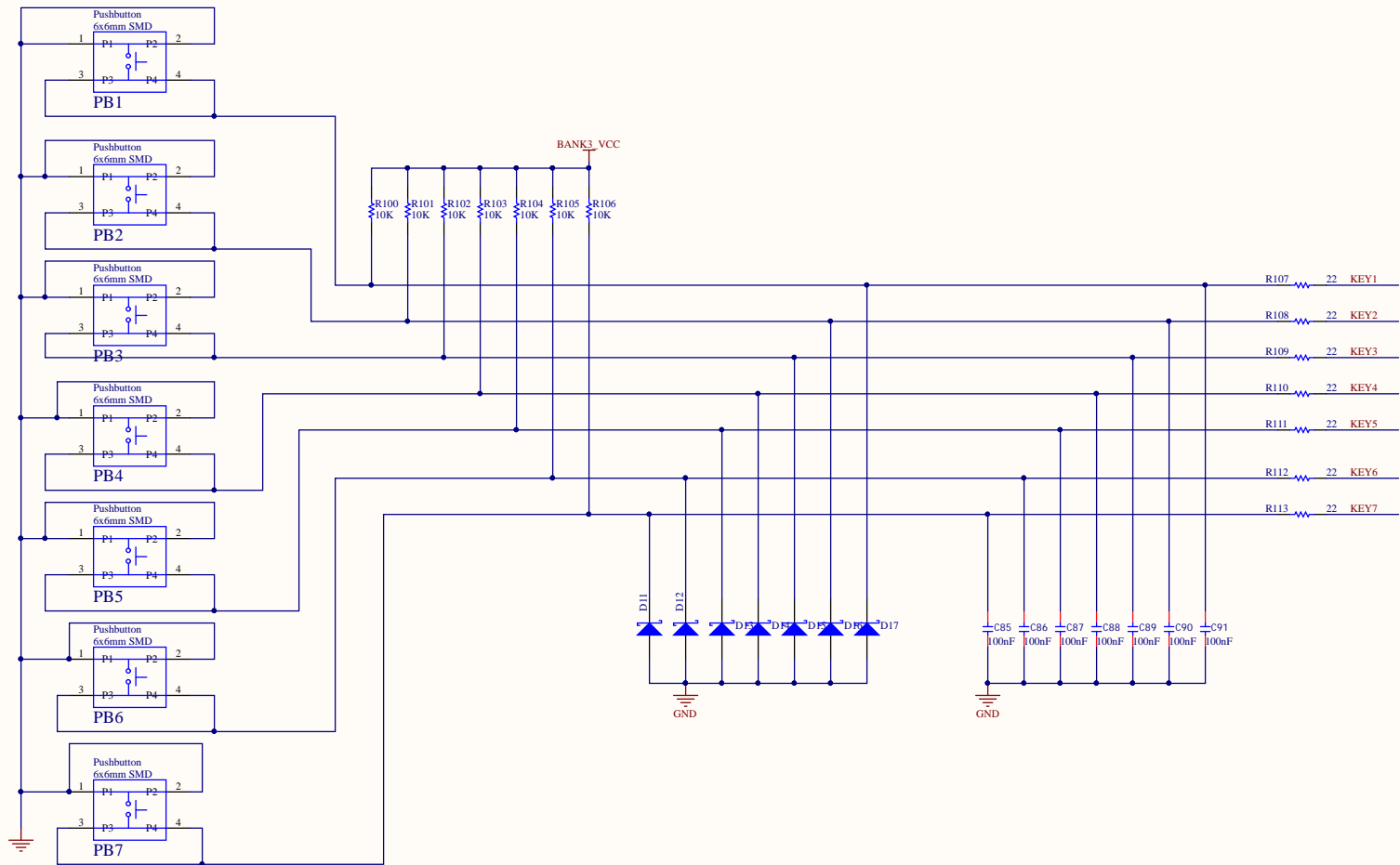


## SEG

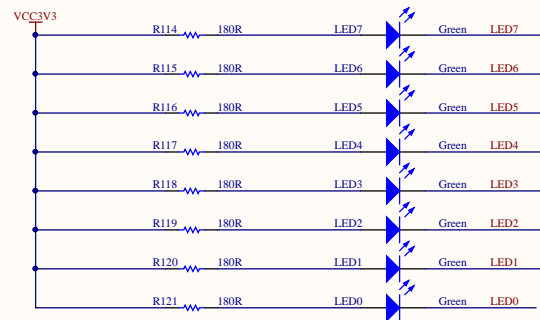


Company: <b>FII</b>		Title: <b>SEG_GPIO</b> of <b>PRA040</b>	
Date: <b>2019-07-20</b>	Time <b>3:21:57 PM</b>	Engineer: <b>RJ WG</b>	Size:
Revision: <b>V3.0</b>	Sheet <b>3</b> of <b>21</b>	<b>B+</b>	

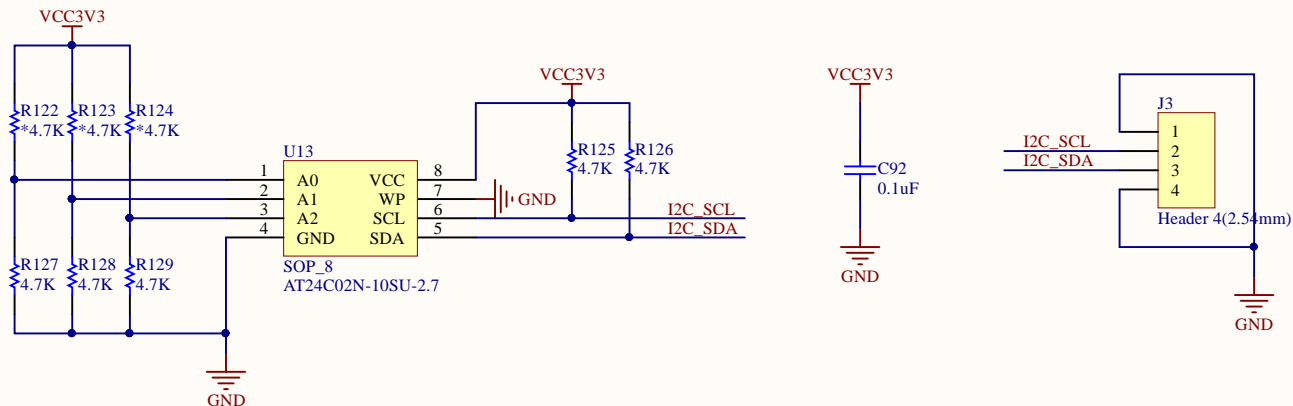
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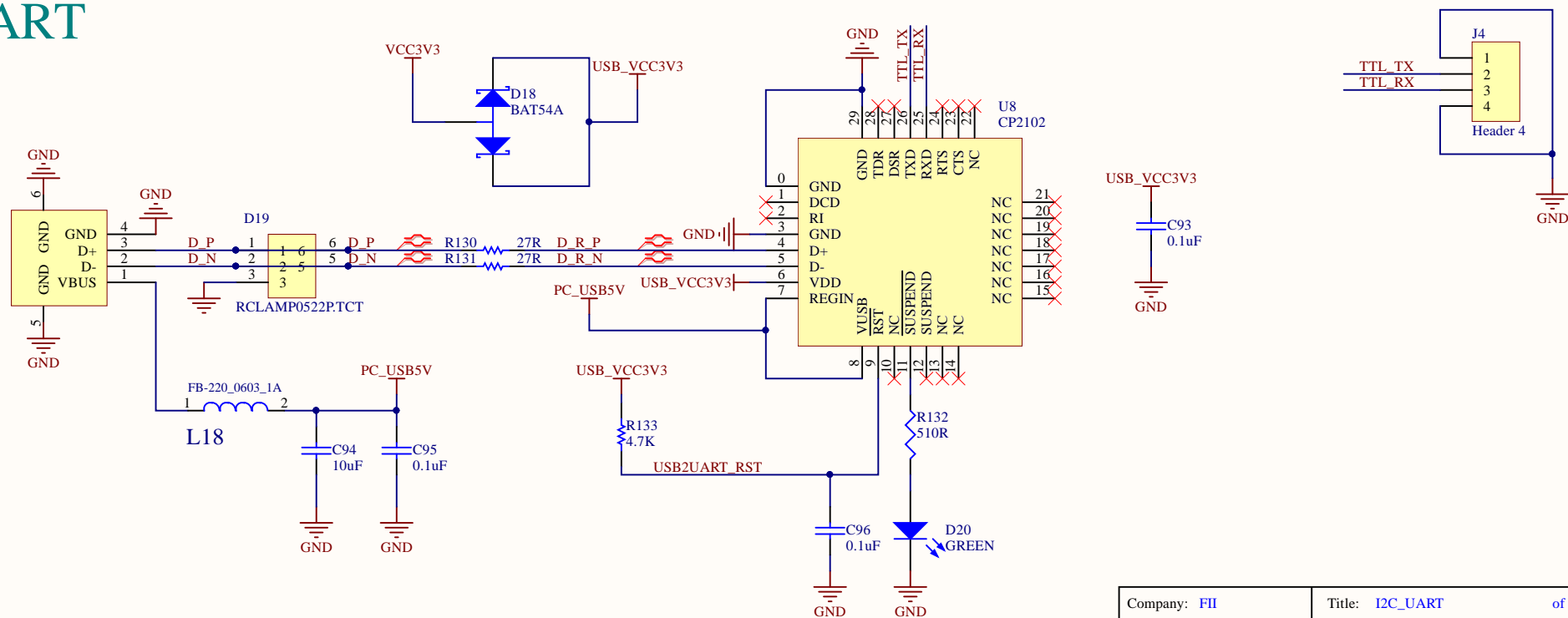
# LED



# I2C

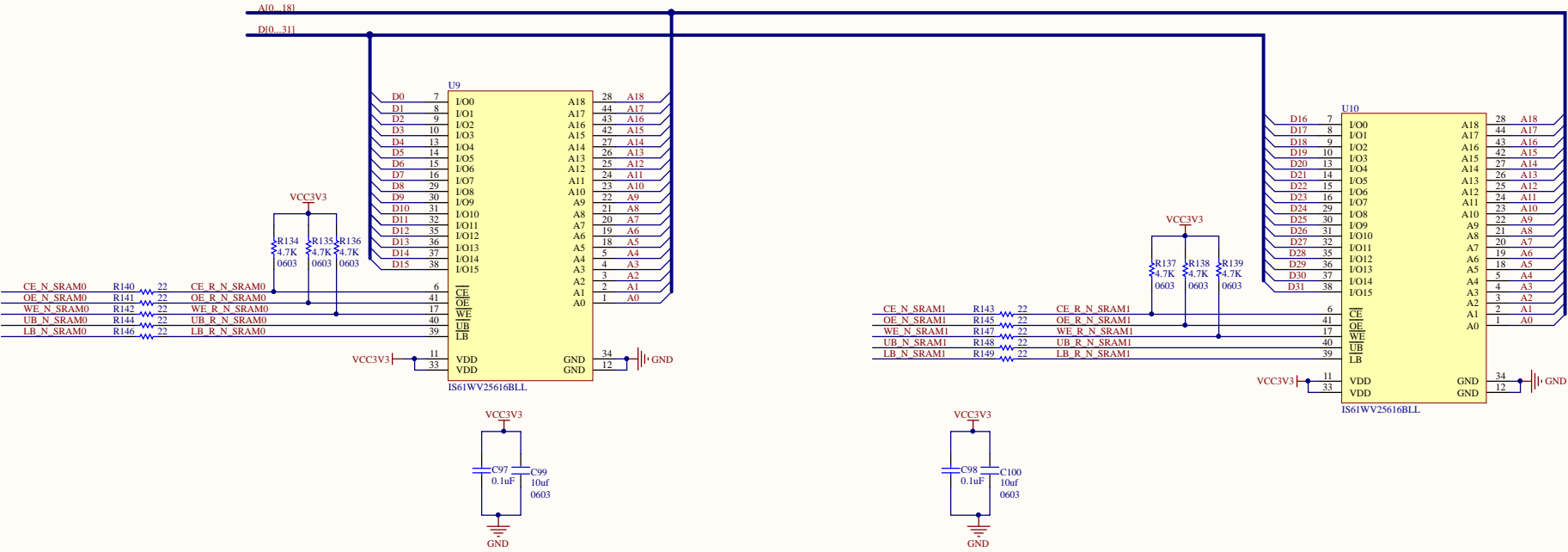


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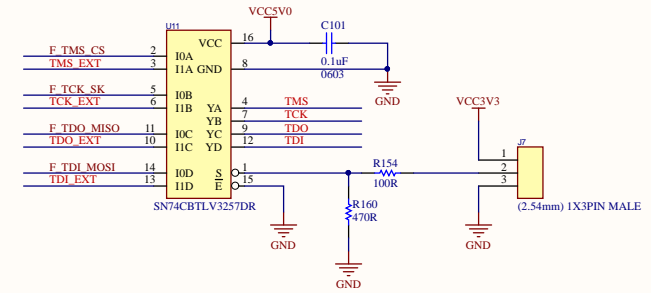
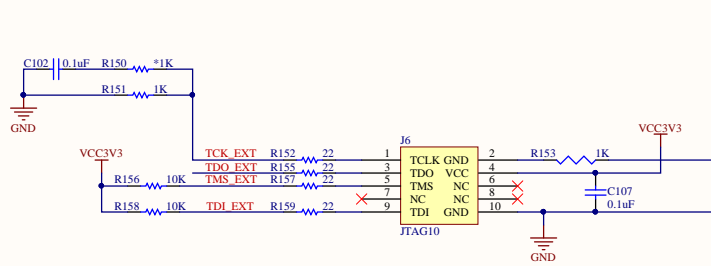


Company: FII	Title: I2C_UART	of PRA040
Date: 2019-07-20	Time 3:21:57 PM	Engineer: RJWG
Revision: V3.0	Sheet 5 of 21	Size: A4

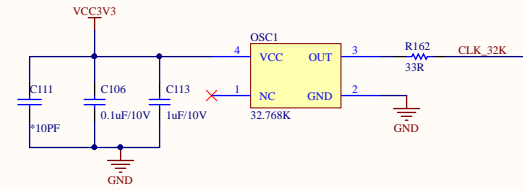
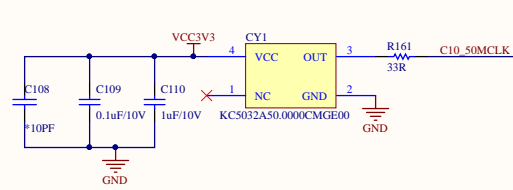
SRAM



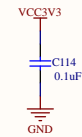
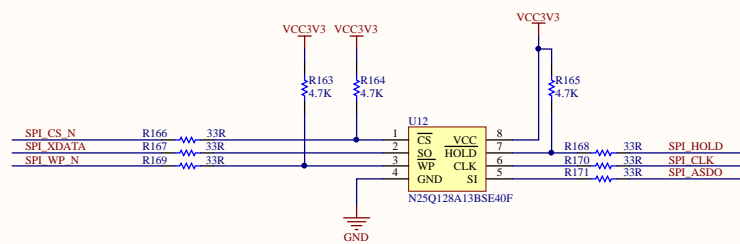
## JTAG



## XTAL



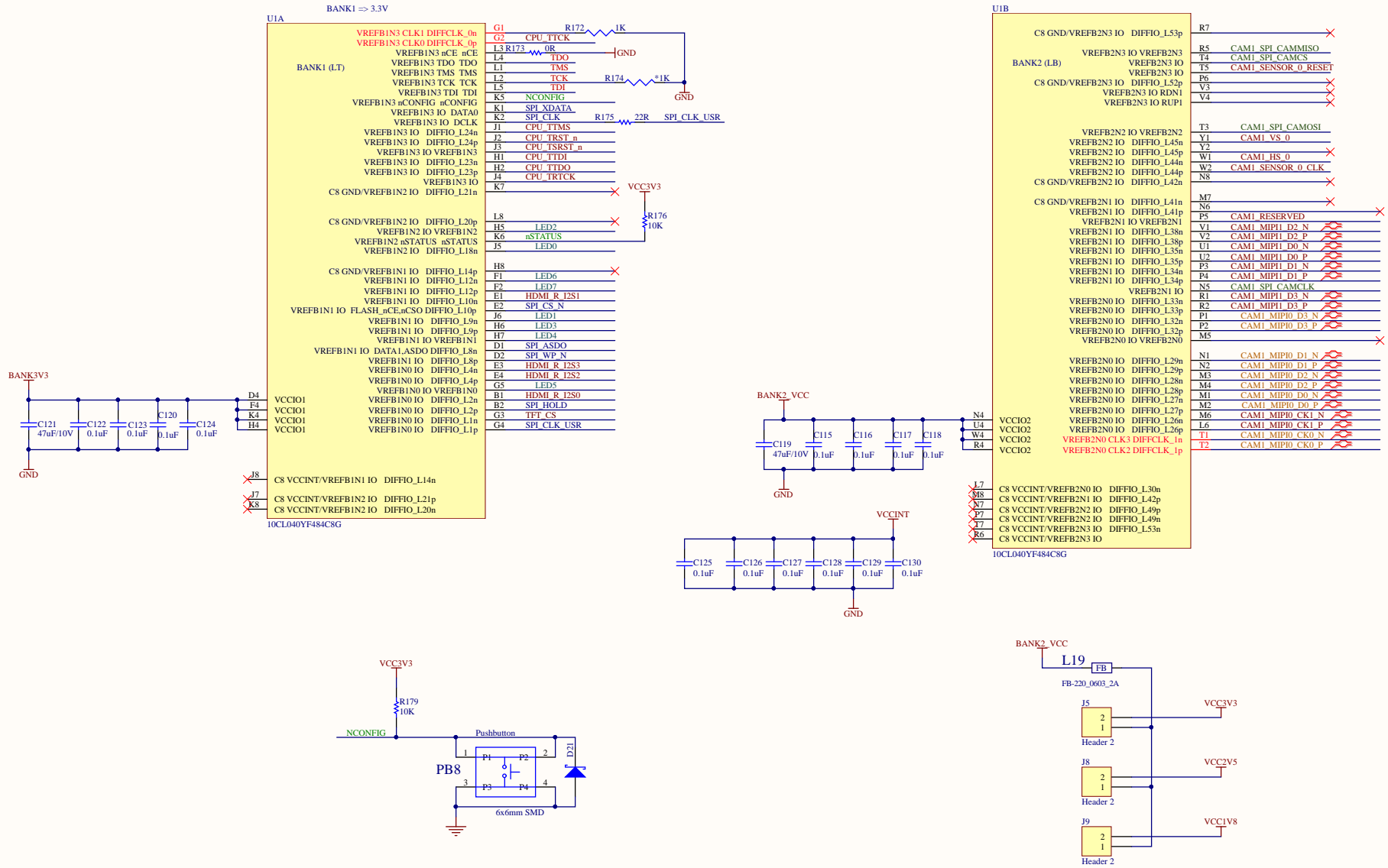
## FLASH



Company: <b>FII</b>		Title: <b>JTAG_OSC_FLASH</b> of <b>PRA040</b>	
Date: <b>2019-07-20</b>	Time <b>3:21:58 PM</b>	Engineer: <b>RJ WG</b>	Size:
Revision: <b>V3.0</b>	Sheet <b>7</b> of <b>21</b>	<b>B+</b>	

## BANK1\_2

BANK2 => 1.8/2.5/3.3V

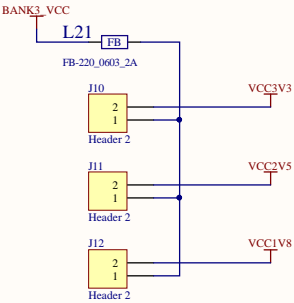
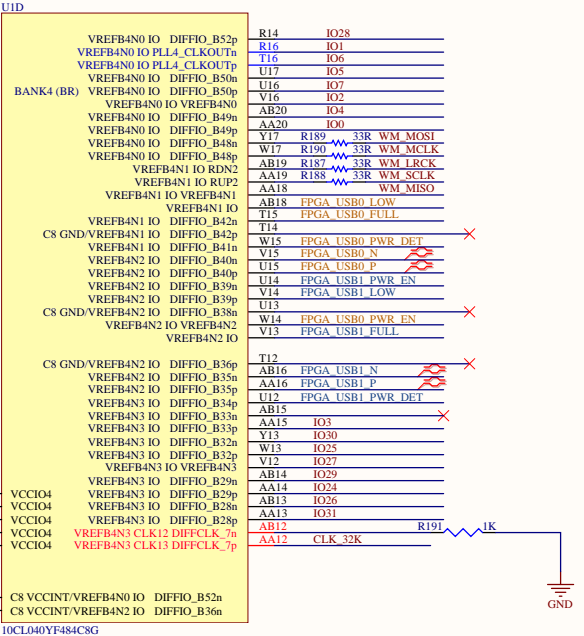
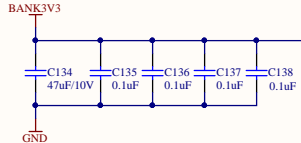
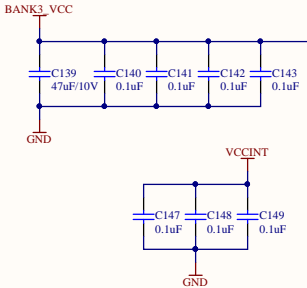
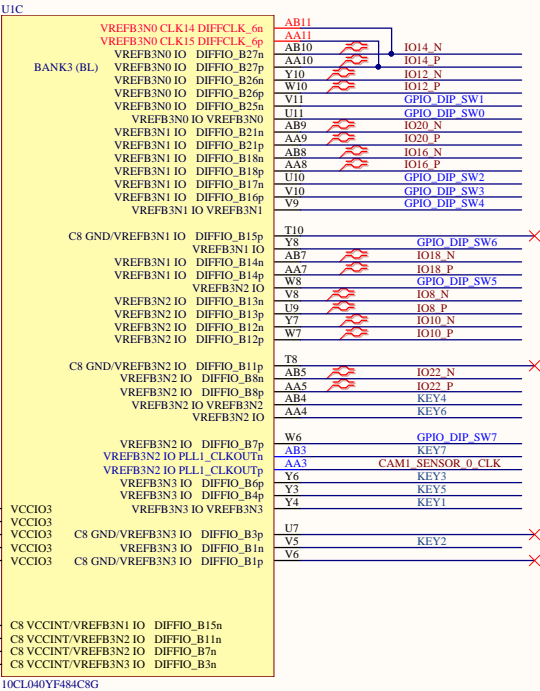




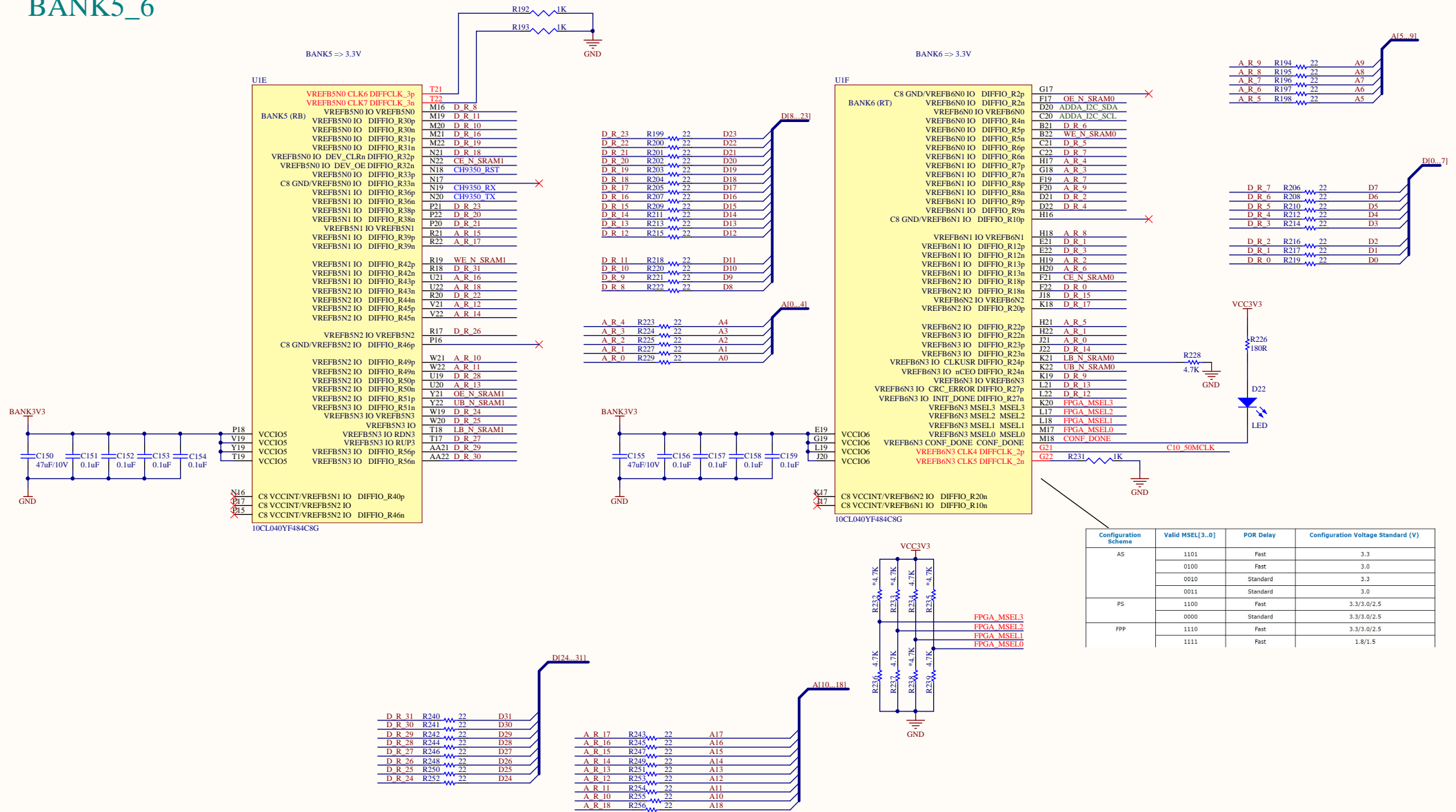
BANK3\_4

BANK3 => 1.8/2.5/3.3V

BANK4 => 3.3V



# BANK5\_6



# BANK\_7\_8

BANK7 => 3.3V

U1G

BANK7 (TR)

VREFB7N3 CLK9 DIFFCLK\_5p  
VREFB7N3 CLK8 DIFFCLK\_5n  
VREFB7N3 IO DIFFIO\_T27p  
VREFB7N3 IO DIFFIO\_T27n  
VREFB7N3 IO DIFFIO\_T28p  
VREFB7N3 IO DIFFIO\_T28n  
VREFB7N3 IO DIFFIO\_T31p  
VREFB7N3 IO DIFFIO\_T31n  
VREFB7N3 IO VREFB7N3  
VREFB7N3 IO DIFFIO\_T35p  
VREFB7N3 IO DIFFIO\_T35n  
VREFB7N3 IO DIFFIO\_T36p  
VREFB7N2 IO DIFFIO\_T36n  
VREFB7N2 IO DIFFIO\_T37p  
VREFB7N2 IO DIFFIO\_T37n  
VREFB7N2 IO VREFB7N2  
VREFB7N2 IO DIFFIO\_T40p  
VREFB7N2 IO DIFFIO\_T40n  
VREFB7N2 IO DIFFIO\_T41p  
VREFB7N1 IO DIFFIO\_T41n  
C8 GND/VREFB7N1 IO DIFFIO\_T42n  
  
VREFB7N1 IO DIFFIO\_T44n  
VREFB7N1 IO VREFB7N1  
VREFB7N1 IO DIFFIO\_T45p  
VREFB7N1 IO DIFFIO\_T45n  
VREFB7N1 IO RDn4  
VREFB7N1 IO RUP4  
VREFB7N1 IO DIFFIO\_T46p  
VREFB7N1 IO PLL2\_CLKOUTp  
VREFB7N0 IO PLL2\_CLKOUTn  
VREFB7N0 IO DIFFIO\_T47p  
VREFB7N0 IO DIFFIO\_T47n  
VREFB7N0 IO VREFB7N0  
C8 GND/VREFB7N0 IO DIFFIO\_T48p  
VREFB7N0 IO DIFFIO\_T49p  
C8 GND/VREFB7N0 IO DIFFIO\_T49n  
VREFB7N0 IO DIFFIO\_T50n  
VREFB7N0 IO DIFFIO\_T51p  
C8 GND/VREFB7N0 IO DIFFIO\_T51n

B12 RGMII RXCK  
A12 SEG 3V3 D4  
E11 SEG PE  
E12 SEG 3V3 D5  
B13 RGMII RX0  
A13 RGMII RXCTL  
B14 RGMII RX2  
A14 RGMII RX1  
E13 SEG 3V3 D3  
D13 I2C\_SCL  
C13 I2C\_SDA  
B15 SEG PA  
A15 RGMII RX3  
E13 SEG PE  
E14 SEG PB  
C15 SEG PD  
B16 SEG PG  
A16 SEG DP  
B17 RGMII TX1  
A17 RGMII TX0  
G13

E15 SEG 3V3 D2  
D15 SEG PC  
B18 RGMII TX3  
A18 RGMII TX2  
A19 RGMII TXCTL  
B19 NPHY MDIO  
C17 NPHY MDC  
B20 RGMII TXCK  
A20 TPEN\_CS  
D19 SEG 3V3 D1  
C19 nRST\_RTL8211  
D17 ETH\_INT\_N  
H14  
F14 SEG 3V3 D0  
G15  
E15 TTL\_TX  
E16 TTL\_RX  
F16

10CL040YF48C8G

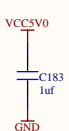
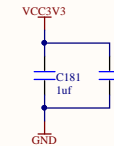
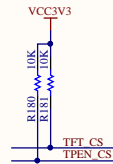
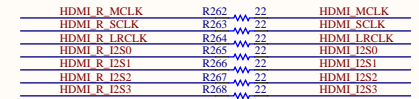
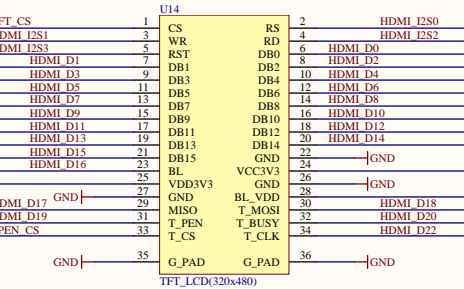
BANK8 => 3.3V

U1H

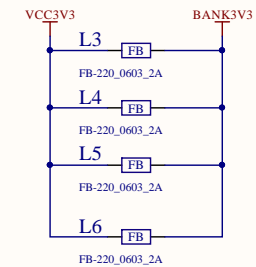
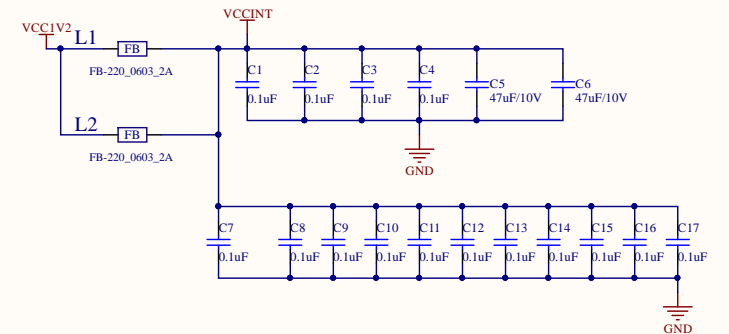
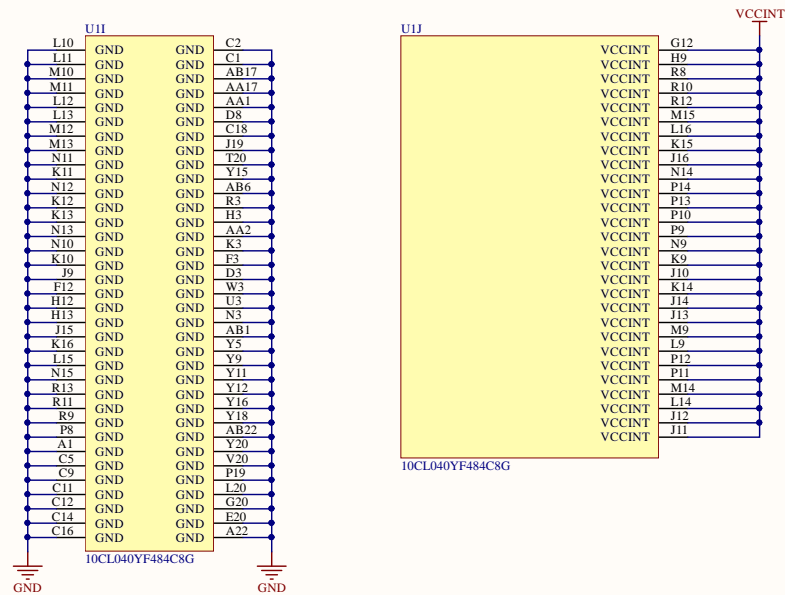
BANK8 (TL)

C8 GND/VREFB8N3 IO  
VREFB8N3 IO PLL3\_CLKOUTp  
VREFB8N3 IO PLL3\_CLKOUTn  
VREFB8N3 IO  
VREFB8N3 IO DIFFIO\_T1p  
VREFB8N3 IO DIFFIO\_T1n  
VREFB8N3 IO DIFFIO\_T3p  
VREFB8N3 IO DIFFIO\_T3n  
VREFB8N3 IO VREFB8N3  
VREFB8N3 IO DIFFIO\_T4p  
VREFB8N3 IO DIFFIO\_T4n  
VREFB8N3 IO DIFFIO\_T5n  
VREFB8N3 IO DIFFIO\_T6p  
VREFB8N2 IO DIFFIO\_T6n  
VREFB8N2 IO DIFFIO\_T7p  
VREFB8N2 IO DIFFIO\_T7n  
VREFB8N2 IO DATA7 DIFFIO\_T7n  
VREFB8N2 IO DATA6 DIFFIO\_T8p  
  
VREFB8N2 IO VREFB8N2  
VREFB8N2 IO DATA5 DIFFIO\_T11p  
C8 GND/VREFB8N1 IO DIFFIO\_T14p  
VREFB8N1 IO DIFFIO\_T16p  
VREFB8N1 IO DIFFIO\_T16n  
VREFB8N1 IO VREFB8N1  
VREFB8N1 IO DIFFIO\_T18p  
VREFB8N1 IO DIFFIO\_T18n  
VREFB8N1 IO DATA4 DIFFIO\_T19p  
VREFB8N1 IO DIFFIO\_T19n  
VREFB8N1 IO DATA3 DIFFIO\_T20p  
VREFB8N0 IO DATA2 DIFFIO\_T20n  
C8 GND/VREFB8N0 IO DIFFIO\_T22n  
VREFB8N0 IO VREFB8N0  
VREFB8N0 IO DIFFIO\_T24p  
VREFB8N0 IO DIFFIO\_T24n  
VREFB8N0 IO DIFFIO\_T25p  
VREFB8N0 IO DIFFIO\_T25n  
C8 GND/VREFB8N0 IO DIFFIO\_T26p  
VREFB8N0 IO DIFFIO\_T26n  
VREFB8N0 CLK11 DIFFCLK\_4p  
VREFB8N0 CLK10 DIFFCLK\_4n

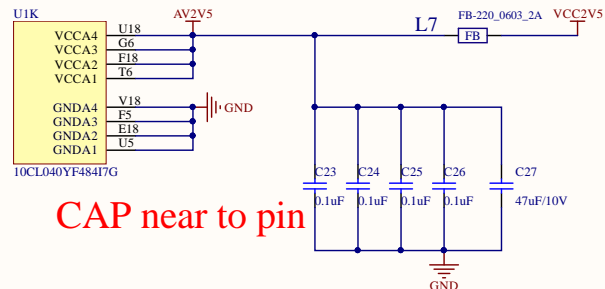
C8 VCCINT/VREFB8N1 IO DIFFIO\_T14n  
C8 VCCINT/VREFB8N2 IO DIFFIO\_T8n  
C8 VCCINT/VREFB8N3 IO DIFFIO\_T5p  
H11  
G10  
G8  
10CL040YF48C8G  
VREFB8N0 IO DIFFIO\_T48n  
VREFB8N0 IO DIFFIO\_T50p  
VREFB8N0 IO DIFFIO\_T44p



## FPGA\_POWER\_GND



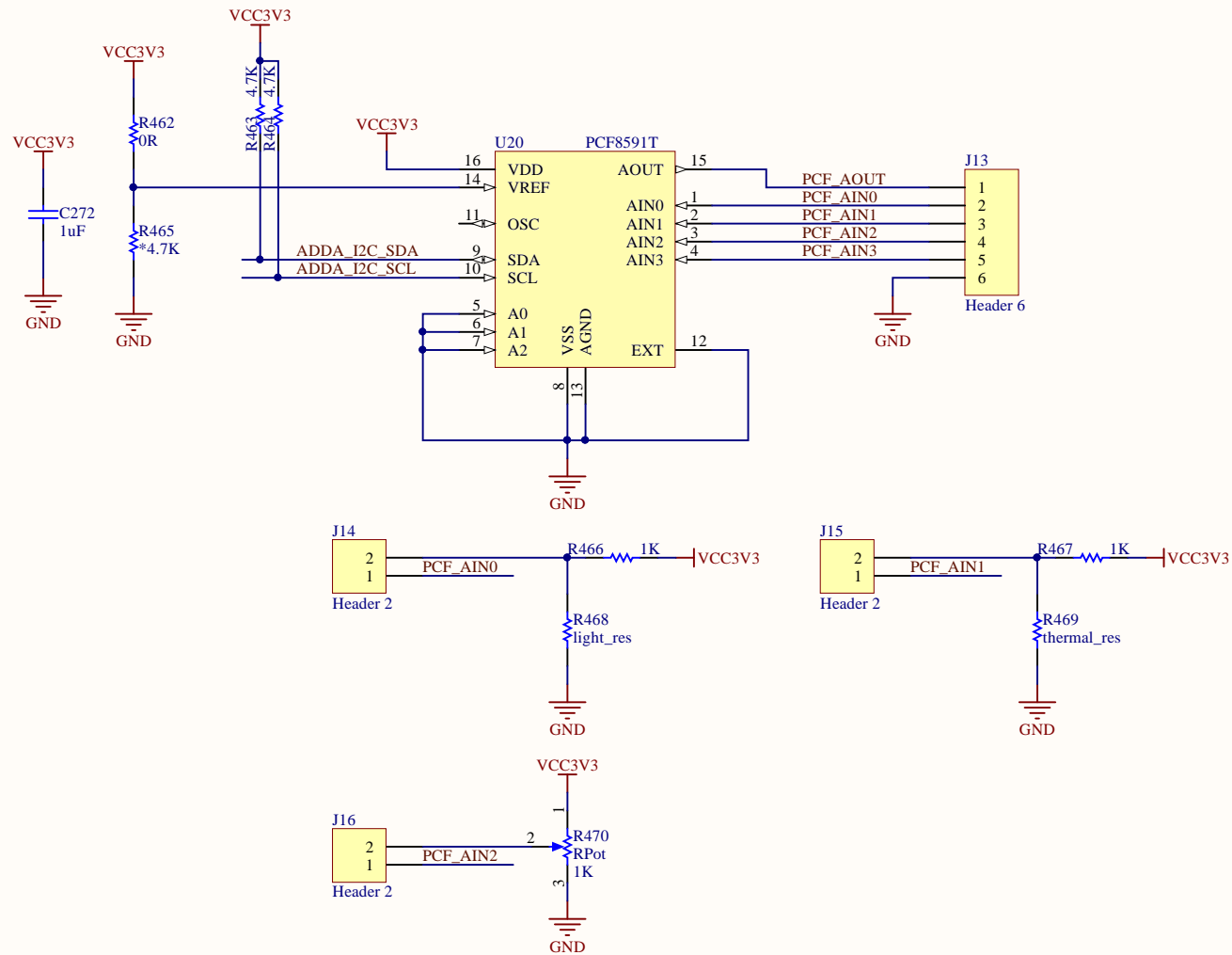
CAP near to pin



CAP near to pin

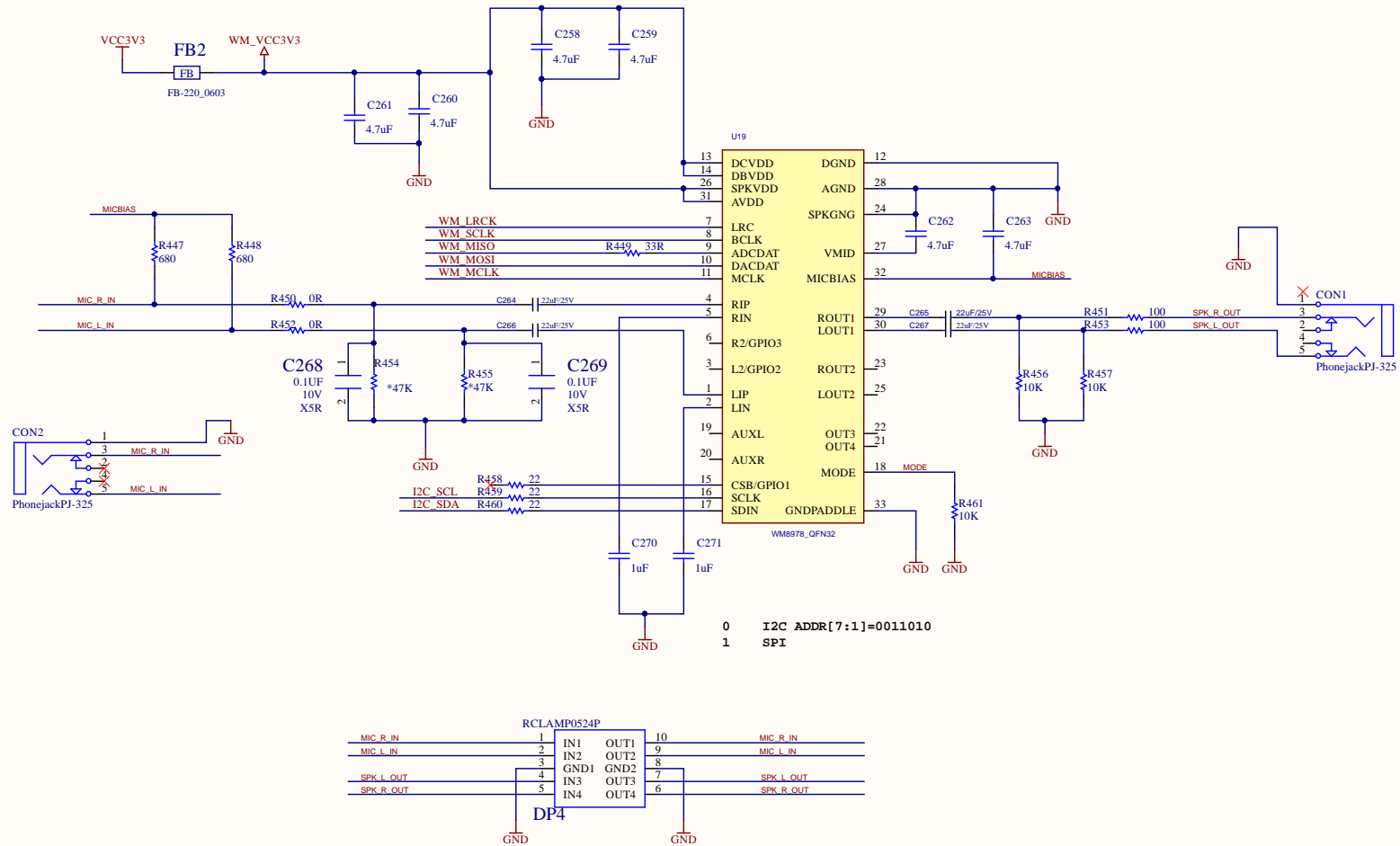
Company: FII		Title: FPGA_POWER_GND of PRA040	
Date: 2019-07-20	Time 3:21:59 PM	Engineer: RJ WG	Size: B
Revision: V3.0	Sheet 12	of 21	

# AD/DA

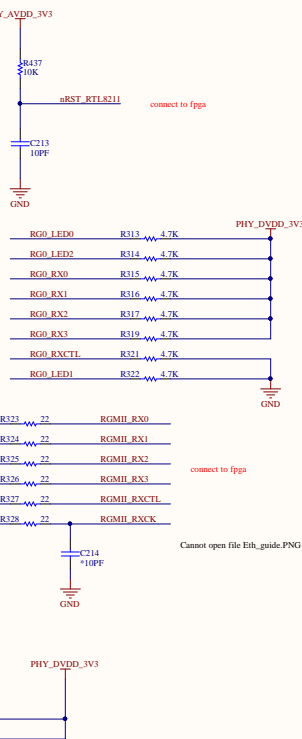
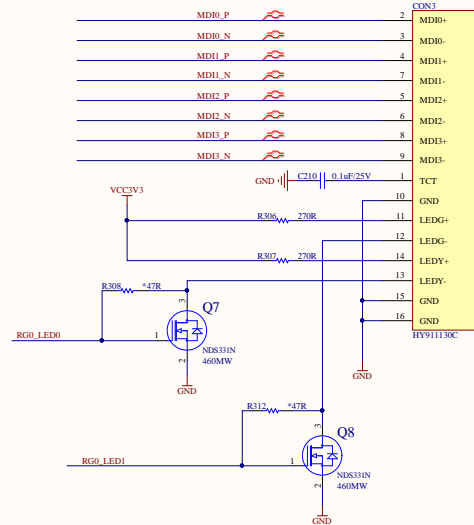
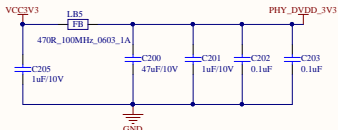


Company: FII	Title: AD_DA	of PRA040
Date: 2019-07-20	Time 3:21:59 PM	Engineer: RJ WG
Revision: V3.0	Sheet 13 of 21	Size: A4

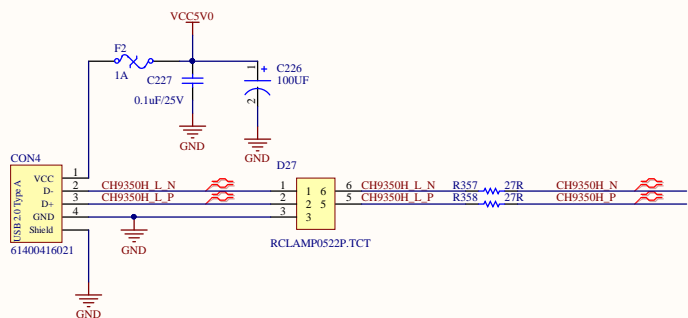
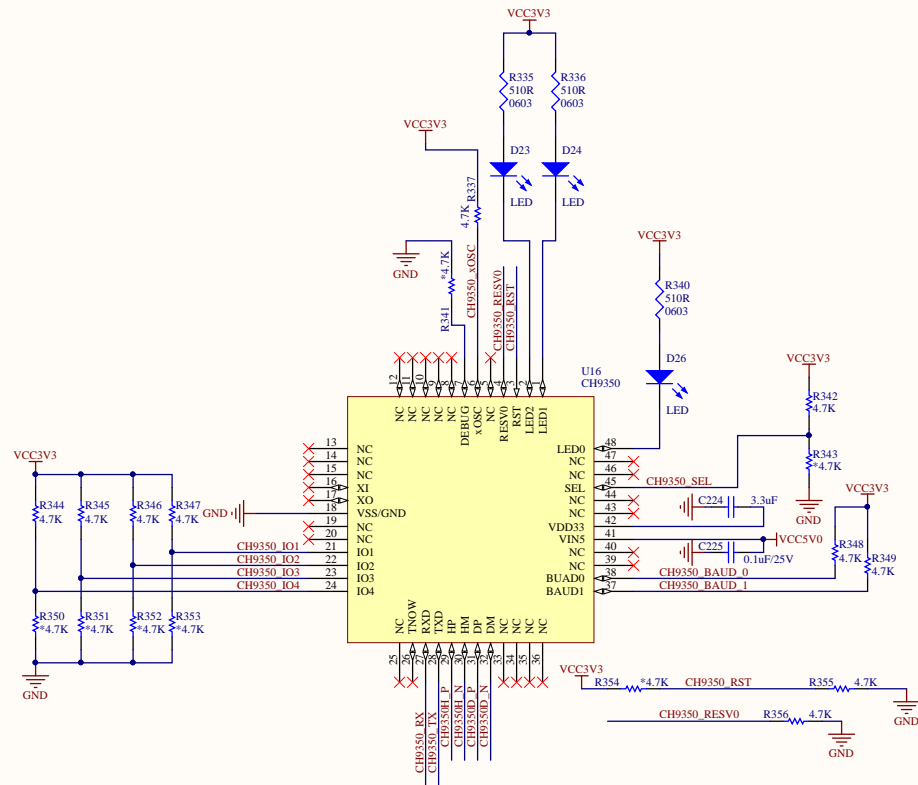
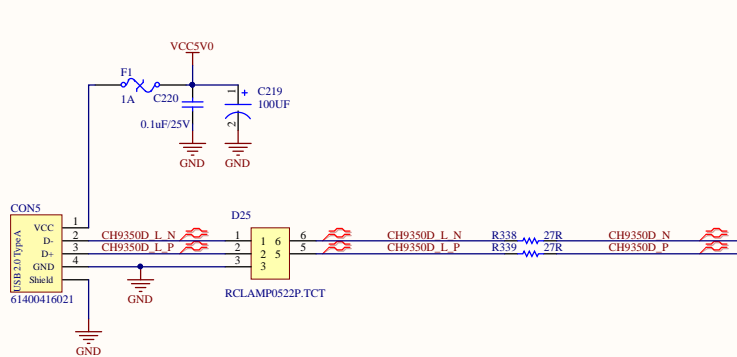
# AUDIO WM8978



# ETHERNET

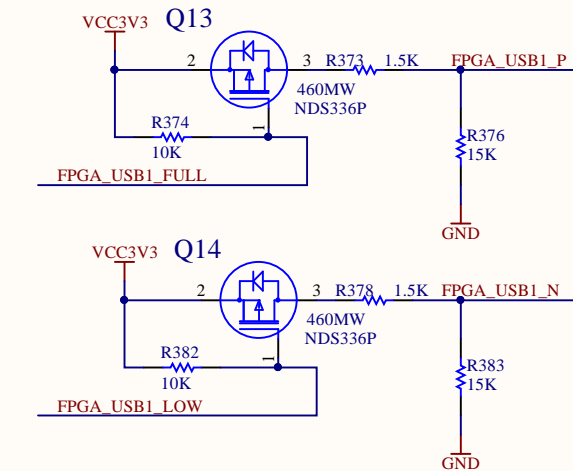
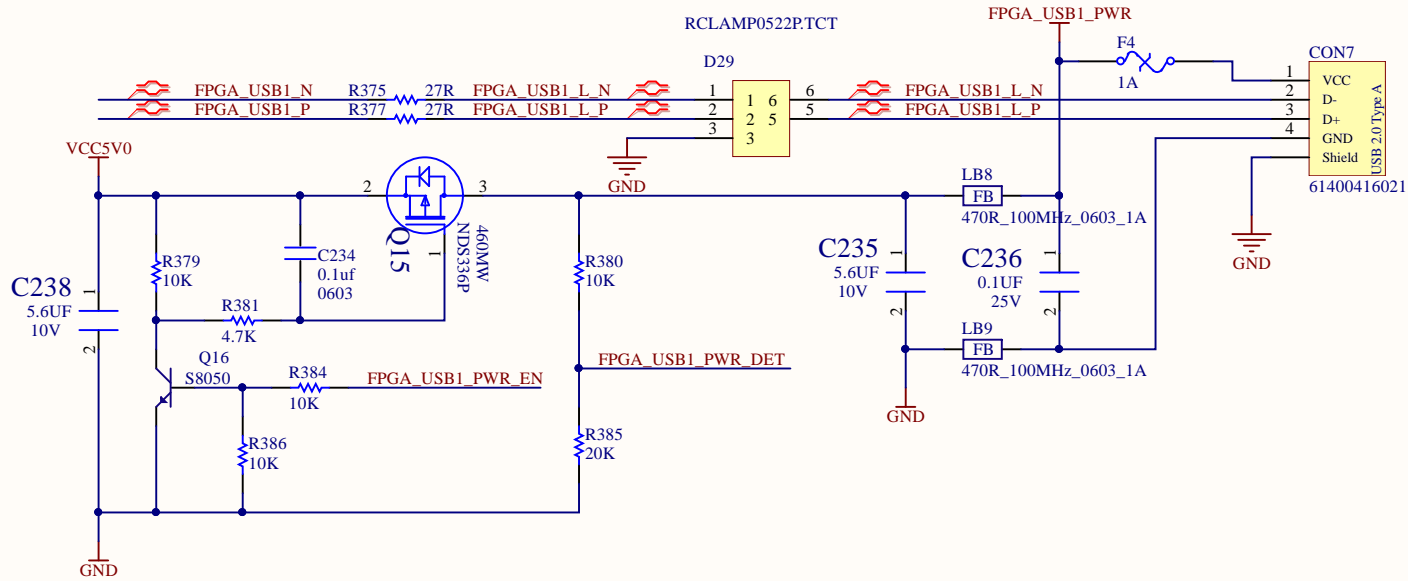
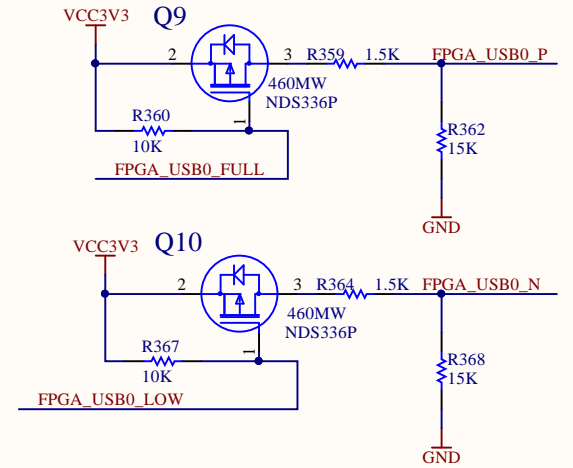
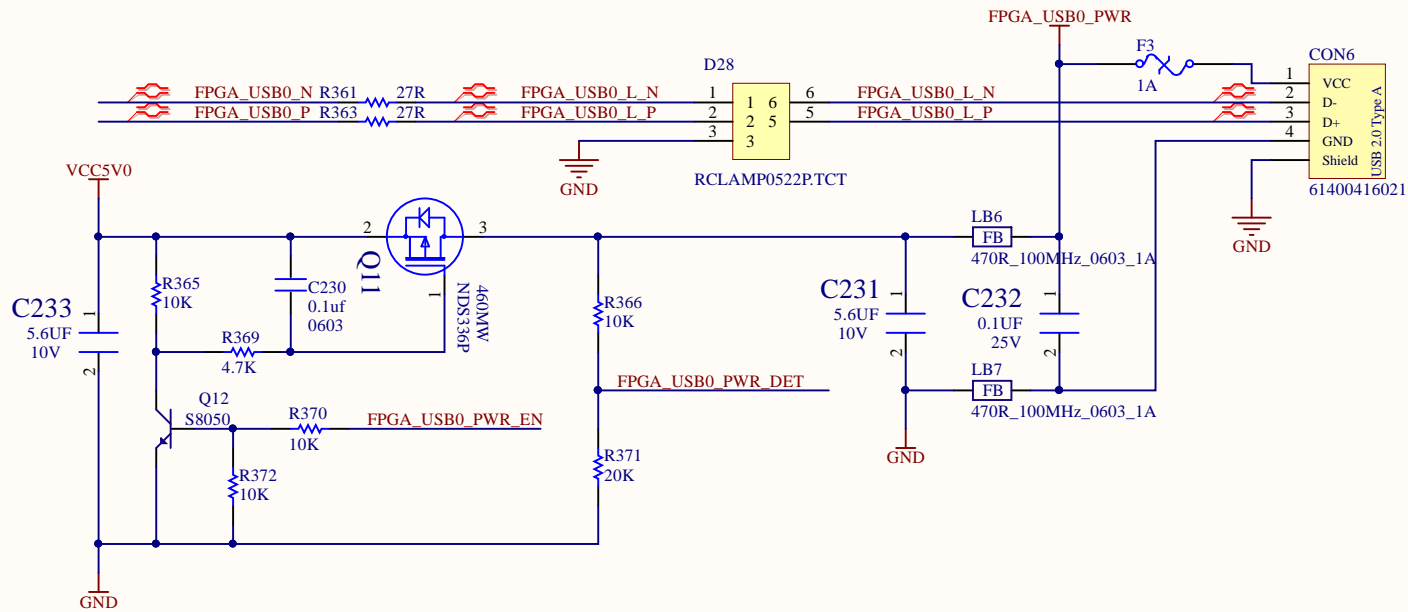


## USB MOUSE/KEYBOARD



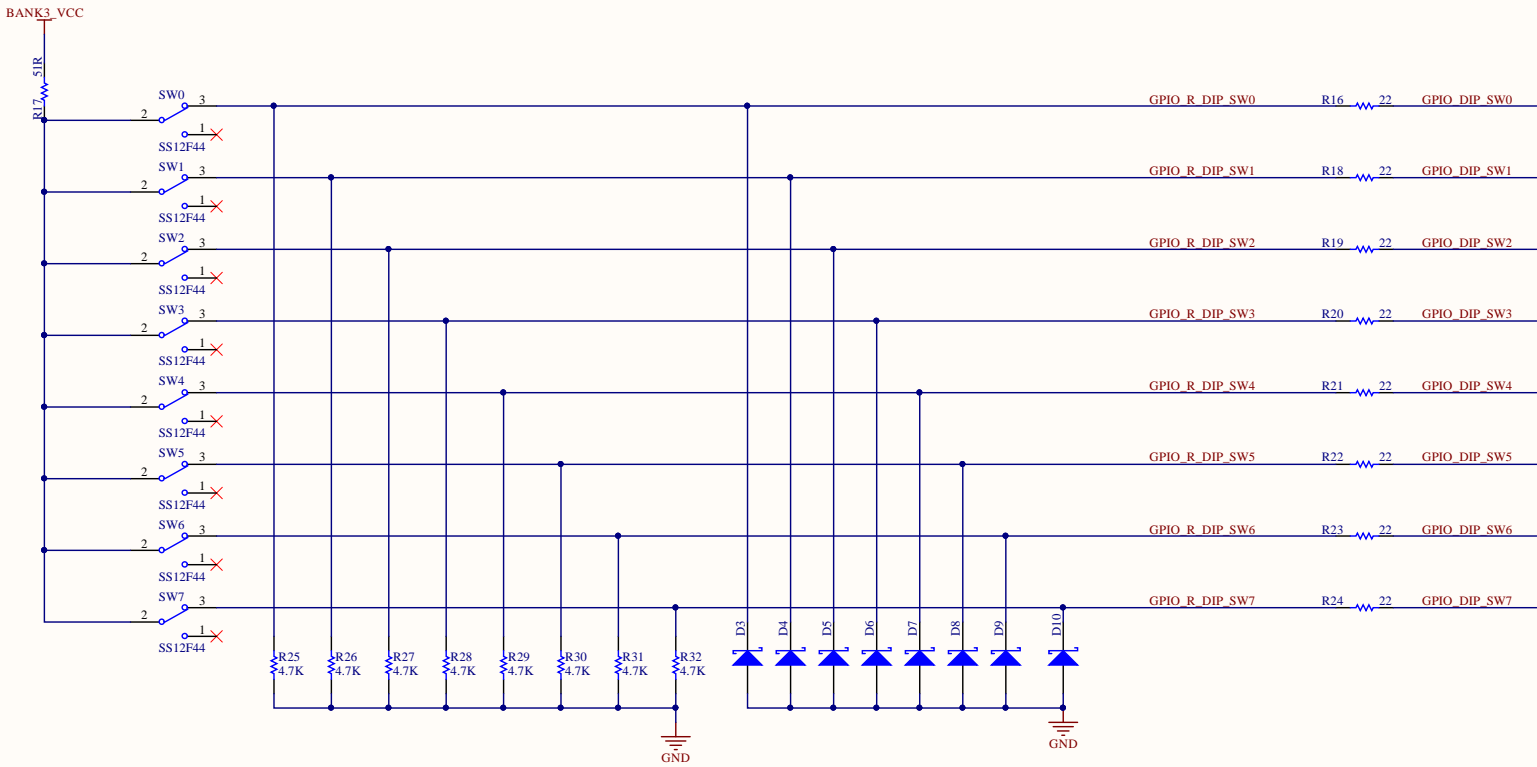


# FPGA USB

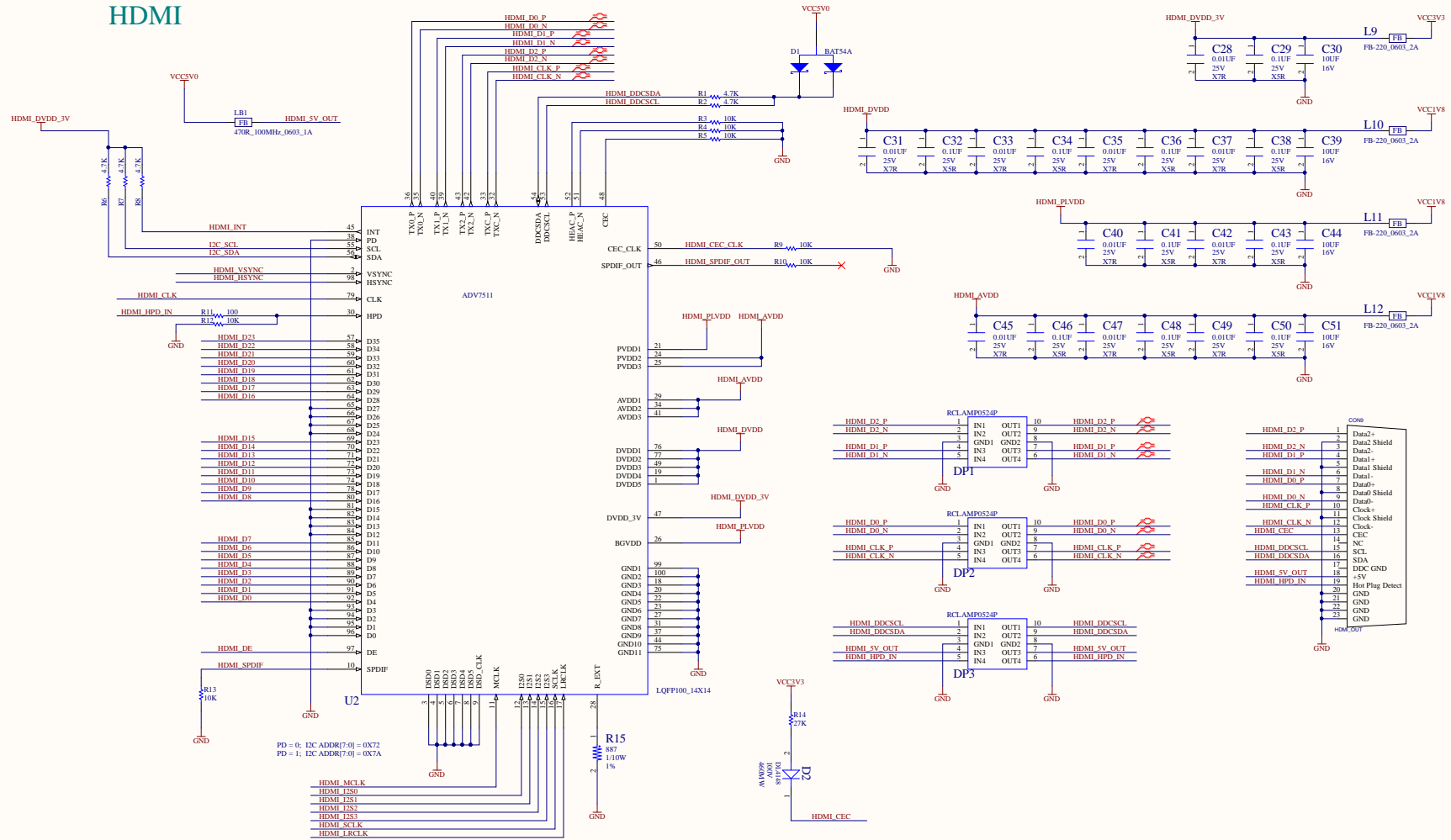


Company: FII	Title: USB_FPGA	of PRA040
Date: 2019-07-20	Time 3:21:59 PM	Engineer: RJ WG
Revision: V3.0	Sheet 17 of 21	Size: A4

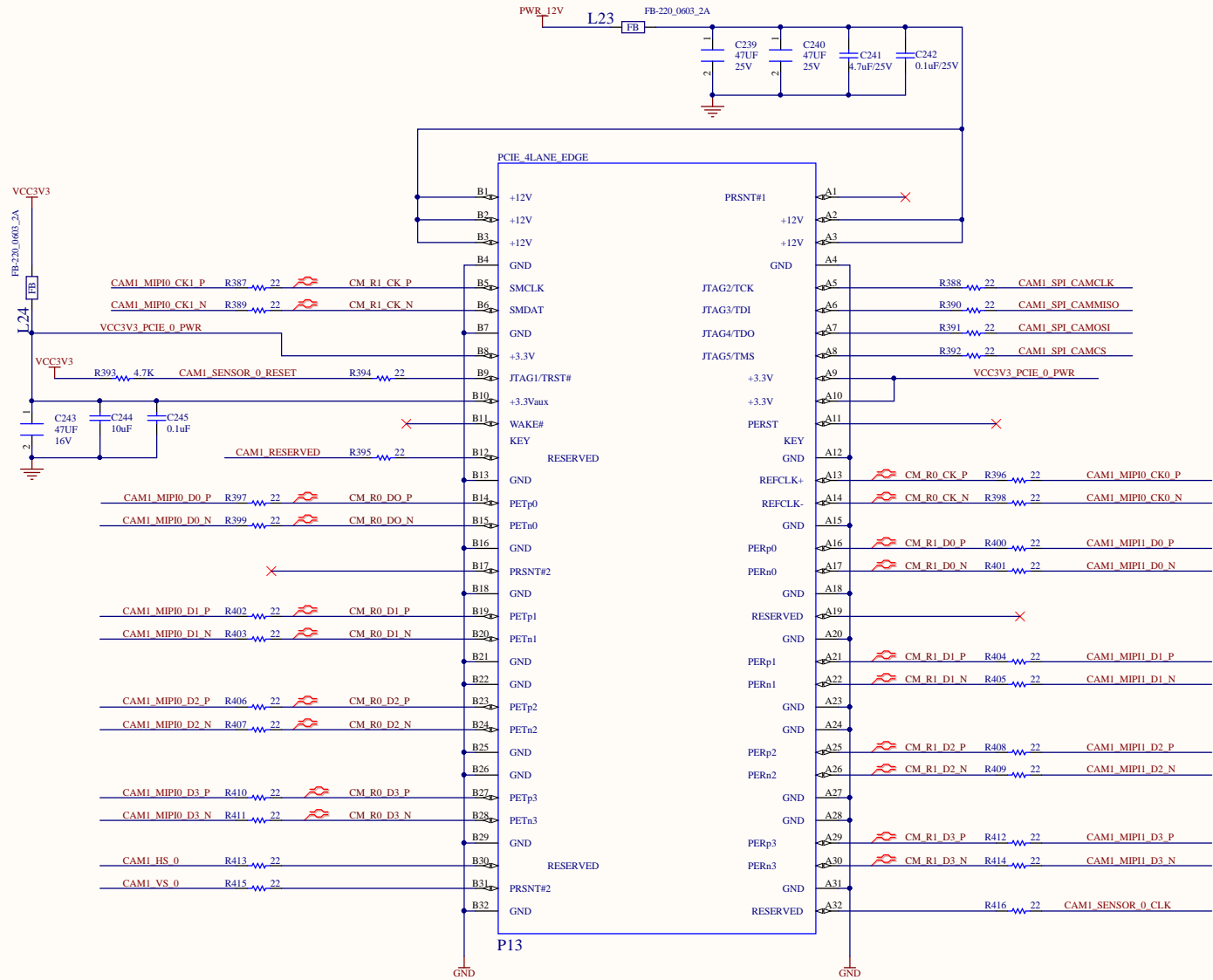
SWITCH



# HDMI



# PCIE



[illegible]