LTspice IV
Intermediate Lab Class Volume 2

Presented by:
Mats Hellberg
Linear Technology FAE

Topics

1. What is Usually Modeled (and What Isn't)
2. Making Circuit Files More Transportable
3. Behavioral Sources
4. Hierarchical Schematics and Automatic Creation of a Schematic Symbol
5. Parameters and Expression Evaluation
6. Thermistor Simulations: Plotting Temperature and Resistance
7. Voltage and Current Controlled Switches
8. Improving Simulation Speed

Summary of Hotlinks Used in this Presentation

- **Class exercise**
- **Solution to exercise**
- **Circuits to explorer at your leisure**

What Usually is Modeled?

- Typical performance at room temperature
- Error amp
  - Gm
  - Source/Sink Current
- Oscillator
  - Frequency
  - Duty Cycle Limits
- Switch logic
- Switch current limit
- Switch beta
- Peak current vs. error voltage
- Slope compensation
- Burst Mode
- Switch minimum on time
- Pulse skipping
- PLL capture & phase lock

What Usually is Not Modeled?

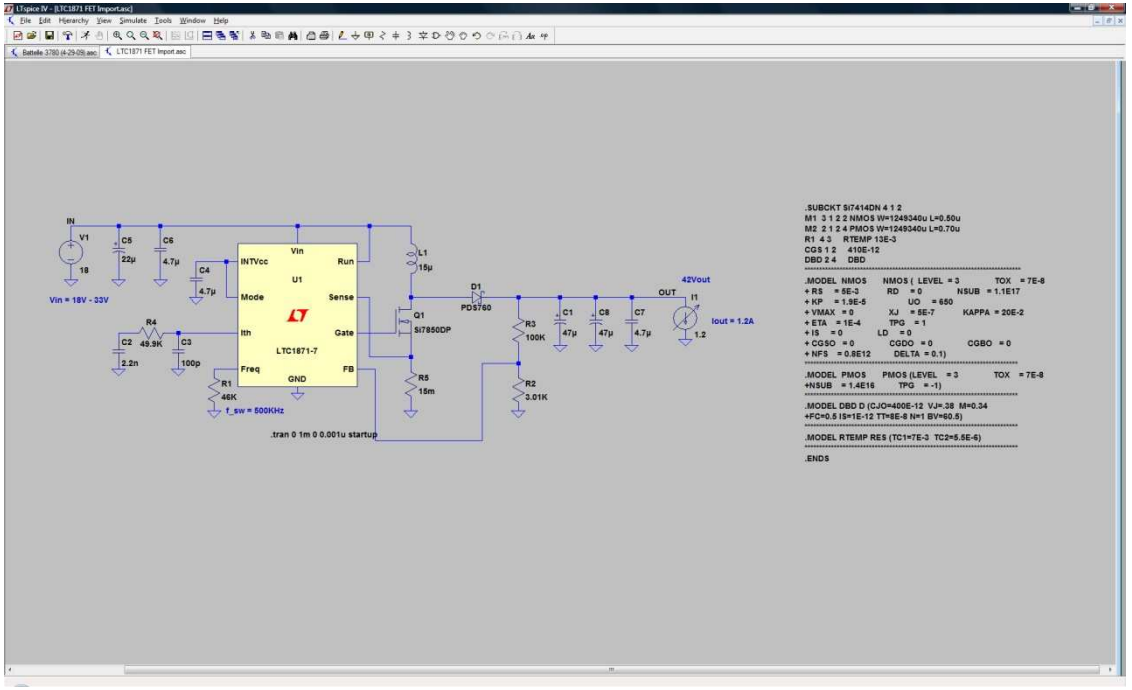
- Production scatter
- Behavior over temperature
- Catastrophic failure modes
- Oscillator injection locked SYNC pin (unless the device has a PLL)

What May or May Not be Modeled?

- Iq in all modes
- Misc features in shutdown

Making Circuit Files More Transportable

- Open model or subckt file and copy text to the clipboard
- Open new spice directive in LTspice
- Paste clipboard contents to directive text box
- Place on schematic
- Easier than using .include for simple models (i.e. SW)

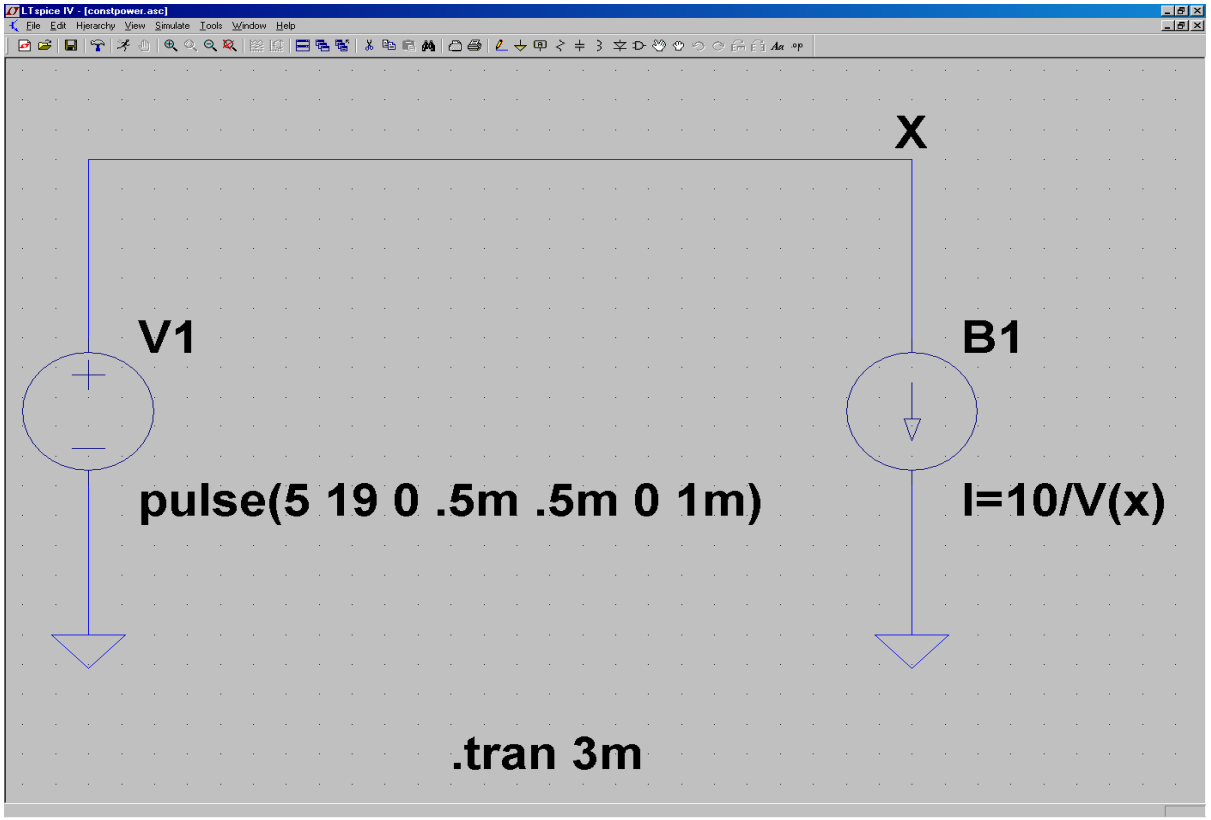


Behavioral Sources

- Behavioral sources are used when the user would like to define a source with an arbitrary expression.
- Expressions can contain the following:
  - Node voltages, e.g., V(n001)
  - Node voltage differences, e.g., V(n001, n002)
  - Circuit element currents; for example, I(S1), the current through switch S1 or Ib(Q1), the base current of Q1. However, it is assumed that the circuit element current is varying quasi-statically, that is, there is no instantaneous feedback between the current through the referenced device and the behavioral source output. Similarly, any ac component of such a device current is assumed to be zero in a small signal linear .AC analysis.
  - The keyword, "time" meaning the current time in the simulation.
  - The keyword "pi" meaning 3.14159265358979323846.
  - Various functions and operations as defined in the help file.

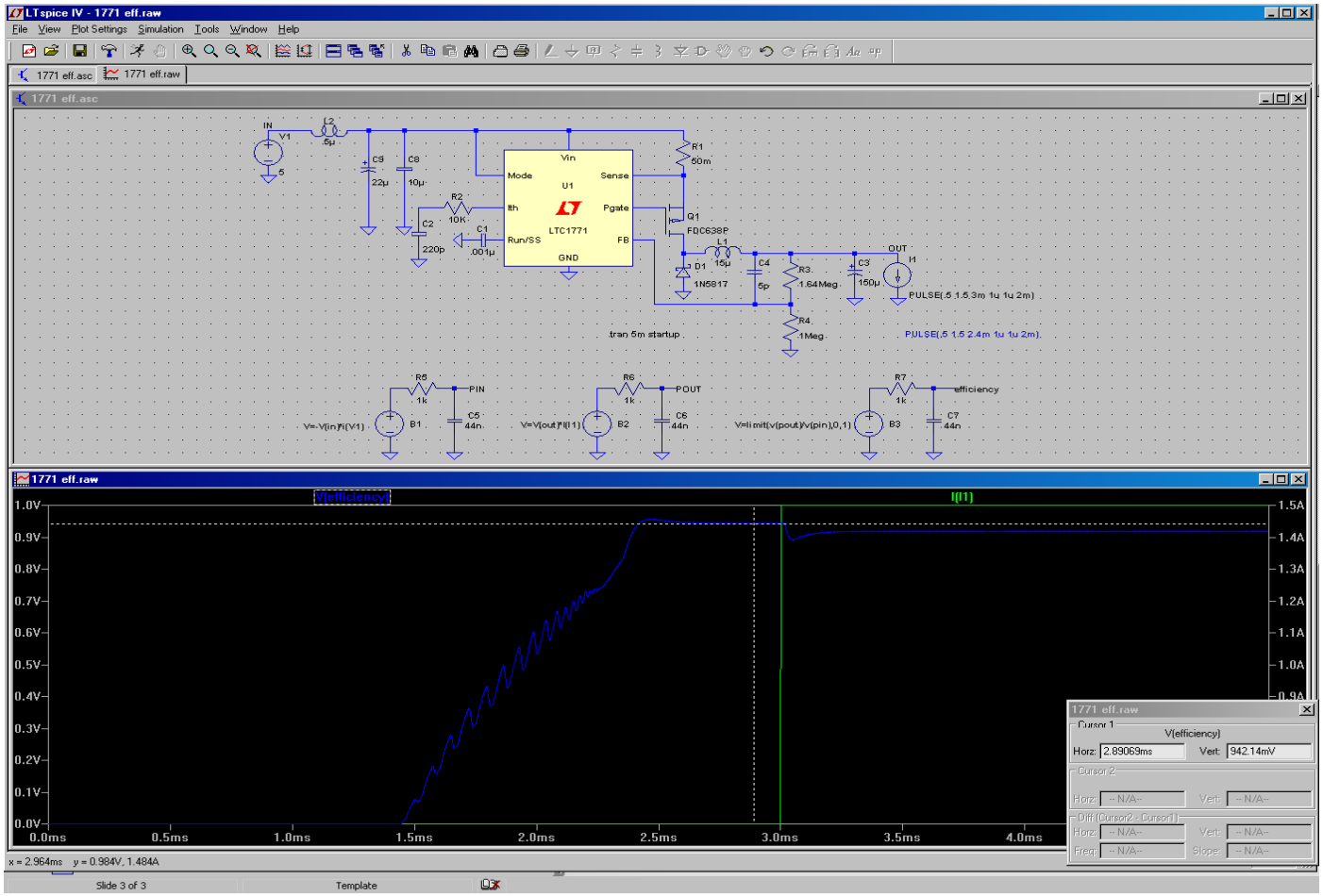
Behavioral Sources

- Open up the simulation file titled “ConstPower.asc” and follow the instructions in the simulation file to create a constant power load.



Behavioral Sources

- Open up the simulation file titled “1771Eff.asc” and follow the instructions in the simulation file.



LTspice Behavioral Simulator

- PSPICE style behavioral modeling
  - Legacy POLY( ) statements
  - Arbitrary expressions
  - Laplace
  - Look-up tables
- Arbitrary capacitance: write an expression for the charge
- Arbitrary inductor: write an expression for the flux
- An original mixed-mode simulator -- not xspice based
- Co-simulation for very complex models

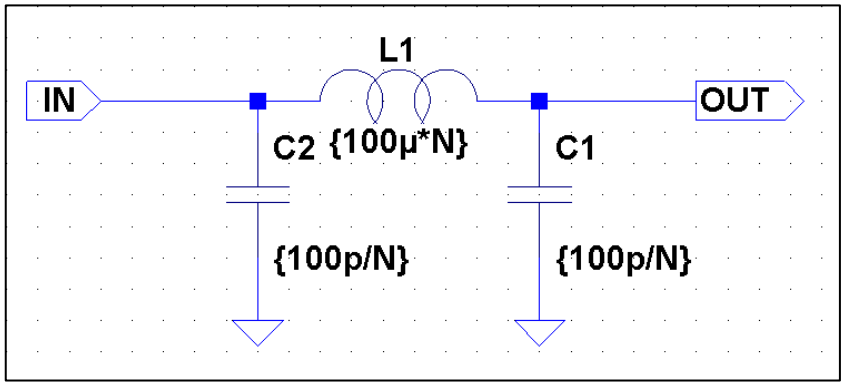
Hierarchical Schematics and Automatic Creation of a Schematic Symbol

Hierarchical Schematics / Schematic Symbols

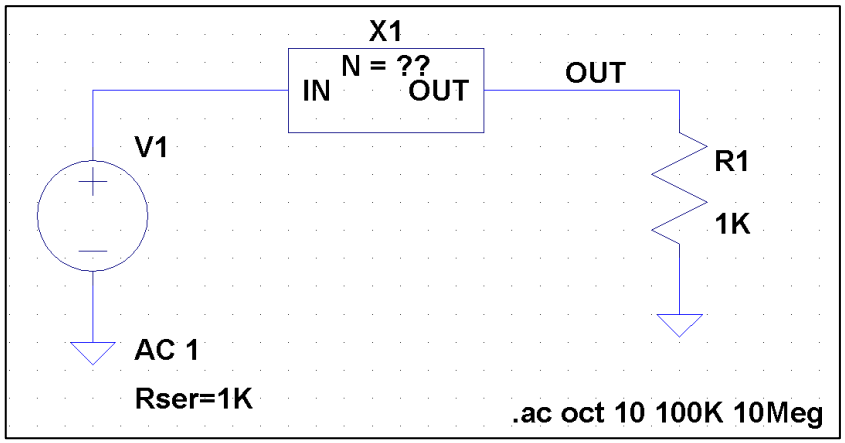
- Hierarchical schematic drafting has powerful advantages
  - Much larger circuits can be drafted than can fit onto a one sheet schematic while retaining the clarity of the smaller schematics
  - Repeated circuitry to be easily handled in an abstract manner, i.e. “black boxes” with full functionality
  - Can be re-used across several schematics

Hierarchical Schematics / Schematic Symbols

The following subcircuit……..



…..can be automatically converted to a hierarchical schematic symbol (X1):

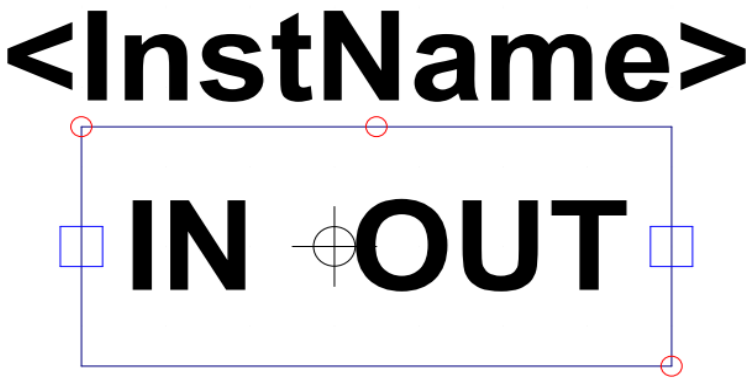


Hierarchical Schematics / Schematic Symbols

- **Exercise:**
- **Open up the simulation file titled “PISectionExample.asc” and follow the instructions in the simulation file.**

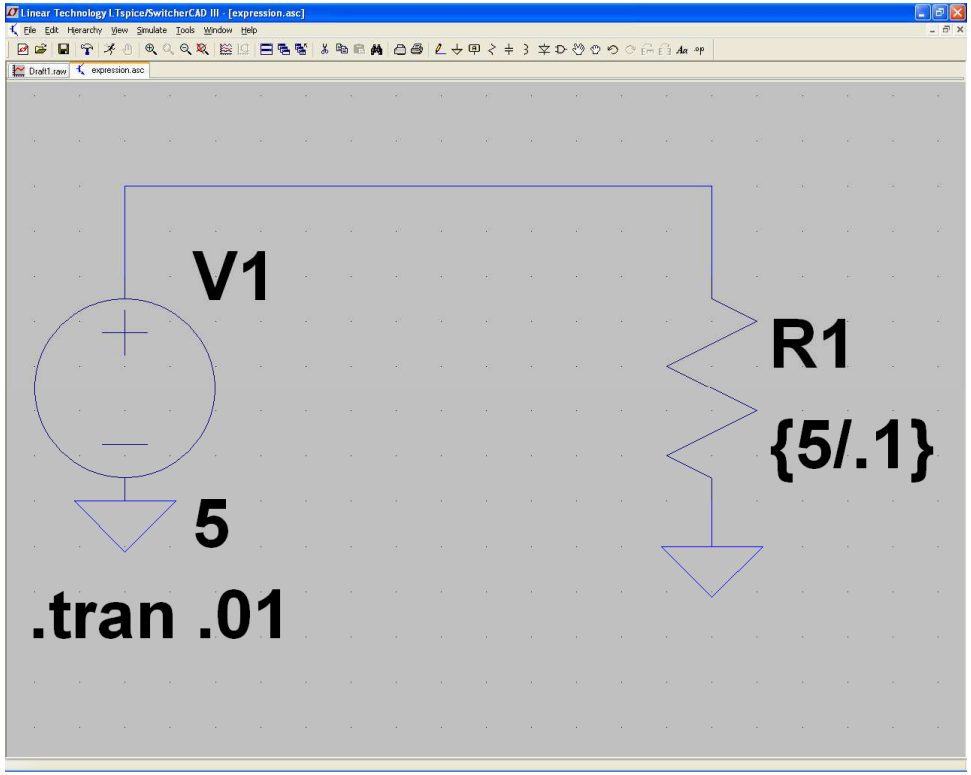
Hierarchical Schematics / Schematic Symbols

- After clicking “Yes” a new sheet titled “PISectionExample.asy” will open
- This hierarchical schematic is automatically saved to the folder – there is no need to manually save
- There is no further effort required, i.e. change <InstName>
- Both the schematic and assembly windows can be closed



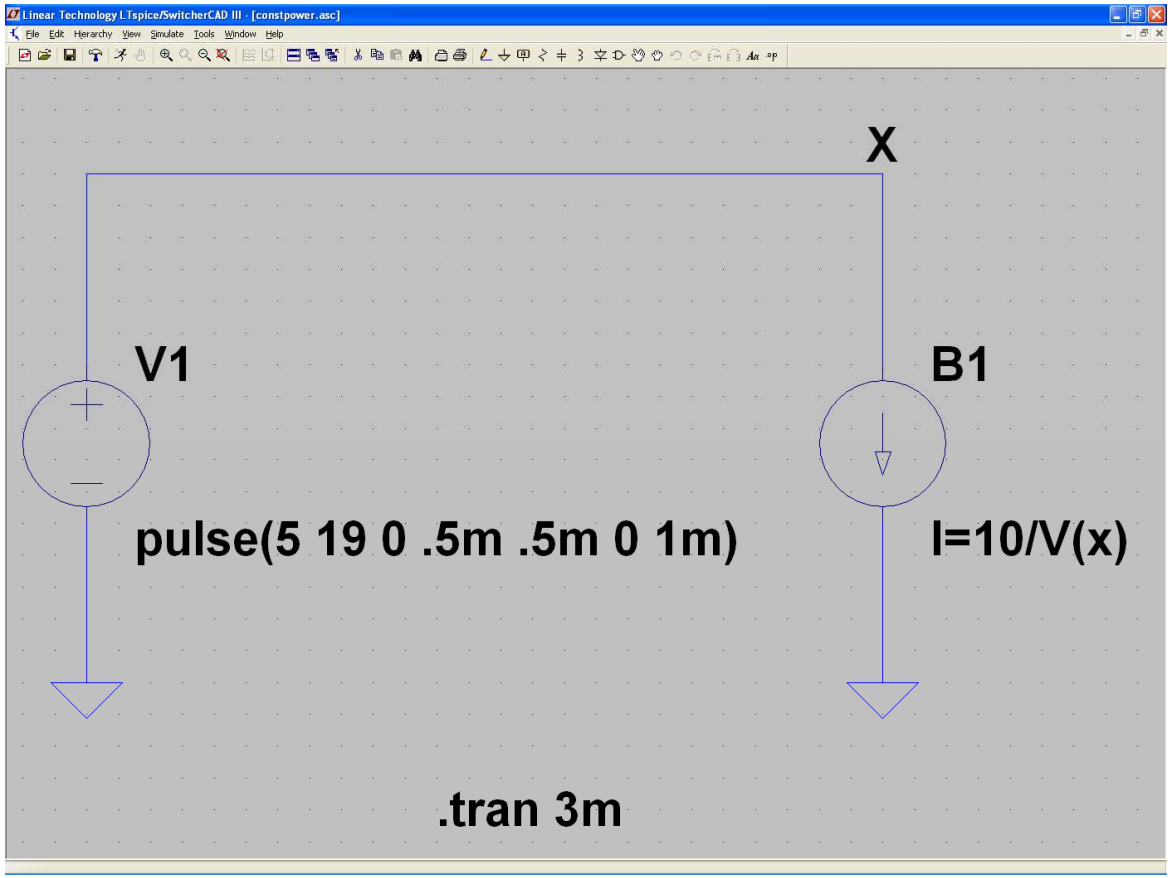
Expression Evaluation

- **When curly braces { } are encountered, the enclosed expression is evaluated on the basis of all relations available at the scope and reduced to a floating point value (evaluated *before* simulation begins).**



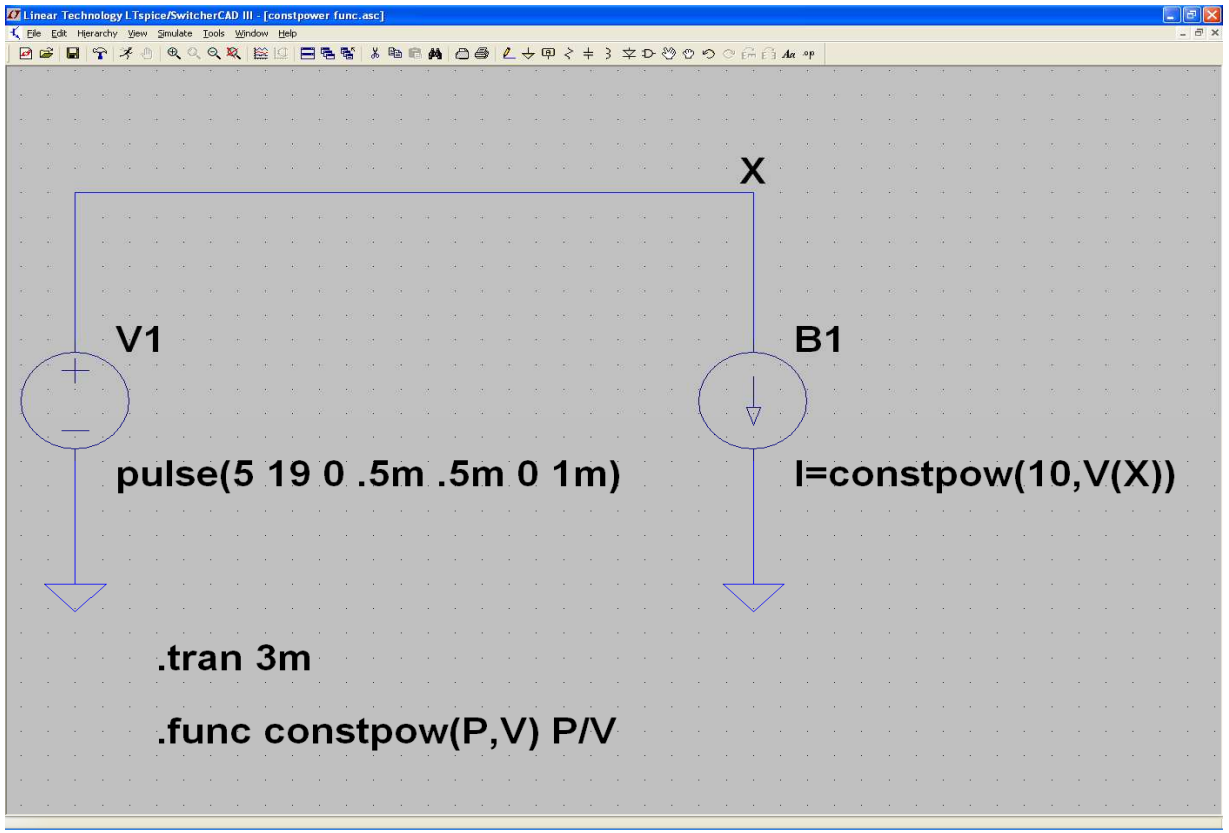
Other Places to Use Expressions

- **Without { }, the expression is not reduced to a value before simulation, but is a calculated *during* simulation in "real time". Below it is used within a behavioral source.**



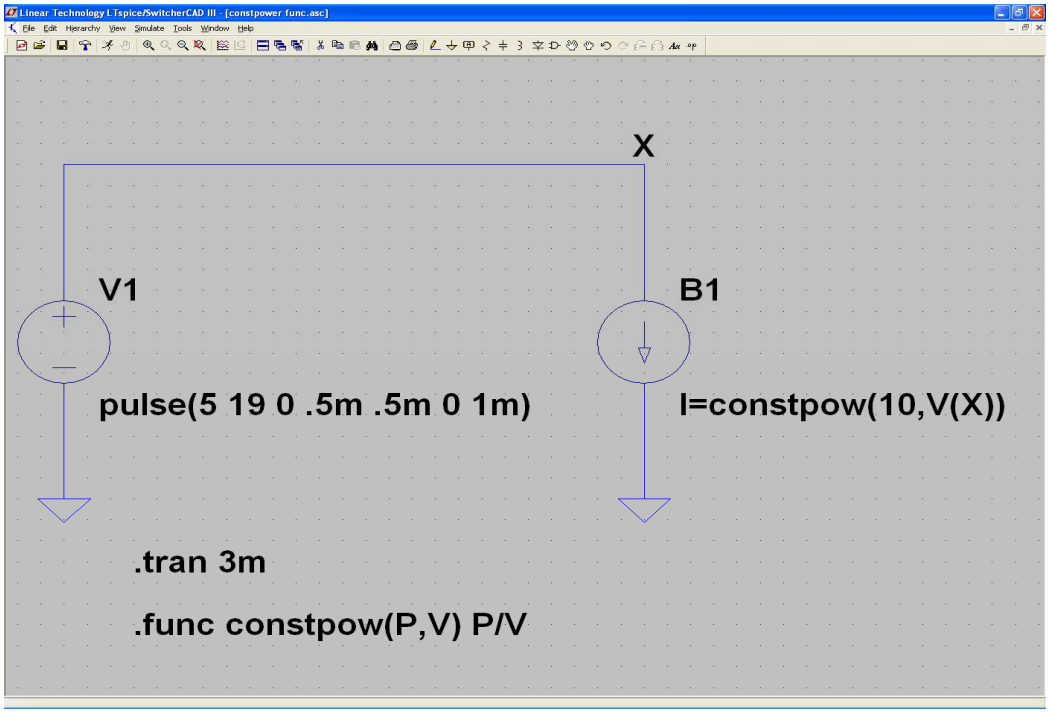
User-Defined Functions/Parameters

- The .func directive allows the creation of user-defined functions for use with user parameterized circuits and behavioral sources



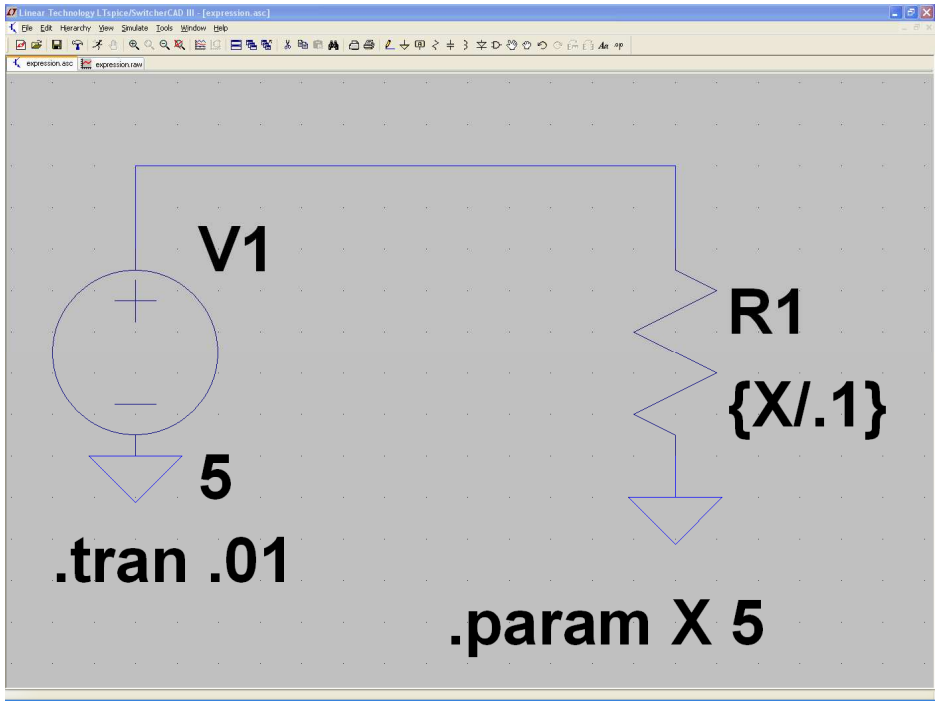
User-Defined Functions/Parameters

- In this example the source B1 calls the function constpow and sends it the parameters of “10” and “V(X)” (the voltage at the node labeled “X”
- .func constpow calculates 10 divided by the voltage at “X” and returns the result to source B1 in “real time”



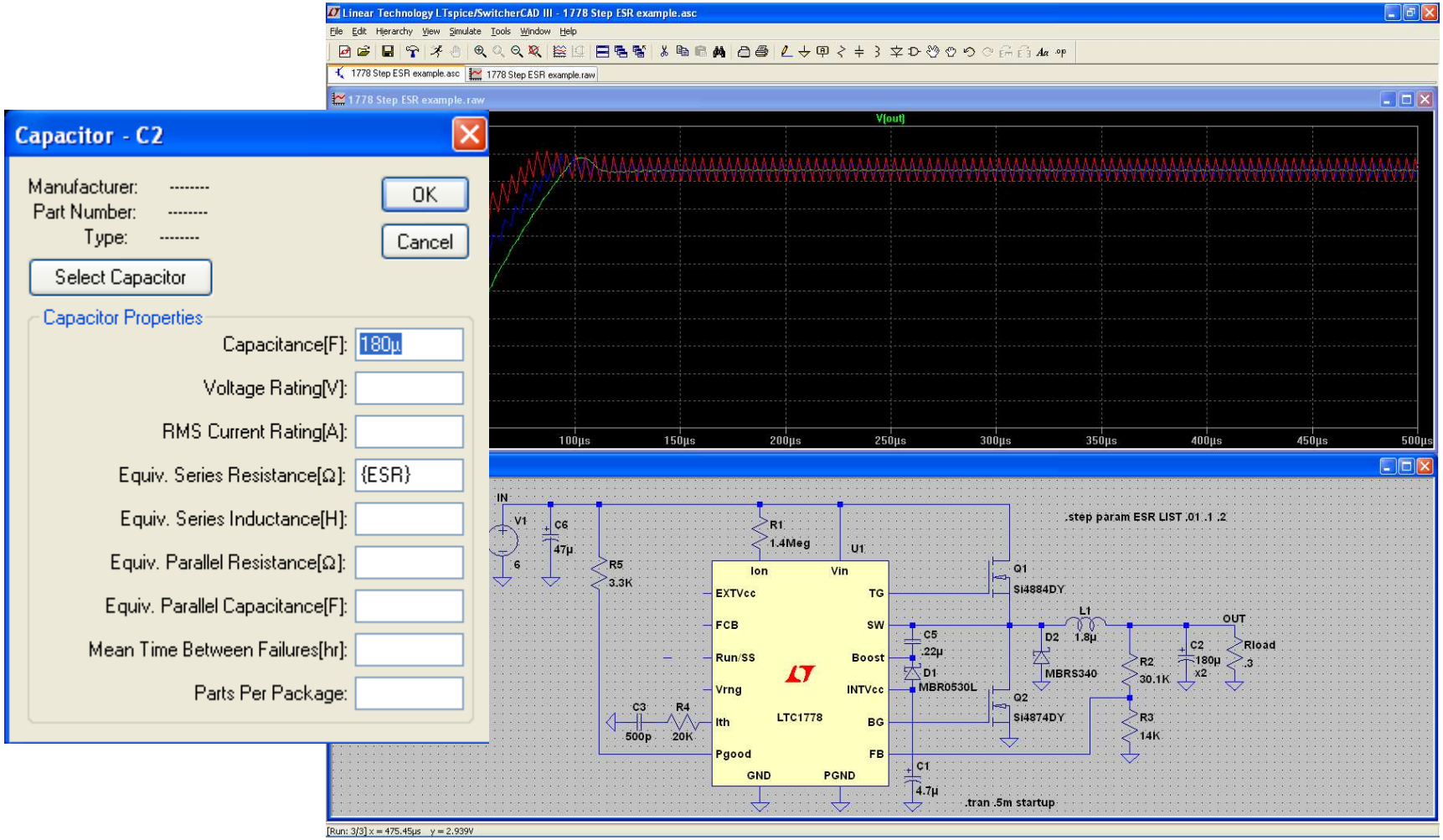
User-Defined Functions/Parameters

- The .param directive allows the creation of user defined variables
- Useful for varying component values without actually editing component properties



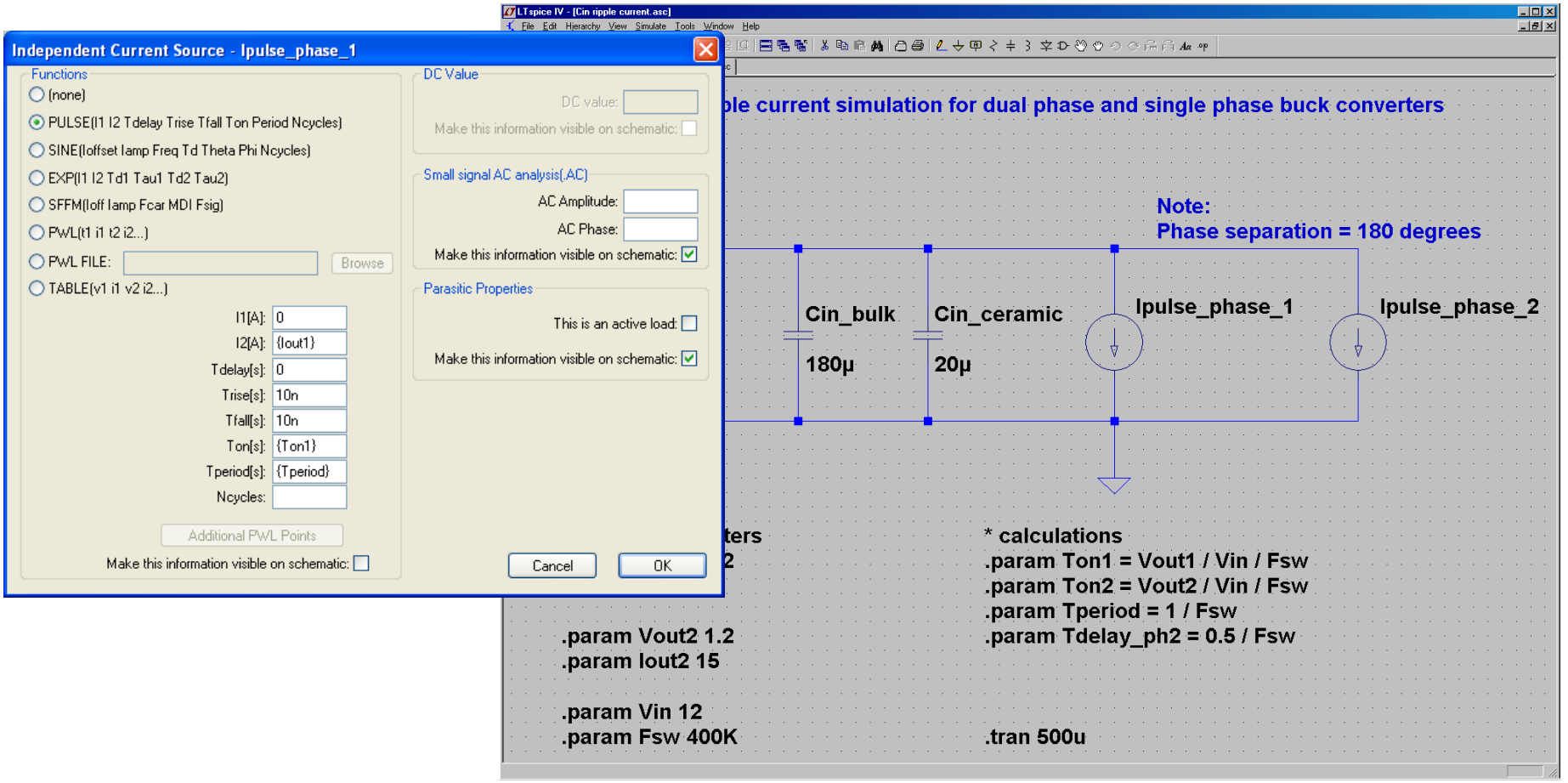
User-Defined Functions/Parameters

- **Parameters can be used within components**



User-Defined Functions/Parameters

- Parameters can also be used within sources.
- Multiple parameters can be used simultaneously

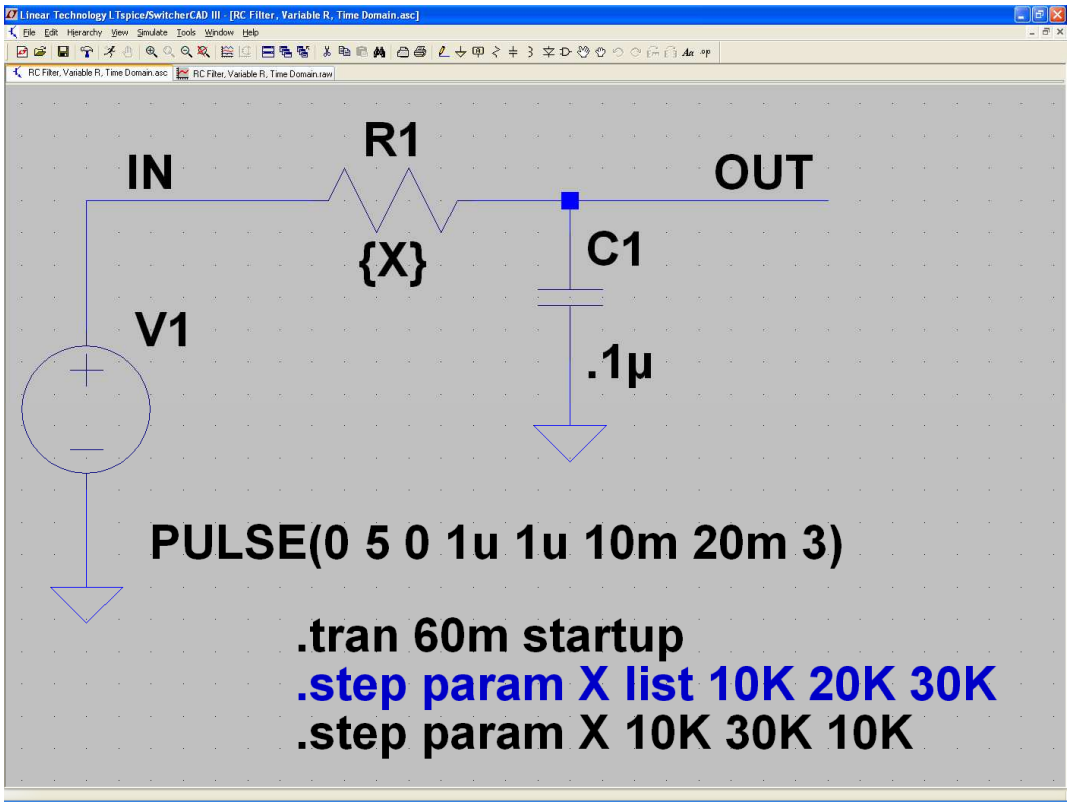


Parameter Sweeps

- The .step command causes the analysis to be repeatedly preformed while stepping a model parameter
- Essentially multiple back-to-back simulation runs with the results of previous runs kept instead of being discarded
- Steps may be linear, logarithmic, or specified as a list of values
- Example: RC network and stepping a list of values

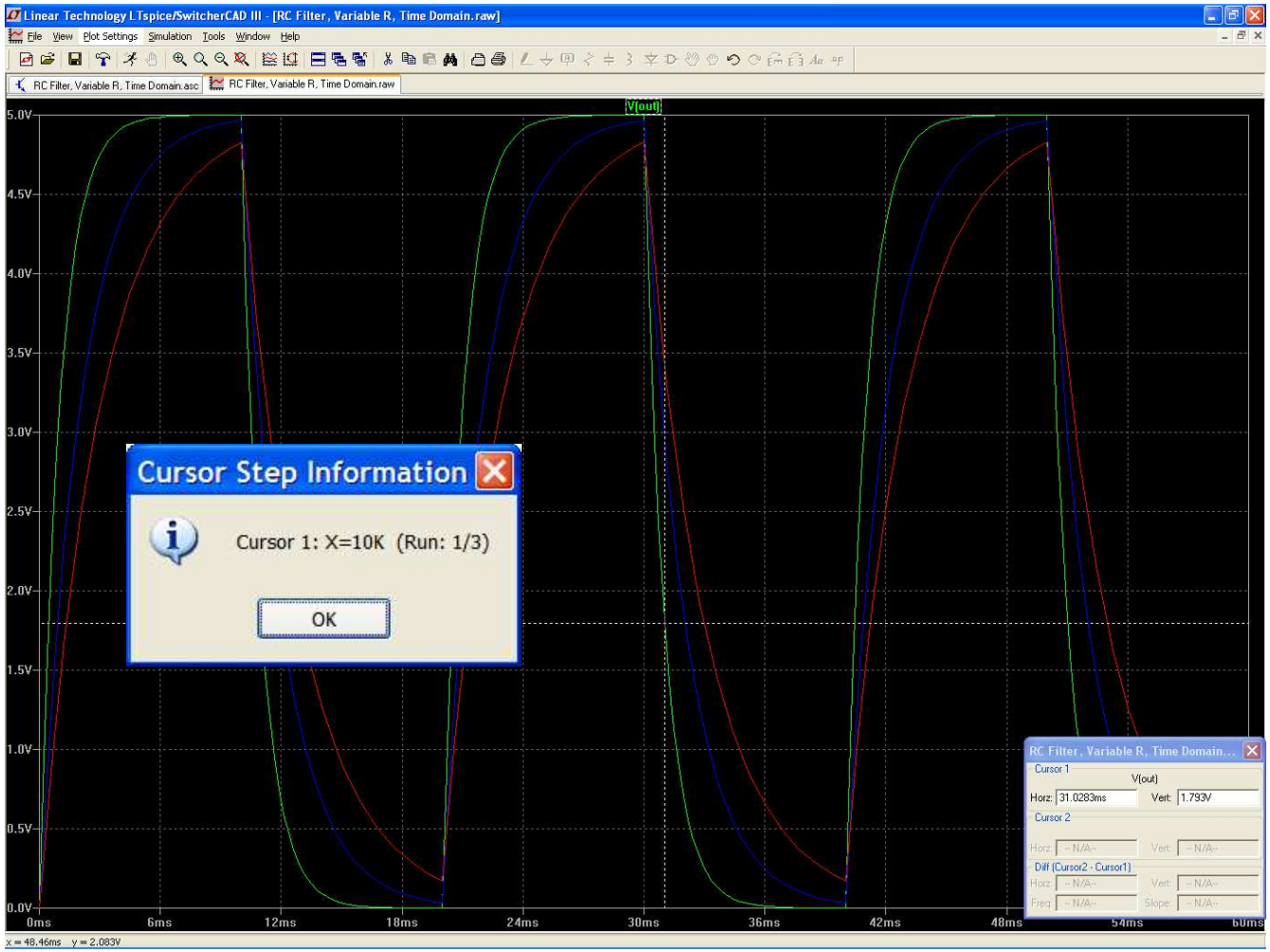
Parameter Sweeps

- Open up the simulation file titled "RCFilterVariableRTimeDomain.asc" and follow the instructions in the simulation file.



Add .step command using Edit pull down menu → SPICE Directive, or by using the hotkey "s".

Parameter Sweep – RC Filter Result

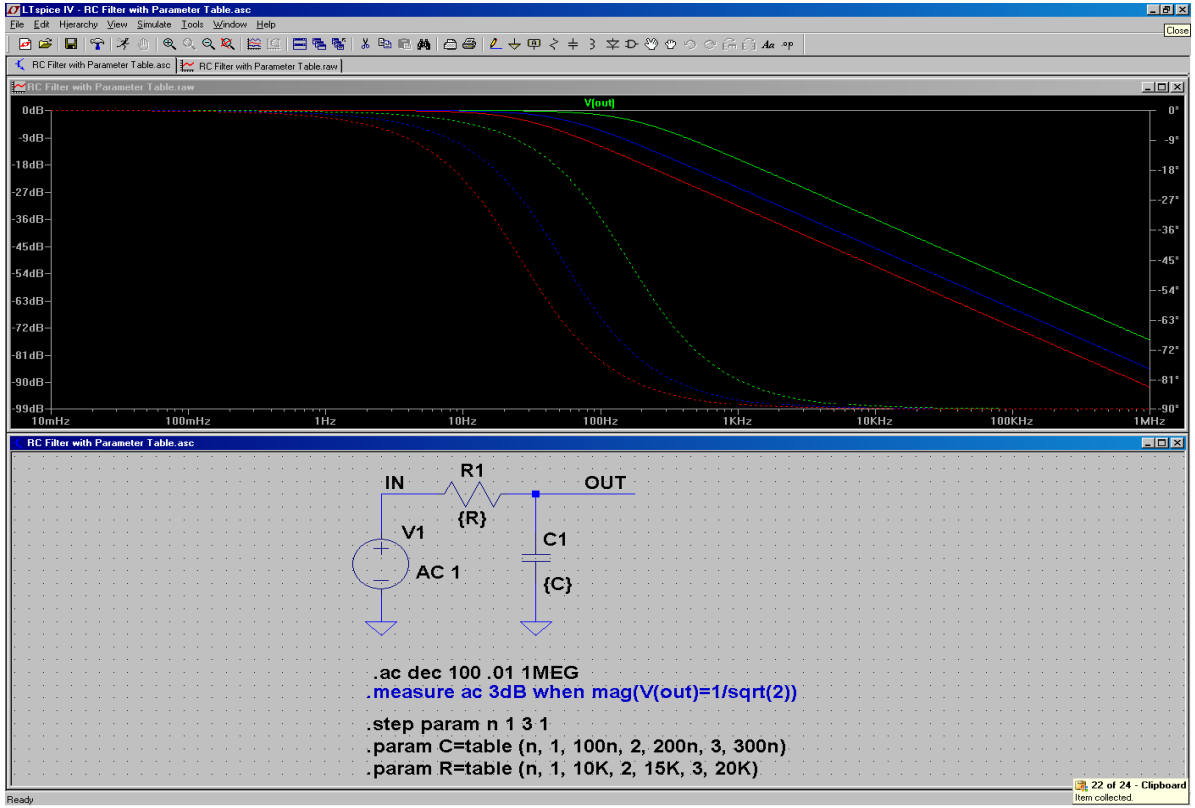


Using the measurement cursor (left-click the *label*), the up/down arrow keys on the keyboard will toggle between waveforms

Right click on the cursor to display which run is associated with each waveform

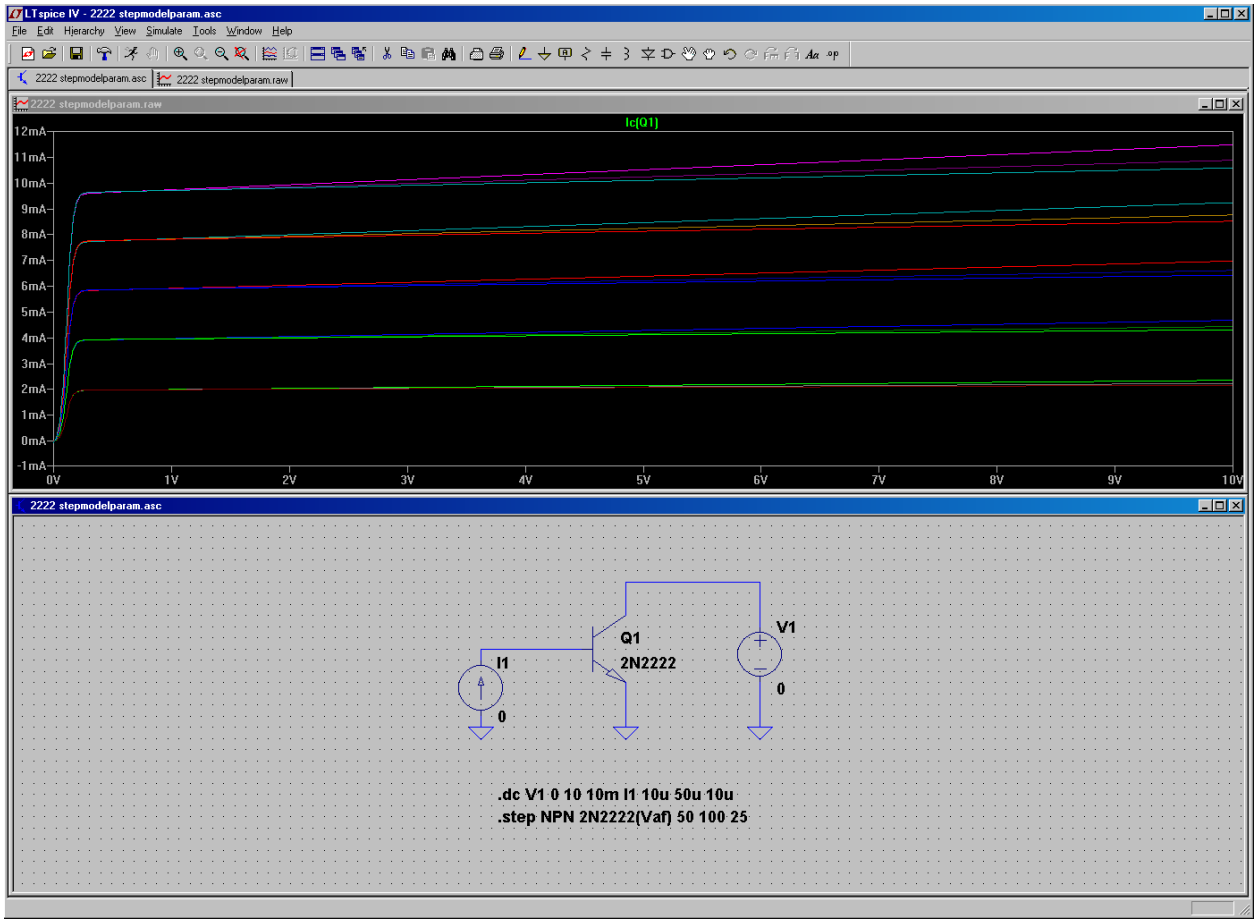
Stepping Multiple Parameters

- The table function can be used to step multiple parameters simultaneously using a table format (ex. pairs of values can be defined and simulated)
- Open up the simulation file titled “RCFilterWithParameterTable.asc” and follow the instructions in the simulation file.



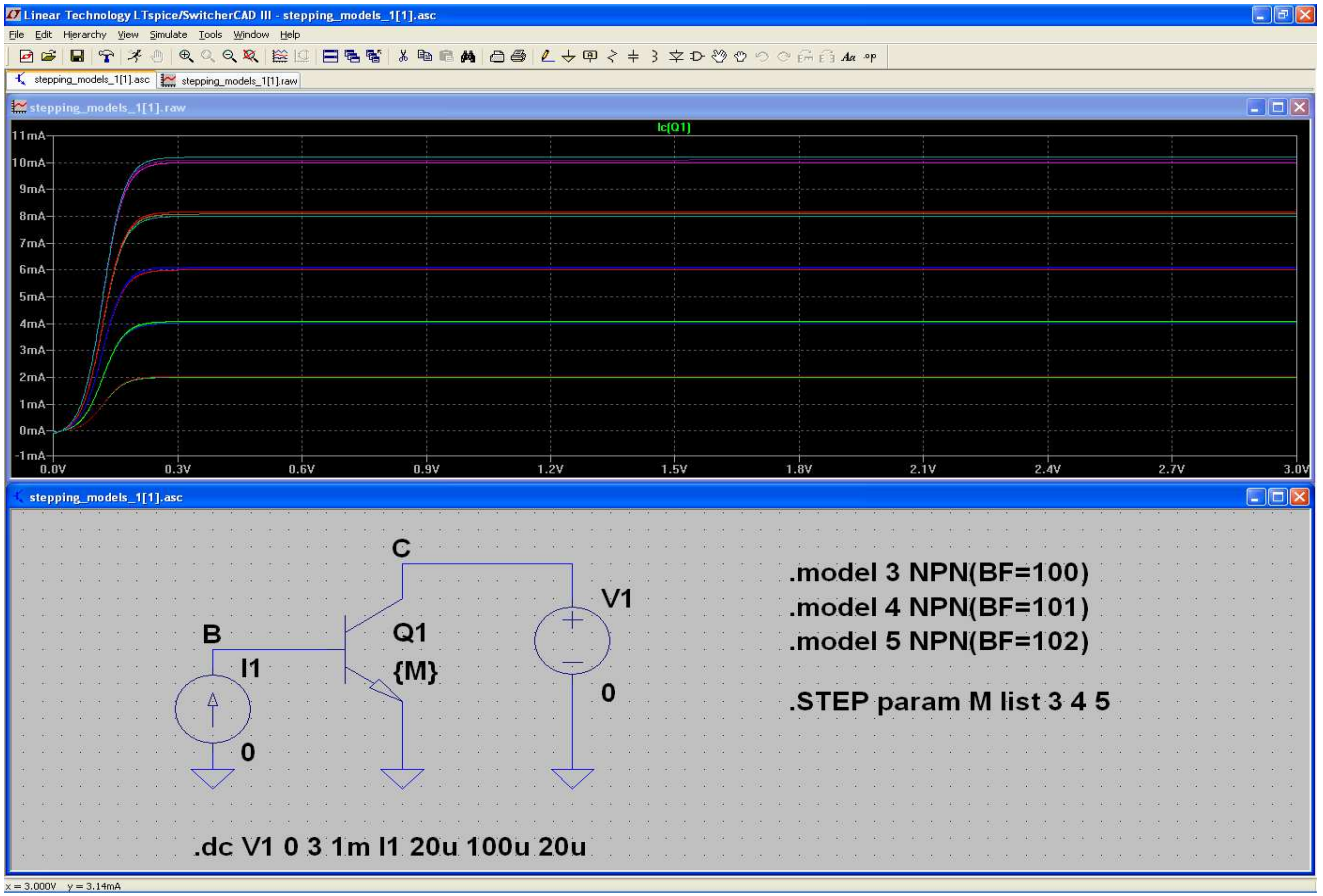
User-Defined Functions/Parameters

- .Model parameters can be stepped
- Open up the simulation file titled “2222StepModelParam.asc” and follow the instructions



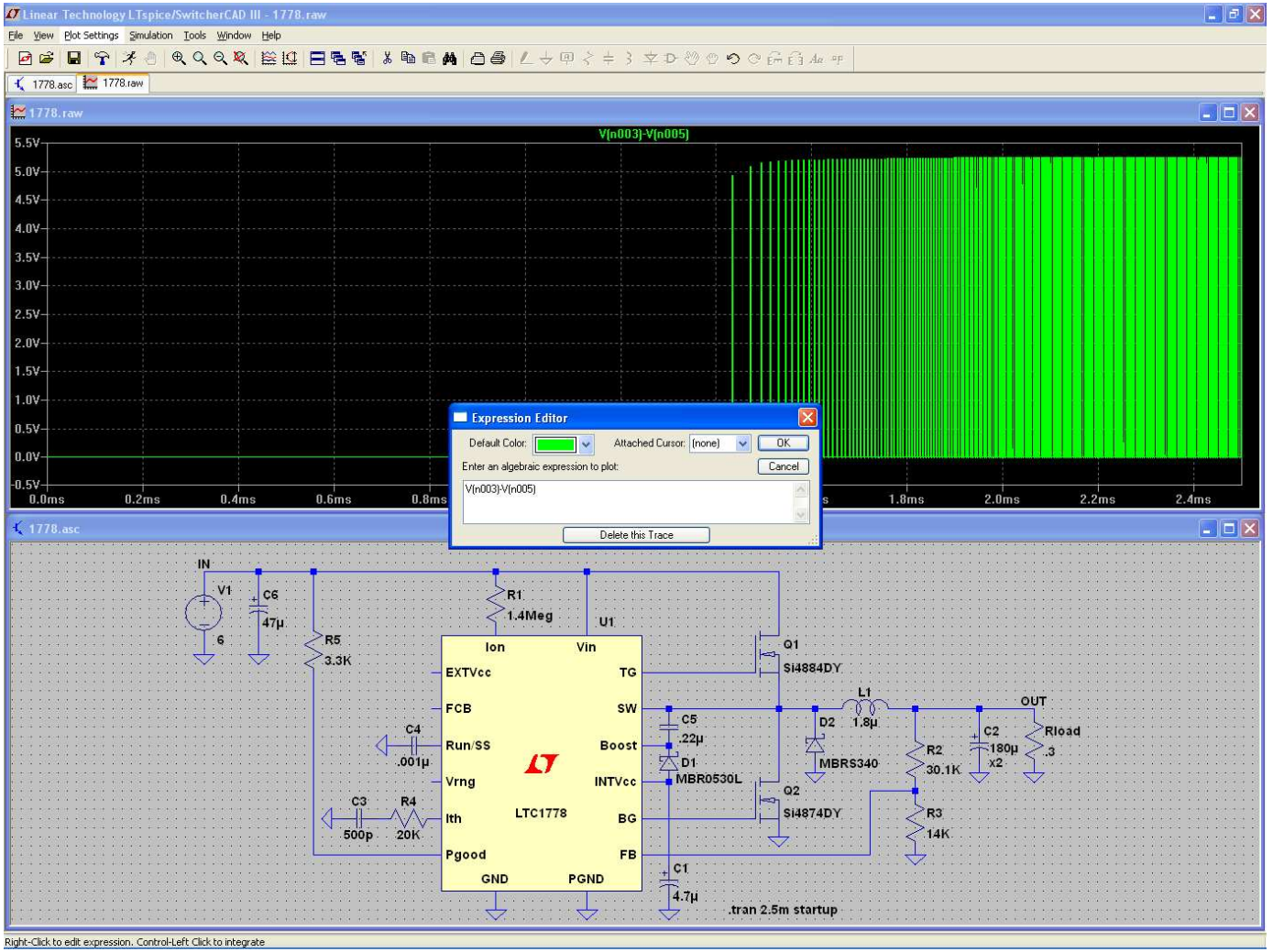
More .step uses

- The .step command can also be used to step which model is being used.
- Open up the simulation file titled “SteppingModels.asc” and follow the instructions in the simulation file.



Other Places to Use Expressions

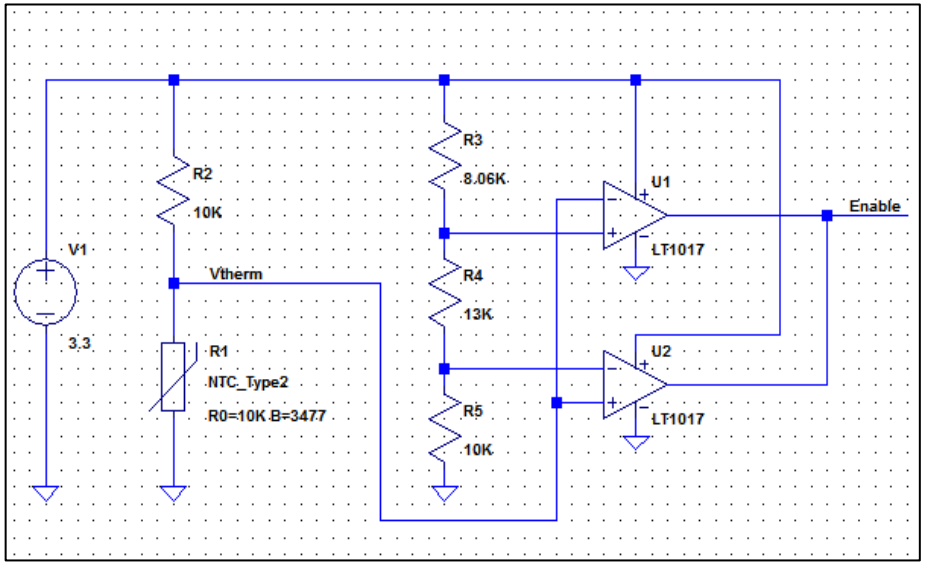
- **Within the waveform editor (right click on trace name)**

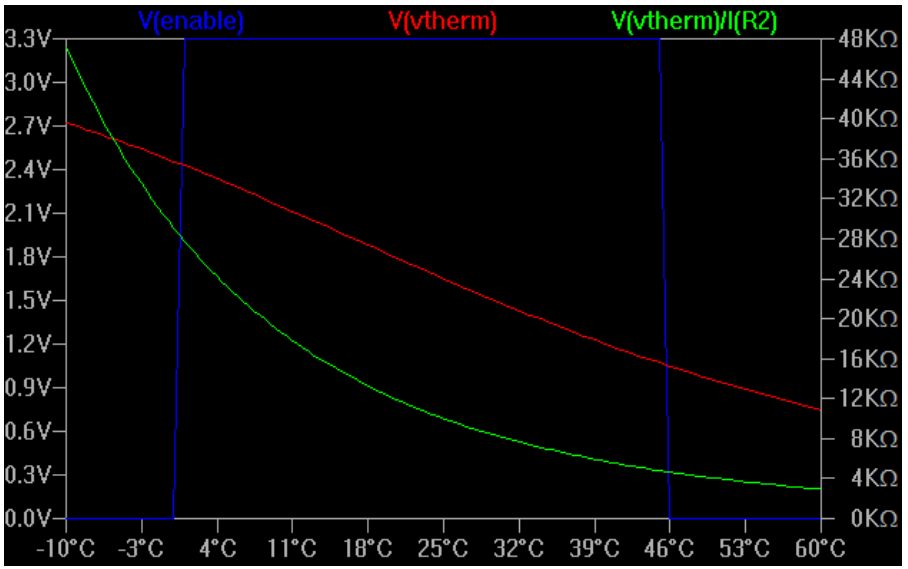


Thermistor Simulations: Plotting Temperature and Resistance

Plotting Temperature and Resistance

- Voltage and/or current are typically plotted on the vertical axis and time is typically plotted on the horizontal axis
- It is possible to plot resistance, temperature, and other parameters on the horizontal and vertical axes
- Thermistor simulation example: navigate to the NTCCircuit.asc simulation file and follow the instructions.





Plotting Temperature and Resistance

Important items to note for the NTCCircuit.asc simulation:

- **The DC operating point ".op" simulation command must be used (see LTspice help regarding DC operating point definition)**
- **The SPICE model for the thermistor is included in the simulation file**
- **A two terminal thermistor schematic symbol with the appropriate device parameters is required**
- **Additional instructions / information is included in the simulation file.**

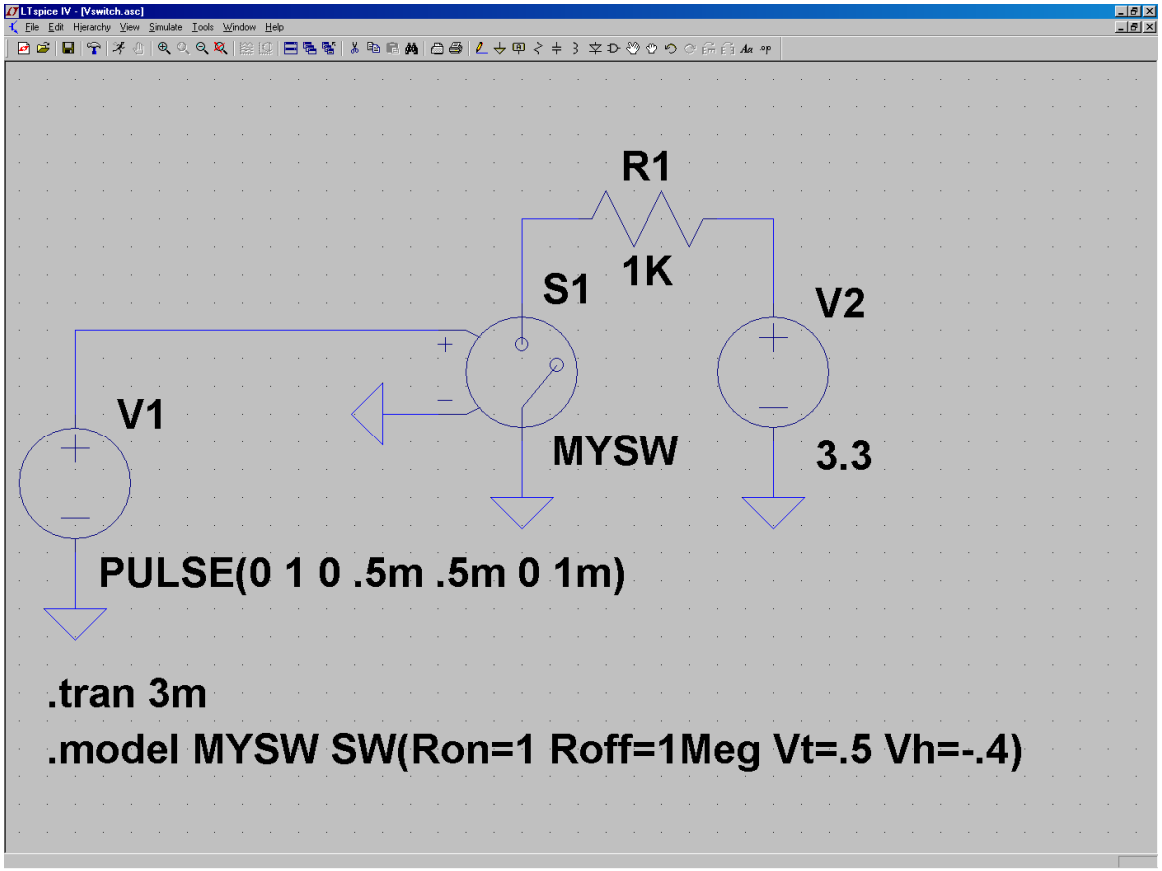
Plotting Temperature and Resistance

Important items to note for the NTCCircuit.asc simulation (cont.):

- **Voltages can be labeled and in this case the voltage across thermistor R1 is labeled Vtherm**
- **Currents cannot be labeled, thus we must determine what LTspice has called the current flowing into thermistor R1**
- **Probing the top terminal of R1 we see the current has been labeled by LTspice as "Ix(R1:A)**
- **Plotting the expression V(vtherm)/Ix(R1:A) therefore plots resistance of R1**
- **Note that probing the bottom terminal of R1 we see that the current has been labeled Ix(R1:B) by LTspice even though in this case the current is the same as the top terminal (but reversed)!**

Voltage/Current Controlled Switch

- A voltage/current controlled switch must have a model defined. This may be done as a SPICE directive directly on the schematic. (ex. Vswitch.asc)



Switch Parameters

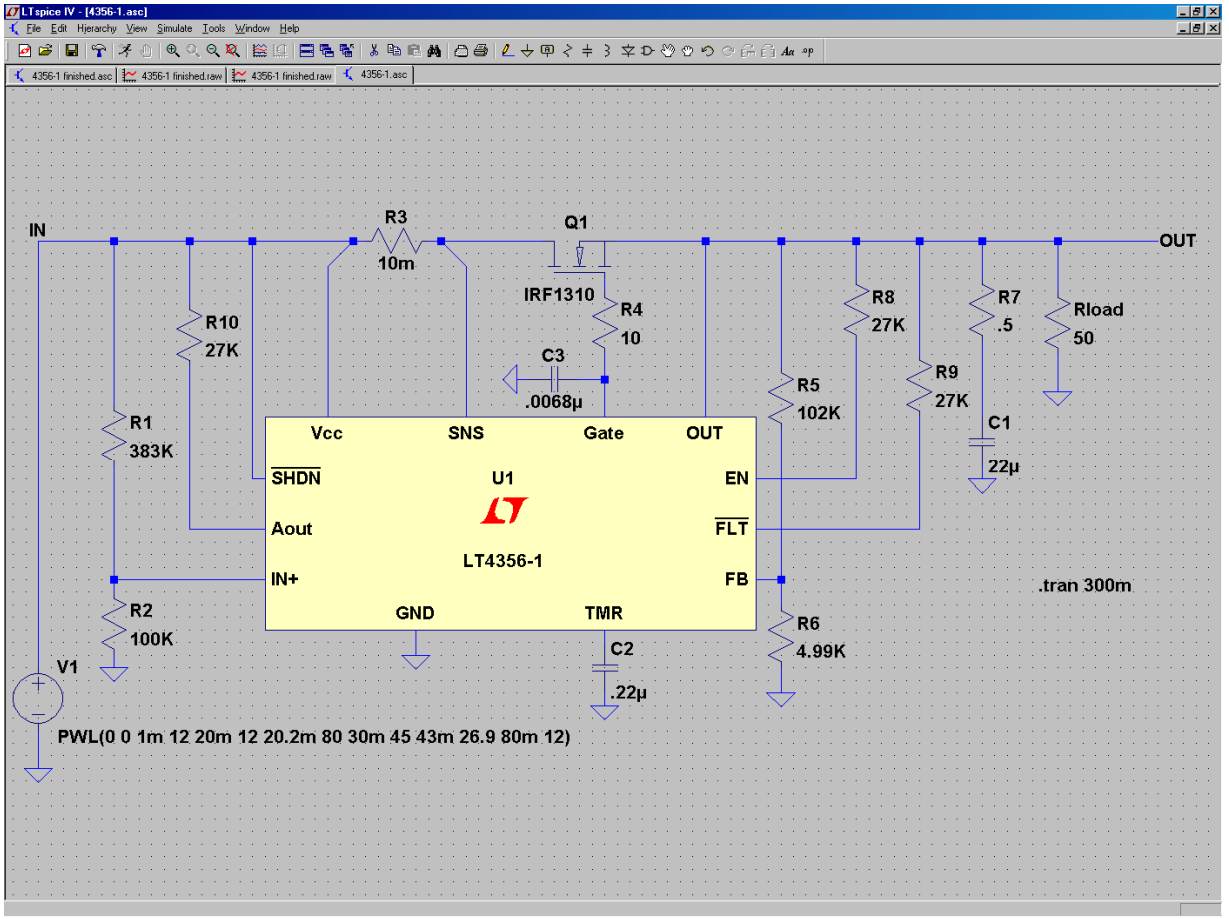
- **The parameters for the switch model are described in the help file.**

Voltage Controlled Switch Model Parameters

Name	Description	Units	Default
Vt	Threshold voltage	V	0.
Vh	Hysteresis voltage	V	0.
Ron	On resistance	Ω	1.
Roff	Off resistance	Ω	1/Gmin
Lser	Series inductance	H	0.
Vser	Series voltage	V	0.
Ilimit	Current limit	A	Infin.

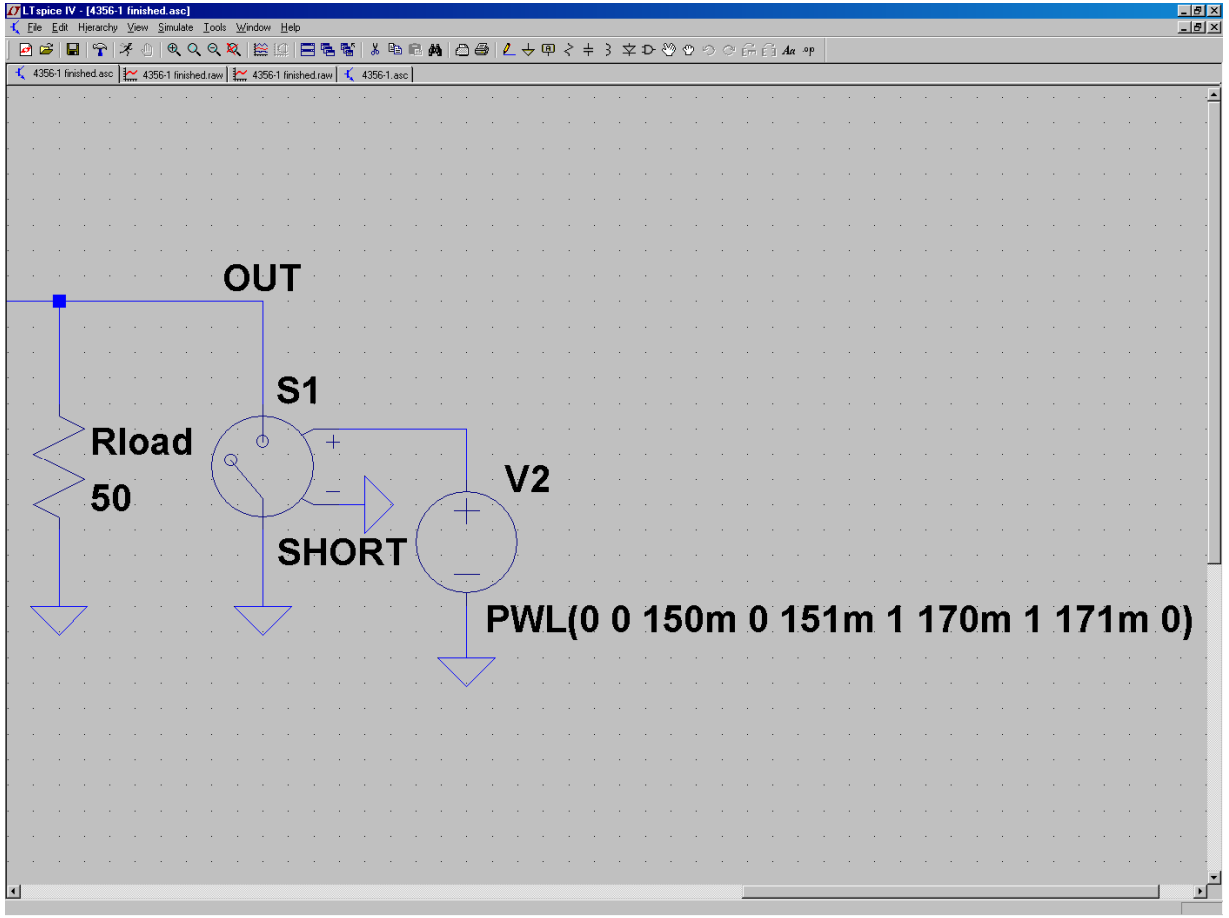
Example of Short Circuit

- Open up the simulation file titled “4356-1.asc” and follow the instructions in the simulation file.



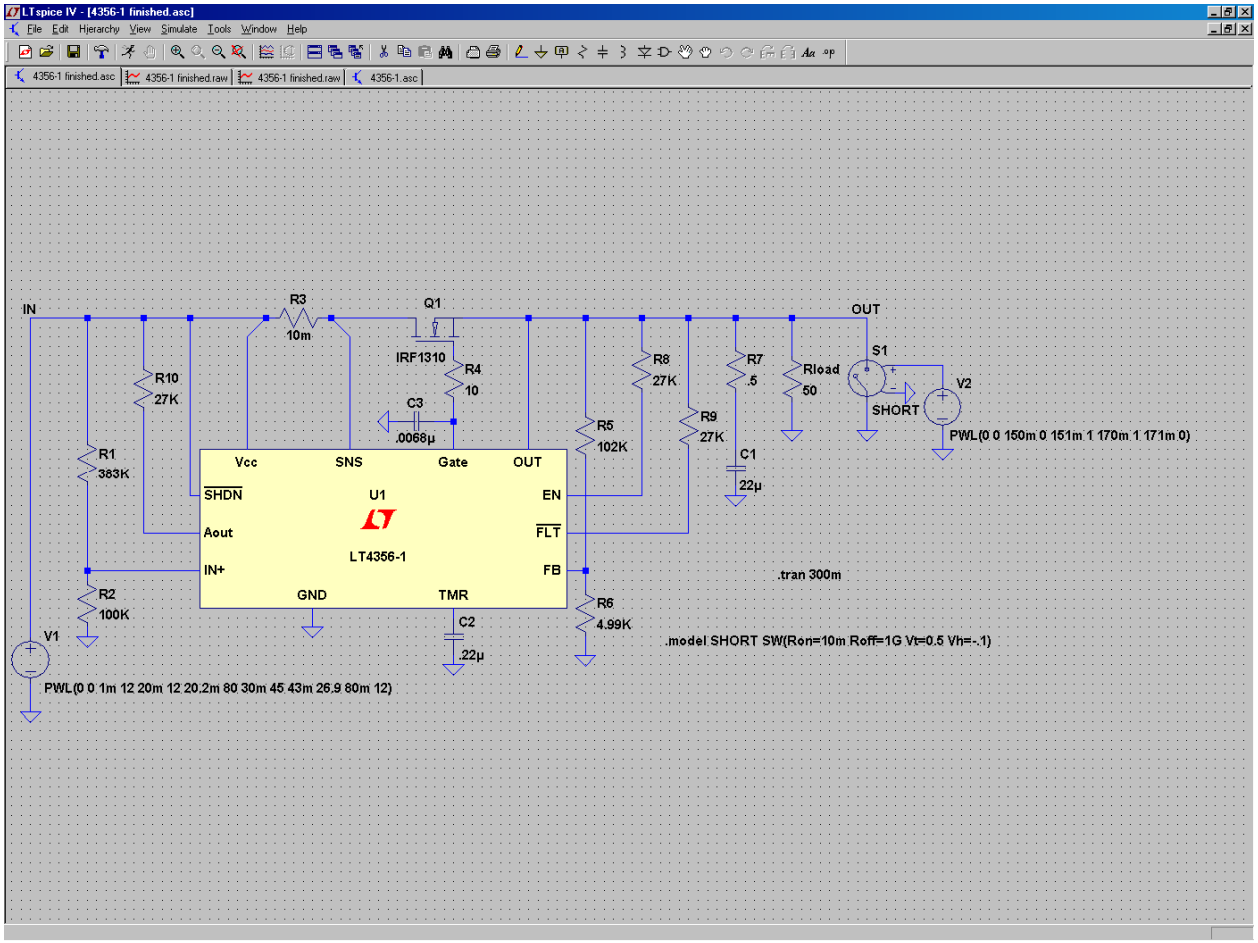
Example of Short Circuit

- **First, set up the switch and its stimulus.**



Example of Short Circuit

- Now, define the switch model.
- ex. .model SHORT SW(Ron=10m Roff=1G Vt=0.5 Vh=-.1)



Example of Short Circuit

PWL(0 0 150m 0 151m 1 170m 1 171m 0)

.model SHORT SW(Ron=10m Roff=1G Vt=0.5 Vh=-.1)

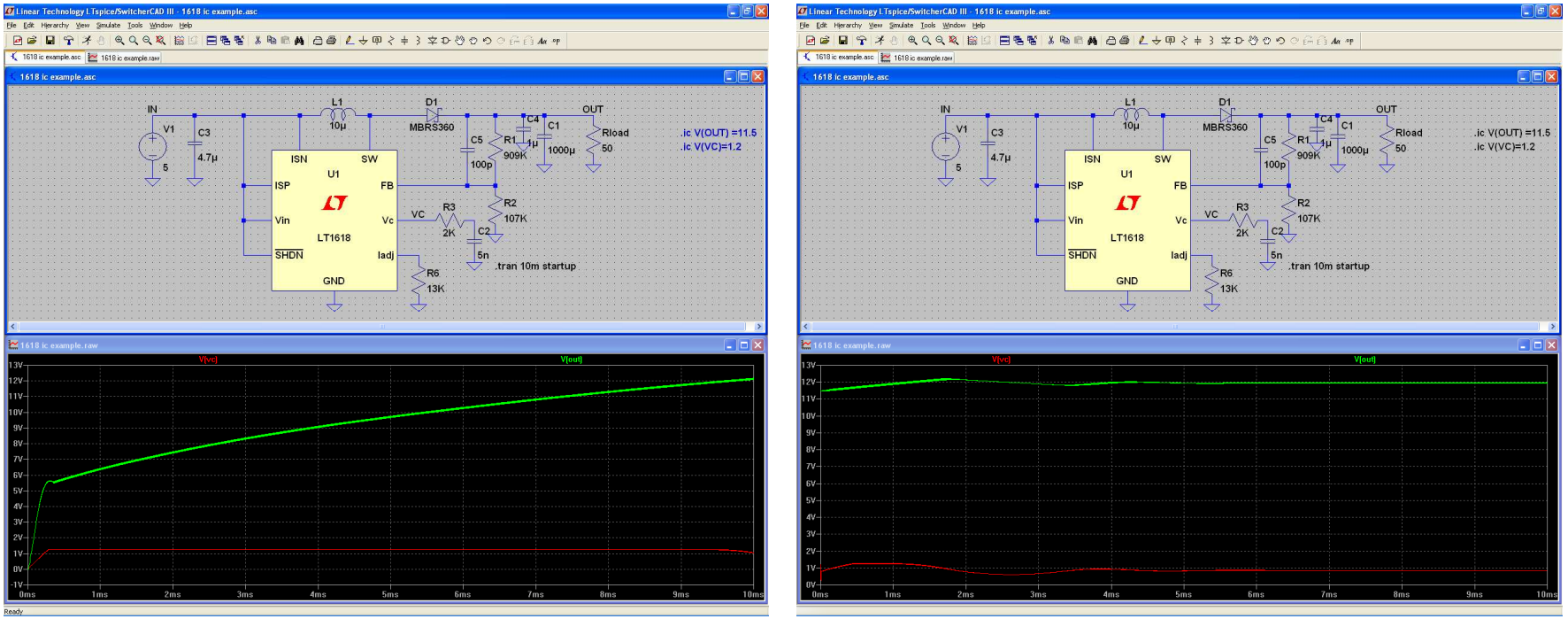
Improving Simulation Speed

Speed Up Techniques

- For a CPU, get one with as large as possible L2 or L3 cache and as high of clock speed as possible
  - SPICE is sparse matrix math intensive
- RAM speed is also important but pretty much automatically scales with a higher performance CPU
- RAM size is a contributing factor, but cache size has a much larger affect. RAM size primarily helps with regards to system performance when multiple applications are running
- A fast hard drive
- Consider disabling anti-virus scan of the .raw file type

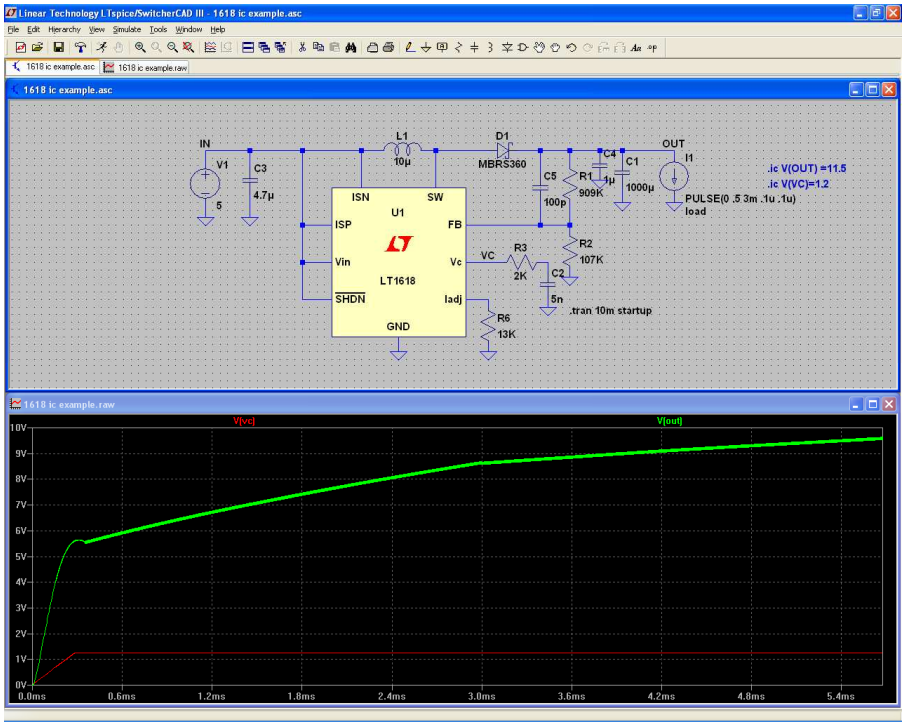
Speed Up Techniques

- Initial Conditions
  - Use .ic spice directive to set initial conditions
    - If output is going to 12V, let's start with it most of the way there!
    - It is sometimes useful to set other nodes to initial conditions as well. Ex. put an initial condition on the VC node



Speed Up Techniques

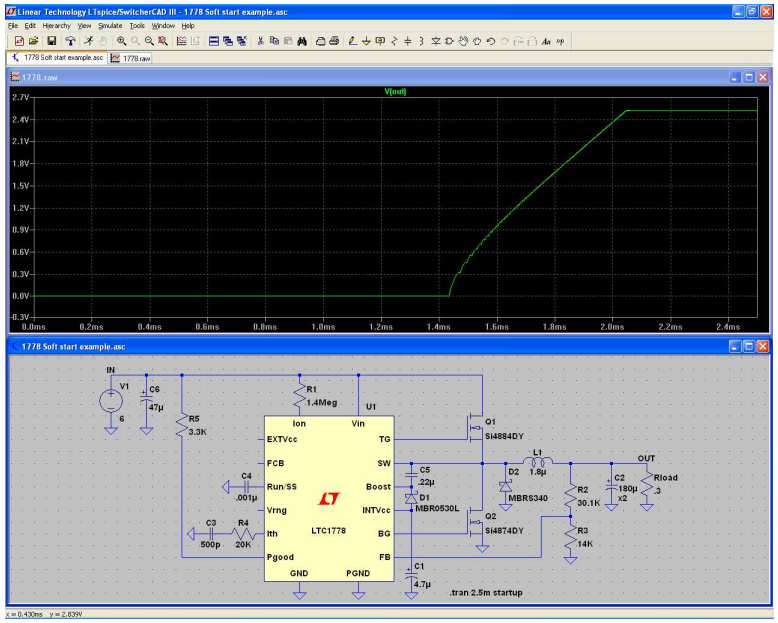
- Delay loads using a Pulse Current for a load
  - The time to get the load to the final value can be less if there is no load present during startup (all of the energy is then going into the output caps)
  - Notice the inflection at 3ms when the load turns on



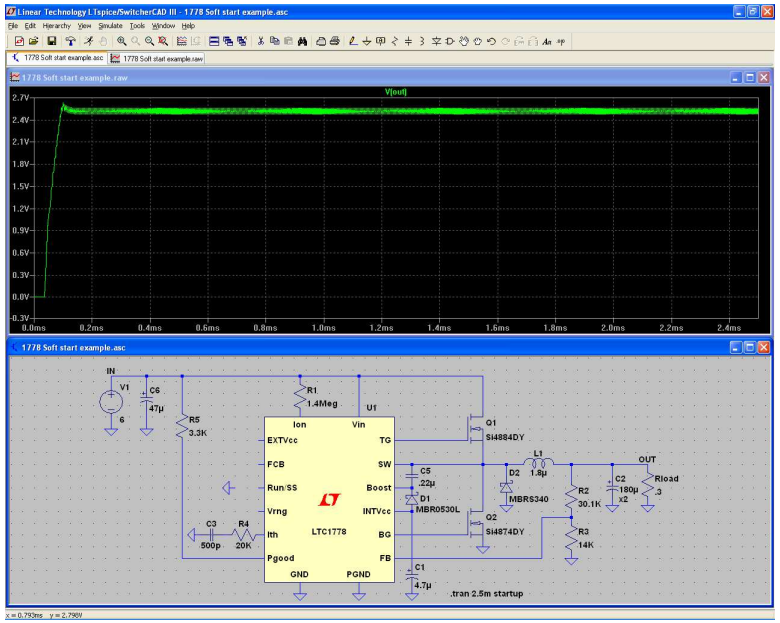
Speed Up Techniques

- **Remove or reduce the soft start from the circuit (frequently a cap)**

With soft start

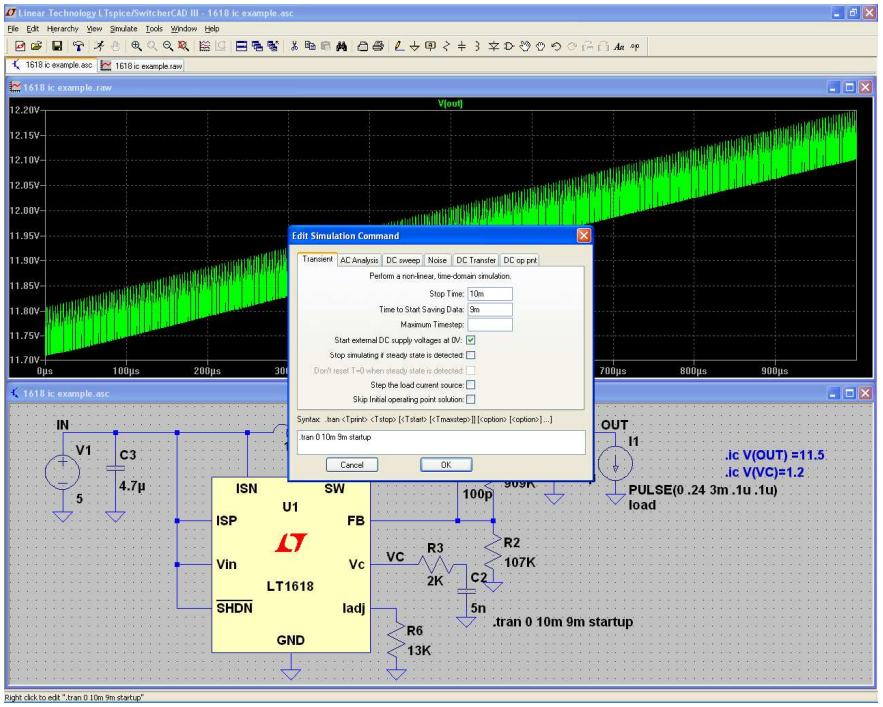


Without soft start



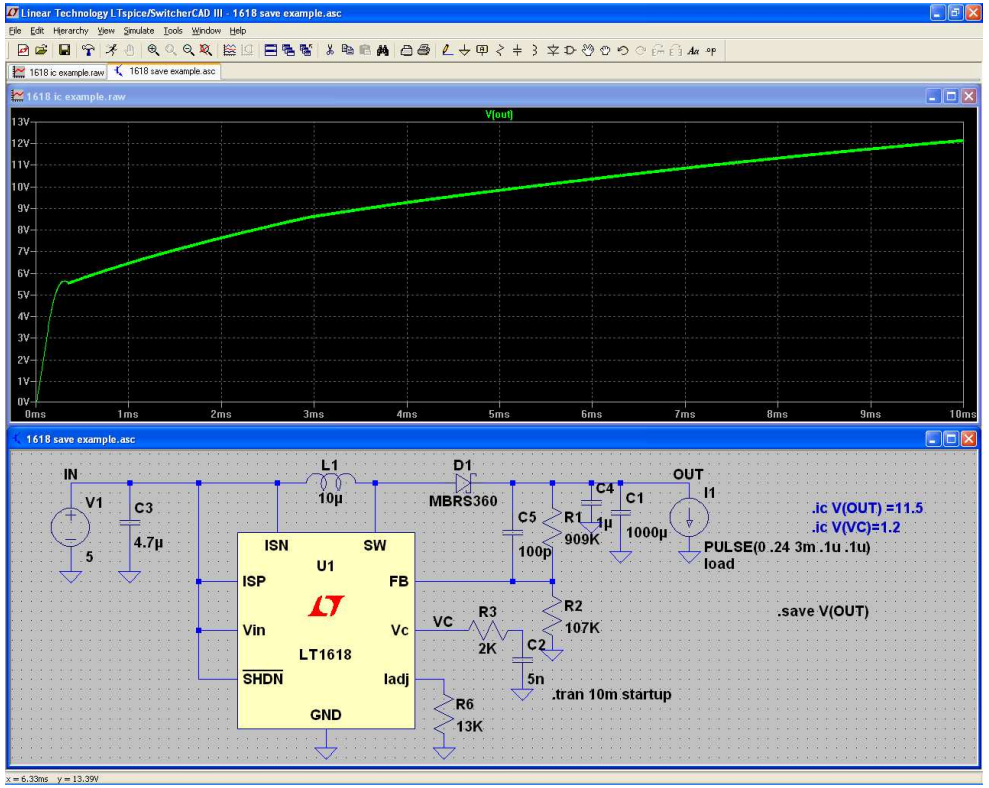
Speed Up Techniques

- Time to start saving data
  - Use this to instruct LTspice to not save any data until the time specified. Fewer things saved to memory/hard drive = more speed.
  - Waveforms before “Time to start saving data” time are lost and not viewable and the analysis data has been thrown away.
- Ex. 108 seconds vs 83 seconds for the 10ms transient analysis if data is only saved for the last 1msec



Speed Up Techniques

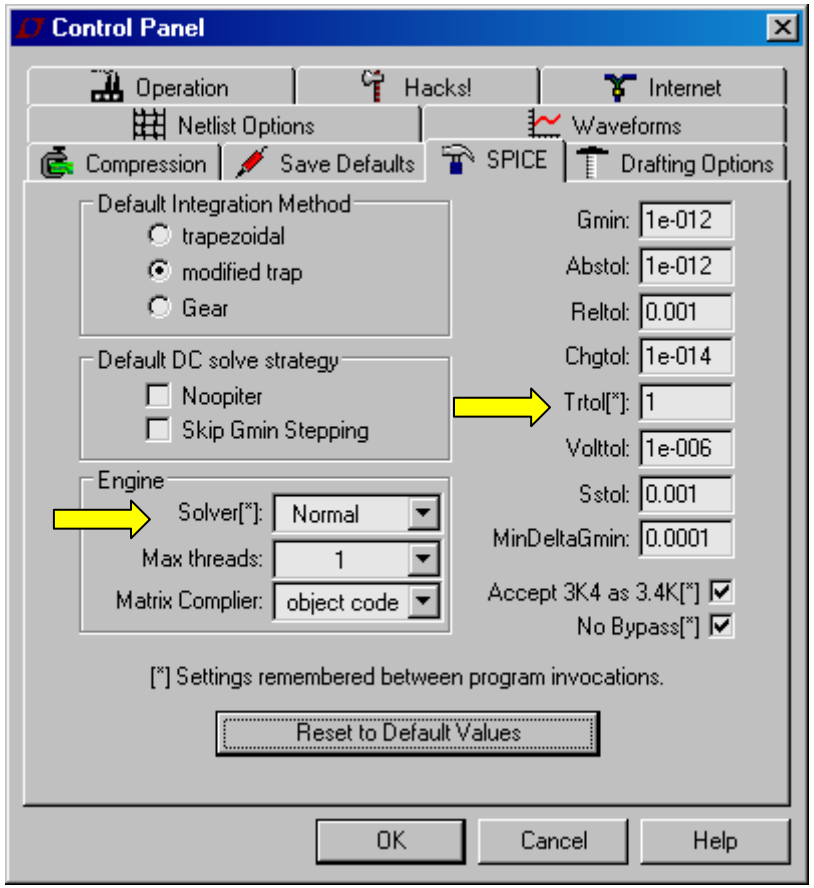
- Use the .save SPICE directive to save only the traces that you need
- Ex.: If you are only interested in Vout, use the .save V(OUT) SPICE directive to only save the OUT node data to the hard drive
- Only the saved nodes are viewable as a waveform, all other simulation data is discarded



Speed Up Techniques

- **Control Panel**
  - **Different Solvers – Normal is faster, but alternate in more accurate. Default is Normal.**

- Trtol (Transient error tolerance) - This parameter is an estimate of the factor by which the actual truncation error is overestimated. Most commercial SPICE programs default this to 7. In LTspice this defaults to 1 so that simulations using the SMPS macromodels are less likely to show any simulation artifacts in their waveforms. Trtol more affects the timestep strategy than directly affects the accuracy of the simulation. For transistor-level simulations, a value larger than 1 is usually a better overall solution. You might find that you get a speed of 2x if you increase trtol without adversely affecting simulation accuracy. Your trtol is remembered between program invocations.

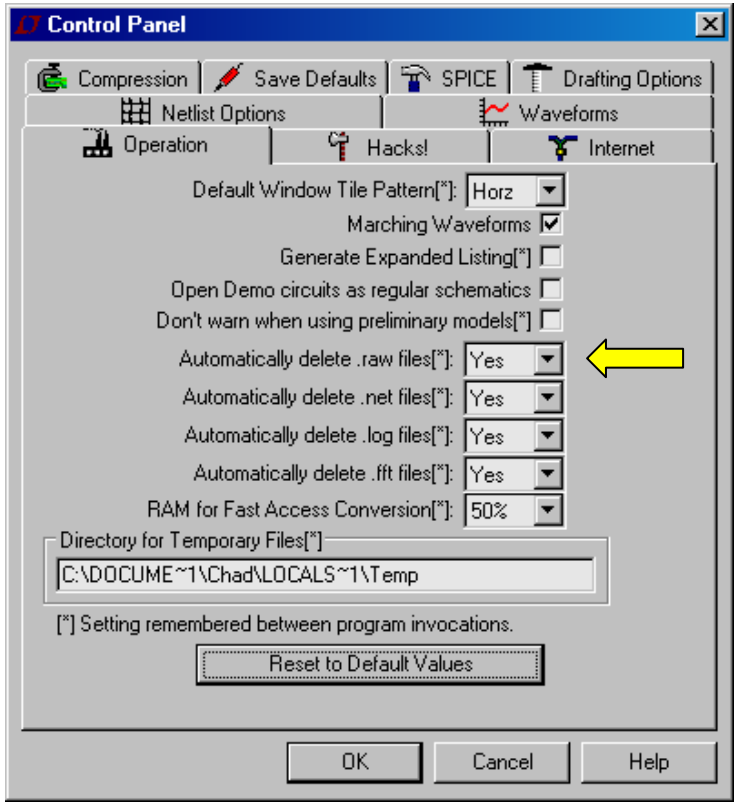


Fast Access File Format

- To reduce the time to plot a new trace from the data file, you can convert the file to an alternative, Fast Access format. This conversion can only be done after the simulation is completed when no new data will be added to the file.
- To convert the file, make the waveform window the active window and execute menu command =>Files=>Convert to Fast Access. This can also be done automatically after the simulation is run by using the .option fastaccess directive.
- Once the file is converted to this format, the load time of a new traces will be reduced typically by a factor equal to the number of data traces that have been saved in the file.
- See Fast.asc and Slow.asc for examples. Caution, these examples can take some time to run.

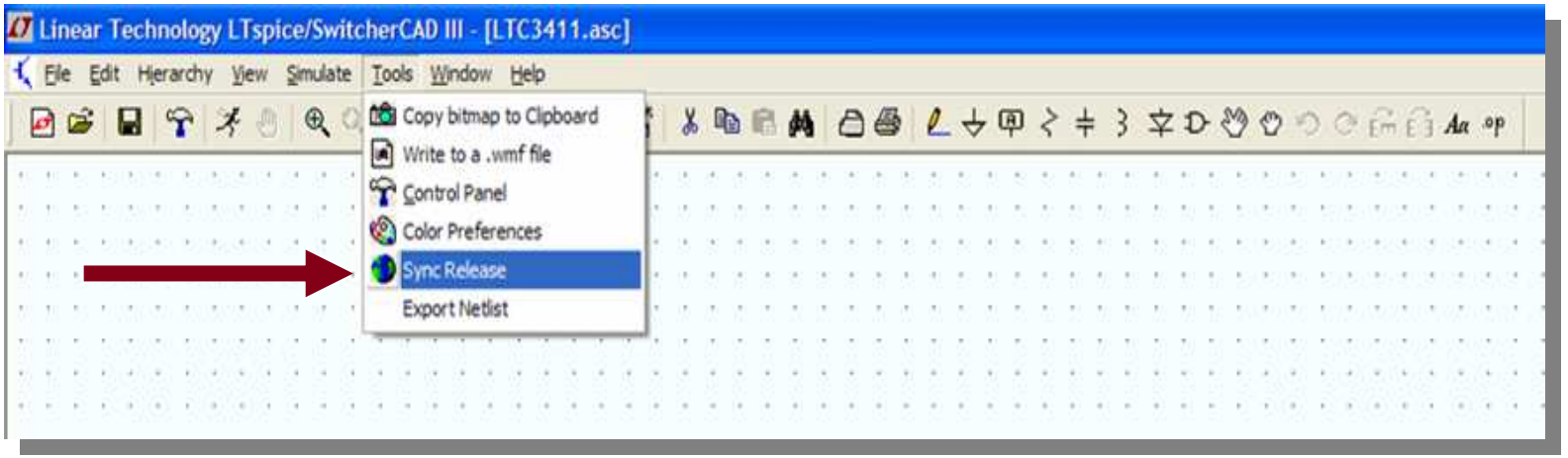
Other System Resource Tricks

- Pause – Under the Simulate Menu. Useful when you need to use your computing resources for something else temporarily.
- Have plenty of defragmented empty hard drive space. This speed up a simulation by a factor of 3 in extreme cases!
- Automatically delete .raw files (the waveform data file). Raw files can be very large (100's of megs +) depending on the number of nodes in a circuit, and the length of the simulation, etc. This option deletes the current raw file when LTspice is closed. This doesn't necessarily speed up simulations, but it helps to maximize free space on your drive.



Reminder to Periodically Sync Release

- Update your release of LTspice to get the latest
  - Software updates
  - Models and examples



Vista users

You must "Run as administrator" scad.exe even if you are logged in as an administrator

Thank you for attending, and happy simulating!

Homework: ***Once you return to the office, go back over the training materials within a week!***