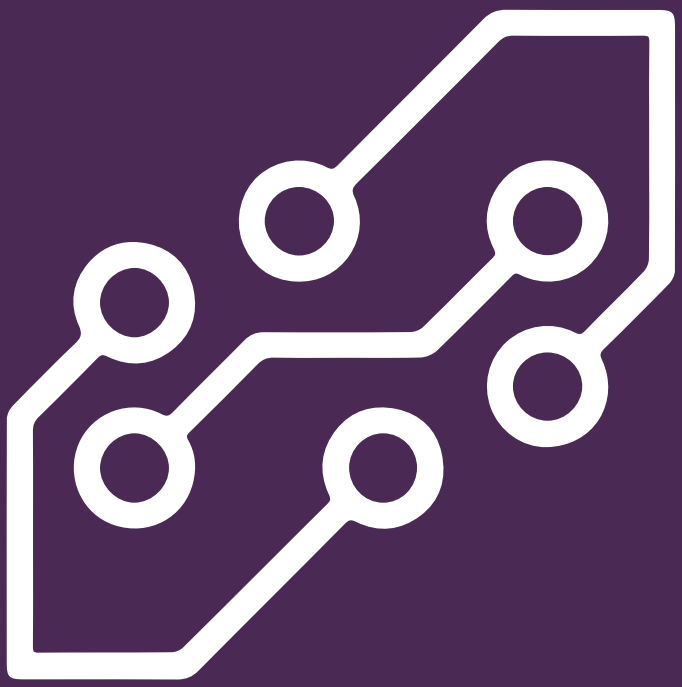
YOUR ROUTE TO DESIGN SUCCESS



EMA Design Automation®

MISSION CRITICAL
THE ROUTE NOT TAKEN

Routing is critical to success.

This may seem like a simple enough idea, but it really must not be understated. According to a Cadence user study, **over 50%** of total design time can be spent in the routing phase. This is why defining your routing process upfront is imperative to a smooth project flow that eliminates unnecessary confusion and can reveal possible speed bumps before they occur.

Preparing the board for routing is an important aspect of the design and begins with determining the placement strategy. After approval, you may move on to the other process steps. These steps will include power distribution, critical nets and constraints, routing, single nets, and final cleanup and verification. A smooth process definition will pave the way for success, ensuring a faster and more accurate turnaround.

Recommended process flow:

Preparing for Routing

1. Component Placement
2. Setting Boundaries
3. PCB Stack-up & Impedance Requirements

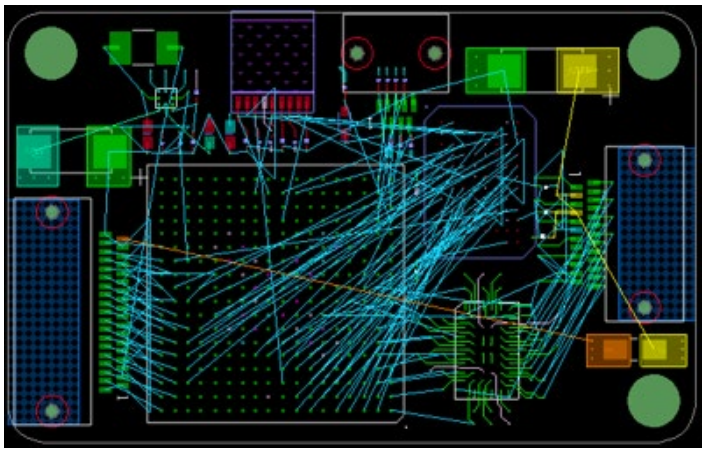
Routing

4. Constraints
5. Fanouts
6. Power Distribution
7. Critical Nets
8. Bulk Routing
9. Final Checks & Cleanup

PLACEMENT STRATEGY
LAYING THE GROUNDWORK

Defining your placement strategy is perhaps the most important step, as it paves the way for the rest of your design process.

Mechanical constraints should be evaluated and implemented (mechanical mounting holes, cut-outs, route keep-out regions). These should be looked at in the beginning, as they can be difficult and costly to correct further in the design process. Connector placements usually have specific x,y locations and should be completed first, followed by adding fixed components so they are locked in. The specific placement is a result of their function; other things plug into them, so they must make sense regarding the overall layout.



Large pin count devices should be placed next.

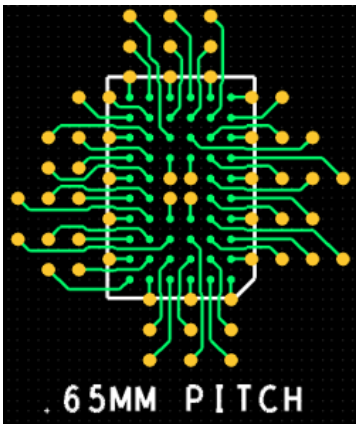
Use the signal rats' nest as a guide for orientation to minimize rats' nest twisting or crossovers for better signal flow and easy routing. Parts should be grouped together by function and the rats' nest optimized for routing, so components are close to each other. This will keep the nets short for better signal quality. Room properties within your CAD tool will greatly help here in sorting out your routes between parts, as they will keep the space between components within the acceptable tolerance. Lastly, decoupling caps should be placed near the device power pins and other sensitive nodes to increase their effectiveness.

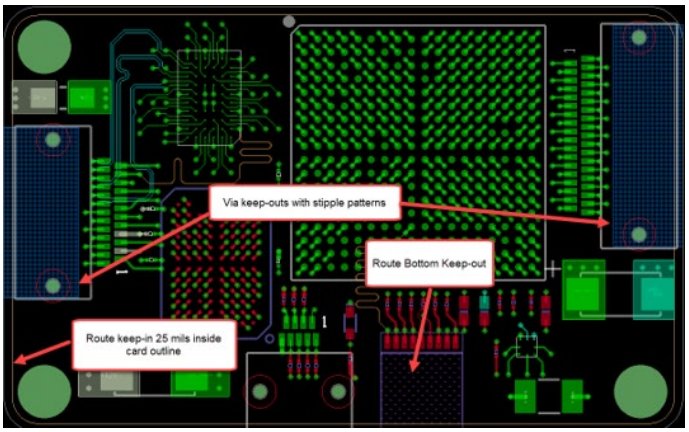
Laying the groundwork in this way will give you an organized base on which to build your design. Much like building blocks, the stronger your base, the sturdier and more reliable the overall structure will be. Though it may seem time-consuming to start, it will make the rest of the design process flow quicker and smoother for everyone involved.

PLACEMENT GRID
TIPS & BEST PRACTICES

Once the strategy has been mapped out, you can begin to place the parts.

First, consider how many layers you will need such as: layers for components, routing signals, power planes, and ground planes. As a best practice, parts can be placed on the coarsest grid based on the pin pitch of most of the parts, as your routing grid will be derived from it. For example, if most of the parts have a 50mil pin pitch, then the routing grid could be 5, 10, 25, or 50mil as a derivative. A mixture of imperial and metric components on the same board is not uncommon. As a rule of thumb, the best way to deal with this mix is to look to the majority to determine which you should use as a guide.





Set your boundaries by defining keep –ins and –outs.

Define route keep –ins to manage clearance of copper planes, vias, and trace routing to the board edge. Places where there are required special connectors with metal shells or cutouts on the board are areas to avoid routing through, as they can short signals. These areas can be managed with keep –outs defined in your placement rules.

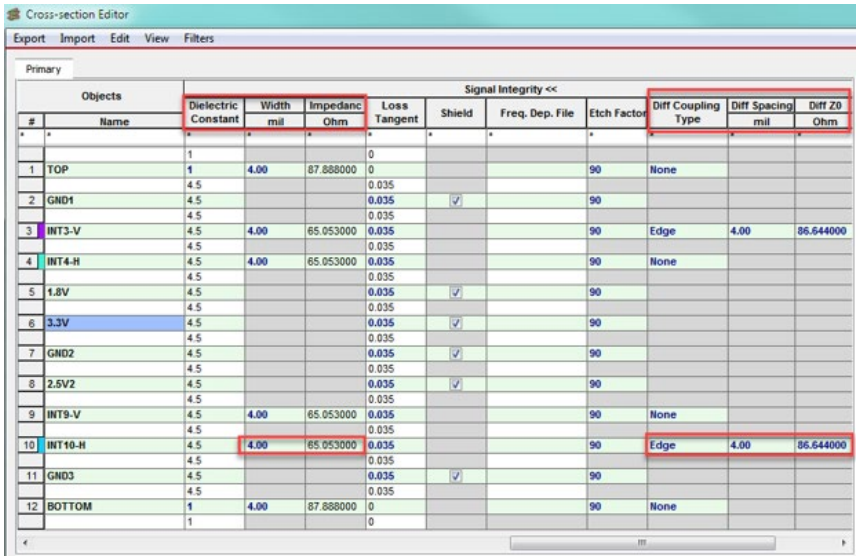
Additionally, be mindful of your manufacturing and assembly requirements. Routing layers should alternate between horzonal and vertical, and critical net routes should be sandwiched between ground layers. Consider areas where there are v-scores, break-off tabs, fiducials, and more, then adjust your keep –outs accordingly. Be aware of split planes, and only use split ground layers as a last resort. As a result of upfront work, the subsequent placement of your routing has a much higher chance of running smoothly without major setbacks.

PCB STACK-UP

IMPEDANCE RESULTS MAY VARY

Take care when defining your stack-up.

It has a direct impact on your differential impedance and single-ended impedance depending on the dielectric constant of the material you use. Impedance targets should also be modeled and evaluated before moving forward. Doing so may entail working with your board fabricator for approval, as they may only have specific materials in stock for a build. Communicating your impedance requirements with them will ensure any impedance is within a tolerable value and will reduce the need for rework later.



Objects		Signal Integrity <<										
#	Name	Dielectric Constant	Width mil	Impedanc Ohm	Loss Tangent	Shield	Freq. Dep. File	Etch Factor	Diff Coupling Type	Diff Spacing mil	Diff Z0 Ohm
1	TOP	1	4.00	87.888000	0			90	None		
2	GND1	4.5			0.035	☑		90			
3	INT3-V	4.5	4.00	65.053000	0.035			90	Edge	4.00	86.644000
4	INT4-H	4.5	4.00	65.053000	0.035			90	None		
5	1.8V	4.5			0.035	☑		90			
6	3.3V	4.5			0.035	☑		90			
7	GND2	4.5			0.035	☑		90			
8	2.5V2	4.5			0.035	☑		90			
9	INT9-V	4.5	4.00	65.053000	0.035			90	None		
10	INT10-H	4.5	4.00	65.053000	0.035			90	Edge	4.00	86.644000
11	GND3	4.5			0.035	☑		90			
12	BOTTOM	1	4.00	87.888000	0			90	None		

In your CAD tool, you should be able to model different impedance values based on the dielectric constant of various materials.

The results will help you define the physical width and gap spacing rules for the differentials pairs in your design. The ability to adjust it as-needed at this point in the process is invaluable, and can alert you to any potential spacing issues before they happen later, when rework can quickly become costly.

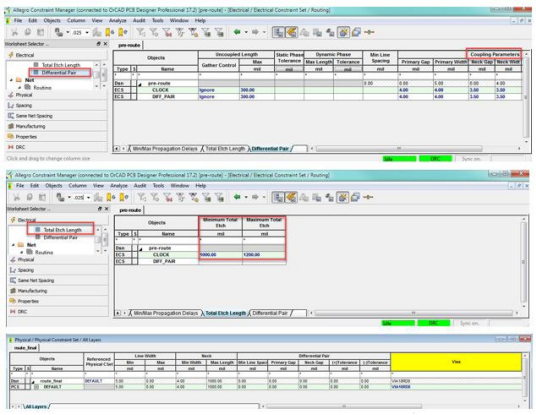
Additional things to be aware of when defining your stack-up are: trace width and space, layer height, and base copper weight. Each of these elements may vary depending on budget limitations and overall project error tolerances.

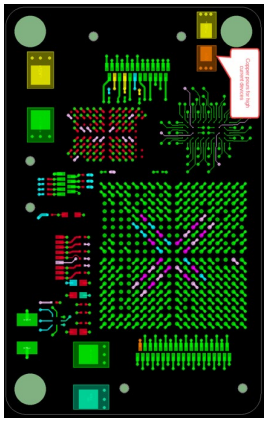
DEFINING CONSTRAINTS
AND FANOUT VIAS

The number of constraints and rules can be numerous and overwhelming.

Each net may have several rules associated with it, and trying to track all of them manually will give you no end of headaches. Ideally, you want to aim for perfection in matching items like trace length and impedance, as errors can result in EMI issues from crosstalk and noise. This is where a built-in constraint management environment within your CAD tools is critical in effectively managing these rules in real-time as your design progresses.

Differential pair parameters are defined in the electrical domain within a constraint manager. Length rules are defined for clock lines, matched groups, and critical nets. Physical trace widths, spacing rules, and via size should be defined by board density and current requirements for any high-power devices. Higher-current devices will have a wider trace width and larger vias to accommodate the current.





Fanouts are used to turn groups of traces into an informal pattern of vias optimized for routing.

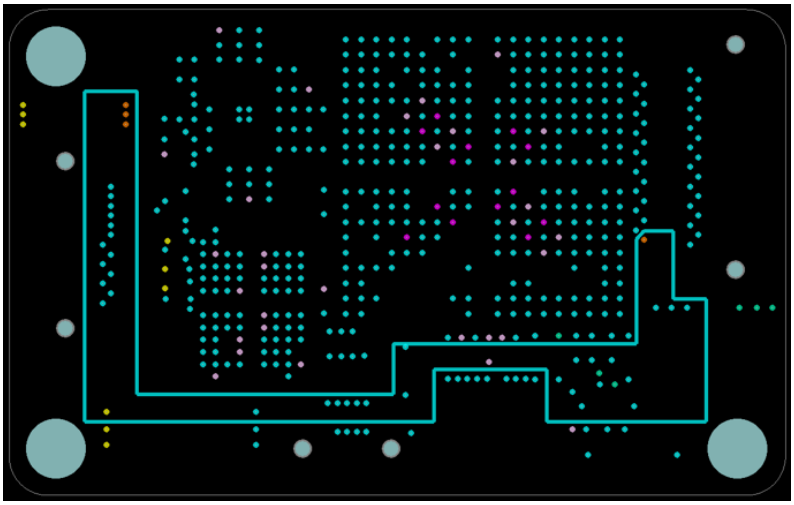
Additionally, fanout vias for signal pins allow access to multiple signal layers. This provides additional space and routing channels for designs with increased density and pin counts. Fanout vias for power must be established for power distribution and to complete connectivity to inner plane layers.

Creating the fan-out grid as a multiple of the pin pitch grid will make a uniform pattern in which to easily place your routing. If you have multiple parts that use the same package, and your CAD tool supports it, consider creating a library element of the fanout so it can easily be reused across all the similar packages. This can be the fastest way to complete test prep.

POWER DISTRIBUTION
PLAN ACCORDINGLY

The next step in the process flow is to ensure all your components receive the proper amount of power to optimize their performance.

This part should run smoothly if you have taken the proper organizational precautions in the previous steps. Done correctly, you should now have a bird's-eye view of the overall component placements and their respective constraints. Now, it is only a matter of connecting voltages to each place they need to go. Getting power to the board is one of the first steps of the schematic phase, and therefore can be the driver for which parts are chosen.



A tip: Use split-plane boundaries for separation between copper pours.

Utilizing split planes will save space and layers by providing power distribution on less layers throughout. This is especially effective if you have a large area where you can pour copper to create plane connections. Assigning colors to different power nets will also help determine split plane boundary locations. You can see this bounding line in the image above. It is usually created with anti-etch and has a minimum of a 10mil width. Separation widths between planes in high voltage areas may be increased to prevent arc-over.

Besides split planes, you can use power planes or power busses. When using power busses, be sure to keep them as wide as possible, as they have more DC resistance. For power planes, use separate planes for analog and digital, and add a ground plane next to each to reduce noise.

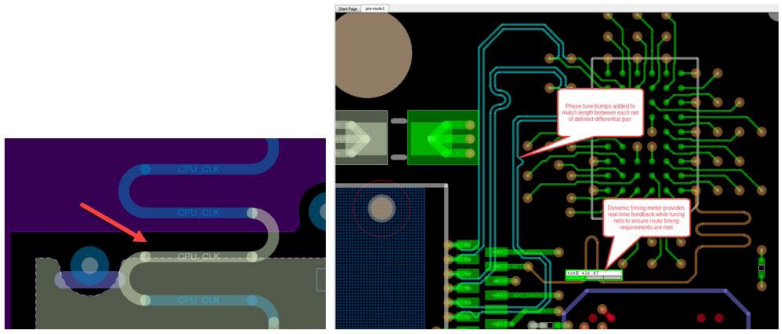
HOW DO I ROUTE THEE?

LET ME COUNT THE WAYS...

Routing Critical Nets

Perhaps the most time-consuming part of the process, you have finally arrived at the part of routing the PCB. Critical nets should be routed first and locked into place, as they must be routed to meet specific impedance and timing requirements. Some CAD tools have an interactive timing meter that will pass or fail based on timing requirements, making it easier for you to establish the correct routing before the next phase.

A common design practice in routing critical nets is to route high-speed signals in between solid planes rather than over plane splits. If a plane split is necessary, ensure the signal does not cross it. Otherwise, impedance discontinuities such as a signal bounce will impact the overall signal integrity along the route. Some CAD tools will also have a useful check in place called “segment over void” that will highlight areas where this crossover occurs.



Tip: Utilize pin swapping where you can for optimal routing.

Doing so will aid in untangling nets and provide the best routing path possible. Also, while it may seem obvious, double check the presence of grounds between all critical nets, keeping some distance between particularly noisey ones.

Clock traces should be kept away from other signals with more spacing, and add flight time delays and tune them as needed. Do not use multiple signal layers for clock signals, as keeping them on the same level will preserve the trace signal integrity. Terminating clock signals will reduce reflection, and point-to-point traces are ideal for direct signal communication. Lastly, avoid using multiple vias, as they can result in impedance mismatch and reflection.

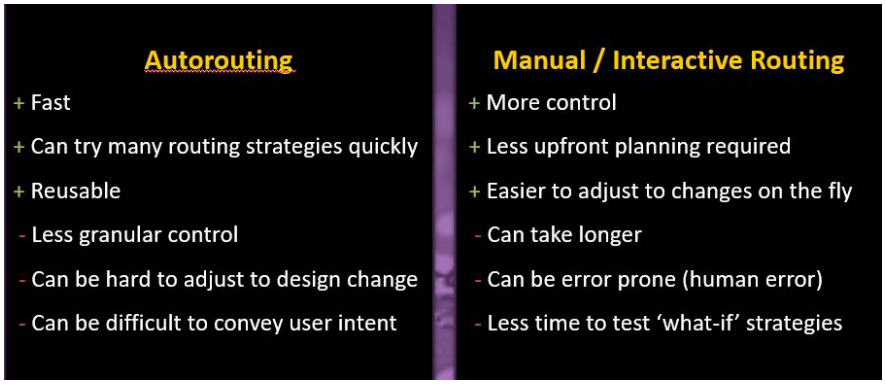
BULK ROUTING

TO AUTOMATE OR NOT– THAT IS THE QUESTION

Bulk Routing

Once all the critical signals are in place, bulk routing can occur. There are several options to consider on this step. Depending on the size of the board and the number of connections, an auto-router may be the logical option. Without proper setup and consideration, this can become a messy process that may yield less-than-perfect results.

In this way, manual or interactive routing will give you more control over the results but will take more time. When done correctly, an auto-router is a great tool for quickly trying many routing strategies, then producing a fast turnaround with reusable files. Ultimately, you must weigh the pros and cons of each solution against the needs of your project and determine the best course of action from there.



For best practice when bulk routing, keep long, parallel single-ended signals away from each other.

If this is not possible, ensure the ground is in between and/or routed on different layers to reduce the occurance of noise and cross-talk between the signals. A common rule-of-thumb is the 3W rule; keep trace space at least three times the width of a single trace measuring from center to center. This will prevent overcrowding and accidental crossovers.

Keep in mind a return path for ground, especially regarding high voltage nets and near voltage regulators. Filter power lines to reduce noise with capacitors where the power supply enters the PCB and voltage regulators, and try to place the capacitor as close to the source as possible. Lastly, check your trace widths to optimize performance and reduce voltage drops.

PCB ROUTE CLEANUP

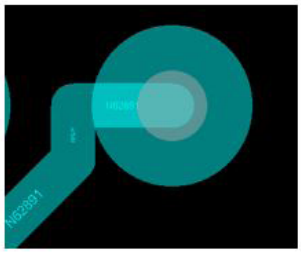
PROACTIVELY CATCH MISTAKES

After routing, you must look for route defects to clean up before sending the board onward in the manufacturing process.

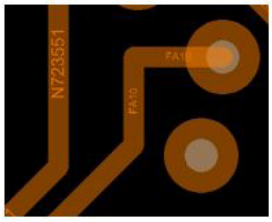
While it may seem banal, taking the time for a thorough inspection now can save you any number of unwanted hiccups in manufacturing, and will help prevent respins. A few things to keep an eye out for are 90-degree corners, non-ideal pad entry, and acute angles. Additionally, you can check for parallel line gaps, uncoupled differential pair segments, arc radius, non-arc corners, and miter or corner sizing. All these checks should be present in your constraint manager.

Additionally, ensure your board is properly grounded in all necessary areas, and that shielding is used where needed. Grounding is extremely important to the functional lifespan of the end-product, and errors can be disastrous. For more details on the process of grounding, read our ebook RF Design: The Wave of the Future.

Acute Angles



Non-ideal Pad Entry



90-degree corners

So how should you find and fix these errors?

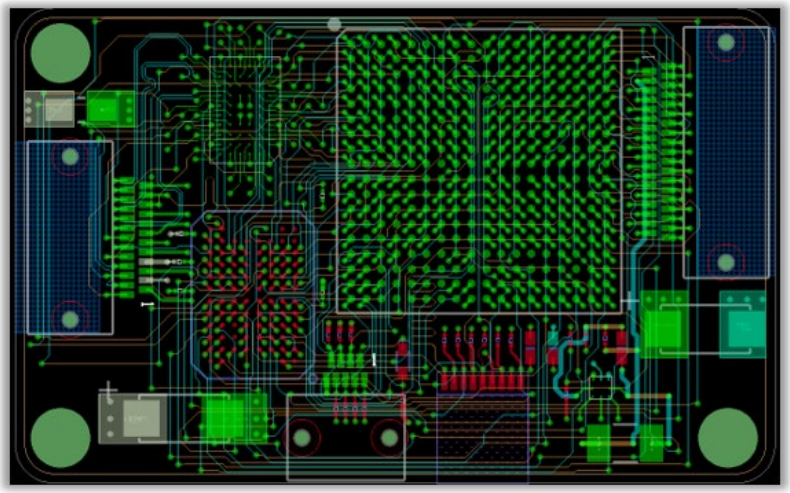
While manual inspection is always an option, it is tedious and prone to human error. These errors are compounded when the problem is not entirely visible at first glance, in cases such as noise, crosstalk, and timing. Ideally, your CAD tool will provide routines to help identify problems for you in real time. Being able to address all your errors at once as you design is a crucial time-saver that will help your project deadlines move along as they should. Therefore, it is important for your CAD tool to live up to the task at hand.

FINAL CONSIDERATIONS

MAKE YOUR CAD TOOL WORK FOR YOU

Even after this long process, chances are you will need to do several passes to ensure your design is manufacturable.

Each pass will undoubtedly take precious time and resources to complete. This is why it is important for your CAD program to provide a way to embed routing constraints and DFM rules and checking into the initial design process. The ability to provide your fabricator with a clean, manufacturable design is the best way to ensure a smooth project delivery every time. You can find more information on DFM best practices in our previous ebook, Ten Common DFM Issues and How to Fix Them.



It is crucial to have PCB design software to match your needs.

The OrCAD family of products has the enhanced design capabilities necessary to easily create, interface, and edit complex routing solutions in real time. Having the ability to catch errors as they occur and fix them before your board is sent to manufacture will vastly improve your productivity and time-to-market schedule.

For an OrCAD solution, contact us at info@ema-eda.com

EMA Design Automation®