EMC Design Rule Checkers

EMC design rule checkers provide an automated method for reviewing circuit board layouts to ensure that certain EMC design guidelines have been adhered to. Most design rules require information about component placement, trace routing and the signals on each trace. All of the rule checkers listed here are capable of reading board layout files to automatically obtain trace routing information. Information about the components and signals is obtained by one or more of the following methods:

- **Manually input by the user**
  - Can be extremely tedious, especially for boards with hundreds of nets.
  - Requires that the user be knowledgeable about signals on each net.
- **Inferred from net names**
  - Substrings such as "+3v", "gnd" or "clk" in a net name often provide important clues as to the nature of the signal on that trace.
  - Requires consistent naming conventions and can not provide detailed information about the nature of the signal required for many guidelines.
- **Obtained from "net classification" algorithms**
  - Requires a component database.
  - Usually only practical when the rule checker is part of larger design environment.
- **Obtained from IBIS files or circuit simulations.**
  - Some of the most critical signals on a circuit board may have been simulated for signal integrity purposes.
  - Some design rule checkers can import simulation data.

LearnEMC does not endorse any specific design rule checking software; however the following products (listed alphabetically) all have the ability to apply built-in and user-defined design guidelines (/guidelines.html) to a variety of printed circuit board layouts.

CST Boardcheck (https://www.cst.com/Products/CSTBC)

492 Old Connecticut Path, Suite 500
Framingham, MA 01701
United States

CST BOARDCHECK is an EMC and SI rule checking program that reads popular board files from Cadence, Mentor Graphics, and Zuken as well as ODB++ (e.g. Altium) files and checks the PCB design against a suite of EMC or SI rules. The kernel used by CST BOARDCHECK is the well known software tool EMSAT originally developed by IBM.

EMSAT (http://www.mossbayeda.com/products/emsat/emsat-overview)

Moss Bay EDA
Manufacturer’s Representative for IBM
23889 NE 112th Cir #2
Redmond, WA 98053

EMSAT is an EMC rule checker, developed by and for IBM EMC engineers, that reads in all popular board layout files and checks the design against a suite of EMC and SI rules. Violation viewing is available in three products: Allegro, Pantheon EMSAT Violation Viewer and the Simbeor BoardAnalyzer. Further investigation of violations found by EMSAT is possible through iQ-Harmony, using trace stimulus to analyze local spectral content, based on very fast algorithms developed at Missouri Science and Technology (formerly UMR).

EMISTREAM (http://www.nec.com/en/global/prod/emistream/)

NEC Informatec Systems, Ltd.
a subsidiary of NEC Corporation
Tokyo, Japan

EMC design rule checking software running under Windows that reads Allegro, Protel, Board Station and other board layout files. Nets are manually assigned properties in a spreadsheet environment.

HyperLynx DRC (http://www.mentor.com/pcb/hyperlynx/electrical-rule-check/)

Mentor Graphics, Inc.
Wilsonville, OR USA 97070-7777

HyperLynx DRC performs PCB design rule checks for issues affecting EMI/EMC, signal integrity, and power integrity. It can be used with board layout platforms by Mentor Graphics, Cadence and Zuken.

Zuken CR-8000 EMC Adviser EX (http://www.zuken.com/en/products/pcb-design/cr-8000/products/emc-adviser-ex)

Zuken, Inc.
Yokohama, Japan

EMC Adviser EX provides EMC design rule checking capability within the Zuken CR-8000 board development environment. Because the environment already has information on the nets and their signals, it is not necessary to manually identify most types of nets. This product cannot be run as a stand-alone rule checker.

Back to Top