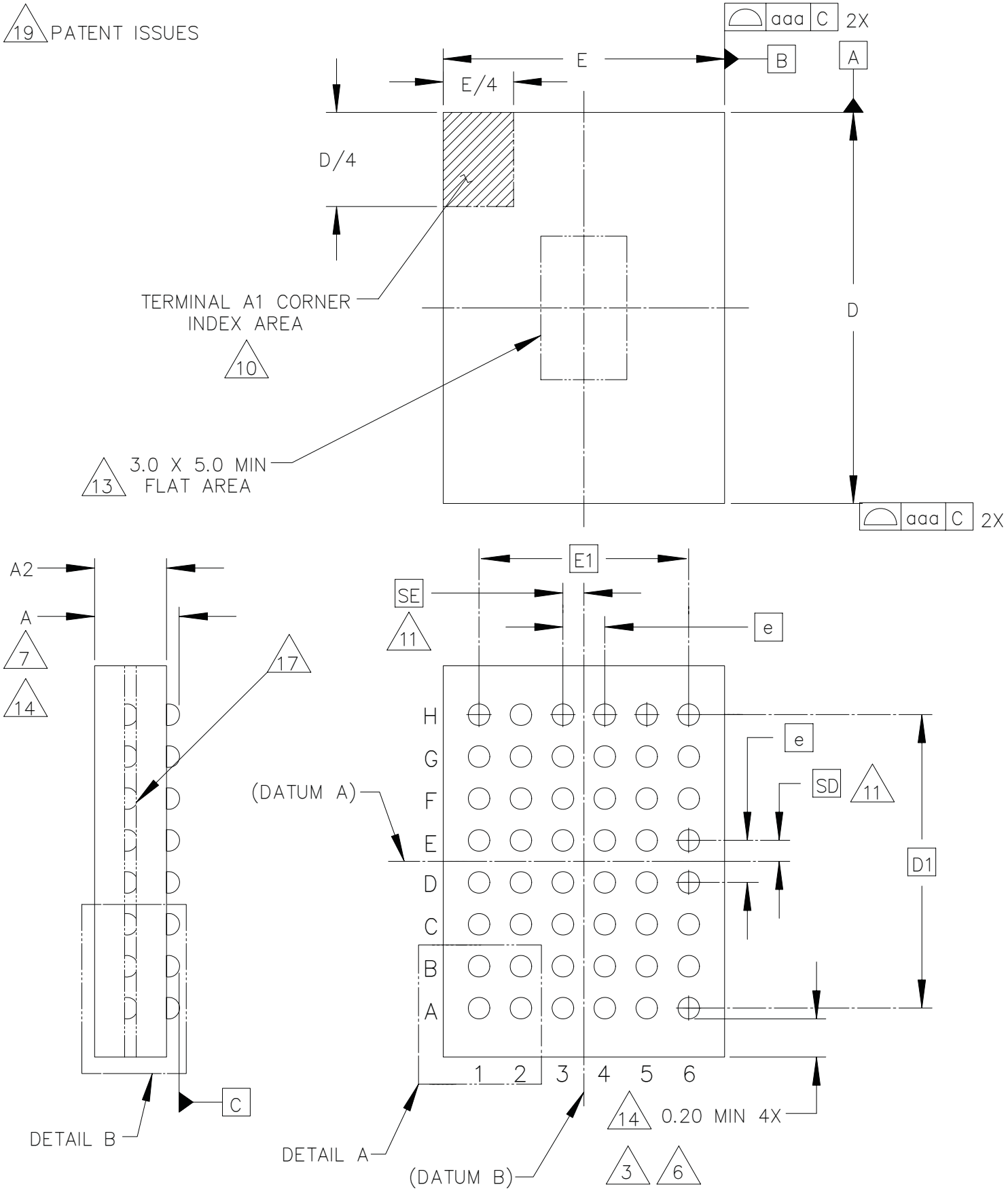
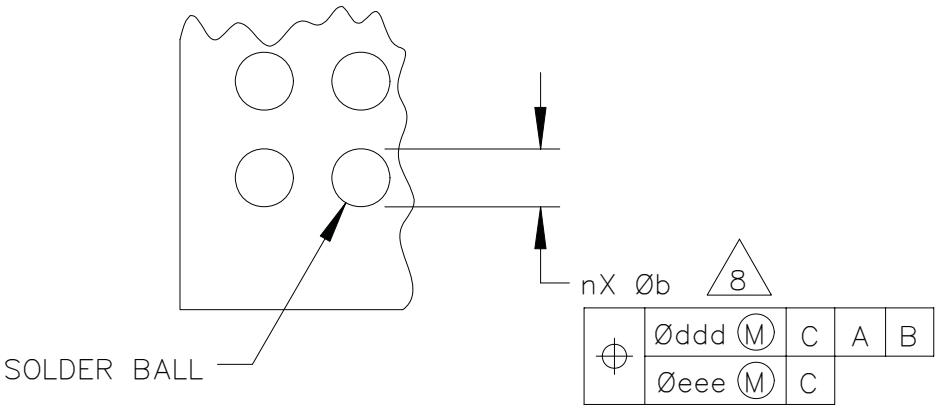
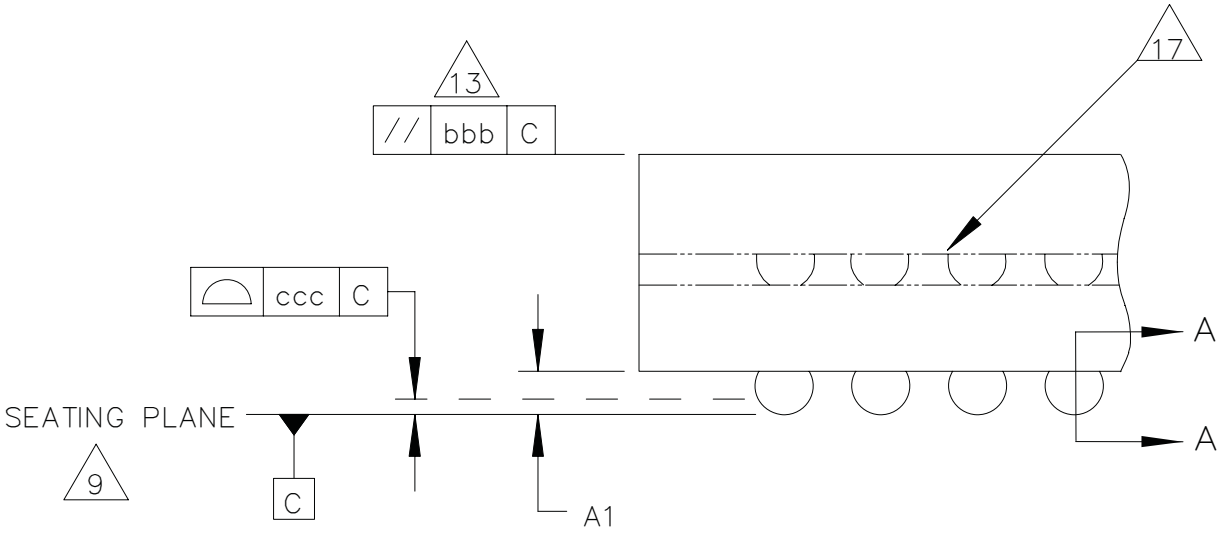


JEDEC SOLID STATE PRODUCT OUTLINE	THIS REGISTERED OUTLINE HAS BEEN PREPARED AND PUBLISHED BY THE JEDEC JC-11 COMMITTEE AND REFLECTS A PRODUCT WITH ANTICIPATED USE IN THE ELECTRONICS INDUSTRY. CHANGES ARE LIKELY TO OCCUR

TITLE:	PACKAGE DESIGNATOR:	ISSUE:	DATE:		PAGE:
RECTANGULAR DIE-SIZE, STACKED BALL GRID ARRAY FAMILY, 0.80mm PITCH	AF1R-PDSB	C	09/08	MO-242	1 OF 12



DETAIL A

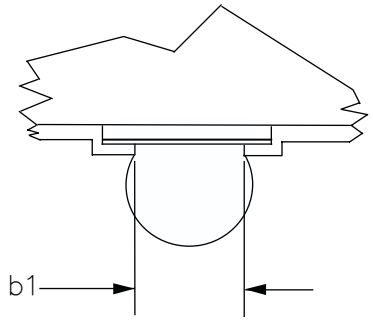


DETAIL B 17

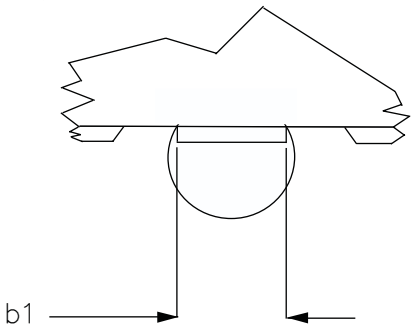
(ROTATED 90° CW)

SECTION A–A

Type 1 SMD
(Solder Mask Defined)

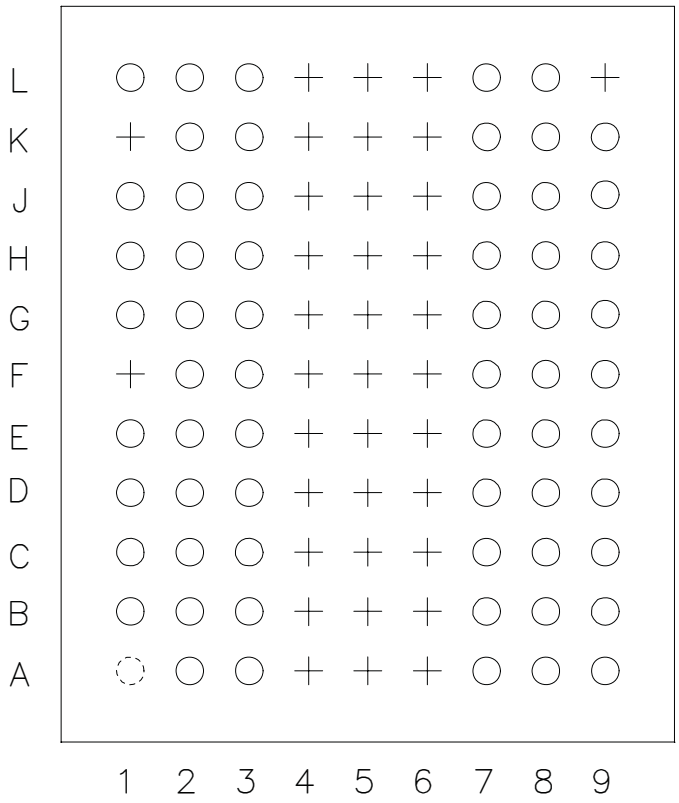


Type 2 NSMD
(Not Solder Mask Defined)

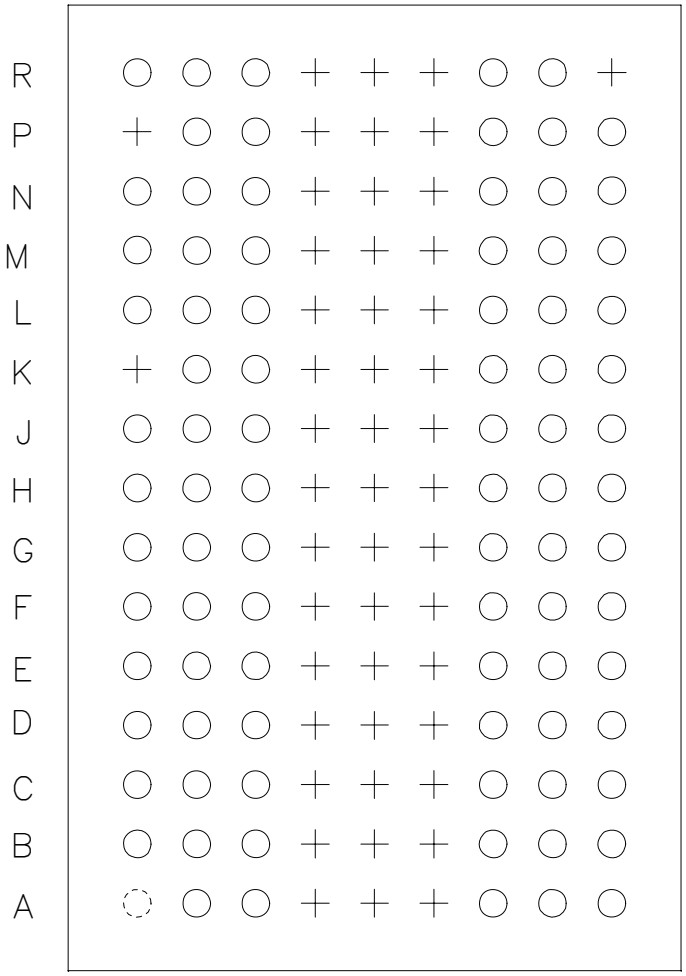


18

JEDEC SOLID STATE PRODUCT OUTLINE	TITLE: RECTANGULAR DIE–SIZE, STACKED BALL GRID ARRAY FAMILY, 0.80mm PITCH	ISSUE: C	DATE: 09/08	MO–242	PAGE: 2 OF 12



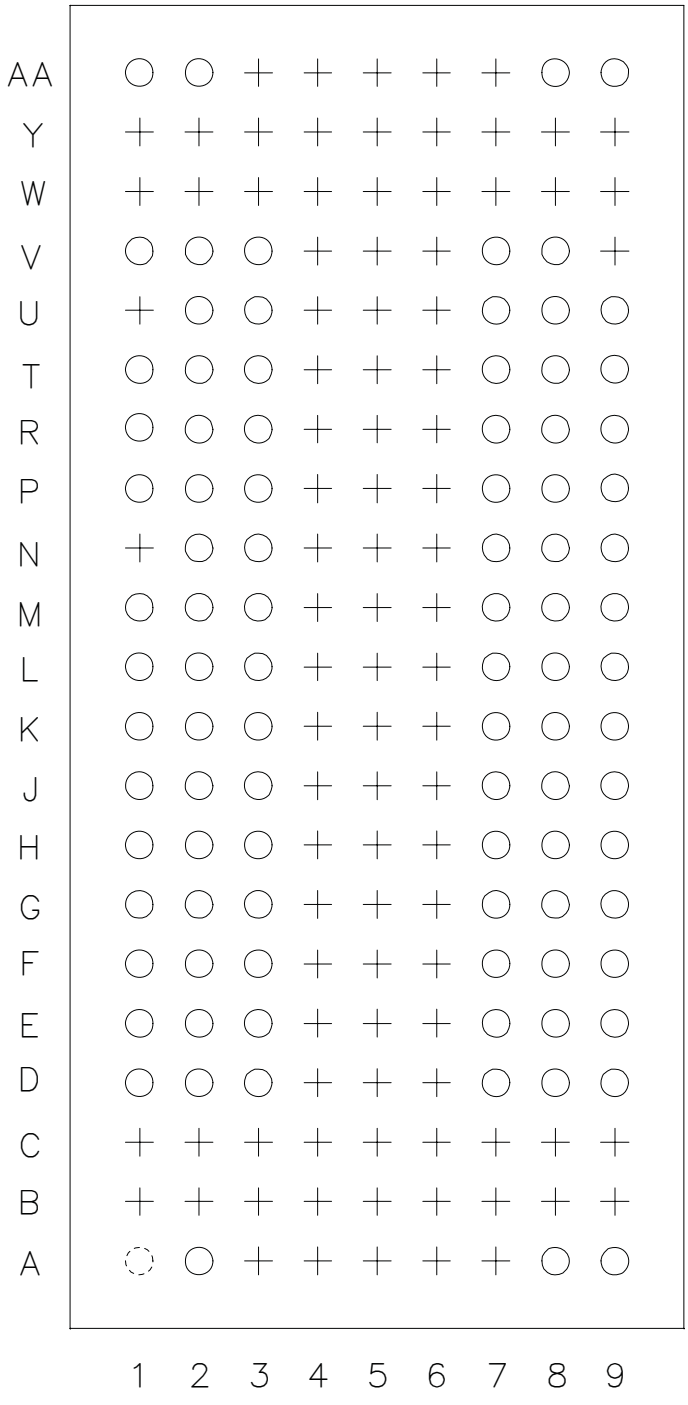
VARIATION AA



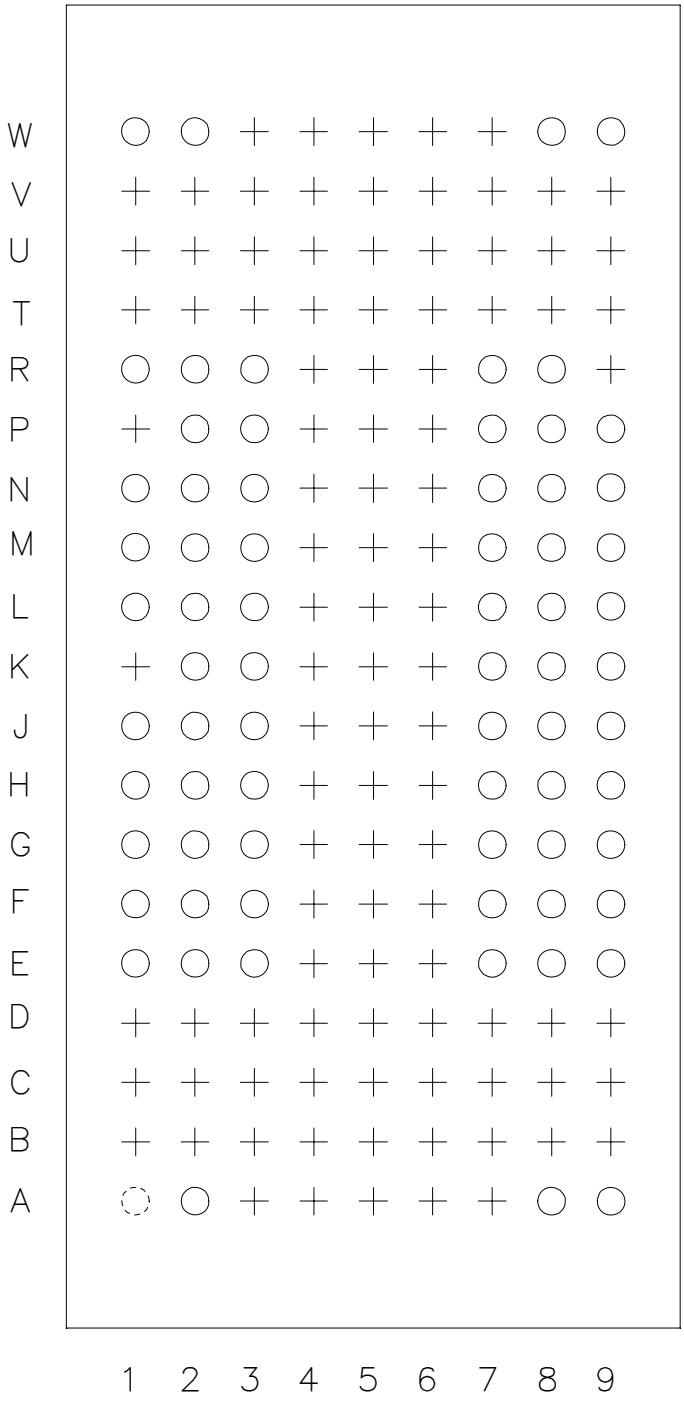
VARIATION AB

+ = DEPOPULATED BALL POSITION

JEDEC SOLID STATE PRODUCT OUTLINE	TITLE: RECTANGULAR DIE–SIZE, STACKED BALL GRID ARRAY FAMILY, 0.80mm PITCH	ISSUE: C	DATE: 09/08	MO–242	PAGE: 3 OF 12



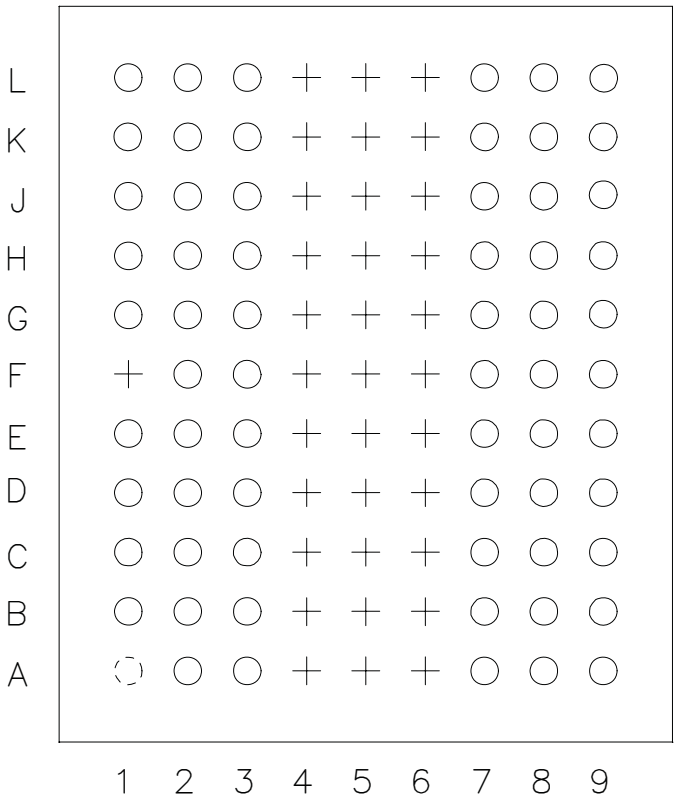
VARIATION AC



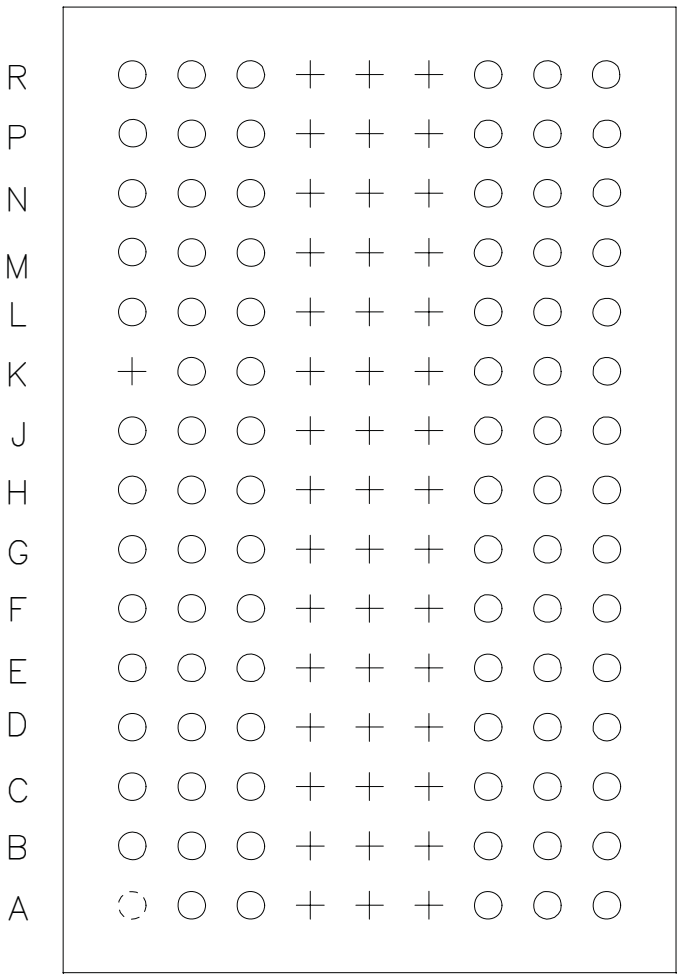
VARIATION AD

+ = DEPOPULATED BALL POSITION

JEDEC SOLID STATE PRODUCT OUTLINE	TITLE: RECTANGULAR DIE–SIZE, STACKED BALL GRID ARRAY FAMILY, 0.80mm PITCH	ISSUE: C	DATE: 09/08	MO–242	PAGE: 4 OF 12



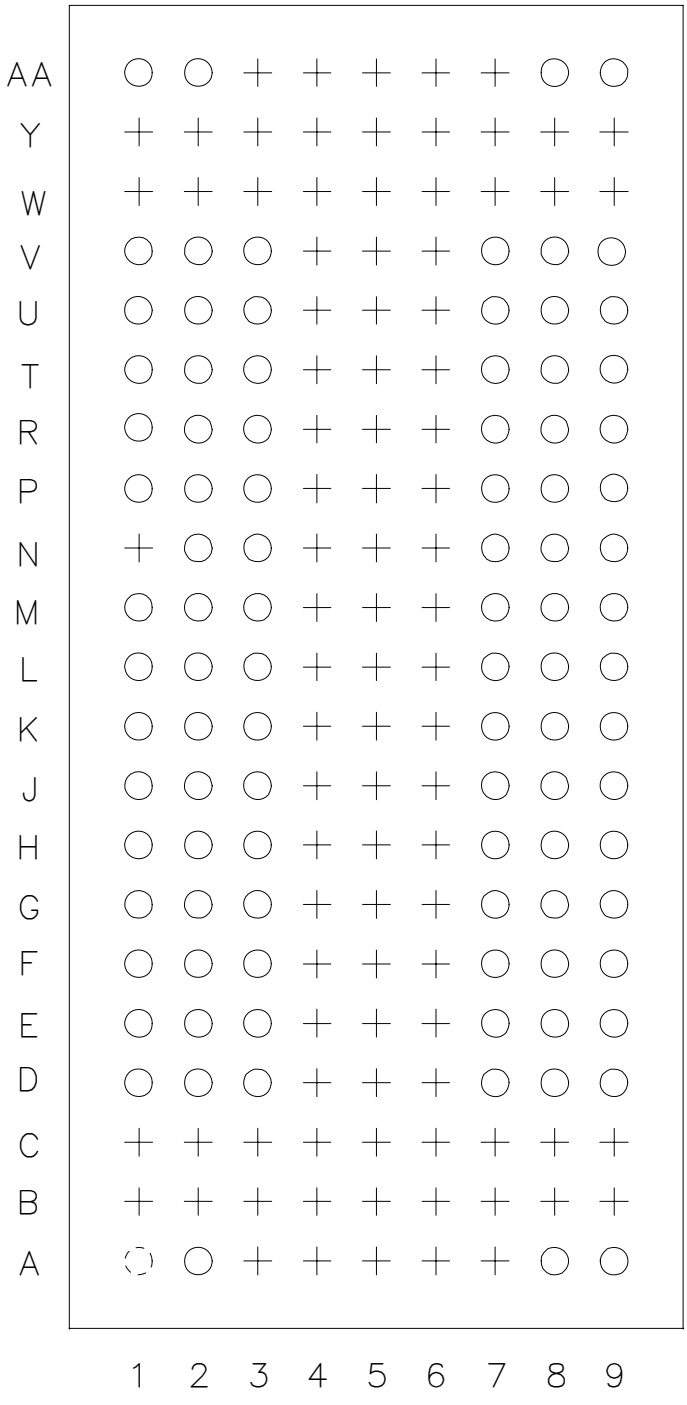
VARIATION BA



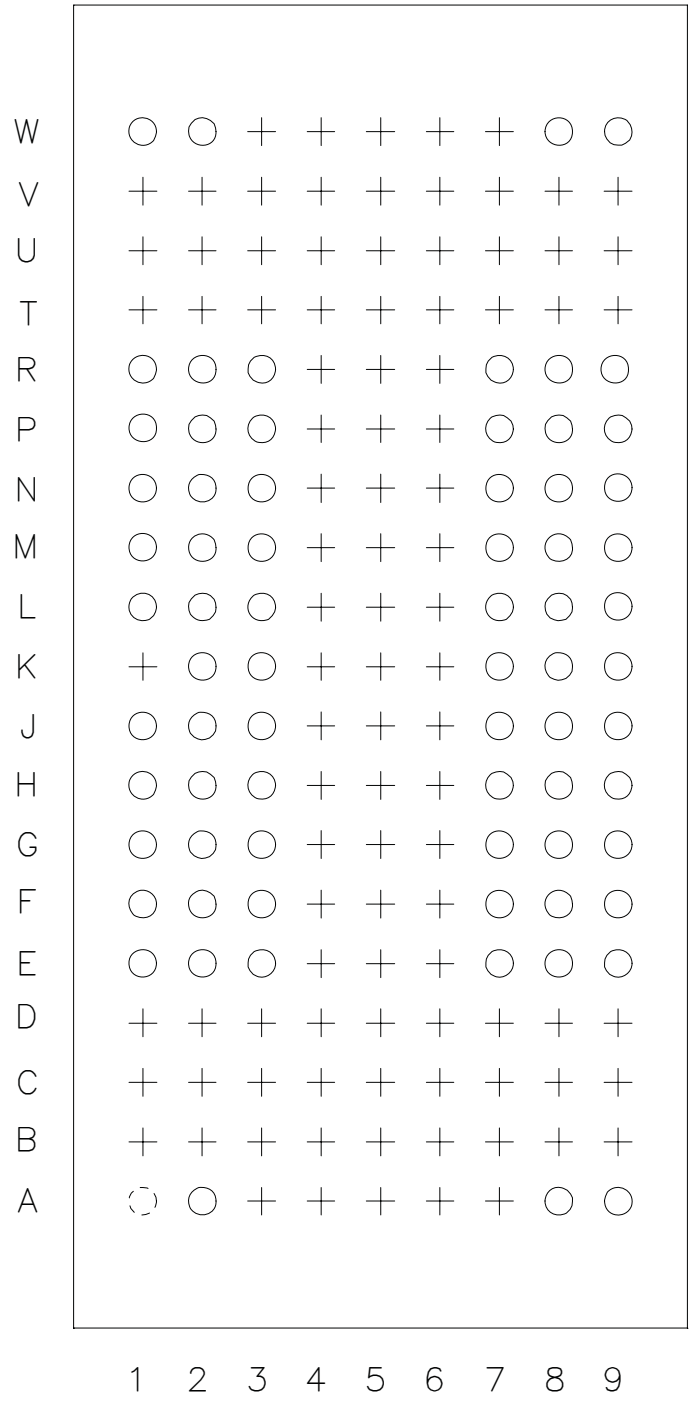
VARIATION BB

+ = DEPOPULATED BALL POSITION

JEDEC SOLID STATE PRODUCT OUTLINE	TITLE: RECTANGULAR DIE–SIZE, STACKED BALL GRID ARRAY FAMILY, 0.80mm PITCH	ISSUE: C	DATE: 09/08	MO–242	PAGE: 5 OF 12



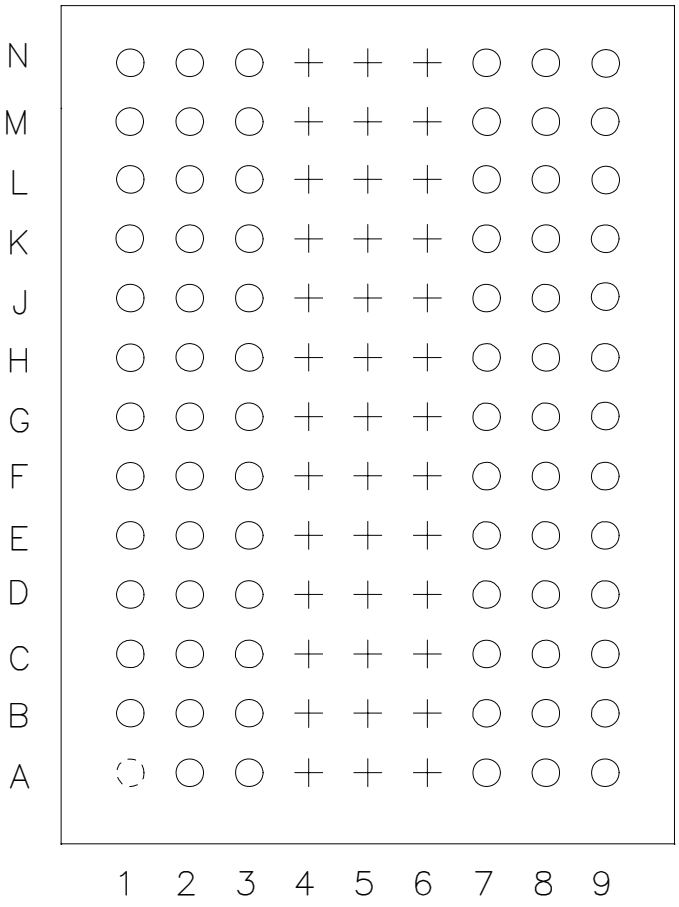
VARIATION BC



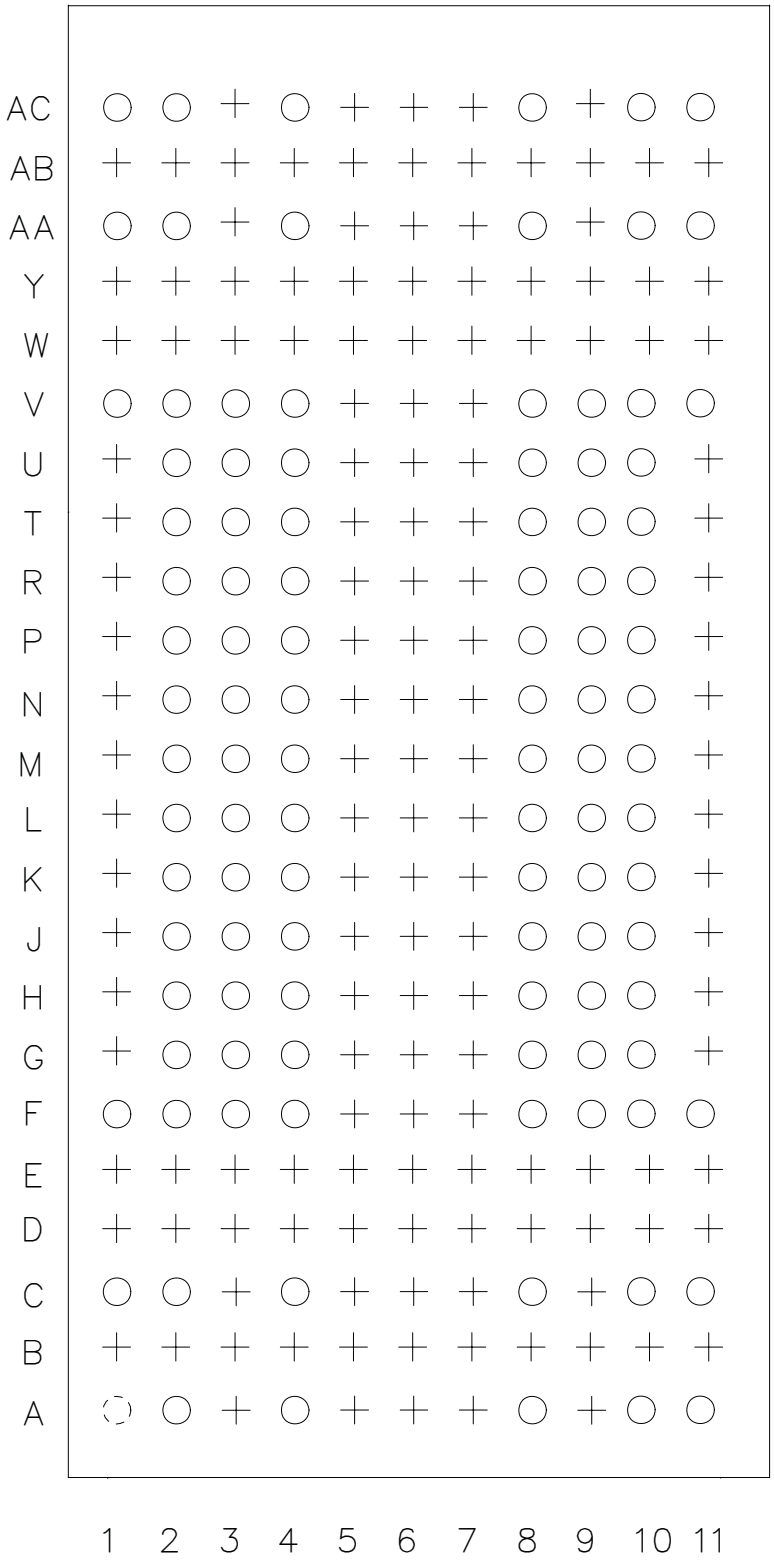
VARIATION BD

+ = DEPOPULATED BALL POSITION

JEDEC SOLID STATE PRODUCT OUTLINE	TITLE: RECTANGULAR DIE–SIZE, STACKED BALL GRID ARRAY FAMILY, 0.80mm PITCH	ISSUE: C	DATE: 09/08	MO–242	PAGE: 6 OF 12



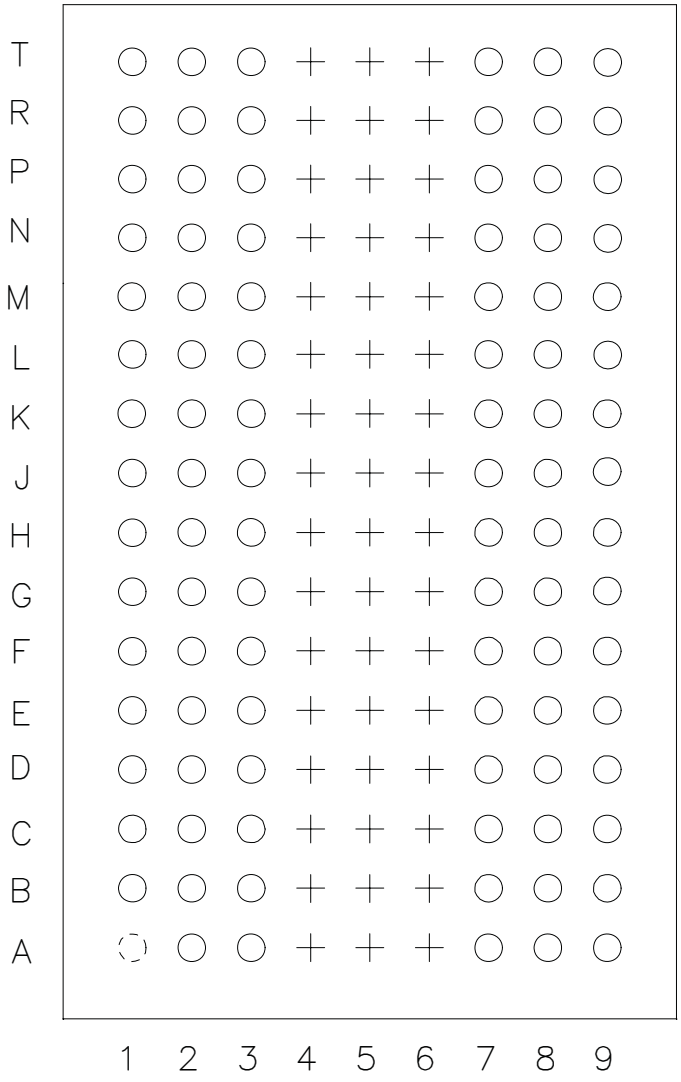
VARIATION CA



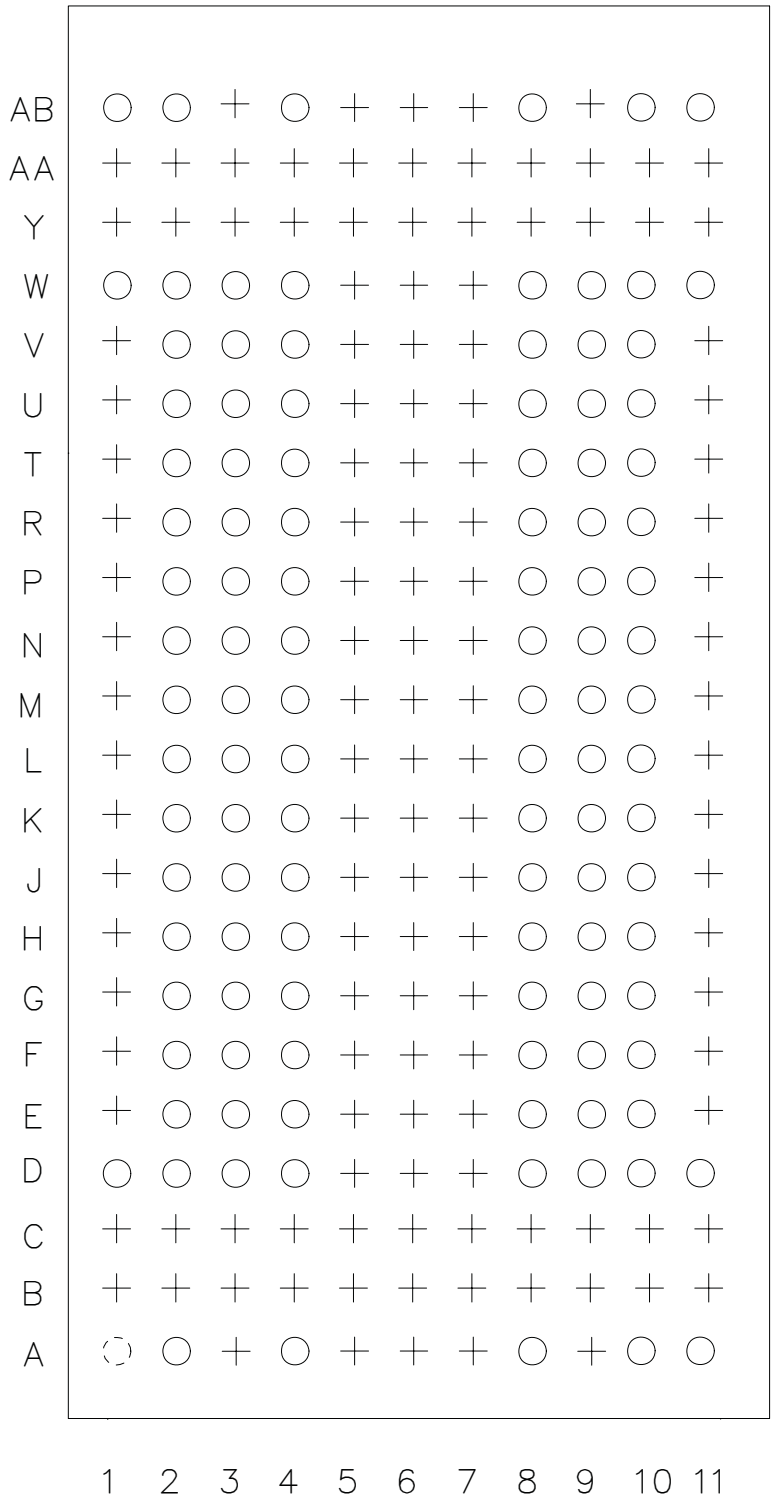
VARIATION CB

+ = DEPOPULATED BALL POSITION

JEDEC SOLID STATE PRODUCT OUTLINE	TITLE: RECTANGULAR DIE–SIZE, STACKED BALL GRID ARRAY FAMILY, 0.80mm PITCH	ISSUE: C	DATE: 09/08	MO–242	PAGE: 7 OF 12



VARIATION CC



VARIATION CD

+ = DEPOPULATED BALL POSITION

JEDEC SOLID STATE PRODUCT OUTLINE	TITLE: RECTANGULAR DIE–SIZE, STACKED BALL GRID ARRAY FAMILY, 0.80mm PITCH	ISSUE: C	DATE: 09/08	MO–242	PAGE: 8 OF 12

SYMBOL	COMMON DIMENSIONS			
	MIN	NOM	MAX	NOTES
A1	0.25	--	--	
A2	0.60	--	--	
b	0.40	0.45	0.50	8
b1	0.30	--	--	
e		0.80		4
REF		11-645		
ISSUE		A		
NOTES		1, 2, 16		

SYMBOL	TOLERANCES OF FORM and POSITION	
	VALUE	NOTES
aaa	0.15	
bbb	0.20	13
ccc	0.12	
ddd	0.15	
eee	0.08	
REF	11-645	11-645
ISSUE	A	A
NOTES	1, 2, 16	

VARIATIONS

VAR	D (MAX)	E (MAX)	D1	E1	MD	ME	n	SD	SE	A (MAX)	REF	ISSUE
AA	15.00	12.50	8.00	6.40	11	9	63	0.0	0.0	3.80	11-645	A
AB	18.00	12.50	11.20	6.40	15	9	87	0.0	0.0	3.80	11-645	A
AC	21.00	12.50	16.00	6.40	21	9	95	0.0	0.0	3.80	11-645	A
AD	21.00	12.50	14.40	6.40	19	9	71	0.0	0.0	3.80	11-645	A
BA	15.00	12.50	8.00	6.40	11	9	65	0.0	0.0	6.60	11.4-716	B
BB	18.00	12.50	11.20	6.40	15	9	89	0.0	0.0	6.60	11.4-716	B
BC	21.00	12.50	16.00	6.40	21	9	97	0.0	0.0	6.60	11.4-716	B
BD	21.00	12.50	14.40	6.40	19	9	73	0.0	0.0	6.60	11.4-716	B
CA	17.00	12.50	9.60	6.40	13	9	78	0.0	0.0	3.80	11.4-800	C
CB	22.00	12.50	17.60	8.00	23	11	106	0.0	0.0	3.80	11.4-800	C
CC	19.00	12.50	12.00	6.40	16	9	96	0.40	0.0	3.80	11.4-800	C
CD	22.00	12.50	16.80	8.00	22	11	112	0.40	0.0	3.80	11.4-800	C
NOTES					5	5	5,12	11	11	7,14		
			1, 2, 16									

NOTES:

1 DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.

2 ALL DIMENSIONING ARE IN MILLIMETERS.

3 SOLDER BALL POSITION DESIGNATION PER JEP 95. SECTION 3.0, SPP-020.

4 THE "e" REPRESENTS THE SOLDER BALL GRID PITCH.

5 SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. "n" IS THE ACTUAL NUMBER OF BALLS FOR MATRIX SIZE MD x ME AND DOES NOT INCLUDE BALLS FROM ANY DEPOPULATED LOCATIONS.

6 6 x 8 MATRIX IS SHOWN FOR ILLUSTRATION PURPOSES ONLY.

7 THIS DIMENSION INCLUDES STAND-OFF HEIGHT "A1", STACKING INTERCONNECT FEATURES, AND PACKAGE BODY THICKNESSES, BUT DOES NOT INCLUDE ATTACHED FEATURES, E.G., EXTERNAL HEATSINK OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AN ATTACHED FEATURE.

8 DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

9 PRIMARY DATUM C (SEATING PLANE) IS DEFINED BY THE CROWNS OF THE SOLDER BALLS.

10 TERMINAL A1 CORNER MUST BE IDENTIFIED ON THE TOP SURFACE BY CHAMFER, INK MARK, METALLIZED MARKINGS, INDENTATION, OR OTHER MEANS ON THE STACK BODY, LID OR INTEGRAL HEATSLUG. SOME ORIENTATION FEATURE ON THE BALL ATTACH SIDE IS RECOMMENDED.

11 BASIC DIMENSIONS SD AND SE ARE DEFINED WITH RESPECT TO DATUMS A AND B, AND LOCATE THE POSITION OF THE CENTER BALLS(s) IN THE OUTER ROW OR COLUMN OF A FULLY POPULATED MD x ME MATRIX. IF THE VALUE OF MD OR ME IS AN ODD NUMBER, THEN SD OR SE = 0; IF IT IS AN EVEN NUMBER, THEN SD OR SE = e/2 .

12 SOLDER BALL ARRAY MAY BE DEPOPULATED BY OMISSION OF BALLS FROM A FULL MD x ME MATRIX.

13 PARALLELISM ON THE TOP SURFACE (bbb) APPLIES ONLY TO THE 3.0mm X 5.0mm MINIMUM FLAT AREA SHOWN ON THE TOP VIEW (SHEET 1). THIS AREA MAY BE USED FOR MARKING OR VACUUM PICKUP

14 THIS IS A CONTROLLING DIMENSION.

15 MAXIMUM BODY SIZES (D AND E) ARE DERIVED FROM ACTUAL BODY SIZES ROUNDED TO THE NEXT HIGHEST 0.50MM INCREMENT (X.00 OR X.50) ACTUAL VALUES FOR D AND E MUST BE OBTAINED FROM STACK PRODUCER.

16 THESE PACKAGES ARE USED MAINLY FOR MEMORY DEVICES.

17 AREA CONTAINS VERTICAL INTERCONNECT BETWEEN UPPER AND LOWER DEVICES, EXACT DESIGN OF THIS FEATURE IS OUTSIDE THE SCOPE OF THIS DOCUMENT. INTERNAL DETAILS SHOWN FOR ILLUSTRATION PURPOSES ONLY AND ARE NOT INTENDED TO IMPLY PART ORIENTATION, PART QUANTITY, CONFIGURATION OR ASSEMBLY.

NOTES:

18 THE SOLDERABLE SURFACE MAY BE DEFINED BY AN OPENING IN THE SOLDER RESIST LAYER (Type 1 "SMD") OR BY THE SIZE OF A METALIZED PAD (Type 2 "NSMD"). IT MAY BE ELLIPTICAL PROVIDED THE RATIO OF THE MAJOR TO MINOR AXES IS NO GREATER THAN 2/1, AND THE SURFACE AREA IS NO LESS THAN THE MINIMUM FOR A CIRCULAR PAD. FOR TYPE 2 DESIGNS, EXPOSED COPPER TRACES ARE PERMITTED OUTSIDE THE b1 PAD AREA.

19 MICRON AND ENTORIAN TECHNOLOGIES HAVE STATED THAT CERTAIN U.S. PATENTS AND PATENT APPLICATIONS MAY APPLY TO CONFIGURATIONS OF THIS OUTLINE. THESE PATENTS AND APPLICATIONS INCLUDE:

MICRON	PATENTS: 6,013,948 6,027,233 6,522,018 6,746,894
ENTORIAN	PATENTS: 6,576,992 6,473,308 6,426,240 6,262,895 PATENT APPLICATIONS: 10/400,309 10/435,192 10/900,073 10/900,265 11/040,564 11/051,815 11/197,267 11/258,438 11/316,505 11/317,425 11/403,081

MICRON AND ENTORIAN INTEND TO COMPLY WITH THE JEDEC PATENT POLICY.

Change Record

If the change involves any words added or deleted (excluding deletion of accidentally repeated words), the change is to be included below. Punctuation changes may or may not be included.

Initial Issue: A	Date: 04/03	JC11 Item Number: 11–645

Change Record History		
Issue: B	Date: 07/06	Item Number: 11.4–716
Description of Changes		
Added variations BA, BB, BC, and BD to support 4–High DDR–2 stacks as defined by JC42.3 Item 1486. Added section AA in compliance with current design guide.		
Issue: C	Date: 09/08	Item Number: 11.4–800
Description of Changes		
Added variations CA, CB, CC, and CD to support DDR–3 stacks as documented in JEDEC Standard No. 79–3B.		