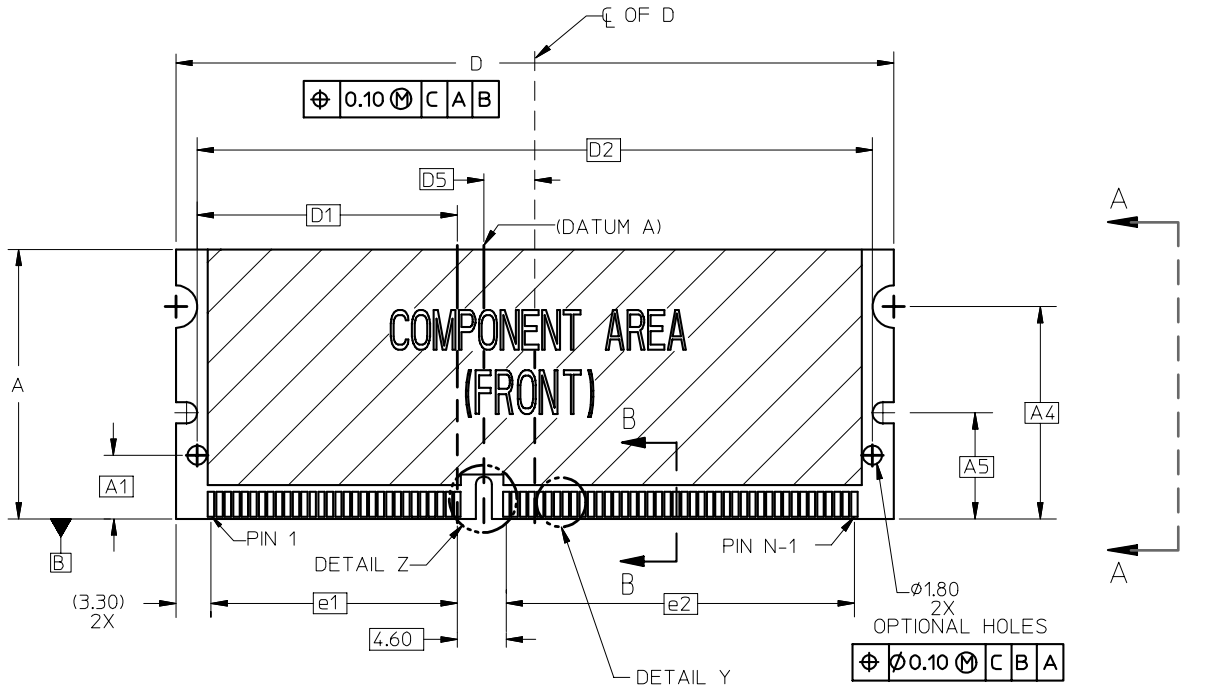
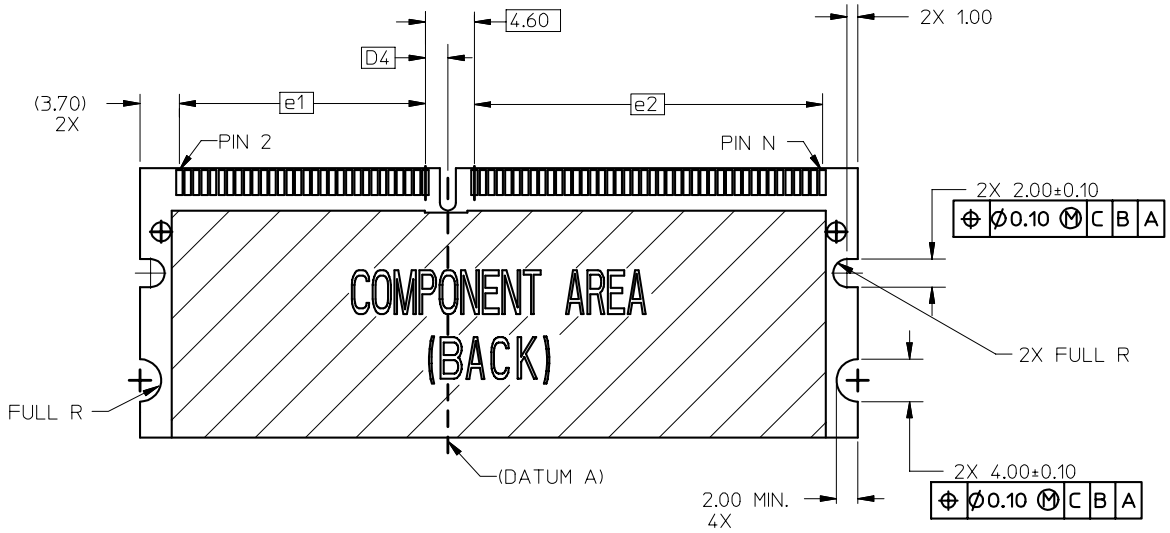
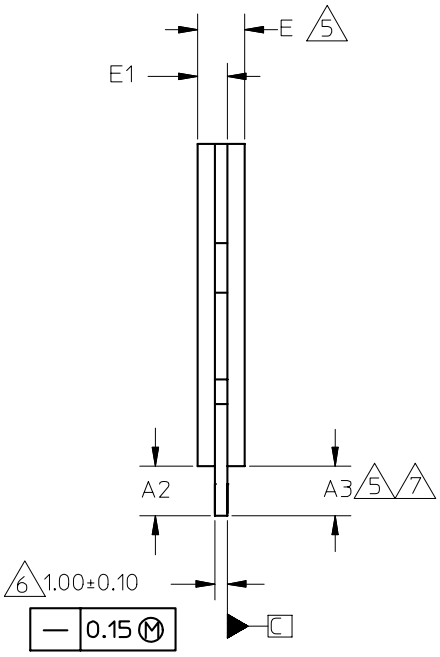




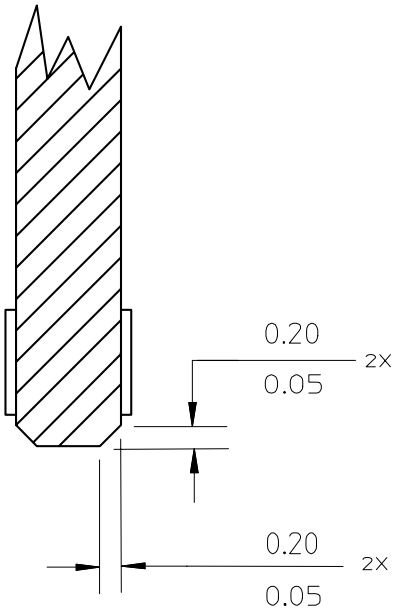
IT HAS BEEN STATED THAT U.S. PATENT NO. 5,227,664 (HELD BY HITACHI) MAY RELATE TO CERTAIN IMPLEMENTATIONS OF THIS PACKAGE OUTLINE.

JEDEC SOLID STATE PRODUCT OUTLINE	THIS *REGISTERED OUTLINE* HAS BEEN PREPARED BY THE JEDEC JC-11 COMMITTEE AND REFLECTS A PRODUCT WITH ANTICIPATED USAGE IN THE ELECTRONICS INDUSTRY; CHANGES ARE LIKELY TO OCCUR.

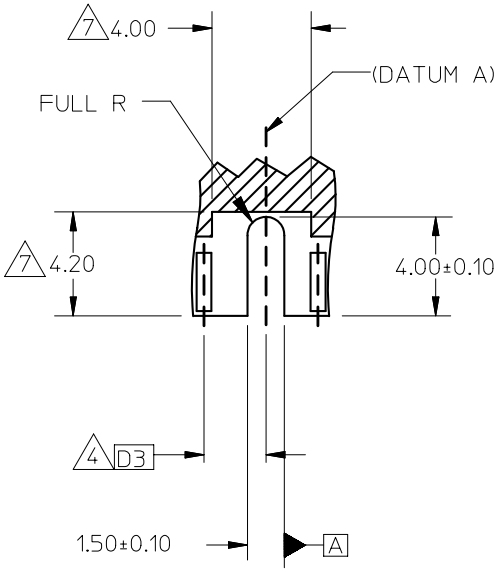
TITLE	PACKAGE DESIGNATOR	ISSUE	DATE		SHEET
DDR1/DDR2 16b/32b SMALL OUTLINE DUAL INLINE MEMORY MODULE (SO-DIMM) FAMILY, 0.8 LEAD CENTERS		A	JUL 06	MO-274	1 OF 8



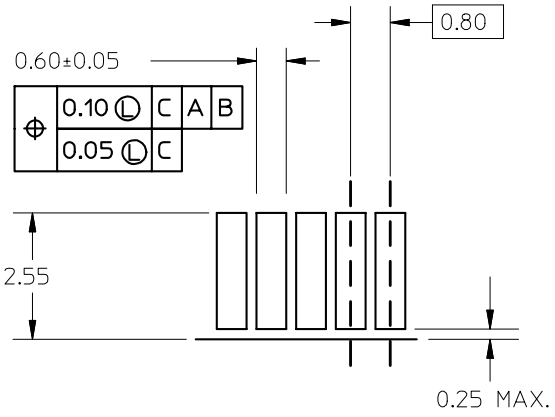
VIEW A-A



8 VIEW B-B
(OPTIONAL)



DETAIL Z



DETAIL Y

JEDEC SOLID STATE PRODUCT OUTLINE	TITLE	DDR1/DDR2 16b/32b SMALL OUTLINE DUAL INLINE MEMORY MODULE (SO-DIMM) FAMILY, 0.8 LEAD CENTERS	ISSUE	DATE		SHEET
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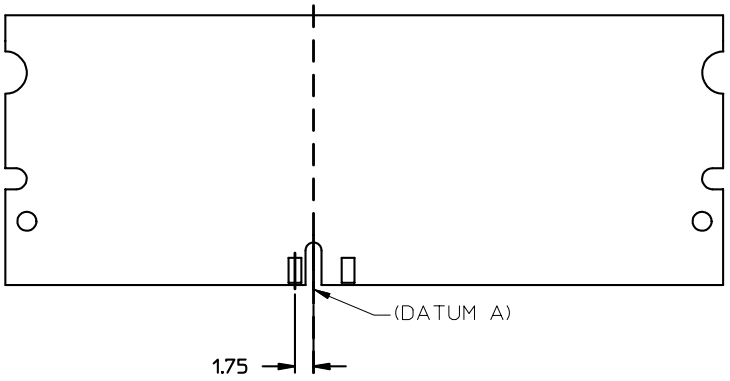
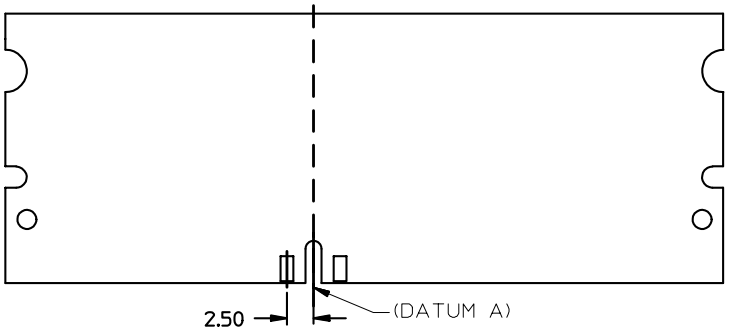
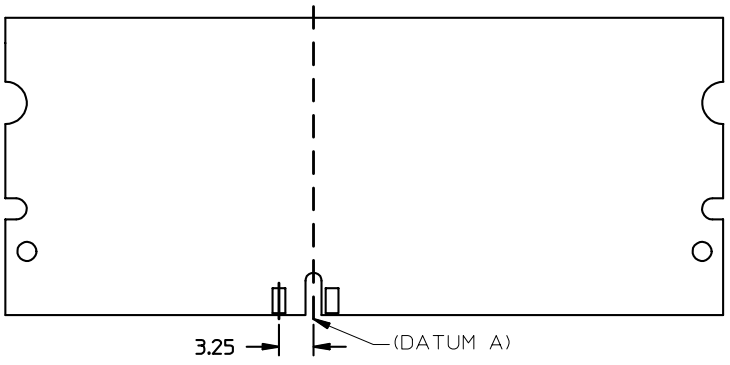
DRAM VARIATIONS

	AB			NOTE
SYMBOL	MIN	NOM	MAX	
A	29.85	30.00	30.15	
A1		6.00 BSC		
A2	4.00			
A3	4.00			5 , 7
A4		20.00 BSC		
A5		10.00 BSC		
D	67.45	67.60	67.75	
D1		15.70 BSC		
D2		63.60 BSC		
D3		2.50 BSC		4
D4		2.10 BSC		
D5		13.60 BSC		
E			3.80	
E1			2.45	5
e1		14.40 BSC		
e2		41.60 BSC		
N		144		
ISSUE		X		
REF				
NOTES		1,2,3		

DRAM VARIATIONS

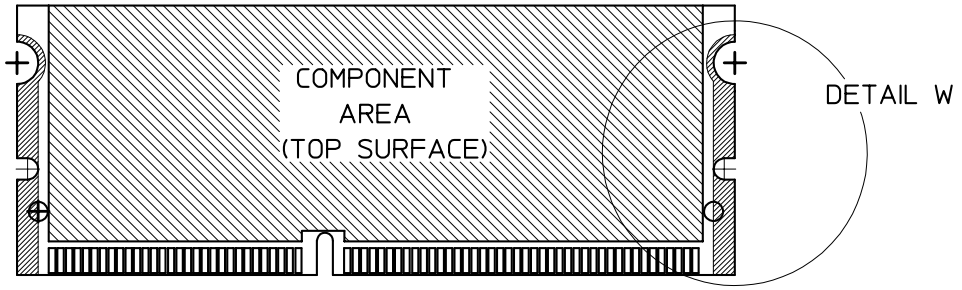
	BA			NOTE
SYMBOL	MIN	NOM	MAX	
A	31.60	31.75	31.90	
A1		6.00 BSC		
A2	4.00			
A3	4.00			5 , 7
A4		20.00 BSC		
A5		10.00 BSC		
D	67.45	67.60	67.75	
D1		15.70 BSC		
D2		63.60 BSC		
D3		1.75 BSC		4
D4		1.35 BSC		
D5		14.35 BSC		
E			3.80	
E1			2.45	5
e1		14.40 BSC		
e2		41.60 BSC		
N		144		
ISSUE		X		
REF				
NOTES		1,2,3		

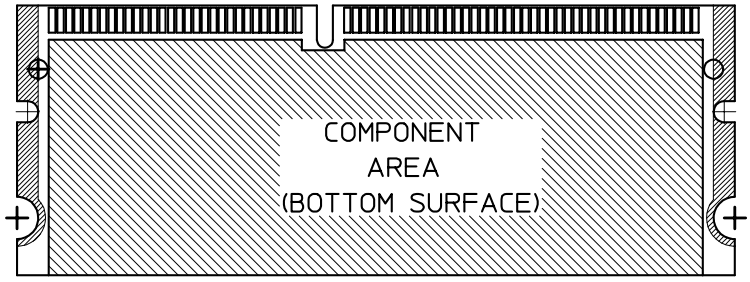
MECHANICAL KEYING
(FRONT VIEWS)

POWER SUPPLY ⚠4	
2.5 V (DDR1)	
1.8 V (DDR2)	
X.X V (TBD)	

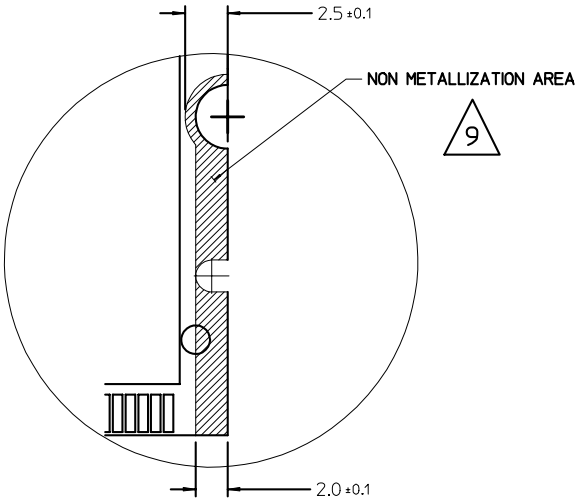
JEDEC SOLID STATE PRODUCT OUTLINE	TITLE	DDR1/DDR2 16b/32b SMALL OUTLINE DUAL INLINE MEMORY MODULE (SO-DIMM) FAMILY, 0.8 LEAD CENTERS	ISSUE	DATE		SHEET
			A	JUL 06	MO-274	4 OF 8

NON-METALLIZATION DEFINITION OUTER LAYERS



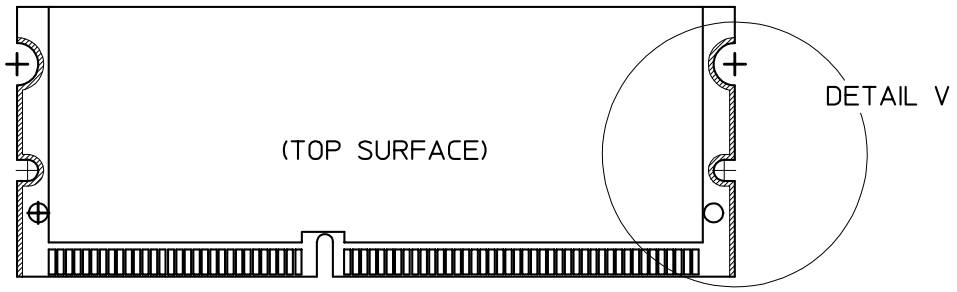


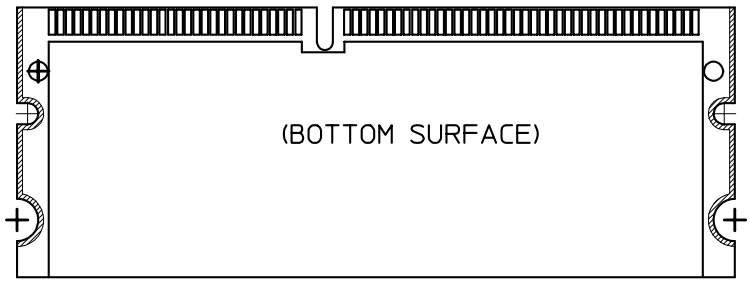
DETAIL W
(4 PLACES)

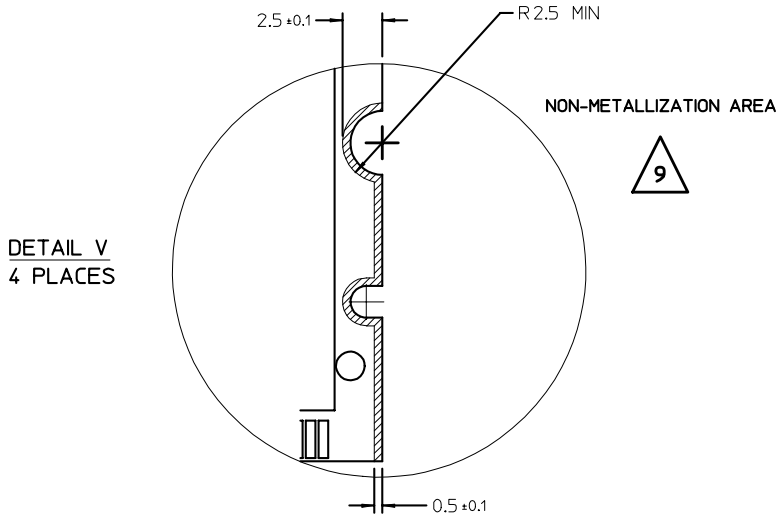


JEDEC SOLID STATE PRODUCT OUTLINE	TITLE DDR1/DDR2 16b/32b SMALL OUTLINE DUAL INLINE MEMORY MODULE (SO-DIMM) FAMILY, 0.8 LEAD CENTERS	ISSUE A	DATE JUL 06	MO-274	SHEET 5 OF 8

NON-METALLIZATION DEFINITION INNER LAYERS







JEDEC SOLID STATE PRODUCT OUTLINE	TITLE	DDR1/DDR2 16b/32b SMALL OUTLINE DUAL INLINE MEMORY MODULE (SO-DIMM) FAMILY, 0.8 LEAD CENTERS	ISSUE A	DATE JUL 06	MO-274	SHEET 6 OF 8

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.

2. TOLERANCES ON ALL DIMENSIONS ±0.15 UNLESS OTHERWISE SPECIFIED.

3. ALL DIMENSIONS ARE mm.

4. VARYING THE POSITION OF THE NOTCH IDENTIFIES THE OPERATIONAL VOLTAGE:
   2.5 VOLT (xA). 1.8 VOLT (xB). X.X VOLT (xC).
   THE JC-42.3 COMMITTEE CONTROLS THE INFORMATION IN THIS COLUMN.
   IT IS SHOWN HERE FOR REFERENCE ONLY, AND IS SUBJECT TO CHANGE.

5. DIMENSIONS APPLICABLE WHEN COMPONENTS MOUNTED ON BOTH SIDES. PCB THICKNESS NOT TO BE EXCEEDED OUT SIDE COMPONENT AREA.

6. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.

7. BORDER OF COMPONENT AREA.

8. THE ADDITION OF THIS BEVEL IS A FABRICATION OPTION AND IS NOT REQUIRED.
   THE BEVEL AIDS THE INSERTION OF THE MODULE INTO THE CONNECTOR.
   THE BEVEL IS NOT TO HIT THE GOLD CONTACTS.

9. METALLIZATION IS DEFINED AS ANY METAL SURFACE THAT HAS A RETURN PATH TO POWER SUPPLY OR GROUND, THROUGH A COMPONENT OR CONDUCTIVE PLANE VCC OR VDD, BLIND OR PLATED THROUGH HOLE (PTH), AS WELL AS NARROW OR WIDE TRACES, ANY SURFACE METALS SUCH AS CONNECTOR PIN IDENTIFICATION, PCB VENDOR CODE, ETC. THAT DO NOT HAVE A METALS AS A RETURN PATH ARE ACCEPTABLE.
   NON-METALLIZATION IS DEFINED AS THE OPPOSITE TO METALLIZATION AND DOES NOT INCLUDE ANY METAL OR CONDUCTIVE ELEMENTS THAT MAY CAUSE ELECTRICAL SHORT CIRCUIT.
   HOWEVER, ANY SURFACE METALS SUCH AS CONNECTOR PIN IDENTIFICATION, PCB VENDOR NAME OR CODE, ETC. THAT DOES NOT HAVE CONDUCTIVE RETURN PATH TO VCC OR VDD IS ACCEPTABLE.

10. LEADING EDGE OF CONTACT PADS SPECIFIED BY THE KEEPOUT ZONE SHALL BE FREE OF BURRS AND EXTERNAL TIE BARS.
    FOR OPTIMUM PERFORMANCE, THE TIE BAR IS TO BE ON AN INNER LAYER SO THAT THE REMNANT CANNOT CAUSE CONTACT DAMAGE.

11. APPLICATION NOTE:
    RECOMMENDED PLATING FOR CONTACT PADS ARE ;
    11.1 PREFERABLE PLATING : ELECTROLYTIC GOLD PLATING 0.76 MICROMETERS MINIMUM OVER ELECTROLYTIC NI 2.00 MICROMETERS MINIMUM.
    11.2 ALTERNATIVE PLATING: GOLD PLATING 0.05-0.75 MICROMETERS OVER NI 2.00 MICROMETERS MINIMUM MUST USE AN ELECTRONIC CONTACT GRADE CORROSIVE BARRIER LUBRICANT.

Change Record

If the changes involves any words added or deleted (excluding deletion of accidentally repeated words),
the change is included. Punctuation changes may or may not be included.

Initial Issue: A	Date: JULY 2006	Item: 11.14-084

Revision History:

Issue:	Date:	Item:

Location	Change from:	Change to:

Issue:	Date:	Item:

Location	Change from:	Change to:

Issue:	Date:	Item:

Location	Change from:	Change to: