User's Manual

DPIO2

Digital Parallel Input Output

PMC module

Rev 1.6

VMETRO

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Old Rev.	Change log	New Rev	Date/Sign
-	Initial version	1.0	06.12.01 / LAH
1.0	Updated for PCB-B, RS422 interface and PECL interface	1.1	02.07.02 / THO
1.1	Corrections done on PECL interface description	1.2	03.07.02 / THO
1.2	Corrections done: a) Small changes done several places b) Jumper descriptions corrected c) Updated MTBF numbers d) Corrections done on setup and hold times. e) Updated part no. for strobe driver on RS422 output PM in acc. To the changed 422 driver used. f) Updated termination resistance for FPDP	1.3	23.10.02 / THO
1.3	New appendix included. Description of how to verify signal quality and timing on front end connector.	1.4	10.03.03/THO
1.4	Changes in table 3 for JP11. Explanation of STROBE termination included. Correction done on data packing description.	1.5	17.11.03/THO
1.5	Default jumpersetting for JP2 and JP3 on DPIO2-EO-PM (PECL personality module) changed from MIDDLE to LEFT. Description of JP11 (table 3) corrected.	1.6	14.05.04/THO

TABLE OF CONTENTS

1 INTRODUCTION

1.1 How To Use This Manual

1.1.1 Purpose

This manual guides the reader through the process of unpacking, setting up and installing the board.

1.1.2 Overview

This manual contains the following chapters:

1. Introduction
2. Product Overview
3. Installation
4. Operation
5. Technical Reference

APPENDIXES

The following information is available in the appendixes:

Appendix A: FPDP Front End
Appendix B: LVDS Front End
Appendix C: RS422 Input Front End
Appendix D: RS422 Output Front End
Appendix E: PECL Input Front End
Appendix F: PECL Output Front End

1.1.3 Conventions used in this manual

The following section describes conventions used in this document.

Symbols	*Meaning*
	The STOP symbol indicates a section of critical importance. Overlooking this information may cause damage to the DPIO2 and/or other equipment.
	Indicates important, but not crucial, information. Still, you should take notice if you want to use all capabilities built into your DPIO2.

1.2 Precautions

Note: Inverted pin assignment is used on the front-end connector. Connections to other equipment should only be done with a correct type of cable (inverted or non-inverted) to insure connection of correct signals. See chapter 5.4 for more information.

Note: It is recommended to use twisted pair cable on DPIO2-LBU, DPIO2-DIU/DOU and on DPIO2-EIU/EOU models due to the balanced input/output signals.
Flat cable is recommended on DPIO2-FBU due to its non-balanced input/output signals.

Note: Before unpacking and installing the DPIO2, read the chapter 3 Installation.

1.3 Related Documents

To get a full understanding on how the DPIO2 works, the following literature should be obtained:

[1] VITA Tel: 1-602-951-8866 http://www.vita.com/	**Front Panel Data Port Protocol and Mechanical Specifications (VITA 17-1998), February 11, 1999.**
[2] PCI Special Interest Group Tel: 1-503-797-4207 http://www.pcisig.com/	**PCI Local Bus Specification Revision 2.1**
[3] IEEE Fax 1-732-981-9334 http://www.ieee.com/	**Draft Standard for a Common Mezzanine Card Family: CMC**
[4] IEEE Fax 1-732-981-9334 http://www.ieee.com/	**Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC**
[5] Dep. of Defense, USA	**MIL-HDBK 217F , Notice 2, Reliability Prediction of Electronic Equipment**

1.4 Technical Support

We provide technical documentation with all of our products. This documentation describes the technology and its performance characteristics.

Although, we have attempted to make this document comprehensive, there may be specific problems or issues this document does not satisfactorily cover. If you have any questions, you can phone us, or send us an email. Our goal is to offer a combination of products and services that provide complete, easy-to-use solutions for your application.

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2 PRODUCT OVERVIEW

2.1 DPIO2 Overview

The DPIO2 is a PCI Mezzanine Card (PMC) designed for high-speed data acquisition and generation. It combines a Digital Parallel Input or Output on one end, a 64-bit PCI bus master/slave interface with a DMA controller on the other end, with a large FIFO in between.

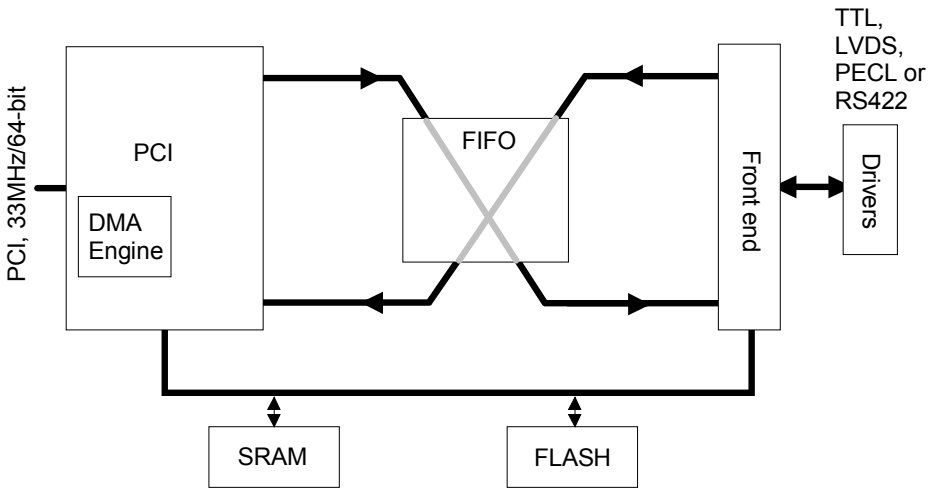

Figure 1: DPIO2 – Functional Block Diagram

In one end a PCI Interface chip provides 64-bit PCI bus master/slave interface with a linked list DMA engine.

In the other end the parallel interface is available through the front panel connector. The logical interface is based on the FPDP standard. The electrical interface can be TTL (FPDP compliant), RS422, PECL or LVDS, depending on what version of the DPIO2 is used.

The DPIO2 can be delivered with two FIFO sizes, either 32K or 128K.

To operate the DPIO2, registers both in the PCI interface chip and on local bus must be accessed.

Different packing options are available. That means that the front panel port can be 32-bit, 16-bit or 10-bit. When less than 32 bit is used, data is packed into 32-bit words before entering the FIFO. A similar unpacking scheme is used in output operation.

When using the DMA engine, both single and linked-list DMA is supported. For linked-list DMA, 64K of descriptors can be set up in the 1MB onboard SRAM.

2.2 DPIO2 features

- 64-bit 33MHz PCI bus
- Advanced linked list DMA
- Abort current transfer and jump to next descriptor
- All byte swap operations
- 32K or 128K deep FIFO
- TTL, LVDS, RS422 or PECL electrical interface in front-end
- Bi-directionality (FPDP and LVDS models only)
- Sample skip and store counters
- Packing options to utilize PCI bandwidth
- Internal or external clock
- FPGA image stored in FLASH is upgradeable

2.3 New Features and Changes Compared to the 1st. Generation DPIO

The main differences between the previous DPIO and the new DPIO2 are the following:

- Inverted front-end connector pinout is used on DPIO2 - **Note: Affects cabling!** (DPIO was using non-inverted front end connector pinout)
- Bi-directionality, can be used as both input and out module (FPDP and LVDS models only).
- Programmable output frequency when generating clock
- Deeper FIFO **(**32k or 128k deep, 32 bits wide)
- Handles higher transfer speed
  (64bit PCI interface and the FPDP II capable up to 400MByte/s)
- Both input and output modules can generate clock or use external clock (software controllable)
- LED indicators for SYNC, SUSPEND, STROB, NRDY and DVALID

2.4 Upgrading of FPGA Firmware

The FLASH, containing the FPGA firmware, may be upgraded by the customer using utility functions distributed with the DPIO2 software drivers.

3 INSTALLATION

The DPIO2 is sensitive to static electricity and can be damaged by static discharge. Always wear a grounded anti-static wrist strap and use grounded, static protected work surfaces when touching the circuit boards and their components.

When the DPIO2 is not mounted in a PMC slot, always keep it in its static protective envelope.

Warning: Do not mount the board in a powered up system!

3.1 Mounting the DPIO2

Note: Forced cooling is mandatory for the DPIO2.

1. Place the DPIO2 and the PMC carrier on a smooth, static protected work surface.
2. Remove the four screws on the bottom side of the DPIO2 located on the PMC front panel and on the 2 PMC spacers. (See drawing.)
3. Mount the DPIO2 on the PMC carrier.
4. Secure the DPIO2 with the four screws from the backside of the PMC carrier.

5. The cable can now be inserted. Make sure that all four screws are fastened tightly. If not, the insertion force when inserting the front panel connector will be directed to the PMC connectors. This can damage the connectors both on the DPIO2 and on the PMC carrier.

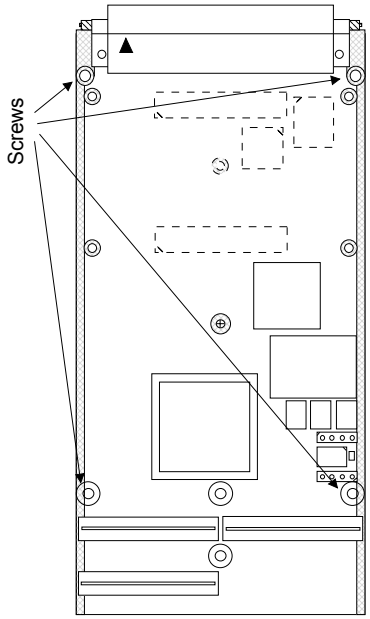

Figure 2: Screws for mounting the DPIO2 on the PMC

3.2 Software Installation

For complete, detailed instructions for installing and using DPIO2 software available from VMETRO, please refer to the appropriate software installation manual.

4 OPERATION

4.1 Structure of the board

There are six main components on the DPIO2 board.
These components are: (see Figure 1)

1. PCI Interface Chip
2. FIFO
3. Front-end Interface Chip
4. Front-end Drivers
5. SRAM
6. FLASH

4.2 PCI Interface Chip

The PCI interface chip makes the board compatible with PCI specification, revision 2.1.

The PCI interface is based on a Xilinx chip with integrated PCI core. The chip supports both 5V and 3.3V signaling on PCI.

PCI Device ID for DPIO2 is DD11h, and VMETRO's vendor ID is 129Ah.

4.2.1 DMA Controller

The DMA controller is located in the PCI interface chip. It can be set up to operate in DMA chain mode with up to 64k descriptor elements. The transfer size of each descriptor element can be varied from 16 bytes to its maximum of (16M-4) bytes.

4.3 FIFO

DPIO2 is populated with either a 32K FIFO or a 128K FIFO. The FIFO is controlled by the PCI interface chip and provides the buffering to operate with maximum throughput.

The same FIFO is used for both input and output directions.

4.4 Front-end Chip and Front-end Drivers

The front-end chip includes logic to communicate with other devices over the front panel. Packing and byte swap is implemented in this chip. The front-end chip is a Xilinx device, which is loaded at power-up from a FLASH. This FLASH can be updated by software.

The front-end drivers provide one of the following electrical interfaces:

- TTL
- LVDS
- RS422
- PECL

For all interfaces, the signaling protocol is in accordance to the FPDP specification.

4.5 SRAM

The 8Mbit SRAM is used to store linked list DMA information.

16 bytes are used for each DMA descriptor. With 1MByte SRAM this yields 64K descriptors.

4.6 FLASH

The 8Mbit FLASH is used to store FPGA images (for front-end chip and PCI interface chip). The FLASH can be overwritten so that new FPGA images can be loaded.

4.7 Data Packing

The default FPGA image supports 10, 16 and 32 bits packing. Contact factory for other packing requirements.

4.8 Personality Modules

Personality modules are used to accommodate different I/O interfaces. The control and data signals from the I/O connector are routed through a personality module to the front-end chip. In this way the interface can be user configurable.

These signals can be directly controlled by the front-end chip by having a one-to-one connection on the signals.

The DPIO2 interfaces are based on FPDP (Front Panel Data Port). The FPDP is a *de facto* standard for a 32-bit parallel port using TTL signaling. FPDP spec can be obtained from VITA (see chapter 1).

The DPIO2 family includes the TTL version (standard FPDP), the LVDS version, the PECL version and the RS422 version.

4.8.1 Removal and Installation of Personality Modules

It may be necessary to remove and reinstall the personality modules (PM) to change the setting of the jumpers located on the side facing against the DPIO2 board. To remove and reinstall the personality module, follow this procedure:

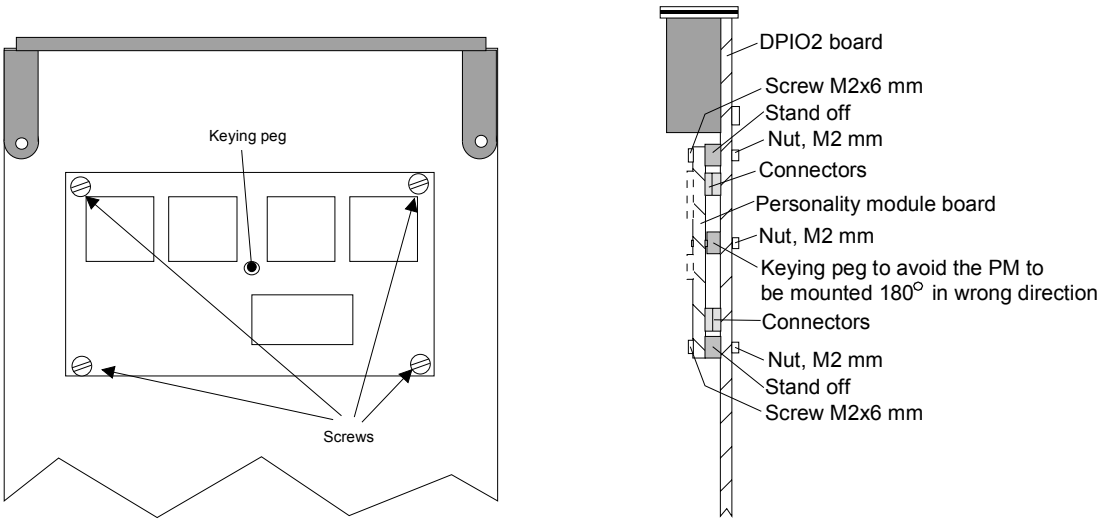

Figure 3: The personality module mounted on the DPIO2 board

1. Loosen the screws in the corners of the PM. It may be necessary to hold the nut on the opposite side with a spanner.

Do <u>NOT</u> loosen the nut for the keying peg!

2. Remove the screws, standoffs and nuts.
3. <u>Carefully</u> loosen the PM board from the DPIO2 board.
4. Make the necessary jumper setting changes.
5. <u>Carefully</u> mount the PM board on the DPIO2 board.

6. Insert the standoffs between the two boards, insert the screws and screw the boards together again. Make sure that the screws are inserted from the PM board side, not from the DPIO2 board side.

4.9 Jumpers

4.9.1 Jumper Overview

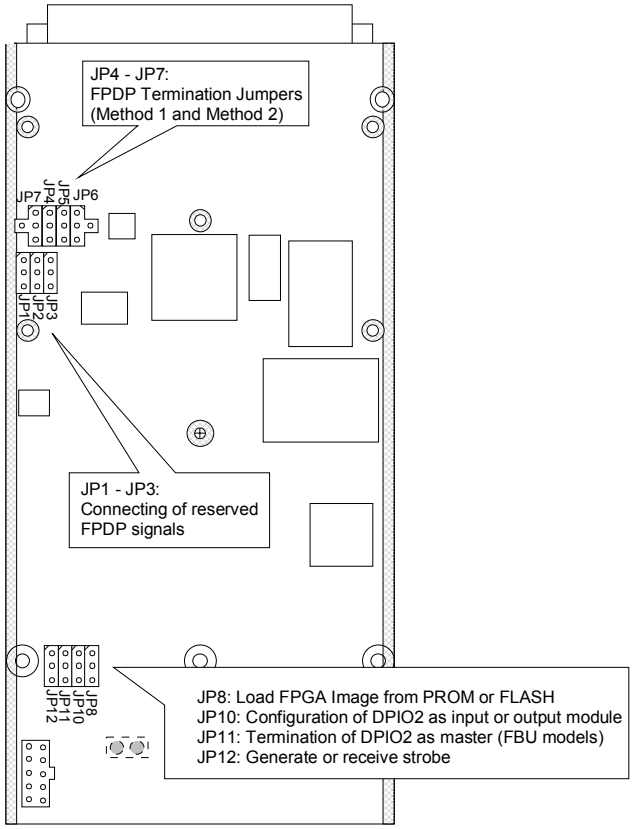

Figure 4: Jumper overview

4.9.2 Jumper Position Definitions

Jumper positions “UP”, “MIDDLE” and “DOWN” are referred to the board when it is held with the front panel connector up and the PMC connectors down, as shown in Figure 4. For the personality modules, jumper positions “Left”, “Right” and “Middle” position are referred to the board when it is held as shown in the figure for the actual board.

4.9.3 Default Jumper Setting

The factory settings of the jumpers are as described in the table below.

Jumper	Position -FBU	Position -DOU -EOU	Position other models	Description
JP1	Up	NA	NA	Reserved 3 signal disconnected from front-end connector.
JP2	Up	NA	NA	Reserved 2 signal disconnected from front-end connector.
JP3	Up	NA	NA	Reserved 1 signal disconnected from front-end connector.
JP4	Up	NA	NA	PECL driver on DPIO2 disconnected from PSTROB signal pin on front-end connector
JP5	Up	NA	NA	PECL driver on DPIO2 disconnected from PSTROB* signal pin on front-end connector
JP6	Down	NA	NA	FPDP: PSTROB* connected to 167Ω/250Ω termination network according to FPDP spec. Method 2.
JP7	Down	NA	NA	FPDP: PSTROB connected to 167Ω /250Ω ohm termination network according to FPDP spec. Method 2.
JP8	Down	Down	Down	Load Front-end Chip and PCI Interface Chip from FLASH
JP10	Up	Down	Up	Up: DPIO2 configured as input module Down: DPIO2 configured as output module
JP11	Up	NA	NA	DPIO2 terminated as “Master” (i. e. located at the end of the bus) (FBU models only).
JP12	Up	Down	Up	Up: DPIO2 configured to receive the strobe signal (PSTROBE/PSTROBE* or STROB) Down: DPIO2 configured to transmit the strobe signal (PSTROBE/PSTROBE* or STROB)

Table 1. Default jumper setting

4.9.4 Jumper Descriptions

4.9.4.1 Jumpers Common for all Models

Jumpers	Function
JP8	**FPGA Loading Options** Position UP: Load FPGA images for Front-end Chip and PCI Chip from the serial PROM. This setting should be used only for recovery after a failing FLASH update (e.g. due to power loss) Position DOWN: Load FPGA images for Front-end Chip and PCI Chip from FLASH. This setting should always be used during normal operation.
JP10	**Power-Up Operating Mode** This jumper is used to define if the DPIO2 after power-up is initialized for use in input mode or output mode. Application software can be used to switch mode. Position UP: DPIO2 is configured for input operation. Position DOWN: DPIO2 is configured for output operation.
JP12	**Power-Up STROBE Direction** This jumper is used to define if the DPIO2 after power-up is initialized to transmitt or receive the strobe signal (PSTROBE/PSTROBE* or STROB). Application software can be used to switch mode. Position UP: DPIO2 configured to receive the strobe signal Position DOWN: DPIO2 configured to transmit the strobe signal

Table 2. Jumpers – Common for all Models

4.9.4.2 DPIO2-FBU Jumpers

The following jumpers are found on the DPIO2-FBU models only. They are used to connect/disconnect FPDP signals to termination circuitry or FPGA I/O pins. The effect of these setting cannot be influenced by software.

Jumpers	Function
JP1	Position UP: FPDP reserved signal FP_RES3 disconnected from front-end FPGA Position DOWN: FPDP reserved signal FP_RES3 connected to front-end FPGA
JP2	Position UP: FPDP reserved signal FP_RES2 disconnected from front-end FPGA Position DOWN: FPDP reserved signal FP_RES2 connected to front-end FPGA
JP3	Position UP: FPDP reserved signal FP_RES1 disconnected from front-end FPGA Position DOWN: FPDP reserved signal FP_RES1 connected to front-end FPGA
JP4	Position UP or no jumper: PECL driver disconnected from PSTROBE signal pin on front-end connector Position DOWN: PECL driver connected to PSTROB signal pin on front-end connector
JP5	Position UP or no jumper: PECL driver disconnected from PSTROBE* signal pin on front-end connector Position DOWN: PECL driver connected to PSTROBE* signal pin on front-end connector
JP6	Position UP: PSTROB* terminated with 330 ohm to GND (driver termination, ref. [1], Method 1) Position MIDDLE: PSTROB* terminated with 110 ohm to PSTROB (receiver termination, Method 1) (provided JP7 in position MIDDLE) Position DOWN: PSTROB* terminated with 169 / 249 ohm pull up / pull down (driver and receiver termination, ref. [1], Method 2)
JP7	Position UP: PSTROB terminated with 330 ohm to GND (driver termination, ref. [1], Method 1) Position MIDDLE: PSTROB terminated with 110 ohm to PSTROB* (receiver termination, Method 1) (provided JP6 in position MIDDLE) Position DOWN: PSTROB terminated with 169 / 249 ohm pull up / pull down (driver and receiver termination, ref. [1], Method 2)
JP11	**Power-Up Signal Termination** This jumper is used to define the power-up state of the termination circuitry connected to the FPDP signals DIR*, NRDY*, SUSPEND* and STROBE. The positioning of this jumper has significance only for DPIO2-FBU. Position UP: DPIO2 is defined as FPDP transmitter/receiver master after power-up. The signals DIR*, NRDY* and SUSPEND* are terminated in accordance to this and in accordance to the operating mode of the DPIO2. STORBE is terminated if DPIO2 is set to receive STROBE. This setting is used when DPIO2 is used in point-to-point applications, and when it is located at the end of the cable in a multi-drop configuration. Position DOWN: The signals DIR*, NRDY*, SUSPEND* STROBE are not terminated. This setting is used in multi-dropped configurations where the DPIO2 is located between the transmitter master and the receiver master on the cable.

Table 3. DPIO2-FBU Jumpers

4.9.4.3 DPIO2-LBU Jumpers

Two jumpers, JP1 and JP2, are found on the DPIO2-LBU models only. They are located on the LVDS personality module. These are located on the side facing against the DPIO2 board, and are used to connect the reserved signal RES3 to the front-end.

Jumpers	Default position	Function	
JP1	Right	Right position:	Connects the reserved signal RES3 to the front-end connector (pin 2 (B1))
		Left position:	Connects pin 2 (B1) on the front-end connector to GND
JP2	Right	Right position:	Connects the reserved signal /RES3 to the front-end connector (pin 1 (A1))
		Left position:	Connects pin 1 (A1) on the front-end connector to GND

Table 4. Jumpers on LVDS Personality Module

To remove or insert these jumpers, the personality module has to be removed from the DPIO2 board. See chapter 4.8.1 on how to remove and reinstall the personality module.

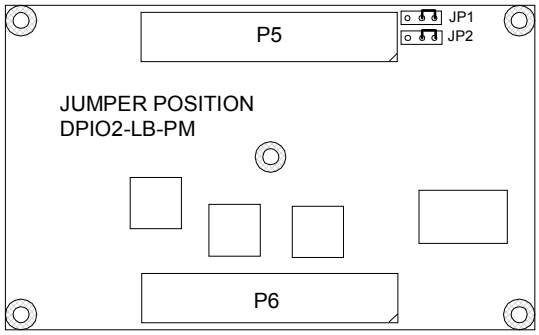

Figure 5: Jumpers on the LVDS Personality module

4.9.4.4 DPIO2-DIU and DPIO2-DOU Jumpers

There are three jumpers, JP1, JP2 and JP3, on the DPIO2-DIU models. They are located on the RS422 personality module. These are located on the side facing against the DPIO2 board. One is used to connect the reserved signal RES3 to the front-end.

Jumpers	Default position	Function	
JP1	Right	Right position:	Connects the reserved signal RES3 to the front-end connector (pin 2 (B1))
		Left position:	Connects pin 2 (B1) on the front-end connector to GND
JP2	Right	Right position:	Connects the reserved signal /RES3 to the front-end connector (pin 1 (A1))
		Left position:	Connects pin 1 (A1) on the front-end connector to GND
JP3	Right	Right position:	Enables driving of NRDY*, SUSPEND*, PIO1 and PIO2
		Left position:	Disables driving of NRDY*, SUSPEND*, PIO1 and PIO2

Table 5. Jumpers on RS422 Personality Module

To remove or insert these jumpers, the personality module has to be removed from the DPIO2 board. See chapter 4.8.1 on how to remove and reinstall the personality module.

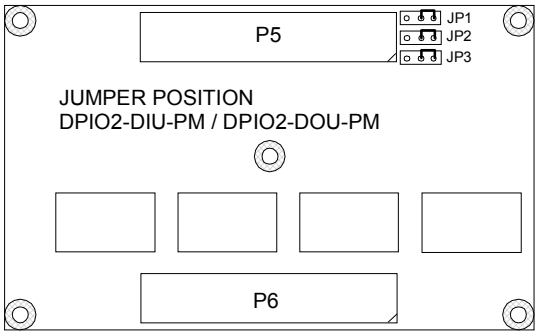

Figure 6: Jumpers on the RS422 Personality modules

4.9.4.5 DPIO2-EIU and DPIO2-EOU Jumpers

There are four jumpers, JP1, JP2, JP3 and JP5 on the DPIO2-EIU and DPIO2-EOU models. The jumpers are located on the personality modules, on the side facing against the DPIO2 board. The functionalities of the jumpers are described in the table below.

Jumpers	Default position	Function	
JP1	Removed	Inserted:	Connects pin 2 and 4 (B1 and D1) on front end connector to GND
		Removed:	Pin 2 and 4 (B1 and D1) on front end connector are disconnected from GND
JP2 / JP3	EIU:Right EOU:Left	Left position:	Connects the strobe generated on the board to the front end connector. Normally used for output modules, but may be used on input modules when input modules shall generate the strobe signal
		Right position:	Connects the strobe receiver circuits on the board to the front end connector. Normally used for input modules, but may be used on output modules when input modules shall generate the strobe signal.
		Middle position:	The same functionality as for the two leftmost positions except that the strobe signal is inverted.
JP5	EIU:Left EOU:Right	Left position:	For DPIO2-EIU only. The strobe signal into the module is connected via a PLL to reduce the hold time (the set up time is increased accordingly).
		Right position:	The strobe signal into the module is bypassed the PLL. This position must be used on output module when the strobe signal is generated at the input module.

Table 6. Jumpers on PECL Personality Module

To remove or insert these jumpers, the personality module has to be removed from the DPIO2 board. See chapter 4.8.1 on how to remove and reinstall the personality module.

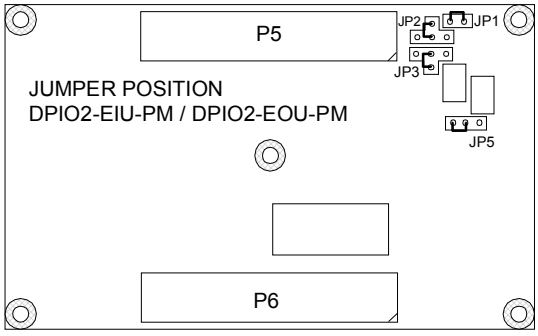

Figure 7: Jumpers on the DPIO2-EIU/EOU Personality module

4.10 Bussed Operation – Terminations

When more than two modules are connected together on the same cable special care needs to be taken regarding how these boards are connected together, and how the signals are terminated. Bussed operation is currently only valid for FPDP (TTL) version of DPIO2.

For correct termination, the modules must be set up with termination at the end of the signal. DPIO2 termination is configurable by hardware and software. Jumpers are used to control the power-up state, while software can override the power-up settings.

FPDP specification defines three categories of boards; Transmitter Master (TM), Receiver Master (RM), and Receiver (R). Point-to-point applications connect one Transmitter Master with one Receiver Master. In multi-drop configurations one or more Receiver boards may be connected to the cable between the TM and RM. Default the DPIO2 is set up as a Receiver Master. This means that the DPIO2 terminates the signals one (and only one) input module is supposed to terminate, according to the FPDP specifications. If the DPIO2 is set up as output (Transmitter Master), the termination will automatically change to terminate the signals an output module is supposed to terminate. It is also possible to set the DPIO2 up to not act as a master. The termination will then automatically be turned off. This must be done for modules connected between the Transmit Master and the Receiver Master.

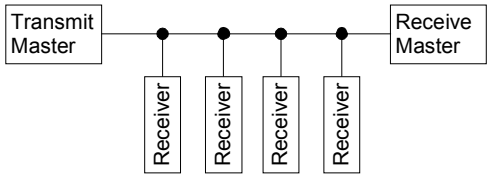

Figure 8: (Multi-drop) Bus application

It is recommended that the system is set up with only one Transmit Master and that this board is located at one end of the cable.

4.11 Flow Control

The DPIO2 supports the flow control defined in the FPDP specification. The Suspend signal is used whenever an input module wants the output to stop transferring data. The DPIO2 as input will assert Suspend when the FIFO almost full flag is going active to prevent FIFO overflow, and release it when the FIFO flag changes back. It is up to the data source to stop transferring data when assertion of Suspend is detected. In output mode the DPIO2 will within a few strobe periods temporarily stop sending data while the Suspend signal is detected active.

Both as input and output, the DPIO2 can turn the flow control functionality off. As input, it will then not assert the Suspend signal even if the FIFO is getting full. Data will in this case be lost. As output, it will continue to send data even if the Suspend signal is asserted.

In addition, on FPDP, there is a signal called NRDY* (not ready). It is used during initialization to indicate that the input module is not ready to receive data yet. On the DPIO2 the signal will be asserted, indicating that the module is not ready to receive data, until the start bit is set. The DPIO2 as output will not send any data before this bit is de-asserted.

4.12 Clocking Options

The DPIO2 has a variety of clocking options to support different clocking schemes in different systems. In a standard FPDP set-up, the output board always sources the strobe, but DPIO2 is designed to be able to source the strobe also as in input mode, and to receive an external strobe in output mode.

When generating strobe, the SW programmable oscillator can be set up with frequencies from 500kHz to 50MHz. This oscillator generally produces an output frequency within 0.1% of the desired output frequency. If the exact frequency required by the application cannot be achieved, it is possible to mount an oscillator carrier board (“OSCAR”) with the desired frequency.

On FPDP there are two versions of strobe signals in use, one TTL strobe and one differential PECL strobe. The DPIO2 is default set up as input, so the PECL signals are default not driven. The DPIO2 as input can choose (SW controllable) between using the TTL or the PECL version of the clock.

In addition the DPIO2 supports clocking on both edges of the strobe. When this functionality is used, a PLL doubles the frequency locally so that the frequency on the cable is half of the actual data frequency.

DPIO2 uses a PLL for frequencies above 10 MHz both on input and on output models. The PLL needs 0.5 ms settling time to synchronize its output. Therefore, for frequencies above 10 MHz 0.5 ms is needed from the time a new strobe frequency is selected until DPIO2 can start its operation.

4.12.1 Switching characteristics when strobe generated on input module

The tables below describe the switching characteristics when DPIO2 is sourcing the strobe in input mode, and when it is receiving an external strobe in output mode.

Input modules

In the calculation of the setup times below, it is neither taken into account the cable delay time for the data and clock nor the clock to output time for the transmitter. To get a correct set-up time, these parameters have to be added to the set-up time:

$$t_{su,\ complete} = t_{su,\ Table\ 7} + t_{co,\ transmitter,\ max} + t_{prop.del.\ cable,clk} + t_{prop.del\ cable,\ data}$$

DPIO2 Model	Set-up time t_{su} [ns] *	Hold time t_h [ns]
DPIO2-FBU TTL strobe	7.2	0
DPIO2-FBU PECL Strobe	4.2	0
DPIO2-LBU	8.8	0
DPIO2-DIU	29.3	0
DPIO2-EIU	9.7	0

** The setup time is not complete, see comment above.*

Table 7. Setup and hold times – DPIO2 Input generating strobe

Output modules

	When using PLL		When not using PLL	
DPIO2 Model	Min t_{co}	Max t_{co}	Min t_{co}	Max t_{co}
DPIO2-FBU TTL strobe	3.0	9.5	4.5	15.0
DPIO2-FBU PECL Strobe	3.5	10.2	5.0	15.8
DPIO2-LBU	3.7	11.3	5.2	16.8
DPIO2-DOU	17.5	32.8	19.0	39.4
DPIO2-EOU	4.0	11.7	5.5	17.3

Table 8. Clock-to-output times – DPIO2 Output receiving strobe

4.12.2 Double clocking

The switching characteristics described for each front end apply to double clocking also. The times then refer to both edges on the clock. However, when using double clocking, it is possible to skew data compared to clock.

The amount of skew is determined by frequency and control register settings. It is possible to adjust the skew with ±2, 4 and 6 time units (tu). This is set by control registers. One time unit is determined by the following formulas:

1/(32*freq*2), where freq is the frequency of strobe when it is between 10 and 25MHz

1/(16*freq*2), where freq is the frequency of strobe when it is between 25 and 50MHz

1/(8*freq*2), where freq is the frequency of strobe when it is above 50MHz

When using 2,4 or 6 time units, the required setup time is decreased and the required hold time is increased for input modules. For out modules clock to output increases.

Using –2, -4 or –6 time units, the required setup time is increased and the required hold time is decreased for input modules. For output modules clock to output decreases and can become negative.

This means that the skew can vary from ±1.25ns to ±7.5ns dependant on frequency. According to FPDP II draft revision 1.0, the hold times should be (when using double clocking) 1.5ns.

The DPIO2-FBU is default set up with 4tu or 2tu skew dependant on frequency by the SW driver. All other models is default set up with zero skew

4.13 Frame Synchronization

The FPDP specification defines several synchronization schemes. The DPIO2 supports all of them, and has support for some additional synchronization schemes as well. The synchronization is handled differently when set up as input or output.

4.13.1 Synchronization as input

DPIO2 supports multiple synchronization schemes as input. Which scheme to use is controlled by the application SW through driver calls.

No synchronization: The DPIO2 will ignore the SYNC* signal and accept data continuously.

Single frame data: Data will be ignored until SYNC* has been detected. From that point data will be accepted until acquisition is stopped.

Repeating frame data: For repeating framed data a synchronization signal is asserted together with the last data in a frame. When receiving such data DPIO2 can be set up to use SYNC* as an EOT (end of transfer) signal. This signal follows the data through the FIFO and is fed to the DMA controller as a synchronization signal. The DMA controller on DPIO2 can be set up to jump to next descriptor in the DMA chain whenever the EOT signal is pulsed.

This mode of operation can be used to support applications where the frame size changes dynamically, as well as applications with a fixed frame size. If there is no other synchronization mechanism between the DPIO2 and the data source, only a partial frame may be acquired by the first DMA descriptor. When using this functionality, a register can be read out, to determine how much data was transferred, before EOT was signaled.

DPIO2 can use SYNC*, PIO1, PIO2 or RES1 as an EOT signal.

SYNC* as D0: Routs SYNC* signal as data bit 0. This setting can be used independently with the other synchronization schemes.

4.13.2 Synchronization as output

DPIO2 supports multiple synchronization schemes as output. Which scheme to use is controlled by the application SW through driver calls.

No synchronization: SYNC* will not be asserted at all.

Single frame data: SYNC* will be asserted prior to first data in a transmit session. In this mode there is no link between the assertion of the SYNC* signal and the linked list DMA controller.

Repeating frame data: The DPIO2 will in this case assert SYNC* for each frame of data. This can be done in three different ways:

- **with first data:** DPIO2 asserts SYNC* together with the first data in the frame. The frame is defined as all data transferred by one DMA descriptor.
- **with last data:** DPIO2 asserts SYNC* together with the last data in the frame. The frame is defined as all data transferred by one DMA descriptor.
- **every n'th sample:** DPIO2 asserts SYNC* together with every *n*'th sample, where the frame size *n* is determined by a register in the DPIO2.

D0 as SYNC*: Routs data bit 0 as SYNC* signal.

4.14 Sending Data with DPIO2

To start data to be transmitted, the following must be done:

- Set up the DPIO2 in output mode
- Start the strobe generation, if necessary
- Set the start bit in the Front-end FPGA.
- Start loading data into the FIFO, either using the built-in DMA controller to read data from PCI memory, or using an external PCI device writing data into the FIFO.

4.15 Receiving data with DPIO2

To receive data, the following must be done:

- Set up the DPIO2 in input mode
- Set the start bit in the Front-end FPGA
- Start draining data from the FIFO using the built-in DMA controller.

5 TECHNICAL REFERENCE

5.1 Electrical Specifications

Power supply voltage:	5V	
Signal levels:	PCI compatible with both 5V and 3.3V signaling.	
Power consumption:		
DPIO2-FBU:	Idle mode:	2.2 W
	Active mode:	3.3 W
DPIO2-LBU:	Idle mode:	2.6 W
	Active mode:	4.3 W
DPIO2-DIU:	Idle mode:	2.6 W
	Active mode:	3.11 W
DPIO2-DOU:	Idle mode:	5.9 W
	Active mode:	6.2 W
DPIO2-EIU:	Idle mode:	3.8 W
	Active mode:	4.5 W
DPIO2-EOU:	Idle mode:	4.8 W
	Active mode:	5.3 W

5.2 Mechanical Specifications

Physical dimensions:	149 x 74 mm
Weight:	
DPIO2-FBU:	77 gram
DPIO2-LBU:	89 gram
DPIO2-DIU:	87 gram
DPIO2-DOU:	87 gram
DPIO2-EIU:	87 gram
DPIO2-EOU:	87 gram

5.3 Mean Time Between Failure (MTBF)

The MTBF values given in the following table are calculated estimations, which represents the inherent reliability of the DPIO2 based on the requirements of [5].

The MTBF values are calculated for different environments. The fact that an MTBF number is provided for a given environment does not mean that operation in this environment is supported. The different environmental definitions are:

GB: Ground, Benign. Equipment intended used in locations with controlled temperature and humidity.

GF: Ground, Fixed. Equipment intended used in locations with moderately controlled temperature and humidity.

NS: Naval, Sheltered. Equipment intended used in shelters or below deck conditions on surface ship and equipment installed in submarines.

AIC: Airborne, Inhabited. Equipment intended used in cargo compartments that can be occupied by an aircrew.

All MTBF values are calculated for an ambient temperature of 25 °C.

The calculations are done for PCB-C version of the main board. The personality modules were PCB-A versions, except from DPIO2-LB-PM, which was of PCB-B version.

DPIO2 model	GB	GF	NS	AIC
DPIO2-FBU/128K MTBF in hours	244090	100530	63473	51919
DPIO2-FBU/32K MTBF in hours	245131	100706	63543	51966
DPIO2-LBU/128K MTBF in hours	247127	108091	66684	56702
DPIO2-LBU/32K MTBF in hours	248195	108295	66762	56758
DPIO2-DIU/128K MTBF in hours	249721	109415	67916	57428
DPIO2-DIU/32K MTBF in hours	250810	109624	67996	57485
DPIO2-DOU/128K MTBF in hours	250445	109972	68562	58123
DPIO2-DOU/32K MTBF in hours	251541	110183	68644	58182
DPIO2-EIU/128K MTBF in hours	257658	115879	72552	60750
DPIO2-EIU/32K MTBF in hours	258818	116113	72643	60814
DPIO2-EOU/128K MTBF in hours	259941	116979	73327	61303
DPIO2-EOU/32K MTBF in hours	261122	117217	73421	61368

Table 9. MTBF Values

5.4 Cable and connectors

Note: Inverted pin assignment is used on the front-end connector. Connections to other equipment should only be done with a correct type of cable (inverted or non-inverted) to insure connection of correct signals.

Note: It is recommended to use twisted pair ribbon cable on DPIO2-LBU and DPIO2-DBU due to the balanced input/output signals.
Ribbon cable is recommended on DPIO2-FBU due to its non-balanced input/output signals

5.4.1 Cables for DPIO2

The following cables are available from VMETRO:

Part number	Description	To be used on
CBL-FPDP-x	Non-inverted 80 pins ribbon cable. The following cable lengths are possible: x=10: 10 cm cable length x=30: 30 cm cable length x=100: 100 cm cable length x=200: 200 cm cable length	DPIO2-FBU when used together with another module with inverted FPDP pin assignment
CBL-FPDP-xI	Inverted 80 pins ribbon cable. (pin 1 on the one connector is connected to pin 80 on the other connector, 2 to 79, etc.) The following cable lengths are possible: x=10: 10 cm cable length x=30: 30 cm cable length x=100: 100 cm cable length x=200: 200 cm cable length	DPIO2-FBU when used together with a module with non-inverted FPDP pin assignment, e. g. the first gen. DPIO.
CBL-TPF80-xM	Non-inverted 80 pins twisted pair cable. The following cable lengths are possible: x=2: 2 m cable length x=5: 5 m cable length x=10: 10 m cable length	DPIO2-LBU/DPIO2-DBU when used together with another module with the same pin assignment as DPIO2-LBU/DPIO2-DBU
CBL-TPF80-xMI	Inverted 80 pins twisted pair cable. (pin 1 on the one connector is connected to pin 80 on the other connector, 2 to 79, etc) The following cable lengths are possible: x=2: 2 m cable length x=5: 5 m cable length x=10: 10 m cable length	DPIO2-LBU/DPIO2-DBU when used together with another module with the opposite pin assignment as DPIO2-LBU/DPIO2-DBU, e. g. the first gen. DPIO-Lx/DPIO-Dx.
CBL-TPF5080-xI	Inverted 50/80 pins twisted pair cable. In one end a 50 pins connector is mounted, in the other end an 80 pins connector is mounted. The following cable lengths are available: x=30 30 cm cable length x=60 60 cm cable length x=90 90 cm cable length x=120 120 cm cable length	Connection of the old version DPIO-EO/EI to the new DPIO2-EOU/EIU.

Table 10. Cables for DPIO2

The DPIO2 uses a 80 pins connector and cabling. Note that inverted pin assignment is used on the connector. For connection to devices with non-inverted pin assignment, an inverted cable is needed. The figure below shows an inverted cable.

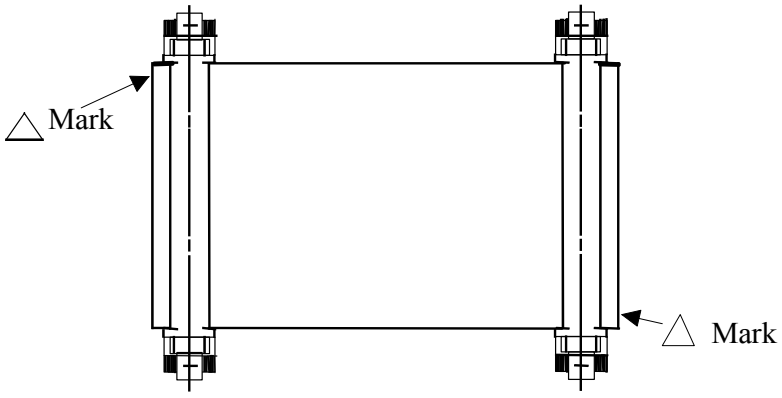

Figure 9: Inverted cable

For connection to devises with inverted pin assignment, a non-inverted cable is needed. The figure below shows a non-inverted cable.

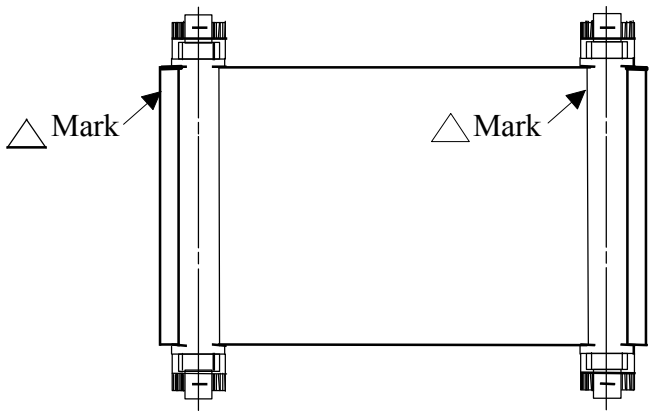

Figure 10: Non-inverted cable

The figure below shows how to count signals on the Front-end connector.

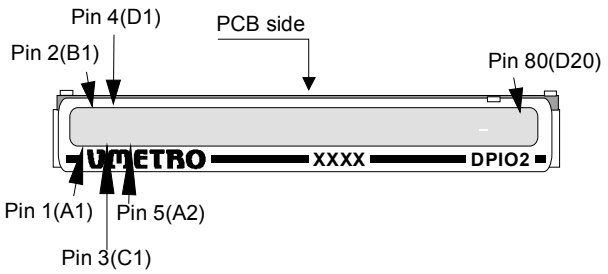

Figure 11: DPIO2 Front Panel

5.4.2 Detailed connector and cable information

The table below shows some suitable connectors for connection of devices to the DPIO2:

Number of pins	To be used on	Manufacturer	Part number
80	Printed circuit boards	KEL	KEL 8831E-080-170L
80	Cables	KEL	KEL 8825E-080-175S

Table 11. Connectors

The figure below describes the PCB lay out for the front-end connector

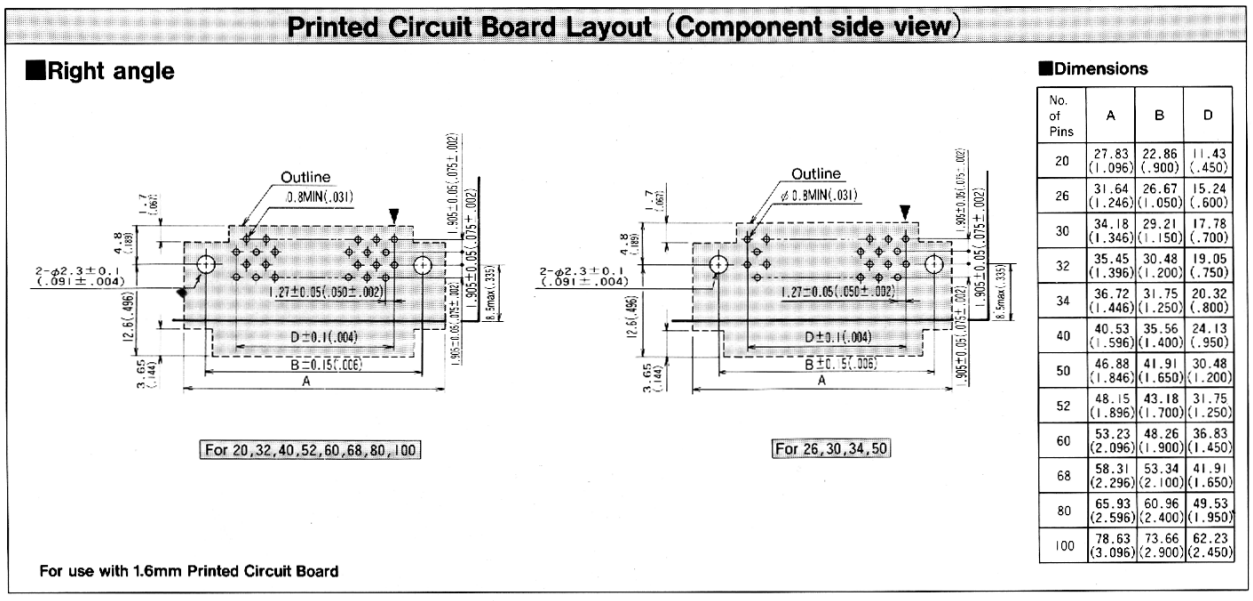

Figure 12: PCB layout of the front-end connector

APPENDIX A. DPIO2-FBU FPDP (TTL) FRONT-END

A.1 Supported Features

This chapter describes the TTL front-end interface for the fully FPDP compliant DPIO2-FBU. For further information regarding FPDP, contact VITA for the specification. Data width is maximum 32 bit, and can operate at speeds up to 40MHz. The module has support for handshake, has user-defined signals, and has data valid bit and synchronization capabilities.

The DPIO2 with FPDP interface will operate at up to 20MHz* at 32 bits with TTL strobe, up to 40MHz* at 32 bits with PECL strobes.

FPDP-II

FPDP-II is a suggested improvement to the current FPDP specification. The maximum frequency is increased to 50MHz and both edges of the strobe is used to clock data, the maximum data rate is increased from 160MB/s to 400MB/s. Either the TTL or the PECL strobes can be used at frequencies up to 50MHz. The DPIO2 has implemented the new FPDP-II suggestions.

Note that the sustained maximum data rate is limited by PCI bandwidth. The DPIO2 supports 64bit/33MHz PCI interface with a maximum through put of 266MB/s.

***Note**: The numbers given above regarding the frequency and transfer rate is only applicable when the data transmitter is generating strobe.

* Limited by FPDP spec.

A.2 Signal Description and Pin Assignments

Note:
Inverted pin assignment is used on the front end connector on DPIO2, while the non-inverted pin assignment was used on the previous generation DPIO.

Signal	Name	Signal Description
D(31:00)	Data Bus	32-bit data bus driven by transmitter.
DIR*	Data Direction	The data source asserts DIR* low. (Open collector)
DVALID*	Data Valid	When asserted, DVALID* indicates that the data bus has valid data. This signal is generated by the data source with each sample.
STROB	Data Strobe	STROB is a free running clock supplied by the Transmitter. Receiver boards should clock data at the rising edge of STROB when DVALID* is asserted.
NRDY*	Not Ready	NRDY* should be asserted by receiver boards, when they are not ready to receive data. Transmitter should not transmit data before NRDY* is negated. (Open collector)
PIO2, PIO1	Programmable I/O	The PIO signals are programmable I/O lines for user-defined functions. They may be configured as inputs or outputs.
PSTROBE	+PECL Data Strobe	This signal along with PSTROBE* are generated by the data source as an optional differential clock and has the same polarity as STROB. For high data rate applications, the differential PECL data strobe should be used instead of STROB.
PSTROBE*	-PECL Data Strobe	This is the negative version of the differential PECL data strobe.
RES1,RES2, RES3		Default not connected. See below on how these signals can be used.
SUSPEND*	Suspend Data	SUSPEND* should be generated by receiver boards to inform the data source of a pending buffer overflow condition. This function may be disabled with control register bit. (Open collector)

Table 12. Signal descriptions - DPIO2-FBU models

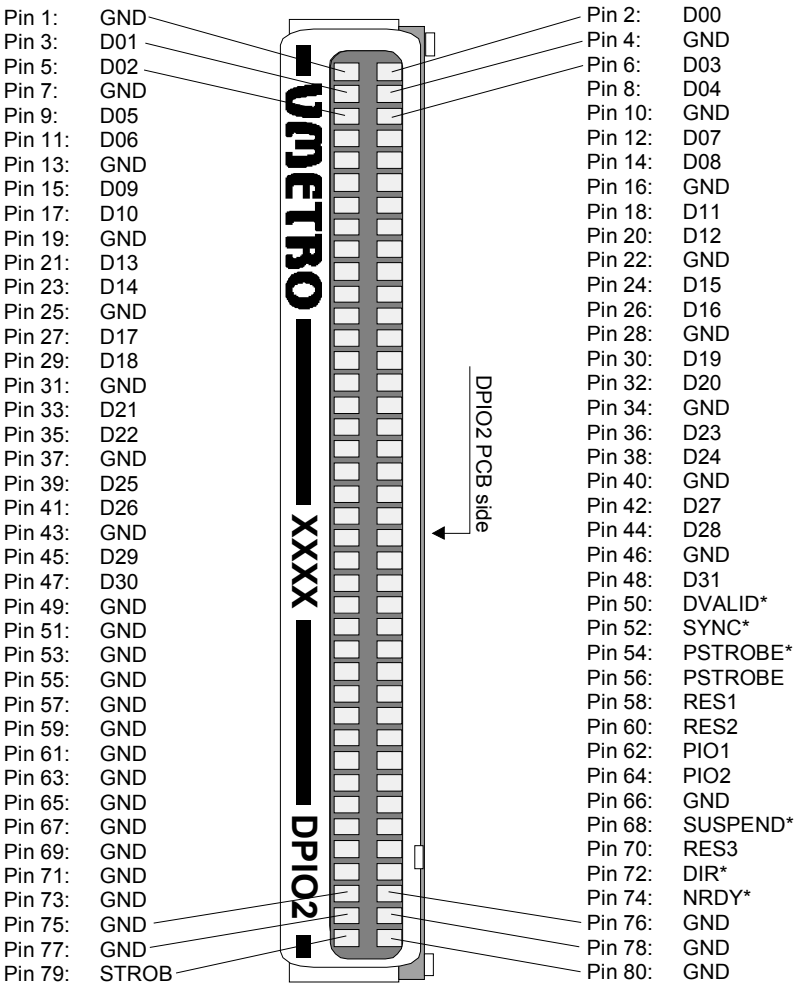

Table 13. Inverted connector pin assignment – DPIO2-FBU models

A.3 Jumpers on DPIO2-FBU Interface

See chapter 4.9.4.2.

A.4 Switching characteristics, DPIO2-FBU

Input Modules

The DPIO2 has different setup and hold times depending on how the DPIO2 is set up. To get the best setup and hold times needed when running at maximum speed, an internal PLL is needed to improve timing. This PLL cannot be used when the frequency of the strobe is below 10MHz. In addition FPDP has two strobes to choose between. The setup and hold times are different when using PECL strobes compared to using TTL strobes.

Parameter symbol	Parameter Description	TTL when using PLL	PECL when using PLL	TTL when not using PLL	PECL when not using PLL
t_{su}	Set-up time	0.9ns	0.4ns	– 0.6ns	– 1.1ns
t_h	Hold time	5.1ns	5.8ns	10.9ns	11.6ns

Table 14. Setup and hold times – DPIO2-FBU in input mode

Output Modules

The FPDP specification recommends to invert the strobe signal out on the cable. That way the data will switch around negative edge of the strobe, and give very good setup and hold times to the input module. In addition an internal PLL is used to improve timing. This PLL cannot be used when the frequency of the strobe is below 10MHz.

The times below are given in respect to the negative edge. To calculate what the times will be compared to the positive edge of the strobe, half a period needs to be added.

Parameter symbol	Parameter Description	Using TTL strobe	Using PECL strobe
Min t_{co}	**Negative** edge of clock to output	– 3.0ns	0ns
Typ t_{co}	**Negative** edge of clock to output	0 – 2	2 – 3
Max t_{co}	**Negative** edge of clock to output	2.7ns	3.7ns

Table 15. Clock to output time – DPIO2-FBU in output mode

A.5 Signal Termination

Signal	Termination	Comment
D[0] – D[31]	27 ohm series resistance	Also when DPIO2-FBU is in input mode.
DVAL*	27 ohm series resistance	Also when DPIO2-FBU is in input mode.
SYNC*	27 ohm series resistance	Also when DPIO2-FBU is in input mode.
STROB	SW controllable, two possibilities: a) 220 ohm to +5V and 330 ohm to GND b) No termination	
SUSPEND*	SW controllable, two possibilities: a) 220 ohm to +5V and 330 ohm to GND b) No termination	In a bussed application, the termination should only be used for master devices.
NRDY*	SW controllable, two possibilities: a) 220 ohm to +5V and 330 ohm to GND b) No termination	In a bussed application, the termination should only be used for master devices.
DIR*	SW controllable, two possibilities: a) 220 ohm to +5V and 330 ohm to GND b) No termination	In a bussed application, the termination should only be used for master devices.
PSTROB / PSTROB*	Method 1 or Method 2 according to FPDP specification	Default is Method 2. See Table 3 for details.
RES1	27 ohm series resistance	Connection of the signal via jumper JP3
RES2	27 ohm series resistance	Connection of the signal via jumper JP2
RES3	27 ohm series resistance	Connection of the signal via jumper JP1
PIO1	27 ohm series resistance	
PIO2	27 ohm series resistance	

Table 16. Signal termination on DPIO2-FBU models

A.6 Line drivers / receivers

Signal	Device Part no	Device manufacturer	Direction
D[0] – D[31]	PI74FCT16501ETA	Pericom	Transceiver
DVAL*	PI74FCT16501ETA	Pericom	Transceiver
SYNC*	PI74FCT16501ETA	Pericom	Transceiver
STROB	49FCT806ASO IDT74FCT3244APG	IDT IDT	Transmitter Receiver
SUSPEND*	N74F3038 IDT74FCT3244APG	Philips IDT	Transmitter Receiver
NRDY*	N74F3038 IDT74FCT3244APG	Philips IDT	Transmitter Receiver
DIR*	N74F3038 IDT74FCT3244APG	Philips IDT	Transmitter Receiver
PSTROB /PSTROB*	MC10ELT28D MC10ELT28D	Motorola Motorola	Transmitter Receiver
RES1	IDTQS3244Q	IDT	Receiver
RES2	IDTQS3244Q	IDT	Receiver
RES3	IDTQS3244Q	IDT	Receiver
PIO1	IDTQS3244Q	IDT	Receiver
PIO2	IDTQS3244Q	IDT	Receiver

Table 17. Line drivers and receivers on DPIO2-FBU models

APPENDIX B. DPIO2-LBU LVDS FRONT-END

B.1 Supported Features

This chapter describes the LVDS front-end interface of the DPIO2-LBU models. The interface is still based on the FPDP protocol, the electrical levels, however, are in accordance to the LVDS standard. Data width is maximum 32 bits, and can operate at speeds up to 50MHz. The model has support for handshake, has user defined signals, and has data valid bit and synchronisation capabilities.

Double clocking

The DPIO2 has a feature that allows using both edges of the strobe to clock data. In this way the data speed can be doubled and this gives a bandwidth of 400MB/s. The clock will still be running at 50MHz.

Note that the sustained maximum data rate is limited by PCI bandwidth. The DPIO2 supports 64bit/33MHz PCI interface with a maximum through put of 266MB/s.

Note: The numbers given above regarding the frequency and transfer rate is only applicable when the data transmitter is generating strobe.

B.2 Signal Description and Pin Assignments

Note: The front end connector pinout is inverted on DPIO2 compared to the first gen. DPIO-Lx.

Signal	Name	Signal Description
D(31:00) /D(31:00)	Data Bus	32-bit data bus driven by transmitter.
DVALID* /DVALID*	Data Valid	When asserted, DVALID* indicates that the data bus has valid data. This signal is generated by the data source with each sample.
STROB /STROB	Data Strobe	STROB is a free running clock. Receiver boards should clock data at the rising edge of STROB when DVALID* is asserted
NRDY* /NRDY*	Not Ready	NRDY* should be asserted by receiver boards, when they are not ready to receive data. Transmitter should not transmit data before NRDY* is negated.
PIO2, PIO1 /PIO2, /PIO1	Programmable I/O	The PIO signals are programmable I/O lines for user-defined functions. They may be configured as inputs or outputs.
RES3 /RES3	Reserved	Reserved signal.
SUSPEND* /SUSPEND*	Suspend Data	SUSPEND* should be generated by receiver boards to inform the data source of a pending buffer overflow condition. This function may be disabled with control register bit.
SYNC* /SYNC*	Sync. Pulse	The transmitter provides sync. pulses to receiver boards to synchronize data transfers. See separate section for details.

DVALID*, /DVALID*, SUSPEND*, /SUSPEND*, SYNC*, /SYNC*, NRDY* and /NRDY* are active low signals.

Table 18. Signal description – DPIO2-LBU models

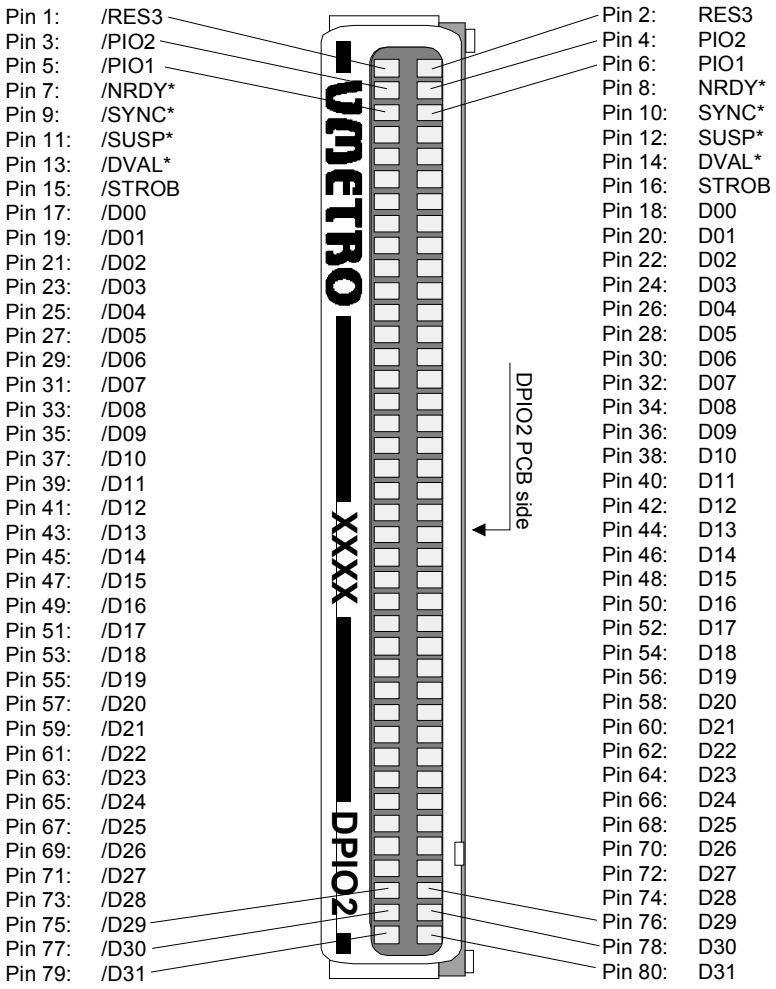

Table 19. Connector pinout – DPIO2-LBU models

B.3 Jumpers on DPIO2-LBU

See chapter 4.9.4.3.

B.4 Switching characteristics, DPIO2-LBU

Input Modules

The DPIO2 has different setup and hold times depending on how the DPIO2 is set up. To get the best setup and hold times needed when running at maximum speed, an internal PLL is used to improve timing. This PLL cannot be used when the frequency of the strobe is below 10MHz.

Parameter symbol	Parameter Description	Using PLL	Not using PLL
t_{su}	Set-up time	4.6ns	3.1ns
t_h	Hold time	1.9ns	7.7ns

Table 20. Setup and hold times – DPIO2-LBU in input mode

Output Modules

The DPIO2 inverts the strobe signal out on the cable. That way the data will switch around negative edge of the strobe, and give very good setup and hold times to the input module. In addition an internal PLL is used to improve timing. This PLL can not be used when the frequency of the strobe is below 10MHz.

The times below are given in respect to the negative edge. To calculate what the times will be compared to the positive edge of the strobe, half a period needs to be added.

Parameter symbol	Parameter Description	t_{co} [ns]
Min t_{co}	**Negative** edge of clock to output	– 0.2
Typ t_{co}	**Negative** edge of clock to output	4 – 5
Max t_{co}	**Negative** edge of clock to output	6.5

Table 21. Clock to output time – DPIO2-LBU in output mode

B.5 Signal termination

All signals have a 110-ohm resistor between the two signals in the LVDS signal pairs.

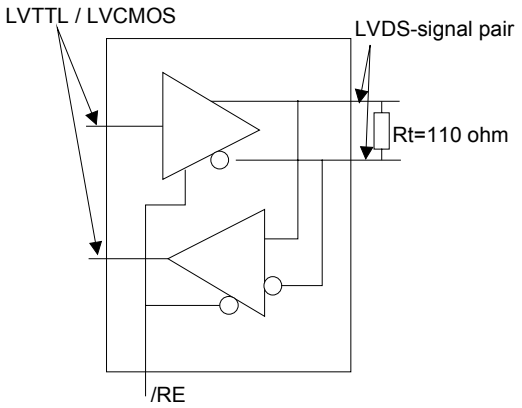

Figure 13 Termination of LVDS signal pair

A Bus LVDS transceiver is used on the LVDS interface, i. e. the driver output and receiver input are internally connected in the transceiver IC package. The driver output is designed for use of termination resistors in both ends for point-to-point applications.

B.6 Line drivers / receivers

Signal	Device Part no	Device manufacturer	Direction
D[0] – D[31] RES3 DVAL* SYNC*	DS92LV090ATVEH	National	Transceiver
STROB NRDY* SUSPEND* PIO1 PIO2	DS92LV040ATLQA	National	Transceiver

Table 22. Line drivers and receivers on DPIO2-LBU models

APPENDIX C. DPIO2-DIU RS422 INPUT FRONT-END

C.1 Supported Features

This chapter describes the RS422 input front-end interface of the DPIO2-DIU models. The interface is still based on the FPDP protocol, the electrical levels, however, are in accordance to the RS422 standard. Data width is maximum 32 bits, and can operate at speeds up to 20MHz. The model has support for handshake, has user defined signals, and has data valid bit and synchronisation capabilities.

Double clocking

The DPIO2 has a feature that allows using both edges of the strobe to clock data. In this way the data speed can be doubled and this gives a bandwidth of 160MB/s. The clock will still be running at 20MHz.

Note: The numbers given above regarding the frequency and transfer rate is only applicable when the data transmitter is generating strobe.

C.2 Signal Description and Pin Assignments

Note: The front end connector pinout is inverted on DPIO2 compared to the first gen. DPIO-Dx.

Signal	Name	Direction	Signal Description
D(31:00) /D(31:00)	Data Bus	I	32-bit data bus driven by transmitter.
DVALID* /DVALID*	Data Valid	I	When asserted, DVALID* indicates that the data bus has valid data. This signal is generated by the data source with each sample.
STROB /STROB	Data Strobe	I	STROB is a free running clock. Receiver boards should clock data at the rising edge of STROB when DVALID* is asserted
NRDY* /NRDY*	Not Ready	O	NRDY* should be asserted by receiver boards, when they are not ready to receive data. Transmitter should not transmit data before NRDY* is negated.
PIO2, PIO1 /PIO2, /PIO1	Program mable I/O	I/O	The PIO signals are programmable I/O lines for user-defined functions. They may be configured as inputs or outputs.
RES3 /RES3	Reserved	I	Reserved for user defined signal.
SUSPEND* /SUSPEND*	Suspend Data	O	SUSPEND* should be generated by receiver boards to inform the data source of a pending buffer overflow condition. This function may be disabled with control register bit.
SYNC* /SYNC*	Sync. Pulse	I	The transmitter provides sync. pulses to receiver boards to synchronize data transfers. See separate section for details.

DVALID*, /DVALID*, SUSPEND*, /SUSPEND*, SYNC*, /SYNC*, NRDY* and /NRDY* are active low signals.

Table 23. Signal description – DPIO2-DIU models

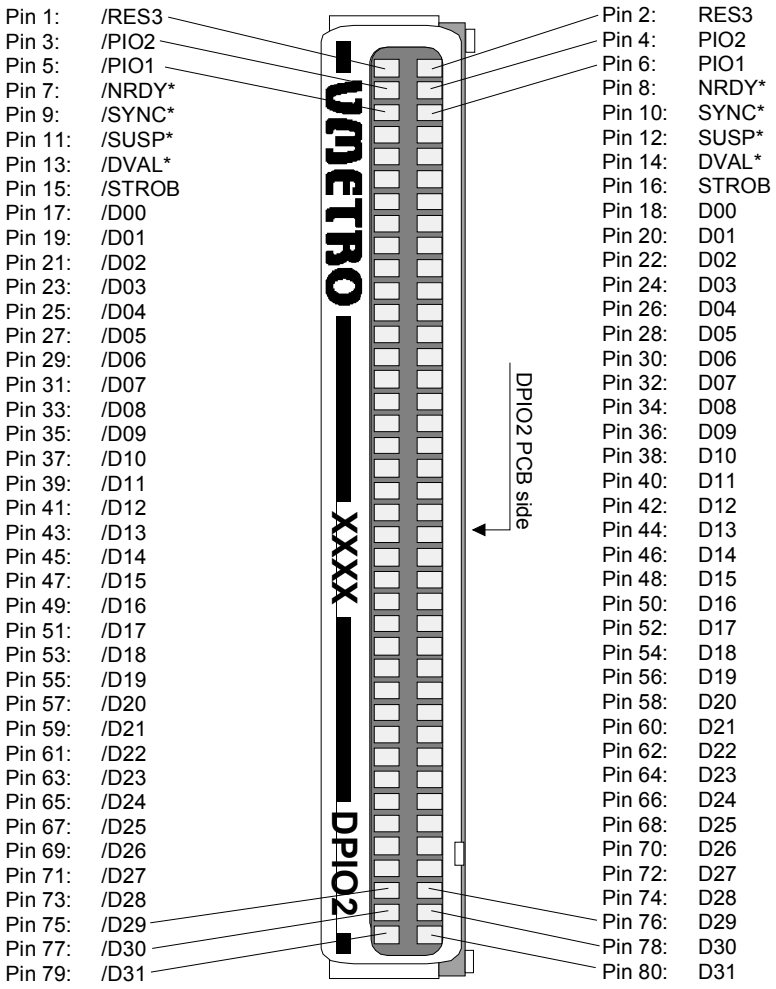

Table 24. Connector pinout – DPIO2-DIU models

C.3 Jumpers on DPIO2-DIU

See chapter 4.9.4.4.

C.4 Switching characteristics, DPIO2-DIU

The DPIO2 has different setup and hold times depending on how the DPIO2 is set up. To get the best setup and hold times needed when running at maximum speed, an internal PLL is used to improve timing. This PLL can not be used when the frequency of the strobe is below 10MHz.

Parameter symbol	Parameter Description	Using PLL	Not using PLL
t_{su}	Set-up time	6.0ns	4.5ns
t_h	Hold time	8.3ns	14.1ns

Table 25. Setup and hold times – DPIO2-DIU

C.5 Signal termination

All input signals have a 110-ohm resistor between the two signals in the RS422 signal pairs. Output signals do not have any termination resistance.

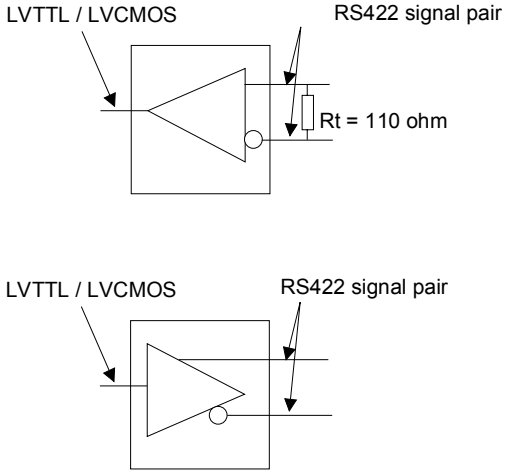

Figure 14 Termination of RS422 signal pair

C.6 Line drivers / receivers

Signal	Device Part no	Device manufacturer	Direction
D[0] – D[31]	SN75976A2DGG	Texas Instruments	Input
RES3			Input
DVAL*			Input
SYNC*			Input
NRDY*			Output
SUSPEND*			Output
PIO1			Input/output
PIO2			Input/output
STROB	SN75ALS176-BD	Texas Instruments	Input

Table 26. Line drivers and receivers on DPIO2-DIU models

APPENDIX D. DPIO2-DOU RS422 OUTPUT FRONT END

D.1 Supported Features

This chapter describes the RS422 output front-end interface of the DPIO2-DOU models. The interface is still based on the FPDP protocol, the electrical levels, however, are in accordance to the RS422 standard. Data width is maximum 32 bits, and can operate at speeds up to 20MHz. The model has support for handshake, has user defined signals, and has data valid bit and synchronisation capabilities.

Double clocking

The DPIO2 has a feature that allows using both edges of the strobe to clock data. In this way the data speed can be doubled and this gives a bandwidth of 160MB/s. The clock will still be running at 20MHz.

Note: The numbers given above regarding the frequency and transfer rate is only applicable when the data transmitter is generating strobe.

D.2 Signal Description and Pin Assignments

Note: The front end connector pinout is inverted on DPIO2 compared to the first gen. DPIO-Lx.

Signal	Name	Direction	Signal Description
D(31:00) /D(31:00)	Data Bus	O	32-bit data bus driven by transmitter.
DVALID* /DVALID*	Data Valid	O	When asserted, DVALID* indicates that the data bus has valid data. This signal is generated by the data source with each sample.
STROB /STROB	Data Strobe	O	STROB is a free running clock. Receiver boards should clock data at the rising edge of STROB when DVALID* is asserted
NRDY* /NRDY*	Not Ready	I	NRDY* should be asserted by receiver boards, when they are not ready to receive data. Transmitter should not transmit data before NRDY* is negated.
PIO2, PIO1 /PIO2, /PIO1	Program mable I/O	I/O	The PIO signals are programmable I/O lines for user-defined functions. They may be configured as inputs or outputs.
RES3 /RES3	Reserved	O	Reserved for user defined signal.
SUSPEND* /SUSPEND*	Suspend Data	I	SUSPEND* should be generated by receiver boards to inform the data source of a pending buffer overflow condition. This function may be disabled with control register bit.
SYNC* /SYNC*	Sync. Pulse	O	The transmitter provides sync. pulses to receiver boards to synchronize data transfers. See separate section for details.

DVALID*, /DVALID*, SUSPEND*, /SUSPEND*, SYNC*, /SYNC*, NRDY* and /NRDY* are active low signals.

Table 27. Signal description – DPIO2-DIU models

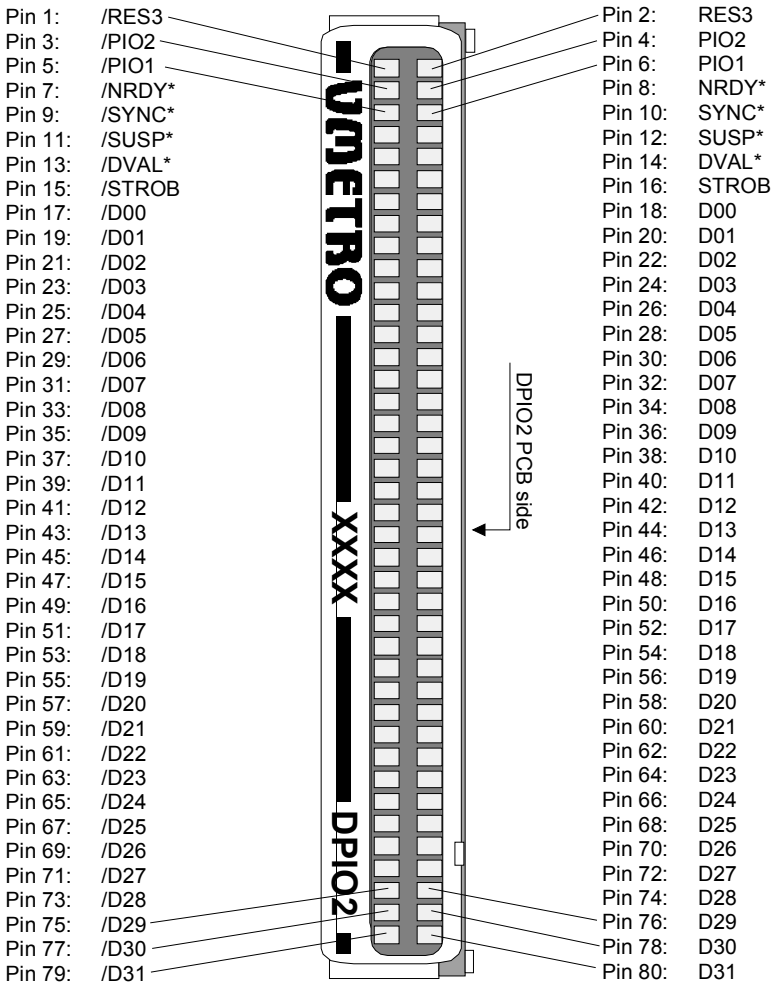

Figure 15 Connector pinout – DPIO2-DOU models

D.3 Jumpers on DPIO2-DOU

See chapter 4.9.4.4.

D.4 Switching characteristics, DPIO2-DOU

The DPIO2 inverts the strobe signal out on the cable. That way the data will switch around negative edge of the strobe, and give very good setup and hold times to the input module. In addition an internal PLL is used to improve timing. This PLL can not be used when the frequency of the strobe is below 10MHz.

The times below are given in respect to the negative edge. To calculate what the times will be compared to the positive edge of the strobe, half a period needs to be added.

Parameter symbol	Parameter Description	t_{co} [ns]
Min t_{co}	**Negative** edge of clock to output	-9
Typ t_{co}	**Negative** edge of clock to output	2 - 8
Max t_{co}	**Negative** edge of clock to output	16.8

Table 28. Clock to output time – DPIO2-DOU in output mode

D.5 Signal termination

All input signals have a 110-ohm resistor between the two signals in the RS422 signal pairs. Output signals do not have any termination resistance.

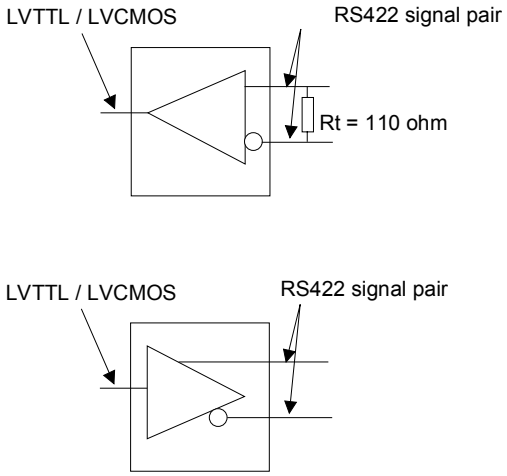

Figure 16 Termination of RS422 signal pair

D.6 Line drivers / receivers

Signal	Device Part no	Device manufacturer	Direction
D[0] – D[31]	SN75976A2DGG	Texas Instruments	Output
RES3			Output
DVAL*			Output
SYNC*			Output
NRDY*			Input
SUSPEND*			Input
PIO1			Input/output
PIO2			Input/output
STROB	SN65ALS176D	Texas Instruments	Output

Table 29. Line drivers and receivers on DPIO2-DOU models

APPENDIX E. DPIO2-EIU PECL INPUT FRONT-END

E.1 Supported Features

This chapter describes the PECL (Positive ECL) input front-end interface of the DPIO2-EIU models. The interface is still based on the FPDP protocol, however, electrical PECL (Positive ECL) levels are used. Data width is maximum 16 bits, and can operate at speeds up to 70MHz. The model has support for handshake, has user defined signals, and has data valid bit and synchronisation capabilities.

Double clocking

The DPIO2 has a feature that allows using both edges of the strobe to clock data. In this way the data speed can be doubled and this gives a bandwidth of 200MB/s. The clock will still be running at 50MHz.

Note: The numbers given above regarding the frequency and transfer rate is only applicable when the data transmitter is generating strobe.

E.2 Signal Description and Assignments

Signal	Name	Direction	Signal Description
D(15:00) /D(15:00)	Data Bus	I	16-bit data bus driven by transmitter.
DVALID* /DVALID*	Data Valid	I	When asserted, DVALID* indicates that the data bus has valid data. This signal is generated by the data source with each sample.
STROB /STROB	Data Strobe	I	STROB is a free running clock. Receiver boards should clock data at the rising edge of STROB when DVALID* is asserted
NRDY* /NRDY*	Not Ready	O	NRDY* should be asserted by receiver boards, when they are not ready to receive data. Transmitter should not transmit data before NRDY* is negated. **Note**: This signal is not available on the PECL models of the first generation of DPIO, DPIO-EO and DPIO-EI.
PIO1 /PIO1	Program mable I/O	I	User defined signal. Status register bit.
PIO2 /PIO2	Program mable I/O	O	User defined signal. Status register bit.
SUSPEND* /SUSPEND*	Suspend Data	O	SUSPEND* should be generated by receiver boards to inform the data source of a pending buffer overflow condition. This function may be disabled with control register bit.
SYNC* /SYNC*	Sync. Pulse	I	The transmitter provides sync. pulses to receiver boards to synchronize data transfers. See separate section for details.

DVALID*, /DVALID*, SUSPEND*, /SUSPEND*, SYNC*, /SYNC*, NRDY* and /NRDY* are active low signals.

Table 30. Signal description – DPIO2-EIU models

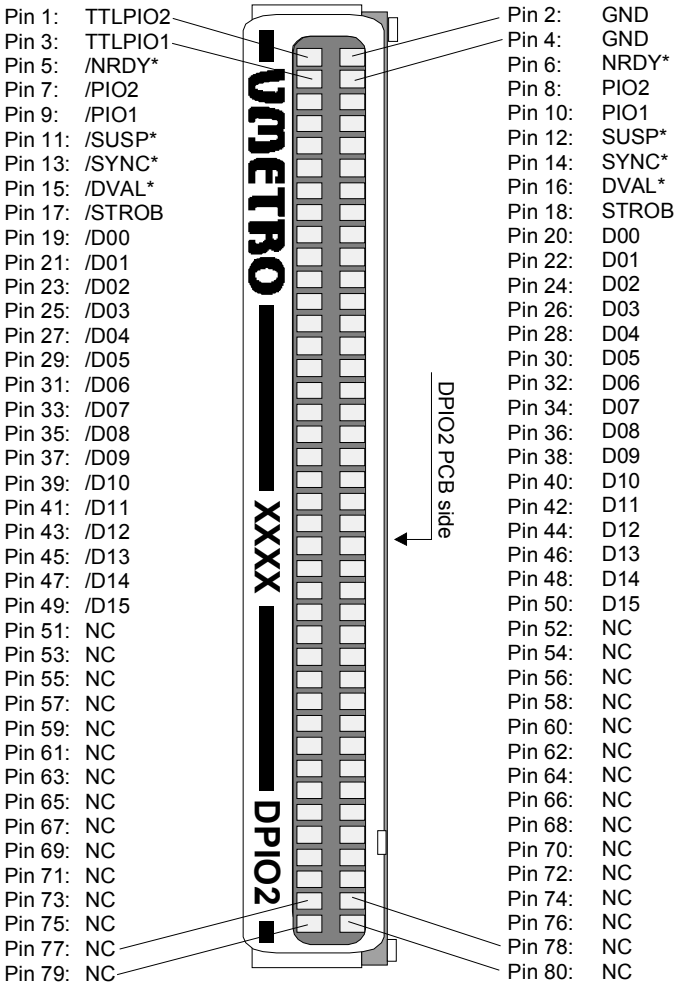

Figure 17 Connector pinout – DPIO2-EIU models

E.3 Jumpers on DPIO2-EIU Interface

See chapter 4.9.4.5.

E.4 Switching characteristics, DPIO2-EIU

The DPIO2 has different setup and hold times depending on how the DPIO2 is set up. To get the best setup and hold times needed when running at maximum speed, an internal PLL is used to improve timing. This PLL cannot be used when the frequency of the strobe is below 10MHz.

In addition a PLL mounted on the personality module may be used on the DPIO2-EIU to achieve 0 ns hold time.

Frequency [MHz]	t_{su} [ns]		t_h [ns]		Comments
	Use of PLL on PM	No use of PLL on PM	Use of PLL on PM	No use of PLL on PM	
f < 10	NA	4.4	NA	9.6	
10 < f < 15	NA		NA		
15.0	12.0		0		
20.0	10.5		0		
25.0	9.5		0.4		
25.1	12.0		0		
30.0	11.0		0		t_{su} =4.4, t_h =9.6 may be chosen if PLL on CBU is disabled (own SW drivers to be written) (PLL on PM disabled)
35.0	10.3	5.9	0	3.8	
40.0	9.7		0		
45.0	9.3		0.4		
50.0	9.0		0.7		
50.1	10.9		0		
55.0	10.5		0		
60.0	10.1		0		
65.0	9.7		0		
70.0	9.5		0.2		
75.0	9.2		0.5		

Table 31. Setup and hold times – DPIO2-EIU

E.5 Signal termination

All input signals have a 110-ohm resistor between the two signals in the PECL signal pairs. Output signals have a 390 ohm resistor connected to ground for each signal in the signal pair.

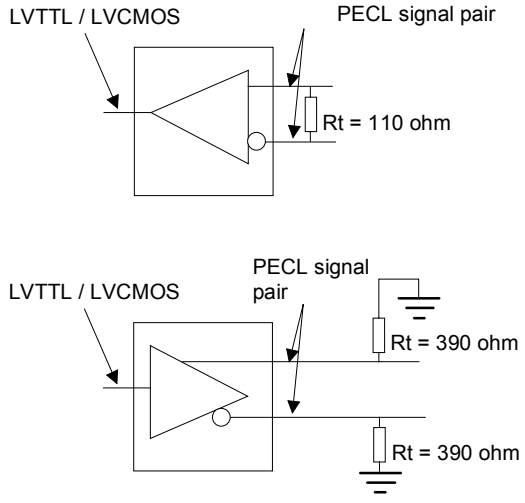

Figure 18 Termination of PECL signal pair

E.6 Line drivers / receivers

Signal	Device Part no	Device manufacturer	Direction
D[0] – D[15] DVAL* SYNC* PIO1	MC100ELT23DT	ON Semiconductor	Input
NRDY* SUSPEND* PIO2	MC100ELT22DT	ON Semiconductor	Output
STROB	MC100ELT28DT	ON Semiconductor	Input/Output

Table 32. Line drivers and receivers on DPIO2-EIU models

APPENDIX F. DPIO2-EOU PECL OUTPUT FRONT-END

F.1 Supported Features

This chapter describes the PECL (Positive ECL) output front-end interface of the DPIO2-EIU models. The interface is still based on the FPDP protocol, however, electrical PECL (Positive ECL) levels are used. Data width is maximum 16 bits, and can operate at speeds up to 70MHz. The model has support for handshake, has user defined signals, and has data valid bit and synchronisation capabilities.

Double clocking

The DPIO2 has a feature that allows using both edges of the strobe to clock data. In this way the data speed can be doubled and this gives a bandwidth of 200MB/s. The clock will still be running at 50MHz.

Note that the sustained maximum data rate is limited by PCI bandwidth. The DPIO2 supports 64bit/33MHz PCI interface with a maximum through put of 266MB/s.

Note: The numbers given above regarding the frequency and transfer rate is only applicable when the data transmitter is generating strobe.

F.2 Signal Description and Assignments

Signal	Name	Direction	Signal Description
D(15:00) /D(15:00)	Data Bus	O	16-bit data bus driven by transmitter.
DVALID* /DVALID*	Data Valid	O	When asserted, DVALID* indicates that the data bus has valid data. This signal is generated by the data source with each sample.
STROB /STROB	Data Strobe	O	STROB is a free running clock. Receiver boards should clock data at the rising edge of STROB when DVALID* is asserted
NRDY* /NRDY*	Not Ready	I	NRDY* should be asserted by receiver boards, when they are not ready to receive data. Transmitter should not transmit data before NRDY* is negated. **Note**: This signal is not available on the PECL models of the first generation of DPIO, DPIO-EO and DPIO-EI.
PIO1 /PIO1	Program mable I/O	O	User defined signal. Status register bit.
PIO2 /PIO2	Program mable I/O	I	User defined signal. Status register bit.
SUSPEND* /SUSPEND*	Suspend Data	I	SUSPEND* should be generated by receiver boards to inform the data source of a pending buffer overflow condition. This function may be disabled with control register bit.
SYNC* /SYNC*	Sync. Pulse	O	The transmitter provides sync. pulses to receiver boards to synchronize data transfers. See separate section for details.

DVALID*, /DVALID*, SUSPEND*, /SUSPEND*, SYNC*, /SYNC*, NRDY* and /NRDY* are active low signals.

Table 33. Signal description – DPIO2-EOU models

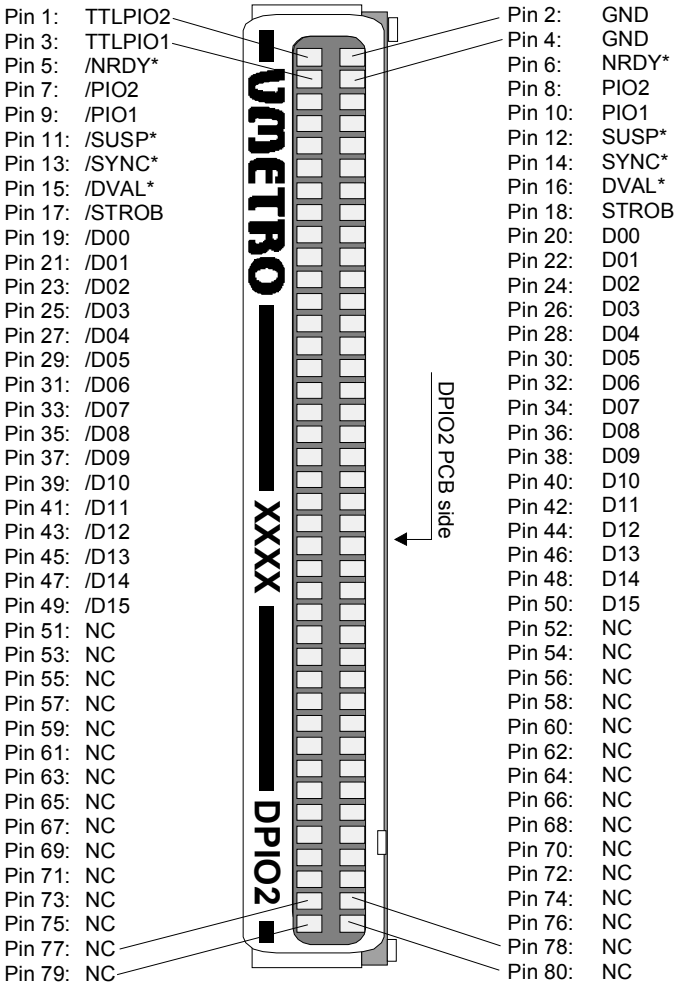

Figure 19 Connector pinout – DPIO2-EOU models

F.3 Jumpers on DPIO2-EOU Interface

See chapter 4.9.4.5.

F.4 Switching characteristics, DPIO2-EOU

The DPIO2 inverts the strobe signal out on the cable. That way the data will switch around negative edge of the strobe, and give very good setup and hold times to the input module. In addition an internal PLL is used to improve timing. This PLL can not be used when the frequency of the strobe is below 10MHz.

The times below are given in respect to the negative edge. To calculate what the times will be compared to the positive edge of the strobe, half a period needs to be added.

Parameter symbol	Parameter Description	t_{co} [ns]
Min t_{co}	**Negative** edge of clock to output	0.5
Typ t_{co}	**Negative** edge of clock to output	2 – 3
Max t_{co}	**Negative** edge of clock to output	5.2

Table 34. Clock to output time – DPIO2-EOU in output mode

F.5 Signal termination

All input signals have a 110-ohm resistor between the two signals in the PECL signal pairs. Output signals have a 390 ohm resistor connected to ground for each signal in the signal pair.

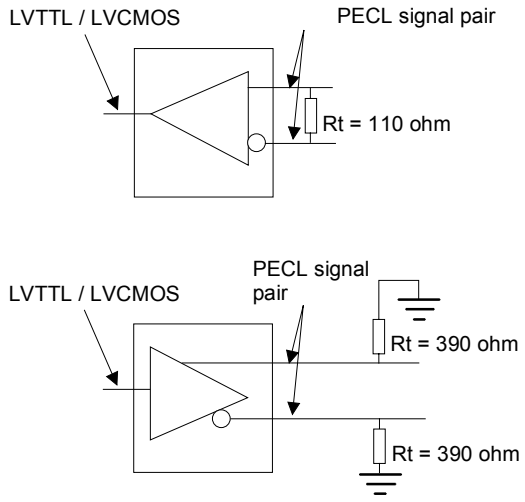

Figure 20 Termination of PECL signal pair

F.6 Line drivers / receivers

Signal	Device Part no	Device manufacturer	Direction
D[0] – D[15] DVAL* SYNC* PIO1	MC100ELT22DT	ON Semiconductor	Output
NRDY* SUSPEND* PIO2	MC100ELT23DT	ON Semiconductor	Input
STROB	MC100ELT28DT	ON Semiconductor	Input/Output

Table 35. Line drivers and receivers on DPIO2-EOU models

APPENDIX G. VERIFICATION OF SIGNAL QUALITY AND TIMIMG AT THE FRONT END CONNECTOR

G.1 Introduction

This appendix describes how to verify signal quality and timing at the front end connector in order to verify robust signaling conditions and troubleshoot sporadic errors occur due to suspected signal integrity problems on the cable.

NOTE: When signal integrity problems are suspected, start troubleshooting by verifying that the cable is properly terminated in the actual application. On
DPIO2-FBU, some of the signal terminations are SW controlled. Other boards may use jumpers or socket-mounted resistors for this purpose

DPIO2 exists in bidirectional as well as input-only and output-only models. When signal integrity problems are suspected, it is important to check that the signal timing on the output device matches the required setup and hold times for the input. It is also important that the terminations of the signals are correct, i.e. that the terminations are in accordance with the signal standard used (e.g. RS422, PECL, etc.).
DPIO2-FBU meets the FPDP timing specification both as input and output.

G.2 Type of sporadic errors

The following sporadic errors may occur:

Bit error
Possible reason: Bad signal quality on STROB or DATA
Violation of setup and hold times

Addition of one or more data words
Possible reason: Bad signal quality on STROB, DVALID or SYNC
Violation of setup and hold times

Loss of one or more data words
Possible reason: Bad signal quality on STROB, DVALID or SYNC
Violation of setup and hold times

G.3 Where to measure

Signal quality should be measured on the input module(s). Measuring signal integrity in a DPIO2 application is a challenge. It is difficult to achieve correct measurements without disturbances. To get the most correct measurements possible, use high quality oscilloscope and probes that are capable of measuring the actual signal frequency.

Avoid long grounding wires. It is often difficult to get access to the signals. The figure and the table below show where the different signals could be measured.

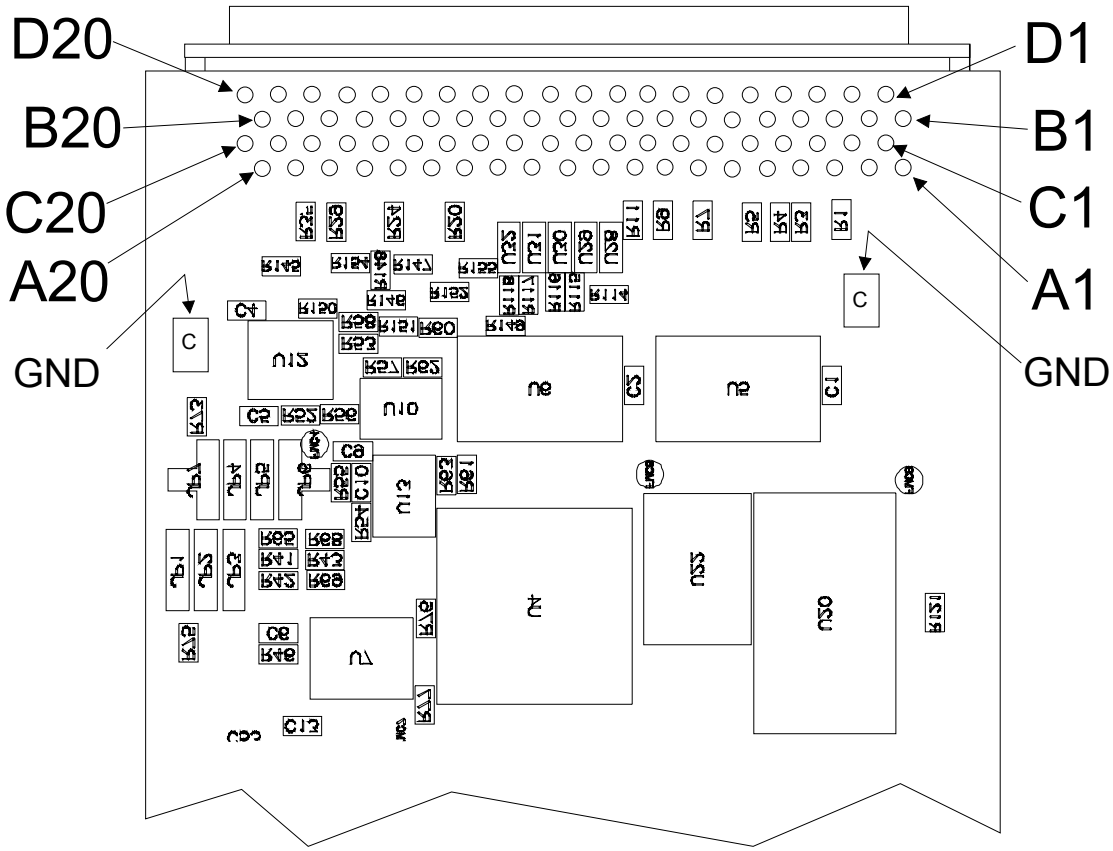

Figure 21 Pin definition on Front End connector

DPIO2 Model	STROB	$\overline{\text{STROB}}$	PSTROB (PECL)	$\overline{\text{PSTROB}}$ (PECL)	DVALID*	$\overline{\text{DVALID*}}$	D[0]	$\overline{\text{D[0]}}$	D[15]	$\overline{\text{D[15]}}$
DPIO2-FBU	C20	NA	D14	B14	B13	NA	B1	NA	D6	
DPIO2-LBU	D4	C4	NA	NA	B4	A4	B5	A5	D12	C12
DPIO2-DIU	D4	C4	NA	NA	B4	A4	B5	A5	D12	C12
DPIO2-EIU	B5	A5	NA	NA	D4	C4	D5	C5	B13	A13

Table 36. Signals on the Front End connector

G.4 Checking signal quality

To check the signal quality, the following should be investigated:

Signal levels

Check that the signal levels are outside the ambiguous zone.

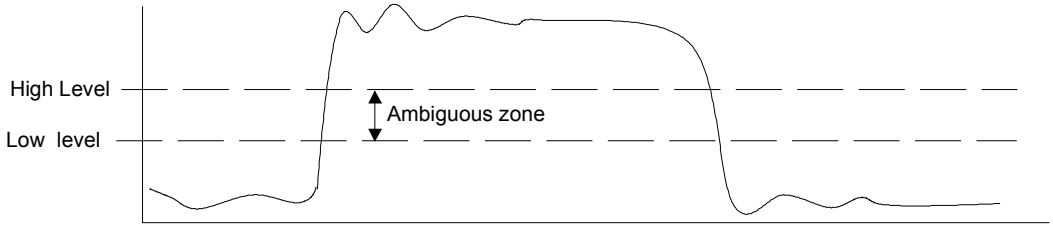

Figure 22 Measurement on DPIO2-FBU

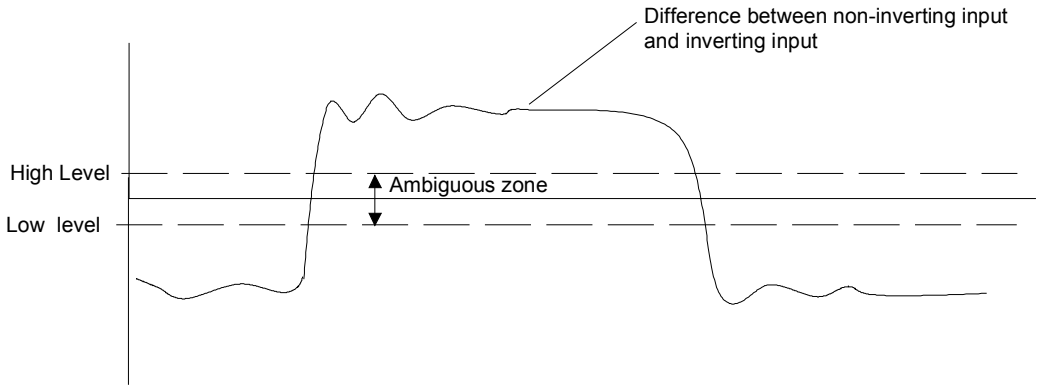

Figure 23 Measurement on DPIO2-LBU/EIU/DIU

Note: On DPIO2-LBU/DIU/EIU, the *difference* between the non-inverting and the inverting input must be measured due to the balanced signal type. The PECL strobe on DPIO2-FBU is also a balanced signal type.

The levels are as follows

	High level	Low level
DPIO2-FBU (TTL)	> 2.0 V	< 0.8V
DPIO2-FBU (PECL STROB)	Non-inv input – inv input > 310 mV	Non-inv input – inv input < -310 mV
DPIO2-LBU (LVDS)	Non-inv input – inv input > 100 mV	Non-inv input – inv input < -100 mV
DPIO2-DIU (RS422)	Non-inv input – inv input > 200 mV	Non-inv input – inv input < -200 mV
DPIO2-EIU (PECL)	Non-inv input – inv input > 310mV	Non-inv input – inv input < -310 mV

Table 37. Signal Levels

Setup and hold times

Compare the timing of STROB and data with the required setup and hold times for the input module.

The setup and hold times for the different models are given in the appendixes for each of the model front end.

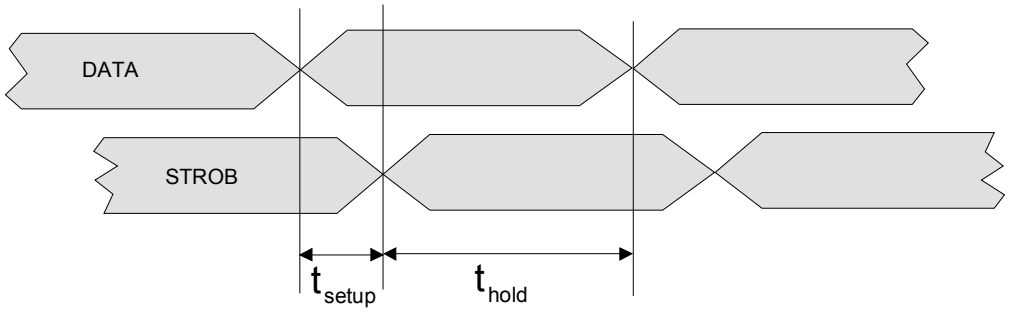

Figure 24 Setup and hold times

G.5 Failure mechanisms

The following examples explain some possible failure mechanisms.

The described mechanisms could be caused by reflections of signals due to a mismatch between cable impedance and cable termination. The different interface standards (TTL, RS422, PECL, LVDS, etc.) have different types of termination. More detailed information about termination is described in the appendixes for each of the model front end. The characteristics of the oscillations will vary with frequency and cable length. The number of loads connected to the same cable will also influence the signal quality. Suggested actions for improving the signal quality are:

Reduce the cable length

Lower the frequency

If multidrop application is used, gather the input modules as close together as possible at one end of the cable and the output module at the other end.

Unintentional clocking of data due to oscillations on clock edges

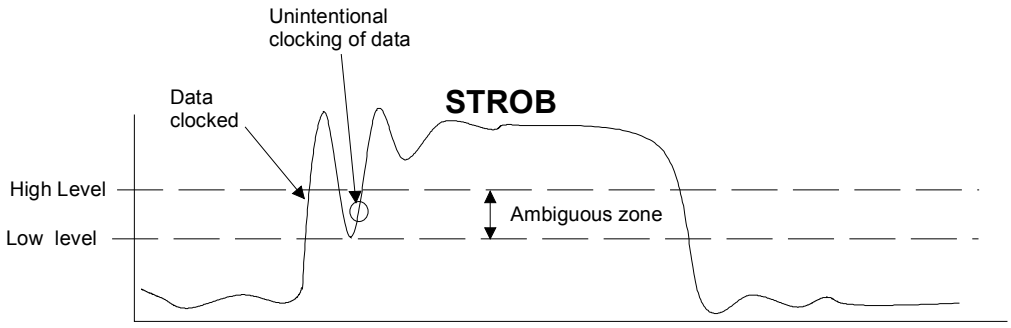

Figure 25 Unintentional clocking of data

Failure mechanism: The strobe signal oscillates and re-enters the ambiguous zone, the positive going edge within the ambiguous zone may cause invalid data to be clocked in.

Unintentional clocking of data due to oscillations on DVALID*

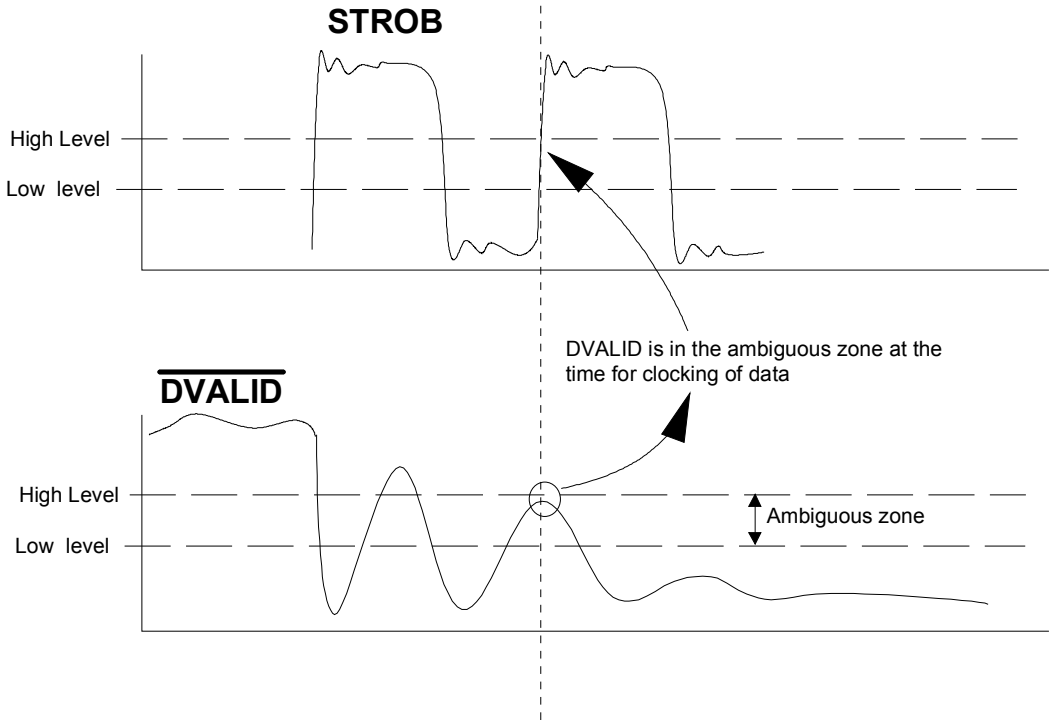

Figure 26 Oscillations on DVALID

Failure mechanism: The DVALID* signal oscillates and enters the ambiguous zone, which occurs at the same time data is clocked in. This may cause the DVALID* signal to be seen as active at the time of clocking in the data.

Data is not clocked due to oscillations on the DVALID signal

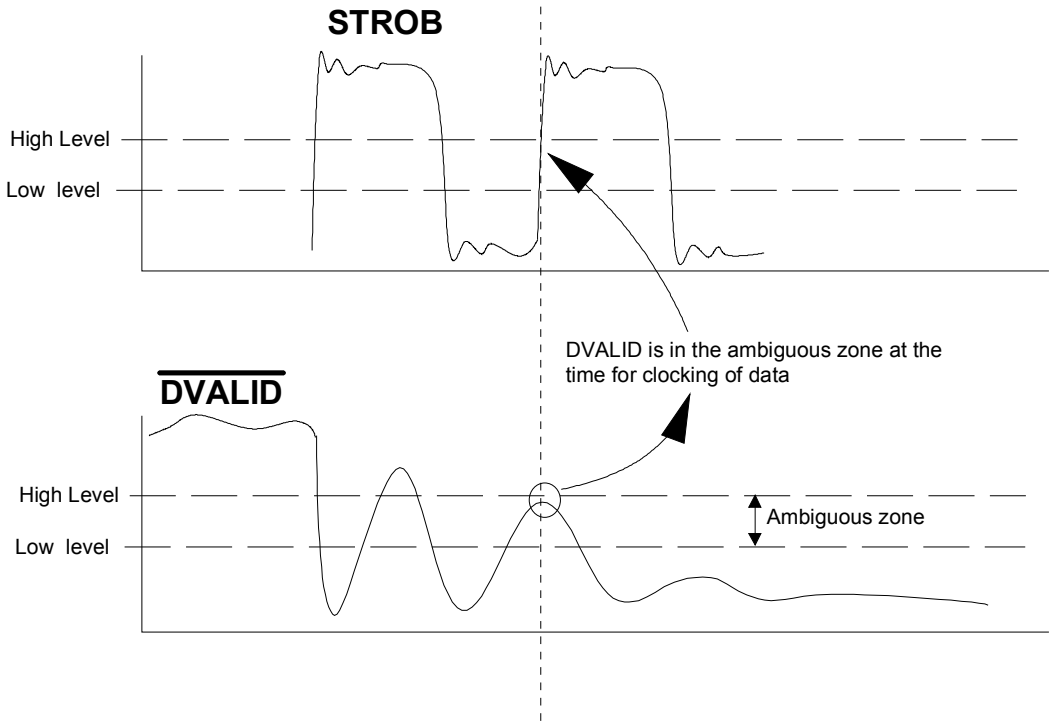

Figure 27 Oscillations on DVALID

Failure mechanism: The DVALID* signal oscillates and enters the ambiguous zone, which occurs at the same time data is clocked in. This may cause the DVALID* signal to be seen as inactive at the time for clocking in data.

Data is wrong due to oscillations on the data signal

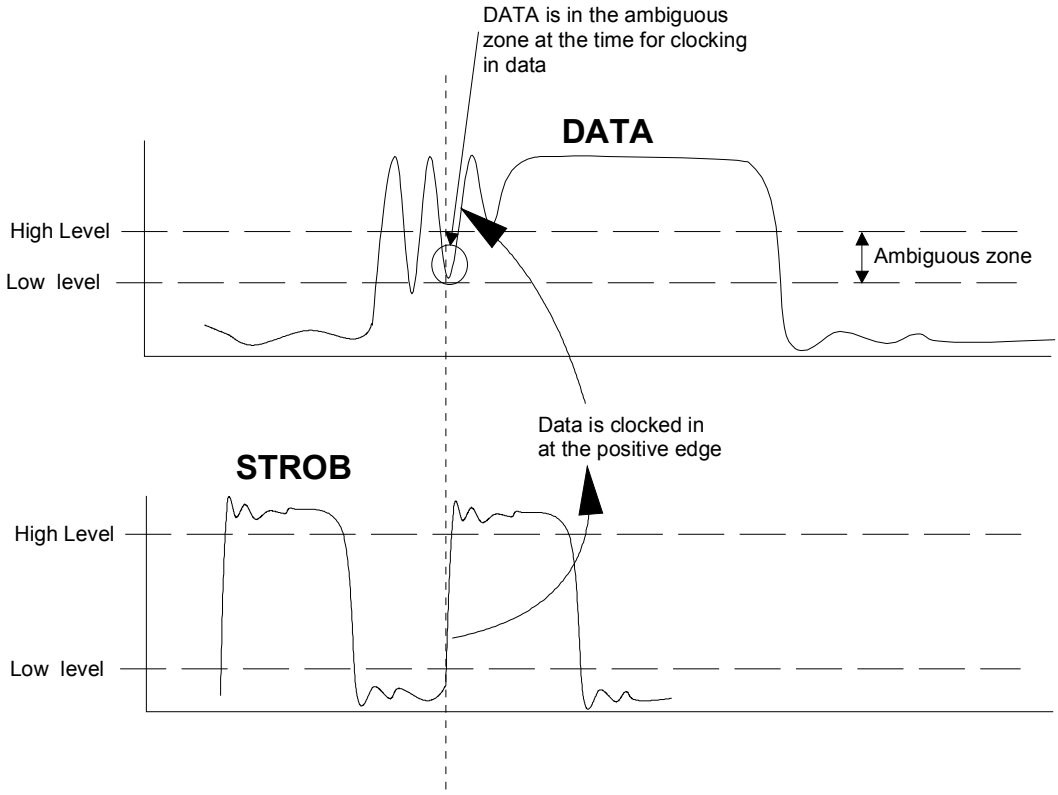

Figure 28 Oscillations on DATA

Failure mechanism: The data signal oscillates and enters the ambiguous zone, which may cause the signal to be seen as a 'zero' by the receiver circuit.

G.6 Fault finding

Find out the kind of error:

- Bit error
- Addition of data
- Loss of data

Bit error
Look at the data bit at the time for clocking the data. Check if the voltage level for the data bit is in the ambiguous zone.
Measure the setup and hold times and compare them with the times given in this manual (see appendix for the actual front end).

Addition of data
Look at the level for the strobe.
Check the level for the DVALID* signal.
Measure the setup and hold times and compare them with the times given in this manual (see appendix for the actual front end).

Loss of data
Check the level of the DVALID* signal at the time of clocking in the data.
Measure the setup and hold times and compare them with the times given in in this manual (see appendix for the actual front end).