



**Related U.S. Application Data**

continuation of application No. 13/801,868, filed on Mar. 13, 2013, now Pat. No. 8,664,699, which is a continuation of application No. 13/113,504, filed on May 23, 2011, now Pat. No. 8,440,546, which is a continuation of application No. 12/564,566, filed on Sep. 22, 2009, now Pat. No. 7,982,296, which is a division of application No. 11/145,574, filed on Jun. 2, 2005, now Pat. No. 7,622,367.

- (60) Provisional application No. 60/577,077, filed on Jun. 4, 2004, provisional application No. 60/601,061, filed on Aug. 11, 2004, provisional application No. 60/650,305, filed on Feb. 4, 2005, provisional application No. 60/663,391, filed on Mar. 18, 2005, provisional application No. 60/677,617, filed on May 4, 2005.

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(56)

**References Cited****U.S. PATENT DOCUMENTS**

4,058,418 A	11/1977	Lindmayer
4,392,451 A	7/1983	Mickelsen et al.
4,471,003 A	9/1984	Cann
4,487,162 A	12/1984	Cann
4,663,828 A	5/1987	Hanak
4,761,335 A	8/1988	Aurichio et al.
4,766,670 A	8/1988	Gazdik et al.
4,784,720 A	11/1988	Douglas
4,855,017 A	8/1989	Douglas
5,041,973 A	8/1991	Lebron et al.
5,086,785 A	2/1992	Gentile et al.
5,118,400 A	6/1992	Wollam
5,178,957 A	1/1993	Kolpe et al.
5,204,144 A	4/1993	Cann et al.
5,313,094 A	5/1994	Beyer et al.
5,403,700 A	4/1995	Heller et al.
5,427,096 A	6/1995	Bogusiewicz et al.
5,434,751 A	7/1995	Cole, Jr. et al.
5,455,178 A	10/1995	Fattinger
5,465,009 A	* 11/1995	Drabik ..... H01L 24/96 257/723
5,469,845 A	11/1995	Delonzor et al.
5,475,514 A	12/1995	Salerno et al.
5,491,350 A	* 2/1996	Unno ..... H01L 33/22 257/81
5,501,893 A	3/1996	Laermer et al.
5,525,815 A	6/1996	Einset
5,545,291 A	8/1996	Smith et al.
5,625,471 A	4/1997	Smith
5,648,148 A	7/1997	Simpson
5,687,737 A	11/1997	Branham et al.
5,691,245 A	11/1997	Bakhit
5,753,529 A	5/1998	Chang et al.
5,757,081 A	5/1998	Chang et al.
5,767,578 A	6/1998	Chang et al.
5,772,905 A	6/1998	Chou
5,783,856 A	7/1998	Smith et al.
5,790,151 A	8/1998	Mills

(56)	References Cited					
U.S. PATENT DOCUMENTS						
5,817,242 A	10/1998	Biebuyck et al.	6,787,052 B1	9/2004	Vaganov	
5,824,186 A	10/1998	Smith et al.	6,814,898 B1	11/2004	Deeman et al.	
5,904,545 A	5/1999	Smith et al.	6,816,380 B2	11/2004	Credelle et al.	
5,907,189 A	5/1999	Mertol	6,844,673 B1	1/2005	Bernkopf	
5,915,180 A	6/1999	Hara et al.	6,848,162 B2	2/2005	Arneson et al.	
5,917,534 A	6/1999	Rajeswaran	6,850,312 B2	2/2005	Jacobsen et al.	
5,928,001 A	7/1999	Gilette et al.	6,856,830 B2	2/2005	He	
5,955,781 A	9/1999	Joshi et al.	6,863,219 B1	3/2005	Jacobsen et al.	
5,976,683 A	11/1999	Liehr et al.	6,864,435 B2	3/2005	Hermanns et al.	
5,998,291 A	12/1999	Bakhit et al.	6,864,570 B2	3/2005	Smith	
6,024,702 A	2/2000	Iverson	6,872,645 B2	3/2005	Duan et al.	
6,057,212 A	5/2000	Chan et al.	6,878,871 B2	4/2005	Scher et al.	
6,080,608 A	6/2000	Nowak	6,881,979 B2	4/2005	Starikov et al.	
6,097,984 A	8/2000	Douglas	6,885,030 B2	4/2005	Onozuka et al.	
6,121,110 A	9/2000	Hong et al.	6,887,450 B2	5/2005	Chen et al.	
6,150,602 A	11/2000	Campbell	6,887,792 B2	5/2005	Perlov et al.	
6,165,391 A	12/2000	Vedamuttu	6,900,094 B2	5/2005	Hammond et al.	
6,171,730 B1	1/2001	Kuroda et al.	6,917,061 B2	7/2005	Pan et al.	
6,225,149 B1	5/2001	Gan et al.	6,936,181 B2	8/2005	Bulthaup et al.	
6,232,136 B1	5/2001	Zavracky et al.	6,949,199 B1	9/2005	Gauzner et al.	
6,236,883 B1	5/2001	Ciaccio et al.	6,949,206 B2	9/2005	Whiteford	
6,265,326 B1	7/2001	Ueno	6,950,220 B2	9/2005	Abramson et al.	
6,267,775 B1	7/2001	Clerc et al.	6,984,934 B2	1/2006	Moller et al.	
6,274,508 B1	8/2001	Jacobsen et al.	6,989,285 B2	1/2006	Ball	
6,276,775 B1	8/2001	Schulte	7,029,951 B2	4/2006	Chen et al.	
6,277,711 B1	8/2001	Wu	7,033,961 B1	4/2006	Smart et al.	
6,277,712 B1	8/2001	Kang et al.	7,067,903 B2	6/2006	Tachibana et al.	
6,281,038 B1	8/2001	Jacobsen et al.	7,116,318 B2	10/2006	Amundson et al.	
6,284,418 B1	9/2001	Trantolo	7,132,313 B2	11/2006	O'Connor et al.	
6,291,896 B1	9/2001	Smith	7,148,512 B2	12/2006	Leu et al.	
6,316,278 B1	11/2001	Jacobsen et al.	7,158,277 B2	1/2007	Berggren et al.	
6,316,283 B1	11/2001	Saurer	7,169,546 B2	1/2007	Suzuki et al.	
6,317,175 B1	11/2001	Salerno et al.	7,169,669 B2	1/2007	Blakers et al.	
6,322,895 B1	11/2001	Canham	7,170,164 B2	1/2007	Chen et al.	
6,334,960 B1	1/2002	Wilson et al.	7,186,624 B2	3/2007	Welser et al.	
6,380,729 B1	4/2002	Smith	7,190,051 B2	3/2007	Mech et al.	
6,403,397 B1	6/2002	Katz	7,195,733 B2	3/2007	Rogers et al.	
6,403,985 B1	6/2002	Fan et al.	7,223,609 B2	5/2007	Anvar et al.	
6,413,790 B1	7/2002	Duthaler et al.	7,223,632 B2	5/2007	Onozuka et al.	
6,417,025 B1	7/2002	Gengel	7,253,442 B2	8/2007	Huang et al.	
6,420,266 B1	7/2002	Smith et al.	7,255,919 B2	8/2007	Sakata et al.	
6,433,401 B1	8/2002	Clark et al.	7,291,540 B2	11/2007	Mech et al.	
6,451,191 B1	9/2002	Bentsen et al.	7,374,968 B2	5/2008	Kornlivich et al.	
6,459,418 B1	10/2002	Comiskey et al.	7,425,523 B2	9/2008	Ikemizu et al.	
6,468,638 B2	10/2002	Jacobsen et al.	7,521,292 B2	4/2009	Rogers et al.	
6,479,395 B1	11/2002	Smith et al.	7,557,367 B2	7/2009	Rogers et al.	
6,517,995 B1	2/2003	Jacobson et al.	7,622,367 B1	11/2009	Nuzzo et al.	
6,518,168 B1	2/2003	Clem et al.	7,629,691 B2	12/2009	Roush et al.	
6,527,964 B1	3/2003	Smith et al.	7,635,755 B2	12/2009	Kaplan et al.	
6,555,408 B1	4/2003	Jacobsen et al.	7,674,882 B2	3/2010	Kaplan et al.	
6,566,744 B2	5/2003	Gengel	7,700,402 B2	4/2010	Wild et al.	
6,580,151 B2	6/2003	Vandeputte et al.	7,704,684 B2	4/2010	Rogers et al.	
6,586,338 B2	7/2003	Smith et al.	7,705,280 B2	4/2010	Nuzzo et al.	
6,590,346 B1	7/2003	Hadley et al.	7,709,961 B2	5/2010	Greenberg et al.	
6,606,079 B1	8/2003	Smith	7,727,575 B2	6/2010	Kaplan et al.	
6,606,247 B2	8/2003	Credelle et al.	7,799,699 B2	9/2010	Nuzzo et al.	
6,608,370 B1	8/2003	Chen et al.	7,842,780 B2	11/2010	Kaplan et al.	
6,623,579 B1	9/2003	Smith et al.	7,932,123 B2	4/2011	Rogers et al.	
6,639,578 B1	10/2003	Comiskey et al.	7,943,491 B2	5/2011	Nuzzo et al.	
6,655,286 B2	12/2003	Rogers	7,972,875 B2	7/2011	Rogers et al.	
6,657,289 B1	12/2003	Craig et al.	7,982,296 B2	7/2011	Nuzzo et al.	
6,661,037 B2	12/2003	Pan et al.	8,039,847 B2	10/2011	Nuzzo et al.	
6,665,044 B1	12/2003	Jacobsen et al.	8,198,621 B2	6/2012	Rogers et al.	
6,666,821 B2	12/2003	Keimel	8,217,381 B2	7/2012	Rogers et al.	
6,667,548 B2	12/2003	O'Connor et al.	8,367,035 B2	2/2013	Rogers et al.	
6,683,663 B1	1/2004	Hadley et al.	8,394,706 B2	3/2013	Rogers et al.	
6,693,384 B1	2/2004	Vicentini et al.	8,440,546 B2	5/2013	Nuzzo et al.	
6,706,402 B2	3/2004	Rueckes et al.	8,470,701 B2	6/2013	Rogers et al.	
6,720,469 B1	4/2004	Curtis et al.	8,552,299 B2	10/2013	Rogers et al.	
6,723,576 B2	4/2004	Nozawa et al.	8,562,095 B2	10/2013	Alleyne et al.	
6,730,990 B2	5/2004	Kondo et al.	8,664,699 B2	3/2014	Nuzzo et al.	
6,731,353 B1	5/2004	Credelle et al.	8,666,471 B2	3/2014	Rogers et al.	
6,743,982 B2	6/2004	Biegelsen et al.	8,679,888 B2	3/2014	Rogers et al.	
6,780,696 B1	8/2004	Schatz	8,722,458 B2	5/2014	Rogers et al.	
6,784,450 B2	8/2004	Pan et al.	8,729,524 B2	5/2014	Rogers et al.	
			8,754,396 B2	6/2014	Rogers et al.	
			8,865,489 B2	10/2014	Rogers et al.	
			8,895,406 B2	11/2014	Rogers et al.	
			8,934,965 B2	1/2015	Rogers et al.	

(56)

**References Cited****U.S. PATENT DOCUMENTS**

8,946,683	B2	2/2015	Rogers et al.	2006/0177479 A1	8/2006	Giachelli et al.
9,057,994	B2	6/2015	Rogers et al.	2006/0178655 A1	8/2006	Santini et al.
9,061,494	B2	6/2015	Rogers et al.	2006/0244105 A1	11/2006	Forbes et al.
9,105,555	B2	8/2015	Rogers et al.	2006/0255341 A1	11/2006	Pinnington et al.
9,105,782	B2	8/2015	Rogers et al.	2006/0273279 A1	12/2006	Kaplan et al.
9,117,940	B2	8/2015	Rogers et al.	2006/0279191 A1	12/2006	Gehegan et al.
9,324,733	B2	4/2016	Rogers et al.	2006/0286488 A1	12/2006	Rogers et al.
9,349,900	B2	5/2016	Rogers et al.	2006/0286785 A1	12/2006	Rogers et al.
2001/0003043	A1	6/2001	Metspalu et al.	2007/0009968 A1	1/2007	Cunningham et al.
2002/0021445	A1	2/2002	Boxhevolnyi et al.	2007/0031607 A1	2/2007	Dubson et al.
2002/0064032	A1*	5/2002	Oohata .....	2007/0032089 A1	2/2007	Nuzzo et al.
			H04N 9/30	2007/0043416 A1	2/2007	Callas et al.
			361/760	2007/0058254 A1	3/2007	Kim
2002/0094701	A1	7/2002	Biegelsen et al.	2007/0073130 A1	3/2007	Finch et al.
2002/0110766	A1	8/2002	Tsai et al.	2007/0166954 A1	7/2007	Yamazaki et al.
2002/0182874	A1	12/2002	Wang et al.	2007/0187862 A1	8/2007	Kaplan et al.
2003/0006527	A1	1/2003	Jacobs et al.	2007/0212730 A1	9/2007	Vepari et al.
2003/0032892	A1	2/2003	Erlach et al.	2007/0227586 A1	10/2007	Zapalac
2003/0047732	A1	3/2003	Yamazaki et al.	2007/0233208 A1	10/2007	Kurtz et al.
2003/0082889	A1	5/2003	Maruyama et al.	2008/0000871 A1	1/2008	Suh et al.
2003/0087476	A1	5/2003	Oohata et al.	2008/0038236 A1	2/2008	Gimble et al.
2003/0138704	A1	7/2003	Mei et al.	2008/0041617 A1	2/2008	Chen et al.
2003/0149456	A1	8/2003	Rottenberg et al.	2008/0055581 A1	3/2008	Rogers et al.
2003/0157795	A1	8/2003	Chung et al.	2008/0085272 A1	4/2008	Kaplan et al.
2003/0178316	A1	9/2003	Jacobs et al.	2008/009322 A1	4/2008	Mech et al.
2003/0209713	A1	11/2003	Kimura et al.	2008/0102096 A1	5/2008	Molin et al.
2003/0222282	A1	12/2003	Fjelstad et al.	2008/0108171 A1	5/2008	Rogers et al.
2003/0227116	A1	12/2003	Halik et al.	2008/0152281 A1	6/2008	Lundquist et al.
2004/0005723	A1	1/2004	Empedocles et al.	2008/0157235 A1	7/2008	Rogers et al.
2004/0026684	A1	2/2004	Empedocles et al.	2008/0183076 A1	7/2008	Witte et al.
2004/0029317	A1	2/2004	Tokushige et al.	2008/0203431 A1	8/2008	Garcia et al.
2004/0079464	A1	4/2004	Kumakura	2008/0212102 A1	9/2008	Nuzzo et al.
2004/0081384	A1	4/2004	Datesman et al.	2008/0239755 A1	10/2008	Parker et al.
2004/0095658	A1	5/2004	Buretea et al.	2008/0280360 A1	11/2008	Kaplan et al.
2004/0112964	A1	6/2004	Empedocles et al.	2008/0288037 A1	11/2008	Neysmith et al.
2004/0136866	A1	7/2004	Pontis et al.	2008/0293919 A1	11/2008	Kaplan et al.
2004/0146560	A1	7/2004	Whiteford et al.	2009/0004737 A1	1/2009	Borenstein et al.
2004/0155290	A1	8/2004	Mech et al.	2009/0028910 A1	1/2009	Desimone et al.
2004/0178390	A1	9/2004	Whiteford	2009/0149930 A1	6/2009	Scheenk
2004/0192062	A1	9/2004	Mikelson	2009/0198293 A1	8/2009	Caulier et al.
2004/0192082	A1	9/2004	Wagner et al.	2009/0199960 A1	8/2009	Nuzzo et al.
2004/0200734	A1	10/2004	Co et al.	2009/0202614 A1	8/2009	Kaplan et al.
2004/0206448	A1	10/2004	Dubrow	2009/0208555 A1	8/2009	Kutler et al.
2004/0211458	A1	10/2004	Gui et al.	2009/0221896 A1	9/2009	Rickert et al.
2004/0211459	A1	10/2004	Suenaga et al.	2009/0232963 A1	9/2009	Kaplan et al.
2004/0250950	A1	12/2004	Dubrow	2009/0234026 A1	9/2009	Kaplan et al.
2004/0252559	A1	12/2004	Gupta	2009/0289246 A1	11/2009	Schneider et al.
2005/0020094	A1	1/2005	Forbes et al.	2009/0294803 A1	12/2009	Nuzzo et al.
2005/0038498	A1	2/2005	Dubrow et al.	2010/0002402 A1	1/2010	Rogers et al.
2005/0082526	A1	4/2005	Bedell et al.	2010/0028451 A1	2/2010	Kaplan et al.
2005/0124712	A1	6/2005	Anderson et al.	2010/0046902 A1	2/2010	Kaplan et al.
2005/0133954	A1	6/2005	Homola	2010/0052112 A1	3/2010	Rogers et al.
2005/0214962	A1	9/2005	Daniels et al.	2010/0055438 A1	3/2010	Kaplan et al.
2005/0227389	A1	10/2005	Bhattacharya et al.	2010/0059863 A1	3/2010	Rogers et al.
2005/0233504	A1*	10/2005	Doi .....	2010/0063404 A1	3/2010	Kaplan et al.
			H01L 21/6835	2010/0065784 A1	3/2010	Kaplan et al.
			438/127	2010/0068740 A1	3/2010	Kaplan et al.
2005/0233546	A1	10/2005	Oohata et al.	2010/0070068 A1	3/2010	Kaplan et al.
2005/0238967	A1	10/2005	Rogers et al.	2010/0072577 A1	3/2010	Nuzzo et al.
2005/0255686	A1	11/2005	Yamano et al.	2010/0096763 A1	4/2010	Kaplan et al.
2005/0260706	A1	11/2005	Kaplan et al.	2010/0120116 A1	5/2010	Kaplan et al.
2005/0261561	A1	11/2005	Jones et al.	2010/0121420 A1	5/2010	Fiset et al.
2006/0038182	A1	2/2006	Rogers et al.	2010/0178304 A1	7/2010	Wang et al.
2006/0048885	A1	3/2006	Constantin et al.	2010/0191328 A1	7/2010	Kaplan et al.
2006/0049485	A1	3/2006	Pan et al.	2010/0196447 A1	8/2010	Kaplan et al.
2006/0076561	A1	4/2006	Hioki et al.	2010/0200752 A1	8/2010	Lee et al.
2006/0084012	A1	4/2006	Nuzzo et al.	2010/0203226 A1	8/2010	Kaplan et al.
2006/0085976	A1	4/2006	Eldridge et al.	2010/0279112 A1	11/2010	Kaplan et al.
2006/0102525	A1	5/2006	Volkel et al.	2010/0283069 A1	11/2010	Rogers et al.
2006/0119853	A1	6/2006	Baumberg et al.	2010/0289124 A1	11/2010	Nuzzo et al.
2006/0127817	A1	6/2006	Ramanujan et al.	2010/0317132 A1	12/2010	Rogers et al.
2006/0129056	A1	6/2006	Leuthardt et al.	2011/0147715 A1	6/2011	Rogers et al.
2006/0132025	A1	6/2006	Gao et al.	2011/0170225 A1	7/2011	Rogers et al.
2006/0134893	A1	6/2006	Savage et al.	2011/0171813 A1	7/2011	Rogers et al.
2006/0159837	A1	7/2006	Kaplan et al.	2011/0187798 A1	8/2011	Rogers et al.
2006/0169989	A1	8/2006	Bhattacharya	2011/0220890 A1	9/2011	Nuzzo et al.
2006/0173364	A1	8/2006	Clancy et al.	2011/0230747 A1	9/2011	Rogers et al.
				2011/0266561 A1	11/2011	Rogers et al.
				2011/0277813 A1	11/2011	Rogers et al.

(56)	References Cited					
U.S. PATENT DOCUMENTS						
2011/0316120 A1	12/2011	Rogers et al.	JP	2003-197881	7/2003	
2012/0157804 A1	6/2012	Rogers et al.	JP	2003258211 A2	9/2003	
2012/0165759 A1	6/2012	Rogers et al.	JP	2003258211 A2	9/2003	
2012/0261551 A1	10/2012	Rogers et al.	JP	2003-289136	10/2003	
2012/0320581 A1	12/2012	Rogers et al.	JP	2003-297974	10/2003	
2012/0321785 A1	12/2012	Rogers et al.	JP	2003-324198	11/2003	
2012/0327608 A1	12/2012	Rogers et al.	JP	2003323132	11/2003	
2013/0036928 A1	2/2013	Rogers et al.	JP	2004-071874	3/2004	
2013/0041235 A1	2/2013	Rogers et al.	JP	2004-327836	11/2004	
2013/0072775 A1	3/2013	Rogers et al.	JP	2005-203762	7/2005	
2013/0100618 A1	4/2013	Rogers et al.	JP	2005-241629	9/2005	
2013/0140649 A1	6/2013	Rogers et al.	JP	2005-244132	9/2005	
2013/0333094 A1	12/2013	Rogers et al.	JP	2006-501690	1/2006	
2014/0163390 A1	6/2014	Rogers et al.	JP	2006-504450	2/2006	
2014/0191236 A1	7/2014	Nuzzo et al.	JP	2006505418	2/2006	
2014/0220422 A1	8/2014	Rogers et al.	JP	2006-186294	7/2006	
2014/0305900 A1	10/2014	Rogers et al.	JP	2007-515391	6/2007	
2014/0323968 A1	10/2014	Rogers et al.	JP	2008-502151	1/2008	
2015/0001462 A1	1/2015	Rogers et al.	JP	2008-502739	1/2008	
2015/0080695 A1	3/2015	Rogers et al.	JP	2009-527564	7/2009	
2015/0132873 A1	5/2015	Rogers et al.	JP	2010-508852	3/2010	
2015/0141767 A1	5/2015	Rogers et al.	JP	2010-509593	3/2010	
2015/0181700 A1	6/2015	Rogers et al.	JP	2010-509644	3/2010	
2015/0207012 A1	7/2015	Rogers et al.	JP	2010-509645	3/2010	
2015/0237711 A1	8/2015	Rogers et al.	JP	2010-522583	7/2010	
2015/0290938 A1	10/2015	Rogers et al.	JP	2010-529230	8/2010	
2015/0373831 A1	12/2015	Rogers et al.	KR	10-2000-0068418	11/2000	
2015/0380355 A1	12/2015	Rogers et al.	KR	10-2004-0030298	4/2001	
2016/0005700 A1	1/2016	Rogers et al.	KR	10-0345624	9/2002	
2016/0027737 A1	1/2016	Rogers et al.	KR	10-2001-0030924	4/2004	
2016/0050750 A1	2/2016	Rogers et al.	KR	10-2004-0088346	10/2004	
2016/0066789 A1	3/2016	Rogers et al.	KR	10-2008-0069553	7/2008	
2016/0072027 A1	3/2016	Rogers et al.	TW	367570	8/1999	
2016/0133843 A1	5/2016	Rogers et al.	TW	494257	7/2002	
2016/0136877 A1	5/2016	Rogers et al.	TW	200503885	2/2005	
			TW	I229780	3/2005	
			TW	200836353	9/2008	
			WO	WO 96/21245	7/1996	
			WO	WO 98/49936	11/1998	
			WO	WO 99/18612	4/1999	
			WO	WO 99/45860	9/1999	
			WO	WO 00/46854	8/2000	
			WO	WO 00/49421	8/2000	
			WO	WO 00/49658	8/2000	
CN	1454045	11/2003	WO	WO 00/55915	9/2000	
CN	101772348	7/2010	WO	WO 00/55916	9/2000	
DE	4241045 C1	5/1994	WO	WO 01/31082	5/2001	
DE	19748173	5/1999	WO	WO 01/33621	5/2001	
EP	0 277 606	8/1988	WO	WO 01/66833	9/2001	
EP	0 929 097	7/1999	WO	WO 01/97284	12/2001	
EP	1326288	7/2003	WO	WO 01/98838	12/2001	
EP	1 357 773	10/2003	WO	WO 02/27701	4/2002	
EP	1 467 224	10/2004	WO	WO 02/43032	5/2002	
EP	1 477 230	11/2004	WO	WO 02/45160	6/2002	
EP	1 498 456	1/2005	WO	WO 02/071137	9/2002	
EP	1 511 096	3/2005	WO	WO 02/073699	9/2002	
EP	1 558 444	8/2005	WO	WO 02/092778	11/2002	
EP	1 613 796	1/2006	WO	WO 02/097708	12/2002	
EP	1 773 240	4/2007	WO	WO 02/097724	12/2002	
EP	1 915 436	4/2008	WO	WO 02/099068	12/2002	
EP	1 726 329	8/2009	WO	WO 03/030194	4/2003	
EP	2 086 749	8/2009	WO	WO 03/032240	4/2003	
EP	2 101 975	9/2009	WO	WO 03/049201	6/2003	
EP	2 107 964	10/2009	WO	WO 03/063211	7/2003	
EP	2 109 634	10/2009	WO	WO 03/085700	10/2003	
EP	2 129 772	12/2009	WO	WO 03/085701	10/2003	
EP	2 206 017	7/2010	WO	WO 03/092073	11/2003	
EP	2 211 876	8/2010	WO	WO 2004/000915	12/2003	
EP	2 249 886	11/2010	WO	WO 2004/001103	12/2003	
JP	H03-220787	9/1991	WO	WO 2004/003535	1/2004	
JP	H06-118441	4/1994	WO	WO 2004/022637	3/2004	
JP	H06-504139	5/1994	WO	WO 2004/022714	3/2004	
JP	H06-163365	6/1994	WO	WO 2004/023527	3/2004	
JP	H07-504782	5/1995	WO	WO 2004/024407	3/2004	
JP	H10-125931	5/1998	WO	WO 2004/027822	4/2004	
JP	H11-026344	1/1999	WO	WO 2004/032190	4/2004	
JP	H11-026733	1/1999	WO	WO 2004/032191	4/2004	
JP	2001-332383	11/2001	WO	WO 2004/032193	4/2004	
JP	2002-092984	3/2002	WO	WO 2004/034025	4/2004	
JP	2002-217391	8/2002				
JP	2002-268585	9/2002				

(56)	References Cited				
FOREIGN PATENT DOCUMENTS					
WO	WO2004/043849	5/2004	WO	WO 2010/126640	11/2010
WO	WO 2004/062697	7/2004	WO	WO 2010/132552	11/2010
WO	WO 2004/086289	10/2004	WO	WO 2010/141133	12/2010
WO	WO 2004/094303	11/2004	WO	WO 2011/005381	1/2011
WO	WO 2004/095536	11/2004	WO	WO 2011/006133	1/2011
WO	WO 2004/100252	11/2004	WO	WO 2011/008842	1/2011
WO	WO 2004/105456	12/2004	WO	WO 2011/011347	1/2011
WO	WO 2004/107973	12/2004	WO	WO 2011/026101	3/2011
WO	WO 2005/000483	1/2005	WO	WO 2011/038401	3/2011
WO	WO 2005/005679	1/2005	WO	WO 2011/041395	4/2011
WO	WO 2005/012606	2/2005	WO	WO 2011/046652	4/2011
WO	WO 2005/015480	2/2005	WO	WO 2011/084450	7/2011
WO	WO 2005/017962	2/2005	WO	WO 2011/112931	9/2011
WO	WO 2005/022120	3/2005	WO	WO 2011/115643	9/2011
WO	WO 2005/029578	3/2005	WO	WO 2016/025430	2/2016
WO	WO 2005/033786	4/2005	WO	WO 2016/025438	2/2016
WO	WO 2005/033787	4/2005	WO	WO 2016/025468	2/2016
WO	WO 2005/054119	6/2005	WO	WO 2016/054348	4/2016
WO	WO 2005/099310	10/2005	OTHER PUBLICATIONS		
WO	WO 2005/104756	11/2005	Adachi et al (1982) "Chemical Etching of InGaAsP/InP DH Wafer," <i>J. Electrochem. Soc.</i> 129:1053-1062.		
WO	WO 2005/106934	11/2005	Adachi et al. (1983) "Chemical Etching Characteristics of (001)GaAs," <i>J. Electrochem. Soc.</i> 130:2427-2435.		
WO	WO 2005/122285	12/2005	Adrega et al. (2010) "Stretchable Gold Conductors Embedded in PDMS and Patterned by Photolithography: Fabrication and Electromechanical Characterization," <i>J. Micromech. Microeng.</i> 20:055025.		
WO	WO 2005/123114	12/2005	Ago et al. (2005) "Aligned Growth of Isolated Single-Walled Carbon Nanotubes Programmed by Atomic Arrangement of Substrate Surface," <i>Chem. Phys. Lett.</i> 408:433-438.		
WO	WO 2006/028996	3/2006	Ago et al. (2006) "Synthesis of Horizontally-Aligned Single-Walled Carbon Nanotubes with Controllable Density on Sapphire Surface and Polarized Raman Spectroscopy," <i>Chem. Phys. Lett.</i> 421:399-403.		
WO	WO 2006/042287	4/2006	Ahmed et al. (Web Release Oct. 11, 2005) "Extending the 3ω-Method to the MHz Range for Thermal Conductivity Measurements of Diamond Thin Films," <i>Diamond Pelat. Mater.</i> 15(2-3):389-393.		
WO	WO 2006/076711	7/2006	Ahn et al. (2007) "Bendable Integrated Circuits on Plastic Substrates by Use of Printed Ribbons of Single-Crystalline Silicon," <i>Appl. Phys. Lett.</i> 90:213501.		
WO	WO 2006/104069	10/2006	Ahn et al. (Dec. 15, 2006) "Heterogeneous Three-Dimensional Electronics by Use of Printed Semiconductor Nanomaterials," <i>Science</i> 314:1754-1757.		
WO	WO 2006/130558	12/2006	Ahn et al. (Jun. 2006) "High-Speed Mechanically Flexible Single-Crystal Silicon Thin-Film Transistors on Plastic Substrates," <i>IEEE Electron Dev. Lett.</i> 27(6):460-462.		
WO	WO 2006/130721	12/2006	Al-Halhouli et al. (2008) "Nanoindentation Testing of SU-8 Photoresist Mechanical Properties," <i>Microelectronic Eng.</i> 85:942-944.		
WO	WO 2007/000037	1/2007	Aliot, E. M. et al. (2009) "EHRA/HRS Expert Consensus on Catheter Ablation of Ventricular Arrhythmias: Developed in a partnership with the European Heart Rhythm Association (EHRA), a Registered Branch of the European Society of Cardiology (ESC), and the Heart Rhythm Society (HRS); in collaboration with the American College of Cardiology (ACC) and the American Heart Association (AHA)," <i>Europace</i> 11:771-817.		
WO	WO 2007/016524	2/2007	Alivisatos et al. (1996) "Semiconductor Clusters, Nanocrystals, and Quantum Dots," <i>Science</i> 271:933-937.		
WO	WO 2007/028003	3/2007	Alivisatos et al. (1998) "From Molecules to Materials: Current Trends and Future Directions," <i>Adv. Mater.</i> 10:1297-1336.		
WO	WO 2007/056183	5/2007	Allen et al. (Feb. 20, 2006) "Nanomaterial Transfer Using Hot Embossing for Flexible Electronic Devices," <i>Appl. Phys. Lett.</i> 88:083112.		
WO	WO 2007/100617	9/2007	Al-Sarawi et al. (Feb. 1998) "A Review of 3-D Packaging Technology," <i>IEEE Trans. Comp. Packag. Manufac. Technol. B</i> 21(1):2-14.		
WO	WO 2007/126412	11/2007	Altman et al. (2003) "Silk-Based Biomaterials," <i>Biomaterials</i> 24:401-416.		
WO	WO 2008/030666	3/2008	Amano et al. (Feb. 3, 1986) "Metalorganic Vapor Phase Epitaxial Growth of a High Quality GaN Film Using an AlN Buffer Layer," <i>Appl. Phys. Lett.</i> 48(5):353-355.		
WO	WO 2008/030960	3/2008			
WO	WO 2008/036837	3/2008			
WO	WO 2008/055054	5/2008			
WO	WO 2008/085904	7/2008			
WO	WO 2008/103464	8/2008			
WO	WO 2008/106485	9/2008			
WO	WO 2008/108838	9/2008			
WO	WO 2008/118133	10/2008			
WO	WO 2008/118211	10/2008			
WO	WO 2008/127401	10/2008			
WO	WO 2008/127402	10/2008			
WO	WO 2008/127403	10/2008			
WO	WO 2008/127404	10/2008			
WO	WO 2008/127405	10/2008			
WO	WO 2008/140562	11/2008			
WO	WO 2008/143635	11/2008			
WO	WO 2008/150861	12/2008			
WO	WO 2009/011709	1/2009			
WO	WO 2009/023615	2/2009			
WO	WO 2009/061823	5/2009			
WO	WO 2009/075625	6/2009			
WO	WO 2009/076088	6/2009			
WO	WO 2009/090398	7/2009			
WO	WO 2009/100280	8/2009			
WO	WO 2009/111641	9/2009			
WO	WO 2009/114115	9/2009			
WO	WO 2009/114689	9/2009			
WO	WO 2009/118678	10/2009			
WO	WO 2009/126689	10/2009			
WO	WO 2009/140588	11/2009			
WO	WO 2009/155397	12/2009			
WO	WO 2010/005707	1/2010			
WO	WO 2010/036807	4/2010			
WO	WO 2010/036992	4/2010			
WO	WO 2010/040528	4/2010			
WO	WO 2010/042798	4/2010			
WO	WO 2010/049881	5/2010			
WO	WO 2010/057142	5/2010			
WO	WO 2010/065957	6/2010			

(56)

**References Cited****OTHER PUBLICATIONS**

- Ambrosy et al. (1996) "Silicon Motherboards for Multichannel Optical Modules," *IEEE Trans. Compon. Pack. A* 19:34-40.
- Amir et al. (2000) "The Influence of Helium-Neon Irradiation on the Viability of Skin Flaps in the Rat," *Br. J. Plast. Surg.* 53:58-62.
- Amsden et al. (Nov. 9, 2009) "Spectral Analysis of Induced Color Change on Periodically Nanopatterned Silk Films," *Opt. Express* 17(23):21271-21279.
- Andersen et al. (2004) "Selecting the Signals for a Brain—Machine Interface," *Curr. Opin. Neurobiol.* 14:720-726.
- Andersson et al. (Oct. 16, 2002) "Active Matrix Displays Based on All-Organic Electrochemical Smart Pixels Printed on Paper," *Adv. Mater.* 14:1460-1464.
- Ando et al. (2004) "Self-Aligned Self-Assembly Process for Fabricating Organic Thin-Film Transistors," *Appl. Phys. Lett.* 85:1849-1851.
- Angadi et al. (Web Release Jun. 1, 2006) "Thermal Transport and Grain Boundary Conductance in Ultrananocrystalline Diamond Thin Films," *J. Appl. Phys.* 99:114301.
- Aoki et al. (2003) "Microassembly of Semiconductor Three Dimensional Photonic Crystals," *Nat. Mater.* 2:117-121.
- Arnold et al. (2003) "Field-Effect Transistors Based on Single Semiconducting Oxide Nanobelts," *J. Phys. Chem. B* 107(3):659-663.
- Ayón et al. (Jan. 1999) "Characterization of a Time Multiplexed Inductively Coupled Plasma Etcher," *J. Electrochem. Soc.* 146(1):339-349.
- Baca et al. (2008) "Semiconductor Wires and Ribbons for High-Performance Flexible Electronics," *Angew. Chem. Int. Ed.* 47:5524-5542.
- Bachtold et al. (Nov. 9, 2001) "Logic Circuits with Carbon Nanotube Transistors," *Science* 294:1317-1320.
- Bae et al. (Jul. 1, 2002) "Single-Crystalline Gallium Nitride Nanobelts," *Appl. Phys. Lett.* 81(1):126-128.
- Ball et al. (2004) "Towards an Implantable Brain-Machine Interface Based on Epicortical Field Potentials," *Biomed. Tech.* 49:756-759.
- Balmer et al. (2005) "Diffusion of Alkanethiols in PDMS and Its Implications on Microcontact Printing ( $\mu$ CP)," *Langmuir* 21(2):622-632.
- Banerjee et al. (May 2001) "3-D ICs: A Novel Chip Design for Improving Deep-Submicrometer Interconnect Performance and Systems-on-Chip Integration," *Proc. IEEE* 89(5):602-633.
- Bao et al. (1997) "High-Performance Plastic Transistors Fabricated by Printing Techniques," *Chem. Mater.* 9:1299-1301.
- Bao et al. (1999) "Printable Organic and Polymeric Semiconducting Materials and Devices," *J. Mater. Chem.* 9:1895-1904.
- Barquins, M. (1992) "Adherence, Friction and Wear of Rubber-Like Materials," *Wear* 158:87-117.
- Bates, F.S. (1991) "Polymer-Polymer Phase Behavior," *Science* 251:898-905.
- Battaglia et al. (2003) "Colloidal Two-Dimensional Systems: CdSe Quantum Shells and Wells," *Angew. Chem. Int. Ed.* 442:5035-5039.
- Bauer et al. (2004) "Biological Applications of High Aspect Ratio Nanoparticles," *J. Mater. Chem.* 14:517-526.
- Berg et al. (2003) "Tailored Micropatters Through Weak Polyelectrolyte Stamping," *Langmuir* 19:2231-2237.
- Bernard et al. (1998) "Printing Patterns of Proteins," *Langmuir* 14(9):2225-2229.
- Bett et al. (Aug. 1999) "III-V Compounds for Solar Cell Applications," *Appl. Phys. A. Mater. Sci.* 69(2):119-129.
- Bhunia et al. (2004) "Free-Standing and Vertically Aligned InP Nanowires Grown by Metalorganic Vapor Phase Epitaxy," *Physica E* 21:583-587.
- Bhushan et al. (Nov. 2004) "Multiwalled Carbon Nanotube AFM Probes for Surface Characterization of Micro/Nanostructures," *Microsyst. Technol.* 10(8-9):633-639.
- Bietsch et al. (Oct. 1, 2000) "Conformal Contact and Pattern Stability of Stamps Used for Soft Lithography," *J. Appl. Phys.* 88(7):4310-4318.
- BIOFLEX—Biocompatible Flexible Electronic Circuits. Available at <http://tfcg.elis.ugent.be/projects/bioflex>. Accessed Feb. 8, 2012.
- Bishay et al. (2000) "Temperature Coefficient of the Surface Resistivity of Two-Dimensional Island Gold Films," *J. Phys. D. Appl. Phys.* 33(18):2218-2222.
- Blanchet et al. (2003) "Large Area, High Resolution, Dry Printing of Conducting Polymers for Organic Electronics," *Appl. Phys. Lett.* 82:463-465.
- Blanchet et al. (2003) "Printing Techniques for Plastic Electronics," *J. Imag. Sci. Tech.* 47(4):296-303.
- Blazdell et al. (Nov. 1999) "Preparation of Ceramic Inks for Solid Freeforming Using a Continuous Jet Printer," *J. Mat. Syn. Process.* 7(6):349-356.
- Boltau et al. (1998) "Surface-Induced Structure Formation of Polymer Blends on Patterned Substrates," *Nature* 391:877-879.
- Boncheva et al. (Mar. 15, 2005) "Magnetic Self-Assembly of Three-Dimensional Surfaces from Planar Sheets," *Proc. Natl. Acad. Sci. USA* 102(11):3924-3929.
- Boncheva et al. (Mar. 8, 2005) "Templated Self-Assembly: Formation of Folded Structures by Relaxation of Pre-Stressed, Planar Tapes. The Path to Ubiquitous and Low-cost Organic Electronic Appliances on Plastic," *Adv. Mater.* 17(5):553-557.
- Bourzac, K. (May/Jun. 2010) "TR10: Implantable Electronics," *Technology Review*, Published by MIT, <http://www.technologyreview.com/biomedicine/25086/?a=f>.
- Bowden et al. (1997) "Self Assembly of Mesoscale Objects into Ordered Two-Dimensional Arrays," *Science* 276:233-235.
- Bowden et al. (1998) "Spontaneous Formation of Ordered Structures in Thin Films of Metals Supported on an Elastomeric Polymer," *Nature* 393:146-149.
- Bowden et al. (2001) "Molecule-Mimetic Chemistry and Mesoscale Self-Assembly," *Acc. Chem. Res.* 34:231-238.
- Bracher et al. (2009) "Shaped Films of Ionotropic Hydrogels Fabricated Using Templates of Patterns Paper," *Adv. Mater.* 21:445-450.
- Bradley et al. (2003) "Flexible Nanotube Electronics," *Nano Lett.*, vol. 3, No. 10, pp. 1353-1355.
- Braun et al. (1999) "Electrochemically Grown Photonic Crystals," *Nature* 402:603-604.
- Britton et al. (Web Release Oct. 25, 2005) "Microstructural Defect Characterization of a Si:H Deposited by Low Temperature HW-CVD on Paper Substrates," *Thin Solid Films* 501(1-2):79-83.
- Brown et al. (2005) "Evaluation of Polydimethylsiloxane Scaffolds with Physiologically-Relevant Elastic Moduli: Interplay of Substrate Mechanics and Surface Chemistry Effects on Vascular Smooth Muscle Cell Response," *Biomaterials* 26:3123-3129.
- Brown et al. (Dec. 19, 2001) "Heterogeneous Materials Integration: Compliant Substrates to Active Device and Materials Packaging," *Mater. Sci. Eng. B* 87(3):317-322.
- Brown, H.R. (1991) "The Adhesion Between Polymers," *Ann. Rev. Mater. Sci.* 21:463-489.
- Bruschi et al. (2001) "Micromachined Silicon Suspended Wires With Submicrometric Dimensions," *Microelectron. Eng.* 57-58:959-965.
- Buma et al. (2001) "High-Frequency Ultrasound Array Element Using Thermoelastic Expansion in an Elastomeric Film," *Appl. Phys. Lett.* 79:548-550.
- Burdinski et al. (2005) "Single Etch Patterning of Stacked Silver and Molybdenum Alloy Layers on Glass Using Microcontact Wave Printing," *J. Am. Chem. Soc.* 127(31):10786-10787.
- Burdinski, D. (non-dated) "Soft Lithography and Microcontact Wave Printing," [http://www.research.philips.com/technologies/light\\_dev\\_microsys/softlitho/index.html](http://www.research.philips.com/technologies/light_dev_microsys/softlitho/index.html), Downloaded May 23, 2007.
- Burge et al. (Jun. 25, 1997) "X-Ray Holography for VLSI Using Synthetic Bilevel Holograms," *Proc. Int. Soc. Opt. Eng.* 3183:2-13.
- Burgin et al. (2000) "Large Area Submicrometer Contact Printing Using a Contact Aligner," *Langmuir* 16:5371-5375.
- Burns et al. (2003) "Printing of Polymer Thin-Film Transistors for Active-Matrix-Display Applications," *J. Soc. Inf. Display* 11:599-604.
- Campbell et al. (2000) "Fabrication of Photonic Crystals for the Visible Spectrum by Holographic Lithography," *Nature* 404:53-56.

(56)

**References Cited****OTHER PUBLICATIONS**

- Cao et al. (2006) "Bilayer Organic-Inorganic Gate Dielectrics for High-Performance, Low-Voltage, Single-Walled Carbon Nanotube Thin-Film Transistors, Complementary Logic Gates, and p-n Diodes on Plastic Substrates," *Adv. Funct. Mater.* 16:2355-2362.
- Cao et al. (2006) "Highly Bendable, Transparent Thin-Film Transistors That Use Carbon-Nanotube-Based Conductors and Semiconductors with Elastomeric Dielectrics," *Adv. Mater.* 18(3):304-309.
- Cao et al. (2006) "Transparent flexible organic thin-film transistors that use printed single-walled carbon nanotube electrodes," *Applied Physics Letters* 88:113511.
- Cao et al. (Jan. 5, 2009) "Ultrathin Films of Single-Walled Carbon Nanotubes for Electronics and Sensors: A Review of Fundamental and Applied Aspects," *Adv. Mater.* 21(1):29-53.
- Cao et al. (Jul. 24, 2008) "Medium-Scale Carbon Nanotube Thin-Film Integrated Circuits on Flexible Plastic Substrates," *Nature* 454:495-500.
- Carr et al. (1998) "Measurement of Nanomechanical Resonant Structures in Single-Crystal Silicon," *J. Vac. Sci. Technol. B* 16:3821-3824.
- Chang et al. (1994) "Process Techniques," "Lithography," and "Device-Related Physics and Principles," In; *GaAs High-Speed Devices: Physics, Technology and Circuit Application*, John Wiley and Sons, New York, pp. 115-278.
- Chaudhury et al. (1991) "Direct Measurement of Interfacial Interactions Between Semispherical Lenses and Flat Sheets of Poly(dimethylsiloxane) and their Chemical Derivatives," *Langmuir* 7:1013-1025.
- Chen et al. (2003) "Characterization of Pd-GaAs Schottky Diodes Prepared by the Electrodes Plating Technique," *Semiconductor. Sci. Technol.* 18:620-626.
- Chen et al. (2003) "Electronic Paper: Flexible Active-Matrix Electronics Ink Display," *Nature* 423:136.
- Chen et al. (2005) "InGaN Nanorings and Nanodots by Selective Area Epitaxy," *Appl. Phys. Lett.* 87:143111.
- Chen et al. (2005) "The Role of Metal-Nanotube Contact in the Performance of Carbon Nanotube Field-Effect Transistors," *Nano Lett.* 5(7):1497-1502.
- Chen et al. (Feb. 27, 2006) "Complementary Carbon Nanotube-Gated Carbon Nanotube Thin-Film Transistor," *Appl. Phys. Lett.* 88:093502.
- Chen et al. (Jun. 2002) Effect of Process Parameters on the Surface Morphology and Mechanical Performance of Silicon Structures After Deep Reactive Ion Etching (DRIE) *J. Microelectromech. Syst.* 11(3):264-275.
- Chen et al. (Mar. 2004) "A Family of Herringbone Patterns in Thin Films," *Scr. Mater.* 50(6):797-801.
- Chen et al. (Mar. 24, 2006) "An Integrated Logic Circuit Assembled on a Single Carbon Nanotube," *Science* 311:1735.
- Chen et al. (Sep. 2004) "Herringbone Buckling Patterns of Compressed Thin Films on Compliant Substrates," *J. Appl. Mech.* 71:597-603.
- Cheng et al. (2005) "Ink-Jet Printing, Self-Assembled Polyelectrolytes, and Electroless Plating: Low Cost Fabrication of Circuits on a Flexible Substrate at Room Temperature," *Macromol. Rapid Commun.* 26:247-264.
- Childs et al. (2002) "Decal Transfer Microlithography: A New Soft-Lithographic Patterning Method," *J. Am. Chem. Soc.* 124:13583-13596.
- Childs et al. (2005) "Masterless Soft-Lithography: Patterning UV/Ozone-Induced Adhesion on Poly(dimethylsiloxane) Surfaces," *Langmuir* 21:10096-10105.
- Childs et al. (Aug. 14, 2004) "Patterning of Thin-Film Microstructures on Non-Planar Substrate Surfaces Using Decal Transfer Lithography," *Adv. Mater.* 16(15):1323-1327.
- Choi et al. (2007) "Biaxially Stretchable 'Wavy' Silicon Nanomembranes," *Nano Lett.* 7(6):1655-1663.
- Choi et al. (Web Release Jan. 25, 2005) "Simple Detachment Patterning of Organic Layers and Its Applications to Organic Light-Emitting Diodes," *Adv. Mater.* 17(2):166-171.
- Chou et al. (2004) "An Orientation-Controlled Pentacene Film Aligned by Photoaligned Polyimide for Organic Thin-Film Transistor Applications," *Adv. Func. Mater.* 14:811-815.
- Chou et al. (Jun. 8, 1999) "Micromachining on (111)-Oriented Silicon," *Sens. Actuators A* 75(3):271-277.
- Chu et al. (2005) "High-Performance Organic Thin-Film Transistors with Metal Oxide/Metal Bilayer Electrode," *Appl. Phys. Lett.* 87:193508.
- Chung et al. (2000) Silicon Nanowire Devices *Appl. Phys. Lett.* 76(15):2068-2070.
- Chung et al. (Jul. 1, 2003) "A Study on Formation of Al and Al<sub>2</sub>O<sub>3</sub> on the Porous Paper by DC Magnetron Sputtering," *Surf. Coat. Technol.* 171(1-3):65-70.
- Clerc, L. (1976) "Directional Differences of Impulse Spread in Trabecular Muscle from Mammalian Heart," *J. Physiol.* 255:335-346.
- Cohen-Karni et al. (2009) "Flexible Electrical Recording from Cells Using Nanowire Transistor Arrays," *Proc. Natl. Acad. Sci. USA* 106:7309-7313.
- Cole et al. (2008) "Patterned Growth and Transfer of ZnO Micro- and Nanocrystals with Size and Location Control," *Adv. Mater.* 20:1474-1478.
- Collins et al. (Apr. 27, 2001) "Engineering Carbon Nanotubes and Nanotube Circuits Using Electrical Breakdown," *Science* 292:706-709.
- Corazza et al. (2007) "Photobiomodulation on the Angiogenesis of Skin Wounds in Rats Using Different Light Sources," *Photomedicine Laser Surg.* 25:102-106.
- Cox, H. L. (1952) "The Elasticity and Strength of Paper and Other Fibrous Materials," *Br. J. Appl. Phys.* 3:72-79.
- Creagh et al. (2003) "Design and Performance of Inkjet Print Heads for Non-Graphic-Arts Applications," *MRS Bull.* 28:807-811.
- Crone et al. (Feb. 3, 2000) "Large-Scale Complementary Integrated Circuits Based on Organic Transistors," *Nature* 403:521-523.
- Crowder et al. (1998) "Low-Temperature Single-Crystal Si TFTs Fabricated on Si Films Processed via Sequential Lateral Solidification," *IEEE Electron. Dev. Lett.* 19:306-308.
- Cui et al. (2001) "Nanowire Nanosensors for Highly Sensitive and Selective Detection of Biological and Chemical Species," *Science* 293:1289-1292.
- Dai et al. (2002) "Gallium Oxide Nanoribbons and Nanosheets," *J. Phys. Chem. B* 106(5):902-904.
- Dai et al. (2003) "Novel Nanostructures of Functional Oxides Synthesized by Thermal Evaporation," *Adv. Funct. Mater.* 13:9-24.
- Davidson et al. (2004) "Supercritical Fluid-Liquid-Solid Synthesis of Gallium Arsenide Nanowires Seeded by Alkanethiol-Stabilized Gold Nanocrystals," *Adv. Mater.* 16:646-649.
- de Gans (2004) "Inkjet Printing of Polymers: State of the Art and Future Developments," *Adv. Mater.* 16(3):203-213.
- De Sio et al. (Web Release May 18, 2005) "Electro-Optical Response of a Single-Crystal Diamond Ultraviolet Photoconductor in Transverse Configuration," *Appl. Phys. Lett.* 86:213504.
- DeBoer et al. (2004) "Organic Single-Crystal Field-Effect Transistors," *Phys. Stat. Sol.* 201:1302-1331.
- Decision dated Jun. 16, 2014, corresponding to Indian Patent Application No. 1366/del/2006.
- Decision of Refusal corresponding to Japanese Patent Application No. P2009-527564, Dispatched Jan. 29, 2013—Japanese language with English translation.
- Decision of Refusal corresponding to Japanese Patent Application No. P2007-515549, Dispatched Sep. 4, 2012—English translation.
- Decision of Rejection corresponding to Korean Patent Application No. 10-2007-7000216, Issued Sep. 19, 2012—includes English translation.
- Decision of Rejection corresponding to Korean Patent Application No. 10-2006-0053675, dated Jul. 30, 2013.
- Decision of Rejection dated Nov. 10, 2014, corresponding to Korean Patent Application No. 10-2013-0131753.

(56)

**References Cited**

## OTHER PUBLICATIONS

- Deen et al. (2004) "Electrical Characterization of Polymer-Based FETs Fabricated by Spin-Coating Poly(3-alkylthiophene)s," *IEEE Trans. Electron Devices* 51:1892-1901.
- Delmerche et al. (1997) "Stability of Molded Polydimethylsiloxane Microstructures," *Adv. Mat.* 9:741-746.
- Deruelle et al. (1995) "Adhesion at the Solid-Elastomer Interface: Influence of Interfacial Chains," *Macromol.* 28:7419-7428.
- Derycke et al. (Sep. 2001) "Carbon Nanotube Inter—and Intramolecular Logic Gates," *Nano Lett.* 1(9):453-456.
- Desai et al. (Feb. 1999) "Nanopore Technology for Biomedical Applications," *Biomed. Microdevices* 2(1):11-40.
- Dick et al. (Jun. 2004) "Synthesis of Branched 'Nanotrees' by Controlled Seeding of Multiples Branching Events," *Nat. Mater.* 3:380-384.
- Dimroth et al. (Mar. 2007) "High Efficiency Multijunction Solar Cells," *MRS Bull.* 32:230-235.
- Ding et al. (Oct. 4, 2004) "Self Catalysis and Phase Transformation in the Formation of CdSe Nanosaws," *Adv. Mater.* 16(19):1740-1743.
- Dinsmore et al. (2002) "Colloidosomes: Selectively Permeable Capsules Composed of Colloidal Particles," *Science* 298:1006-1009.
- Divlansky et al. (2003) "Fabrication of Three-Dimensional Polymer Photonic Crystal Structures Using Single Diffraction Element Interference Lithography," *Appl. Phys. Lett.* 82(11):1667-1669.
- Dodabalapur A. (Apr. 2006) "Organic and Polymer Transistors for Electronics," *Mater Today* 9(4):24-30.
- Dodabalapur et al. (1995) "Organic Transistors: Two-Dimensional Transport and Improved Electrical Characteristics," *Science* 268:270-271.
- Duan et al. (2000) "General Synthesis of Compound Semiconductor Nanowires," *Adv. Mater.* 12:298-302.
- Duan et al. (2003) "High-performance Thin-Film Transistors Using Semiconductor Nanowires and Nanoribbons," *Nature* 425:274-278.
- Duan X. (2003) "Semiconductor Nanowires: From Nanoelectronics to Macroelectronics," Abstract from a presentation given at the 11<sup>th</sup> Foresight Conference on Molecular Nanotechnology, Oct. 10-20, Burlingame, CA.
- Duboz et al. (1998) "Transistors and Detectors Based on GaN-Related Materials," In: *Group III Nitride Semiconductor Compounds*, Gill, B. ed., Clarendon, Oxford, pp. 343-387.
- Duesberg et al. (2000) "Polarized Raman Spectroscopy on Isolated Single-Wall Carbon Nanotubes," *Phys. Rev. Lett.*, vol. 85, No. 25, pp. 5436-5439.
- Duffy et al. (1998) "Rapid Prototyping of Microfluidic Systems in Poly(dimethylsiloxane)," *Anal. Chem.* 70:4974-4984.
- Dupuis et al. (2008) "History, Development, and Applications of High-Brightness Visible Light-Emitting Diodes," *IEEE J. Lightwave Tech.* 26:1154-1171.
- Durkop et al. (2004) "Extraordinary Mobility in Semiconducting Carbon Nanotube," *Nano Lett.* 4(1):35-39.
- Eder et al. (Apr. 5, 2004) "Organic Electronics on Paper," *Appl. Phys. Lett.* 84(14):2673-2675.
- Edrington et al. (2001) "Polymer-Based Photonic Crystals," *Adv. Mater.* 13:421-425.
- Efimenko et al. (Oct. 15, 2002) "Surface Modification of Sylgard-184 Poly(dimethyl Siloxane) Networks by Ultraviolet and Ultra-violet/Ozone Treatment," *J. Colloid Interface Sci.* 254(2):306-315.
- Eftekhari, G. (1993) "Variation in the Effective Richardson Constant of Metal—GaAs and Metal—InP Contacta Due to the Effect of Processing Parameters," *Phys. Status Solid A-Appl. Res.* 140:189-194.
- English Translation of Notice of Reasons for Rejection issued for Japanese Patent Application No. P2007-515549, issued Dec. 20, 2011.
- Ensell, G. (1995) "Free Standing Single-Crystal Silicon Microstructures," *J. Micromech. Microeng.* 5:1-4.
- Exam Report, Written Opinion and Response to Written Opinion, Corresponding to Singapore Patent Application No. 2007/18082-1, Mailed Beginning Aug. 26, 2009.
- Examination Report and Response, Corresponding to Malaysian Patent Application No. PI 20062672, Mailed Aug. 28, 2009.
- Examination Report corresponding to European Patent Application No. 05 755 193.9, dated Jul. 7, 2011.
- Examination Report corresponding to Indian Patent Application No. 1366/DEL/2006, dated Jun. 10, 2011.
- Examination Report dated Sep. 3, 2014, for corresponding European Patent Application No. 05755193.9.
- Examination Report, Corresponding to European Application No. EP 05 756 327.2, Dated Jan. 20, 2010.
- Examination Report, Corresponding to European Patent Application No. 07841968.6, dated Apr. 27, 2012.
- Examination Report, Corresponding to Malaysian Patent Application No. PI 20092343, Mailed Jun. 15, 2010.
- Examination Report, Corresponding to Singapore Patent Application No. 200608359-6, Completed on Aug. 27, 2008.
- Examination Report, Response and Search Report, Corresponding to Malaysian Patent Application No. PI 20062537, Nov. 20, 2009.
- Examination Report, Written Opinion and Response, Corresponding to Singapore Patent Application No. 2007/18082-1, Mailed beginning Feb. 26, 2009.
- Extended European Search Report dated Jan. 16, 2015, corresponding to European Patent Application No. 13003427.5.
- Extended European Search Report dated Sep. 2, 2014, for corresponding European Patent Application No. 13003426.7.
- Extended European Search Report dated Sep. 4, 2014, for corresponding European Patent Application No. 13003428.3.
- Faez et al. (1999) "An Elastomeric Conductor Based on Polyaniline Prepared by Mechanical Mixing," *Polymer* 40:5497-5503.
- Feigner et al. (1996) "Flexural Rigidity of Microtubules Measured with the Use of Optical Tweezers," *J. Cell Sci.* 109:509-516.
- Fink et al. (1999) "Block Copolymers as Photonic Bandgap Materials," *J. Lightwave Tech.* 17:1963-1969.
- First Examination Report dated Nov. 8, 2013 for corresponding Indian Patent Application No. 7581/DELNP/2006.
- First Office Action issued Apr. 30, 2014, for corresponding Chinese Patent Application No. 2012101571627.
- First Office Action, Corresponding to Chinese Patent Application No. 201110077508.8, issued Feb. 17, 2012.
- Flewitt et al. (2005) "Low-Temperature Deposition of Hydrogenated Amorphous Silicon in an Electron Cyclotron Resonance Reactor for Flexible Displays," *Proc. IEEE* 93:1364-1373.
- Folch et al. (1999) "Wafer-Level In-Registry Microstamping," *J. Microelectromech. Syst.* 8:85-89.
- Forment et al. (2004) "Influence of Hydrogen Treatment and Annealing Processes Upon the Schottky Barrier Height of Au/n-GaAs and Ti/n-GaAs Diodes," *Semicond. Sci. Technol.* 19:1391-1396.
- Forrest et al. (2004) "The Path to Ubiquitous and Low-Cost Organic Electronic Appliances on Plastic," *Nature* 428:911-918.
- Fortunato et al. (2005) "Flexible a-Si: H Position-Sensitive Detectors," *Proc. IEEE* 93:1281-1286.
- Fortunato et al. (Sep. 2008) "High-Performance Flexible Hybrid Field-Effect Transistors Based on Cellulose Fiber Paper," *IEEE Electron. Dev. Lett.* 29(9):988-990.
- Freeman et al. (2000) "Spatial Spectral Analysis of Human Electrocardiograms Including the Alpha and Gamma Bands," *J. Neurosci. Methods* 95:111-121.
- Freire et al. (1999) "Thermal Stability of Polyethylene Terephthalate (PET): Oligomer Distribution and Formation of Volatiles," *Packag. Technol. Sci.* 12:29-36.
- Freund, L.B. (2000) "The Mechanics of Electronic Materials," *Int. J. Solids Struct.* 37:185-196.
- Friedman et al. (2005) "Nanotechnology: High-Speed Integrated Nanowire Circuits," *Nature* 434:1085.
- Fu et al. (Jan. 10, 2003) "Patterning of Diamond Microstructures on Si Substrate by Bulk and Surface Micromachining," *J. Mater. Process. Technol.* 132(1-3):73-81.

(56)

**References Cited****OTHER PUBLICATIONS**

- Furneaux et al. (1989) "The Formation of Controlled-Porosity Membranes from Anodically Oxidized Aluminum," *Nature* 337:147-149.
- Gan et al. (2002) "Preparation of Thin-Film Transistors With Chemical Bath Deposited CdSe and CdS Thin Films" *IEEE Trans. Electron. Dev.* 49:15-18.
- Gao et al. (Sep. 9, 2005) "Conversion of Zinc Oxide Nanobelts into Superlattice-Structures Structures Nanohelices," *Science* 309:1700-1704.
- Garcia et al. (2004) "Etchant Anisotropy Controls the Step Bunching Instability in KOH Etching of Silicon," *Phys. Rev. Lett.* 93(16):166102.
- Gardner et al. (1965) "Physical Aspects of the Internal Water Relations of Plant Leaves," *Plant Physiol.* 40:705-710.
- Garnier et al. (1994) "All-Polymer Field-Effect Transistor Realized by Printing Techniques," *Science* 265:1684-1686.
- Geim et al. (Mar. 2007) "The Rise of Graphene," *Nature Mater.* 6:183-191.
- Geissler et al. (2003) "Fabrication of Metal Nanowires Using Microcontact Printing," *Langmuir* 19(15):6301-6311.
- Geissler et al. (Jun. 2003) "Selective Wet-Etching of Microcontact-Printed Cu Substrates with Control Over the Etch Profile," *Microelec. Eng.* 67-68:326-332.
- Gelinck et al. (2000) "High-Performance All-Polymer Integrated Circuits," *Appl. Phys. Lett.* 77:1487-1489.
- Gelinck et al. (2004) "Flexible Active-Matrix Displays and Shift Registers Based on Solution-Processed Organic Transistors," *Nat. Mater.* 3:106-110.
- Georgakilas et al. (2002) "Wafer-Scale Integration of GaAs Optoelectronic Devices with Standard Si Integrated Circuits Using a Low-Temperature Bonding Procedure," *Appl. Phys. Lett.* 81:5099-5101.
- Givargizov, E.I. (1991) "Applications," In; *Oriented Crystallization on Amorphous Substrates*, Plenum Press, New York, pp. 341-363.
- Goetting et al. (1999) "Microcontact Printing of Alkanephosphonic Acids on Aluminum: Pattern Transfer by Wet Chemical Etching," *Langmuir* 15:1182-1191.
- Goldman et al. (1996) "Correlation of Buffer Strain Relaxation Modes with Transport Properties of Two-Dimensional Electron Gases," *J. Appl. Phys.* 80:6849-6854.
- Goldmann et al. (2004) "Hole Mobility in Organic Single Crystals Measured by a "Flip-Crystal" Field-Effect Technique," *J. Appl. Phys.* 96:2080-2086.
- Goldsmith, T.H. (Sep. 1990) "Optimization, Constraint, and History in the Evolution of Eyes," *Quart. Rev. Biol.* 65(3):281-322.
- Gratz et al. (1991) "Atomic Force Microscopy of Atomic-Scale Ledges and Etch Pits Formed During Dissolution of Quartz," *Science*, 251:1343-1346.
- Gray et al. (Dec. 2001) "Screen Printed Organic Thin Film Transistors (OTFTs) on a Flexible Substrate," *Proc. SPIE* 4466:89-94.
- Gray et al. (Mar. 5, 2004) "High-Conductivity Elastomeric Electronics," *Adv. Mater.* 16(5):393-397.
- Grayson, T. (2002) "Curved Focal Plane Wide Field of View Telescope Design," *Proc. SPIE* 4849:269-274.
- Gruen et al. (Mar. 21, 1994) "Fullerenes as Precursors for Diamond Film Growth Without Hydrogen or Oxygen Additions," *Appl. Phys. Lett.* 65(12):1502-1504.
- Gudiksen et al. (Web Release Apr. 18, 2001) "Synthetic Control of the Diameter and Length of Single Crystal Semiconductor Nanowires," *J. Phys. Chem. B* 105:4062-4064.
- Guo et al. (Aug. 19, 2002) "Metal-Insulator-Semiconductor Electrostatics of Carbon Nanotubes," *Appl. Phys. Lett.* 81(8):1486-1488.
- Gur et al. (2005) "Air-Stable All-Inorganic Nanocrystal Solar Cells Processed from Solution," *Science* 310:462-465.
- Gurbuz et al. (Jul. 2005) "Diamond Semiconductor Technology for RF Device Applications," *Solid State Electron.* 49(7):1055-1070.
- Haisma et al. (2002) "Contact Bonding, Including Direct-Bonding in a Historical and Recent Context of Materials Science and Technology, Physics and Chemistry," *Mater. Sci Eng.* 37:1-60.
- Halik et al. (2004) "Low-Voltage Organic Transistors with an Amorphous Molecular Gate Dielectric," *Nature* 431:963-966.
- Hamed et al. (May 2007) "Towards Woven Logic from Organic Electronic Fibres," *Nat. Mater.* 6:357-362.
- Hamilton et al. (2004) "Field-Effect Mobility of Organic Polymer Thin-Film Transistors," *Chem. Mater.* 16:4699-4704.
- Han et al. (2005) "Template-Free Directional Growth of Single-Walled Carbon Nanotubes on a-and r-Plane Sapphire," *J. Am. Chem. Soc.* 127:5294-5295.
- Harada et al. (2001) "Catalytic Amplification of the Soft Lithographic Patterning of Si. Nonelectrochemical Orthogonal Fabrication of Photoluminescent Porous Si Pixel Arrays," *J. Am. Chem. Soc.* 123:8709-8717.
- Harkonen et al. (Jun. 8, 2006) "4 W Single-Transverse Mode VECSEL Utilizing Intra-Cavity Diamond Heat Spreader," *Electron Lett.* 42(12):693-694.
- Hayase et al. (2001) "Photoangioplasty with Local Motexafin Lutetium Delivery Reduces Macrophages in a Rabbit Post-Balloon Injury Model," *Cardiovascular Res.* 49:449-455.
- He et al. (2005) "Si Nanowire Bridges in Microtrenches: Integration of Growth into Device Fabrication," *Adv. Mater.* 17:2098-2102.
- Heffelfinger et al. (1997) "Steps and the structure of the (0001)  $\alpha$ -alumina surface," *Surf. Sci.*, 370:L168-L172.
- Hillborg et al. (Web Release Dec. 30, 2003) "Nanoscale Hydrophobic Recovery: A Chemical Force Microscopy Study of UV/Ozone-Treated Cross-Linker Poly(dimethylsiloxane)," *Langmuir* 20(3):785-794.
- Hines et al. (2005) "Nanotransfer Printing of Organic and Carbon Nanotube Thin-Film Transistors on Plastic Substrates," *Appl. Phys. Lett.* 86:163101.
- Hollenberg et al. (2006) "A MEMS Fabricated Flexible Electrode Array for Recording Surface Field Potentials," *J. Neurosci. Methods* 153:147-153.
- Holmes et al. (Feb. 25, 2000) "Control of Thickness and Orientation of Solution-Grown Silicon Nanowires," *Science* 287:1471-1473.
- Horan et al. (Jun. 2005) "In Vitro Degradation of Silk Fibroin," *Biomaterials* 26(17):3385-3393.
- Horn et al. (1992) "Contact Electrification and Adhesion Between Dissimilar Materials," *Science* 256:362-364.
- Hoyer, P. (1996) "Semiconductor Nanotube Formation by a Two-Step Template Process," *Adv. Mater.* 8:857-859.
- Hsia et al. (2005) "Collapse of Stamps for Soft Lithography Due to Interfacial Adhesion," *Appl. Phys. Lett.* 86:154106.
- Hsu et al. (2002) "Amorphous Si TFTs on Plastically Deformed Spherical Domes," *J. Non-Crystalline Solids* 299-302:1355-1359.
- Hsu et al. (2003) "Nature of Electrical Contacts in a Metal—Molecule—Semiconductor System," *J. Vac. Sci. Technol. B* 21(4):1928-1935.
- Hsu et al. (Jan. 15, 2004) "Spherical Deformation of Compliant Substrates with Semiconductor Device Islands," *J. Appl. Phys.* 95(2):705-712.
- Hsu et al. (Mar. 2004) "Effects of Mechanical Strain on TFT's on Spherical Domes," *IEEE Trans. Electron Dev.* 51(3):371-377.
- Hu et al. (1997) "Using Soft Lithography to Fabricate GaAs/AIGaAs Heterostructure Field Effect Transistors," *Appl. Phys. Lett.* 71:2020-2022.
- Hu et al. (1999) "Chemistry and Physics in One Dimension: Synthesis and Properties of Nanowires and Nanotubes," *Acc. Chem. Res.* 32:435-445.
- Hu et al. (2004) "Percolation in Transparent and Conducting Carbon Nanotube Networks," *Nano Lett.*, vol. 4, No. 12, pp. 2513-2517.
- Hu et al. (2009) "Highly Conductive Paper for Energy-Storage Devices," *Proc. Natl. Acad. Sci. USA* 106:21490-21494.
- Hu et al. (2010) "Stretchable, Porous, and Conductive Energy Textiles," *Nano Lett.* 10:708-714.
- Huang et al. (2001) "Directed Assembly of One-Dimensional Nanostructures into Functional Networks," *Science* 291:630-633.
- Huang et al. (2001) "Room-Temperature Ultraviolet Nanowire Nanolasers," *Science* 292:1897-1899.
- Huang et al. (2003) "Growth of Millimeter-Long and Horizontally Aligned Single-Walled Carbon Nanotubes on Flat Substrates," *J. Am. Chem. Soc.*, 125:5636-5637.

(56)

**References Cited****OTHER PUBLICATIONS**

- Huang et al. (2004) "Long and Oriented Single-Walled Carbon Nanotubes Grown by Ethanol Chemical Vapor Deposition," *J. Phys. Chem. B.* 108:16451-16456.
- Huang et al. (2004) "Self-Organizing High-Density Single-Walled Carbon Nanotube Arrays from Surfactant Suspensions," *Nanotechnol.* 15:1450-1454.
- Huang et al. (2005) "Nanomechanical Architecture of Strained Bilayer Thin Films: From Design Principles to Experimental Fabrication," *Adv. Mater.* 17(23):2860-2864.
- Huang et al. (2005) "Nanowires for Integrated Multicolor Nanophotonics," *Small* 1(1):142-147.
- Huang et al. (2005) "Nonlinear Analyses of Wrinkles in a Film Bonded to a Compliant Substrate," *J. Mech. Phys. Solids* 53:2101-2118.
- Huang et al. (2005) "Stamp Collapse in Soft Lithography," *Langmuir* 21:8058-8068.
- Huang et al. (Jan. 16, 2001) "Catalytic Growth of Zinc Oxide Nanowires by Vapor Transport," *Adv. Mater.* 13(2):113-116.
- Huck et al. (2000) "Ordering of Spontaneously Formed Buckles on Planar Surfaces," *Langmuir* 16:3497-3501.
- Huie, J.C. (2003) "Guided Molecular Self Assembly: A review of Recent Efforts," *Smart Mater. Struct.* 12:264-271.
- Huitema et al. (2001) "Plastic Transistors in Active-Matrix Displays," *Nature* 414:599.
- Hur et al. (2005) "Printed thin-film transistors and complementary logic gates that use polymer-coated single-walled carbon nanotube networks," *J. Appl. Phys.*, 98, 114302.
- Hur et al. (2005) "Organic Nanodelectrics for Low Voltage Carbon Nanotube Thin Film Transistors and Complementary Logic Gates," *J. Am. Chem. Soc.* 127:13808-13809.
- Hur et al. (Dec. 2004) "Nanotransfer Printing by Use of Noncovalent Surface Forces: Applications to Thin-Film Transistors that Use Single-Walled Carbon Nanotube Networks and Semiconducting Polymers," *Appl. Phys. Lett.* 85(23):5730-5732.
- Hur et al. (Jun. 13, 2005) "Extreme Bendability of Single Walled Carbon Nanotube Networks Transferred From High-Temperature Growth Substrates to Plastic and Their Use in Thin-Film Transistors," *Appl. Phys. Lett.* 243502.
- Hutchinson et al. (1992) "Mixed Mode Cracking in Layered Materials," *Adv. Appl. Mech.* 29:63-191.
- Imparato et al. (2005) "Excimer Laser Induced Crystallization of Amorphous Silicon on Flexible Polymer Substrates," *Thin Solid Films* 487:58-62.
- International Search Report and Written Opinion, Corresponding to International Application No. PCT/US10/50468, Mailed Jan. 6, 2011.
- International Search Report and Written Opinion, Corresponding to International Application No. PCT/US10/60425, Mailed May 25, 2011.
- International Search Report and Written Opinion, Corresponding to International Application No. PCT/2005/014449, Mailed Jul. 3, 2008.
- International Search Report and Written Opinion, Corresponding to International Application No. PCT/US04/40192, Mailed Jul. 6, 2005.
- International Search Report and Written Opinion, Corresponding to International Application No. PCT/US07/74293, Mailed Jul. 24, 2008.
- International Search Report and Written Opinion, Corresponding to International Application No. PCT/US07/77217, Mailed Jun. 3, 2008.
- International Search Report and Written Opinion, Corresponding to International Application No. PCT/US07/82633, Mailed May 16, 2008.
- International Search Report and Written Opinion, Corresponding to International Application No. PCT/US09/47442, Mailed Sep. 21, 2009.
- International Search Report and Written Opinion, Corresponding to International Application No. PCT/US2006/032125, Mailed Mar. 21, 2008.
- International Search Report and Written Opinion, Corresponding to International Application No. PCT/US2009/036192, Mailed Jul. 6, 2009.
- International Search Report and Written Opinion, Corresponding to International Application No. PCT/US2009/058231, Mailed Nov. 17, 2009.
- International Search Report and Written Opinion, Corresponding to International Application No. PCT/US2010/034520, Mailed Sep. 24, 2010.
- International Search Report and Written Opinion, Corresponding to International Application No. PCT/US2010/042585, Mailed May 25, 2011.
- International Search Report and Written Opinion, Corresponding to International Application No. PCT/US2011/028094, Mailed Jul. 14, 2011.
- International Search Report and Written Opinion, Corresponding to International PCT Application No. PCT/US05/19354, Dated Apr. 18, 2007.
- International Search Report and Written Opinion, Corresponding to International PCT Application No. PCT/US2006/021161, Mailed Feb. 28, 2008.
- International Search Report and Written Opinion, Corresponding to International PCT Application No. PCT/US2007/022959, Mailed Oct. 14, 2008.
- International Search Report and Written Opinion, Corresponding to International PCT Application No. PCT/US2007/077759, Mailed Apr. 11, 2008.
- International Search Report and Written Opinion, Corresponding to International PCT Application No. PCT/US2007/079070, Mailed Apr. 23, 2008.
- Isberg et al. (Sep. 6, 2002) "High Carrier Mobility in Single-Crystal Plasma-Deposited Diamond," *Science* 297:1670-1672.
- Islam et al. (Jan. 16, 2003) "High Weight Fraction Surfactant Solubilization of Single-Wall Carbon Nanotubes in Water," *Nano Lett.* 3(2):269-273.
- Ismach et al. (2004) "Atomic-Step-Templated Formation of Single Wall Carbon Nanotube Patterns," *Angew. Chem. Int. Ed.* 43:6140-6143.
- Itoh et al. (1991) "Cathodoluminescence Properties of Undoped and Zn-Doped  $\text{Al}_{x}\text{Ga}_{1-x}\text{N}$  Grown by Metalorganic Vapor Phase Epitaxy," *Jap. J. Appl. Phys.* 30:1604-1608.
- Jabbour et al. (2001) "Screen Printing for the Fabrication of Organic Light-Emitting Devices," *IEEE J. Select. Top. Quantum Electron.* 7:769-773.
- Jackman et al. (Aug. 4, 1995) "Fabrication of Submicrometer Features on Curved Substrates by Microcontact Printing," *Science* 269:664-666.
- Jacobs et al. (2001) "Submicrometer Patterning of Charge in Thin-Film Electrets," *Science* 291:1763-1766.
- Jacobs et al. (2002) "Fabrication of a Cylindrical Display by Patterned Assembly," *Science* 296:323-325.
- Jain et al. (2000) "III-Nitrides: Growth, Characterization, and Properties," *J. Appl. Phys.* 87:965-1006.
- Jain et al. (2005) "Flexible Electronics and Displays: High-Resolution, Roll-to-Roll, Projection Lithography and Photoblation processing Technologies for High-Throughput Production," *Proc. IEEE* 93:1500-1510.
- James et al. (1998) "Patterned Protein Layers on Solid Substrates by This Stamp Microcontact Printing," *Langmuir* 14:742-744.
- Jang et al. (2003) "Lateral Growth of Aligned Multiwalled Carbon Nanotubes Under Electric Fields," *Solid State Commun.* 126:305-308.
- Jang et al. (2006) "Low-Voltage and High-Field-Effect Mobility Organic Transistors with a Polymer Insulator," *Appl. Phys. Lett.* 88:072101.
- Javey et al. (2002) "High-k Dielectrics for Advanced Carbon-Nanotube Transistors and Logic Gates," *Nature Mater.* 1:241-246.
- Javey et al. (2005) "High Performance n-Type Carbon Nanotube Field-Effect Transistors with Chemically Doped Contacts," *Nano Lett.*, vol. 5, No. 2, pp. 345-348.

(56)

**References Cited****OTHER PUBLICATIONS**

- Javey et al. (Aug. 7, 2003) "Ballistic Carbon Nanotube Field-Effect Transistors," *Nature* 424:654-657.
- Jenkins et al. (1994) "Gallium Arsenide Transistors: Realization Through a Molecularly Designs Insulator," *Science* 263:1751-1753.
- Jeon et al. (1995) "Patterning of Dielectric Oxide Thin Layers by Microcontact Printing of Self-Assembled Monolayers," *J. Mater. Res.* 10:2996-2999.
- Jeon et al. (2003) "Structural and Mechanical Properties of Woven Fabrics Employing Peirce's Model," *Textile Res. J.* 73:929-933.
- Jeon et al. (2004) "Fabricating Complex Three-Dimensional Nanostructures with High Resolution Conformable Phase Masks," *Proc. Natl. Acad. Sci. USA* 101:12428-12433.
- Jeon et al. (Aug. 4, 2004) "Three Dimensional Nanofabrication with Rubber Stamps and Conformable Photomasks," *Adv. Mater.* 16(15):1369-1375.
- Jiang et al. (Oct. 2, 2007) "Finite Deformation Mechanics in Buckled Thin Films on Compliant Supports," *Proc. Natl. Acad. Sci. USA* 104(40):15607-15612.
- Jiang et al. (1999) "Preparation of Macroporous Metal Films from Colloidal Crystals," *J. Am. Chem. Soc.* 121:7957-7958.
- Jiang et al. (2002) "Polymer-on-Polymer Stamping: Universal Approaches to Chemically Patterned Surfaces," *Langmuir* 18:2607-2615.
- Jiang et al. (2007) "Mechanical Properties of Robust Ultrathin Silk Fibroin Films," *Adv. Funct. Mater.* 17:2229-2237.
- Jin et al. (2004) "Scalable Interconnection and Integration of Nanowire Devices Without Registration," *Nano Lett.* 4:915-919.
- Jin et al. (2004) "Soft Lithographic Fabrication of an Image Sensor Array on a Curved Substrate," *J. Vac. Sci. Technol. B* 22(5):2548-2551.
- Jin et al. (Aug. 2005) "Water-Stable Silk Films with Reduced  $\beta$ -Sheet Content," *Adv. Funct. Mater.* 15(8):1241-1247.
- Jin et al. (Web Release Jan. 23, 2004) "Biomaterial Films of *Bombyx mori* Silk Fibroin with Poly(ethylene oxide)," *Biomacromolecules* 5(3):711-717.
- Jiyun, C.H. (2003) "Guided Molecular Self-Assembly: A Review of Recent Efforts," *Smart Mater. Struct.* 12:264-271.
- Joachim et al. (Nov. 30, 2000) "Electronics Using Hybrid-Molecular and Mono-Molecular Devices," *Nature* 408:541-548.
- Johnson et al. (1999) "Ordered Mesoporous Polymers of Tunable Pore Size from Colloidal Silica Templates," *Science* 283:963-965.
- Jones et al. (Jul./Aug. 2004) "Stretchable Wavy Metal Interconnects," *J. Vac. Sci. Technol. A* 22(4):1723-1725.
- Joo et al. (2006) "Low-Temperature Solution-Phase Synthesis of Quantum Well Structures CdSe Nanoribbons," *J. Am. Chem. Soc.* 128(17):5632-5633.
- Jortner et al. (2002) "Nanostructured Advanced Materials Perspectives and Directions," *Pure Appl. Chem.* 74(9):1491-1506.
- Joselevich (2002) "Vectorial Growth of Metallic and Semiconducting Single-Wall Carbon Nanotubes," *Nano Lett.*, vol. 2, No. 10, pp. 1137-1141.
- Kadish et al. (1988) "Interaction of Fiber Orientation and Direction of Impulse Propagation with Anatomic Barriers in Anisotropic Canine Myocardium," *Circulation*. 78:1478-1494.
- Kagan (1999) "Organic-Inorganic Hybrid Materials as Semiconducting Channels in Thin-Film Field-Effect Transistors," *Science* 286:945-947.
- Kagan et al. (2001) "Patterning Organic-Inorganic Thin-Film Transistors Using Microcontact Printed Templates," *Appl. Phys. Lett.* 79(21):3536-3538.
- Kagan et al. (2003) *Thin Film Transistors*, Dekker, New York, pp. 1-34.
- Kane et al. (2000) "Analog and Digital Circuits Using Organic Thin-Film Transistors on Polyester Substrates," *IEEE Electron. Dev. Lett.* 21:534-536.
- Kang et al. (2007) "Printed Multilayer Superstructures of Aligned Single-Walled Carbon Nanotubes for Electronic Applications," *Nano Lett.* 7(11):3343-3348.
- Kang et al. (Apr. 2007) "High-Performance Electronics Using Dnese, Perfectly aligned Arrays of Single-Walled Carbon Nanotubes," *Nat. Nanotechnol.* 2(4):230-236.
- Kar et al. (2005) "Controlled Synthesis and Photoluminescence Properties of ZnS Nanowires and Nanoribbons," *J. Phys. Chem. B* 109(8):3298-3302.
- Kar et al. (2005) "Synthesis and Optical Properties of CdS Nanoribbons," *J. Phys. Chem. B*, 109(41):19134-19138.
- Kar et al. (2006) "Shape Selective Growth of CdS One-Dimensional Nanostructures by a Thermal Evaporation Process," *J. Phys. Chem. B*, 110(10):4542-4547.
- Karnik et al. (2003) "Lateral Polysilicon p<sub>+</sub>-p-n<sup>+</sup>and p<sup>+</sup>-n-n<sup>+</sup>Diodes," *Solid-State Electronics* 47:653-659.
- Karnik et al. (2003) "Multiple Lateral Polysilicon Diodes as Temperature Sensors for Chemical Microreaction Systems," *Jpn. J. Appl. Phys.* 42:1200-1205.
- Kato et al. (2004) "The Characteristic Improvement of Si(111) Metal-Oxide-Semiconductor Field-Effect Transistor by Long-Time Hydrogen Annealing," *Jpn. J. Appl. Phys.* 43(10):6848-6853.
- Katz et al. (2001) "Synthetic Chemistry for Ultrapure, Processable, and High-Mobility Organic Transistor Semiconductors," *Acc. Chem. Res.* 34:359-369.
- Katz, H.E. (2004) "Recent Advances in Semiconductor Performance and Printing Processes for Organic Transistor-Based Electronics," *Chem. Mater.* 16:4748-4756.
- Kawata et al. (2001) "Finer Features for Functional Microdevices," *Nature* 412:697- 698.
- Kellis et al. (2009) "Human Neocortical Electrical Activity Recorded on Nonpenetrating Microwire Arrays: Applicability for Neuroprostheses," *Neurosurg. Focus* 27(1):E9.
- Kendall, D.L. (1979) "Vertical Etching of Silicon at Very High Aspect Ratios," *Ann. Rev. Mater. Sci.* 9:373-403.
- Khakani et al. (2006) "Lateral Growth of Single Wall Carbon Nanotubes on Various Substrates by Means of an 'All-Laser' Synthesis Approach," *Diamond Relat. Mater.* 15:1064-1069.
- Khan et al. (1993) "High Electron Mobility Transistor Based on a GaN-Al<sub>x</sub>Ga<sub>1-x</sub>N Heterojunction," *Appl. Phys. Lett.* 63:1214-1215.
- Khang et al. (2006) "A Stretchable Form of Single-Crystal Silicon for High-Performance Electronics on Rubber Substrates," *Science* 311:208-212.
- Kilby, J.S. (1976) "Invention of the Integrated Circuit," *IEEE Trans. Electron. Dev.* 23:648-654.
- Kim et al. (2000) "Field Emission from Carbon Nanotubes for Displays," *Diamond and Related Mater.* 9(3-6):1184-1189.
- Kim et al. (2002) "Nanolithography Based on Patterned Metal Transfer and Its Application to Organic Electronic Devices," *Appl. Phys. Lett.* 80:4051-4053.
- Kim et al. (2003) "Epitaxial Self-Assembly of Block Copolymers on Lithographically Defined Nanopatterned Substrates," *Nature* 424:411-414.
- Kim et al. (2008) "Stretchable Electronics: Materials Strategies and Devices," *Adv. Mater.* 20:4887-4892.
- Kim et al. (2009) "Integrated Wireless Neural Interface Based on the Utah Electrode array," *Biomed. Microdevices* 11:453-466.
- Kim et al. (2009) "Optimized Structural Designs for Stretchable Silicon Integrated Circuits," *Small* 5(24):2841-2847.
- Kim et al. (Apr. 25, 2008) "Stretchable and Foldable Silicon Integrated Circuits," *Science* 320:507-511.
- Kim et al. (Dec. 2, 2008) "Materials and Noncoplanar Mesh Designs for Integrated Circuits with Linear Elastic Responses to Extreme Mechanical Deformations," *Proc. Natl. Acad. Sci. USA* 105(48):18675-18680.
- Kim et al. (Jan. 2008) "Complementary Logic Gates and Ring Oscillators Plastic Substrates by Use of Printed Ribbons Single-Crystalline Silicon," *IEEE Electron. Dev. Lett.* 29(1):73-76.
- Kim et al. (Nov. 15, 1999) "Direct Observation of Electron Emission Site on Boron-Doped Polycrystalline Diamond Thin Films Using an Ultra-High-Vacuum Scanning Tunneling Microscope," *Appl. Phys. Lett.* 75(20):3219-3221.
- Kim et al. (Oct. 17, 2010) "Waterproof AlInGaP optoelectronics on stretchable substrates with applications in biomedicine and robotics," *Nature Materials* 9:929-937.

(56)

**References Cited****OTHER PUBLICATIONS**

- Kim et al. (Oct. 2004) "Organic TFT Array on a Paper Substrate," *IEEE Electron. Dev. Lett.* 25(10):702-704.
- Kim et al. (Web Release Apr. 18, 2010) "Dissolvable Films of Silk Fibroin for Ultrathin Conformal Bio-Integrated Electronics," *Nature Materials* 9:511-517.
- Kim et al. (Web Release Feb. 29, 2008) "Highly Emissive Self-Assembled Organic Nanoparticles Having Dual Color Capacity for Targeted Immunofluorescence Labeling," *Adv. Mater.* 20(6):1117-1121.
- Kim et al. (Web Release Jul. 31, 2008) "Complementary Metal Oxide Silicon Integrated Circuits Incorporating Monolithically Integrated Stretchable Wavy Interconnects," *Appl. Phys. Lett.* 93(4):044102.
- Kim et al. (Web Release Jul. 6, 2009) "Ultrathin Silicon Circuits with Strain-Isolation Layers and Mesh Layouts for High-Performance Electronics on Fabric, Vinyl, Leather and Paper," *Adv. Mater.* 21(36):3703-3707.
- Kim et al. (Web Release Sep. 29, 2009) "Silicon Electronics on Silk as a Path to Bioreversible, Implantable Devices," *Appl. Phys. Lett.* 95:133701-133703.
- Kim, Y.S. (Web Release Aug. 9, 2005) "Microheater-Integrated Single Gas Sensor Array Chip Fabricated on Flexible Polyimide Substrate," *Sens. Actuators B* 114(1):410-417.
- Klauck et al. (2002) "High-Mobility Polymer Gate Dielectric Pentacene Thin Film Transistors," *J. Appl. Phys.* 92:5259-5263.
- Klein-Wiele et al. (2003) "Fabrication of Periodic Nanostructures by Phase-Controlled Multiple-Beam Interference," *Appl. Phys. Lett.* 83(23):4707-4709.
- Knipp et al. (2003) "Pentacene Thin Film Transistors on Inorganic Dielectrics: Morphology, Structural Properties, and Electronic Transport," *Appl. Phys. Lett.* 93:347-355.
- Ko et al. (2006) "Bulk Quantities of Single-Crystal Silicon Micro-/Nanoribbons Generated from Bulk Wafers," *Nano Lett.* 6(10):2318-2324.
- Ko et al. (2010) "Flexible Carbon Nanofiber Connectors with Anisotropic Adhesion Properties," *Small* 6:22-26.
- Ko et al. (Aug. 7, 2008) "A Hemispherical Electronic Eye Camera Based on Compressible Silicon Optoelectronics," *Nature* 454:748-753.
- Ko et al. (Web Release Oct. 28, 2009) "Curvilinear Electronics Formed Using Silicon Membrane Circuits and Elastomeric Transfer Elements," *Small* 5(23):2703-2709.
- Kocabas et al. (2004) "Aligned Arrays of Single-Walled Carbon Nanotubes Generated from Random Networks by Orientationally Selective Laser Ablation," *Nano Lett.*, vol. 4, No. 12, pp. 2421-2426.
- Kocabas et al. (2005) "Guided Growth of Large-Scale, Horizontally Aligned Arrays of Single-Walled Carbon Nanotubes and Their Use in Thin-Film Transstors," *Small* 1(11):1110-1116.
- Kocabas et al. (2006) "Large Area Aligned Arrays of SWNTs for High Performance Thin Film Transistors," American Physical Society, APS March Meeting, Mar. 13-17, Abstract # W31.004.
- Kocabas et al. (2006) "Spatially Selective Guided Growth of High-Coverage Arrays and Random Networks of Single-Walled Carbon Nanotubes and Thir Integration into Electronic Devices," *J. Am. Chem. Soc.* 128:4540-4541.
- Kocabas et al. (2007) "Experimental and Theoretical Studies of Transport Through Large Scale, Partially Aligned Arrays of Single-Walled Carbon Nanotubes ni Thin Film Type Transistors," *Nano Lett.* 7(5):1195-1202.
- Kocabas et al. (Feb. 5, 2008) "Radio Frequency Analog Electronics Based on Carbon Nanotube Transistors," *Proc. Natl. Acad. Sci. USA* 105(5):1405-1409.
- Kodambaka et al. (2006) "Control of Si Nanowire Growth by Oxygen," *Nano Lett.* 6(6):1292-1296.
- Koide et al. (2000) "Patterned Luminescence of Organic Light-Emitting Diodes by Hot Microcontact Printing (HμCP) of Self-Assembled Monolayers," *J. Am. Chem. Soc.* 122:11266-11267.
- Konagai et al. (1978) "High Efficiency GaAs Thin Film Solar Cells by Peeled Film Technology," *J. Cryst. Growth* 45:277-280.
- Kong et al. (2004) "Single-Crystal Nanorings Formed by Epitaxial SelfCoating of Polar Nanobelts," *Science* 303:1348-1351.
- Kong et al. (Jan. 28, 2000) "Nanotube Molecular Wires as Chemical Sensors," *Science* 287:622-625.
- Kong et al. (Oct. 2003) "Structure of Indium Oxide Nanobelts," *Solid State Commun.* 128(1):1-4.
- Kong et al. (Oct. 29, 1998) "Synthesis of Individual Single-Walled Carbon Nonotubes on Patterned Silicon Wafers," *Nature* 395:878-881.
- Kudo et al. (Web Release Jun. 13, 2006) "A Flexible and Wearable Glucose Sensor Based on Functional Polymers with Soft-MEMS Techniques," *Biosens. Bioelectron.* 22:558-562.
- Kulkarni et al. (2002) "Mesoscale Organization of Metal Nanocrystals," *Pure Appl. Chem.* 74(9):1581-1591.
- Kumar et al. (1993) "Features of Gold Having Micrometer to Centimeter Dimensions can be Formed Through a Combination of Stamping with an Elastomeric Stamp and an Alkanethiol "Ink" Followed by Chemical Etching," *Appl. Phys. Lett.* 63(4):2002-2004.
- Kumar et al. (1994) "Patterning Self-Assembled Monolayers: Applications in Materials Science," *Langmuir* 10:1498-1511.
- Kumar et al. (2002) "Thermally-Stable Low-Resistance Ti/Al/Mo/Au Multilayer Ohmic Contacts on n—GaN," *J. Appl. Phys.* 92:1712-1714.
- Kumar et al. (2005) "Percolating in Finite Nanotube Networks," *Phys. Rev. Lett.*, 95, 066802.
- Kuo et al. (1985) "Effect of Mismatch Strain on Band Gap in III-V Semiconductors," *J. Appl. Phys.* 57:5428-5432.
- Kuykendall et al. (Aug. 2004) "Crystallographic Alignment of High Density Gallium Nitride Nanowire Arrays," *Nat. Mater.* 3:524-528.
- Lacour et al. (2005) "Stretchable Interconnects for Elastic Electronic Surfaces," *Proc. IEEE* 93:1459-1467.
- Lacour et al. (2010) "Flexible and Stretchable Micro-Electrodes for in Vitro and n Vivo Neural Interfaces," *Med. Biol. Eng. Comput.* 48:945-954.
- Lacour et al. (Apr. 14, 2003) "Stretchable Gold Conductors on Elastomeric Substrates," *Appl. Phys. Lett.* 82(15):2404.
- Lacour et al. (Apr. 2004) "Design and Performance of Thin Metal Film Interconnects for Skin-Like Electronic Circuits," *IEEE Electron. Dev. Lett.* 25(4):179-181.
- Lacour et al. (Dec. 2004) "An Elastically Stretchable TFT Circuit," *IEEE Electron. Dev. Lett.* 25(12):792-794.
- Lacour et al. (Web Release Jul. 14, 2006) "Stiff Subcircuit Islands of Diamondlike Carbon for Stretchable Electronics," *J. Appl. Phys.* 100:014913.
- Lacour et al. (Web Release May 16, 2006) "Mechanisms of Reversible Stretchability of Thin Metal Films on Elastomeric Substrates," *Appl. Phys. Lett.* 88:204103.
- Laimer et al. (Mar. 1997) "Diamond Growth in a Direct-Current Low-Pressure Supersonic Plasmatjet," *Diamond Relat. Mater.* 6:406-410.
- Lambacher et al. (2004) "Electrical Imaging of Neuronal Activity by Multi-Transistor-Array (MTA) Recording at 7.8 μm Resolution," *Appl. Phys. A* 79:1607-1611.
- Landes et al. (2002) "Some Properties of Spherical and Rod-Shaped Semiconductor and Metal Nanocrystals," *Pure Appl. Chem.* 74(9):1675-1692.
- Law et al. (2004) "Semiconductor Nanowires and Nanotubes," *Ann. Rev. Mater. Res.* 34:83-122.
- Law et al. (Aug. 27, 2004) "Nanoribbon Waveguides for Subwavelength Photonics Integration," *Science* 305:1269-1273.
- Lawrence et al. (2008) "Bioactive Silk Protein Biomaterial Systems for Optical Devices," *Biomacromolecules* 9:1214-1220.
- Lay et al. (2004) "Simple Route to Large-Scale Ordered Arrays of Liquid-Deposited Carbon Nanotubes," *Nano Lett.*, vol. 4, No. 4, pp. 603-606.
- Leclercq et al. (1998) "III-V Micromachined Devices for Microsystems," *Microelectronics J.* 29:613-619.
- Lecomte et al. (Apr. 2006) "Degradation Mechanism of Diethylene Glycol Units in a Terephthalate Polymer," *Polym. Degrad. Stab.* 91(4):681-689.

(56)

**References Cited****OTHER PUBLICATIONS**

- Lee et al. (2000) "Thin Film Transistors for Displays on Plastic Substrates," *Solid State Electron.* 44:1431-1434.
- Lee et al. (2003) "High-Performance Poly-Si TFTs on Plastic Substrates Using a Nano-Structured Separation Layer Approach," *IEEE Elec. Dev. Lett.* 24:19-21.
- Lee et al. (2004) "Organic Light-Emitting Diodes Formed by Soft Contact Lamination," *Proc. Natl. Acad. Sci. USA* 101(2):429-433.
- Lee et al. (2005) "A Printable Form of Single-Crystalline Gallium Nitride for Flexible Optoelectronic Systems," *Small* 1:1164-1168.
- Lee et al. (2005) "Large-Area, Selective Transfer of Microstructured Silicon ( $\mu$ -Si): A Printing-Based Approach to High-Performance Thin0Film Transistors Supported on Flexible Substrata," *Adv. Mater.* 17:2332-2336.
- Lee et al. (2006) "Micron and Submicron Patterning of Polydimethylsiloxane Resists on Electronic Materials by Decal Transfer Lithography and Reactive Ion-Beam Etching: Application to the Fabrication of High-Mobility, Thin-Film Transistors," *Appl. Phys. Lett.* 100:084907/1-7.
- Lee et al. (Apr. 2005) "Fabrication of Stable Metallic Patterns Embedded in Poly(dimethylsiloxane) and Model Applications in Non-Planar Electronic and Lab-on-a-Chip Device Patterning," *Adv. Funct. Mater.* 15(4):557-566.
- Lee et al. (Dec. 1999) "The Surface/Bulk Micromachining (SBM) Process: A New Method for Fabricating Released MEMS in Single Crystal Silicon," *J. Microelectromech. Syst.* 8(4):409-416.
- Lee et al. (Feb. 2001) "Application of Carbon Nanotubes to Field Emission Displays," *Diamond and Related Mater.* 10(2):265-270.
- Lee et al. (Feb. 2005) "Weave Patterned Organic Transistors on Fiber for E-Textiles," *IEEE Trans. Electron. Dev.* 52(2):269-275.
- Leong et al. (2009) "Tetherless Thermobiochemical Actuated Microgrippers," *Proc. Natl. Acad. Sci. USA* 106:703-709.
- Létant et al. (Jun. 2003) "Functionalized Silicon Membranes for Selective Bio-Organisms Organisms Capture," *Nat. Mater.* 2:391-395.
- Li et al. (2002) "High-Resolution Contact Printing with Dendrimers," *Nano Lett.* 2(4):347-349.
- Li et al. (2003) "Ultrathin Single-Crystalline-Silicon Cantilever Resonators: Fabrication Technology and Significant Specimen Size effect on Young's Modulus," *Appl. Phys. Lett.* 83:3081-3083.
- Li et al. (2004) "Electrospinning of Nanofibers: Reinventing the Wheel," *Adv. Mater.* 16(14):1151-1170.
- Li et al. (2006) "Catalyst-Assisted Formation of Nanocantilever Arrays on ZnS Nanoribbons by Post-Annealing Treatment," *J. Phys. Chem. B* 110(13):6759-6762.
- Li et al. (Dec. 2005) "Compliant Thin Film Patterns of Stiff Materials as Platforms for Stretchable Electronics," *J. Mater. Res.* 20(12):3274-3277.
- Li et al. (Jul. 1, 2002) "ZnO Nanobelts Grown on Si Substrate," *Appl. Phys. Lett.* 81:144-146.
- Lieber, C. (2001) "The Incredible Shrinking Circuit," *Sci. Am.* 285(3):58-64.
- Lieber, C.M. (2003) "Nanoscale Science and Technology: Building a Big Future from Small Things," *MRS. Bull.* 28:486-491.
- Lim et al. (2005) "Flexible Membrane Pressure Sensor," *Sens. Act. A* 119:332-335.
- Lima et al. (2007) "Creating Micro—and Nanostructures on Tubular and Spherical Surfaces," *J. Vac. Sci. Technol. B* 25(6):2412-2418.
- Lin et al. (Sep. 2005) "High-Performance Carbon Nanotube Field-Effect Transistor With Tunable Polarities," *IEEE Trans. Nano* 4(5):481-489.
- Linder et al. (1994) "Fabrication Technology for Wafer Through-Hole Interconnections and Three-Dimensional Stacks of Chips and Wafers," *Proc. IEEE Micro. Electro Mech. Syst.* 349-354.
- Ling et al. (2004) "Thin Film Deposition, Patterning, and Printing in Organic Thin Film Transistors," *Chem. Mater.* 16:4824-4840.
- Liu et al. (1999) "Controlled deposition of individual single-walled carbon nanotubes on chemically functionalized templates," *Chem. Phys. Lett.*, 303:125-129.
- Long et al. (1990) "Heterostructure FETs and Bipolar Transistors," In: *Gallium Arsenide Digital Integrated Circuit Design*, McGraw-Hill, New York, pp. 58-69.
- Loo et al. (2002) "Additive, Nanoscale Patterning of Metal Films with a Stamp and a Surface Chemistry Mediated Transfer Process: Applications in Plastic Electronics," *Appl. Phys. Lett.* 81:562-564.
- Loo et al. (2002) "High-Resolution Transfer Printing on GaAs Surfaces Using Alkane Dithiol Monolayers," *J. Vac. Sci. Technol. B* 20(6):2853-2856.
- Loo et al. (2002) "Interfacial Chemistries for Nanoscale Transfer Printing," *J. Am. Chem. Soc.* 124:7654-7655.
- Loo et al. (2002) "Soft, Conformable Electrical Contacts for Organic Semiconductors: High-Resolution Plastic Circuits by Lamination," *Proc. Natl. Acad. Sci. USA* 99(16):10252-10256.
- Loo et al. (2003) "Electrical Contacts to Molecular Layers by Nanotransfer Printing," *Nano Lett.* 3(7):913-917.
- Lopes et al. (Sep. 2004) "Thermal Conductivity of PET/(LDPE/AI) Composites Determined by MDSC," *Polym. Test.* 23(6):637-643.
- Lu et al. (Apr. 2010) "Water-Insoluble Silk Films with Silk I Structure," *Acta Biomater.* 6(4):1380-1387.
- Lu et al. (Dec. 2006) "Electronic Materials-Buckling Down for Flexible Electronics," *Nat. Nanotechnol.* 1:163-164.
- Lu et al. (Jul. 19, 2005) "One Dimensional Hole Gas in Germanium/Silicon Nanowire Heterostructures," *Proc. Nat. Acad. Sci. USA* 102(29):10046-10051.
- Lu et al. (Nov. 2008) "Nanowire Transistor Performance Limits and Applications," *IEEE Trans Electron Dev.* 55(11):2859-2876.
- Luan et al. (1992) "An Experimental Study of the Source/Drain Parasitic Resistance Effects in Amorphous Silicon Thin Film Transistors," *J. Appl. Phys.* 72:766-772.
- Ma et al. (2004) "Single-Crystal CdSe Nanosaws," *J. Am. Chem. Soc.* 126(3):708-709.
- Mack et al. (2006) "Mechanically Flexible Thin-Film Transistors that Use Ultrathin Ribbons of Silicon Derived from Bulk Wafers," *Appl. Phys. Lett.* 88:213101.
- Madou, M. (1997) "Etch-Stop Techniques," In: *Fundamentals of Microfabrication*, CRC Press, New York, pp. 193-199.
- Maikap et al. (2004) "Mechanically Strained-Si NMOSFETs," *IEEE Electron. Dev. Lett.* 25:40-42.
- Maldovan et al. (2004) "Diamond-Structured Photonic Crystals," *Nature Materials* 3:593-600.
- Mandlik et al. (Aug. 2006) "Fully Elastic Interconnects on Nanopatterned Elastomeric Substrates," *IEEE Electron Dev. Lett.* 27(8):650-652.
- Manna et al. (Web Release May 25, 2003) "Controlled Growth of Tetrapod-Branched Inorganic Nanocrystals," *Nat. Mater.* 2:382-385.
- Markovich et al. (1999) "Architectonic Quantum Dot Solids," *Acc. Chem. Res.* 32:415-423.
- Marquette et al. (2004) "Conducting Elastomer Surface Texturing: A Path to Electrode Spotting Application to the Biochip Production," *Biosens. Bioelectron.* 20:197-203.
- Martensson et al. (2004) "Nanowire Arrays Defined by Nanoimprint Lithography," *Nano Lett.* 4:699-702.
- Martin, C.R. (1995) "Template Synthesis of Electronically Conductive Polymer Nanostructures," *Acc. Chem. Res.* 28:61-68.
- Mas-Torrent et al. (2006) "Large Photoresponsivity in High-Mobility Single-Crystal Organic Field-Effect Phototransistors," *ChemPhysChem* 7:86-88.
- Masuda et al. (2000) "Fabrication of Ordered Diamonds/Metal Nanocomposite Structures," *Chem. Lett.* 10:1112-1113.
- Matsunaga et al. (2003) "An Improved GaAs Device Model for the Simulation of Analog Integrated Circuit," *IEEE Trans. Elect. Dev.* 50:1194-1199.
- McAlpine et al. (2003) "High-Performance Nanowire Electronics and Photonics on Glass and Plastic Substrates," *Nano Lett.* 3:1531-1535.
- McAlpine et al. (2005) "High-Performance Nanowire Electronics and Photonics and Nanoscale Patterning on Flexible Plastic Substrates," *Proc. IEEE* 93:1357-1363.
- McCalldin et al. (1971) "Diffusivity and Solubility of Si in the Al Metallization of Integrated Circuits," *Appl. Phys. Lett.* 19:524-517.

(56)

**References Cited****OTHER PUBLICATIONS**

- Mehring C. et al. (2003) Inference of hand movements from local field potentials in monkey motor cortex. *Nature Neurosci.* 6, 1253-1254.
- Meisel et al. (2004) "Three-Dimensional Photonic Crystals by Holographic Lithography Using the Umbrella Configuration: Symmetries and Complete Photonic Band Gaps," *Phys. Rev. B*, 70:165101:1-10.
- Meitl et al. (2004) "Solution Casting and Transfer Printing Single-Walled Carbon Nanotube Films," *Nano Lett.* 4:1643-1647.
- Meitl et al. (2006) "Transfer Printing by Kinetic Control of Adhesion to an Elastomeric Stamp," *Nat. Mater.* 5:33-38.
- Meitl et al. (Web Release Feb. 22, 2007) "Stress Focusing for Controlled Fracture in Microelectromechanical Systems," *Appl. Phys. Lett.* 90:083110.
- Melosh et al. (2003) "Ultrahigh-Density Nanowire Lattices and Circuits," *Science* 300:112-115.
- Menard et al. (2004) "A Printable Form of Silicon for High Performance Thin Film Transistors on Plastic Substrates," *Appl. Phys. Lett.* 84:5398-5400.
- Menard et al. (2004) "Improved Surface Chemistries, Thin Film Deposition Techniques, and Stamp Designs for Nanotransfer Printing," *Langmuir* 20:6871-6878.
- Menard et al. (2004) "High-Performance n—and p-Type Single-Crystal Organic Transistors with Free-Space Gate Dielectrics," *Adv. Mat.* 16:2097-2101.
- Menard et al. (2005) "Bendable Single Crystal Silicon Thin Film Transistors Formed by Printing on Plastic Substrates," *Appl. Phys. Lett.* 86(093507):1-3.
- Menard et al. (2007) Micro—and Nanopatterning Techniques for Organic Electronic and Optoelectronic Systems, *Chem. Rev.* 107:1117-1160.
- Miao et al. (2003) "Micromachining of Three-Dimensional GaAs Membrane Structures Using High-Energy Nitrogen Implantation," *J. Micromech. Microeng.* 13:35-39.
- Michalske et al. (1985) "Closure and Repropagation of Healed Cracks in Silicate Glass," *J. Am. Ceram. Soc.* 68:586-590.
- Michel et al. (2001) Printing Meets Lithography: Soft Approaches to High-Resolution Patterning, *IBM J. Res. Dev.* 45:697-719.
- Miller et al. (2002) "Direct Printing of Polymer Microstructures on Flat and Spherical Surfaces Using a Letterpress Technique," *J. Vac. Sci. Technol. B* 20(6):2320-2327.
- Milliron et al. (2004) "Colloidal Nanocrystal Heterostructures with Linear and Branched Topology," *Nature* 430:190-195.
- Min, G. (Apr. 4, 2003) "Plastic Electronics and Their Packaging Technologies," *Syn. Metals.* 135:141-143.
- Minev et al. (2010) "Impedance Spectroscopy on Stretchable Microelectrode Arrays," *Appl. Phys. Lett.* 97:043707.
- Mirkin et al. (2001) "Emerging Methods for Micro—and Nanofabrication," *MRS Bulletin* 26(7):506-507.
- Misewich et al. (May 2, 2003) "Electronically Induced Optical Emission from a Carbon Nanotube FET," *Science* 300:783-786.
- Mishra et al. (2002) "AlGaN/GaN HEMTs—an Overview of Device Operation and Applications," *Proc. IEEE* 90:1022-1031.
- Mitzi et al. (2004) "High-Mobility Ultrathin Semiconducting Films Prepared by Spin Coating," *Nature* 428:299-303.
- Moon et al. (2002) "Ink-Jet Printing of Binders for Ceramic Components," *J. Am. Ceram. Soc.* 85:755-762.
- Moore et al. (Sep. 9, 2003) "Individually Suspended Single-Walled Carbon Nanotubes in Various Surfactants," *Nano Lett.* 3(10):1379-1382.
- Morales et al. (Jan. 9, 1998) "A Laser Ablation Method for the Synthesis of Crystalline Semiconductor Nanowires," *Science* 279:208-211.
- Morent et al. (2007) "Adhesion Enhancement by a Dielectric Barrier Discharge of PDMS used for Flexible and Stretchable Electronics," *J. Phys. D. Appl. Phys.* 40:7392-7401.
- Mori et al. (1978) "A New Etching Solution System, H<sub>3</sub>PO<sub>4</sub>, H<sub>2</sub>O<sub>2</sub>, H<sub>2</sub>O, for GaAs and Its Kinetics," *J. Electrochem. Soc.* 125:1510-1514.
- Morkoc et al. (1995) "High-Luminosity Blue and Blue-Green Gallium Nitride Light-Emitting Diodes," *Science* 267:51-55.
- Morkved et al. (1994) "Mesoscopic Self-Assembly of Gold Islands on Diblock-Copolymer Films," *Appl. Phys. Lett.* 64:422-424.
- Morra et al. (1990) "On the Aging of Oxygen Plasma-Treated Polydimethylsiloxane Surfaces," *J. Colloid Interface Sci.* 137:11-24.
- Murakami et al. (2005) "Polarization Dependence of the Optical Absorption of Single-Walled Carbon Nanotubes," *Phys. Rev. Lett.*, 94, 087402.
- Murphy et al. (2008) "Modification of Silk Fibroin Using Diazonium Coupling Chemistry and the Effects on hMSC Proliferation and Differentiation," *Biomaterials* 29:2829-2838.
- Namazu et al. (2000) "Evaluation of Size Effect on Mechanical Properties of Single Crystal Silicon by Nanoscale Bending Test Using AFM," *J. MEMS* 9:450-459.
- Nath et al. (2002) "Nanotubes of the Disulfides of Groups 4 and 5 Metals," *Pure Appl. Chem.* 74(9):1545-1552.
- Nathan et al. (2000) "Amorphous Silicon Detector and Thin Film Transistor Technology for Large-Area Imaging of X-Rays," *Microelectron. J.* 31:883-891.
- Nathan et al. (2002) "Amorphous Silicon Technology for Large Area Digital X-Ray and Optical Imaging," *Microelectronics Reliability* 42:735-746.
- Newman et al. (2004) "Introduction to Organic Thin Film Transistors and Design of n-Channel Channel Organic Semiconductors," *Chem. Mater.* 16:4436-4451.
- Nirmal et al. (1999) "Luminescence Photophysics in Semiconductor Nanocrystals," *Acc. Chem. Res.* 32:407-414.
- Noda et al. (1996) "New Realization Method for Three-Dimensional Photonic Crystal in Optical Wavelength Region," *Jpn. J. Appl. Phys.* 35:L909-L912.
- Nomura et al. (2004) "Room-Temperature Fabrication of Transparent Flexible Thin-Film Transistors Using Oxide Semiconductors," *Nature* 432:488-492.
- Notice of Allowance corresponding to Korean Patent Application No. 10-2012-7010094, dated Jul. 25, 2012.
- Notice of Allowance corresponding to Korean Patent Application No. 10-2007-7000216, dated Jun. 26, 2013.
- Notice of Allowance dated Dec. 25, 2014, corresponding to Korean Patent Application No. 10-2013-7022417.
- Notice of Allowance dated Feb. 25, 2013, for corresponding Korean Patent Application No. 10-2012-7010094.
- Notice of Allowance dated Februry 3, 2015 corresponding to Japanese Patent Application No. 2012-139129.
- Notice of Allowance dated Feb. 3, 2015 corresponding to Japanese Patent Application No. 2012-139132.
- Notice of Allowance dated Feb. 3, 2015 corresponding to Japanese Patent Application No. 2012-139129.
- Notice of Allowance dated Mar. 30, 2015, corresponding the U.S. Appl. No. 14/220,923.
- Notice of Allowance dated May 28, 2014, for corresponding Korean Patent Application No. 10-2013-7022416.
- Notice of Final Rejection dated Jan. 6, 2015, corresponding the Japanese Patent Application No. P2013-000174.
- Notice of Grant dated Jul. 31, 2014, corresponding to Malaysian Patent Application No. PI 20052553.
- Notice of Preliminary Rejection corresponding to Korean Patent Application No. 10-2006-0053675, dated Nov. 12, 2012.
- Notice of Preliminary Rejection corresponding to Korean Patent Application No. 10-2007-7000216, dated Feb. 21, 2013.
- Notice of Preliminary Rejection corresponding to Korean Patent Application No. 10-2007-7000216, dated Oct. 19, 2011.
- Notice of Preliminary Rejection corresponding to Korean Patent Application No. 10-2012-7010094, dated May 25, 2012.
- Notice of Preliminary Rejection corresponding to Korean Patent Application No. 10-2012-7030789, dated Feb. 25, 2013.
- Notice of Preliminary Rejection corresponding to Korean Patent Application No. 10-2013-0131753, dated Jan. 29, 2014.
- Notice of Preliminary Rejection corresponding to Korean Patent Application No. 10-2013-7034843, dated Mar. 31, 2014.
- Notice of Preliminary Rejection corresponding to Korean Patent Application No. 10-2013-7022417, dated Apr. 28, 2014.

(56)

**References Cited****OTHER PUBLICATIONS**

- Notice of Preliminary Rejection dated Feb. 27, 2014, corresponding to Korean Patent Application No. 10-2013-7034843.
- Notice of Preliminary Rejection dated Sep. 24, 2014, corresponding to Korean Patent Application No. 10-2014-0096828.
- Notice of Preliminary Rejection dated Sep. 29, 2013, for corresponding Korean Patent Application No. 10-2013-7022416.
- Notice of Preliminary Rejection dated Sep. 29, 2013, for corresponding Korean Patent Application No. 10-2013-7022417.
- Notice of Reasons for Rejection corresponding to Japanese Patent Application No. P2006-165159, dispatched Apr. 16, 2013.
- Notice of Reasons for Rejection corresponding to Japanese Patent Application No. P2006-165159, Dispatched Apr. 24, 2012—includes English translation.
- Notice of Reasons for Rejection corresponding to Japanese Patent Application No. P2008-514820, Dispatched May 8, 2012—includes English translation.
- Notice of Reasons for Rejection corresponding to Japanese Patent Application No. P2009-546361, Dispatched Jul. 3, 2012—includes English translation.
- Notice of Reasons for Rejection dated Sep. 2, 2014, corresponding to the Japanese Patent Application No. P2013-169101.
- Notice of Reasons for Rejection issued for Japanese Patent Application No. P2007-515549, issued Dec. 20, 2011.
- Notice of Reasons for Rejection issued for Japanese Patent Application No. P2012-139132, Dispatched Jan. 21, 2014—includes English translation.
- Notice of Reasons for Rejection issued for Japanese Patent Application No. P2012-139129, Dispatched Jan. 21, 2014—includes English translation.
- Notice of Reasons for Rejection issued for Japanese Patent Application No. P2013-000174, Dispatched Apr. 1, 2014—includes English translation.
- Novoselov et al. (Oct. 22, 2004) "Electric Field Effect in Atomically Thin Carbon Films," *Science* 306:666-669.
- O'Connell et al. (Jul. 26, 2002) "Bang Gap Fluorescence from Individual Single-Walled Caarbon Nanotubes," *Science* 297:593-596.
- O'Riordan et al. (2004) "Field Configured Assembly: Programmed Manipulation and Self-Assembly at the Mesoscale," *Nano Lett.* 4:761-765.
- Odum et al. (2002) "Improved Pattern Transfer in Soft Lithography Using Composite Stamps," *Langmuir* 18(13):5314-5320.
- Office Action and Response, Corresponding to Malaysian Patent Publication No. PI 20052553, Mailed Mar. 13, 2009 and Dec. 8, 2009.
- Office Action and Response, Corresponding to U.S. Appl. No. 11/423,287, Mailed Feb. 13, 2008.
- Office Action and Response, Corresponding to U.S. Appl. No. 11/421,654, Mailed Sep. 29, 2009.
- Office Action and Response, Corresponding to U.S. Appl. No. 11/858,788, Mailed Beginning Jan. 28, 2011.
- Office Action Corresponding to Chinese Patent Application No. 200780041127.6, Issued Apr. 8, 2011.
- Office Action Corresponding to Chinese Patent Application No. 200780049982.1, Issued May 12, 2010.
- Office Action Corresponding to Chinese Patent Application No. 201010519400.5, issued Nov. 2, 2011.
- Office Action Corresponding to Chinese Patent Application No. 201010519400.5, issued Oct. 30, 2012.
- Office Action corresponding to Japanese Patent Application No. P2015-040251, dispatched, Mar. 8, 2016.
- Office action Corresponding to Korean Patent Application No. 10-2006-7010632, Completed Nov. 22, 2007.
- Office Action corresponding to Korean Patent Application No. 10-2015-7017151, dated Mar. 17, 2016—with English translation.
- Office Action corresponding to Taiwanese Patent Application No. 095119788, issued Mar. 26, 2013, with English translation.
- Office Action Corresponding to U.S. Appl. No. 11/851,182, Mailed Apr. 1, 2010.
- Office Action Corresponding to U.S. Appl. No. 11/851,182, Mailed Jun. 7, 2011.
- Office Action Corresponding to U.S. Appl. No. 12/398,811, Mailed Nov. 26, 2012.
- Office Action corresponding to U.S. Appl. No. 12/405,475, mailed Jun. 8, 2011.
- Office Action corresponding to U.S. Appl. No. 13/441,618, mailed May 23, 2013.
- Office Action dated Dec. 17, 2014, corresponding to U.S. Appl. No. 14/220,923.
- Office Action dated Jul. 30, 2014, corresponding to Taiwan Patent Application No. 099127004.
- Office Action, Corresponding to Chinese Patent Application No. 200780048002.6, Issued Apr. 13, 2010.
- Office Action, Corresponding to Chinese Patent Application No. 200580013574.1, Issued May 11, 2010.
- Office Action, Corresponding to Taiwan Patent Application No. 095121212, Issued May 7, 2010.
- Office Action, corresponding to U.S. Appl. No. 11/851,182, mailed Oct. 29, 2010.
- Office Action, Corresponding to U.S. Appl. No. 11/981,380, Mailed Sep. 23, 2010.
- Office Actions and Responses, Corresponding to U.S. Appl. No. 11/145,542, Mailed between Apr. 5, 2007 and Dec. 23, 2008.
- Office Actions and Responses, Corresponding to U.S. Appl. No. 11/981,380, Mailed Beginning Sep. 23, 2010.
- Office Actions Corresponding to Chinese Patent Application No. 200480035731.4, Issued Mar. 27, 2009 and Dec. 3, 2010.
- Office Actions, Corresponding to Chinese Patent Application No. 200580018159.5, Issued Jan. 23, 2009 and Feb. 12, 2010.
- Ohzono et al. (2004) "Ordering of Microwrinkle Patterns by Compressive Strain," *Phys. Rev. B* 69(13):132202.
- Ohzono et al. (Web Release Jul. 7, 2005) "Geometry-Dependent Stripe Rearrangement Processes Induced by Strain on Preordered Microwrinkle Patterns," *Langmuir* 21(16):7230-7237.
- Omenetto et al. (2008) "A New Route for Silk," *Nature Photon.* 2:641-643.
- Ong et al. (2004) "High-Performance Semiconducting Polythiophenes for Organic Thin-Film Transistors," *J. Am. Chem. Soc.* 126:3378-3379.
- Ong et al. (2005) "Design of High-Performance Regioregular Polythiophenes for Organic Thin-Film Transistors," *Proc. IEEE* 93:1412-1419.
- Origin Energy (May 2004) "Fact Sheet—Sliver Cells," www.orginenergy.com.au/sliver.
- Ouyang et al. (2002) "High-Performance, Flexible Polymer Light-Emitting Diodes Fabricated by a Continuous Polymer Coating Process," *Adv. Mat.* 14:915-918.
- Ouyang et al. (2008) "High Frequency Properties of Electro-Textiles for Wearable Antenna Applications," *IEEE Trans. Antennas Propag.* 56(2):381-389.
- Ouyang et al. (Web Release Mar. 20, 2000) "Conversion of Some Siloxane Polymers to Silicon Oxide by UV/Ozone Photochemical Processes," *Chem. Mater.* 12(6):1591-1596.
- Overholt et al. (2005) "Photodynamic Therapy for Esophageal Cancer using a 180° Windowed Esophageal Balloon," *Lasers in Surg. Med.* 14:27-33.
- Pan et al. (2001) "Nanobelts of Semiconducting Oxides," *Science* 291:1947-1949.
- Panay et al. (2003) "Sharp Excitation from Single InAs Quantum Dots in GaAs Nanowires," *Appl. Phys. Lett.* 83:2238-2240.
- Pardo et al. (2000) "Application of Screen Printing in the Fabrication of Organic Light-Emitting Devices," *Adv. Mater.* 12(17):1249-1252.
- Park et al. (1997) "Block Copolymer Lithography: Periodic Arrays of  $\sim 10^{11}$  Holes in 1 Square Centimeter," *Science* 276:1401-1404.
- Park et al. (1998) "Fabrication of Three-Dimensional Macroporous Membranes with Assemblies of Microspheres as templates," *Chem. Mater.* 10:1745-1747.
- Park et al. (Aug. 2009) "Printed Assemblies of Inorganic Light-Emitting Diodes for Deformable and Semitransparent Displays," *Science* 325:977-981.

(56)

**References Cited****OTHER PUBLICATIONS**

- Park et al. (Web Release Feb. 22, 2009) "Biodegradable Luminescent Porous Silicon Nanoparticles for in Vivo Applications," *Nature Mater.* 8:331-336.
- Parker et al. (2009) "Biocompatible Silk Printed Optical Waveguides," *Adv. Mater.* 21:2411-2415.
- Partial European Search Report dated Sep. 3, 2014, corresponding to European Patent Application No. 13003427.5.
- Patolsky et al. (2006) "Detection, Stimulation, and Inhibition of Neuronal Signals with High-Density Nanowire Transistor Arrays," *Science* 313:1100-1104.
- Patton et al. (Mar. 1998) "Effect of Diamond like Carbon Coating and Surface Topography on the Performance of Metal Evaporated Magnetic Tapes," *IEEE Trans Magn.* 34(2):575-587.
- Paul et al. (Apr. 2003) "Patterning Spherical Surfaces at the Two Hundred Nanometer Scale Using Soft Lithography," *Adv. Func. Mater.* 13(4):259-263.
- Pearson et al. (1999) "GaN: Processing, Defects, and Devices," *J. Appl. Phys.* 86:1-78.
- Peng et al. (Mar. 2, 2000) "Shape Control of CdSe Nanocrystals," *Nature* 404:59-61.
- Perry et al. (2008) "Nano—and Micropatterning of Optically Transparent, Mechanically Robust, Biocompatible Silk Fibroin Films," *Adv. Mater.* 20:3070-3072.
- Piazza et al. (2005) "Protective Diamond-Like Carbon Coatings for Future Optical Storage Disks," *Diamond Relat. Mater.* 14:994-999.
- Pimparkar et al. (Feb. 2007) "Current-Voltage Characteristics of Long-Channel Nanobundle Thin-Film Transistors: A 'Bottom-Up' Perspective," *IEEE Electron Dev. Lett.* 28(2):157-160.
- Podzorov et al. (2005) "Hall Effect in the Accumulation Layers on the Surface of Organic Semiconductors," *Phys. Rev. Lett.* 95:226601.
- Pushpa et al. (2002) "Stars and Stripes. Nanoscale Misfit Dislocation Patterns on Surfaces," *Pure Appl. Chem.* 74(9):1663-1671.
- Qian et al. (2006) "Scaling Effects of Wet Adhesion in Biological Attachment Systems," *Acta Biomaterialia* 2:51-58.
- Quake et al (2000) "From Micro—to Nanofabrication with Soft Materials," *Science* 290:1536-1540.
- Radtke et al. (Feb. 5, 2007) "Laser-Lithography on Non-Planar Surfaces," *Opt. Exp.* 15(3):1167-1174.
- Raman et al. (1989) "Study of Mesa Undercuts Produced in GaAs with H<sub>3</sub>PO<sub>4</sub>-Based Etchants," *J. Electrochem. Soc.* 136:2405-2410.
- Randall et al. (2005) "Permeation-driven flow in poly(dimethylsiloxane) microfluidic devices," *Proc. Nat. Acad. Sci. USA* 102(31):10813-10818.
- Rao et al. (2003) "Large-scale assembly of carbon nanotubes," *Nature*, 425:36-37.
- Razavi et al. (2009) "Three Dimensional Nanopillar Array Photovoltaics on Low Cost and Flexible Substrates," *Nature Materials* 8:648-653.
- Razeghi et al. (1994) "High-Power Laser Diode Based on in GaAs Alloys," *Nature* 369:631-633.
- Razouk et al. (Sep. 1979) "Dependence of Interface State Density on Silicon Thermal Oxidation Process Variables," *J. Electrochem. Soc.* 126(9):1573-1581.
- Reuss et al. (Jul. 2005) "Macroelectronics: Perspectives on Technology and Applications," *Proc. IEEE* 93(7):1239-1256.
- Reuss et al. (Jun. 2006) "Macroelectronics," *MRS Bull.* 31:447-454.
- Ribas et al. (1998) "Bulk Micromachining Characterization of 1.2  $\mu\text{m}$  HEMT MMIC Technology for GaAs MEMS Design," *Mater. Sci. Eng. B* 51:267-273.
- Ridley et al. (1999) "All-Inorganic Field Effect Transistors Fabricated by Printing," *Science* 286:746-749.
- Roberts et al. (1979) "Looking at Rubber Adhesion," *Rubber Chem. Technol.* 52:23-42.
- Roberts et al. (Mar. 2006) "Elastically Relaxed Free-Standing Strained-Silicon Nanomembranes," *Nat. Mater.* 5:388-393.
- Robinson et al. (1983) "GaAs Readied for High-Speed Microcircuits," *Science* 219:275-277.
- Roelkens et al. (Dec. 2005) "Integration of InP/InGaAsP Photodetectors onto Silicon-on-Insulator Waveguide Circuits," *Optics Express* 13(25):10102-10108.
- Rogers et al. (1997) "Using an Elastomeric Phase Mask for Sub-100 nm Photolithography in the Optical Near Field," *Appl. Phys. Lett.* 70:2658-2660.
- Rogers et al. (1998) "Generating ~90 Nanometer Features Using Near Field Contact Mode Photolithography with an Elastomeric Phase Mask," *J. Vac. Sci. Technol.* 16(1):59-68.
- Rogers et al. (1998) "Quantifying Distortions in Soft Lithography," *J. Vac. Sci. Technol.* 16:88-97.
- Rogers et al. (1998) "Using Printing and Molding Techniques to Produce Distributed Feedback and Bragg Reflector Resonators for Plastic Lasers," *Appl. Phys. Lett.* 73:1766-1768.
- Rogers et al. (1999) "Printing Process Suitable for Reel-to-Reel Production of High-Performance Organic Transistors and Circuits," *Adv. Mater.* 11(9):741-745.
- Rogers et al. (2002) "Paper-Like Electronic Displays: Large-Area Rubber-Stamped Plastic Sheets of Electronics and Microencapsulated Electrophoretic Inks," *Proc. Nat. Acad. Sci. USA* 98:4835-4840.
- Rogers et al. (2002) "Printed Plastic Electronics and Paperlike Displays," *J. Polym. Sci. Part A. Polym. Chem.* 40:3327-3334.
- Rogers et al. (Mar. 2000) "Organic Smart Pixels and Complementary Inverter Circuits Formed on Plastic Substrates by Casting and Rubber Stamping," *IEEE Electron Dev. Lett.* 21(3):100-103.
- Rogers, J. (Jul. 9, 2010) "Farewell to Flatland," *Science* 329:138-139.
- Rogers, J.A. (2001) "Rubber Stamping for Plastic Electronics and Fiber Optics," *MRS Bulletin* 26(7):530-534.
- Rogers, J.A. (2001) "Toward Paperlike Displays," *Science* 291:1502-1503.
- Rosenblatt et al. (2002) "High Performance Electrolyte Gated Carbon Nanotube Transistors," *Nano Lett.* 2(8):869-872.
- Rotkin et al. (2003) "Universal Description of Channel Conductivity for Nanotube and Nanowire Transistors," *Appl. Phys. Lett.* 83:1623-1625.
- Roundy et al. (2003) "Photonic Crystal Structure with Square Symmetry within Each Layer and a Three-Dimensional Band Gap," *Appl. Phys. Lett.* 82:3835-3837.
- Rubehn et al. (2009) "A MEMS based Flexible Multichannel ECoG-Electrode Array," *J. Neural Eng.* 6:036003.
- Ruchhoeft et al. (2000) "Optimal Strategy for Controlling Linewidth on Spherical Focal Surface Arrays," *J. Vac. Sci. Technol.* B 18(6):3185-3189.
- Ryu et al. (2009) "Human Cortical Prostheses: Lost in Translation?" *Neurosurg Focus* 27(1):E5.
- Samuelson et al. (2004) "Semiconductor Nanowires for Novel One-Dimensional Devices," *Physica E* 21:560-567.
- Sangwal et al. (1997) "Nature of multilayer steps on the {100} cleavage planes of MgO single crystals," *Surf. Sci.*, 383:78-87.
- Santin et al. (1999) "In vitro Evaluation of the Inflammatory Potential of the Silk Fibroin," *J. Biomed. Mater. Res.* 46:382-389.
- Sanyal et al. (2002) "Morphology of Nanostructures Materials," *Pure Appl. Chem.* 74(9):1553-1570.
- Sazonov et al. (2005) "Low-Temperature Materials and Thin-Film Transistors for Flexible Electronics," *Proc. IEEE* 93:1420-1428.
- Scherlag et al. (1969) "Catheter Technique for Recording His Bundle Activity in Man," *Circulation* 39:13-18.
- Schermer et al. (Web Release Apr. 28, 2005) "Thin-Film GaAs Epitaxial Lift-Off Solar Cells for Space Applications," *Prog. Photovoltaics: Res. Applic.* 13:587-596.
- Schermer et al. (Web Release Jan. 19, 2006) "Photon Confinement in High-Efficiency, Thin-Film III-V Solar Cells Obtained by Epitaxial Lift-Off," *Thin Solid Films* 511-512:645-653.
- Schindl et al. (2003) "Direct Stimulatory Effect of Low-Intensity 670-nm Laser Irradiation on Human Endothelial Cell Proliferation," *Br. J. Dermatol.* 148:334-336.
- Schlegel et al. (2002) "Structures of quartz (1010)—(1011)-water interfaces determined by X-ray reflectivity and atomic force microscopy of natural growth surfaces," *Geochim. Cosmochim. Acta*, vol. 66, No. 17, pp. 3037-3054.

(56)

**References Cited****OTHER PUBLICATIONS**

- Schmid et al. (2003) "Preparation of metallic Films on Elastomeric Stamps and Their Application on Contact Processing and Contact Printing," *Adv. Funct. Mater.* 13:145-153.
- Schmid et al. (Mar. 25, 2000) "Siloxane Polymers for High-Resolution, High-Accuracy Accuracy Soft Lithography," *Macromolecules* 33(8):3042-3049.
- Schmid et al. (May 11, 1998) "Light—Coupling Masks for Lens-less, Sub-wavelength Optical Lithography," *Appl. Phys. Lett.* 72(19):2379-2381.
- Schmidt et al. (Mar. 8, 2001) "Thin Solid Films Roll up into Nanotubes," *Nature* 410:168.
- Schneider et al. (2008) "Mechanical Properties of Silicones for MEMS," *J. Micromech. Microeng.* 18:065008.
- Schon et al. (1995) "Ambipolar Pentacene Field-Effect Transistors and Inverters," *Science* 287:1022-1023.
- Schriber et al. (1998) "The Effectiveness of Silane Adhesion Promotors in the Performance of Polyurethane Adhesives," *J. Adhesion* 68:31-44.
- Scnable et al. (1969) "Aluminum Metallization; Advantages and Limitations for Integrated Circuit Applications," *IEEE* 57:1570-1580.
- Scorzoni et al. (Oct. 4, 2004) "On the Relationship Between the Temperature coefficient of Resistance and the Thermal Conductance of Integrated Metal Resistors," *Sens Actuators A* 116(1):137-144. Search and Examination Report, Corresponding to Singapore Application No. 200904208-6, Mailed Dec. 17, 2010.
- Search Report and Examination Report Corresponding to Singapore Patent Application No. 200901178-4, Completed Mar. 13, 2010.
- Search Report and First Written Opinion, Corresponding to Singapore Patent Application No. 200902530-5, Mailed Jun. 10, 2010.
- Search Report and Written Opinion, Corresponding to Singapore Application No. 200901451-5, Mailed Dec. 22, 2010.
- Search Report Corresponding to Singapore Patent Application No. SG 200607372-0, Mailed Oct. 17, 2007.
- Search Report Corresponding to Taiwanese Patent Application No. 095121212, Completed Oct. 8, 2010.
- Search Report Corresponding to Taiwanese Patent Application No. 100139527, Completed Mar. 21, 2014.
- Search Report, Corresponding to Republic of China (Taiwan) Patent Application No. 094118507, Dated Feb. 24, 2007.
- Second Office Action Corresponding to Chinese Patent Application No. 200780041127.6, Issues May 2, 2012.
- Second Office Action dated Jan. 26, 2015, corresponding to Chinese Patent Application No. 2012101571627.
- Seidel et al. (2004) "High-Current Nanotube Transistors," *Nano Lett.*, vol. 4, No. 5, pp. 831-834.
- Sekitani et al. (2005) "Bending Experiment on Pentacene Field-Effect Transistors on Plastic Films," *Appl. Phys. Lett.* 86:073511.
- Sekitani et al. (2009) "Stretchable Active-Matrix Organic Light-Emitting Diode Display Using Printable Elastic Conductors," *Nature Mater.* 8:494-499.
- Sekitani et al. (Sep. 12, 2008) "A Rubberlike Stretchable Active Matrix Using Elastic Conductors," *Science* 321:1468-1472.
- Sen et al. (2002) "Nonequilibrium Processes for Generating Silicon Nanostructures in Single-Crystalline Silicon," *Pure Appl. Chem.* 74(9):1631-1641.
- Serikawa et al. (May 1, 2000) "High-Mobility Poly-Si Thin Film Transistors Fabricated on Stainless-Steel Foils by Low-Temperature Processes Using Sputter-Depositions," *Jpn. J. Appl. Phys.* 39:L393-L395.
- Servanti et al. (2005) "Functional Pixel Circuits for Elastic AMOLED displays," *Proc. IEEE* 93:1257-1264.
- Service, R.F. (Aug. 15, 2003) "Electronic Textiles Charge Ahead," *Science* 301:909-911.
- Shan et al. (2004) "From Si Source Gas Directly to Positioned, Electrically Contained Si Nanowires: The Self-Assembling 'Grow-in-Place' Approach," *Nano Lett.* 4(11):2085-2089.
- Sharp et al. (2003) "Holographic Photonic Crystals with Diamond Symmetry," *Phys. Rev. B* 68:205102/1-205102/6.
- Sheraw et al. (2002) "Organic Thin-Film Transistor-Driven Polymer-Dispersed Liquid Crystal Displays on Flexible Polymeric Substrates," *Appl. Phys. Lett.* 80:1088-1090.
- Shetty et al. (2005) "Formation and Characterization of Silicon Films on Flexible Polymer Substrates," *Mater. Lett.* 59:872-875.
- Shi et al. (2001) "Free-Standing Single Crystal Silicon Nanoribbons," *J. Am. Chem. Soc.* 123(44):11095-11096.
- Shi et al. (Sep. 2000) "Synthesis of Large Areas of Highly Oriented, Very Long Silicon Nanowires," *Adv. Mater.* 12(18):1343-1345.
- Shin et al. (2003) "PDMS-Based Micro PCr Chip with Parylene Coating," *J. Micromech. Microeng.* 13:768-774.
- Shtein et al. (Oct. 15, 2004) "Direct Mask-Free Patterning of Molecular Organic Semiconductors Using Organic Vapor Jet Printing," *J. Appl. Phys.* 96(8):4500-4507.
- Shull et al. (1998) "Axisymmetric Adhesion Tests of Soft Materials," *Macromol. Chem. Phys.* 199:489-511.
- Siegel et al. (2009) "Thin, lightweight, Foldable Thermochromic Displays on Paper," *Lab Chip* 9:2775-2781.
- Siegel et al. (2010) "Foldable Printed Circuit Boards on Paper Substrates," *Adv. Funct. Mater.* 20:28-35.
- Siegel et al. (Web Release Feb. 7, 2007) "Microsolidics: Fabrication of Three-Dimensional Metallic Microstructures in Poly(dimethylsiloxane)," *Adv. Mater.* 19(5):727-733.
- Sim et al. (1993) "An Analytical Back-Gate Bias Effect Model for Ultrathin SOI CMOS Devices," *IEEE Trans. Elec. Dev.* 40:755-765.
- Sirringhaus et al. (2003) "Inkjet Printing of Functional Materials," *MRS Bull.* 28:802-806.
- Sirringhaus et al. (Dec. 15, 2000) "High-Resolution Inkjet Printing of All-Polymer Transistor Circuits," *Science* 290:2123-2126.
- Sirringhaus, H. (2005) "Device Physics of Solution-Processed Organic Field-Effect Transistors," *Adv. Mater.* 17:2411-2425.
- Smay et al. (2002) "Colloidal Inks for Directed Assembly of 3-D Periodic Structures," *Langmuir* 18:5429-5437.
- Smith et al. (2000) "Electric-Field Assisted Assembly and Alignment of Metallic Nanowires," *Appl. Phys. Lett.* 77(9):1399-1401.
- Snow et al. (2003) "Random networks of carbon nanotubes as an electronic material," *Appl. Phys. Lett.* vol. 82, No. 13, pp. 2145-2147.
- Snow et al. (2005) "High-mobility carbon-nanotube transistors on a polymeric substrate," *Appl. Phys. Lett.*, 86, 033105.
- So et al. (2008) Organic Light-Emitting Devices for Solid-State Lighting, *MRS Bull.* 33:663-669.
- Sofia et al. (2001) "Functionalized Silk-Based Biomaterials for Bone Formation," *J. Biomed. Mater. Res.* 54:139-148.
- Someya et al. (2005) "Conformable, Flexible, Large-Area Networks of Pressure and Thermal Sensors with Organic Transistor Active Matrixes," *Proc. Nat. Acad. Sci. USA* 102:12321-12325.
- Someya et al. (2005) "Integration of Organic FETs with Organic Photodiodes for a Large Area, Flexible, and Lightweight Sheet Image Scanners," *IEEE Trans. Electron Devices* 52:2502-2511.
- Someya et al. (Jul. 6, 2004) "A Large-Area, Flexible, Pressure Sensor Matric with Organic Field-Effect Transistors for Artificial Skin Applications," *Proc. Nat. Acad. Sci. USA* 101(27):9966-9970.
- Someya, T. (Aug. 7, 2008) "Electronic Eyeballs," *Nature* 454:703-704.
- Soole et al. (Mar. 1991) "InGaAs Metal-Semiconductor-Metal Photodetectors for Long Wavelength Optical Communications," *IEEE J. Quantum Electron.* 27(3):737-752.
- Soong et al. (1984) "Adverse Reactions to Virgin Silk Sutures in Cataract Surgery," *Ophthalmology* 91:479-483.
- Srinivasan et al. (Web Release Mar. 26, 2007) "Piezoelectric/Ultrananocrystalline Diamond Heterostructures for High-Performance Multifunctional Micro/Nanoelectromechanical Systems," *Appl. Phys. Lett.* 90:134101.
- Stafford et al. (Aug. 2004) "A Buckling-Based Metrology for Measuring the Elastic Moduli of Polymeric Thin Films," *Nature Mater.* 3:545-550.
- Star et al. (2004) "Nanotube Optoelectric Memory Devices," *Nano Lett.*, vol. 4, No. 9, pp. 1587-1591.
- Stella Project—Stretchable Electronics for Large-Area Applications. Available at [www.stella-project.de](http://www.stella-project.de). Accessed Feb. 8, 2012.
- Storm et al. (Aug. 2003) "Fabrication of Solid-State Nanopores with Single-Nanometre Precision," *Nat. Mater.* 2:537-540.

(56)

**References Cited****OTHER PUBLICATIONS**

- Streetman et al. (2000) "Intrinsic Material," In; *Solid State Electronic Devices*, 5<sup>th</sup> Ed., Prentice Hall; Upper Saddle River, NJ; pp. 74-75.
- Strukov et al. (2005) "CMOL FPGA: A Reconfigurable Architecture for Hybrid Digital Circuits with Two-Terminal Nanodevices," *Nanotechnology* 16:888-900.
- Su et al. (2000) "Lattice-Oriented Growth of Single-Walled Carbon Nanotubes," *J. Phys. Chem. B* 104(28):6505-6508.
- Substantive Examination Adverse Report mailed Sep. 30, 2014, for corresponding Malaysian Patent Application No. PI 20092343.
- Substantive Examination Adverse Report, Corresponding to Malaysian Patent Application No. PI 20090622, Dated Sep. 28, 2012.
- Substantive Examination Adverse Report, Corresponding to Malaysian Patent Application No. PI 20092343, Dated Apr. 30, 2014.
- Substantive Examination Adverse Report, Corresponding to Malaysian Patent Application No. PI 2011004896, Dated Apr. 15, 2014.
- Substantive Examination Clear Report dated Oct. 31, 2014, corresponding to Malaysian Patent Application No. PI 20092343.
- Substantive Examination Clear Report mailed Jun. 13, 2014, for corresponding Malaysian Patent Application No. PI 20052553.
- Substantive Examination Report corresponding to Malaysian Patent Application No. PI 20052553, mailed Jul. 15, 2011.
- Substantive Examination Report corresponding to Malaysian Patent Application No. PI 20094997, mailed Aug. 15, 2012.
- Substantive Examination: Clear Report, Corresponding to Malaysian Patent Application No. PI 20062672, issued May 13, 2011.
- Sum et al. (2009) "Near-Infrared Spectroscopy for the Detection of Lipid Core Coronary Plaques," *Curr. Cardiovasc. Imag. Rep.* 2:307-315.
- Suman et al. (Apr. 2005) "Toward the Ultimate Tribological Interface: Surface Chemistry and Nanotribology of Ultrananocrystalline Diamond," *Adv. Mater.* 17(8):1039-1045.
- Sun et al. (2004) "Fabricating Semiconductor Nano/Microwires and Transfer Printing Ordered Arrays of Them onto Plastic Substrates," *Nano Lett.* 4:1953-1959.
- Sun et al. (2005) "Advances in Organic Field-Effect Transistors," *J. Mater. Chem.* 15:53-65.
- Sun et al. (2005) "Bendable GaAs Metal-Semiconductor Field-Effect Transistors Formed with a Printed GaAs Wire Arrays on Plastic Substrates," *Appl. Phys. Lett.* 87:083501.
- Sun et al. (2005) "Photolithographic Route to the Fabrication of Micro/Nanowires of III-V Semiconductors," *Adv. Fuct. Mater.* 15:30-40.
- Sun et al. (2007) "Controlled Buckling of Semiconductor Nanoribbons for Stretchable Electronics," *Nat. Nanotechnol.* 1:201-207.
- Sun et al. (2007) "Structural Forms of Single Crystal Semiconductor Nanoribbons for High-Performance Stretchable Electronics," *J. Mater. Chem.* 17:832-840.
- Sun et al. (Aug. 2007) "Inorganic Semiconductors for Flexible Electronics," *Adv. Mater.* 19(15):1897-1916.
- Sun et al. (Nov. 2006) "Buckled and Wavy Ribbons of GaAs for High-Performance Electronics on Elastomeric Substrates," *Adv. Mater.* 18(21):2857-2862.
- Sundar et al. (2004) "Elastomeric Transistor Stamps: Reversible Probing of Charge Transport in Organic Crystals," *Science* 303:1644-1646.
- Suo et al. (Feb. 22, 1999) "Mechanics of Rollable and Foldable Film-on-Foil Electronics," *Appl. Phys. Lett.* 74(8):1177-1179.
- Supplementary European Search Report. Corresponding to European Application No. EP 09 71 6695, Mailed Jun. 26, 2012.
- Supplementary European Search Report corresponding to European Patent Application No. 05 75 5193, completed Mar. 1, 2011.
- Supplementary European Search Report Corresponding to European Patent Application No. 07 84 1968, Completed Mar. 31, 2011.
- Supplementary European Search Report, Corresponding to European Application No. 04 81 2651, Completed Oct. 19, 2010.
- Supplementary European Search Report, Corresponding to European Application No. 05 75 6327, Completed Sep. 25, 2009.
- Swain et al. (2004) "Curved CCD Detector Devices and Arrays for Multi-Spectral Astrophysical Application and Terrestrial Stereo Panoramic Cameras," *Proc. SPIE* 5499:281-301.
- Sze et al. (1985) *Semiconductor Devices, Physics and Technology*, 2<sup>nd</sup> ed., Wiley, New York, pp. 190-192.
- Sze, S. (1985) *Semiconductor Devices: Physics and Technology*, New York: Wiley, pp. 428-467.
- Sze, S. (1988) *VLSI Technology*, McGraw-Hill, 327-374, 566-611.
- Sze, S. (1994) *Semiconductor Sensors*, John Wiley and Sons: New York, pp. 17-95.
- Takamoto et al. (Jan. 20, 1997) "Over 30% Efficient InGaP/GaAs Tandem Solar Cells," *Appl. Phys. Lett.* 70(3):381-383.
- Talapin et al. (Oct. 7, 2005) "PbSe Nanocrystal Solids for n—and p-Channel Thin Film Field-Effect Transistors," *Science* 310:86-89.
- Tan et al. (Apr. 12, 2004) "Performance Enhancement of InGaN Light Emitting Diodes by Laser-Lift-off and Transfer from Sapphire to Copper Substrate," *Appl. Phys. Lett.* 84(15):2757-2759.
- Tanase et al. (2002) "Magnetic Trapping and Self-Assembly of Multicomponent Nanowires," *J. Appl. Phys.* 91:8549-8551.
- Tang et al. (2005) "One-Dimensional Assemblies of Nanoparticles: Preparation, Properties, and Promise," *Adv. Mater.* 17:951-962.
- Tao et al. (2003) "Langmuir-Blodgett Silver Nanowire Monolayers for Molecular Sensing Using Surface-Enhanced Raman Spectroscopy," *Nano Lett.* 3:1229-1233.
- Tate et al. (2000) "Anodization and Microcontact Printing on Electroless Silver: Solution-Based Fabrication Procedures for Low-Voltage Electronic Systems with Organic Active Components," *Langmuir* 16:6054-6060.
- Teshima et al. (2001) "Room-Temperature Deposition of High-Purity Silicon Oxide Films by RF Plasma-Enhanced CVD," *Surf. Coat. Technol.* 146-147:451-456.
- Theiss et al. (1998) "PolySilicon Thin Film Transistors Fabricated at 100° C. on a Flexible Plastic Substrate," *IEDM* 98:257-260.
- Thornwood et al. (Oct. 1, 1990) "Utilizing Optical Lithography in the Sub-Micron Dimensional Regime," *IBM Tech. Disc. Bull.* 33(5):187-188.
- Timko et al. (2009) "Electrical Recording from Hearts with Flexible Nanowire Device Arrays," *Nano Lett.* 9:914-918.
- Toader et al. (2004) "Photonic Band Gap Architectures for Holographic Lithography," *Phys. Rev. Lett.* 043905/1-043905/4.
- Toader et al. (2004) "Photonic Band Gaps Based on Tetragonal Lattices of Slanted Pores," *Phys. Rev. Lett.* 90:233901/1-233901/4.
- Tong (1999) *Semiconductor Wafer Bonding: Science and Technology*, John Wiley; New York, pp. 187-221.
- Trau et al. (1997) "Microscopic Patterning of Orientated Mesoscopic Silica Through Guided Growth," *Nature* 390:674-676.
- Trentler et al. (1995) "Solution-Liquid-Solid Growth of Crystalline III-V Semiconductors: An Analogy to Vapor-Liquid-Solid Growth," *Science* 270:1791-1794.
- Tseng et al. (Web Release Dec. 19, 2003) "Monolithic Integration of Carbon Nanotube Devices with Silicon MOS Technology" *Nano Lett.* 4(1):123-127.
- Uejikoga, S. (2002) "Low-Temperature Polycrystalline Silicon Thin-Film Transistor Technologies for System-on-Glass Displays," *MRS Bull.* 27:881-.
- Urruchi et al. (2000) "Etching of DLC Films Using a Low Intensity Oxygen Plasma Jet," *Diamond Relat. Mater.* 9:685-688.
- Vanfleteren, Sweet: Stretchable and Washable Electronics for Embedding Textiles. Available at [ftp://ftp.cordis.europa.eu/pub/ist/docs/mnd/ws-sfit\\_en.pdf](http://ftp.cordis.europa.eu/pub/ist/docs/mnd/ws-sfit_en.pdf). Accessed Feb. 8, 2012.
- Vanhollenbeke et al. (2000) "Compliant Substrate Technology: Integration of Mismatched Materials for Opto-Electronic Applications," *Prog. Cryst. Growth Charact. Mater.* 41(1-4):1-55.
- Velev et al. (1997) "Porous silica via colloidal crystallization," *Nature* 389:447-448.
- Vepari et al. (Aug. Sep. 2007) "Silk as a Biomaterial," *Prog. Polym. Sci.* 32(8-9):991-1007.
- Vilan et al. (2000) "Molecular Control Over Au/GaAs Diodes," *Nature* 404:166-168.
- Vinck et al. (2003) "Increased Fibroblast Proliferation Induced by Light Emitting Diode and Low Power Laser Irradiation," *Lasers Med. Sci.* 18:95-99.

(56)

**References Cited****OTHER PUBLICATIONS**

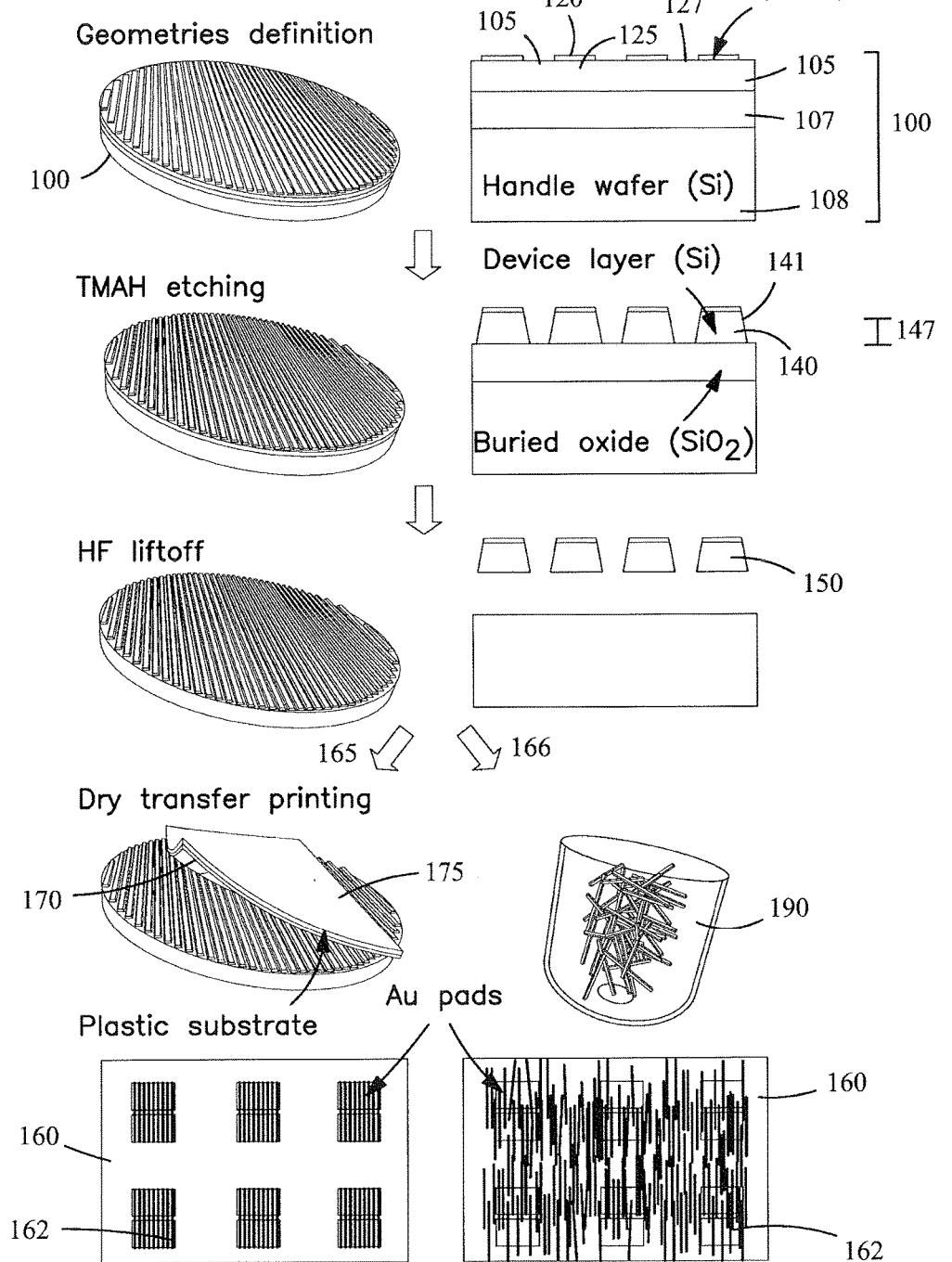
- Viventi et al. (Mar. 2010) "A Conformal, Bio-Interfaced Class of Silicon Electronics for Mapping Cardiac Electrophysiology," *Sci. Transl. Med.* 2(24):24ra22.
- Vlasov et al. (2001) "On-Chip Natural Assembly of Silicon Photonic Bandgap Crystals," *Nature* 414:289-293.
- Voss, D. (2000) "Cheap and Cheerful Circuits," *Nature* 407:442-444.
- Wagner et al. (2003) "Silicon for Thin-Film Transistors," *Thin Solid Films* 430:15-19.
- Wagner et al. (2005) "Electronic Skin: Architecture and Components," *Physica E* 25:326-334.
- Wagner et al. (Mar. 1, 1964) "Vapor-Liquid-Solid Mechanism of Single Crystal Growth," *Appl. Phys. Lett.* 4(5):89-90.
- Waksman et al. (2008) "Photopoint Photodynamic Therapy Promotes Stabilization of Atherosclerotic Plaques and Inhibits Plaque Progression," *J. Am. Coll. Cardiol.* 52:1024-1032.
- Wang et al. (2003) "A Solution-Phase, Precursor Route to Polycrystalline SnO<sub>2</sub> Nanowires that can be Used for Gas Sensing under Ambient Conditions," *J. Am. Chem. Soc.* 125:16176-16177.
- Wang et al. (2005) "Electronically Selective Chemical Functionalization of Carbon Nanotubes: Correlation between Raman Spectral and Electrical Responses," *J. Am. Chem. Soc.*, 127:11460-11468.
- Wang et al. (2005) "Oxidation Resistant Germanium Nanowires: Bulk Synthesis, Long Chain Alkanethiol Functionalization, and Langmuir-Blodgett Assembly," *J. Am. Chem. Soc.* 127(33):11871-11875.
- Wang et al. (2006) "Direct Synthesis and Characterization of CdS Nanobelts," *Appl. Phys. Lett.* 89:033102.
- Wang et al. (Aug-Sep. 2008) "In Vivo Degradation of Three-Dimensional Silk Fibroin Scaffolds," *Biomaterials* 29(24-25):3415-3428.
- Waxman et al. (2009) "In vivo Validation of a Catheter-Based Near-Infrared Spectroscopy System for Detection of Lipid Core Coronary Plaques: Initial Results of the Spectacl Study," *J. Am. Coll. Cardiol. Img.* 2:858-868.
- Waxman, S. (2008) "Near-Infrared Spectroscopy for Plaque Characterization," *J. Interv. Cardiol.* 21:452-458.
- Weber et al. (Jan. 2004) "A Novel Low-Cost, High Efficiency Micromachined Silicon Solar Cell," *IEEE Electron Device Lett.* 25(1):37-39.
- Wen et al. (Web Release Dec. 4, 2004) "Controlled Growth of Large-Area, Uniform, Vertically Aligned Arrays of a-Fe<sub>2</sub>O<sub>3</sub> Nanobelts and Nanowires," *J. Phys. Chem. B* 109(1):215-220.
- Whang et al. (2003) "Large-Scale Hierarchical Organization of Nanowire Arrays for Integrated Nanosystems," *Nano Lett.* 3(9):1255-1259.
- Williams et al. (Oct. 2006) "Growth and Properties of Nanocrystalline Diamond Films," *Phys. Stat. Sol. A* 203(13):3375-3386.
- Williams et al. (Web Release Jan. 23, 2006) "Comparison of the Growth and Properties of Ultrananocrystalline Diamond and Nanocrystalline Diamond," *Diamond Relat. Mater.* 15:654-658.
- Willner et al. (2002) "Functional Nanoparticle Architectures for Senoric, Optoelectronic, and Bioelectronic Applications," *Pure Appl. Chem.* 74(9):1773-1783.
- Wilson et al. (2006) "EECoG Factors Underlying Multimodal Control of a Brain—Computer Computer Interface," *IEEE Trans. Neural Syst. Rehabil. Eng.* 14:246-250.
- Wind et al. (May 20, 2002) "Vertical Scaling of Carbon Nanotube-Field-Effect Transistors Using Top Gate Electrodes," *Appl. Phys. Lett.* 80(20):3871-3819.
- Wise et al. (Jul. 2008) "Microelectrodes, Microelectronics, and Implantable Neural Microsystems," *Proc. IEEE* 96(7):1184-1202.
- Won et al. (2004) "Effect of Mechanical and Electrical Stresses on the Performance of an a-Si:H TFT on Plastic Substrate," *J. Electrochem. Soc.* 151:G167-G170.
- Wong-Riley et al. (2005) "Photobiomodulation Directly Benefits Primary Neurons Functionally Inactivated by Toxins," *J. Biol. Chem.* 280:4761-4771.
- Woodburn et al. (1996) "Phototherapy of Cancer and Atheromatous Plaque with Texaphyrins," *J. Clin. Laser Med. Surg.* 14:343-348.
- Wu et al. (2001) "Amorphous Silicon Crystallization and Polysilicon Thin Film Transistors on SiO<sub>2</sub> Passivated Steel Foil Substrates," *Appl. Surf. Sci.* 175-176:753-758.
- Wu et al. (2001) "Direct Observation of Vapor-Liquid-Solid Nanowire Growth," *J. Am. Chem. Soc.* 123(13):3165-3166.
- Wu et al. (2001) "Thermal Oxide of Polycrystalline Silicon on Steel Foil as a Thin-Film Transistor Gate Dielectric," *Appl. Phys. Lett.* 78:3729-3731.
- Wu et al. (2002) "Block-by-Block Growth of Single-Crystalline Si/SiGe Superlattice Nanowires," *Nano Lett.* 2(2):83-86.
- Wu et al. (2002) "Growth of Au-Catalyzed Ordered GaAs Nanowire Arrays by Molecular-Beam Epitaxy," *Appl. Phys. Lett.* 81:5177-5179.
- Wu et al. (2002) "Inorganic Semiconductor Nanowires: Rational Growth, Assembly, and Novel Properties," *Chem. Eur. J.* 8(6):1261-1268.
- Wu et al. (2003) "Growth, Branching, and Kinking of Molecular-Beam Epitaxial (110) GaAs Nanowires," *Appl. Phys. Lett.* 83:3368-3370.
- Wu et al. (Jul. 1, 2004) "Single-Crystal Metallic Nanowires and Metal/Semiconductor Nanowire Heterostructures," *Nature* 430:61-65.
- Wu et al. (Nov. 2002) "Complementary Metal-Oxide-Semiconductor Thin-Film Transistor Circuits from a High-Temperature Polycrystalline Silicon Process on Steel Foil Substrates," *IEEE Trans. Electr. Dev.* 49(11):1993-2000.
- Xia (1998) "Soft Lithography" *Angew. Chem. Int. Ed.* 37:551-575.
- Xia et al. (1996) "Shadowed Sputtering of Gold on V-Shaped Microtrenches Etched in Silicon and Applications in Microfabrication," *Adv. Mater.* 8(9):765-768.
- Xia et al. (1998) "Soft Lithography," *Annu. Rev. Mater. Sci.* 28:153-184.
- Xia et al. (1999) "Unconventional Methods for Fabricating and Patterning Nanostructures," *Chem. Rev.* 99:1823-1848.
- Xia et al. (2003) "One-Dimensional Nanostructures: Synthesis, Characterization and Applications," *Adv. Mater.* 15:353-389.
- Xia et al. (Jul. 19, 1996) "Complex Optical Surfaces Formed by Replica Molding Against Elastomeric Masters," *Science* 273:347-349.
- Xiang et al. (Mar. 25, 2006) "Ge/Si Nanowire Heterostructures as High-Performance Field-Effect Transistors," *Nature* 441:489-493.
- Xiao et al. (2003) "High-mobility thin-film transistors based on aligned carbon nanotubes," *Appl. Phys. Lett.*, vol. 83, No. 1, pp. 150-152.
- Xie et al. (May 2003) "Polymer-Controlled Growth of Sb<sub>2</sub>Se<sub>3</sub> Nanoribbons Via a Hydrothermal Process," *J. Cryst. Growth* 252(4):570-574.
- Xin et al. (Jun. 2005) "Evaluation of Polydimethylsiloxane Scaffolds with Physiologically-Relevant Elastic Moduli: Interplay of Substrate Mechanics and Surface Chemistry Effects on Vascular Smooth Muscle Cell Response," *Biomaterials* 26(16):3123-3129.
- Yang et al. (1997) "Mesoporous Silica with Micrometer-Scale Designs," *Adv. Mater.* 9:811-814.
- Yang et al. (2000) "Stability of Low-Temperature Amorphous Silicon Thin Film Transistors Formed on Glass and Transparent Plastic Substrates," *J. Vac. Sci. Technol. B* 18:683-689.
- Yang et al. (2002) "Creating Periodic Three-Dimensional Structures by Multibeam Interface of Visible Laser," *Chem. Mater.* 14:2831-2833.
- Yang et al. (Dec. 2007) "RFID Tag and RF Structures on a Paper Substrate Using Inkjet-Printing Technology," *IEEE Trans. Microw. Theory Tech.* 55(12):2894-2901.
- Yang, P. (2005) "The Chemistry and Physics of Semiconductor Nanowires," *MRS Bull.* 30:85-.
- Yanina et al. (2002) "Terraces and ledges on (001) spinel surfaces," *Surf. Sci.*, 513:L402-L412.
- Yao et al. (2008) "Seeing Molecules by Eye: Surface Plasmon Resonance Imaging at Visible Wavelengths with High Spatial Resolution and Submonolayer Sensitivity," *Angew. Chem.* 47:5013-5017.

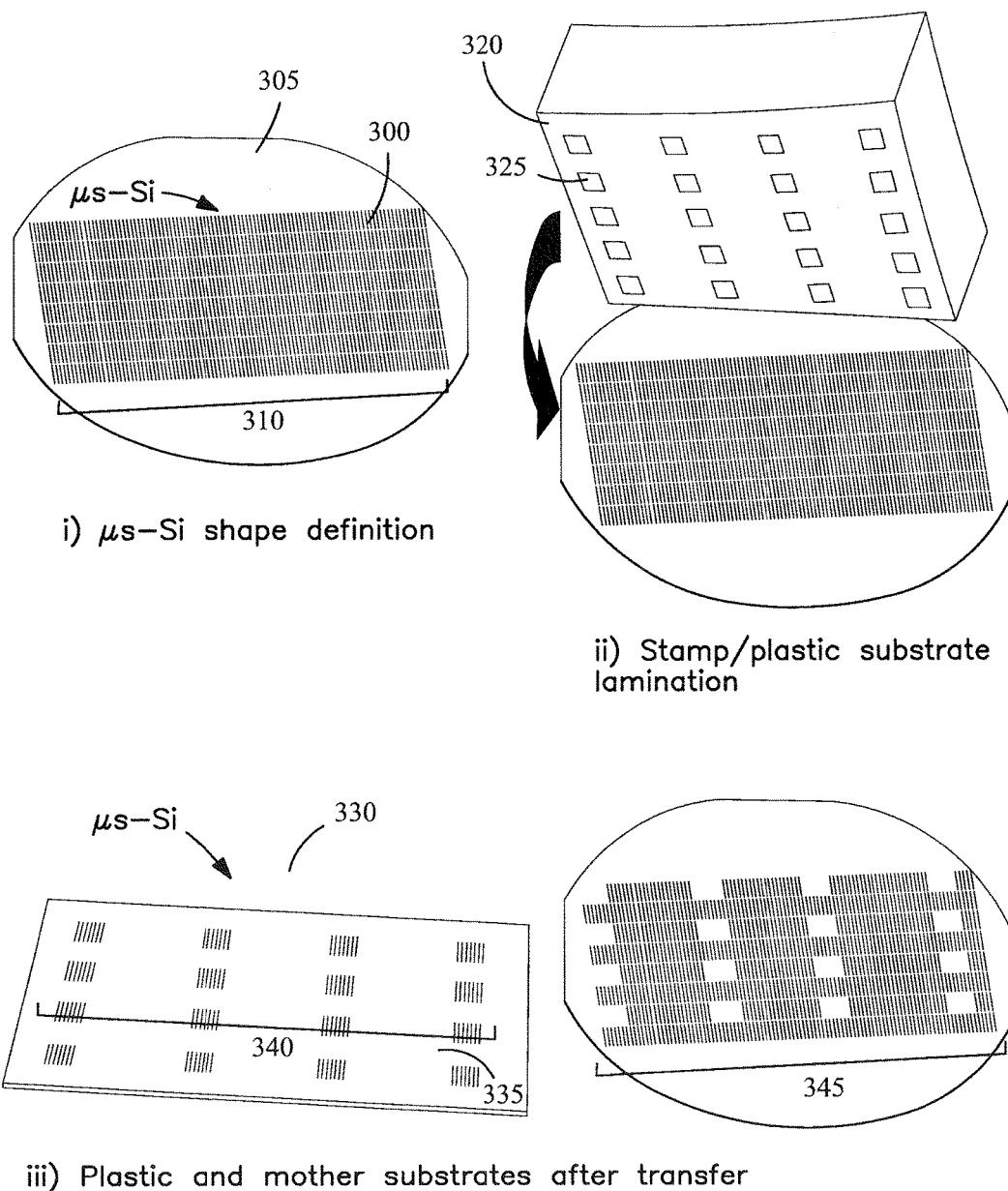
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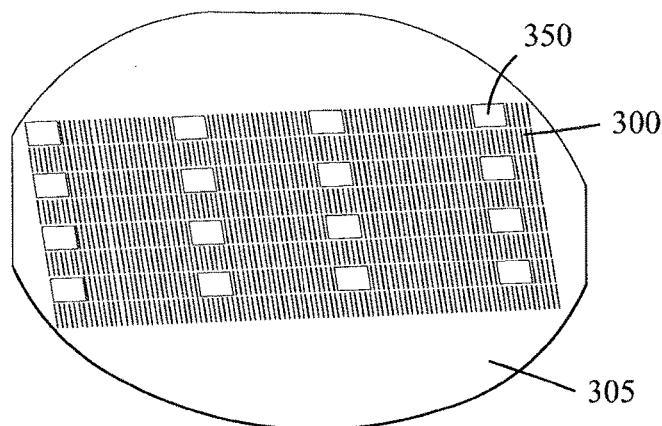
**References Cited****OTHER PUBLICATIONS**

- Yao et al. (2010) "Functional Nanostructured Plasmonic Materials," *Adv. Mater.* 22:1102-1110.
- Yao et al. (Mar. 2000) "High-Field Effect Electrical Transport in Single-Walled Carbon Nanotubes," *Phys. Rev. Lett.* 84(13):2941-2944.
- Yeager et al. (Aug. 30, 2008) "Characterization of Flexible ECoG Electrode Arrays for Chronic Recording in Awake Rats," *J. Neurosci. Methods* 173(2):279-285.
- Yeh et al. (1994) "Fluidic Self-Assembly for the Integration of GaAs Light Emitting Diodes on Si Substrates," *IEEE Photon. Technol. Lett.* 6:706-708.
- Yin et al. (2000) "A Soft Lithography Approach to the Fabrication of Nanostructures of Single Crystalline Silicon with Well-Defined Dimensions and Shapes," *Adv. Mater.* 12: 1426-1430.
- Yin et al. (2005) "Colloidal Nanocrystal Synthesis and the Organic-Inorganic Interface," *Nature* 437:664-670.
- Yoon et al. (2005) "Low-Voltage Organic Field-Effect Transistors and Inverters Enabled by Ultrathin Cross-Linked Polymers as Gate Dielectrics," *J. Am. Chem. Soc.* 127:10388-10395.
- Yu et al. (2000) "Silicon Nanowires: Preparation, Device Fabrication, and Transport Properties," *J. Phys. Chem. B* 104(50):11864-11870.
- Yu et al. (2003) "Solution-Liquid-Solid Growth of Soluble GaAs Nanowires," *Adv. Mater.* 15:416-419.
- Yu et al. (2003) "Two-Versus Three-Dimensional Quantum Confinement in Indium Phosphide Wires and Dots," *Nat. Mater.* 2:517-520.
- Yu et al. (2004) "The Yield Strength of Thin Copper Films on Kapton," *J. Appl. Phys.* 95:2991-2997.
- Yuan et al. (2006) "High-Speed Strained-Single-Crystal-Silicon Thin-Film Transistors on Flexible Polymers," *J. Appl. Phys.* 100:013708.
- Yurelki et al. (Jul. 24, 2004) "Small-Angle Neutron Scattering from Surfactant-Assisted Aqueous Dispersions of Carbon Nanotubes," *J. Am. Chem. Soc.* 126(32):9902-9903.
- Zakhidov et al. (1998) "Carbon Structure with Three-Dimensional Periodicity at Optical Wavelengths," *Science* 282:897-901.
- Zaumseil et al. (2003) "Nanoscale Organic Transistors that use Source/Drain Electrodes Supported by High Resolution Rubber Stamps," *Appl. Phys. Lett.* 82(5):793-795.
- Zaumseil et al. (2003) "Three-Dimensional and Multilayer Nanostructures Formed by Nanotransfer Printing," *Nano Lett.* 3(9):1223-1227.
- Zhang et al. (2001) "Electric-field-directed growth of aligned single-walled carbon nanotubes," *Appl. Phys. Lett.*, vol. 79, No. 19, pp. 3155-3157.
- Zhang et al. (2005) "Low-Temperature Growth and Photoluminescence Property of ZnS Nanoribbons," *J. Phys. Chem. B* 109(39):18352-18355.
- Zhang et al. (2006) "Anomalous Coiling of SiGe/Si and SiGe/Si/Cr Helical Nanobelts," *Nano Lett.* 6(7):1311-1317.
- Zhang et al. (Apr. 2003) "Oxide-Assisted Growth of Semiconducting Nanowires," *Adv. Mater.* 15(7-8):635-640.
- Zhang et al. (Apr. 5, 2004) "Structure and Photoluminescence of ZnSe Nanoribbons Grown by Metal Organic Chemical Vapor Deposition," *Appl. Phys. Lett.* 84(14):2641-2643.
- Zhang et al. (Feb. 9, 2006) "Electronic Transport in Nanometre-Scale Silicon-on-Insulator Membranes," *Nature* 439:703-706.
- Zhao et al. (Mar. 2007) "Improved Field Emission Properties from Metal-Coated Diamond Films," *Diamond Relat Mater.* 16(3):650-653.
- Zheng et al. (1998) "Sudden Cardiac Death in the United States, 1989 to 1998," *Circulation* 104, 2158-2163.
- Zheng et al. (2004) "Shape-and Solder-Directed Self-Assembly to Package Semiconductor Device Segments," *Appl. Phys. Lett.* 85:3635-3637.
- Zheng et al. (Aug. 31, 2004) "Sequential Shape-and-Solder-Directed Self Assembly of Functional Microsystems," *Proc. Natl. Acad. Sci. USA* 101(35):12814-12817.
- Zhou et al. (2002) "An Efficient Two-Photon-Generated Photoacid Applied to Positive-Tone 3D Microfabrication," *Science* 296:1106-1109.
- Zhou et al. (2004) "p-Channel, n-Channel Thin Film Transistors and p-n Diodes Based on Single Wall Carbon Nanotube Networks," *Nano Lett.* 4:2031-2035.
- Zhou et al. (2005) "Band Structure, Phonon Scattering, and the Performance Limit of Single-Walled Carbon Nanotube Transistors," *Phys. Rev. Lett.* 95:146805.
- Zhou et al. (2005) "Mechanism for Stamp Collapse in Soft Lithography," *Appl. Phys. Lett.* 87:251925.
- Zhu et al. (2005) "Spin on Dopants for High-Performance Single Crystal Silicon Transistors on Flexible Plastic Substrates," *Appl. Phys. Lett.* 86(133507)1-3.
- Zipes et al. (2006) "ACC/AHA/ESC 2006 Guidelines for Management of Patients With Ventricular Arrhythmias and the Prevention of Sudden Cardiac Death: A Report of the American College of Cardiology/American Heart Association Task Force and the European Society of Cardiology Committee for Practice Guidelines (Writing Committee to Develop Guidelines for Management of Patients With Ventricular Arrhythmias and the Prevention of Sudden Cardiac Death)," *Circulation* 114:385-484.
- Office Action corresponding to European Patent Application No. 13003427.5, issued Jan. 2, 2017, 4 pages.
- Second Office Action dated Dec. 30, 2016, for Chinese Patent Application No. 201310435963X, including English translation.
- Examination Report (Communication pursuant to Article 94(3) EPC) dated Apr. 29, 2016, for European Patent Application No. 13003426.7.
- Substantive Examination Clear Report dated Jan. 31, 2017, for Malaysian Patent Application No. PI2011004896.
- Office Action corresponding to European Patent Application No. 13003428.3, issued Nov. 7, 2016, 4 pages.
- Office action corresponding to European Patent Application No. 05755193.9, issued Nov. 11, 2016, 5 pages.
- Notice of Reasons for Rejection dated May 30, 2017, corresponding to Japanese Patent Application No. P2016-172185 (including English translation).
- First Office Action dated May 22, 2017, for Chinese Patent Application No. 201410647568.2 (including English translation).

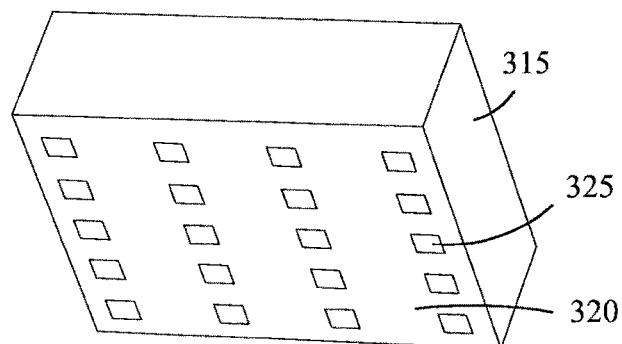
\* cited by examiner

**Fig.1**

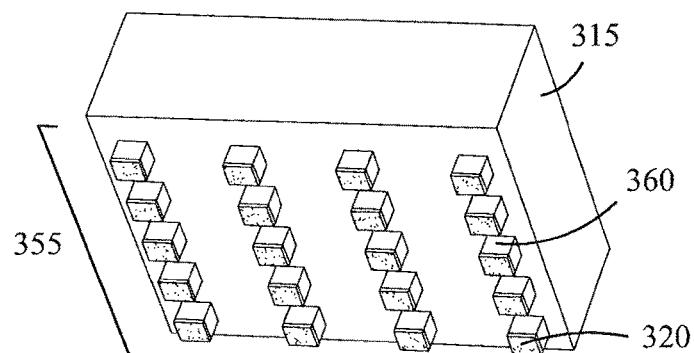
**Fig.2**

**Fig.3A**

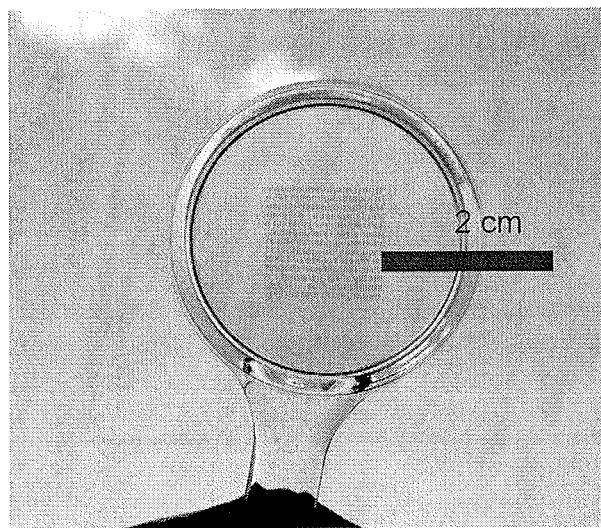
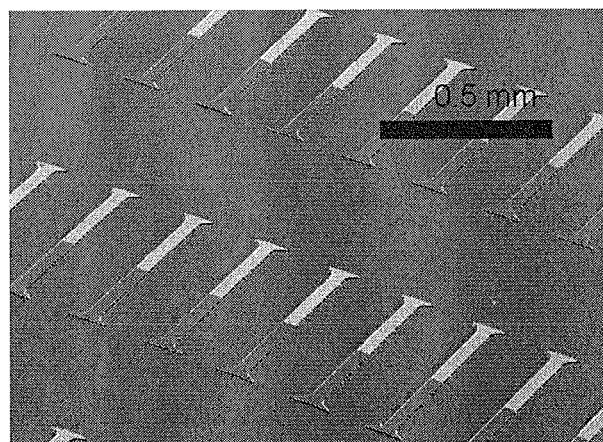
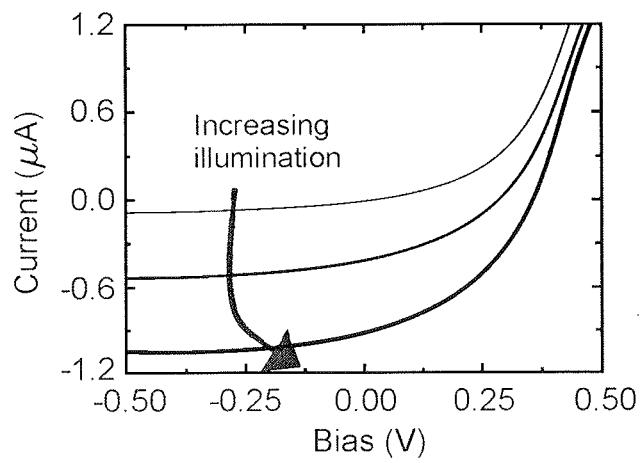
a) Selective coating of the mother substrate with an adhesive material

**Fig.3B**

b) Flat stamp (or plastic substrate) selectively coated with an adhesive

**Fig.3C**

c) Structured stamp inked with an adhesive

**Fig. 3D****Fig. 3E****Fig. 3F**

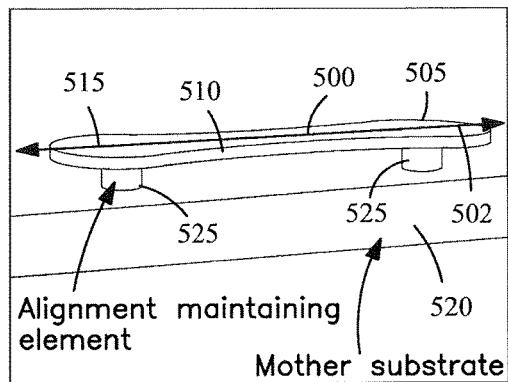
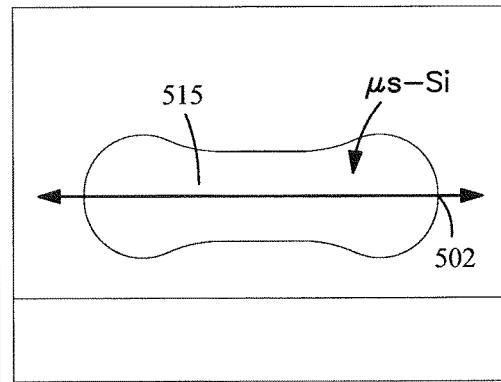
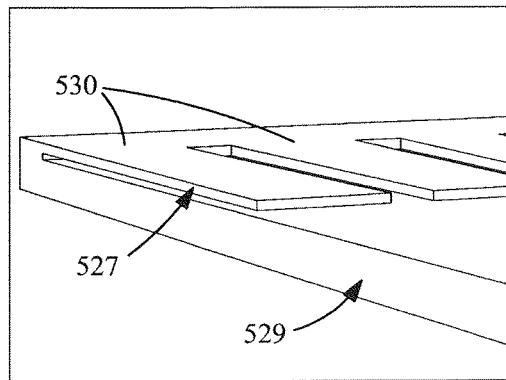
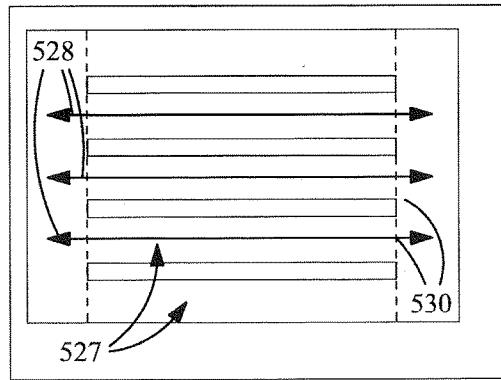
**Fig.4A1****Fig.4A2****Fig.4B1****Fig.4B2**

Fig. 5A

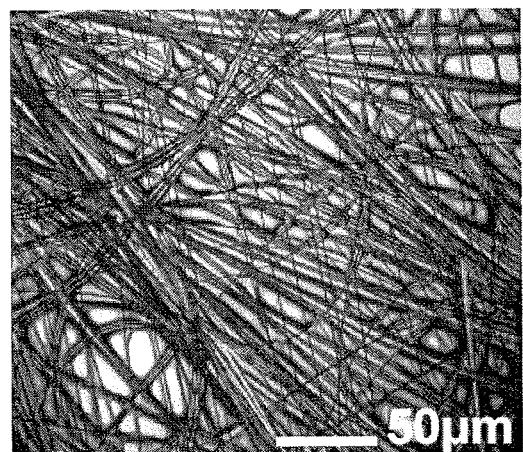


Fig. 5B

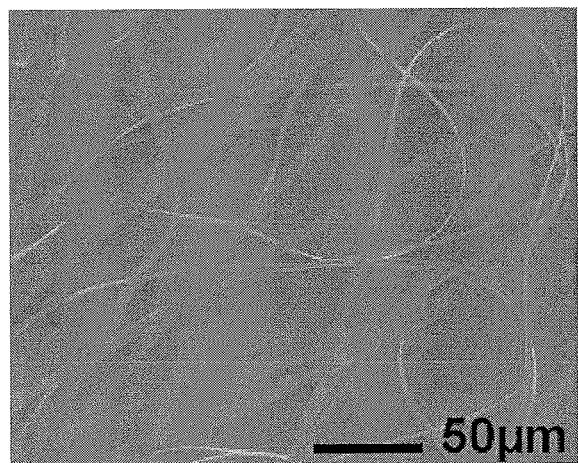
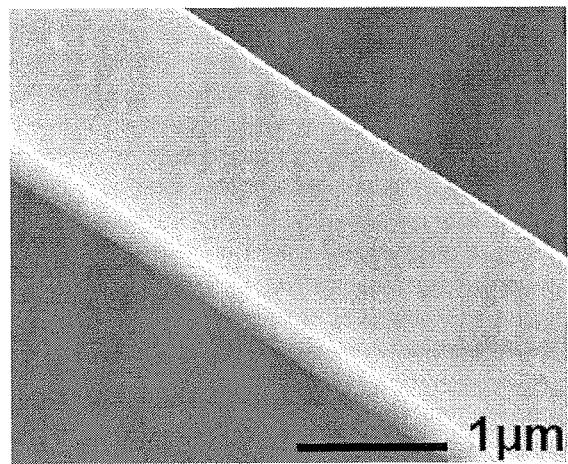


Fig. 5C



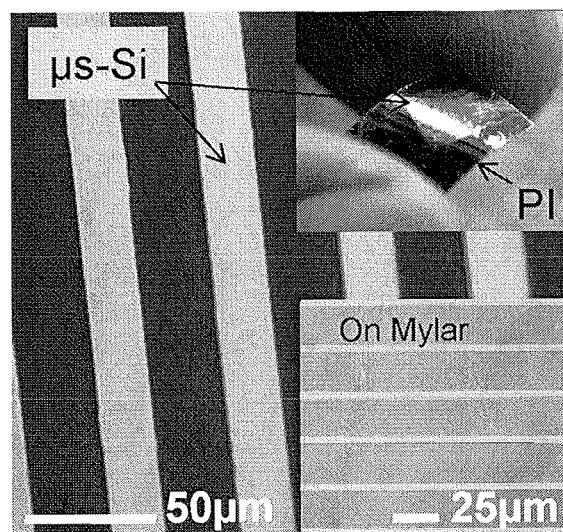
**Fig. 6**

Fig. 7

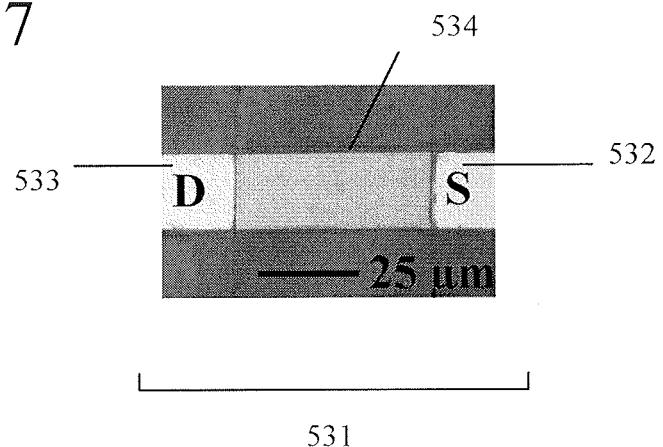


Fig. 8

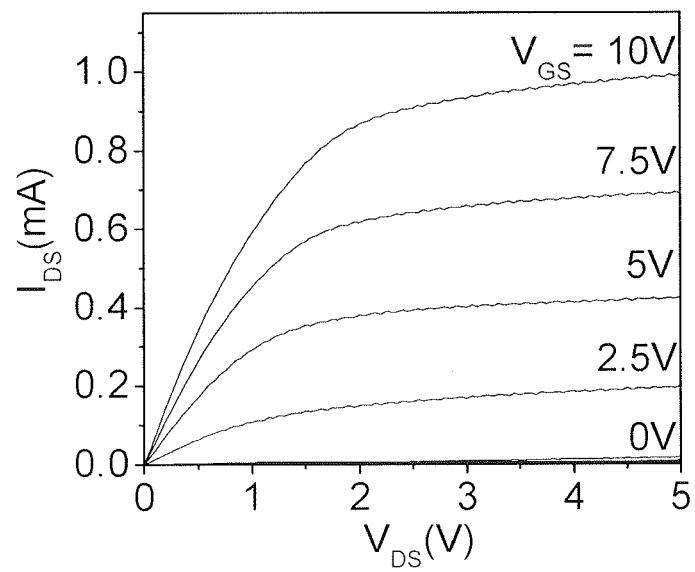
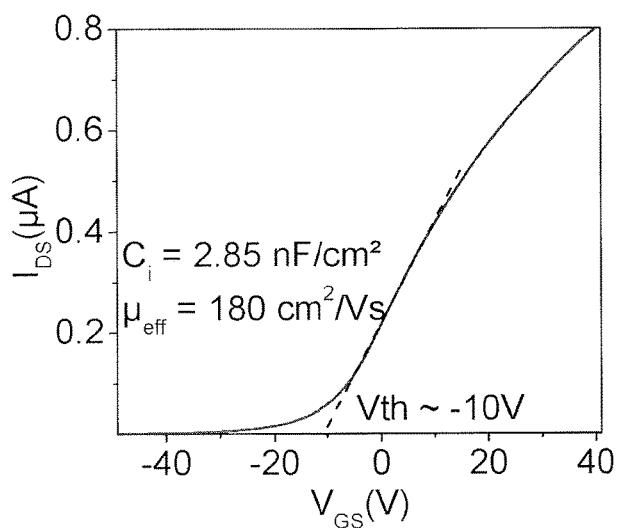
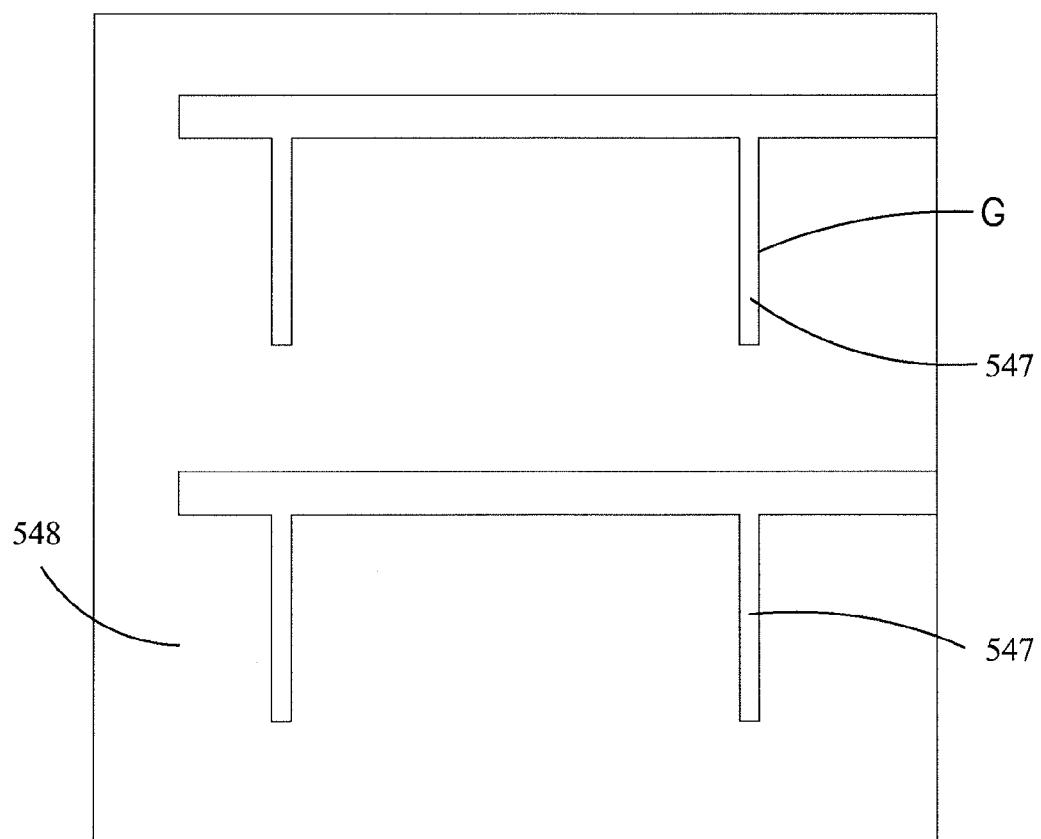
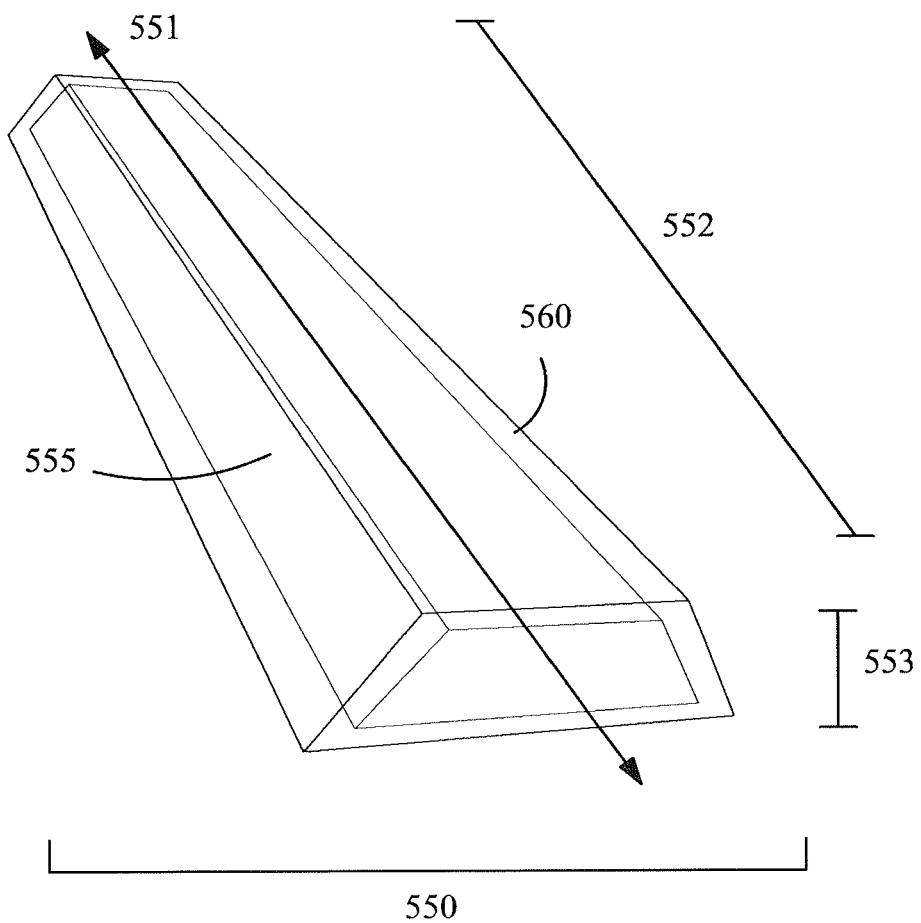
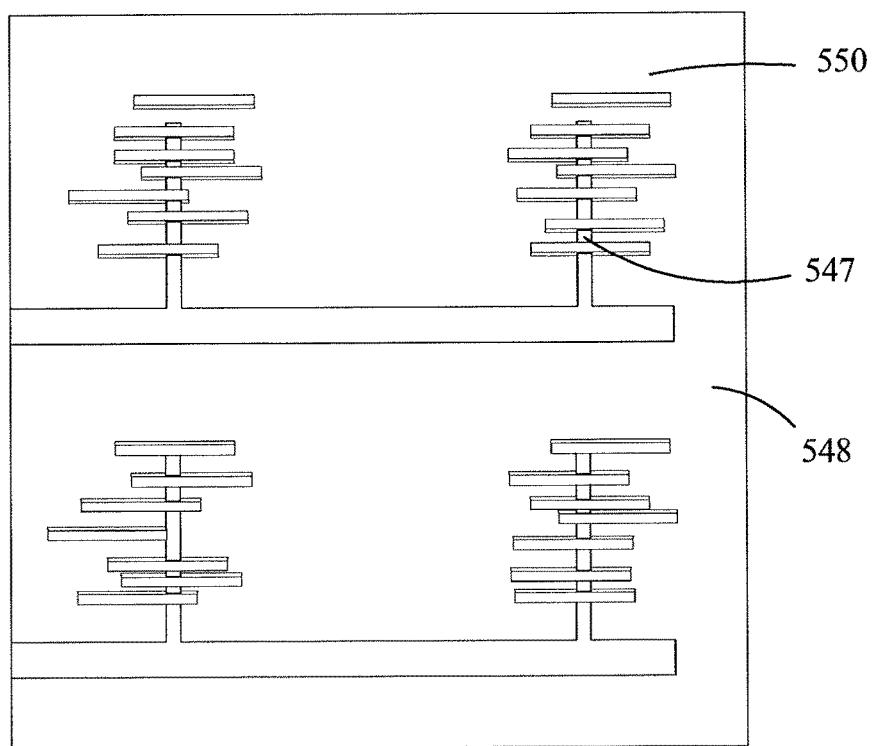


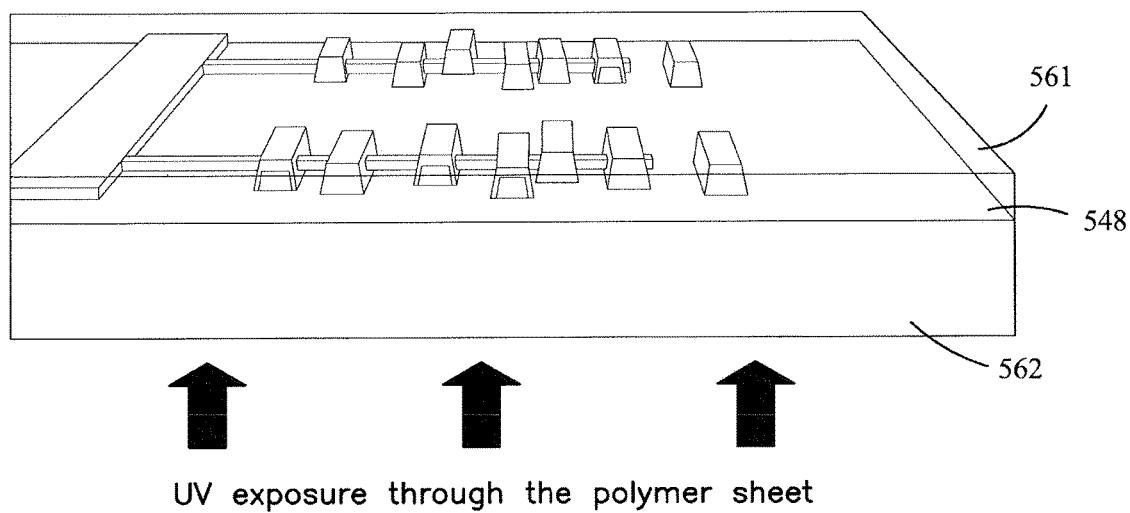
Fig. 9

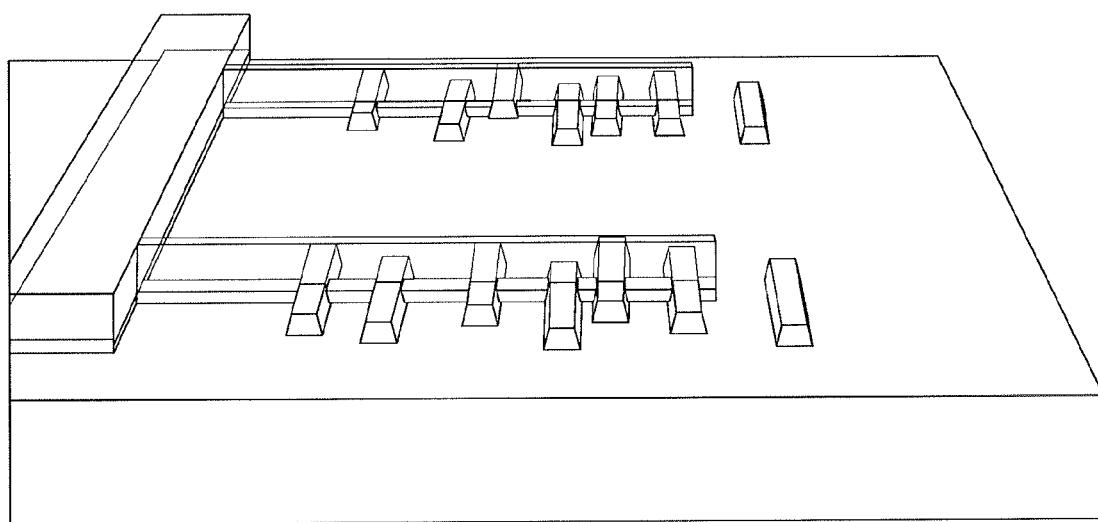


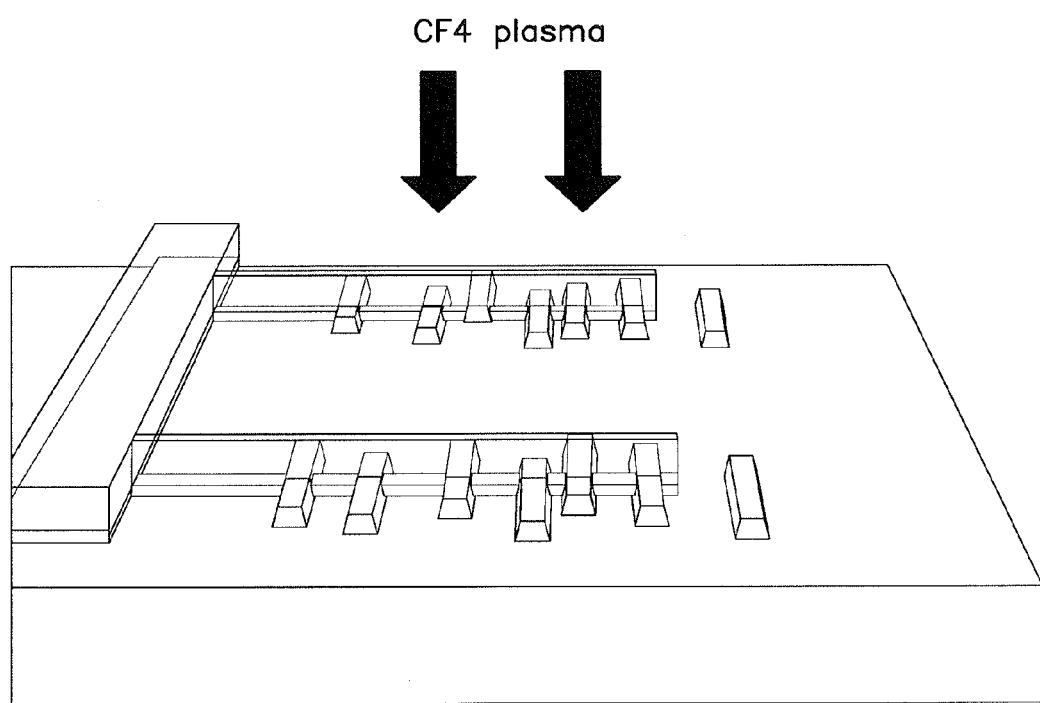
**Fig.10A**

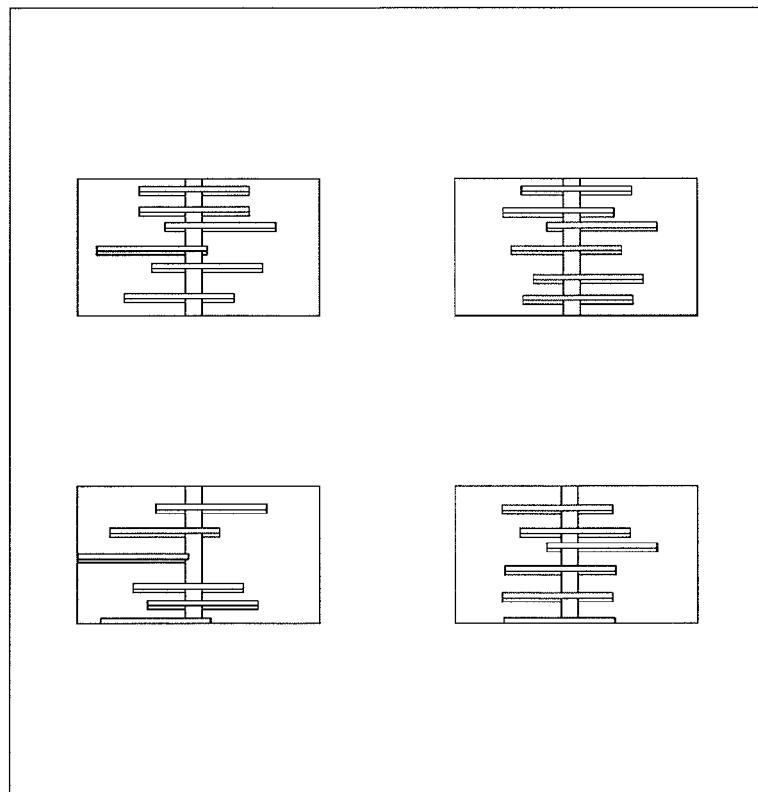
**Fig.10B**

**Fig.10C**

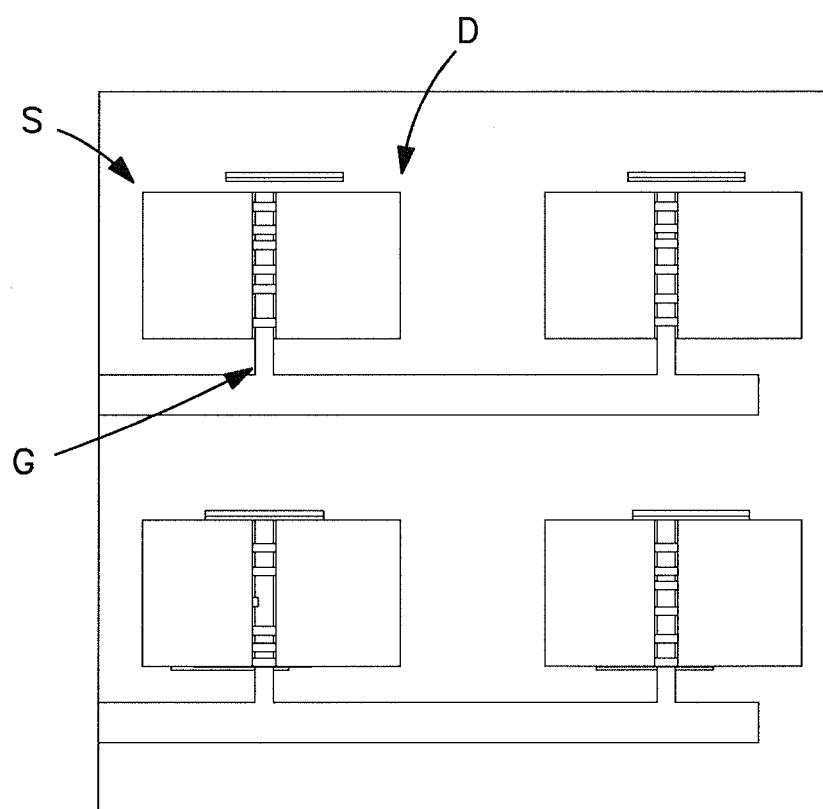
**Fig.10D**

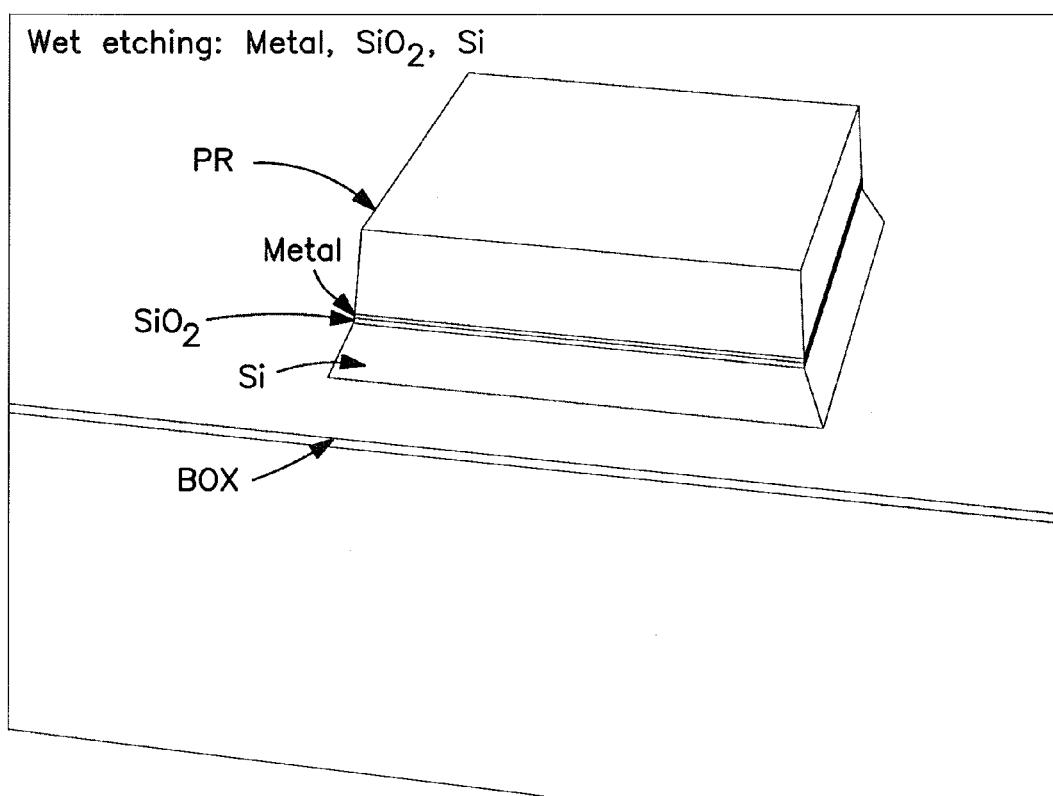
**Fig.10E**

**Fig.10F**

**Fig.10G**

REM: The alignment does not have to be very precise,  
the channel will be defined in the next step

**Fig.10H**

**Fig.11A**

**Fig.11B**

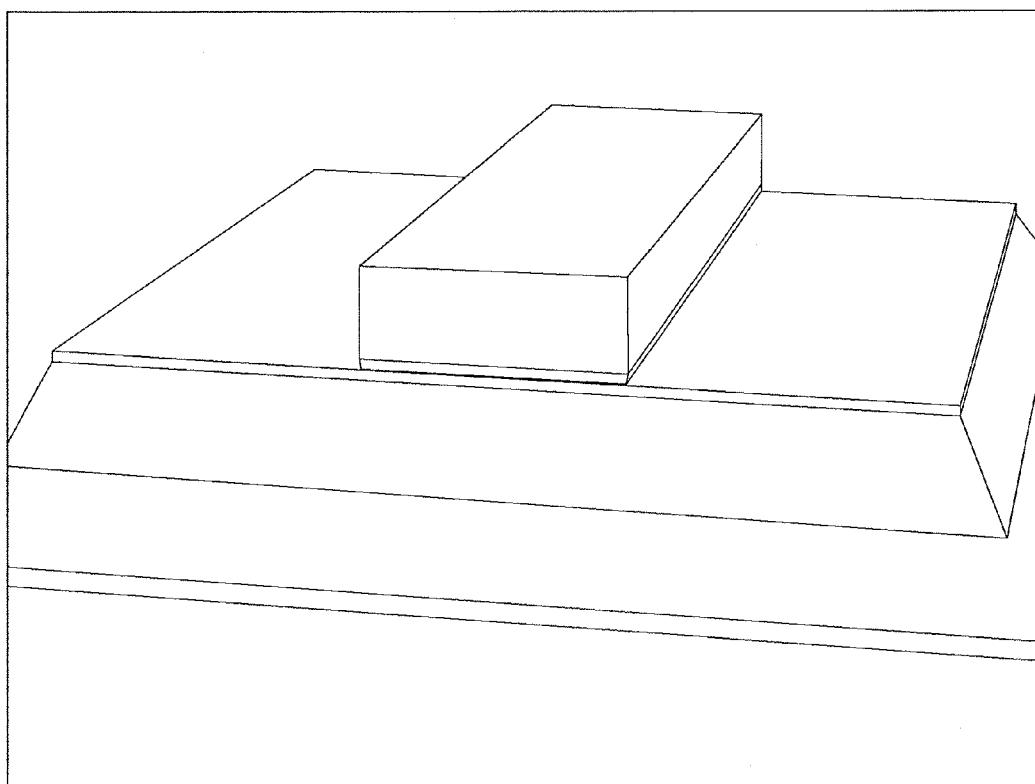


Fig. 11C

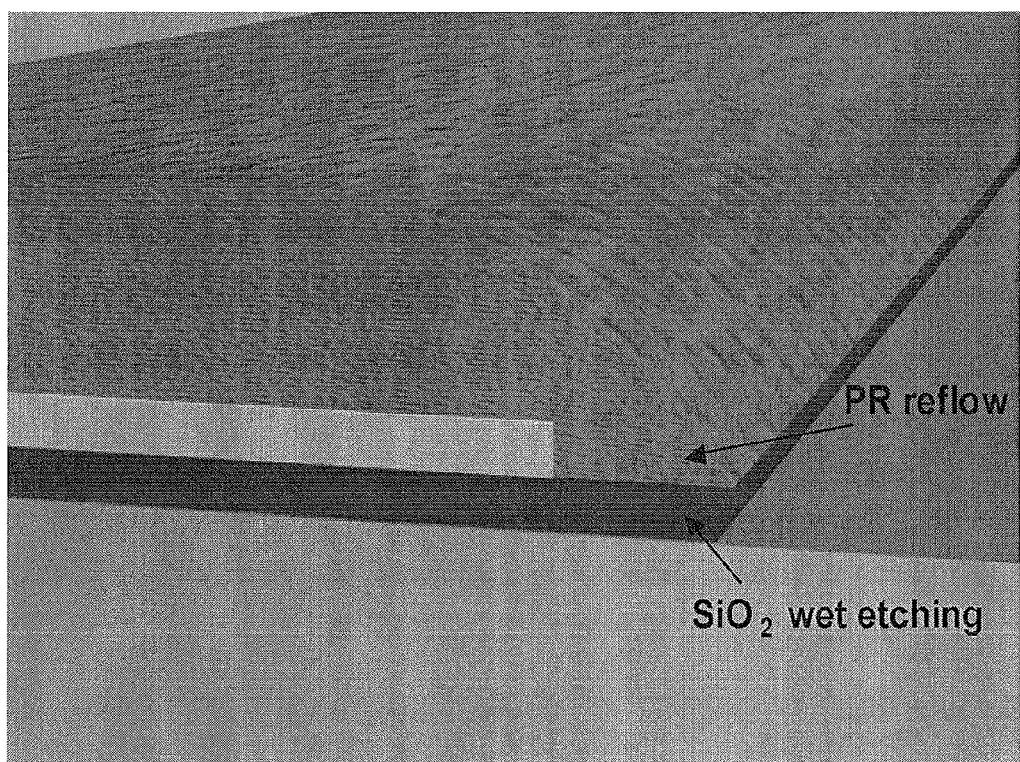
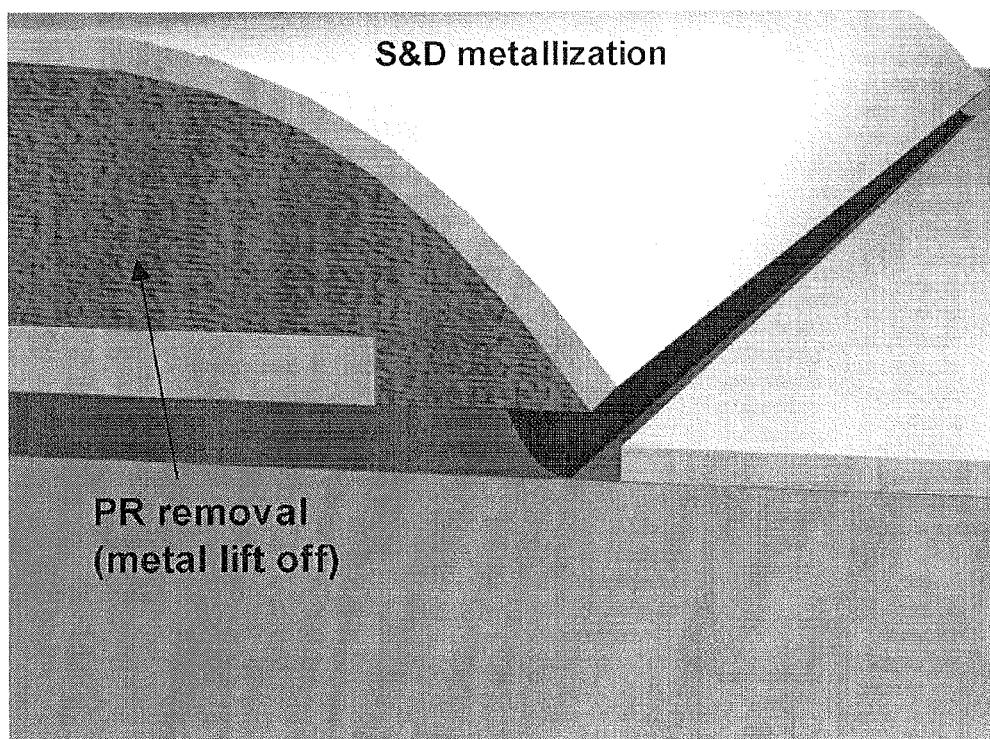


Fig. 11D



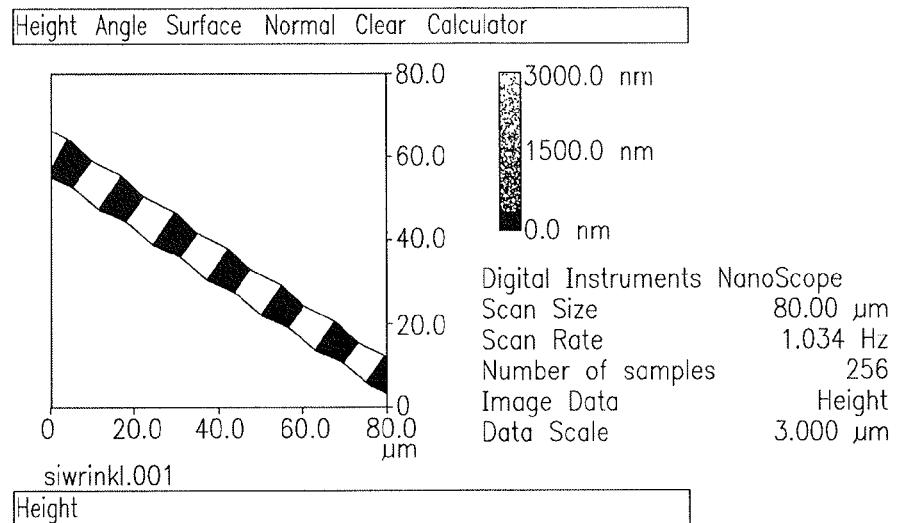


Fig. 12A

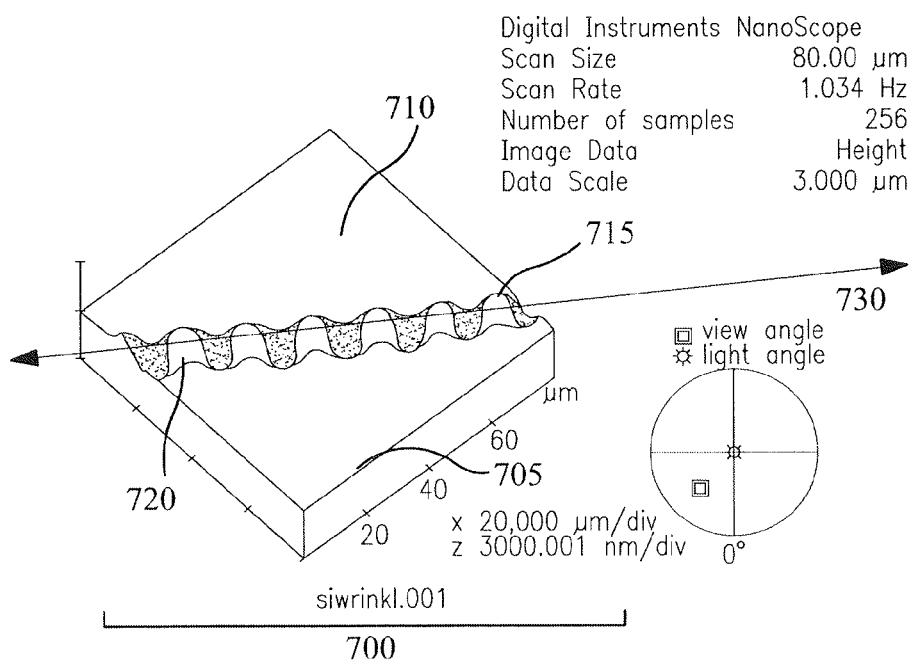


Fig. 12B

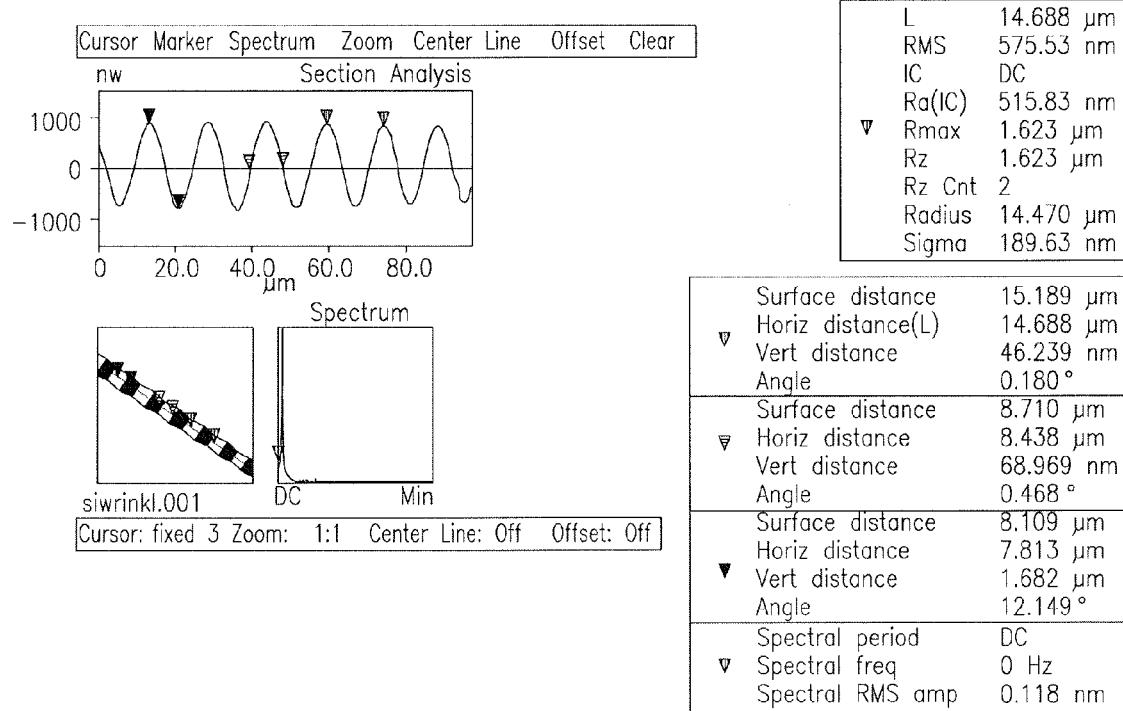


Fig. 12C

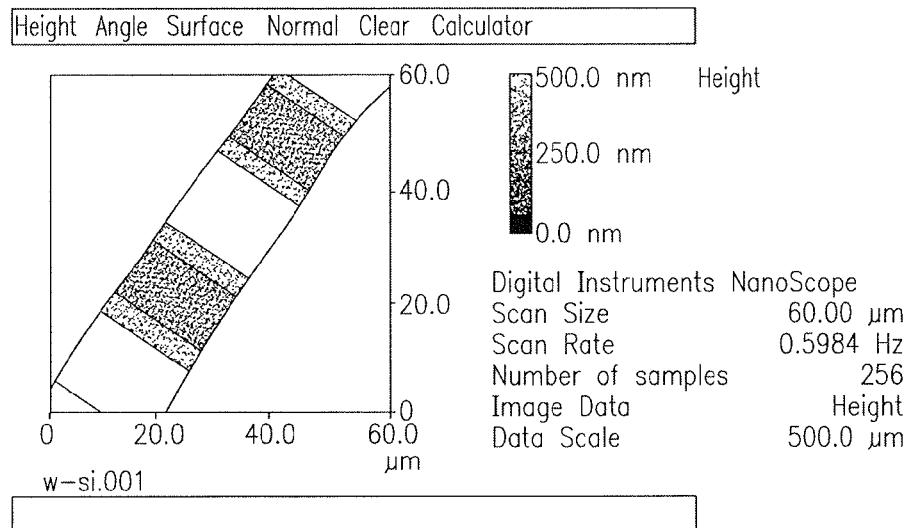


Fig. 13A

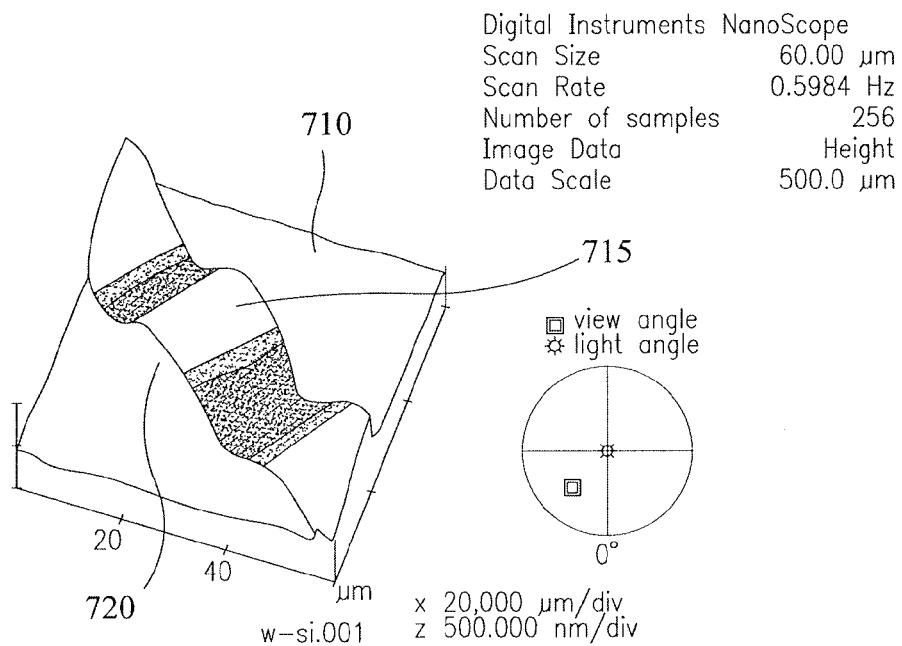


Fig. 13B

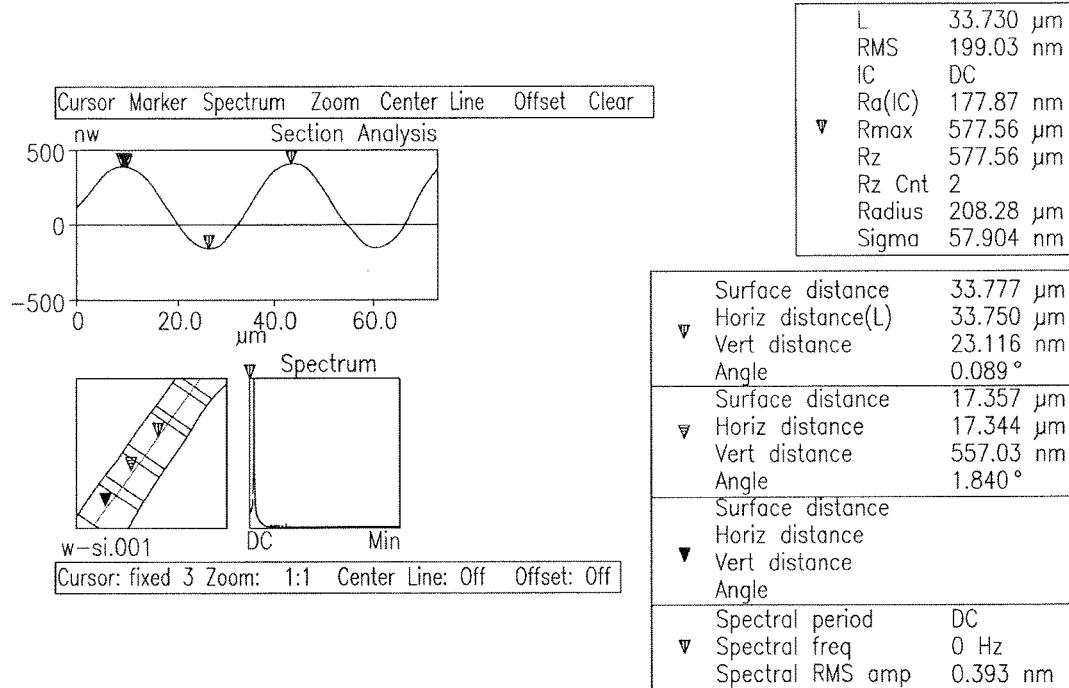


Fig. 13C

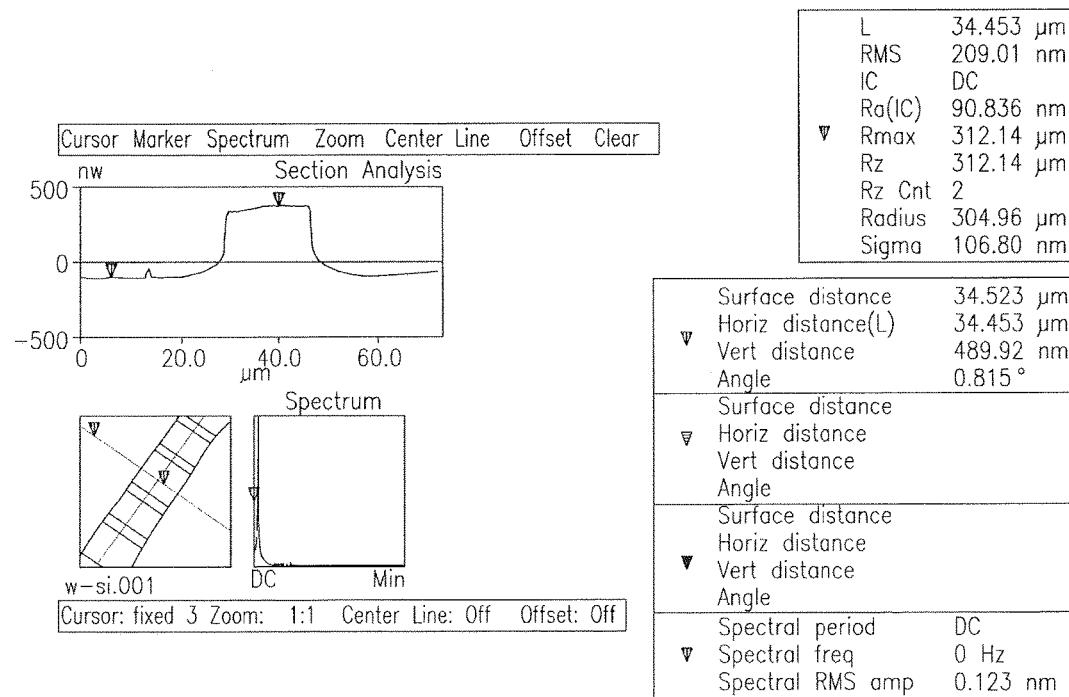


Fig. 13D

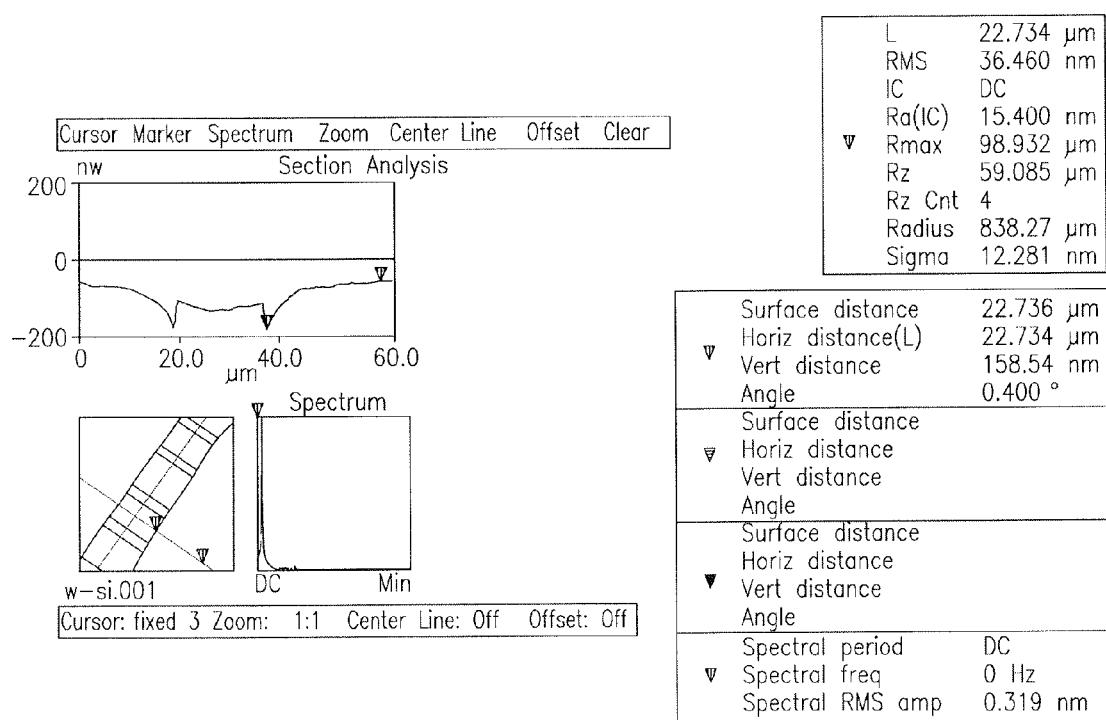


Fig. 13E

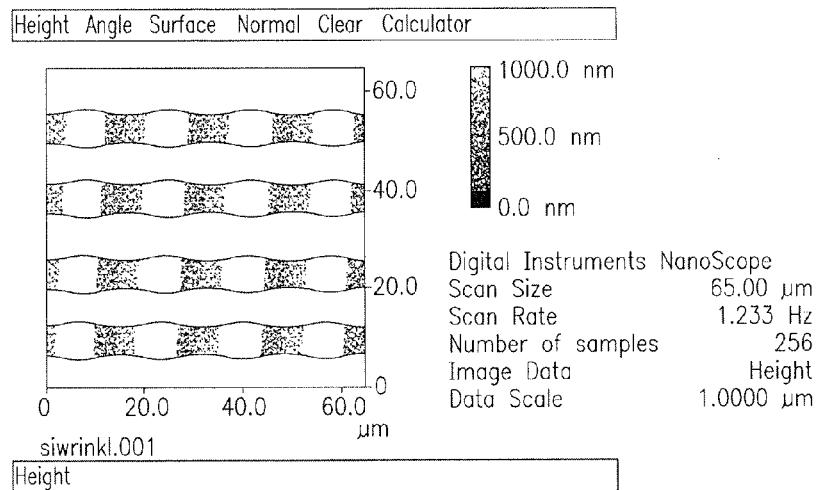


Fig. 14A

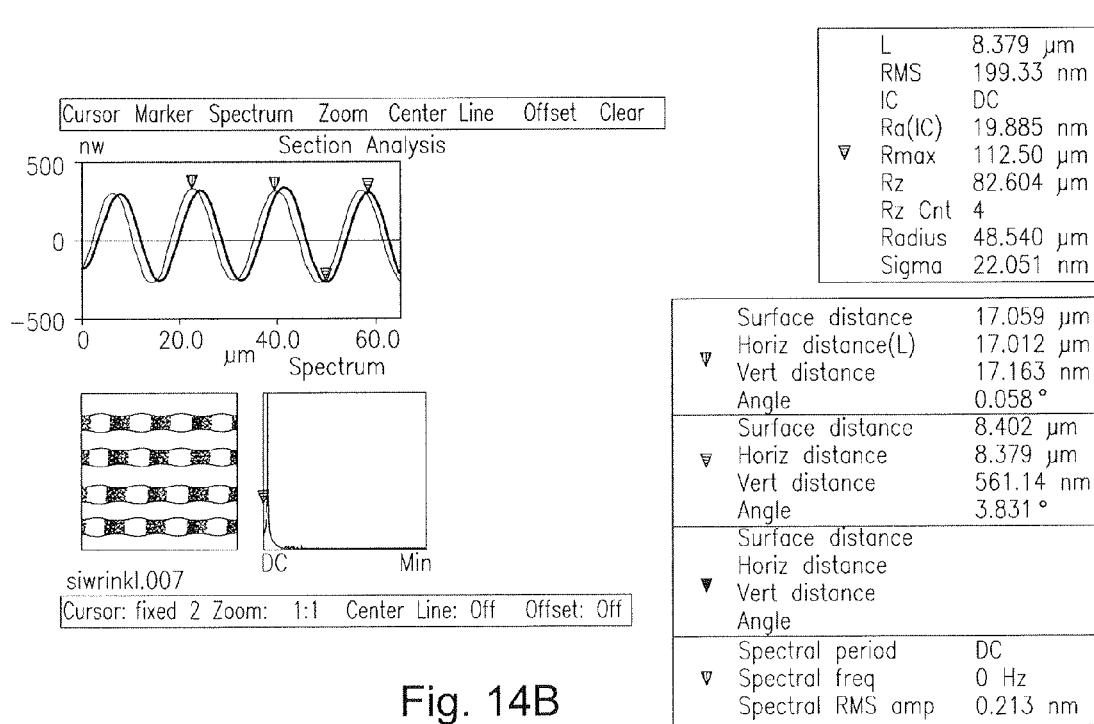


Fig. 14B

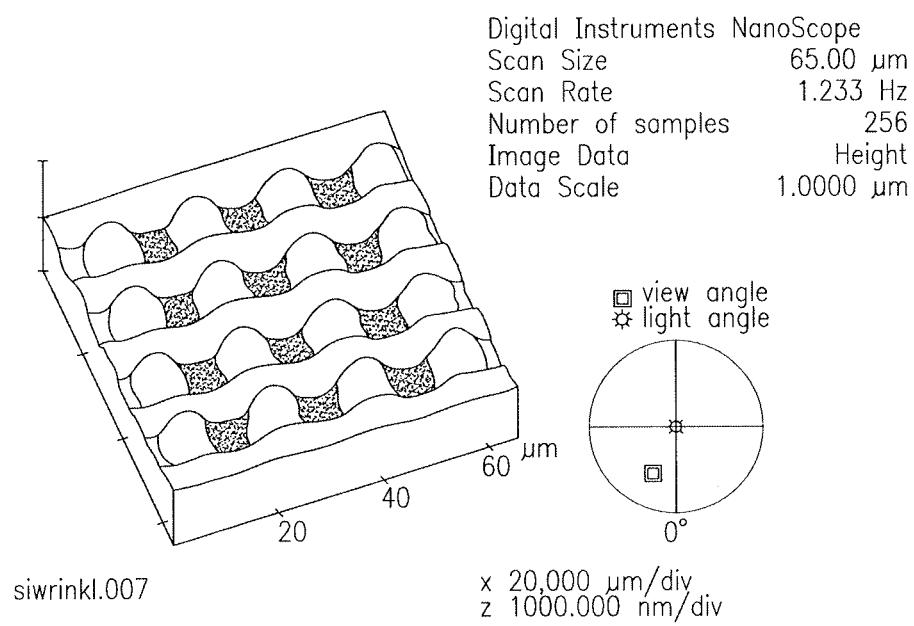


Fig. 14C

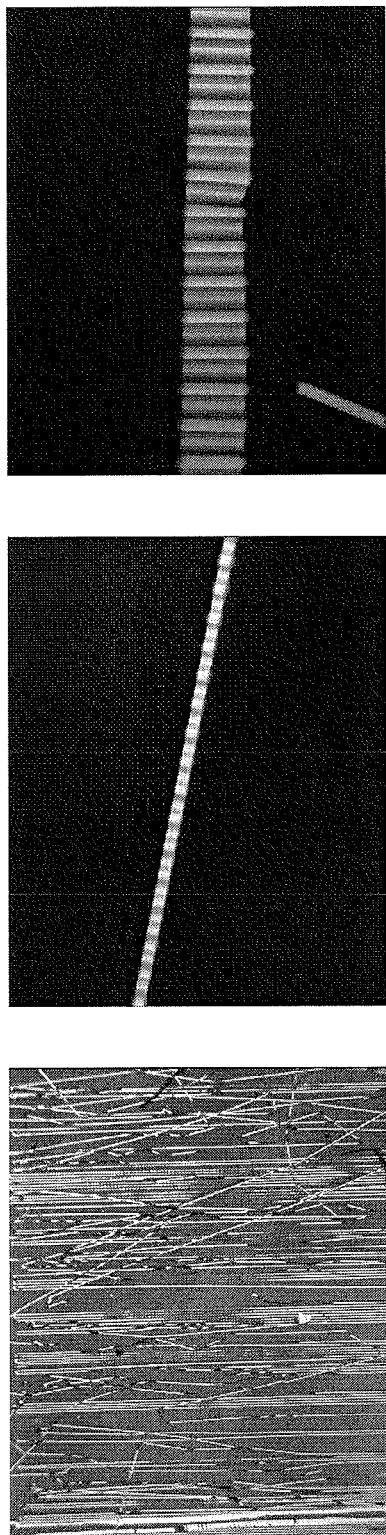


Fig. 15: Stretchable semiconductor element

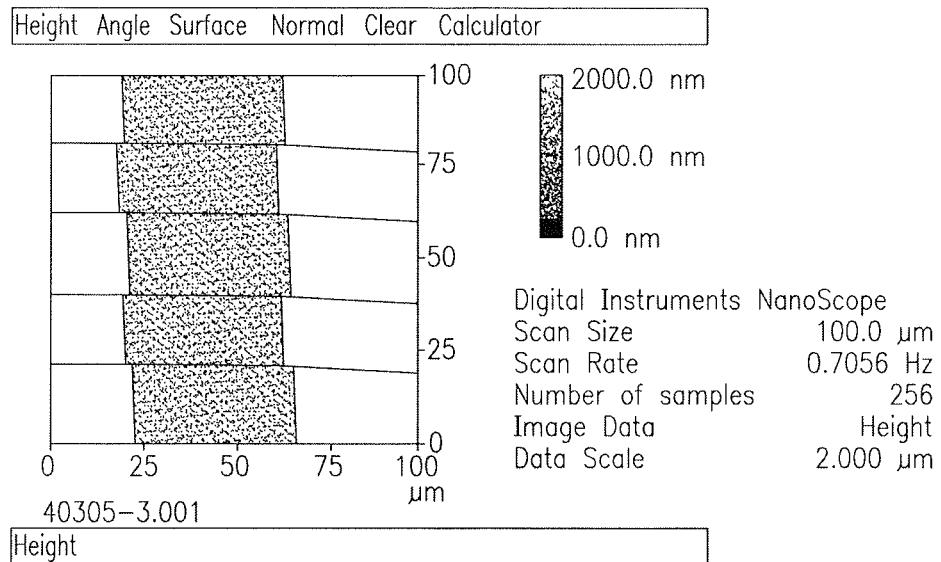


Fig. 16A

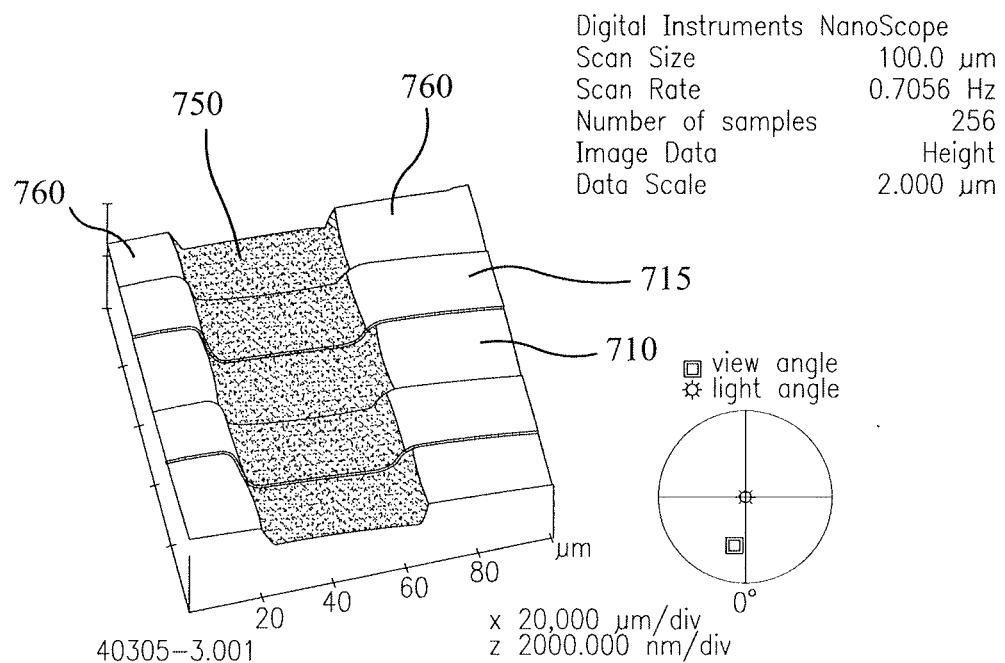


Fig. 16B

**Fig. 17**

1. Providing a prestrained elastic substrate in an expanded state. (e.g. roll pressing or bending)



2. Bonding at least a portion of the internal surface of a printable semiconductor structure to the external surface of the prestrained elastic substrate in an expanded state.

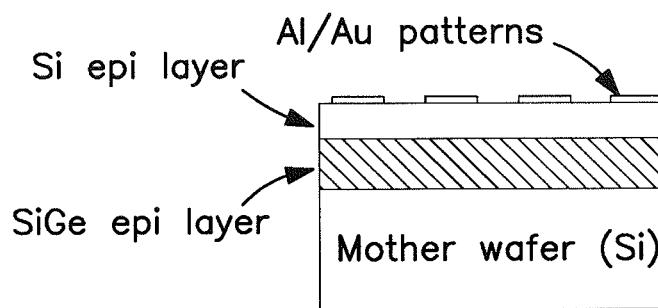


3. Allowing the elastic substrate to relax at least partially, wherein relaxation of the elastic substrate bends the internal surface of the printable semiconductor structure

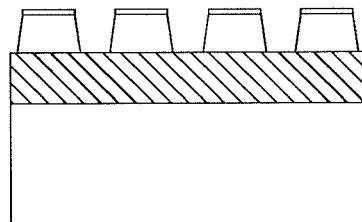


OPTIONAL

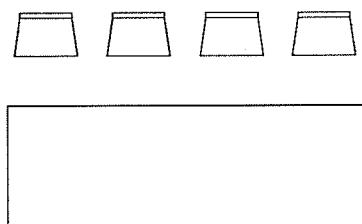
4. Transfer printable semiconductor having curved internal substrate to a flexible receiving substrate.

**Fig.18A**

i)  $\mu$ s-Si shape definition



ii)  $\mu$ s-Si wet etching



iii) Si-Ge selective wet etching

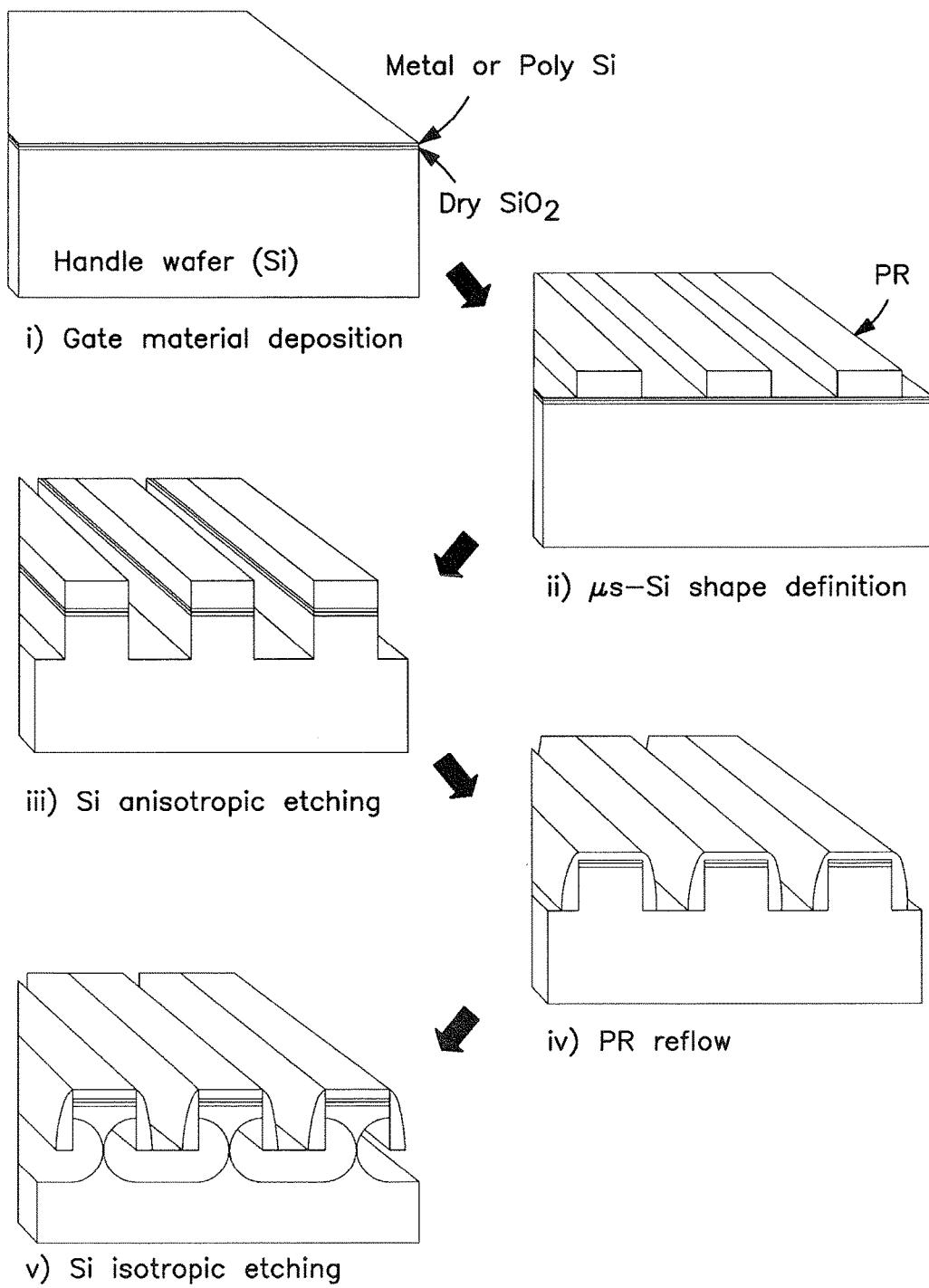
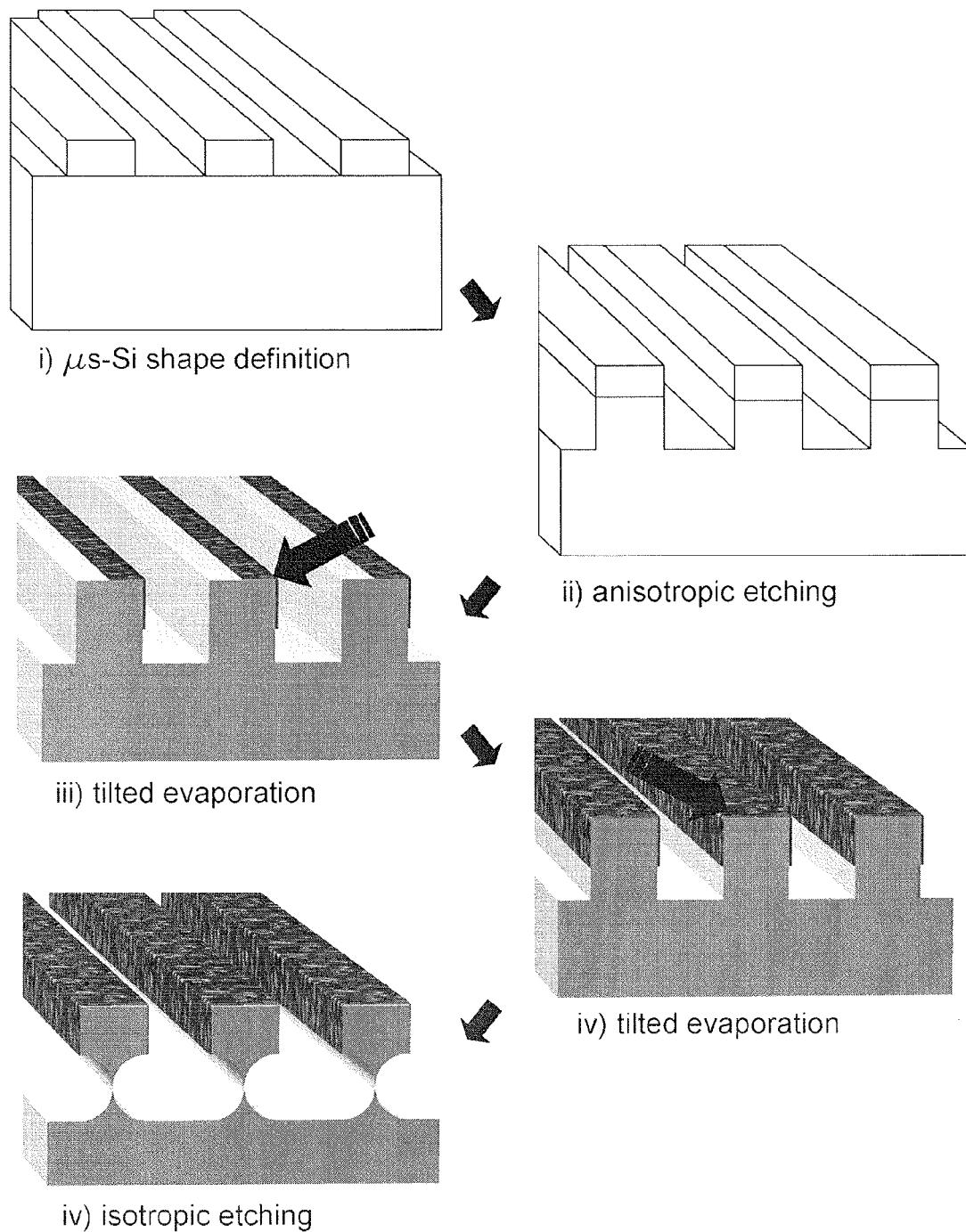
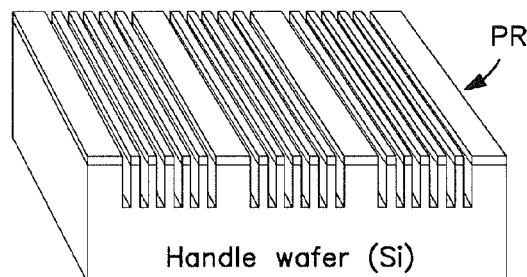
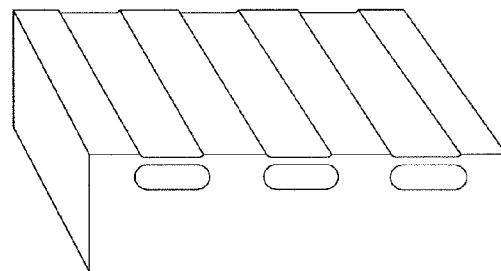
**Fig.18B**

Fig. 18C

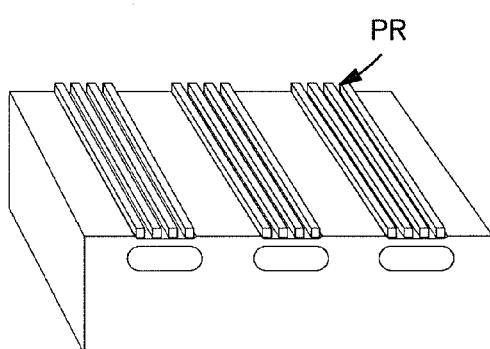


**Fig.18D**

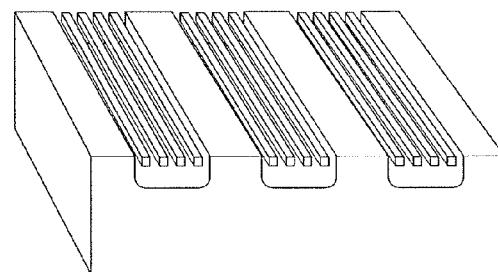
i) Si anisotropic etching



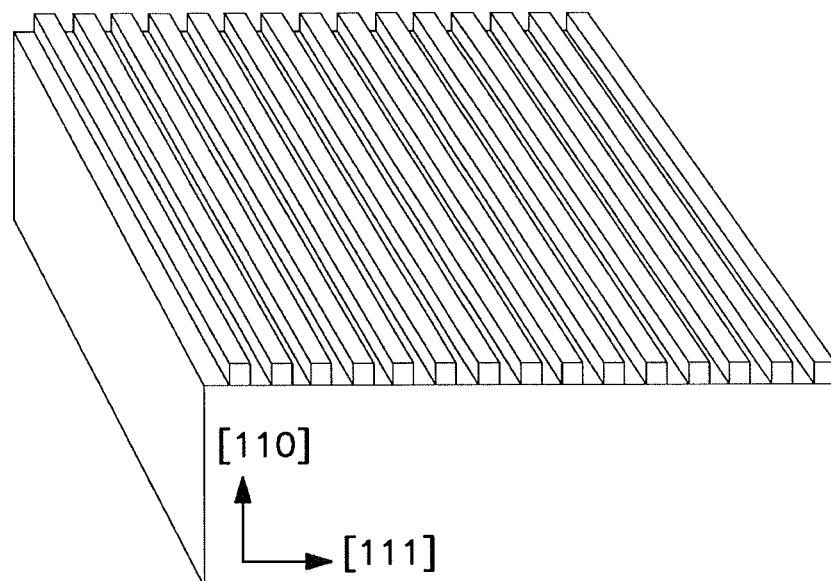
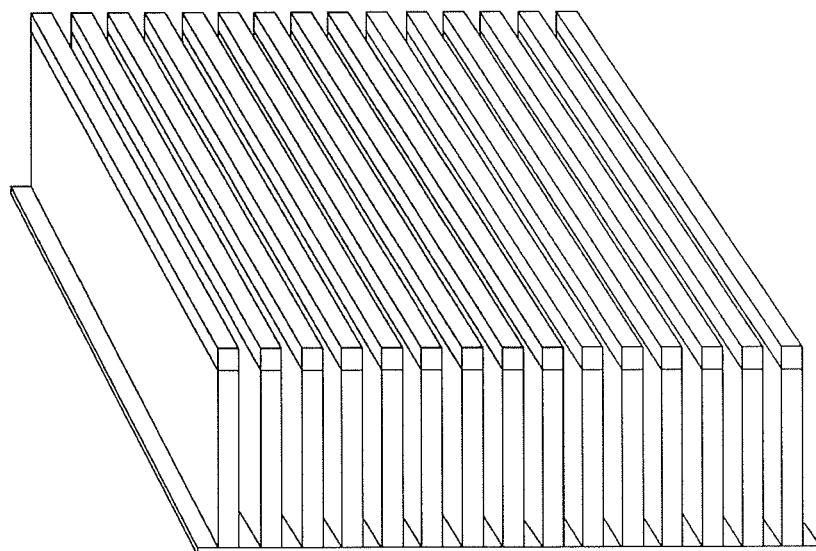
ii) Si annealing in N<sub>2</sub>



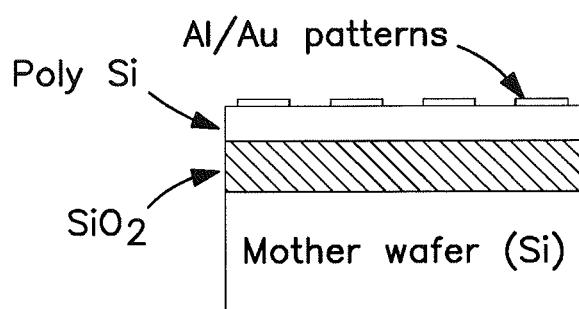
iii) μs-Si shape definition



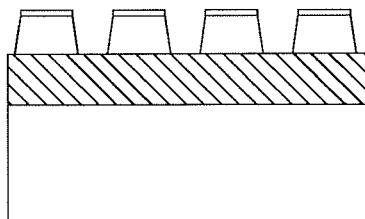
iii) Si etching

**Fig.18E**i)  $\mu$ s-Si shape definition

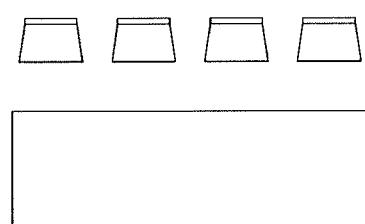
ii) anisotropic wet chemical etching

**Fig.18F**

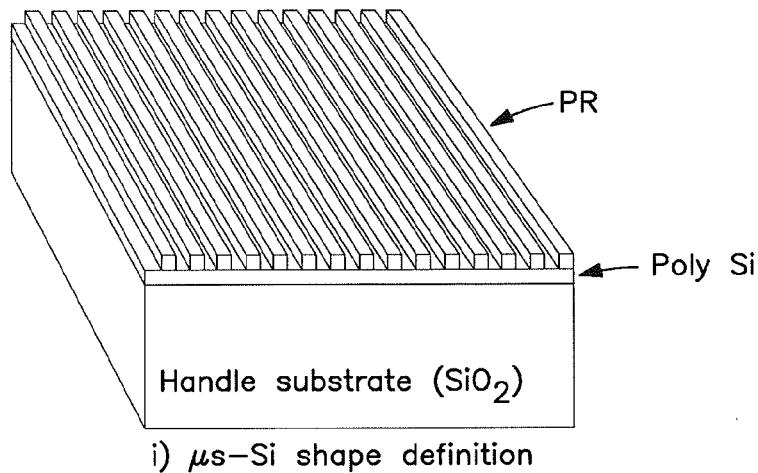
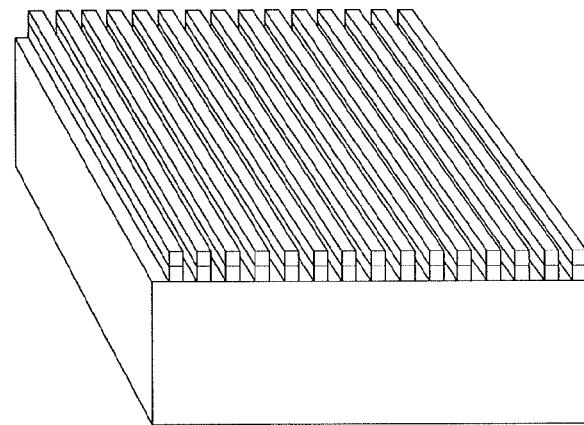
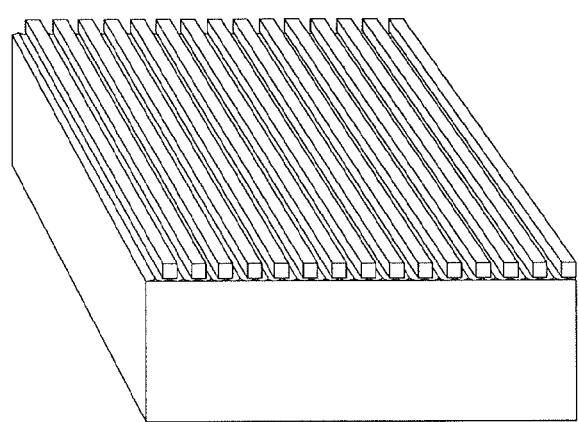
i)  $\mu\text{s-Si}$  shape definition

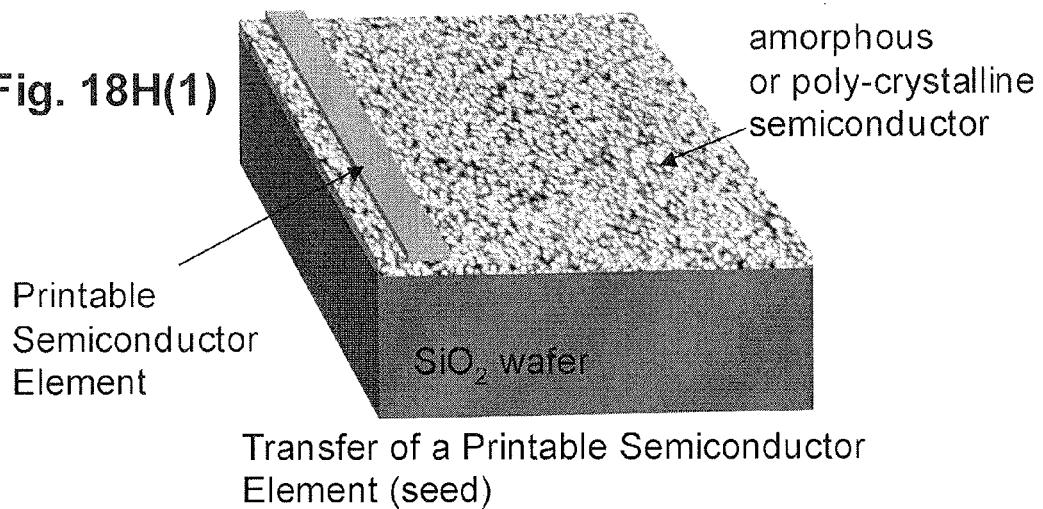
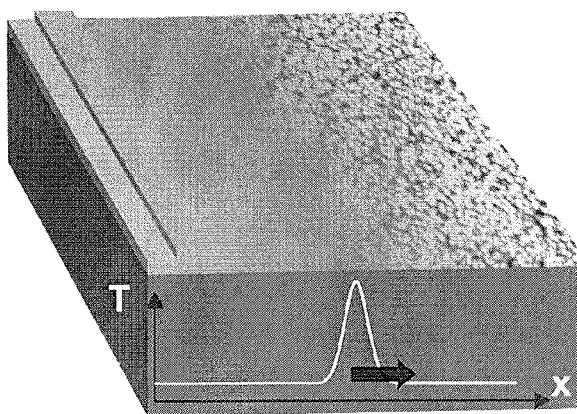
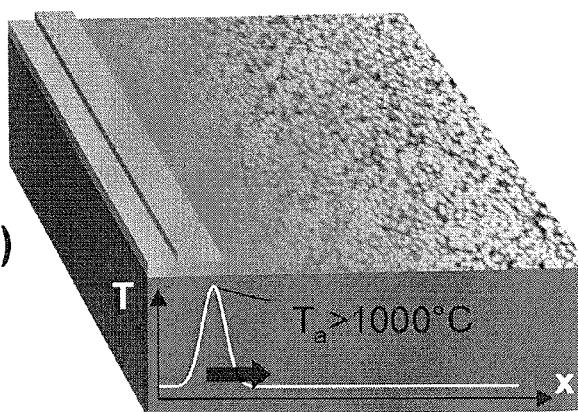


ii)  $\mu\text{s-Si}$  wet etching

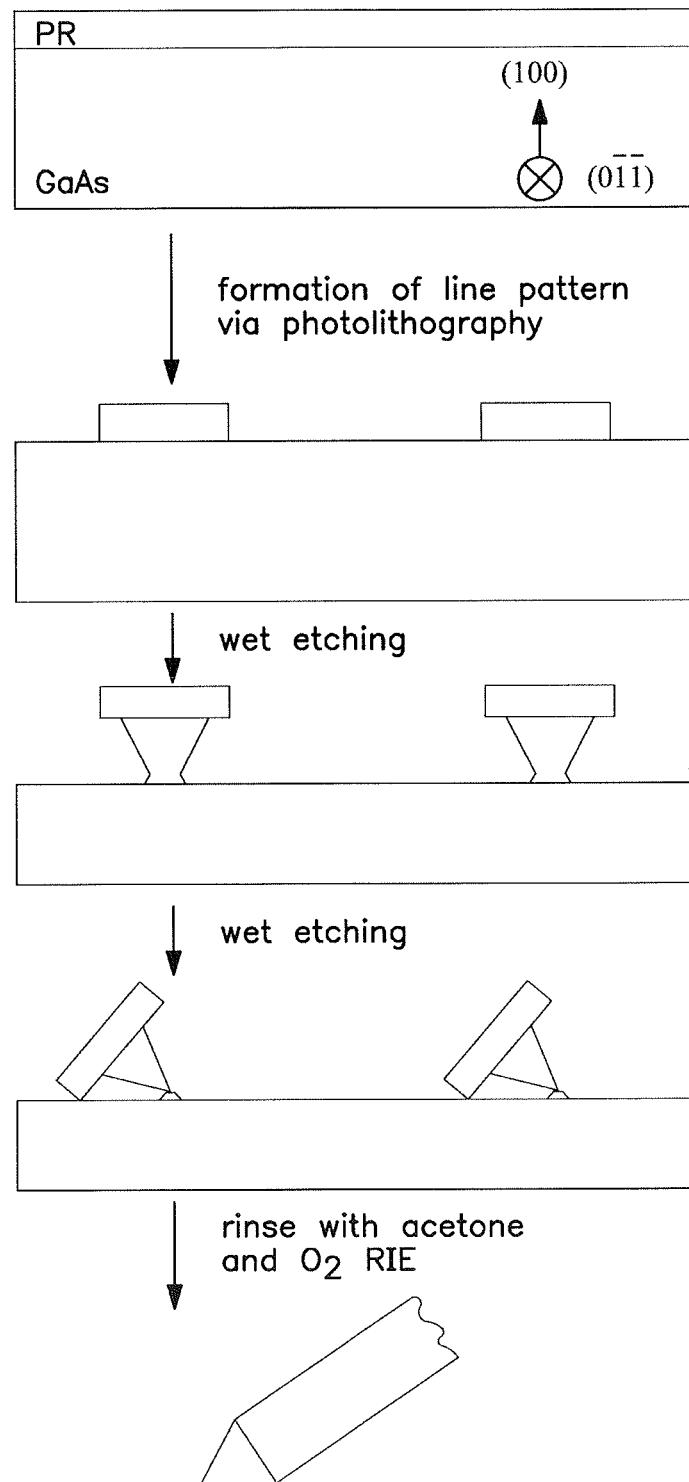


iii) Liftoff:  $\text{SiO}_2$  selective wet etching

**Fig.18G**i)  $\mu\text{s-Si}$  shape definitioni)  $\mu\text{s-pSi}$  wet etchingiii) Liftoff:  $\text{SiO}_2$  selective wet etching

**Fig. 18H(1)****Fig. 18H(2)**

Annealing of the thin film

**Fig.18I**

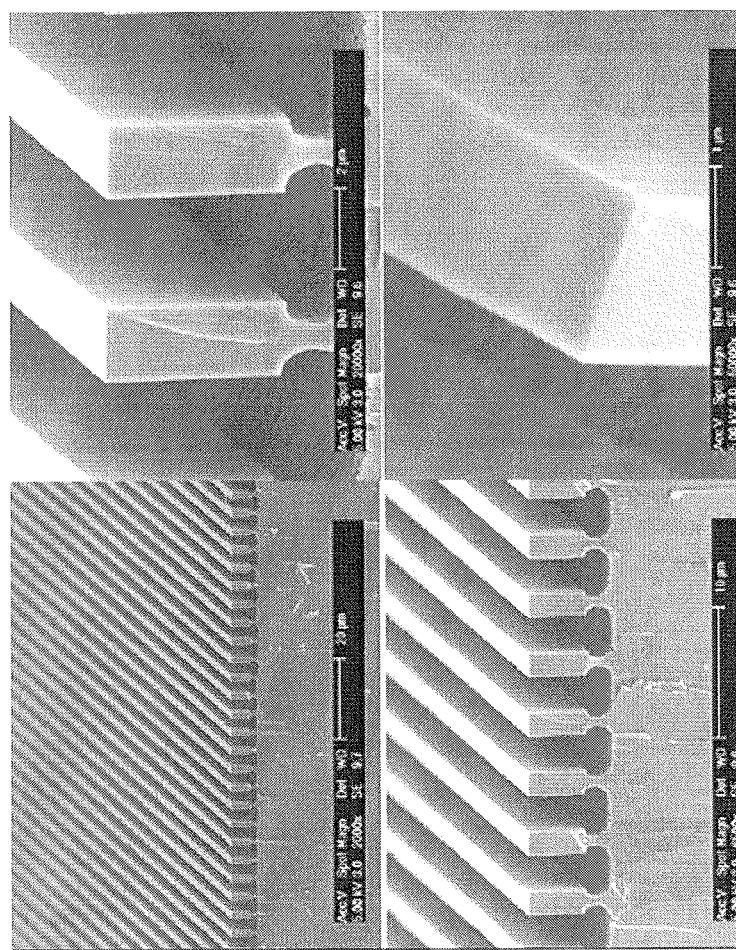
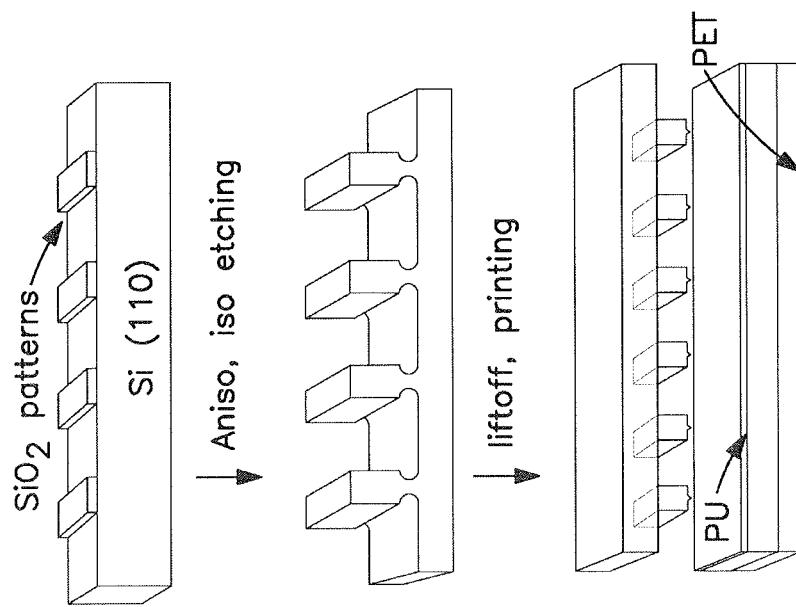


Fig. 18J



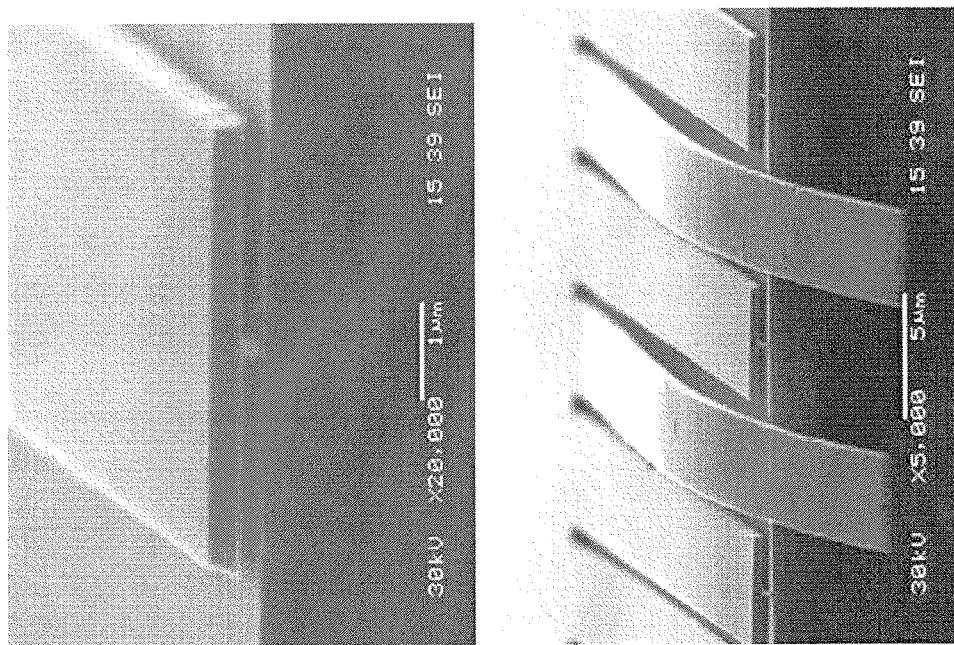
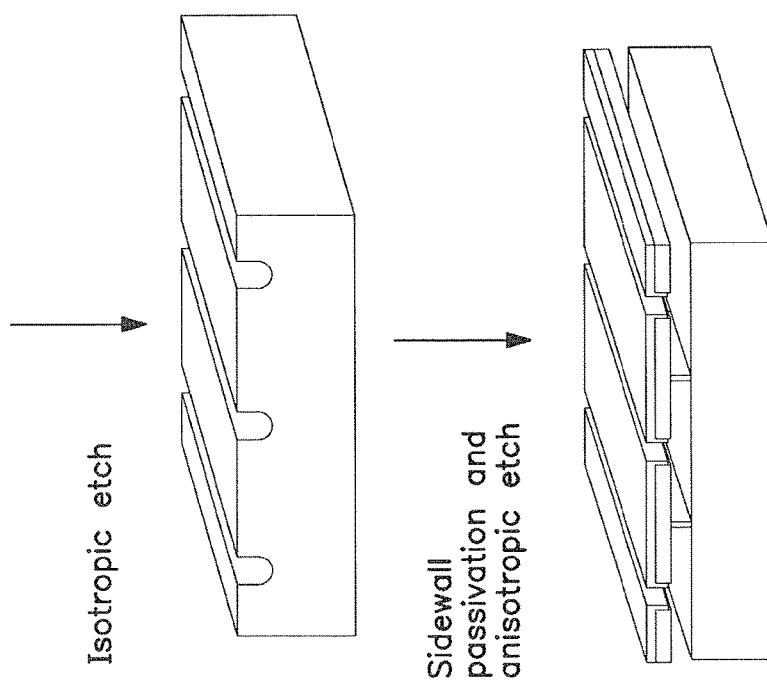
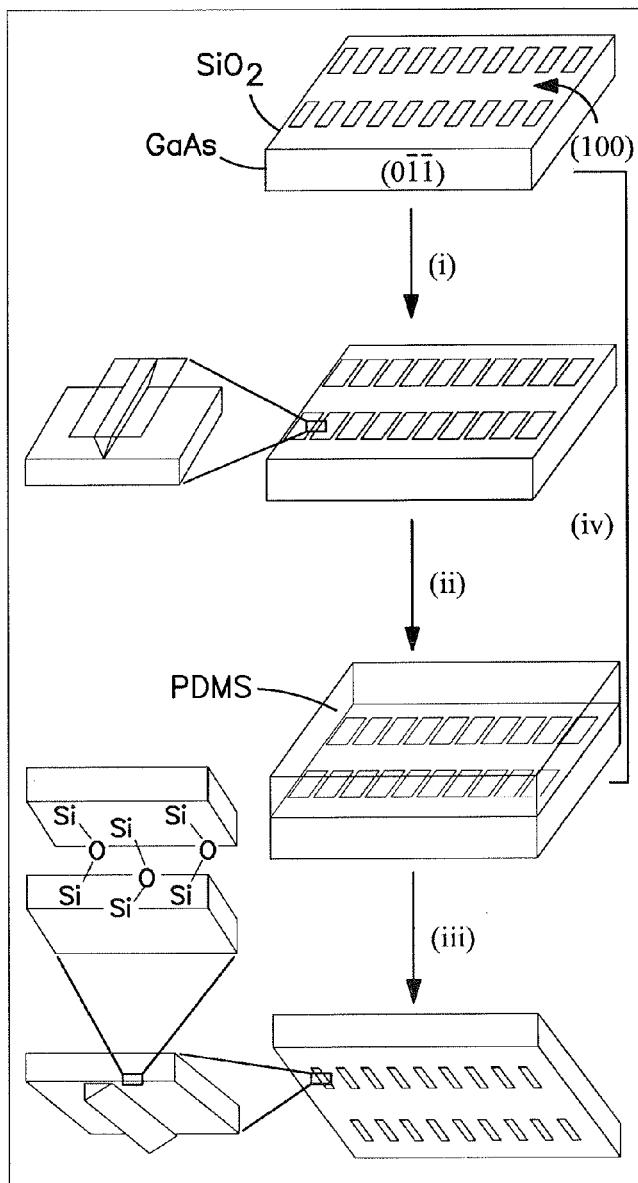
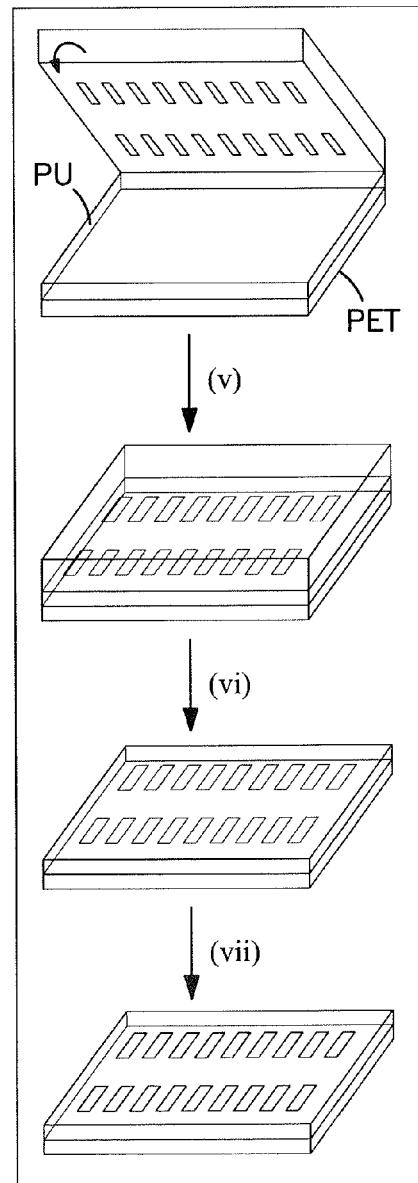
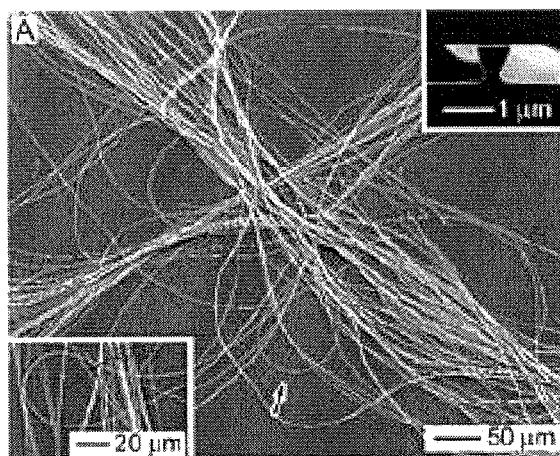
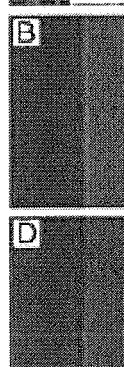
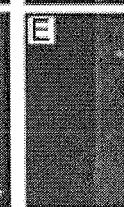
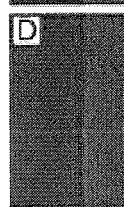
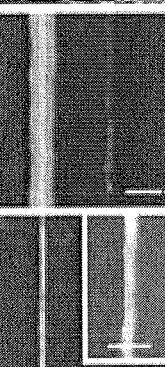
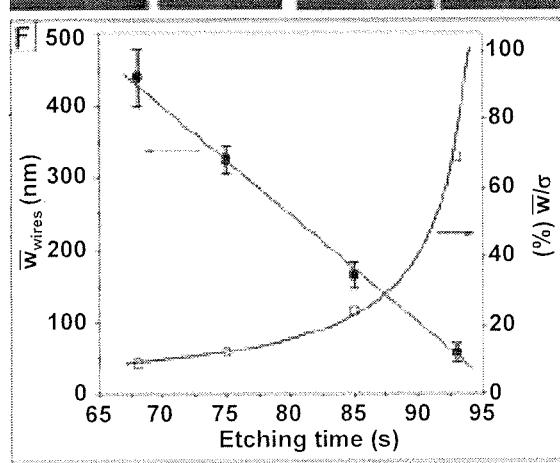
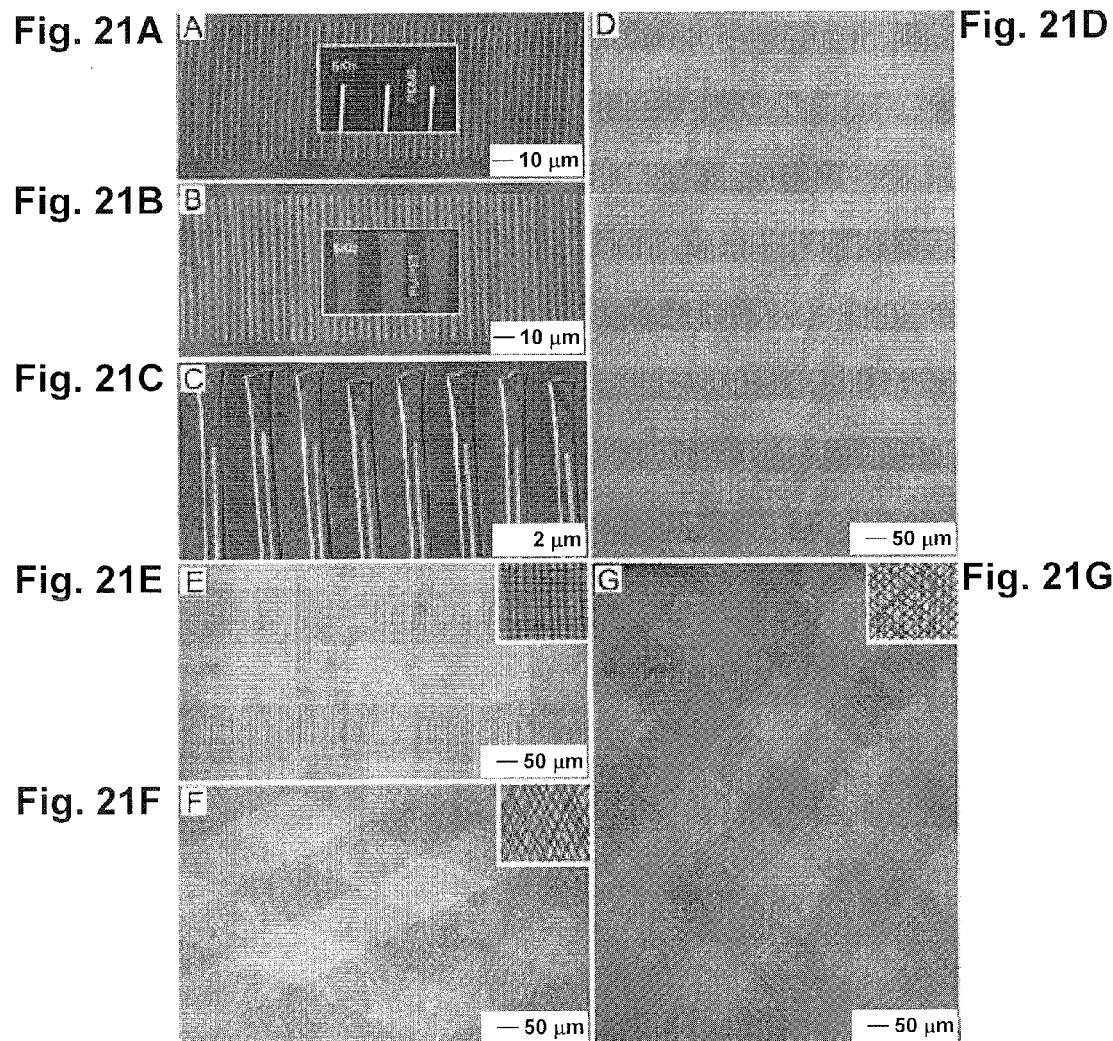


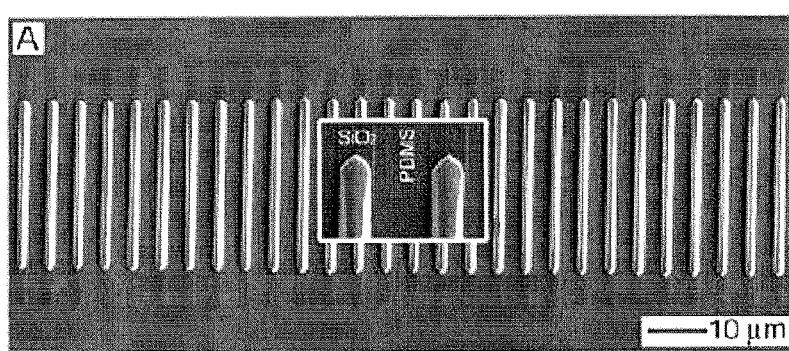
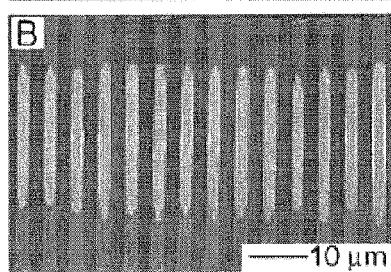
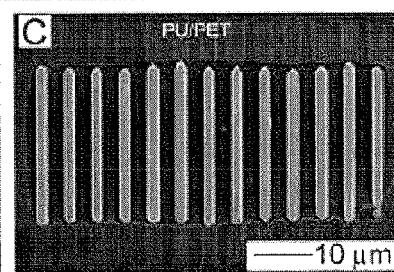
Fig.18K



**Fig.19A****Fig.19B**

**Fig. 20A****Fig. 20B****Fig. 20D****Fig. 20C****Fig. 20E****Fig. 20F**



**Fig. 22A****Fig. 22B****C****Fig. 22C**

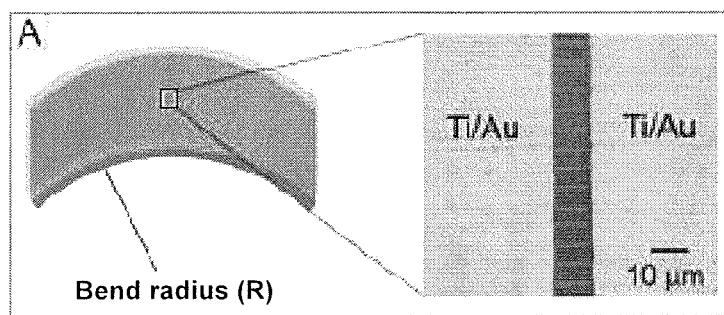
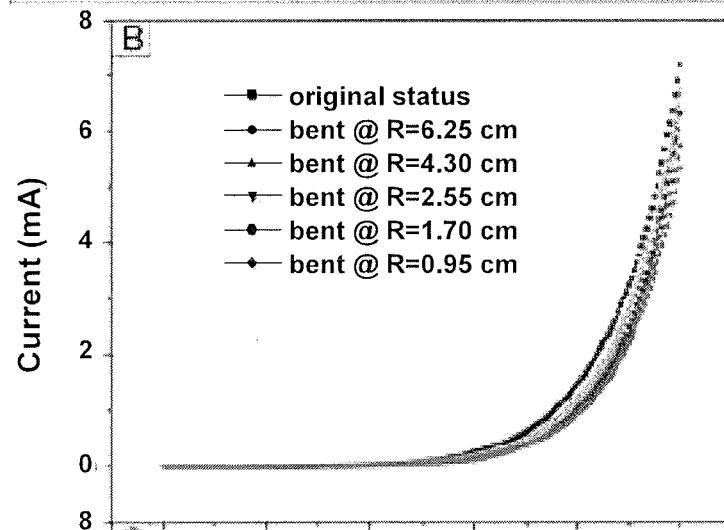
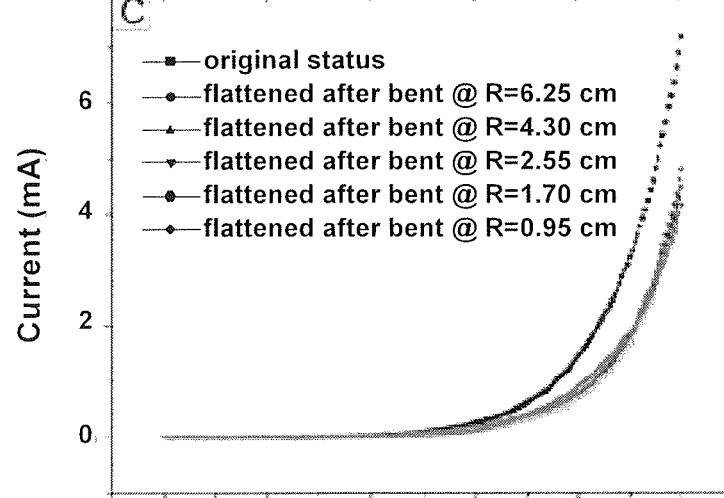
**Fig. 23A****Fig. 23B****Fig. 23C**

Fig. 24

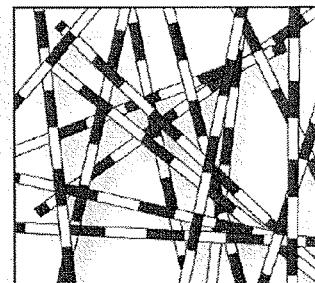
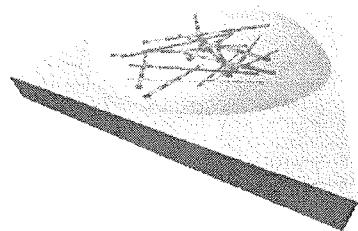
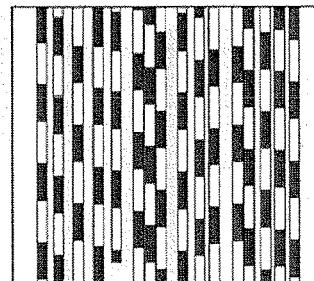
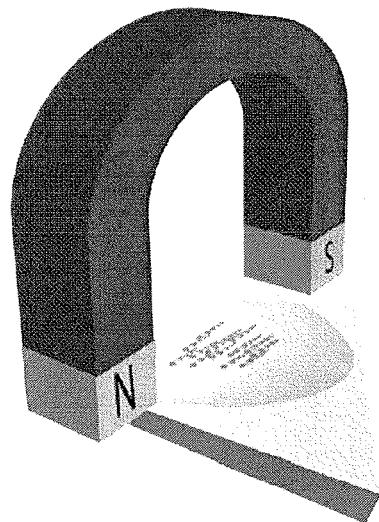
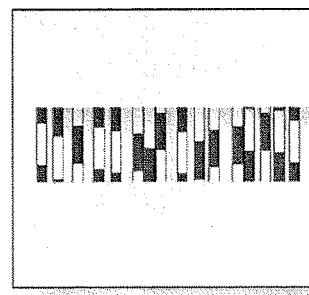
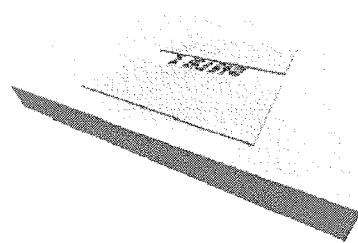
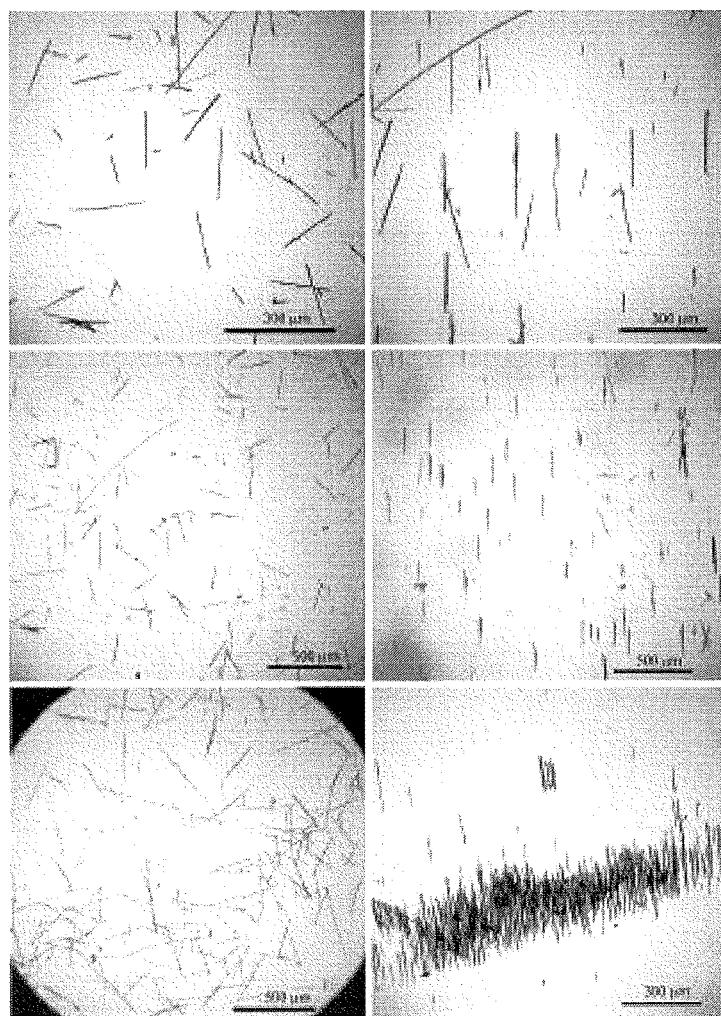
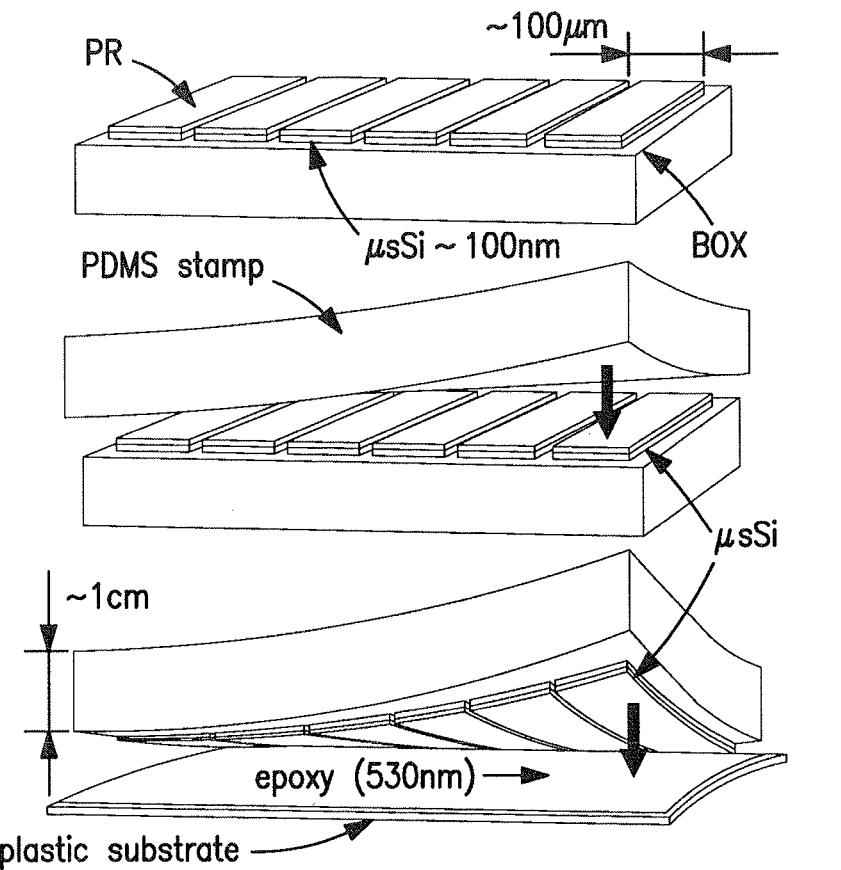
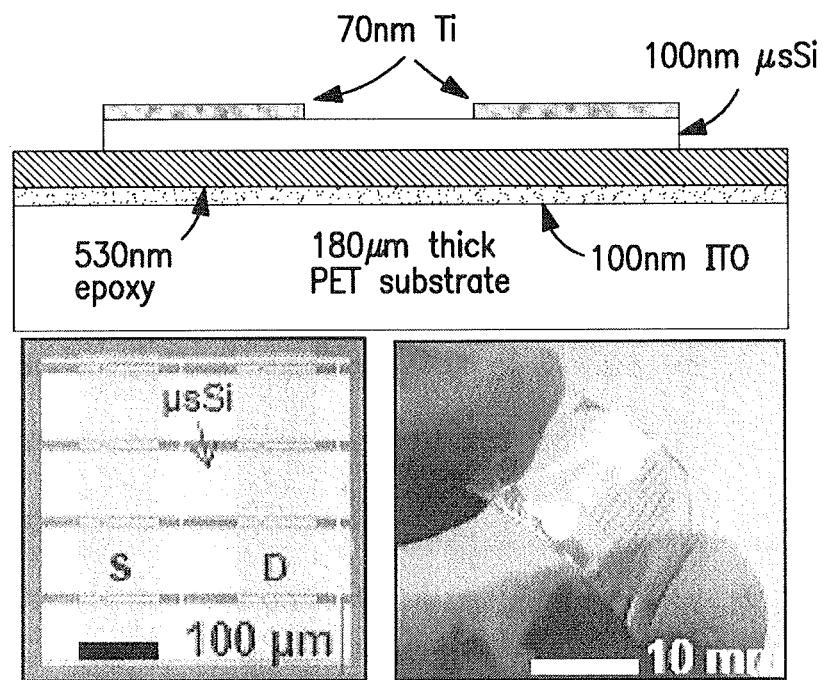
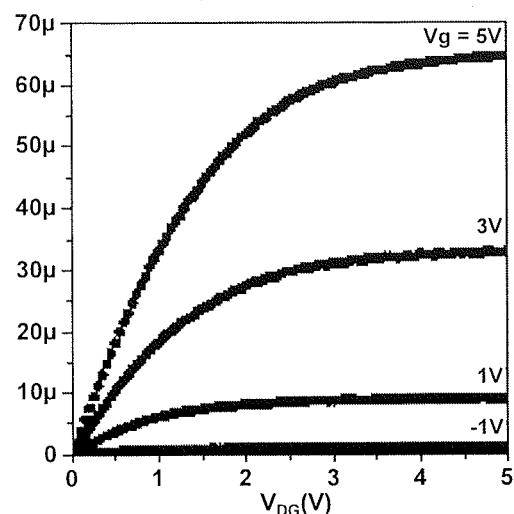
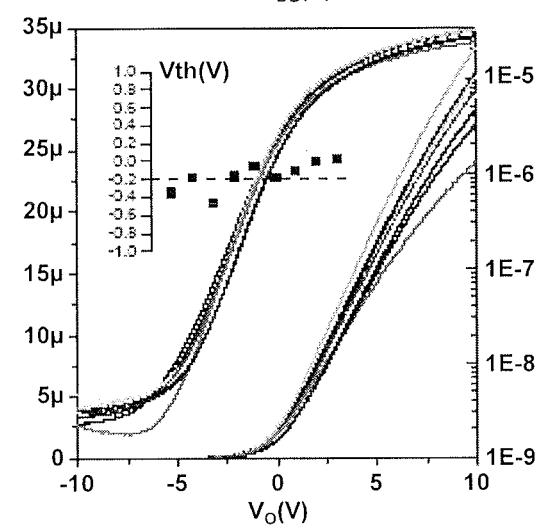
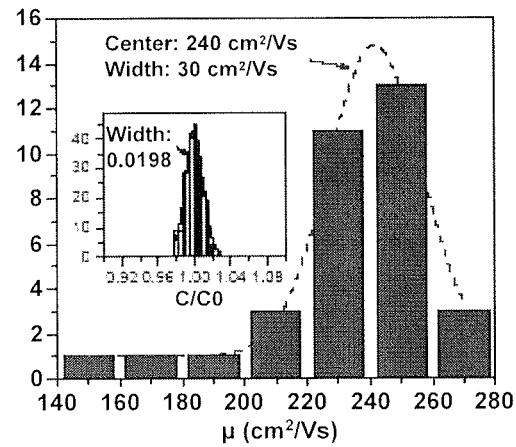
**I. Dispersal in Solution and Casting on Substrate**Magnetic Tags (light)  
on Microstructured  
Semiconductor (dark)**II. Organization in Magnetic Field****III. Metallization**

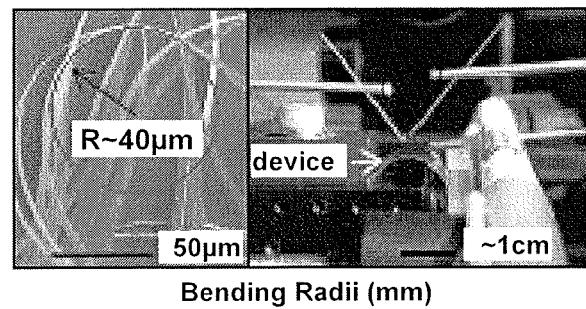
Fig 25



Magnetically tagged microstructures dispersed in solution and cast on a substrate (left). Influence of Magnetic field (right).

**Fig.26A****Fig.26B**

**Fig. 27A****Fig. 27B****Fig. 27C**



Bending Radii (mm)

Fig. 28A

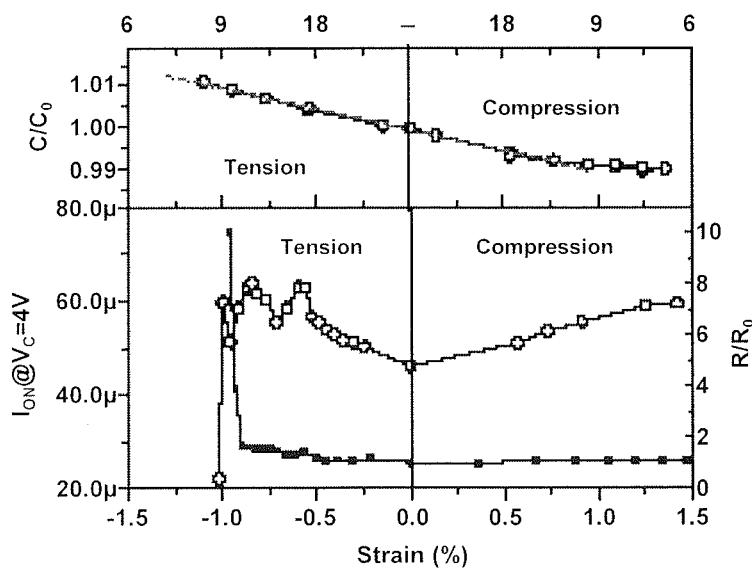
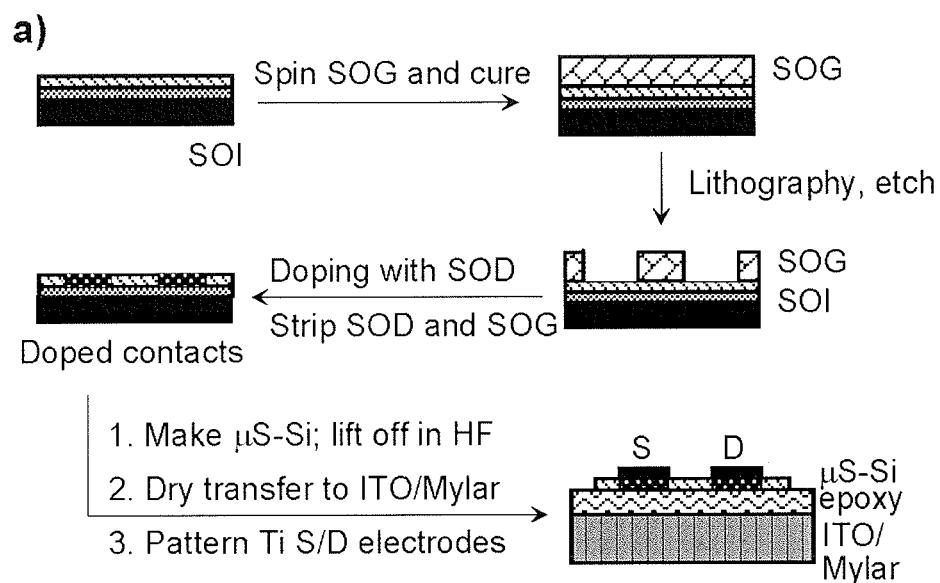
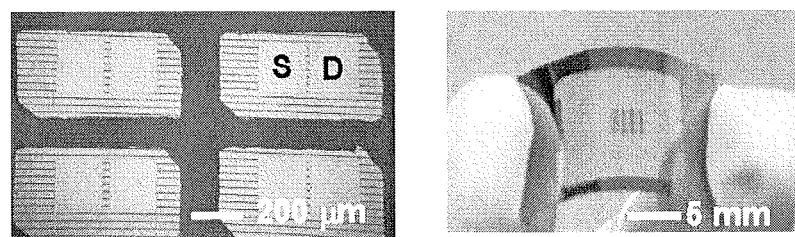


Fig. 28B



**Fig. 29A**



**Fig. 29B**

Fig. 30A

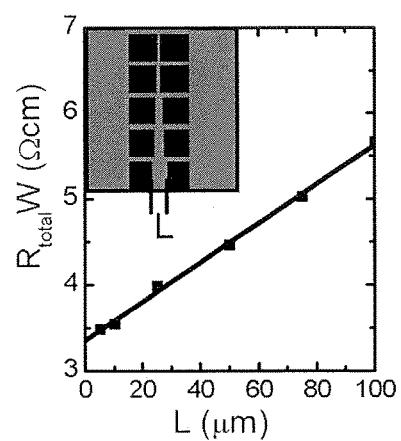


Fig. 30B

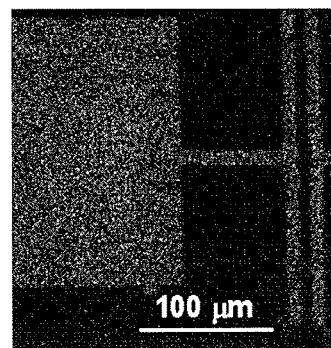


Fig. 31A

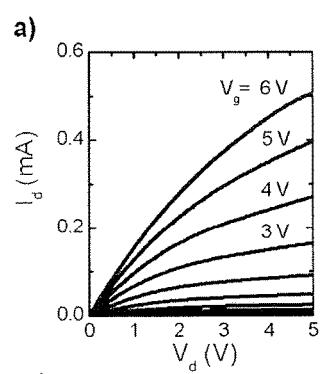


Fig. 31C

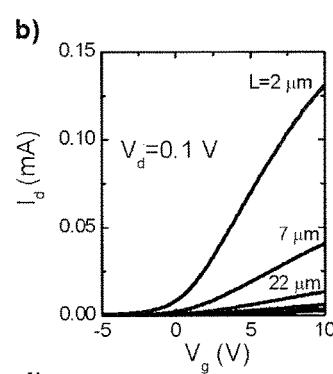
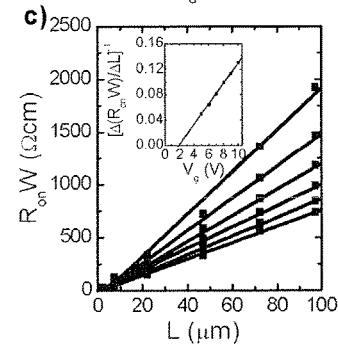


Fig. 31B

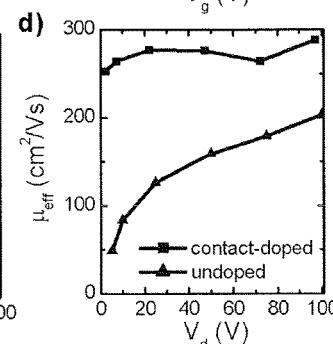


Fig. 31D

Fig. 32A

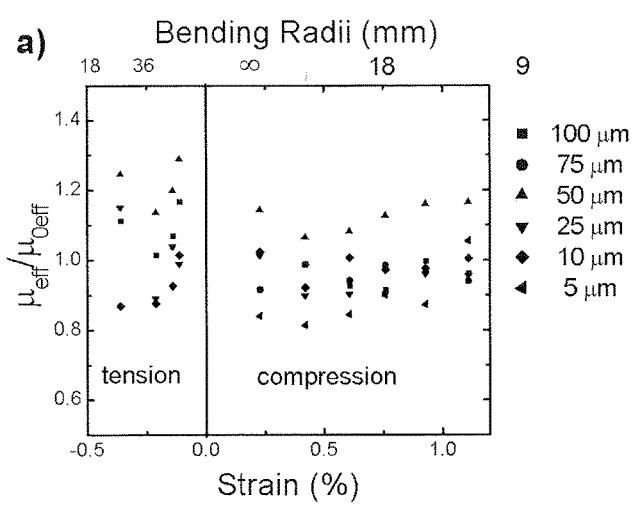


Fig. 32B

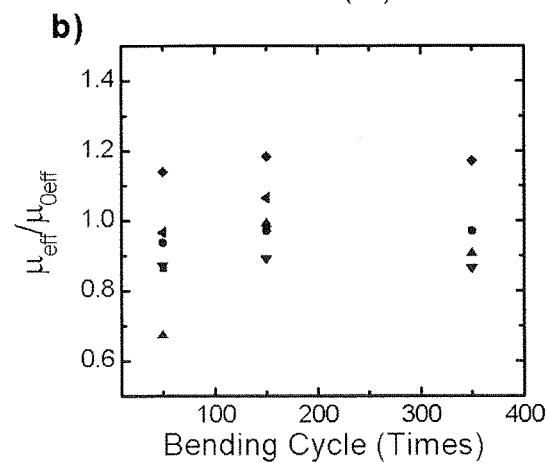
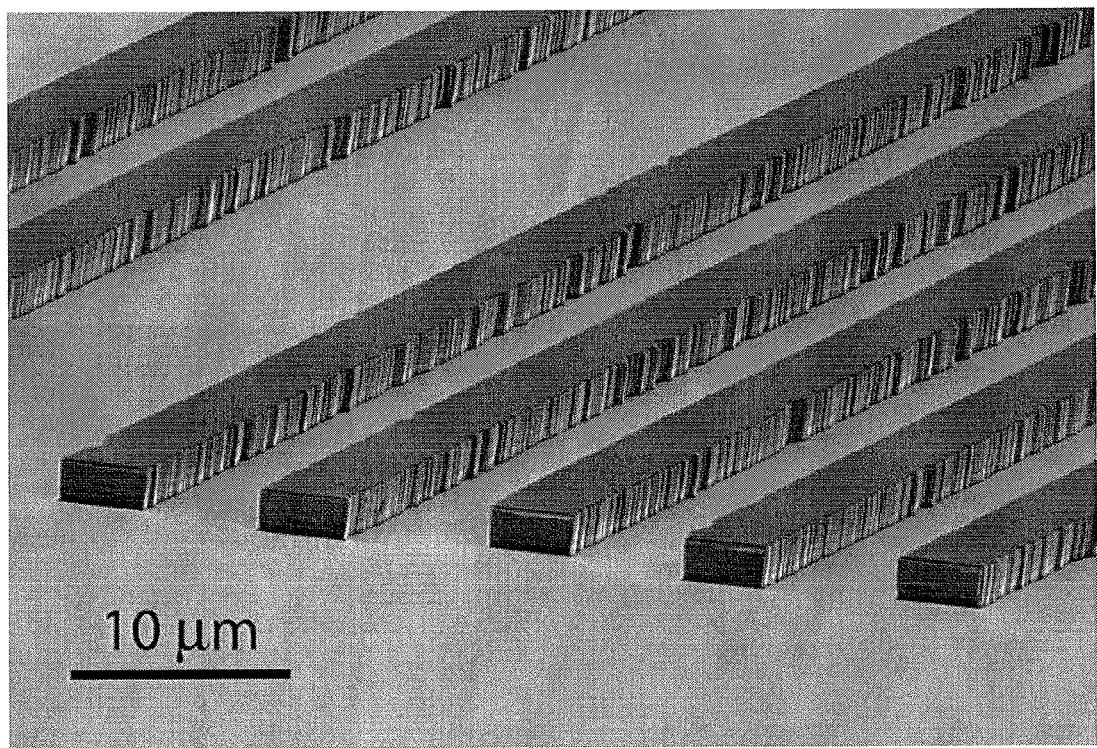


Fig. 33



Provide high quality semiconductor material, such as a single crystal silicon wafer.



Process semiconductor material to generate adjacent N doped and P doped layers, for example using spin on dopants.



1. Pattern and etch processed semiconductor material to define physical dimensions of the printable P-N junction.
2. Lift-off processing to generate monolithic structure comprising the printable P-N junction.
3. Optionally, deposit contacts prior to lift-off, for example, via vapor deposition of metal(s).



Assemble printable P-N junction on substrate using (i) solution printing or (ii) dry transfer printing.



Optionally, deposit contacts onto P-N junction on substrate, for example, via vapor deposition of metal(s).

Fig. 34A

Fig. 34B

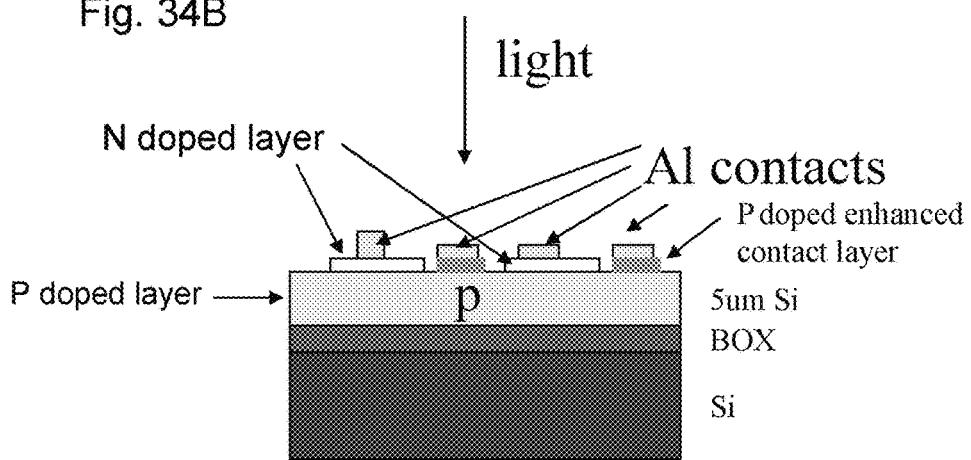
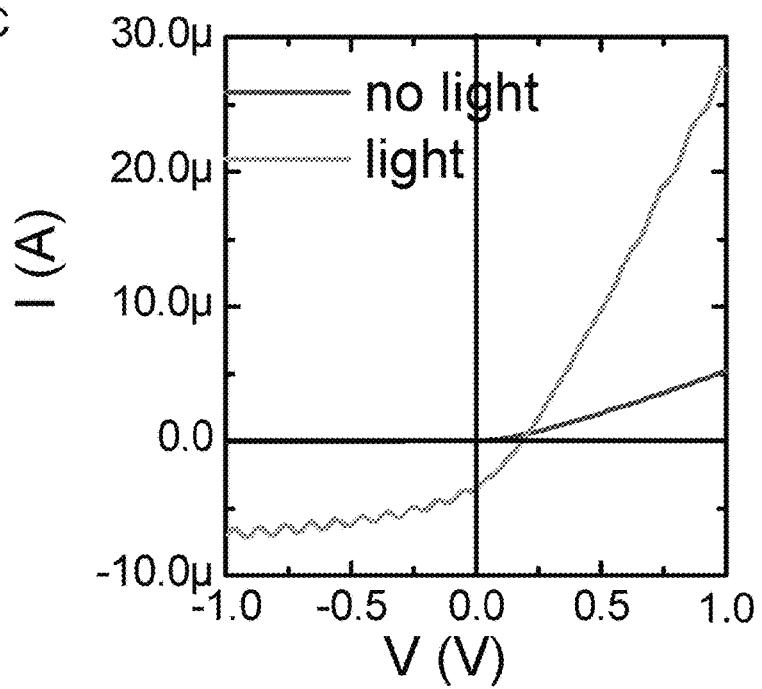


Fig. 34C



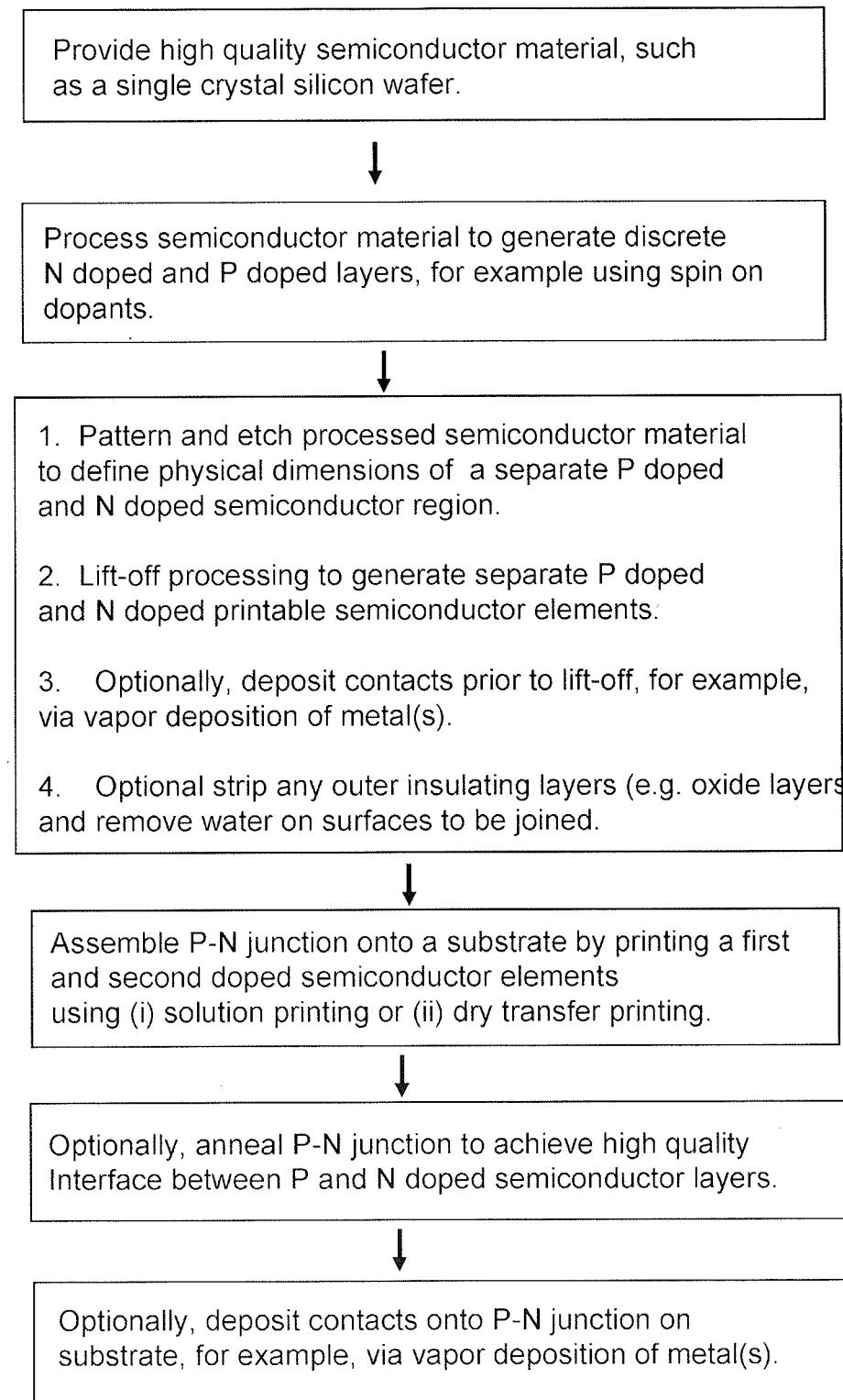


Fig. 35A

Fig. 35B

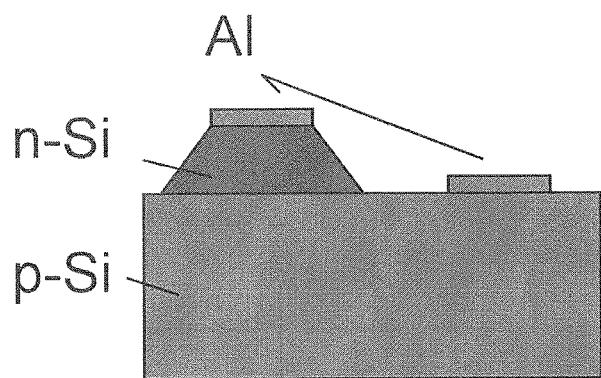


Fig. 35C

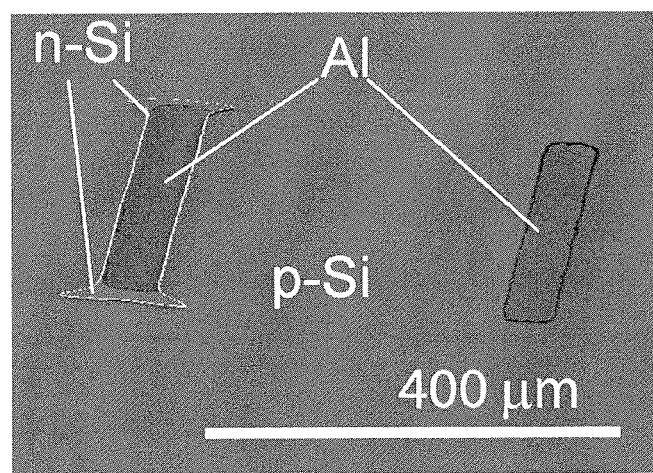


Fig. 35D

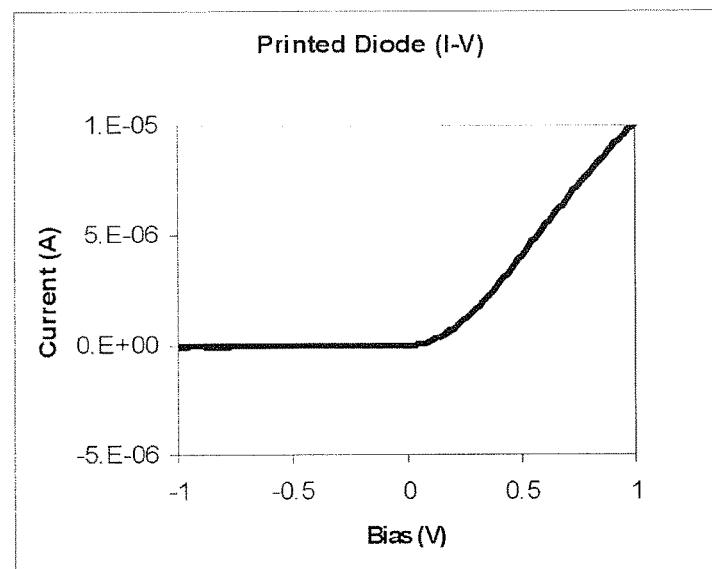
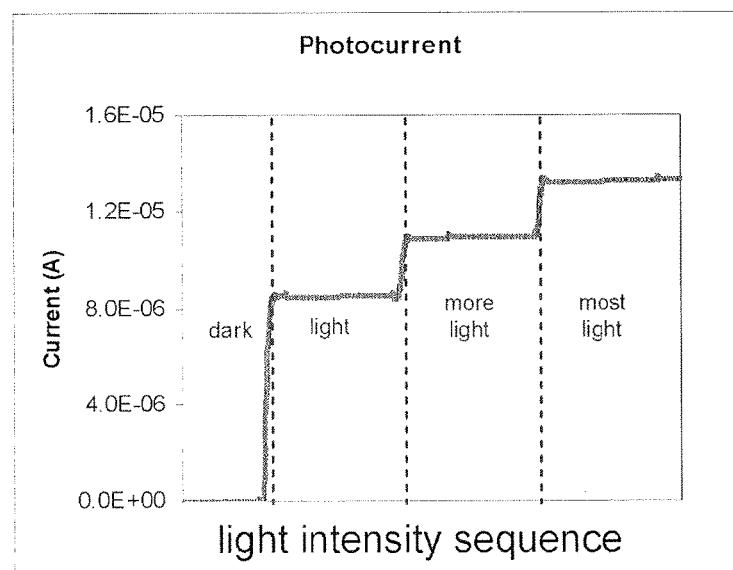


Fig. 35E



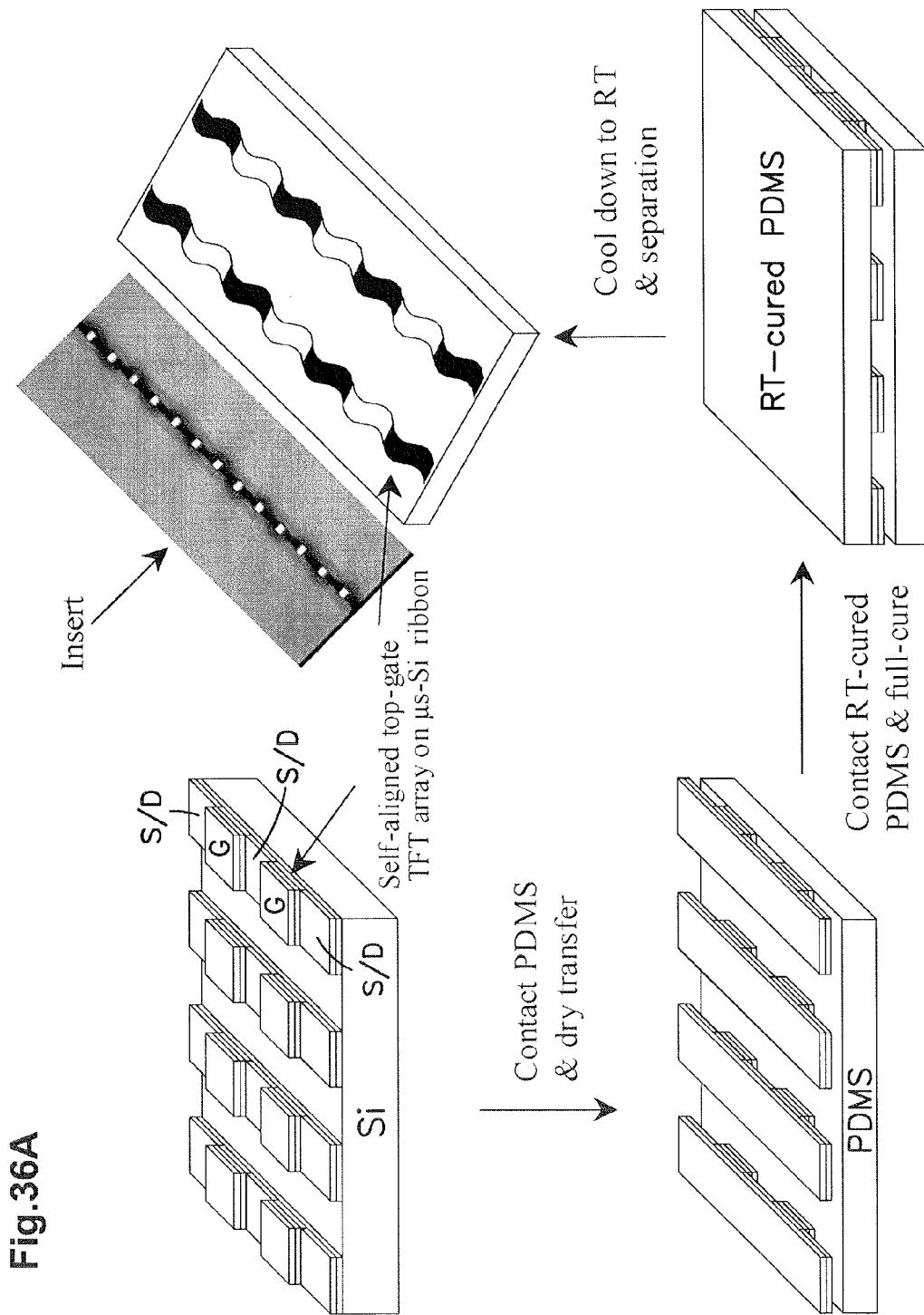
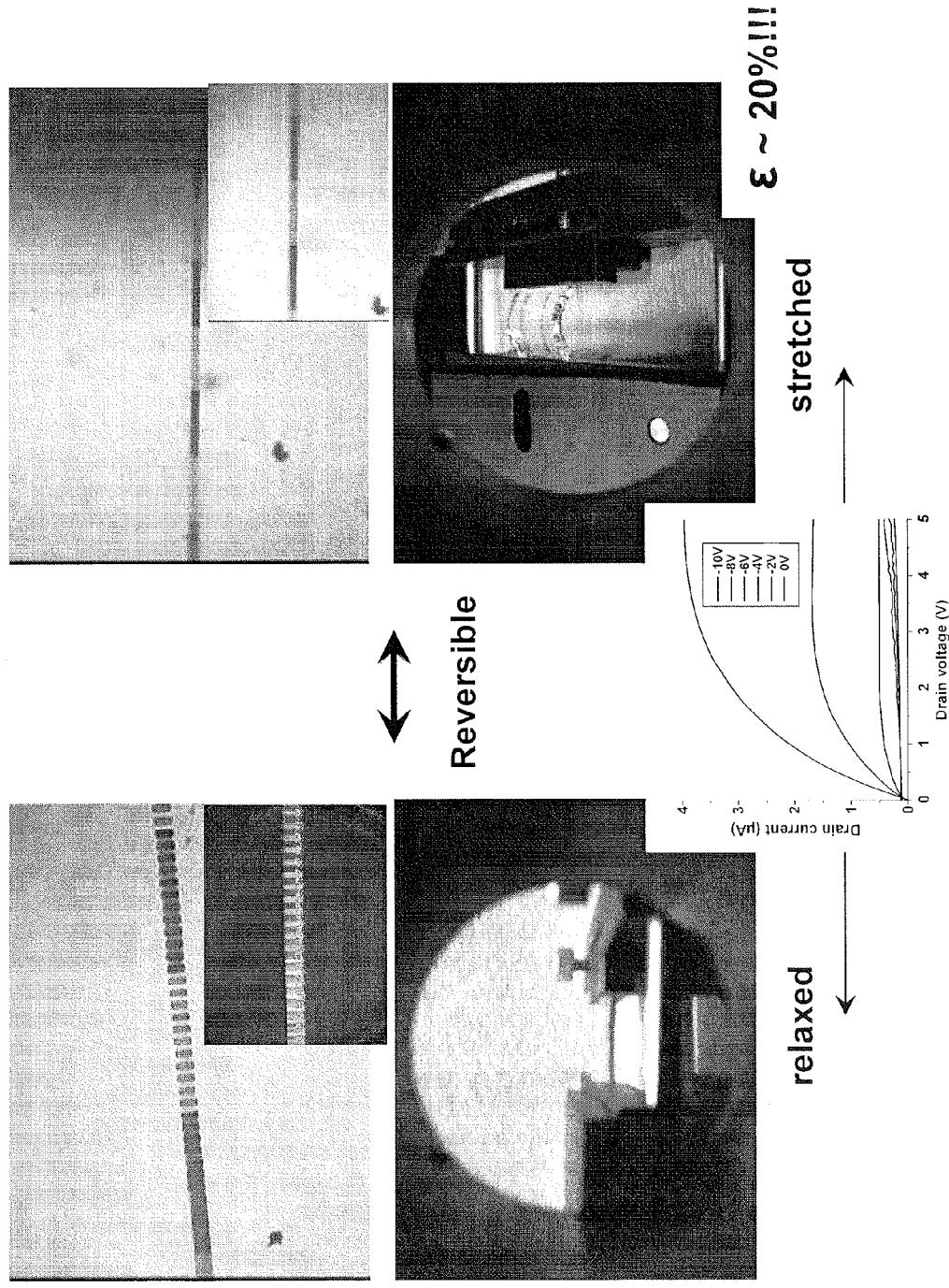


Fig. 36B      **Stretchable  $\mu$ -Si Transistors on Rubber Substrates**



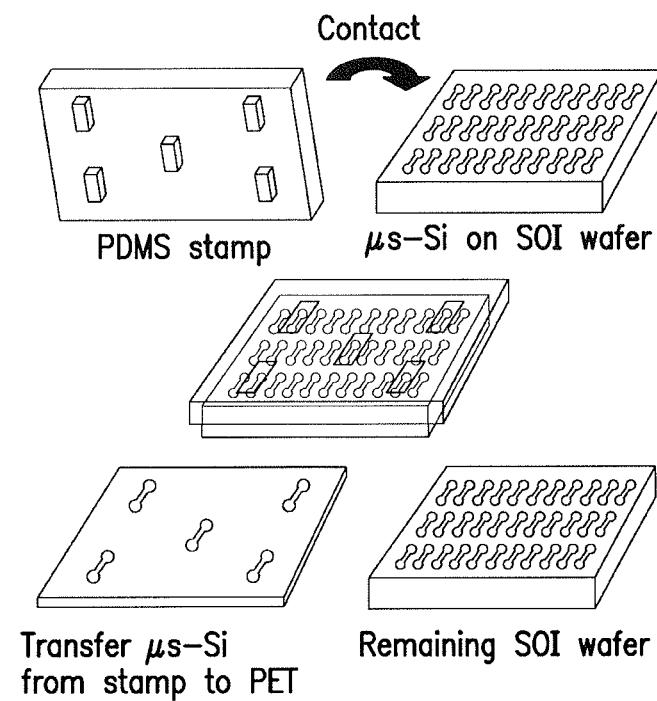
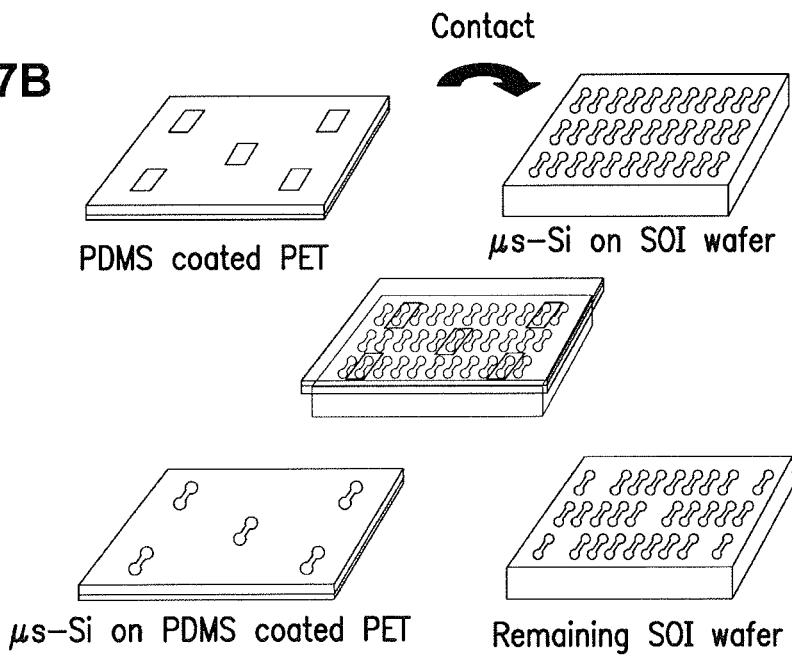
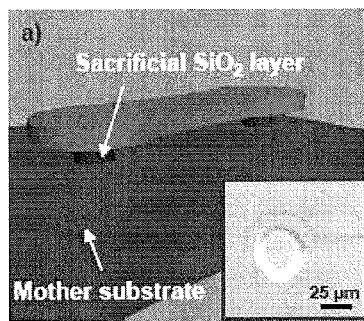
**Fig.37A****Fig.37B**

Fig. 38A



b)

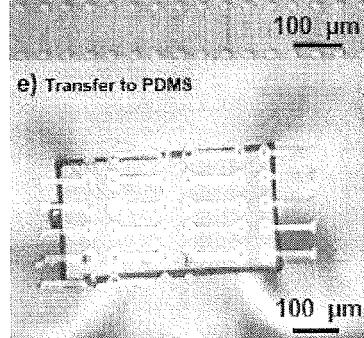


c) SOI after Etching BOX

d) SOI after transfer

Fig. 38C

Fig. 38B



e) Transfer to PDMS



Fig. 38F

Fig. 38E

Fig. 38D

Fig. 39A

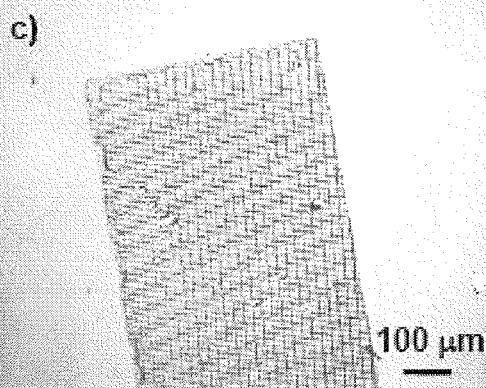
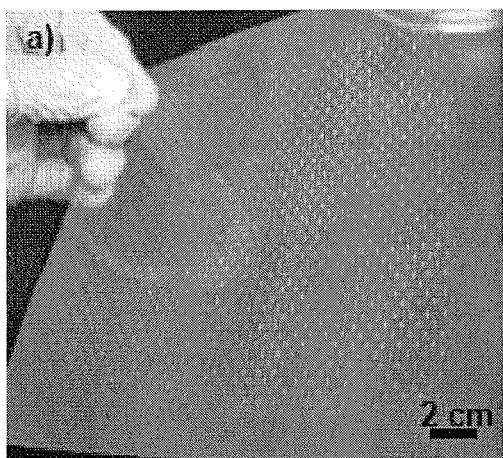


Fig. 39C

Fig. 39B

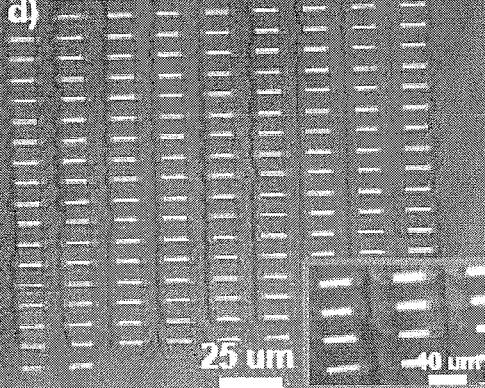
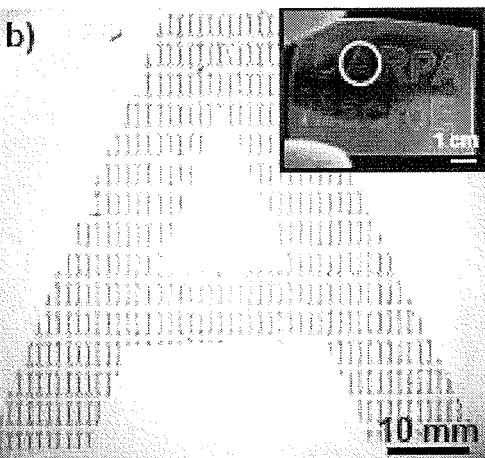


Fig. 39D

Fig. 40A

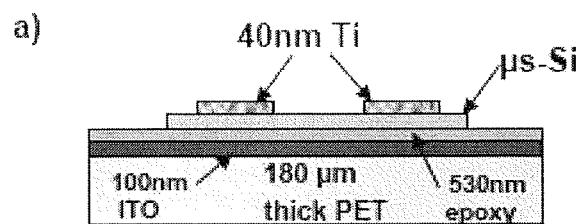


Fig. 40B

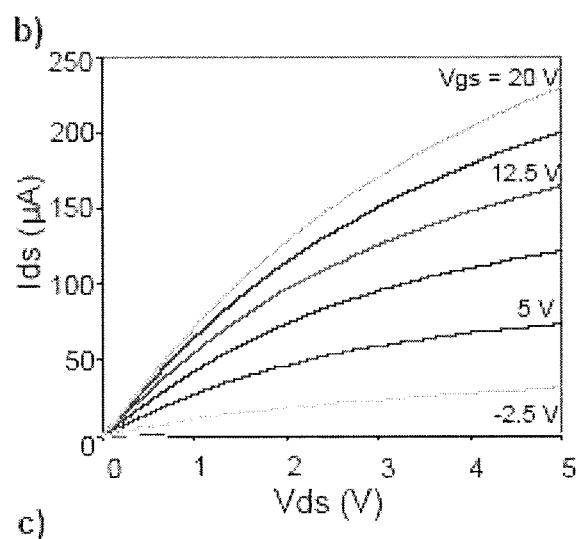


Fig. 40C

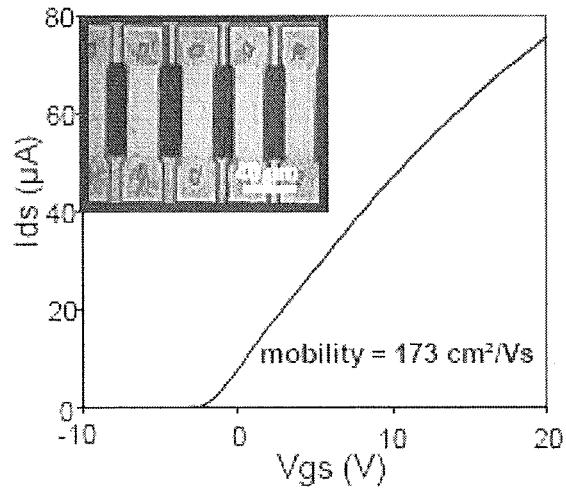


Fig. 41

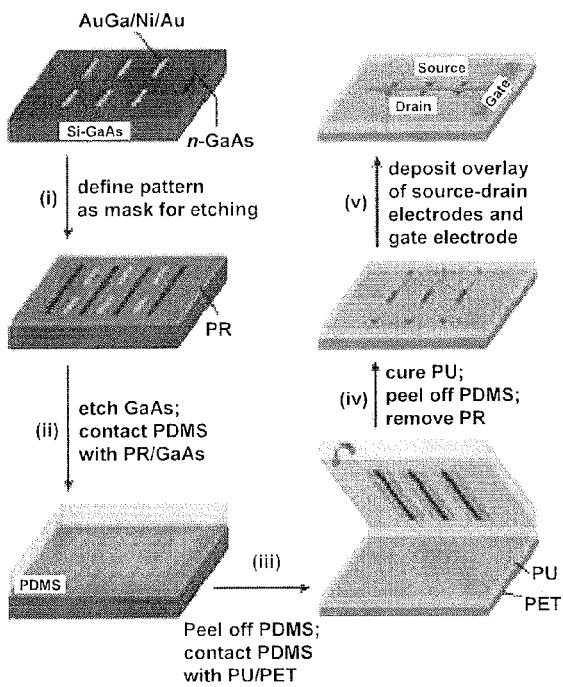


Fig. 42A

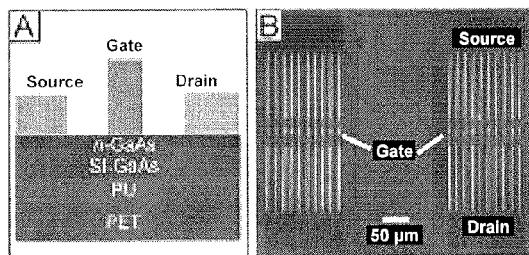


Fig. 42B

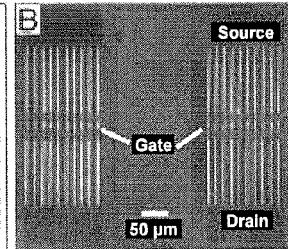
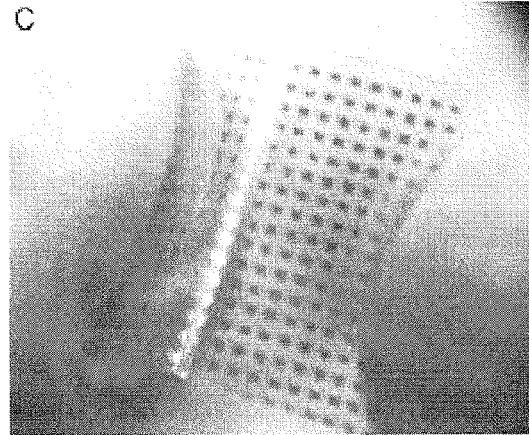
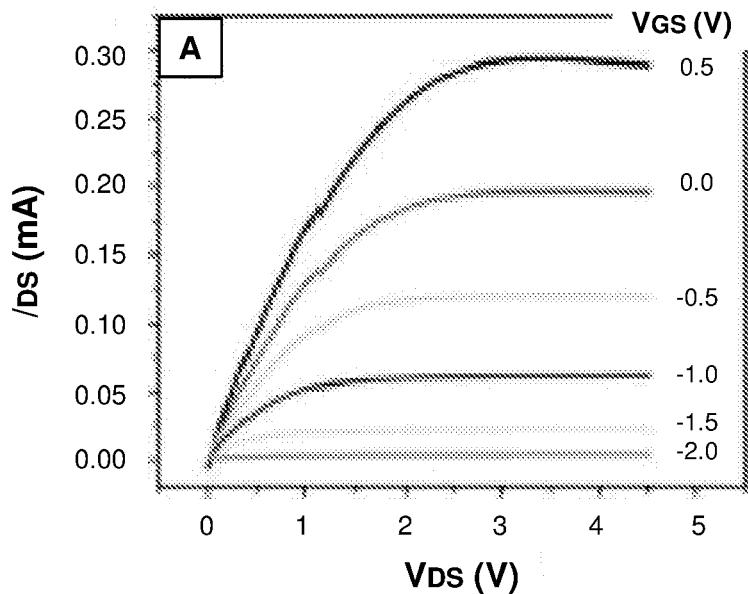
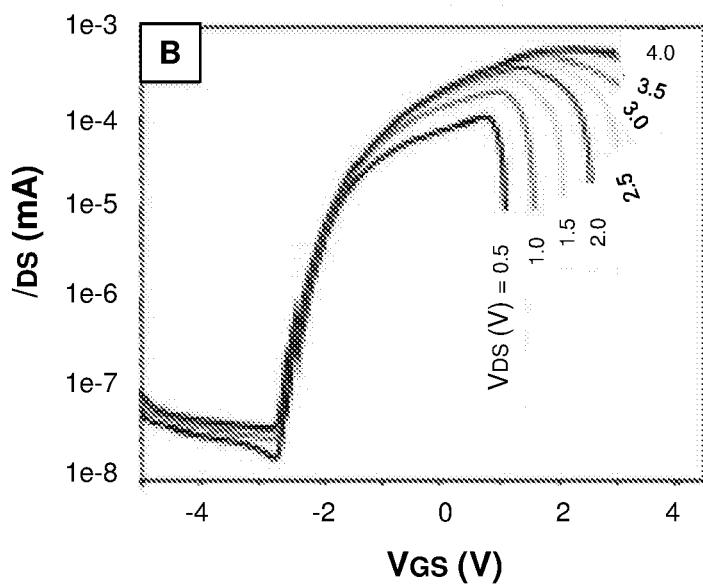


Fig. 42C



**FIG. 43A****FIG. 43B**

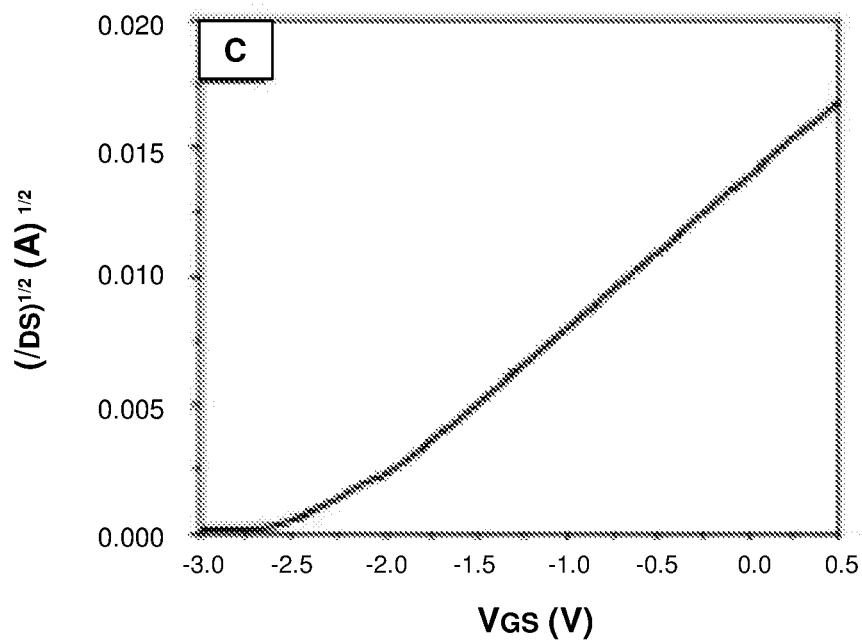
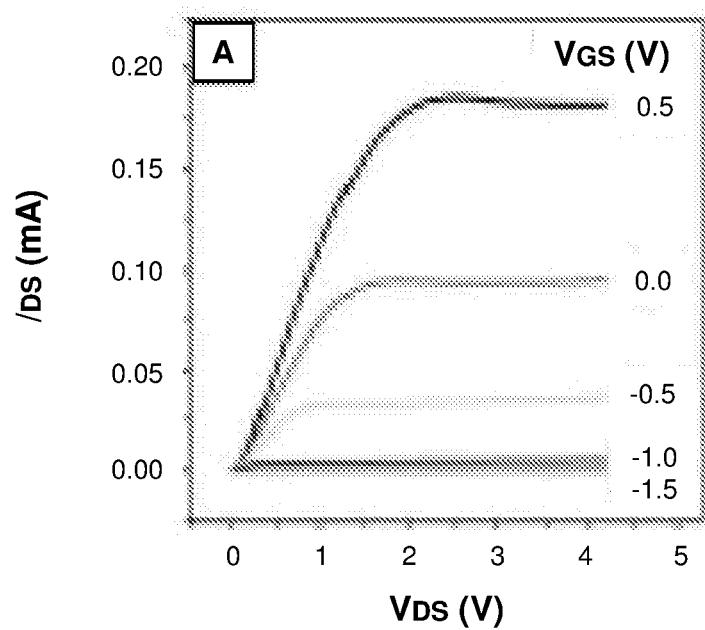
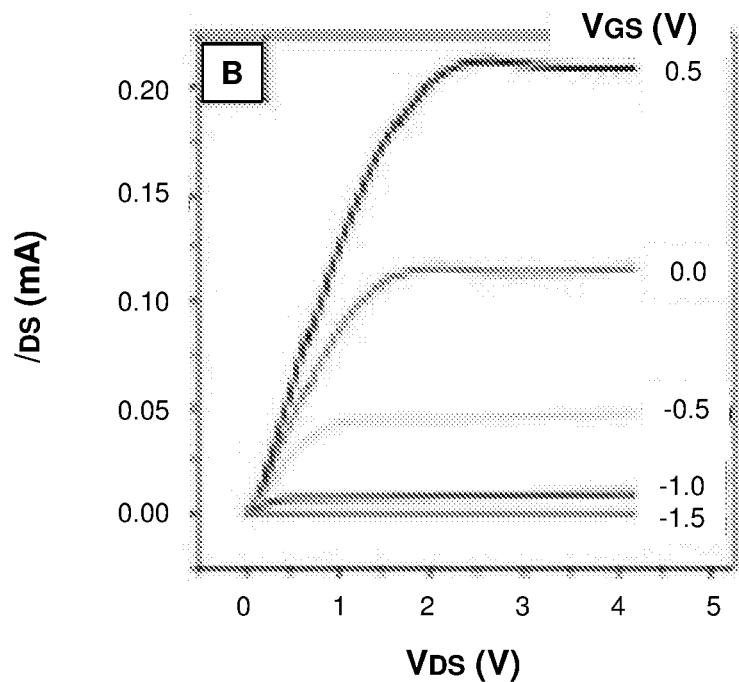


FIG. 43C

**FIG. 44A****FIG. 44B**

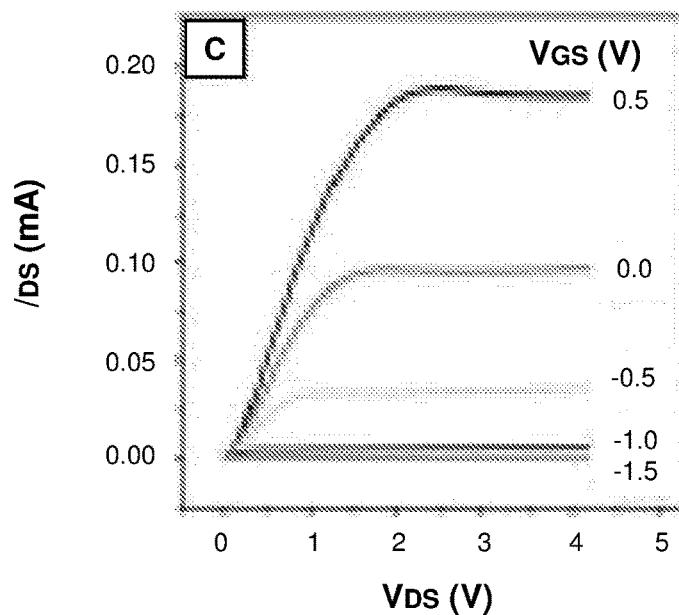
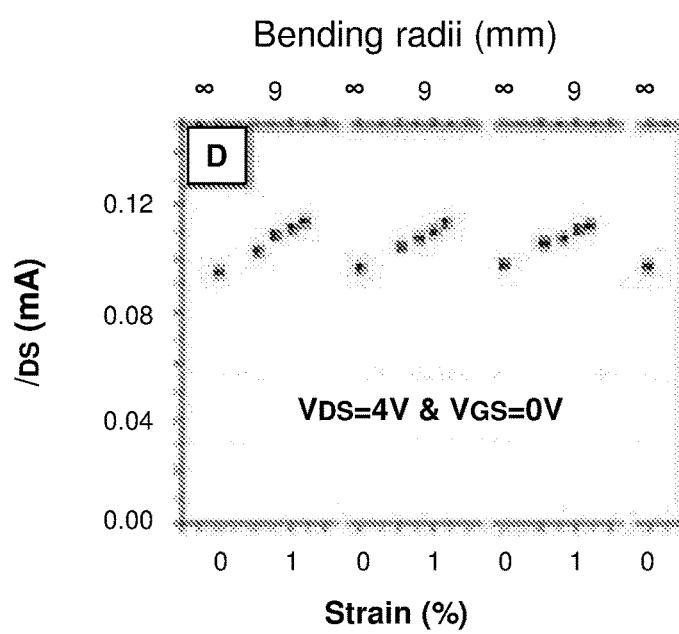
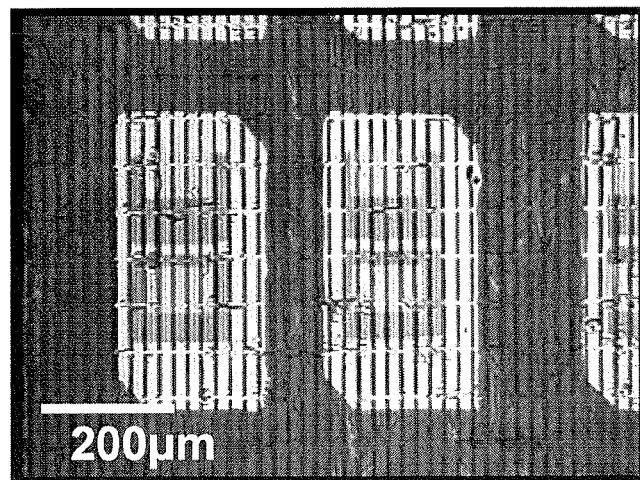
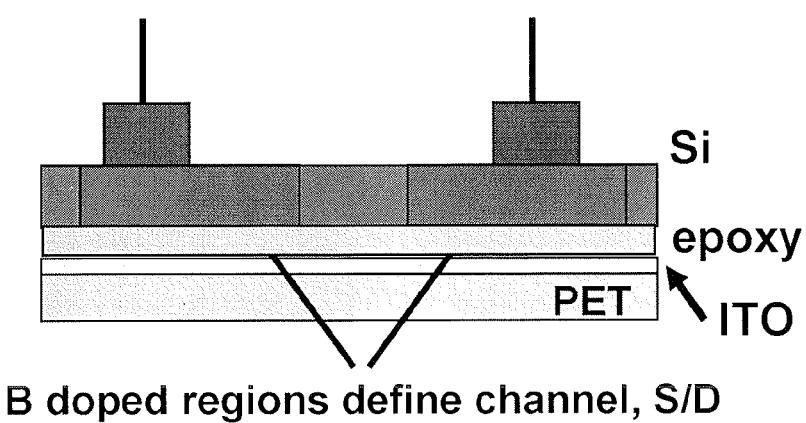
**FIG. 44C****FIG. 44D**

Fig. 45: P Type  $\mu$ S-Si bottom gate TFTs



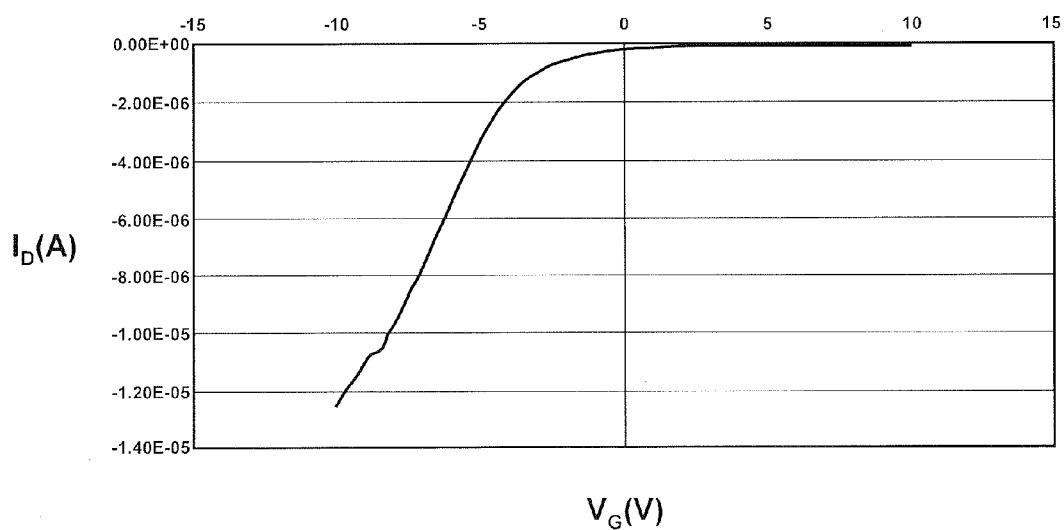
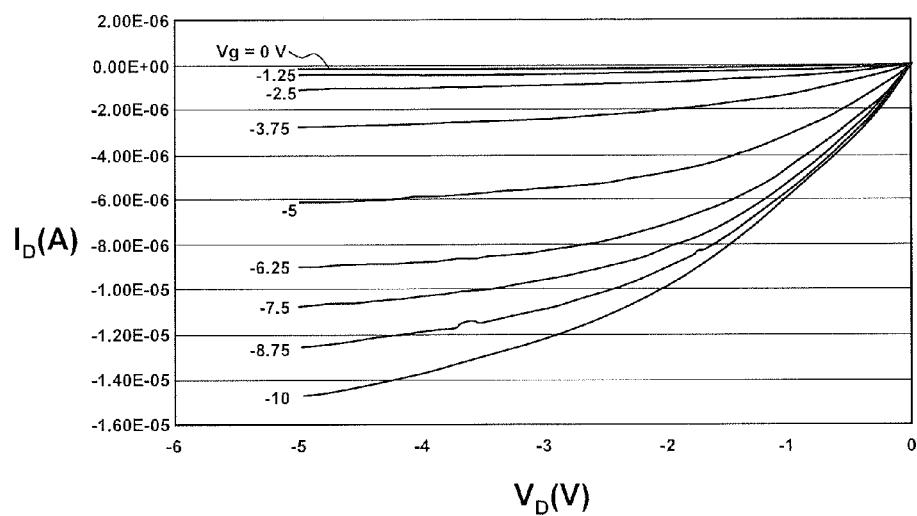
Mobilities btwn 80 & 150 cm<sup>2</sup>/Vs

Fig. 45 (cont'd)

Fig. 46: Complementary Logic Gate (Inverter) on Plastic

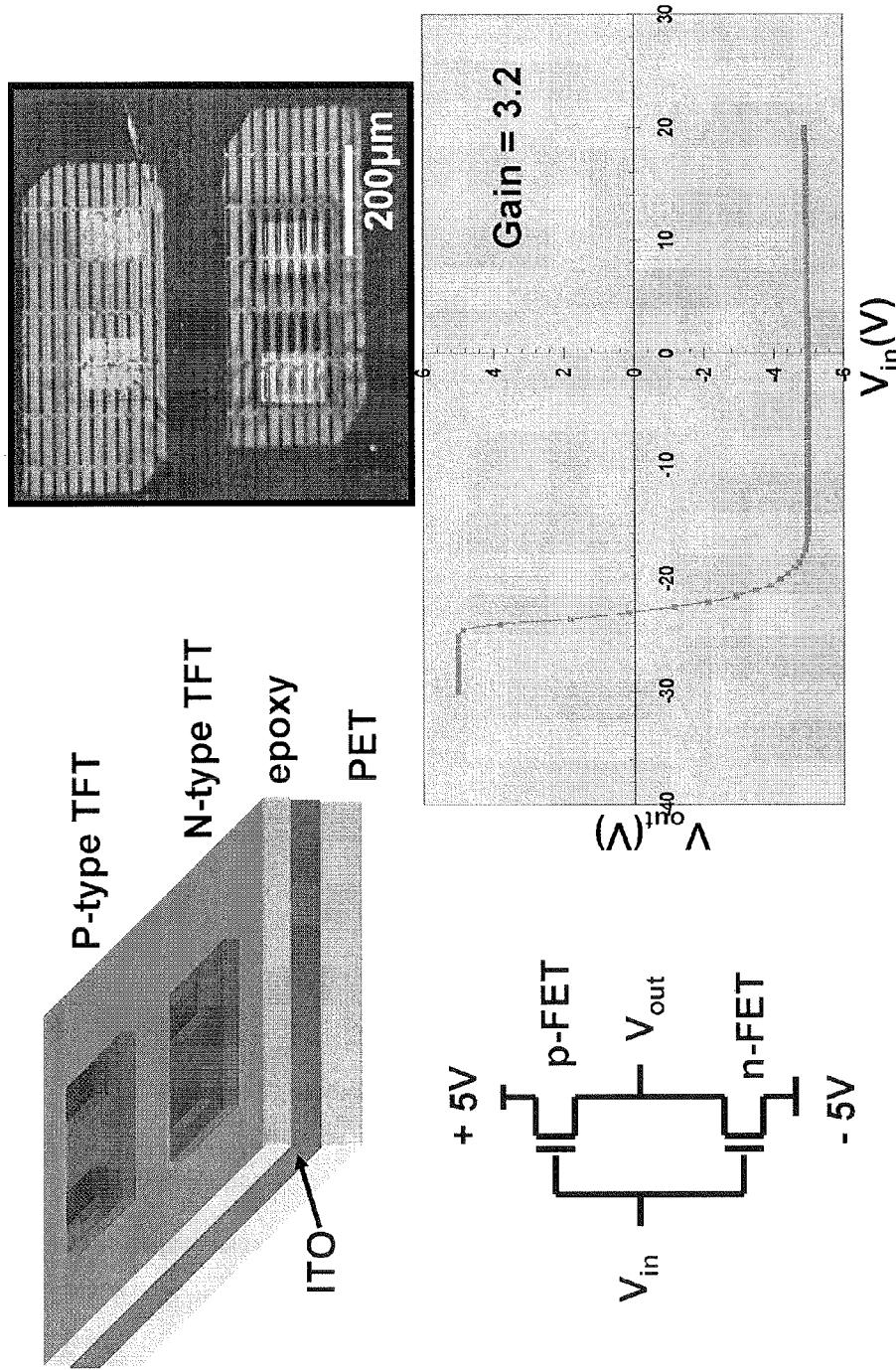
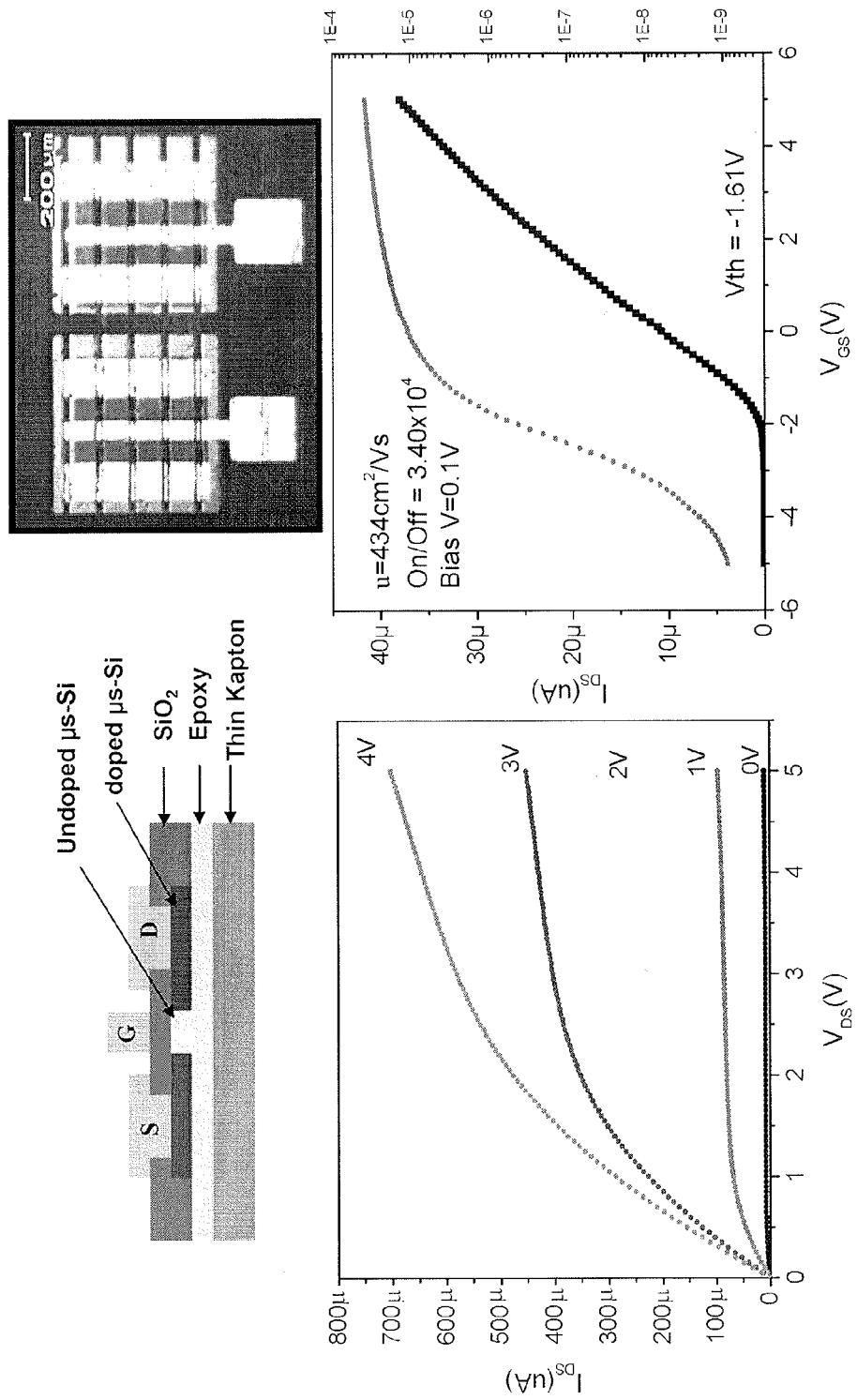


Fig. 47: Top Gate  $\mu$ s-Si Transistors on Plastic



**1**

**METHODS AND DEVICES FOR  
FABRICATING AND ASSEMBLING  
PRINTABLE SEMICONDUCTOR ELEMENTS**

**CROSS REFERENCE TO RELATED  
APPLICATIONS**

This application is a continuation of U.S. patent application Ser. No. 14/155,010, filed Jan. 14, 2014, which is a continuation of U.S. patent application Ser. No. 13/801,868, filed Mar. 13, 2013, now U.S. Pat. No. 8,664,699, which is a continuation of U.S. patent application Ser. No. 13/113,504, filed on May 23, 2011, now U.S. Pat. No. 8,440,546, which is a continuation of U.S. patent application Ser. No. 12/564,566, filed on Sep. 22, 2009, now U.S. Pat. No. 7,982,296, which is a division of U.S. Nonprovisional patent application Ser. No. 11/145,574, filed Jun. 2, 2005, now U.S. Pat. No. 7,622,367, which claims priority under 35 U.S.C. 119(e) to U.S. Provisional Patent Application Nos. 60/577,077, 60/601,061, 60/650,305, 60/663,391 and 60/677,617, filed on Jun. 4, 2004, Aug. 11, 2004, Feb. 4, 2005, Mar. 18, 2005, and May 4, 2005, respectively, all of which are hereby incorporated by reference in their entireties to the extent not inconsistent with the disclosure herein.

**STATEMENT REGARDING FEDERALLY  
SPONSORED RESEARCH OR DEVELOPMENT**

This invention was made, at least in part, with United States governmental support awarded by Department of Energy under Grant No. DEFG02-91 ER45439 and the Defense Advanced Projects Agency under Contract F8650-04-C-710. The United States Government has certain rights in this invention.

**BACKGROUND OF INVENTION**

Since the first demonstration of a printed, all polymer transistor in 1994, a great deal of interest has been directed at a potential new class of electronic systems comprising flexible integrated electronic devices on plastic substrates. [Garnier, F., Hajlaoui, R., Yassar, A. and Srivastava, P., Science, Vol. 265, pgs 1684-1686] Recently, substantial research has been directed toward developing new solution processable materials for conductors, dielectrics and semiconductors elements for flexible plastic electronic devices. Progress in the field of flexible electronics, however, is not only driven by the development of new solution processable materials but also by new device component geometries, efficient device and device component processing methods and high resolution patterning techniques applicable to plastic substrates. It is expected that such materials, device configurations and fabrication methods will play an essential role in the rapidly emerging new class of flexible integrated electronic devices, systems and circuits.

Interest in the field of flexible electronics principally arises out of several important advantages provided by this technology. First, the mechanical ruggedness of plastic substrate materials provides electronic devices less susceptible to damage and/or electronic performance degradation caused by mechanical stress. Second, the inherent flexibility of these substrate materials allows them to be integrated into many shapes providing for a large number of useful device configurations not possible with brittle conventional silicon based electronic devices. For example, bendable flexible electronic devices are expected to enable fabrication of new devices, such as electronic paper, wearable computers and

**2**

large-area high resolution displays, that are not easily achieved with established silicon based technologies. Finally, the combination of solution processable component materials and plastic substrates enables fabrication by continuous, high speed, printing techniques capable of generating electronic devices over large substrate areas at low cost.

The design and fabrication of flexible electronic devices exhibiting good electronic performance, however, present a number of significant challenges. First, the well developed methods of making conventional silicon based electronic devices are incompatible with most plastic materials. For example, traditional high quality inorganic semiconductor components, such as single crystalline silicon or germanium semiconductors, are typically processed by growing thin films at temperatures (>1000 degrees Celsius) that significantly exceed the melting or decomposition temperatures of most plastic substrates. In addition, most inorganic semiconductors are not intrinsically soluble in convenient solvents that would allow for solution based processing and delivery. Second, although many amorphous silicon, organic or hybrid organic-inorganic semiconductors are compatible with incorporation into plastic substrates and can be processed at relatively low temperatures, these materials do not have electronic properties capable of providing integrated electronic devices capable of good electronic performance. For example, thin film transistors having semiconductor elements made of these materials exhibit field effect mobilities approximately three orders of magnitude less than complementary single crystalline silicon based devices. As a result of these limitations, flexible electronic devices are presently limited to specific applications not requiring high performance, such as use in switching elements for active matrix flat panel displays with non-emissive pixels and in light emitting diodes.

Progress has recently been made in extending the electronic performance capabilities of integrated electronic devices on plastic substrates to expand their applicability to a wider range of electronics applications. For example, several new thin film transistor (TFT) designs have emerged that are compatible with processing on plastic substrate materials and exhibit significantly higher device performance characteristics than thin film transistors having amorphous silicon, organic or hybrid organic-inorganic semiconductor elements. One class of higher performing flexible electronic devices is based on polycrystalline silicon thin film semiconductor elements fabricated by pulse laser annealing of amorphous silicon thin films. While this class of flexible electronic devices provides enhanced device electronic performance characteristics, use of pulsed laser annealing limits the ease and flexibility of fabrication of such devices, thereby significantly increasing costs. Another promising new class of higher performing flexible electronic devices is devices that employ solution processable nanoscale materials, such as nanowires, nanoribbons, nanoparticles and carbon nanotubes, as active functional components in a number of macroelectronic and microelectronic devices.

Use of discrete single crystalline nanowires or nanoribbons has been evaluated as a possible means of providing printable electronic devices on plastic substrates that exhibit enhanced device performance characteristics. Duan et al. describe thin film transistor designs having a plurality of selectively oriented single crystalline silicon nanowires or CdS nanoribbons as semiconducting channels [Duan, X., Niu, C., Sahl, V., Chen, J., Parce, J., Empedocles, S. and Goldman, J., Nature, Vol. 425, pgs. 274-278]. The authors

report a fabrication process allegedly compatible with solution processing on plastic substrates in which single crystalline silicon nanowires or CdS nanoribbons having thicknesses less than or equal to 150 nanometers are dispersed into solution and assembled onto the surface of a substrate using flow-directed alignment methods to produce the semiconducting element of a thin film transistor. An optical micrograph provided by the authors suggests that the disclosed fabrication process prepares a monolayer of nanowires or nanoribbons in a substantially parallel orientation and spaced apart by about 500 nanometers to about 1,000 nanometers. Although the authors report relatively high intrinsic field effect mobilities for individual nanowires or nanoribbons ( $\approx 119 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ), the overall device field effect mobility has recently been determined to be “approximately two orders of magnitude smaller” than the intrinsic field effect mobility value reported by Duan et al. [Mitzi, D. B., Kosbar, L. L., Murray, C. E., Copel, M., Afzali, A., *Nature*, Vol. 428, pgs. 299-303]. This device field effect mobility is several orders of magnitude lower than the device field effect mobilities of conventional single crystalline inorganic thin film transistors, and is likely due to practical challenges in aligning, densely packing and electrically contacting discrete nanowires or nanoribbons using the methods and device configurations disclosed in Duan et al.

Use of a nanocrystal solutions as precursors to polycrystalline inorganic semiconductor thin films has also been explored as a possible means of providing printable electronic devices on plastic substrates that exhibit higher device performance characteristics. Ridley et al. disclose a solution processing fabrication method wherein a solution cadmium selenide nanocrystals having dimensions of about 2 nanometers is processed at plastic compatible temperatures to provide a semiconductor element for a field effect transistor. The authors report a method wherein low temperature grain growth in a nanocrystal solution of cadmium selenide provides single crystal areas encompassing hundreds of nanocrystals. Although Ridley et al. report improved electrical properties relative to comparable devices having organic semiconductor elements, the device mobilities achieved by these techniques ( $\approx 1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ) are several orders of magnitude lower than the device field effect mobilities of conventional single crystalline inorganic thin film transistors. Limits on the field effect mobilities achieved by the device configurations and fabrication methods of Ridley et al. are likely to arise from the electrical contact established between individual nanoparticles. Particularly, the use of organic end groups to stabilize nanocrystal solutions and prevent agglomeration may impede establishing good electrical contact between adjacent nanoparticles that is necessary for providing high device field effect mobilities.

Although Duan et al. and Ridley et al. provide methods for fabricating thin film transistors on plastic substrates, the device configurations described employ transistors comprising mechanically rigid device components, such as electrodes, semiconductors and/or dielectrics. Selection of a plastic substrate with good mechanical properties may provide electronic devices capable of performing in flexed or distorted orientations. However, such motion is expected to generate mechanical strain on the individual rigid transistor device components. This mechanical strain may induce damage to individual components, for example by cracking, and also may degrade or disrupt electrical contact between device components.

It will be appreciated from the foregoing that there is currently a need in the art for methods and device configurations for fabricating integrated electronic semiconductor

containing devices on plastic substrates. Printable semiconductor elements having good electrical characteristics are needed to allow effective device fabrication at temperatures compatible with assembly on plastic polymer substrates. In addition, methods of printing semiconductor materials onto large areas of plastic substrates are needed to enable continuous, high speed printing of complex integrated electrical circuits over large substrate areas. Finally, fully flexible electronic devices capable of good electronic performance in flexed or deformed device orientations are needed to enable a wide range of new flexible electronic devices.

#### SUMMARY OF THE INVENTION

The present invention provides methods, devices and device components for fabricating structures and/or devices, such as semiconductor-containing electronic devices, on substrate surfaces, such as plastic substrates. Specifically, the present invention provides printable semiconductor elements for fabricating electronic devices, optoelectronic devices and other functional electronic assemblies by flexible, low cost printing methods. It is an object of the present invention to provide methods and devices for fabricating semiconductor elements, such as unitary single crystalline inorganic semiconductors having selected physical dimensions ranging from about 10 s of nanometers to about 10 s of centimeters, which are capable of high precision assembly on substrate surfaces via a range of printing techniques. It is another object of the present invention to provide methods for assembling and/or patterning printable semiconductor elements using dry transfer contact printing and/or solution printing techniques which provide good placement accuracy and pattern fidelity over large substrate areas. It is further an object of the present invention to provide good electronic performance integrated electronic and/or optoelectronic devices comprising one or more printable semiconductor elements supported by a plastic substrate, particularly fully flexible thin film transistors having printable semiconductor elements exhibiting good electronic performance characteristics, such as field effect mobilities, threshold voltages and on-off ratios.

In one aspect the present invention provides methods of fabricating high performance electronic and/or optoelectronic devices or device components having one or more printable components, such as a printable semiconductor element. Electronic and optoelectronic devices which may be fabricated by the methods of the present invention, include but are limited to, transistors, diodes, light emitting diodes (LEDs), lasers, organic light emitting diodes (OLEDs), microelectromechanical systems (MEMS) and nanoelectromechanical systems (NEMS). Particularly, the present invention provides methods of assembling semiconductor elements and/or other device components via printing techniques into electronic and/or optoelectronic devices or device components which exhibit performance characteristics comparable to single crystalline semiconductor based devices fabricated by conventional high temperature processing methods.

In an embodiment of the present invention useful for device fabrication on substrates having low melting or decomposition temperatures, such as plastic substrates and semiconductor substrates, methods of the present invention comprise independently performable fabrication steps of: (1) forming one or more discrete, high quality semiconductor elements and (2) assembling and/or patterning these semiconductor elements and other device components on a substrate surface. For example, the present invention

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includes methods wherein independent, high quality printable inorganic semiconductors are generated by masking and etching bulk single crystalline inorganic semiconductor materials fabricated by conventional high temperature processing methods, such as high temperature (>1000 Celsius) film growth, doping and other processing techniques. After fabrication, such printable inorganic semiconductors are assembled onto one or more substrates surface by printing techniques which may be performed at relatively low temperatures (<about 400 degrees Celsius). An advantage of having independently performable preparation and patterning/assembly steps is that each step may be performed at ambient conditions, such as temperatures and ambient contamination levels (i.e. if clean room conditions are needed), which optimize the efficiencies, flexibilities and utilities of each independently performable fabrication step. For example, the present methods allow semiconductor materials to be fabricated at the high temperatures needed to generate high quality single crystalline semiconductors. Semiconductor element patterning and/or assembly, however, may be subsequently carried out at substantially lower temperatures favorable for device fabrication on substrates having low melting or decomposition temperatures, such as plastic substrates. In this manner, high performance devices may be fabricated on a wide range of substrate surfaces without significant melting, decomposition or damage to the substrate surface. Another advantage of separating semiconductor fabrication from semiconductor/device assembly is that integration of the semiconductor elements into high performance devices and device components may be achieved by a wide range of low cost and flexible assembly methods, such as dry transfer and solution printing techniques, which do not require clean room conditions and are compatible with continuous, high speed device fabrication on large areas of substrates. In the context of this aspect of the present invention, the present methods are compatible with printing on substrates comprising virtually any material, including plastic substrates and non-plastic substrates, such as semiconductor wafers, for example silicon wafers or GaAs wafers.

In another aspect, the present invention provides printable semiconductor elements for integration into high performance electrical and optoelectronic devices and device components. In the context of the present invention, the term "printable" relates to materials, structures, device components and/or integrated functional devices that may be transferred, assembled, patterned, organized and and/or integrated onto or into substrates without exposure of the substrate to high temperatures (i.e. at temperatures less than or equal to about 400 degrees Celsius). Printable semiconductors of the present invention may comprise semiconductor structures that are able to be assembled and/or integrated onto substrate surfaces by dry transfer contact printing and/or solution printing methods. Exemplary semiconductor elements of the present invention may be fabricated by "top down" processing of a range of inorganic semiconductor materials including, but not limited to, single crystalline silicon wafers, silicon on insulator wafers, polycrystalline silicon wafers and GaAs wafers. Printable semiconductor elements derived from high quality semiconductor wafers, for example semiconductor wafers generated using conventional high temperature vapor deposition processing techniques, are beneficial for applications requiring good electronic performance because these materials have better purities and extents of crystallization than materials prepared using "bottom up" processing techniques, such as conventional techniques for making nanocrystals and

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nanowires. Another advantage provided by the "top-down" processing methods of the present invention is that printable semiconductor elements and arrays of printable semiconductor elements may be fabricated in well defined orientations and patterns, unlike "bottom-up" processing methods typically used for fabricating nanowires and nanoparticles. For example, semiconductor elements may be fabricated in arrays having positions and spatial orientations directly corresponding to the eventual positions and spatial orientations of these elements in functional devices or arrays of functional devices, such as transistor arrays or diode arrays.

Printable semiconductor elements may comprise unitary, single crystalline inorganic semiconductor structures having wide range of shapes, such as ribbon (or strips), discs, platelets, blocks, post, cylinders or any combinations of these shapes. Printable semiconductor elements of the present invention may have a wide range of physical dimensions, for example, thicknesses ranging from about 10 nanometers to about 100 microns, widths ranging from about 50 nanometers to about 1 millimeter and lengths ranging from about 1 micron to about 1 millimeter. Use of semiconductor elements having thicknesses greater than about 10 nanometers and widths greater than about 500 nanometer are preferred for some application because these dimensions may provide electronic devices exhibiting good electronic performance, such as thin film transistors having a device field effect mobility greater than or equal to about  $100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , and preferably greater than or equal to about  $300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and more preferably greater than or equal to about  $800 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . In addition, semiconductor elements having widths greater than about 10 nanometers can be assembled on substrates by a range of printing techniques with good placement accuracy and pattern fidelity.

Printable semiconductor elements of the present invention may also be provided with an alignment maintaining element that mechanically connects the printable semiconductor element to a mother substrate, such as a semiconductor wafer. Alignment maintaining elements are useful for maintaining a selected orientation and/or position of a printable semiconductor element during transfer, assembly and/or integration processing steps. Alignment maintaining elements are also useful for maintaining relative positions and orientations of a plurality of semiconductor elements defining a selected pattern of semiconductor elements during transfer, assembly and/or integration processing steps. In methods of the present invention, alignment maintaining elements preserve selected positions and orientations during contact (and bonding) of the printable semiconductor elements with the contact surface of a conformable transfer device. Useful alignment maintaining elements in this aspect of the present invention are capable of disengaging from the printable semiconductor elements upon movement of the conformable transfer device without significantly changing the selected positions and orientations of the printable semiconductor elements. Disengagement is typically achieved by fracture or release of the alignment maintaining elements during movement of the transfer device.

In one embodiment of the present invention, the printable semiconductor element has a peanut shape characterized by wider ends and a narrow central region. In this embodiment, alignment maintaining elements are provided via incomplete isotropic etching beneath the wider ends and complete isotropic etching beneath the central region. This processing lead to a semiconductor element connected to a mother substrate a two points corresponding to each end of the semiconductor element. In another embodiment, the printable semiconductor element has a ribbon shape extending

along a central longitudinal axis. In this embodiment, alignment maintaining elements connect the both ends of the ribbon along the longitudinal axis to the mother substrate. In each embodiment, binding of the ribbon shaped or peanut shaped semiconductor element to the contact surface of a transfer device and movement of the transfer device results in fracture of both alignment maintaining elements and release of the printable semiconductor element from the mother substrate.

Printable semiconductor elements of the present invention have independently selectable physical dimensions, such as widths, heights, thicknesses surface roughness, and flatness, that are selectable with a high degree of accuracy. In an exemplary embodiment, physical dimensions of printable semiconductor elements may be selected to within less than about 5%. Large numbers of printable semiconductor elements having highly uniform selected physical dimension may be fabricated using the methods of the present invention. In an exemplary embodiment, large numbers of printable semiconductor elements can be fabricated having physical dimensions that vary by less than about 1%. The present invention, therefore, provides printable semiconductor elements without a significant size and shape distributions, in contrast to conventional methods of generating nanowires. A significant advantage of this approach is that structures and devices that integrate printable semiconductor elements of the present invention do not need to be built to tolerate dispersion in size and shape of the semiconductor elements. In some embodiments, printable semiconductor elements of the present invention have very low surface roughness, for example having a surface roughness less than about 0.5 nanometers root mean square. Printable semiconductor elements of the present invention may have one or more flat surfaces. This configuration is beneficial in some device fabrication applications because flat surfaces are useful for establishing interfaces with other device components, such as conducting, semiconducting and/or dielectric device components.

Further, the present methods and compositions of matter provide printable semiconductor elements comprising high quality semiconductor materials. In some embodiments useful for fabricating high performance electrical devices, printable semiconductor elements have a purity with a factor of about 1000 or less of conventional semiconductor wafer materials fabricated via high temperature processing techniques. For example, the present invention provides high purity semiconductor elements having oxygen impurities less than about 5 to 25 parts per million atoms, carbon impurities less than about 1 to 5 parts per million atoms, and heavy metal impurities less than or equal to about 1 part per million atoms (ppma), preferably less than or equal to about 100 parts per billion atoms (ppba) for some applications, and more preferably less than or equal to about 1 part per billion atoms (ppba) for some applications. Printable semiconductor elements having low levels of heavy metal impurities (e.g. less than about 1 parts per million atoms) are beneficial for applications and devices requiring good electronic performance, as the presence of heavy metals in semiconductor materials can severely degrade their electrical properties.

In addition, printable semiconductor elements of some aspects of the present invention have a very low resistivity gradient, for example a less than about 5% to 10% variation across their areas. This aspect of the present invention provides enhanced doping uniformity with respect to conventional semiconductor materials derived from "bottom up" processing techniques, such as nanowire and nanocrystal materials. Further, printable semiconductor elements of

the present invention may comprise semiconductor materials exhibiting very few dislocations, for example less than 500 dislocations per square centimeter. Use of semiconductor elements comprising high quality semiconductor materials is beneficial for device fabrication applications requiring good electronic performance.

In addition, the present methods and compositions of matter provide printable semiconductor elements having highly uniform compositions. In this context, uniform composition refers to piece-to-piece uniformity with respect to purity, dopant concentrations, dopant spatial distributions and extents of crystallization. The high purities and good uniformity with respect to the composition of printable semiconductor elements of the present provide functional devices exhibiting enhanced reliability with respect to devices fabricated from conventional semiconductor materials derived from "bottom up" processing techniques, such as nanowire and nanocrystal materials.

Printable semiconductor elements of the present invention preferably have at least one smooth surface, such as the top or bottom surface of a microribbon, preferably exhibiting deviations from average surface position of less than 10 nanometers, and more preferably for some applications exhibiting deviations from average surface position of less than 1 Angstrom. Smooth surfaces of printable semiconductor elements of the present invention allow effective electrical contact and/or physical integration to be established with other device components in an integrated electronic device or optoelectronic device.

Alternatively, printable semiconductor elements of the present invention may comprise composite semiconductor elements having a semiconductor structure operationally connected to one or more additional structures, such as dielectric structures, conducting structures (e.g. electrode), additional semiconductor structures or any combination of these. Printable composite semiconductor elements provide materials and device components that may be easily and effectively integrated into complex electronic or optoelectronic devices. In addition, the assembly methods of the present invention allow printable semiconductor elements to be provided in array geometries wherein adjacent elements are close to each other, for example within 100 nanometers to 1 micron of each other. For example, a printable semiconductor element of the present invention comprises a unitary structure having a high quality semiconductor structure, such as a single crystalline inorganic semiconductor, operationally connected to an inorganic dielectric structure, such as a silicon oxide layer. This embodiment of the present invention is particular useful for fabrication of high performance thin film transistors because semiconductor and dielectric components may be assembled in a single printing step, and because use of unitary structures comprising both semiconductor and dielectric components results in insulator configurations exhibiting very low leakage of electric current from gate electrode to the semiconductor element or source and drain electrodes. In another embodiment, printable semiconductor elements of the present invention may comprise integrated functional devices, such as diodes, LEDs, transistors and OLEDs, which may be easily incorporated onto substrate surfaces.

The methods and compositions of the present invention provide a processing platform enabling fabrication of functional devices exhibiting enhanced reliability with respect to devices based on semiconductor materials generated via "bottom up" processing techniques, such as nanowires and nanocrystals. In this context, reliability refers to the capability of a functional devices to exhibit good electronic

properties over extended operating periods and refers to piece-to-piece uniformity with respect to electrical properties of an ensemble of device fabricated using the present methods and compositions. For example, devices of the present invention exhibit very uniform threshold voltages (e.g. standard deviation of less than 0.08V) and very uniform device mobilities (e.g. standard deviation of less than about 13%). This represents improvements in uniformities of threshold voltages and device mobilities of a factor of about 40 and a factor of about 8, respectively, over nanowire based devices. The exceptional reliability of functional devices of the present invention is provided, at least in part, by the high degree of uniformity of the compositions and physical dimensions accessible using printable semiconductor elements of the present invention.

In another aspect, the present invention provides an electrical device comprising a first electrode, a second electrode and a printable semiconductor element positioned in electrical contact with said first and second electrodes. In one embodiment useful for applications requiring good electrical device performance, the printable semiconductor element comprises a unitary inorganic semiconductor structure having physical dimensions and shape that provides a fill factor between said first and second electrodes greater than or equal to about 20%, preferably greater than or equal to about 50% for some applications and more preferably greater than or equal to about 80% for some applications. Optionally, electrically devices of this embodiment may further comprise additional printable semiconductor elements, for example printable elements substantially longitudinally oriented, and optionally not in physical contact with each other. Importantly, multiple printable semiconductor elements of the present invention may be configured in devices or device arrays in a manner providing large fill factors (e.g. greater than or equal to 20%, 50% or 80%) and good electronic performance, in contrast to systems involving densely packed nanowire arrays. In one embodiment, the printable semiconductor element has at least one cross sectional dimension greater than or equal to about 500 nanometers. In one embodiment, the printable semiconductor element has a ratio of length to width equal to or less than about 10, preferably equal to or less than about 1.5 in for some applications. In one embodiment, the printable semiconductor element has a ratio of thickness to width equal to or less than about 0.1, preferably equal to or less than about 0.01 for some applications.

This aspect of the present invention further comprises arrays of electrical devices, such as transistors, diodes, photovoltaic devices, light emitting devices, comprising a first electrode, a second electrode and a plurality printable semiconductor elements positioned in electrical contact with the first and second electrode. In one embodiment, an array of electrical devices comprises over 20 printable semiconductor elements, preferably over 50 printable semiconductor elements for some applications and, more preferably over 100 printable semiconductor elements for some applications. In one embodiment useful for applications requiring good electrical device performance, the printable semiconductor elements provide a fill factor between said first and second electrodes greater than or equal to about 20%, preferably greater than or equal to about 50% for some applications and more preferably greater than or equal to about 80% for some applications. Printable semiconductor elements may be substantially longitudinally oriented with respect to a selected alignment axis, such as a selected alignment axis that extends along an axis which connects the closest points of said first and second electrical contacts. In

one embodiment, the relative positions and orientations of the printable semiconductor elements are selected to within less than or equal to about 5 microns. In one embodiment providing good end to end registration of the semiconductor elements, each of said printable semiconductor elements extends a length and terminates in first and second ends. In this embodiment, the first ends of said printable semiconductor elements are positioned within 5 microns of the first electrode and the second ends of said printable semiconductor elements are positioned within 5 microns of said second electrode. In one embodiment, an array of electrical devices of the present invention comprises a plurality of printable semiconductors are provided in a configuration such that they are substantially longitudinally oriented, are not in physical contact with each other (i.e. do not overlap), and are in electrical contact with first and second electrodes. In one embodiment, at least one physical dimension, such as average length, average width and/or average thickness, of the printable semiconductor elements in the array of electrical devices varies by less than about 10%, preferably less than about 5% for some applications. In this embodiment, the printable semiconductor elements in the array have selected physical dimensions, such as average lengths, average widths and/or average thickness, that do not vary significantly (i.e. less than about 10%) from each other.

In another aspect, the present invention provides a transistor having a printable semiconductor element. In one embodiment, a transistor of the present invention comprises a source electrode, a printable semiconductor element, a gain electrode and a gate electrode. In this configuration, the source electrode and gain electrode are both in electrical contact with, and separated by, the printable semiconductor element, and the gate electrode is separated from the printable semiconductor element by the dielectric. The printable semiconductor element may comprise a unitary crystalline inorganic semiconductor structure having a thickness greater than or equal to about 50 nanometers, preferably for some applications greater than or equal to 100 nanometers and even more preferably for some applications greater than or equal to 200 nanometers. The present invention also includes a transistor having a plurality of printable semiconductor elements in contact with source and drain electrodes. Use of a plurality of printable semiconductor elements in a single transistor may be beneficial in some applications because it may reduce the overall positional accuracy tolerances for various device components such as, source, drain and gate electrodes and dielectrics in field effect transistors. The present invention also includes embodiments wherein the printable semiconductor element is a stretchable semiconductor element. Use of one or more stretchable semiconductor elements in transistors of the present invention is beneficial because it provides good device performance and mechanical ruggedness in flexed, stretched or deformed device orientations.

In another embodiment, the present invention provides a high performance transistor supported by and/or in physical contact with a plastic substrate, such as a polyimide, polycarbonate or Mylar substrate. Transistors of this embodiment of the present invention may have a printable semiconductor element comprising a single crystalline inorganic semiconductor structure, such as a silicon or germanium. Such device configurations exhibit good device performance characteristics, such as field effect mobilities, threshold voltages, switching frequencies and on-off ratios. In an exemplary embodiment, a thin film transistor on a plastic substrate has a device field effect mobility comparable to the device field effect mobility of a transistor having a semi-

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conductor element comprising a crystalline semiconductor fabricated by conventional high temperature processing methods, for example a device field effect mobility greater than or equal to  $300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , more preferably greater than or equal to  $800 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . In another embodiment, the present invention provides a Si-MOS transistor having a single crystalline silicon printable semiconductor element capable of high frequency operation, such as operation at frequencies up to about 280 MHz.

In another embodiment, the present invention provides complementary metal-oxide semiconductor circuits comprising printable semiconductor elements. For example, printable semiconducting elements having lightly N (or P) type doped area between two highly P (or N) type doped area are used to form CMOS circuits. This capability is particularly interesting for applications requiring low power consumptions, as CMOS technology has a much smaller power dissipation over NMOS technology. Moreover, the CMOS technology has no static power dissipation, so this technology is particularly well suited for battery operated electronic systems. Finally, circuits design using CMOS technology are usually more compact than any over semiconductor technology, so more devices per surface area can be integrated.

In one embodiment, the dielectric and the semiconductor components of a transistor of this aspect of the present invention may comprise a unitary composite printable semiconductor element. Alternatively, the dielectric, gate electrode and semiconductor element of a transistor of this aspect of the present invention may comprise a unitary composite printable semiconductor element. Use of a composite printable semiconductor element having integrated semiconductor and insulator structures is preferred for some applications because it may provide very high quality dielectric—semiconductor interfaces in thin film transistors which exhibit very low leakage. In addition, use of a composite printable semiconductor element having integrated semiconductor and insulator structures also provides for efficient assembly of device components without the need for spin casting steps for integrating a dielectric layer in a thin film transistor.

In another embodiment, the present invention provides stretchable semiconductor elements capable of withstanding significant strain without fracturing. Stretchable semiconductor conductor elements of the present invention may exhibit good electronic performance even when undergoing significant strain, such as strain greater or equal about 0.5%, preferably 1% and more preferably 2%. Stretchable semiconductor elements of the present invention preferred for some applications are also flexible, and thus are capable of significant elongation, flexing, bending or deformation along one or more axes. Stretchable semiconductors that are flexible may also exhibit good electronic performance when in flexed, expanded, contracted, bent and/or deformed states. Stretchable and flexible semiconductor elements of the present invention may be printable, and may comprise composite semiconductor elements having a semiconductor structure operationally connected to other device components, such as dielectrics, electrodes and other semiconductors. The present invention includes a wide range of electronic and/or optoelectronic devices having stretchable and/or flexible semiconductor elements, such as transistors, diodes, LEDs, OLEDS, laser, micro- and nano-electromechanical devices.

A stretchable semiconductor element of the present invention comprises a flexible substrate having a supporting surface and a printable semiconductor structure having a

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curved internal surface. In this embodiment, at least a portion of the curved internal surface of the semiconductor structure is bonded to the supporting surface of the flexible substrate. Exemplary semiconductor structures having curved internal surfaces useful in present invention comprise bent semiconductor structures. In the context of this description, a “bent semiconductor structure” refers to a semiconductor structure having a curved conformation resulting from the application of a force. Bent semiconductor structures may have one or more folded regions. Bent semiconductor structures may be present in a coiled conformation or in a wrinkled conformation. Semiconductor structures having curved internal surfaces, such as bent semiconductor structures, may be bonded to a flexible substrate in a conformation that is under strain, such as a strain less than about 30%, a strain less than about 10% or a strain less than 1%.

Curved internal surfaces of stretchable semiconductors of the present invention may have any contour profile providing stretchability or flexibility including, but not limited to, contour profiles characterized by at least one convex region, at least one concave region or a combination of at least one convex region and at least one concave region. In an embodiment, the curved internal surface of a stretchable and/or flexible semiconductor element has a contour profile characterized by a substantially periodic wave or a substantially aperiodic wave. In the context of this description, periodic and aperiodic waves may be any two or three dimensional wave form including but not limited to, sine waves, square waves, Aries functions, Gaussian waves, Lorentzian waves, or any combination of these. For example, an stretchable and flexible semiconductor element of the present invention comprises a bent semiconductor ribbon having a curved internal surface with a contour profile characterized by a substantially periodic wave extending along the length of the ribbon. Stretchable and flexible semiconductor elements of this embodiment may be expandable or contractible along an axis extending along the length of the ribbon, and may be bendable or deformable along one or more other axes.

The contour profile of semiconductor structures in this embodiment of the present invention may change when mechanically stressed or when forces are applied to the semiconductor element. Therefore, the ability to change contour profile of exemplary semiconductor structures may provide for their ability to expand, contract, flex, deform and/or bend without experiencing significant mechanical damage, fracture or a substantial reduction in electrical performance. The curved internal surface of the semiconductor structure may be continuously bonded to the supporting surface (i.e. bound at substantially all points along the curved internal surface). Alternatively, the curved internal surface of the semiconductor structure may be discontinuously bonded to the supporting surface, wherein the curved internal surface is bonded to the supporting surface at selected points along the curved internal surface.

The present invention also includes stretchable electronic devices and/or device components comprising a combination of a printable semiconductor structure and additional integrated device components, such as electrical contacts, electrodes, conducting layers, dielectric layers, and additional semiconductor layers (e.g. doped layers, P-N junctions etc.), all of which having curved internal surfaces that are supported by supporting surfaces of a flexible substrate. The curved internal surface configurations of the additional integrated device components enable them to exhibit good electronic performance even when undergoing significant

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strain, such as maintaining electrical conductivity or insulation with a semiconductor element while in a stretched or bent configuration. Additional integrated device components in this aspect of the present invention may have a bent configuration, such as a coiled or wrinkled configuration, as described above, and may be fabricated using techniques similar to those used to fabricate stretchable semiconductor elements. In one embodiment, for example, stretchable device components, including a stretchable semiconductor element, are fabricated independently and then interconnected. Alternatively, the semiconductor containing device may be fabricated in a planar configuration, and the resulting planar device is subsequently processed to provide curved internal surfaces to all or some of the device components.

Printable semiconductor elements of the present invention may comprise heterogeneous semiconductor elements exhibiting enhanced properties, such as enhanced mechanical, electrical, magnetic and/or optical properties, useful in a variety of device environments and configurations. Heterogeneous semiconductor elements are multicomponent structures comprising a semiconductor in combination with one or more additives. In this context of this description, additives comprise elements, molecules and complexes, aggregates and particles thereof, that are different from the semiconductor in which they are combined, such as additives having a different chemical compositions and/or physical states (e.g. crystalline, semicrystalline or amorphous states). Useful additives in this aspect of the invention include other semiconductor materials, N-type and P-type dopants such as arsenic, boron, and antimony, structural enhancers, dielectric materials and conducting materials. Heterogeneous semiconductor elements of the present invention include structures having spatial homogeneous compositions, such as uniformly doped semiconductor structures, and include structures having spatial inhomogeneous compositions, such as semiconductor structures having dopants with concentrations that vary spatially in one, two or three dimensions (i.e. a spatially inhomogeneous dopant distribution in the semiconductor element).

In another aspect, heterogeneous semiconductor elements comprise semiconductor structures having additional integrated functional device components, such as dielectric layers, electrodes, electrical contacts, doped contact layers, P-N junctions, additional semiconductor layers, and integrated multilayer stacks for charge confinement. Additional integrated functional device components of this aspect of the present invention include both semiconductor-containing structures and non-semiconductor-containing structures. In one embodiment, heterogeneous semiconductor elements comprise functional devices, such as transistors, diodes or solar cells, or multielement functional device components that are capable of being effectively patterned, assembled and/or interconnected on a substrate material.

Use of printable heterogeneous semiconductor elements provides certain advantages in the fabrication methods of the present invention. First, the "top down" processing approach of the present methods allows virtually any type of semiconductor processing, such as spatially controlled doping, to be carried out in fabrication steps separate from subsequent fabrication steps of (i) defining the spatial dimensions of the semiconductor elements and (ii) assembling the semiconductor elements on substrates and into functional devices. Separation of semiconductor processing from devices and device component assembly and interconnection in the present methods allows processing of semiconductor materials to be carried out under a range of conditions useful for generating very high quality semiconductor containing

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materials, including single crystal semiconductors having doped regions with well defined concentrations and spatial dopant distributions, and integrated, semiconductor multilayer stacks exhibiting high purities. For example, separation of semiconductor processing and device component assembly, allows for semiconductor processing at high temperatures and under conditions of highly controlled levels of impurities. Second, use of heterogeneous semiconductor elements comprising a plurality of integrated device components and/or functional devices allows for efficient high throughput printing of functional devices and arrays thereof in a commercially beneficial manner. For example, device fabrication methods of the present invention using heterogeneous semiconductor elements comprising a plurality of interconnected device components reduces the net number of fabrication steps and/or lowers the costs involved in manufacturing some devices.

In another aspect, the present invention provides methods of assembling, positioning, organizing, transferring, patterning and/or integrating printable semiconductor elements onto or into substrates via a range of printing methods, including dry transfer contact printing or solution printing techniques. Printing methods of the present invention are capable of integrating one or more semiconductor elements onto or into a substrate in a manner which does not substantially affect their electrical properties and/or mechanical characteristics. In addition, printing methods of the present invention are capable of assembling semiconductor elements onto or into selected regions of a substrate and in selected spatial orientations. Further, printing methods of the present invention are capable of integrating semiconductor elements and other device components into and/or onto a substrate in a manner providing high performing electronic and optoelectronic devices by establishing good conductivity between selected device components, good insulation between selected device components and/or good spatial alignment and relative positioning between device components.

In one embodiment of the present invention, semiconductor elements are assembled onto a substrate surface by dry transfer contact printing methods, such as soft lithographic microtransfer or nanotransfer methods. In one method, one or more printable semiconductor elements are contacted with a conformable transfer device having one or more contact surface(s). Contact established between the contact surface(s) and the printable semiconductor element(s) binds or associates the semiconductor element(s) to the contact surface(s). Optionally, conformal contact is established between the contact surface(s) and the printable semiconductor element(s) to facilitate binding or associate of these elements. At least a portion of the semiconductor element(s) disposed on the contact surface(s) is subsequently contacted with a receiving surface of the substrate. Optionally, the conformable transfer device also establishes conformal contact between the contact surface(s) having the semiconductor element(s) disposed thereon and at least a portion of the receiving surface. Separation of the contact surface of the conformable transfer device and the semiconductor element(s) transfers the semiconductor element(s) onto the receiving surface, thereby assembling the semiconductor element on the receiving surface of the substrate. In an embodiment preferred for device fabrication applications, printable semiconductor elements are positioned and/or integrated onto the substrate in selected regions and in selected spatial orientations. Optionally, the transfer process is repeated multiple times to provide patterning on large areas of a receiving surface of a substrate. In this embodiment, the

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transfer stamp having printable semiconductor elements is contacted with a different region of the receiving substrate for each successive patterning step. In this manner very large areas of a receiving surface may be patterned with semiconductor elements derived from a single mother wafer.

An advantage of the use of dry transfer contact printing methods in the present invention is that patterns of printable semiconductor elements may be transferred and assembled onto substrate surfaces in a manner preserving selected spatial orientations of semiconductor elements which define the pattern. This aspect of the present invention is particularly beneficial for applications wherein a plurality of printable semiconductor elements are fabricated in well defined positions and relative spatial orientations which directly correspond to a selected device configuration or array of device configurations. Transfer printing methods of the present invention are capable of transferring, positioning and assembling printable semiconductor elements and/or printable semiconductor containing functional devices including, but not limited to, transistors, optical waveguides, microelectromechanical systems, nanoelectromechanical systems, laser diodes, or fully formed circuits.

In another embodiment, the present invention provides selective transfer and assembly methods wherein some, but not all, of the printable semiconductors provided are transferred and assembled onto or into a substrate. In this embodiment, the conformable transfer device is capable of binding selectively to specific printable semiconductor elements provided. For example, the conformable transfer device may have a selected three dimensional relief pattern on its external surface having recessed regions and relief features. In this embodiment, recessed regions and relief features may be positioned such that only selected printable semiconductor elements are contacted by one or more contact surfaces provided by the relief pattern, and subsequently transferred and assembled onto the substrate surface. Alternatively, the conformable transfer device may have a contact surface or plurality of contact surfaces having a selected pattern of binding regions, such as chemically modified regions having hydroxyl groups extending from the contact surface and/or regions having one or more adhesive surface coatings. In this embodiment, only those semiconductor elements that are contacted with the binding regions on the contact surface(s) are bound to the transfer device, and subsequently transferred and assembled onto the substrate surface. An advantage of selective transfer and assembly methods of the present invention is that a first pattern of printable semiconductor elements characterized by a first set of positions and spatial orientations may be used to generate a second pattern of printable semiconductor elements different from the first pattern and characterized by a second set of positions and spatial orientations, corresponding to a selected device configuration or array of device configurations.

An exemplary conformable transfer device of the present invention comprises a dry transfer stamp, such as an elastomeric transfer stamp or composite, multi-layer patterning device. Conformable transfer devices useful for the present invention include patterning devices comprising a plurality of polymer layers as described in U.S. patent application Ser. No. 11/115,954, entitled "Composite Patterning Devices for Soft Lithography", filed with the U.S. Patent and Trademark Office on Apr. 27, 2005, which is hereby incorporated by reference in its entirety. An exemplary patterning device useable in the methods of the present invention comprises a polymer layer having a low Young's Modulus, such as a poly(dimethylsiloxane) (PDMS) layer, preferably for some

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applications having a thickness selected from the range of about 1 micron to about 100 microns. Use of a low modulus polymer layer is beneficial because it provides transfer devices capable of establishing good conformal contact with one or more printable semiconductor elements, particularly printable semiconductor elements having curved, rough, flat, smooth and/or contoured exposed surfaces, and capable of establishing good conformal contact with substrate surfaces having a wide range of surface morphologies, such as 10 curved, rough, flat, smooth and/or contoured substrate surfaces.

Optionally, transfer devices of the present invention may further comprise a second layer having an external surface opposite an internal surface, and having a high Young's modulus, such as high modulus polymer layer, ceramic layer, glass layer or metal layer. In this embodiment, the internal surface of the first polymer layer and the internal surface of the second high modulus layer are arranged such that a force applied to the external surface of the second high 15 modulus layer is transmitted to the first polymer layer. Use of a high modulus second polymer layer (or backing layer) in transfer devices of the present invention is beneficial because it provides transfer devices having a net flexural rigidity large enough to provide good binding, transfer and 20 assembly characteristics. For example, use of a transfer device having a net flexural rigidity selected from the range of about  $1 \times 10^{-7}$  Nm to about  $1 \times 10^{-5}$  Nm minimizes distortions of the positions of semiconductor elements and/or other structures bound to the contact surface(s) upon establishing conformal contact with a substrate surface. Use of a 25 high modulus, rigid backing layer also is beneficial for preventing degradation of the printable semiconductor elements during transfer, for example by prevent cracking of the printable semiconductor layers. This attribute provides 30 methods and devices of assembling printable semiconductor elements exhibiting high placement accuracy and good pattern fidelity. Transfer devices of the present invention may comprise additional layers, including polymer layers, for providing easy handling and maintenance, good thermal 35 properties and for providing uniform distribution of a force applied to the transfer device to the entire contact surface(s), as taught in U.S. patent application Ser. No. 11/115,954, entitled "Composite Patterning Devices for Soft Lithography", filed with the U.S. Patent and Trademark Office on Apr. 45 27, 2005 which is incorporated by reference in its entirety herein.

In another approach, the principles of 'soft adhesion' are used to guide the transfer. Here, the viscoelastic nature of the surface material on the transfer element leads to a peel force (i.e. the force that can lift objects from a surface) that depends on peel rate. At high peel rates, this force is large enough to remove objects from a substrate and transfer them onto a transfer element, even when the static surface energy of the transfer element is lower than that of the substrate. At 50 low peel rates, this peel force is low. In some embodiments, by contacting a transfer element that supports an array of objects against a final substrate, and then peeling the element away slowly leads to the transfer of these objects from the transfer element to the substrate. This approach of the present invention using controlled peeling rates can be used in combination with the other transfer approaches described herein.

Transfer devices of the present invention may have a single continuous contact surface or a plurality of discontinuous contact surfaces. The contact surface(s) of transfer devices of the present invention may be defined by a selected 55 three-dimensional dimensional relief pattern having

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recessed regions and relief features having selected physical dimensions. Contact surfaces useful in the present invention may be capable of binding printable semiconductor elements by van der Waals forces, covalent bonds, adhesive layers, chemically modified regions such as regions having hydroxyl groups disposed on their surfaces, dipole-dipole forces or combinations of these. Transfer devices of the present invention may have contact surfaces having any area.

A number of methods may be used to facilitate transfer of printable semiconductor elements from a contact surface into or onto a substrate surface. In an exemplary embodiment, the difference in surface energy of the substrate surface and the contact surface promotes transfer to the substrate surface. For example, transfer may be effectively achieved from a contact surface comprised of a PDMS layer having a lower surface energy to a substrate surface having a higher surface energy, such as a polyimide, polycarbonate or Mylar surface. In addition, a plastic substrate surface may be softened or partially melted by heating prior to and/or during contact with printable semiconductor elements to be transferred, thereby generating semiconductor elements embedded in the substrate. Allowing the substrate to cool and harden prior to separation of the contact surface from the semiconductor elements promotes efficient transfer. Alternatively, the substrate surface may have one or more chemical modified regions exhibiting an enhanced affinity of the substrate for the semiconductor elements. For example, modified regions may be covered by one or more adhesive layers or may be modified such that they undergo efficient covalent bonding, attractive van der Waals forces, dipole-dipole forces or combinations of these with semiconductor elements to promote efficient transfer and assembly. Alternatively, a partial polymerized polymer precursor may be contacted with the semiconductor elements or other device components and, subsequently polymerized, resulting in formation of a substrate having semiconductor elements embedded therein.

In an exemplary embodiment, printable semiconductor elements are fabricated having top surfaces coated with a thin release layer, such as a layer of photoresist used as a photomask patterned onto a substrate during the definition and fabrication of the printable semiconductor elements. The contact surface of a conformable transfer device is brought into conformal contact with the coated surfaces of the printable semiconductor element. The release layer facilitates bonding of the printable semiconductor elements to the contact surface of the transfer device. Surfaces of the printable semiconductor elements not coated with the release layer are then contacted with a receiving surface of a substrate. Next, the release layer is removed, for example by exposure to an appropriate solvent such as acetone, thereby separating the printable semiconductor elements from conformable transfer device. Optionally, the receiving surface may be coated with one or more adhesive layers to facilitate transfer of the printable semiconductor elements.

In another embodiment of the present invention, printable semiconductor elements are assembled onto a substrate surface by solution printing. In the context of this description, the term "solution printing" is intended to refer to processes whereby one or more structures, such as printable semiconductor elements, are dispersed into a carrier medium, such as a carrier fluid or solvent, and delivered in a concerted manner to selected regions of a substrate surface. In an exemplary solution printing method, delivery of structures to selected regions of a substrate surface is achieved by methods that are independent of the morphol-

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ogy and/or physical characteristics of the substrate surface undergoing patterning. In another embodiment, printable semiconductor elements remain suspended in a solvent until the solvent evaporates, or until an applied force, such as an electrostatic force, magnetic force or force provided by an acoustic wave, pulls the printable semiconductor elements out of solution and onto selected regions of the substrate. This functionality may be provided by selection of appropriate physical dimensions and masses of the printable semiconductor elements necessary to avoid premature sedimentation. In this way, the solution printing methods of the present invention differ materially from some fluidic self assembly methods in which elements suspended in a carrier medium fall out of solution due to the force of gravity and statistically fall into recessed regions of a substrate.

A method of assembling a printable semiconductor element on a receiving surface of a substrate of the present invention comprises the step dispersing a printable semiconductor element in a carrier medium, thereby generating a suspension comprising the semiconductor element in the carrier medium. The semiconductor element is delivered to the substrate by solution printing the suspension onto the receiving surface, thereby assembling the semiconductor element onto said receiving surface. In this embodiment, solution printing may be provided by a number of techniques known in the art including, but not limited to, ink jet printing, thermal transfer printing, and screen printing. Solution printing methods of the present invention may also employ self assembly alignment techniques. In one embodiment, for example, alignment, positioning and registration of printable semiconductor elements having patterned hydrophobic and hydrophilic groups are aligned on a receiving surface having complimentary patterned hydrophobic regions (such as methyl terminated surface groups) and hydrophilic regions (such as carboxylic acid terminated surface groups). Solution printing methods of the present invention may also employ capillary action of drops containing dispersed printable semiconductor elements to achieve alignment, positioning and registration.

Optionally, a number of methods may be used in the present invention to control the orientation, alignment and selective deposition of semiconductor elements and/or other device components on the substrate surface. These methods enable fabrication of complex integrated electronic and optoelectronic devices comprising a plurality of interconnected device components having precisely specified relative positions and spatial orientations. For example, electrostatic forces, acoustic waves and/or magnetostatic forces may be employed to facilitate positioning semiconductor elements and other device components in specific locations and in selected spatial orientations on a substrate surface. Alternatively, the properties and/or composition of the substrate surface itself may be modified in selected regions to achieve accurate placement of semiconductor elements and other device components. For example, selected regions of the substrate surface may be chemically modified such that they exhibit a selective affinity for semiconductor elements. In addition, the electrical properties of the substrate surface may be modified, for example by formation of potential holes in specific surface regions, to facilitate selective integration, orientation and alignment of printable semiconductor elements and other device components.

Printing methods of the present invention have a number of advantages important for the fabrication of high performance electronic and/or optoelectronic devices. First, printing methods of the present invention are capable of transferring and assembling inorganic single crystalline

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semiconductor structures without exposing these structures to mechanical strain large enough to induce significant damage or degradation, such as damage from cracking. Second, printing methods of the present invention are capable of positioning one or more semiconductor elements on selected regions of a substrate surface in selected orientations with good placement accuracy (i.e. good spatial registration with respect to a selected region of a receiving surface), preferably with spatial deviations from absolutely correct orientations and locations on a substrate less than or equal to 5 microns. Third, printing methods of the present invention are capable of generating patterns comprising a plurality of semiconductor elements, other device elements, integrated function devices or any combination of these having good fidelity with respect to a selected spatial configuration, such as a spatial configuration corresponding to a functional device or array of devices. Fourth, printing methods of the present invention may be carried out at relatively low temperatures (i.e. temperatures less than about 400 Celsius), and therefore are compatible with a wide range of substrates, particularly plastic substrates. Finally, printing methods of the present invention provide a low cost means of fabricating high performance electronic and/or optoelectronic devices, and do not require clean room conditions.

The present compositions and related methods of assembling, positioning, organizing, transferring, patterning and/or integrating printable semiconductor elements onto or into substrates may be used to fabricate virtually any structure comprising one or more semiconductor elements. These methods are particularly useful for fabricating complex integrated electronic or optoelectronic devices or device arrays, such as arrays of diodes, light emitting diodes, solar cells, transistors (FET and bipolar), and thin film transistors. The present compositions and related methods are also useful for fabrication of systems level integrated electrical circuits, such as complementary logic circuits, wherein printable semiconductor elements are printed onto a substrate in well defined spatial orientations and interconnected to form a desired circuit design. In one embodiment of this aspect of the invention, printable N-type and P-type heterogeneous semiconductor elements with selected dopant concentrations and dopant spatial distributions are assembled and interconnected to fabricate complex integrated circuits. In another embodiment, a plurality of printable semiconductor elements comprising different semiconductor materials are printed onto the same substrate and interconnected to fabricate complex integrated circuits.

The assembly methods of the present invention, however, are not limited to semiconductors. Rather these methods are broadly compatible with a wide range of materials that are not semiconductors. Materials that may be transferred and/or assembled by the methods of the present invention include, but are not limited to, insulating materials such as SiO<sub>2</sub>, connecting materials such as conductors, optical elements such as active optical materials, passive optical materials and fiber optic elements, materials for sensing applications and magnetic materials. Accordingly, the present methods, devices and device components may be used to fabricate a wide range of microsized and/or nanosized structures and assemblies of structures, such as microfluidic devices and structures, NEMS devices and arrays of NEMS devices and MEMS devices and arrays of MEMS devices. Particularly, the transfer and assembly methods of the present invention may be used to generate complex three-dimensional structures, such as integrated circuits, by sequential overlay of a plurality of printing levels.

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The present compositions, and related fabrication, assembly and interconnection methods are useful for fabricating devices, particularly semiconductor based devices, on large areas of a wide range of substrates. A benefit of the present methods is that they are compatible with device assembly at temperatures that are compatible with most flexible substrates, including polymer materials such as thermoplastic materials, thermoset materials, reinforced polymer materials and composite polymer materials. However, the present methods are equally applicable to device fabrication on rigid and/or brittle substrates including ceramic materials, glasses, dielectric materials, conductors, metals and semiconductor materials. The applicability of these methods to device fabrication on brittle materials arises from the very low force imparted to substrates using the printing methods of the present invention. The present compositions and fabrication methods are also compatible with device fabrication on more unusual substrate materials, such as paper, wood and rubber, and contoured substrates, including curved substrates, curved rigid substrates, concave substrates, and convex substrates. For example, the present methods are capable of assembling and integrating printable semiconductor elements and other device components (e.g. electrodes, dielectric layers, P-N junctions etc.) on substrates, including rigid and flexible substrates, having a radius of curvature ranging from about 10 microns to about 10 meters.

In another aspect, the present fabrication methods are capable of heterogeneous integration of printable semiconductor elements into functional substrates. For example, the printing methods of the present invention are capable of depositing and integrating printable semiconductor elements into substrates having well defined semiconductor regions, conducting regions and/or insulating regions. An advantage of the present fabrication methods is that printable semiconductor elements can be printed onto functional substrates, such as integrated circuits or components of integrated circuits, in selected orientations and positions with high placement accuracy, particularly in the context of dry transfer contact printing methods of the present invention.

Printable semiconductor elements of the present invention may be fabricated from a wide range of materials. Useful precursor materials for fabricating printable semiconductor elements include semiconductor wafer sources, including bulk semiconductor wafers such as single crystalline silicon wafers, polycrystalline silicon wafers, germanium wafers; ultra thin semiconductor wafers such as ultra thin silicon wafers; doped semiconductor wafers such as P-type or N-type doped wafers and wafers with selected spatial distributions of dopants (semiconductor on insulator wafers such as silicon on insulator (e.g. Si—SiO<sub>2</sub>, SiGe); and semiconductor on substrate wafers such as silicon on substrate wafers and silicon on insulator. Further, printable semiconductor elements of the present invention may be fabricated from scrap or unused high quality or reprocessed semiconductor materials that are left over from semiconductor device processing using conventional methods. In addition, printable semiconductor elements of the present invention may be fabricated from a variety of nonwafer sources, such as a thin films of amorphous, polycrystalline and single crystal semiconductor materials (e.g. polycrystalline silicon, amorphous silicon, polycrystalline GaAs and amorphous GaAs) that is deposited on a sacrificial layer or substrate (e.g. SiN or SiO<sub>2</sub>) and subsequently annealed.

The present invention also includes methods of making printable semiconductor elements and flexible semiconductor elements. These methods enable fabrication of printable

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semiconductor elements and flexible semiconductor elements from a wide range of precursor materials, such as silicon on insulator wafers, single crystalline silicon wafers, thin films of polycrystalline crystalline silicon, ultra thin silicon wafers and germanium wafers. In addition, these methods are capable of generating printable semiconductor elements having a wide range of shapes and physical dimensions. Further, the present methods enable low cost fabrication of large arrays/patterns of printable semiconductor elements in well defined, relative spatial orientations.

In another aspect, the present invention provides a method for assembling a printable semiconductor element on a receiving surface of a substrate comprising the steps of: (1) providing the printable semiconductor element comprising a unitary inorganic semiconductor structure; (2) contacting the printable semiconductor element with a conformable transfer device having a contact surface, wherein contact between the contact surface and the printable semiconductor element binds or associates the printable semiconductor element to the contact surface, thereby forming the contact surface having the printable semiconductor element disposed thereon; (3) contacting the printable semiconductor element disposed on the contact surface with the receiving surface of the substrate; and (4) separating the contact surface of the conformable transfer device and the printable semiconductor element, wherein the printable semiconductor element is transferred onto the receiving surface, thereby assembling the printable semiconductor element on the receiving surface of the substrate. In one embodiment, this method of the present invention further comprises the steps of: (1) providing additional printable semiconductor elements each of which comprising a unitary inorganic semiconductor structure; (2) contacting the printable semiconductor elements with a conformable transfer device having a contact surface, wherein contact between the contact surface and the printable semiconductor element binds or associates the printable semiconductor elements to the contact surface and generates the contact surface having the printable semiconductor elements disposed thereon in relative orientations comprising a selected pattern of the printable semiconductor elements; (3) contacting the printable semiconductor elements disposed on the contact surface with the receiving surface of the substrate; and (4) separating the contact surface of the conformable transfer device and the printable semiconductor elements, wherein the printable semiconductor elements are transferred onto the receiving surface in the relative orientations comprising the selected pattern.

In another aspect, the present invention provides a method for assembling a printable semiconductor element on a receiving surface of a substrate comprising the steps of: (1) providing the printable semiconductor element comprising a unitary inorganic semiconductor structure, wherein the printable semiconductor element has at least one cross sectional dimension greater than or equal to about 500 nanometers; (2) dispersing the semiconductor element in a solvent, thereby generating a suspension comprising the semiconductor element in the solvent; and (3) delivering the semiconductor element to the substrate by solution printing the suspension onto the receiving surface thereby assembling the semiconductor element onto the receiving surface. In one embodiment, this method of the present invention further comprises the steps: (1) providing additional printable semiconductor elements, wherein each of the additional printable semiconductor elements has at least one cross sectional dimension greater than or equal to about 500 nanometers; (2) dispersing the semiconductor elements in

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the solvent, thereby generating a suspension comprising the semiconductor elements in the solvent; and (3) delivering the semiconductor elements to the substrate by solution printing the suspension onto the receiving surface, thereby assembling the semiconductor elements onto the receiving surface.

In another aspect, the present invention provides a method of fabricating a printable semiconductor element comprising the steps of: (1) providing a wafer having an external surface, the wafer comprising a semiconductor; (2) masking a selected region of the external surface by applying a mask; (3) etching (optionally anisotropically etching) the external surface of the wafer, thereby generating a relief structure on the wafer and at least one exposed surface of the wafer, wherein the relief structure has a masked side and one or more unmasked sides; (4) applying a mask to at least a portion of the unmasked sides of the relief structure; (5) at least partially etching the exposed surfaces of the wafer, thereby releasing a portion of the relief structure from the wafer and fabricating the printable semiconductor element. In this embodiment, mask may be applied to the unmasked sides of the relief structure by angled deposition methods, such as sputtering or vapor deposition, or by flowing a portion of the mask on the external surface onto the unmasked sides

In another aspect, the present invention provides a method of fabricating a printable semiconductor element comprising the steps of: (1) providing a wafer having an external surface, the wafer comprising a semiconductor; (2) masking selected regions of the external surface by applying a first mask; (3) etching (optionally anisotropically etching) the external surface of the wafer, thereby generating a plurality of relief structures; (4) annealing the wafer, thereby generating an annealed external surface; (5) masking selected regions of the annealed external surface by applying a second mask; and (6) etching (optionally anisotropically etching) the annealed external surface, thereby generating the semiconductor element.

In another aspect, the present invention provides a method of fabricating a printable semiconductor element comprising the steps of: (1) providing an ultra thin wafer having an external surface, the wafer comprising a semiconductor and having a selected thickness along an axis orthogonal to the external surface; (2) masking selected regions of the external surface by applying a mask; (3) etching (optionally anisotropically etching) the external surface of the wafer, wherein the wafer is etched throughout the thickness along the axis orthogonal to the external surface, thereby generating the printable semiconductor element.

In another embodiment, the present invention provides a method for making a flexible semiconductor element comprising the steps of: (1) providing a printable semiconductor structure having an internal surface; (2) providing a prestrained elastic substrate in an expanded state, wherein the elastic substrate has an external surface; and (3) bonding the internal surface of the printable semiconductor structure to the external surface of the prestrained elastic substrate in an expanded state; and allowing the elastic substrate to relax at least partially to a relaxed state, wherein relaxation of the elastic substrate bends the internal surface of the printable semiconductor structure thereby generating a semiconductor element having a curved internal surface. In an exemplary embodiment, the prestrained elastic substrate is expanded along a first axis, a second axis orthogonal to the first axis or both. The prestrained elastic substrate in an expanded state may be formed by bending the elastic substrate or rolling the elastic substrate. Optionally, the method of this

aspect of the present invention may further comprise the step of transferring the semiconductor having a curved internal surface to a receiving substrate that is flexible.

In another embodiment, the present invention provides a method for fabricating a printable semiconductor element connected to a mother wafer via one or more alignment maintaining elements comprising the steps of: (1) providing the mother wafer having an external surface, the wafer comprising an inorganic semiconductor material; (2) masking a selected region of the external surface by applying a mask; (3) etching the external surface of the wafer, thereby generating a relief structure and at least one exposed surface of the wafer, wherein the relief structure has a masked side and one or more unmasked sides; (4) etching the exposed surfaces of the wafer; and (5) stopping etching of the exposed structure so that complete release of the relief structure is prevented, thereby fabricating the printable semiconductor element connected to a mother wafer via one or more alignment maintaining elements. In one embodiment of this method the printable semiconductor element has a peanut shape with a first end and a second end, wherein the alignment maintaining elements connect the first and second ends of the printable semiconductor element to the mother wafer. In another embodiment of this method the printable semiconductor element has a ribbon shape with a first end and a second end, wherein the alignment maintaining elements connect the first and second ends of the printable semiconductor element to the mother wafer.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 schematically illustrates an exemplary method of the present invention for producing and assembling printable semiconductor elements comprising ribbons of single crystalline silicon.

FIG. 2 provides a schematic diagram illustrating a selective dry transfer contact printing method for assembling printable semiconductor element on a receiving surface of a substrate.

FIGS. 3A-C, are schematic diagrams showing devices, device configurations and device components useful in selective dry transfer contact printing methods of the present invention. FIG. 3D provides a photograph of an array of photodiodes printed onto a spherical surface of a polycarbonate lens (FL 100 mm). FIG. 3E provides a scanning electron micrograph of an array of photodiodes printed onto the curved surface of a spherical glass lens (FL 1000 mm). Contrast in the image provided in FIG. 3E is slightly enhanced to show p-doped regions. FIG. 3F provides a plot of electric current ( $\mu$ A) verse bias potential (volts) illustrating the light response of the photodiodes pictured in FIG. 3E.

FIGS. 4A1 and 4A2 show a preferred shape of a printable semiconductor element for assembly methods of the present invention using dry transfer contact printing. FIG. 4A1 provides a perspective view and FIG. 4A2 provides a top plan view. FIGS. 4B1 and 4B2 show a preferred shape of a printable semiconductor element for assembly methods of the present invention using dry transfer contact printing. FIG. 4B1 provides a perspective view and FIG. 4B2 provides a top plan view.

FIG. 5A-C presents optical and scanning electron micrographs of a range of printable semiconductor elements comprising microstrips of single crystalline silicon having selected physical dimensions

FIG. 6 presents an image of transferred printable semiconductor elements comprising single crystalline silicon microstrips on a PDMS coated polyimide sheet.

FIG. 7 presents an optical micrograph image of a thin film transistor having a printable semiconductor element.

FIG. 8 provides a plot showing current-voltage (IV) characteristics of a device made on a pre-oxidized Si wafer.

FIG. 9 provides a plot showing transfer characteristics measured at  $V_{DS}=0.1$  V of a device made on a Mylar sheet coated with ITO gate and polymer dielectric.

FIGS. 10A-H provide a schematic diagrams illustrating a method of the present invention for making an array of thin film transistors having composite printable semiconductor elements.

FIGS. 11A-D provide diagrams illustrating a method of the present invention for making a printable device comprising integrated gate electrode, gate dielectric, semiconductor, source electrode and drain electrode.

FIG. 12A, FIG. 12B and FIG. 12C provide an atomic force micrographs showing a stretchable printable semiconductor element of the present invention.

FIG. 13A, FIG. 13B, FIG. 13C, FIG. 13D and FIG. 13E show atomic force micrographs providing an expanded view of a semiconductor structure having curved internal surface.

FIG. 14A, FIG. 14B and FIG. 14C show atomic force micrographs of an array of stretchable printable semiconductor elements of the present invention.

FIG. 15 shows optical micrographs of stretchable printable semiconductor elements of the present invention.

FIG. 16A and FIG. 16B show atomic force micrographs of a stretchable printable semiconductor element of the present invention having a semiconductor structure bonded to a flexible substrate having a three dimensional relief pattern on its supporting surface.

FIG. 17 shows a flow diagram illustrating an exemplary method of making a stretchable semiconductor element of the present invention.

FIG. 18A shows an exemplary method of making printable semiconductor elements from a Si—Ge epi substrate.

FIG. 18B shows an exemplary method for fabricating printable semiconductor elements from a bulk silicon substrate, preferably a single crystalline silicon substrate.

FIG. 18C shows another exemplary method of fabricating printable semiconductor elements from a bulk silicon substrate, preferably a single crystalline silicon substrate.

FIG. 18D shows yet another exemplary method of fabricating printable semiconductor elements from a bulk silicon substrate, preferably a single crystalline silicon substrate.

FIG. 18E shows an exemplary method of fabricating printable semiconductor elements from an ultra thin silicon substrate.

FIG. 18F shows an exemplary method for making printable semiconductor elements from a thin film of polycrystalline silicon on a supporting substrate.

FIG. 18G shows an exemplary method for making printable semiconductor elements from a thin film of polycrystalline silicon on a  $\text{SiO}_2$  substrate.

FIGS. 18H(1) and 18H(2) illustrate a method for making single crystalline semiconductor thin films using printable semiconductor elements of the present invention.

FIG. 18I shows an exemplary method of fabricating printable semiconductor elements comprising micro-wires from GaAs substrate.

FIG. 18J shows an alternative method for fabricating printable semiconductor elements comprising single crystalline silicon ribbons.

FIG. 18K shows an alternative method for fabricating printable semiconductor elements comprising single crystalline silicon ribbons.

FIG. 19A provides a schematic diagram illustrating the steps of an exemplary method of generating nanowire arrays of GaAs and FIG. 19B provides a schematic diagram illustrating transferring nanowire arrays of GaAs to a substrate, such as plastic substrate comprising poly(ethylene terephthalate) (PET) sheet coated with a thin layer of cured polyurethane (PU).

FIG. 20A provides a scanning electron micrograph of free-standing GaAs wires obtained from GaAs wafer patterned with isolated SiO<sub>2</sub> lines. FIGS. 20B-E show scanning electron micrograph images of individual wires obtained by etching the GaAs wafer patterned with 2 μm wide SiO<sub>2</sub> lines. FIG. 20F provides a plot showing the dependence of the average width,  $\bar{w}_{wires}$ , of the top surfaces of wires fabricated by the present methods on etching time.

FIGS. 21A-G shows images of a variety of GaAs wire arrays printed on PDMS and PU/PET substrates.

FIGS. 22A-C shows scanning electron micrograph images of an InP wire array on PMDS and PU/PET substrates.

FIG. 23A provides a schematic diagram and image of an exemplary two terminal diode device comprising GaAs wire arrays. FIG. 23B shows the current-voltage (I-V) curves recorded for the two terminal diode device at different bend radii indicating that the two terminal diode device comprising GaAs wire arrays exhibited expected diode characteristics. FIG. 23C shows the current-voltage (I-V) curves measured for the two terminal diode device after relaxation after bending at different bend radii.

FIG. 24 provides a schematic diagram illustrating an exemplary method of the present invention for solution printing printable semiconductor elements having handle elements comprising magnetic tags.

FIG. 25 provides several optical images demonstrating the use of solution printing methods of the present invention to generate well order arrays of microstructures having handle elements comprising thin nickel layers.

FIG. 26A illustrates the steps used to fabricate exemplary bendable thin film transistors devices of the present invention. FIG. 26B presents a schematic illustration of the bottom gate device configuration of the thin film transistor together with high and low magnification optical images of part of the device array.

FIG. 27A presents current voltage characteristics of a bendable thin film transistor of the present invention that shows an effective device mobility of 140 cm<sup>2</sup>/Vs in the saturation regime and 260 cm<sup>2</sup>/Vs in the linear regime, as evaluated by application of standard field effect transistor models that ignore the effects of contacts. FIG. 27B presents transfer characteristics of several devices, plotted on linear (left axis) and logarithmic (right axis) scales. FIG. 27C shows the distribution of the linear effective mobilities of several bendable thin film transistors fabricate by the present methods.

FIG. 28A presents a high-resolution scanning electron micrograph of solution cast ribbons (left inset) illustrating the remarkable flexibility of the printable single crystal silicon semiconductor elements. The right inset in FIG. 28A shows a picture of the experimental setup used to bend the bendable thin film transistors evaluated in this study. FIG. 28B shows the small (<1%) linear variation of the epoxy dielectric capacitance when subject to tensile and compressive strains (see top inset). The lower inset in FIG. 28B

presents the variation of the saturation current of a device measured for a gate and drain bias voltages of both 4 V.

FIG. 29A presents a schematic representation of a fabrication process for generating transistors comprising printable heterogeneous semiconductor elements on a PET substrate. FIG. 29B shows optical images of several devices having heterogeneous printable semiconductor elements fabricated using the present techniques.

FIG. 30A shows a plot of the normalized resistance,  $R_{total}W_{as}$  as a function of L, for an arrangement of printable heterogeneous semiconductor elements and contact pads used to characterize the contact resistances (see inset). FIG. 30B shows Time-of-Flight Secondary Ion Mass Spectroscopy (TOF-SIMS) measurements that show the use of patterned SOG as a diffusion barrier (See, Schematic in FIG. 29A) localizes the dopants to desired regions in the silicon. In the image shown in FIG. 30B, the bright red color indicates high phosphorous concentration.

FIGS. 31A-D shows measurements corresponding to transistors comprising printable contact doped silicon semiconductor elements on an epoxy/ITO/PET substrate. FIG. 31A provides typical current-voltage characteristics of a single crystal silicon transistor with doped contacts on a PET substrate, with L=7 microns and W=200 microns. From the bottom to top,  $V_G$  varies from -2 V to 6 V. FIG. 31B provides transfer curves ( $V_d=0.1$  V) of devices with channel lengths, from top to bottom, of 97 microns, 72 microns, 47 microns, 22 microns, 7 microns, and 2 microns. The channel width in each case is 200 microns. FIG. 31C shows the width-normalized resistance of devices in the ON state ( $R_{on}W$ ) as a function of channel length L at different gate voltages. The solid lines represent linear fits. The scaling is consistent with contacts that have negligible influence on device performance for this range of channel lengths. the inset in FIG. 31C shows the sheet conductance [ $\Delta(R_{on}W)/\Delta L$ ]<sup>-1</sup>, determined from the reciprocal of the slopes of the linear fitting in FIG. 31C, as a function of gate voltage. FIG. 31D shows effective mobility, evaluated in the linear regime, as a function of channel length for the devices with undoped (triangle) and doped (square) contacts.

FIG. 32A shows the change of the effective device mobility, normalized by the value in the unbent state,  $\mu_{eff}$ , as a function of strain (or bending radius). FIG. 32B presents normalized effective mobilities  $\mu_{eff}/\mu_{eff}$  after several hundred bending cycles (to a radius of 9.2 mm) that cause compressive strain at the device to vary between 0 and 0.98%.

FIG. 33 shows an example of a composite semiconductor structure fabricated using a heterogeneous integration method of the present invention comprising gallium nitride microstructures direct-bonded onto a silicon wafer (1 0 0).

FIG. 34A provides a process flow diagram schematically illustrating processing steps in a fabrication pathway for making a solar cell comprising a printable P-N junction. 34B shows a schematic diagram of a solar cell device configuration generated by the fabrication pathway illustrated in FIG. 34A. FIG. 34C shows the photodiode response observed upon illumination of a solar cell device having the configuration shown in FIG. 34B.

FIG. 35A provides a process flow diagram schematically illustrating processing steps in an alternative fabrication pathway for making a solar cell comprising printable P and N doped semiconductor layers. FIG. 35B shows a schematic diagram of a solar cell device generated using the fabrication pathway illustrated in FIG. 35A. FIG. 35C shows a SEM image of a top view of the solar cell schematically depicted in FIG. 35B. FIG. 35D provides a plot of current verse bias

demonstrating the photodiode response of the solar cell shown in FIG. 35C. FIG. 35E shows plots of current versus bias corresponding to several different illumination intensities demonstrating the photodiode response of the solar cell shown in FIG. 35C.

FIG. 36A shows a process flow diagram illustrating an exemplary method of making an array of stretchable thin film transistors. FIG. 36B shows provides optical micrographs of an array of stretchable thin film transistors in relaxed and stretched configurations.

FIG. 37A provides a schematic diagram showing a processing method of the present invention (Method I) for patterning  $\mu$ -Si elements onto a plastic substrate. FIG. 37B provides a schematic diagram illustrating an alternative processing method of the present invention (Method II) for patterning  $\mu$ -Si elements onto a plastic substrate.

FIG. 38A shows the design of the so-called peanut shaped  $\mu$ -Si objects used in methods of the present invention. Inset optical image in FIG. 38A shows the optimized HF etching condition where the buried oxide under the channel is removed while a sacrificial SiO<sub>2</sub> portion remains. FIG. 38B shows an example of loss of this order when the Si objects are overetched in HF solution. FIGS. 38C, 38D, 38E and 38F shows a series of micrographs that depicts the progression of each step of the  $\mu$ -Si transfer as effected using Method I.

FIGS. 39A and 39B provide optical images of the selective transfer of the  $\mu$ -Si onto PU/PET sheet by 3600 PDMS stamp. FIG. 39C is an optical micrograph of a section of a Sylgard 184 coated PET substrate to which the  $\mu$ -Si has been chemically bonded and subsequently transferred. A higher magnification image of the  $\mu$ -Si transferred in this way is shown in FIG. 39D.

FIG. 40A illustrates an exemplary device geometry of a device fabricated using the peanut shaped  $\mu$ -Si based on a transfer using Method I. FIG. 40B provides I-V curves of  $\mu$ -Si TFTs at a range of gate voltage ( $V_g$ =−2.5 V to 20 V). FIG. 40C shows the transfer characteristics, measured at a constant source-drain voltage ( $V_{sd}$ =1 V), indicated the effective mobility was 173 cm<sup>2</sup>/Vs. The inset in FIG. 40C shows an optical micrograph of actual device of the present invention.

FIG. 41 provides a schematic process flow diagram depicting steps involved in the process for fabricating  $\mu$ -GaAs MESFETs on a poly(ethylene terephthalate) (PET) substrate. Anisotropic chemical etching produces wires from a standard (100) GaAs wafer. A printing technique that uses an elastomeric stamp transfers these wires from the wafer to the plastic device substrate in a manner that preserves spatial organization (i.e. ordered arrays). PR denotes photoresist.

FIG. 42A presents a schematic showing a cross section view of the geometry of a GaAs wire based MESFET on a plastic substrate (PU/PET). The source/drain electrodes form ohmic contacts to the n-GaAs layer. FIG. 42B shows a representative image of two GaAs wire based MESFETs on plastic each of which uses an array of ten GaAs wires, fabricated according to the process flow diagram of FIG. 41. FIG. 42C shows the image of a 2 cm×2 cm PET sheet with hundreds of transistors, clearly demonstrating its flexibility.

FIGS. 43A, 43B and 43C present results from a GaAs MESFET with a channel length of 50  $\mu$ m, a gate length of 15  $\mu$ m, similar to the one shown in FIG. 42B. FIG. 43A shows the current-voltage (between drain and source electrodes) curves at gate voltages between 0.5 to −2.0 V with steps of 0.5 V. FIG. 43B shows the transfer characteristics (i.e.,  $I_{DS}$  vs.  $V_{GS}$ ) of a GaAs MESFET of the present invention measured at different  $V_{DS}$ . FIG. 43C shows the

transfer curve at  $V_{DS}$ =4 V, plotted as  $(I_{DS})^{1/2}$  vs.  $V_{GS}$ , clearly showing a linear relationship as expected for a MESFET.

FIGS. 44A and 44B show gate-modulated current-voltage characteristics of a GaAs wire based MESFET on a flexible 5 PET substrate (A) before bending; (B) after bending to a bend radius of 8.4 mm. FIG. 44C shows the gate-modulated current-voltage characteristics of the GaAs wire based MESFET after relaxing the bent substrate to its flat, unbent state. FIG. 44D shows the variation of  $I_{DS}$  at  $V_{DS}$ =4 V and  $V_{GS}$ =0 10 V in 3 cycles in terms of bending (with different surface strains)/unbending, indicating that these MESFETs survive multiple bending cycles that cause the tensile strain at the device to vary between 0% and 1.2%, without significant change of their performance (<20%).

FIG. 45 provides a schematic diagram illustrating an exemplary device configuration of the present invention for a P type bottom gate thin film transistor on a plastic substrate.

FIG. 46 provides a schematic diagram illustrating an 20 exemplary device configuration of the present invention for a complementary logic gate on a plastic substrate.

FIG. 47 provides a schematic diagram illustrating an 25 exemplary device configuration of the present invention for a top gate thin film transistor on a plastic substrate.

#### DETAILED DESCRIPTION OF THE INVENTION

Referring to the drawings, like numerals indicate like 30 elements and the same number appearing in more than one drawing refers to the same element. In addition, hereinafter, the following definitions apply:

“Printable” relates to materials, structures, device components and/or integrated functional devices that are capable 35 of transfer, assembly, patterning, organizing and/or integrating onto or into substrates without exposure of the substrate to high temperatures (i.e. at temperatures less than or equal to about 400 degrees Celsius). In one embodiment of the present invention, printable materials, elements, device components and devices are capable of transfer, assembly, patterning, organizing and/or integrating onto or into substrates via solution printing or dry transfer contact printing.

“Printable semiconductor elements” of the present invention 40 comprise semiconductor structures that are able to be assembled and/or integrated onto substrate surfaces, for example using by dry transfer contact printing and/or solution printing methods. In one embodiment, printable semiconductor elements of the present invention are unitary single crystalline, polycrystalline or microcrystalline inorganic semiconductor structures. In this context of this 45 description, a unitary structure is a monolithic element having features that are mechanically connected. Semiconductor elements of the present invention may be undoped or doped, may have a selected spatial distribution of dopants 50 and may be doped with a plurality of different dopant materials, including P and N type dopants. The present invention includes microstructured printable semiconductor elements having at least one cross sectional dimension greater than or equal to about 1 micron and nanostructured 55 printable semiconductor elements having at least one cross sectional dimension less than or equal to about 1 micron. Printable semiconductor elements useful in many applications 60 comprises elements derived from “top down” processing of high purity bulk materials, such as high purity crystalline semiconductor wafers generated using conventional high temperature processing techniques. In one embodiment, printable semiconductor elements of the pres-

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ent invention comprise composite structures having a semiconductor operational connected to at least one additional device component or structure, such as a conducting layer, dielectric layer, electrode, additional semiconductor structure or any combination of these. In one embodiment, printable semiconductor elements of the present invention comprise stretchable semiconductor elements and/or heterogeneous semiconductor elements.

“Cross sectional dimension” refers to the dimensions of a cross section of device, device component or material. Cross sectional dimensions include width, thickness, radius, and diameter. For example, printable semiconductor elements having a ribbon shape are characterized by a length and two cross sectional dimensions; thickness and width. For example, printable semiconductor elements having a cylindrical shape are characterized by a length and the cross sectional dimension diameter (alternatively radius).

“Fill factor” refers to the percentage of the area between two elements, such as first and second electrodes, that is occupied by a material, element and/or device component. In one embodiment of the present invention, first and second electrodes are provided in electrical contact with one or more printable semiconductor elements that provide a fill factor between first and second electrodes greater than or equal to 20%, preferably greater than or equal to 50% for some applications and more preferably greater than or equal to 80% for some applications.

“Supported by a substrate” refers to a structure that is present at least partially on a substrate surface or present at least partially on one or more intermediate structures positioned between the structure and the substrate surface. The term “supported by a substrate” may also refer to structures partially or fully embedded in a substrate.

“Solution printing” is intended to refer to processes whereby one or more structures, such as printable semiconductor elements, are dispersed into a carrier medium and delivered in a concerted manner to selected regions of a substrate surface. In an exemplary solution printing method, delivery of structures to selected regions of a substrate surface is achieved by methods that are independent of the morphology and/or physical characteristics of the substrate surface undergoing patterning. Solution printing methods useable in the present invention include, but are not limited to, ink jet printing, thermal transfer printing, and capillary action printing.

“Substantially longitudinally oriented” refers to an orientation such that the longitudinal axes of a population of elements, such as printable semiconductor elements, are oriented substantially parallel to a selected alignment axis. In the context of this definition, substantially parallel to a selected axis refers to an orientation within 10 degrees of an absolutely parallel orientation, more preferably within 5 degrees of an absolutely parallel orientation.

“Stretchable” refers to the ability of a material, structure, device or device component to be strained without undergoing fracture. In an exemplary embodiment, a stretchable material, structure, device or device component may undergo strain larger than about 0.5% without fracturing, preferably for some applications strain larger than about 1% without fracturing and more preferably for some applications strain larger than about 3% without fracturing.

The terms “flexible” and “bendable” are used synonymously in the present description and refer to the ability of a material, structure, device or device component to be deformed into a curved shape without undergoing a transformation that introduces significant strain, such as strain characterizing the failure point of a material, structure,

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device or device component. In an exemplary embodiment, a flexible material, structure, device or device component may be deformed into a curved shape without introducing strain larger than or equal to about 5%, preferably for some applications larger than or equal to about 1%, and more preferably for some applications larger than or equal to about 0.5%.

“Semiconductor” refers to any material that is a material that is an insulator at a very low temperature, but which has appreciable electrical conductivity at a temperatures of about 300 Kelvin. In the present description, use of the term semiconductor is intended to be consistent with use of this term in the art of microelectronics and electrical devices. Semiconductors useful in the present invention may comprise element semiconductors, such as silicon, germanium and diamond, and compound semiconductors, such as group IV compound semiconductors such as SiC and SiGe, group III-V semiconductors such as AlSb, AlAs, Aln, AlP, BN, GaSb, GaAs, GaN, GaP, InSb, InAs, InN, and InP, group III-V ternary semiconductors alloys such as  $Al_xGa_{1-x}As$ , group II-VI semiconductors such as CsSe, CdS, CdTe, ZnO, ZnSe, ZnS, and ZnTe, group I-VII semiconductors CuCl, group IV-VI semiconductors such as PbS, PbTe and SnS, layer semiconductors such as PbI<sub>2</sub>, MoS<sub>2</sub> and GaSe, oxide semiconductors such as CuO and Cu<sub>2</sub>O. The term semiconductor includes intrinsic semiconductors and extrinsic semiconductors that are doped with one or more selected materials, including semiconductor having p-type doping materials and n-type doping materials, to provide beneficial electrical properties useful for a given application or device. The term semiconductor includes composite materials comprising a mixture of semiconductors and/or dopants. Specific semiconductor materials useful for in some applications of the present invention include, but are not limited to, Si, Ge, SiC, AlP, AlAs, AlSb, GaN, GaP, GaAs, GaSb, InP, InAs, GaSb, InP, InAs, InSb, ZnO, ZnSe, ZnTe, CdS, CdSe, ZnSe, ZnTe, CdS, CdSe, CdTe, HgS, PbS, PbSe, PbTe, AlGaAs, AlInAs, AlInP, GaAsP, GaInAs, GaInP, AlGaAsSb, AlGaInP, and GaInAsP. Porous silicon semiconductor materials are useful for applications of the present invention in the field of sensors and light emitting materials, such as light emitting diodes (LEDs) and solid state lasers. Impurities of semiconductor materials are atoms, elements, ions and/or molecules other than the semiconductor material(s) themselves or any dopants provided to the semiconductor material. Impurities are undesirable materials present in semiconductor materials which may negatively impact the electrical properties of semiconductor materials, and include but are not limited to oxygen, carbon, and metals including heavy metals. Heavy metal impurities include, but are not limited to, the group of elements between copper and lead on the periodic table, calcium, sodium, and all ions, compounds and/or complexes thereof. Gold is a specific heavy metal impurity which significantly degrades the electrical properties of semiconductors.

“Plastic” refers to any synthetic or naturally occurring material or combination of materials that can be molded or shaped, generally when heated, and hardened into a desired shape. Exemplary plastics useful in the devices and methods of the present invention include, but are not limited to, polymers, resins and cellulose derivatives. In the present description, the term plastic is intended to include composite plastic materials comprising one or more plastics with one or more additives, such as structural enhancers, fillers, fibers, plasticizers, stabilizers or additives which may provide desired chemical or physical properties.

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"Dielectric" and "dielectric material" are used synonymously in the present description and refer to a substance that is highly resistant to flow of electric current. Useful dielectric materials include, but are not limited to,  $\text{SiO}_2$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{TiO}_2$ ,  $\text{ZrO}_2$ ,  $\text{Y}_2\text{O}_3$ ,  $\text{SiN}_4$ ,  $\text{STO}$ ,  $\text{BST}$ ,  $\text{PLZT}$ ,  $\text{PMN}$ , and  $\text{PZT}$ .

"Polymer" refers to a molecule comprising a plurality of repeating chemical groups, typically referred to as monomers. Polymers are often characterized by high molecular masses. Polymers useable in the present invention may be organic polymers or inorganic polymers and may be in amorphous, semi-amorphous, crystalline or partially crystalline states. Polymers may comprise monomers having the same chemical composition or may comprise a plurality of monomers having different chemical compositions, such as a copolymer. Cross linked polymers having linked monomer chains are particularly useful for some applications of the present invention. Polymers useable in the methods, devices and device components of the present invention include, but are not limited to, plastics, elastomers, thermoplastic elastomers, elastoplastics, thermostats, thermoplastics and acrylates. Exemplary polymers include, but are not limited to, acetal polymers, biodegradable polymers, cellulosic polymers, fluoropolymers, nylons, polyacrylonitrile polymers, polyamide-imide polymers, polyimides, polyarylates, polybenzimidazole, polybutylene, polycarbonate, polyesters, polyetherimide, polyethylene, polyethylene copolymers and modified polyethylenes, polyketones, poly(methyl methacrylate, polymethylpentene, polyphenylene oxides and polyphenylene sulfides, polyphthalamide, polypropylene, polyurethanes, styrenic resins, sulphone based resins, vinyl-based resins or any combinations of these.

"Elastomer" refers to a polymeric material which can be stretched or deformed and return to its original shape without substantial permanent deformation. Elastomers commonly undergo substantially elastic deformations. Exemplary elastomers useful in the present invention may comprise, polymers, copolymers, composite materials or mixtures of polymers and copolymers. Elastomeric layer refers to a layer comprising at least one elastomer. Elastomeric layers may also include dopants and other non-elastomeric materials. Elastomers useful in the present invention may include, but are not limited to, thermoplastic elastomers, styrenic materials, olefinic materials, polyolefin, polyurethane thermoplastic elastomers, polyamides, synthetic rubbers, PDMS, polybutadiene, polyisobutylene, poly(styrene-butadiene-styrene), polyurethanes, polychloroprene and silicones.

The term "electromagnetic radiation" refers to waves of electric and magnetic fields. Electromagnetic radiation useful for the methods of the present invention includes, but is not limited to, gamma rays, X-rays, ultraviolet light, visible light, infrared light, microwaves, radio waves or any combination of these.

"Good electronic performance" and "high performance" are used synonymously in the present description and refer to devices and device components have electronic characteristics, such as field effect mobilities, threshold voltages and on-off ratios, providing a desired functionality, such as electronic signal switching and/or amplification. Exemplary printable semiconductor elements of the present invention exhibiting good electronic performance may have intrinsic field effect mobilities greater than or equal  $100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , preferably for some applications greater than or equal to about  $300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . Exemplary transistors of the present invention exhibiting good electronic performance may have device field effect mobilities great than or equal to about 100

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$\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , preferably for some applications greater than or equal to about  $300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , and more preferably for some applications greater than or equal to about  $800 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . Exemplary transistors of the present invention exhibiting good electronic performance may have threshold voltages less than about 5 volts and/or on-off ratios greater than about  $1 \times 10^4$ .

"Large area" refers to an area, such as the area of a receiving surface of a substrate used for device fabrication, greater than or equal to about 36 inches squared.

"Device field effect mobility" refers to the field effect mobility of an electrical device, such as a transistor, as computed using output current data corresponding to the electrical device.

"Conformal contact" refers to contact established between surfaces, coated surfaces, and/or surfaces having materials deposited thereon which may be useful for transferring, assembling, organizing and integrating structures (such as printable semiconductor elements) on a substrate surface. In one aspect, conformal contact involves a macroscopic adaptation of one or more contact surfaces of a conformable transfer device e to the overall shape of a substrate surface. In another aspect, conformal contact involves a microscopic adaptation of one or more contact surfaces of a conformable transfer device to a substrate surface leading to an intimate contact with out voids. The term conformal contact is intended to be consistent with use of this term in the art of soft lithography. Conformal contact may be established between one or more bare contact surfaces of a conformable transfer device and a substrate surface. Alternatively, conformal contact may be established between one or more coated contact surfaces, for example contact surfaces having a transfer material, printable semiconductor element, device component, and/or device deposited thereon, of a conformable transfer device and a substrate surface. Alternatively, conformal contact may be established between one or more bare or coated contact surfaces of a conformable transfer device and a substrate surface coated with a material such as a transfer material, solid photoresist layer, prepolymer layer, liquid, thin film or fluid.

"Placement accuracy" refers to the ability of a transfer method or device to transfer a printable element, such as a printable semiconductor element, to a selected position, either relative to the position of other device components, such as electrodes, or relative to a selected region of a receiving surface. "Good placement" accuracy refers to methods and devices capable of transferring a printable element to a selected position relative to another device or device component or relative to a selected region of a receiving surface with spatial deviations from the absolutely correct position less than or equal to 50 microns, more preferably less than or equal to 20 microns for some applications and even more preferably less than or equal to 5 microns for some applications. The present invention provides devices comprising at least one printable element transferred with good placement accuracy.

"Fidelity" refers to a measure of how well a selected pattern of elements, such as a pattern of printable semiconductor elements, is transferred to a receiving surface of a substrate. Good fidelity refers to transfer of a selected pattern of elements wherein the relative positions and orientations of individual elements are preserved during transfer, for example wherein spatial deviations of individual elements from their positions in the selected pattern are less than or equal to 500 nanometers, more preferably less than or equal to 100 nanometers.

"Young's modulus" is a mechanical property of a material, device or layer which refers to the ratio of stress to strain for a given substance. Young's modulus may be provided by the expression;

$$E = \frac{(\text{stress})}{(\text{strain})} = \left( \frac{L_0}{\Delta L} \times \frac{F}{A} \right); \quad (\text{II})$$

wherein E is Young's modulus,  $L_0$  is the equilibrium length,  $\Delta L$  is the length change under the applied stress, F is the force applied and A is the area over which the force is applied. Young's modulus may also be expressed in terms of Lame constants via the equation:

$$E = \frac{\mu(3\lambda + 2\mu)}{\lambda + \mu}; \quad (\text{III})$$

wherein  $\lambda$  and  $\mu$  are Lame constants. High Young's modulus (or "high modulus") and low Young's modulus (or "low modulus") are relative descriptors of the magnitude of Young's modulus in a give material, layer or device. In the present invention, a High Young's modulus is larger than a low Young's modulus, preferably about 10 times larger for some applications, more preferably about 100 times larger for other applications and even more preferably about 1000 times larger for yet other applications.

In the following description, numerous specific details of the devices, device components and methods of the present invention are set forth in order to provide a thorough explanation of the precise nature of the invention. It will be apparent, however, to those of skill in the art that the invention can be practiced without these specific details.

This invention provides methods and devices for fabricating printable semiconductor elements and assembling printable semiconductor elements onto substrate surfaces. The present invention provides a variety of semiconductor elements that are printable including single crystalline inorganic semiconductors, composite semiconductor elements comprising a semiconductor structure operationally connected to one or more other device components, and stretchable semiconductor elements. The methods, devices and device components of the present invention are capable of generating high performance electronic and optoelectronic devices and arrays of devices, such as thin film transistors on flexible plastic substrates.

FIG. 1 schematically illustrates exemplary methods of the present invention for producing and assembling printable semiconductor elements comprising ribbons of single crystalline silicon. The process begins by providing a silicon-on-insulator (SOI) substrate 100 having a thin single crystalline silicon layer 105, a buried  $\text{SiO}_2$  layer 107 and Si handling layer 108. Optionally, the surface native oxide layer on thin single crystalline silicon layer 105, if present, may be removed, for example by exposing the surface of the SOI substrate 100 to dilute (1%) HF. Upon adequately stripping the native oxide layer, selected regions of external surface 110 of SOI substrate 100 are masked, thereby forming a pattern of mask elements 120, masked regions 125 and exposed surface regions 127 on external surface 110. In the embodiment shown in FIG. 1, external surface 110 is patterned with rectangular aluminum and gold surface layers which provide mask elements 120 that are capable of inhibiting etching of the masked regions 125 of external

surface 110. Mask elements 120 may have any size and shape including, but not limited to, square, rectangular, circular, elliptical, triangular shapes or any combinations of these shapes. In an exemplary embodiment, patterns of 5 Al/Au layers providing mask elements having desired geometries are fabricated using microcontact printing, nanocontact printing techniques, or photolithography, and etching methods (TFA for Au; AL-11 premixed Cyantec etchant for Al). Deposition of mask elements comprising thin metal 10 films may be provided by an electron beam evaporator, such as a Temescal BJD1800, for example by sequential deposition of Al (20 nm; 0.1 nm/s) and then Au (100 nm; 1 nm/s).

External surface 110 of SOI substrate 100 is anisotropically etched downward. As shown in FIG. 1, although 15 material is selectively removed from exposed surface regions 127, mask elements 120 prevent etching of masked regions 125, thereby generating a plurality of relief features 140 comprising single crystalline silicon structures having slightly angled side walls 141. In an exemplary embodiment 20 wherein relief features have side walls 141 having a thickness 147 of about 100 nanometers, exposed surface regions 127 are exposed to tetramethylammonium hydroxide (TMAH) for about 3.5 minutes. In this embodiment, etching generates smooth sidewalls on relief features 140 of single 25 crystal silicon having Al/Au mask elements 120, preferably with deviations from average surface positions of less than 10 nanometers. Relief features 140 may be lifted off of the substrate 100 when the underlying  $\text{SiO}_2$  layer 107 is partially or completely isotropically etched away, for example using 30 concentrated (49%) HF. Liftoff of the relief features 140 generates printable semiconductor elements 150 comprising discrete single crystalline silicon structures having one surface covered by a mask element. Mask elements 120, Al/Au layers in the present example, may be removed or may be 35 integrated directly into a final device structure, for example, as the source and drain electrodes in a thin film transistor. As shown in FIG. 1, the printable semiconductor elements 150 may be assembled onto the receiving surface of substrate surface 160, such as a plastic substrate, by either dry transfer 40 contact printing techniques (schematically shown by arrow 166) or by solution casting methods (schematically shown by arrow 165). Both assembly methods may be carried out at room temperature in an ambient environment and, therefore, are compatible with a wide range of substrates, including 45 low cost, flexible plastic substrates.

Use of dry transfer contact printing methods to assemble 50 printable semiconductor elements has the benefit of taking advantage of the known orientations and positions of the printable semiconductor elements just prior to their liftoff from the SOI substrate. In this case, procedures similar to those of soft lithographic transfer printing techniques are used to move the printable semiconductor elements from the SOI (after etching away the  $\text{SiO}_2$  but before lifting off the silicon) to desired locations on the device substrate. In 55 particular, a conformable elastomeric transfer element picks up the objects from the SOI surface and transfers them to a desired substrate. Similarly, the printable semiconductor elements can be directly transferred onto thin plastic substrates by Au cold welding using receptacle pads defined on the surface of the target substrate.

In an exemplary method, at least a portion of printable 60 semiconductor elements 150 are brought into conformal contact with the contact surface 170 of a conformable transfer device 175, such as an elastomeric transfer stamp, polymer transfer device or composite polymer transfer device, thereby bonding at least a portion of printable semiconductor elements 150 onto the contact surface 170.

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Printable semiconductor elements 150 disposed on the contact surface 170 of conformable transfer device 175 are brought into contact with a receiving surface of substrate 160, preferably in a manner establishing conformal contact between contact surface 170 and the receiving surface of substrate 160. Contact surface 170 is separated from printable semiconductor elements 150 in contact with receiving surface of substrate 160, thereby assembling printable semiconductor elements 150 onto the receiving surface. This embodiment of the present invention is capable of generating a pattern on the receiving surface comprising printable semiconductor elements 150 in well defined positions and spatial orientations. In the embodiment shown in FIG. 1, printable semiconductor elements 150 are operationally connected to gold pads 162 present on the receiving surface of substrate 160.

FIG. 2 provides a schematic diagram illustrating a selective dry transfer contact printing method for assembling printable semiconductor element on a receiving surface of a substrate. A plurality of printable semiconductor elements 300 are fabricated on a mother substrate 305 in a first pattern 310 of printable semiconductor elements 300 characterized by well defined positions and spatial orientations. A conformable transfer device 315 having a contact surface 320 with a plurality of discrete binding regions 325 is brought into conformal contact with at least a portion of printable semiconductor elements 300 on mother substrate 305. Binding regions 325 on contact surface 320 are characterized by an affinity for printable semiconductor elements 310, and may be chemically modified regions, such regions having hydroxyl groups extending from the surface of a PDMS layer, or regions coated with one or more adhesive layers. Conformal contact transfers at least a portion of printable semiconductor elements 310 which contact binding regions 325 on contact surface 320. Printable semiconductor elements 310 transferred to contact surface 320 are brought into contact with receiving surface 330 of substrate 335, which may be a flexible substrate such as a plastic substrate. Subsequent separation of semiconductor elements 310 and contact surface 320 results in assembly of the semiconductor elements 310 on receiving surface 330 of substrate 335, thereby generating a second pattern 340 of printable semiconductor elements characterized by well defined positions and spatial orientations different from the first pattern of printable semiconductor elements 340. As shown in FIG. 2, the printable semiconductor elements 340 that remain on mother substrate 305 are characterized by a third pattern 345 of printable semiconductor elements different from first and second patterns of printable semiconductor elements. Printable semiconductor elements 340 comprising the third pattern 345 may be subsequently transferred to and/or assembled onto substrate 335 or another substrate using the printing methods of the present invention, including selective dry transfer methods.

FIGS. 3A-C, are schematic diagrams showing devices, device configurations and device components useful in selective dry transfer contact printing methods of the present invention. FIG. 3A shows a plurality of printable semiconductor elements 300 on a mother substrate 305, wherein selected printable semiconductor elements 300 have one or more adhesive coatings 350. As shown in FIG. 3A, adhesive coatings 350 are provided in a well defined pattern. FIG. 3B shows a conformable transfer device 315 having a contact surface 320 with a plurality of discrete binding regions 325 provided in a well defined pattern. FIG. 3C shows a conformable transfer device 315 having a three dimensional relief pattern 355 comprising relief features 360 provided in

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a well defined pattern. In the embodiment shown in FIG. 3C, relief pattern 355 provides a plurality of contact surfaces 320 that may be optionally coated with one or more adhesive layers. Patterns of adhesive coatings 350, binding regions 325 and relief features 360 preferably corresponding to relative positions and spatial orientations of printable semiconductor elements 300 in device configurations or device array configurations, such as thin film transistor array configurations.

Use of dry transfer printing methods are useful in the present invention for assembling, organizing and integrating printable semiconductor elements on substrates having a wide range of compositions and surface morphologies, including curved surfaces. To demonstrate this functional capability of the present methods and compositions, semiconductor elements comprising silicon photodiodes were printed directly (i.e. no adhesive) onto the curved surfaces of a variety of optical lenses using dry transfer printing methods employing an elastomeric stamp. FIG. 3D provides a photograph of an array of photodiodes printed onto a spherical surface of a polycarbonate lens (FL 100 mm). FIG. 3E provides a scanning electron micrograph of an array of photodiodes printed onto the curved surface of a spherical glass lens (FL 1000 mm). Contrast in the image provided in FIG. 3E is slightly enhanced to show p-doped regions. FIG. 3F provides a plot of electric current ( $\mu$ A) verse bias potential (volts) illustrating the light response of the photodiodes pictured in FIG. 3E.

FIGS. 4A1 and 4A2 show a preferred shape of a printable semiconductor element for assembly methods of the present invention using dry transfer contact printing. FIG. 4A1 provides a perspective view and FIG. 4A2 provides a top plan view. Printable semiconductor element comprises a ribbon 500 extending along a central longitudinal axis 502 having a first end 505, center region 510 and second end 515. As shown in FIG. 4A, the width of ribbon 500 selectively varies along its length. Particularly, first and second ends 505 and 515 are wider than center region 510. In an exemplary method, ribbon 500 is formed by etching mother substrate 520. In this embodiment, mother substrate is isotropically exposed to an enant until ribbon 500 is only attached to mother substrate 520 by two alignment maintaining elements comprising sacrificial layers 525 proximate to first and second ends 505 and 515. At this point in the fabrication process the etching process is stopped, and the ribbon 500 is brought into contact with and/or bonded to a conformable transfer device. Sacrificial layers 525 are broken and ribbon 500 is released as the transfer device is moved away from mother substrate 520. This method may also be applied to dry transfer contact printing of a plurality of printable semiconductor elements having shapes as shown in FIG. 4. An advantage of this method of the present invention is that the orientations and relative positions of a plurality of ribbons 500 on mother substrate 520 may be precisely preserved during transfer, assembly and integration steps. Exemplary ranges for the thickness of the sacrificial layers are ~1 um down to ~100 nm with ribbons widths between ~2 um and 100 um. Interestingly, the cleavage of the ribbons typically occurs at the extremity of the objects (very close to the point/edge where the ribbons are attached to the mother wafer). Wide ribbons usually do not distort during the lift-off process are they are bonded to the stamp.

FIGS. 4B1 and 4B2 show a preferred shape of a printable semiconductor element for assembly methods of the present invention using dry transfer contact printing. FIG. 4B1 provides a perspective view and FIG. 4B2 provides a top plan view. Printable semiconductor element comprises rib-

bons 527 extending along a parallel central longitudinal axes 528. Ribbons 527 are held in a selected position and orientation by alignment maintaining elements 530 which connect at least on end of the ribbon along the central longitudinal axes 528 to mother substrate 529. alignment maintaining elements 530 are fabricated during patterning of ribbons 527 by not defining one or both ends of the ribbon along their central longitudinal axes. Alignment maintaining elements 530 are broken and ribbons 527 are released upon contact with the ribbons with the contact surface of a transfer device and subsequent movement away from mother substrate 520.

To achieve assembly by solution printing, at least a portion of printable semiconductor elements 150 are dispersed into a carrier medium, thereby generating a suspension 190 comprising semiconductor element elements 150 in the carrier medium. Printable semiconductor elements 150 are delivered to the substrate and assembled by solution printing the suspension onto the receiving surface of substrate 160. Solution printing may be provided by a number of techniques known in the art including, but not limited to, ink jet printing, thermal transfer printing and screen printing. In the embodiment shown in FIG. 1, printable semiconductor elements 150 are operationally connect to gold pads 162 present on the receiving surface of substrate 160.

FIG. 5A-C presents optical and scanning electron micrographs of a range of printable semiconductor elements 150 comprising microstrips of single crystalline silicon having selected physical dimensions. Printable semiconductor elements are shown in ethanol suspensions and as cast onto substrates of various types. FIG. 5A shows an optical micrograph of a solution cast tangled mat of silicon rods (widths 2 microns; thickness 2 microns; lengths ~15 millimeters). The inset image shows printable silicon strips (roughly 10 million of them) dispersed in a solution of ethanol. The low resolution SEM image in FIG. 5B illustrates the mechanical flexibility range of some flat microstrips (thickness 340 nanometers; widths 5 microns; lengths ~15 millimeters) solution casted onto a bare silicon wafer. FIG. 5C presents a high resolution SEM image of one of these objects. Note the extremely smooth sidewalls generated by the anisotropic wet etching procedures.

Printable semiconductor elements in the form of wires, platelets and disks may also be formed using the methods of the present invention. By use of large area soft lithographic techniques, it is possible, in a single low cost processing sequence, to produce large numbers (i.e. billions) of printable semiconductor elements with lateral dimensions down to 50 nm and with nearly any geometry. Printable semiconductor elements having lateral dimension as small as 20 nanometer may also be fabricated by the methods of present invention. For use in thin film transistors in flexible electronic systems, printable semiconductor elements comprising long (~10 microns) and narrow (~1 microns) strips of single crystalline silicon are particularly useful.

FIG. 6 presents an image of transferred printable semiconductor elements comprising single crystalline silicon microstrips on a PDMS coated polyimide sheet having a thickness of about 25 microns. The top inset pictures illustrate the intrinsic flexibility of this system. The bottom inset shows a top view micrograph of printable silicon dense microstrips (25 microns wide, ~2 microns spaced apart) cold welded on a thin Ti/Au coated Mylar sheet. As shown in FIG. 6, the printable semiconductor elements comprising silicon microstrips are well aligned and transferred with controlled orientation. No cracking of the printable semiconductor elements induced by assembly was observed upon

careful examination using scanning electron microscopy, even when the substrate was bent significantly. Similar results were obtained (without the need of an elastomeric layer) using a Au coated thin Mylar sheet as illustrated by the bottom inset micrograph picture. A coverage density close to 100% can be achieved in this manner.

The present invention also provides composite printable semiconductor elements comprising a semiconductor structure operationally connect to one or more other device components, such as dielectric elements, conducting elements (i.e. electrodes) or additional semiconductor elements. An exemplary printable semiconductor elements of the present invention that is particularly useful for fabricating thin film transistors comprises an integrated semiconductor and dielectric element. Such composite printable semiconductor elements provide transistors having high quality, leak free dielectrics and avoids the need for separate spin casting steps for fabricating the dielectric element in a thin film transistor. In addition, use of composite printable semiconductor elements enables efficient device fabrication on large substrate areas by low cost printing techniques.

The following references relate to self assembly techniques which may be used in methods of the present invention to transfer, assembly and interconnect printable semiconductor elements via contact printing and/or solution printing techniques: (1) "Guided molecular self-assembly: a review of recent efforts", Jiyun C Huie *Smart Mater. Struct.* (2003) 12, 264-271; (2) "Large-Scale Hierarchical Organization of Nanowire Arrays for Integrated Nanosystems", Whang, D.; Jin, S.; Wu, Y.; Lieber, C. M. *Nano Lett.* (2003) 3(9), 1255-1259; (3) "Directed Assembly of One-Dimensional Nanostructures into Functional Networks", Yu Huang, Xiangfeng Duan, Qingqiao Wei, and Charles M. Lieber, *Science* (2001) 291, 630-633; and (4) "Electric-field assisted assembly and alignment of metallic nanowires", Peter A. Smith et al., *Appl. Phys. Lett.* (2000) 77(9), 1399-1401.

All references cited in this application are hereby incorporated in their entireties by reference herein to the extent that they are not inconsistent with the disclosure in this application. Some references provided herein are incorporated by reference to provide details concerning sources of starting materials, additional starting materials, additional reagents, additional methods of synthesis, additional methods of analysis and additional uses of the invention. It will be apparent to one of ordinary skill in the art that methods, devices, device elements, materials, procedures and techniques other than those specifically described herein can be applied to the practice of the invention as broadly disclosed herein without resort to undue experimentation. All art-known functional equivalents of methods, devices, device elements, materials, procedures and techniques specifically described herein are intended to be encompassed by this invention.

U.S. Patent Application Nos. 60/577,077, 60/601,061, 60/650,305, 60/663,391 and 60/677,617 filed on Jun. 4, 2004, Aug. 11, 2004, Feb. 4, 2005, Mar. 18, 2005, and May 4, 2005, respectively, are hereby incorporated by reference herein in their entireties to the extent not inconsistent with the disclosure of this application.

When a group of materials, compositions, components or compounds is disclosed herein, it is understood that all individual members of those groups and all subgroups thereof are disclosed separately. When a Markush group or other grouping is used herein, all individual members of the group and all combinations and subcombinations possible of the group are intended to be individually included in the

disclosure. Every formulation or combination of components described or exemplified herein can be used to practice the invention, unless otherwise stated. Whenever a range is given in the specification, for example, a temperature range, a time range, or a composition range, all intermediate ranges and subranges, as well as all individual values included in the ranges given are intended to be included in the disclosure.

As used herein, "comprising" is synonymous with "including," "containing," or "characterized by," and is inclusive or open-ended and does not exclude additional, unrecited elements or method steps. As used herein, "consisting of" excludes any element, step, or ingredient not specified in the claim element. As used herein, "consisting essentially of" does not exclude materials or steps that do not materially affect the basic and novel characteristics of the claim. In each instance herein any of the terms "comprising," "consisting essentially of" and "consisting of" may be replaced with either of the other two terms.

**Example 1: Thin Film Transistor Having a  
Printable Semiconductor Element**

The ability of printable semiconductor elements of the present invention to provide semiconductor channels in thin film transistors was verified by experimental studies. Specifically, it is a goal of the present invention to provide thin film transistors capable of fabrication on a flexible plastic substrates by printing methods. Further, it is a goal of the present invention to provide high performance thin film transistors on plastic substrates having field effect mobilities, on-off ratios and threshold voltages similar to or exceeding thin film transistors fabricated by convention high temperature processing methods.

FIG. 7 presents an optical micrograph image of a thin film transistor having a printable semiconductor element. The illustrated transistor 531 comprises source electrode 532, drain electrode 533, printable semiconductor element 534, dielectric (not shown in the micrograph in FIG. 7) and gate electrode (also not shown in the micrograph in FIG. 7). The thin film transistor is supported by a substrate comprising of a Mylar sheet coated with indium tin oxide (ITO, ~100 nanometers thick) as a gate and a photocured epoxy as a gate dielectric (SU8-5; Microchem Corp). The capacitance of the dielectric ( $2.85 \text{ nF/cm}^2$ ) was evaluated using capacitor test structures formed near the device. This device uses a solution cast printable semiconductor element comprising a ~5 millimeter long, 20 micron width and 340 nanometer thick microstrip fabricated from a p-doped SOI wafer (Soitec) with a 340 nanometer device layer thickness and resistivity of 14-22 ohm cm. A 25 nanometer thick layer of SiO<sub>2</sub> was grown on top of the silicon by dry oxidation in a horizontal quartz tube furnace. Source and drain electrodes of Al (20 nanometer)/Au (180 nanometer) where defined by lift-off techniques. The semiconductor channel length is 50 microns and the width is 20 microns.

FIGS. 8 and 9 show electrical measurements collected from thin film transistors of the present invention having a printable semiconductor element. The device operates similarly to a back gated SOI device with a top contact configuration. The semiconductor uses a width equal to a 20 microns microstrip of single crystal silicon in a channel whose length is equal to 50 microns. The printable semiconductor element in this case was patterned by solution casting methods. The source/drain contacts were defined by photolithography and lift off.

FIG. 8 provides a plot showing current-voltage (IV) characteristics of a device made on a pre-oxidized Si wafer. FIG. 9 provides a plot showing transfer characteristics measured at  $V_{DS}=0.1 \text{ V}$  of a device made on a Mylar sheet 5 coated with ITO gate and polymer dielectric. The slope of this curve defines an effective device mobility (using the physical width of the source and drain electrodes, which is equal to the width of the semiconductor element microstrip in this case) of  $180 \text{ cm}^2/\text{Vs}$ . The Al/Au metallization for the 10 contacts to the printable semiconductor element provides reasonably low resistance Schottky barrier contacts to the silicon, as expected for an Al (work function of 4.2 eV) metallization on p-doped silicon. Aluminum is well known to diffuse rapidly into silicon, but no special care was taken 15 to avoid localized aluminum-silicon interactions as no post metallization high temperature annealing step was carried out. The on/off ratio of this device is slightly lower than  $10^3$ . Analysis of the transfer characteristic of FIG. 9 indicates a 20 linear field effect mobility of  $180 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  using a parallel plate model for the dielectric capacitance. This analysis ignores the effects of contacts and processing induced changes in the threshold voltage.

Even with perfect contacts, there are theoretical arguments to suggest that transistors which incorporate very high 25 aspect ratio (i.e. ultra large length to width ratios) semiconducting elements in the channel region (i.e. nanotubes or nanowires) will have responses that are different than those of conventional devices. To avoid these effects, we chose 30 printable semiconductor elements comprising microstrips having widths on the same order of magnitude with the transistor channel length. The properties (mobilities, normalized transconductance, on/off ratio) observed here are ~ $\frac{3}{4}$  to those of thin film transistors made on the SOI substrate after etching of the Si but before liftoff. In these 35 measurements the buried SiO<sub>2</sub> oxide acts as the dielectric and the silicon supporting substrate acts as the gate electrode. This result demonstrates that the processing steps used to produce the printable semiconductor elements and to transfer it to the device substrate do not alter significantly the 40 properties of the silicon or its surfaces that result from the initial patterning and silicon etching steps. It also indicates that the van der Waals interface with the SU8 dielectric is capable of supporting good device properties.

A principle advantage of the fabrication method of the 45 present example is that it separates the crystal growth and processing of the silicon from the plastic substrate and other components of the devices. In addition, the methods of processing printable semiconductor elements of the present invention are highly flexible in the processing sequences and 50 in the materials choices that are possible. For example, an SiO<sub>2</sub> layer can be formed on one side of the silicon (by, for example, growing a thermal oxide before lifting off the Si elements or lifting the SOI buried oxide together with the Si device layer) to yield an integrated dielectric, in a strategy 55 similar to that for the integrated source/drain metallization demonstrated here. A dielectric introduced in this manner may avoid the significant challenges that can be associated with leakage, hysteresis, doping, trapping, etc. in many solution cast thin dielectrics on plastic substrates.

FIGS. 10A-H provide a schematic diagram illustrating a 60 method of the present invention for making an array of thin film transistors having composite printable semiconductor elements. As shown in FIG. 10A, gate electrodes 547 are deposited on the surface 548 of a thin sheet of a flexible substrate, such as Kapton, Mylar or PET. Gate electrodes 65 may be patterned on the flexible substrate by any means known in the art including but not limited to photolithog-

raphy, microtransfer printing, nanotransfer printing, soft lithography or combinations of these. As shown in FIG. 10B, the method further comprises the step of fabricating a plurality of composite printable semiconductor elements 550 comprising single crystalline silicon structures 555 operationally connected to a SiO<sub>2</sub> dielectric element 560. As illustrated in FIG. 10B, composite printable semiconductor elements 550 have a ribbon shape extending a selected length 552 along a central longitudinal axis 551. Composite printable semiconductor element 550 has a selected thickness 553 and a width that varies as a function of thickness.

As shown in FIG. 10C, the method further comprises the step of assembling composite printable semiconductor elements 550 onto gate electrodes 547 and substrate 548 via dry transfer contact printing or solution printing. Composite printable semiconductor elements 550 are oriented such that SiO<sub>2</sub> dielectric elements 560 are in contact with gate electrodes 547. As shown in FIG. 10D, the method further comprises the step of spin coating a thin layer of positive photoresist 561 on the patterned surface of substrate 548. Alternatively, the thin layer of positive photoresist 561 may be applied to the pattern surface of substrate 548 using a roller. Regions of photoresist 561 not masked by gate electrodes 547 are exposed to a beam of electromagnetic radiation transmitted through underside 562 of substrate 548. Use of an optically transmissive substrate 548 is preferred for this method of the present invention, particularly a substrate 548 that is at least partially transparent in ultraviolet and/or visible regions of the electromagnetic spectrum. As shown in FIG. 10E, the method further comprises the step of developing the thin photoresist layer. As shown in this figure, the regions of thin photoresist layer 561 that are shadow masked by the gate electrodes are undeveloped. As shown in FIG. 10F, the method further comprises the step of dry or wet etching the integrated SiO<sub>2</sub> dielectric, thereby opening contacts for source and drain electrodes. In the embodiment illustrated by FIG. 10F this is achieved by exposing the patterned surface of substrate 548 to a CF<sub>4</sub> plasma. As shown in FIG. 10G, the method further comprises the step of defining source and drain electrodes by shadow mask evaporation. The alignment of semiconductor elements, source electrodes and drain electrodes does not need to be very precise because the semiconductor channels will be defined in the next fabrication step. As shown in FIG. 10H, the method further comprises the step of defining the semiconductor channel by lifting off the positive resist, for example by exposure to a solvent such as acetone.

FIGS. 11A-D provide diagrams illustrating a method of the present invention for making a printable device comprising integrated gate electrode, gate dielectric, semiconductor, source electrode and drain electrode. As shown in FIG. 11A, a high quality gate dielectric is grown by thermal oxidation of the surface of a SOI wafer. Next, the gate electrode material (such as metal or doped poly-silicon) is deposited. Selected regions of the top surface are subsequently masked using for example a lithography process. In one embodiment, an array of identical patterns with controlled spacing will be defined in a single masking step. Printable semiconductor elements are then fabricated by anisotropically wet and/or dry etching. Preferentially, three different selective etching processes are carried out sequentially to etch away the exposed areas of the gate electrode material, the gate dielectric and the top silicon layer.

A lithography process, as shown in FIG. 11B, is used to define the channel of the transistors. In this process step, the exposed areas of the gate electrode material are etched away (dry or wet etching). As shown in FIG. 11C, the photo-resist

is then heated above its glass transition, thereby initiating a reflow process. The reflowing distance of the photoresist can be selected by carefully selecting an appropriate thickness of the photo-resist layer, the glass transition temperature of the photo-resist layer or the temperature and duration of the reflow process. The exposed areas of the gate dielectric are then etched using an HF solution.

Next, a metallization process, as shown in FIG. 11D, is carried out, followed by lifting off the metal deposited onto the photoresist to complete the fabrication of a printable device. The source and drain electrodes are self aligned with the gate, and the spacing between source and drain electrodes may be selected by the adjusting the different parameters, such as temperature and duration, of the reflow process.

The printable device shown in FIG. 11D may be transferred and assembled onto a substrate, such as a plastic substrate, by the dry transfer or solution printing methods of the present invention. The self aligned process illustrated in FIGS. 11A-D presents a simple way to integrate all the elements necessary for the realization of a printable device, such as a MOSFET device. A significant advantage of this fabrication method of the present invention is that all processes steps which require temperatures incompatible with plastic substrates (e.g. requiring temperature>about 400 Celsius) may be carried on the SOI substrate prior to lifting off and transferring the device to the substrate. For example, additional processing steps such as doping of the source and drain contact areas, formation of silicide layers, and high temperature annealing of the device could be performed prior to transferring the elements onto a plastic substrate.

#### Example 2: Stretchable Printable Semiconductor Elements

The present invention provides stretchable printable semiconductor elements capable of providing good performance when stretched, flexed or deformed. Further, stretchable printable semiconductor elements of the present invention may be adapted to a wide range of device configurations to provide fully flexible electronic and optoelectronic devices.

FIG. 12 provides an atomic force micrograph showing a stretchable printable semiconductor element of the present invention. The stretchable printable semiconductor element 700 comprises a flexible substrate 705 having a supporting surface 710 and a bent semiconductor structure 715 having a curved internal surface 720. In this embodiment, at least a portion of the curved internal surface 720 of bent semiconductor structure 715 is bonded to the supporting surface 710 of the flexible substrate 705. The curved internal surface 720 may be bonded supporting surface 710 at selected points along internal surface 720 or at substantially all points along internal surface 720. The exemplary semiconductor structure illustrated in FIG. 12 comprises a bent ribbon of single crystalline silicon having a width equal to about 100 microns and a thickness equal to about 100 nanometers. The flexible substrate illustrated in FIG. 12 is a PDMS substrate having a thickness of about 1 millimeter. Curved internal surface 720 has a contour profile characterized by a substantially periodic wave extending along the length of the ribbon. As shown in FIG. 12, the amplitude of the wave is about 500 nanometers and the peak spacing is approximately 20 microns. FIG. 13 shows an atomic force micrograph providing an expanded view of a bent semiconductor structure 715 having curved internal surface 720. FIG. 14 shows an atomic force micrograph of an array of stretchable printable

semiconductor elements of the present invention. Analysis of the atomic force micrograph in FIG. 14 suggests that the bent semiconductor structures are compressed by about 0.27%. FIG. 15 shows optical micrographs of stretchable printable semiconductor elements of the present invention.

The contour profile of curved surface 720 allows the bent semiconductor structure 715 to be expanded or contracted along deformation axis 730 without undergoing substantial mechanical strain. This contour profile may also allow the semiconductor structure to be bent, flexed or deformed in directions other than along deformation axis 730 without significant mechanical damage or loss of performance induced by strain. Curved surfaces of semiconductor structures of the present invention may have any contour profile providing good mechanical properties, such as stretchability, flexibility and/or bendability, and/or good electronic performance, such as exhibiting good field effect mobilities when flexed, stretched or deformed. Exemplary contour profiles may be characterized by a plurality of convex and/or concave regions, and by a wide variety of wave forms including sine waves, Gaussian waves, Aries functions, square waves, Lorentzian waves, periodic waves, aperiodic waves or any combinations of these. Wave forms useable in the present invention may vary with respect to two or three physical dimensions.

FIG. 16 shows an atomic force micrograph of a stretchable printable semiconductor element of the present invention having a bent semiconductor structure 715 bonded to a flexible substrate 705 having a three dimensional relief pattern on its supporting surface 710. The three-dimensional relief pattern comprises recessed region 750 and relief features 760. As shown in FIG. 16, bent semiconductor structure 715 is bound to supporting surface 710 in recessed region 750 and on relief features 760.

FIG. 17 shows a flow diagram illustrating an exemplary method of making a stretchable semiconductor element of the present invention. In the exemplary method, a prestrained elastic substrate in an expanded state is provided. Prestraining can be achieved by any means known in the art including, but not limited to, roll pressing and/or prebending the elastic substrate. An exemplary elastic substrate useable in this method of the present invention is a PDMS substrate having a thickness equal to about 1 millimeter. The elastic substrate may be prestrained by expansion along a single axis or by expansion along a plurality of axes. As shown in FIG. 17, at least a portion of the internal surface of a printable semiconductor structure is bonded to the external surface of the prestrained elastic substrate in an expanded state. Bonding may be achieved by covalent bonding between the internal surface of the semiconductor surface, by van der Waals forces, by using adhesive or any combinations of these. In an exemplary embodiment wherein the elastic substrate is PDMS, the supporting surface of the PDMS substrate is chemically modified such that it has a plurality of hydroxyl groups extending from its surface to facilitate covalent bonding with a silicon semiconductor structure. Referring back to FIG. 17, after binding the prestrained elastic substrate and semiconductor structure, the elastic substrate is allowed to relax at least partially to a relaxed state. In this embodiment, relaxation of the elastic substrate bends the internal surface of said printable semiconductor structure, thereby generating a semiconductor element having a curved internal surface.

As shown in FIG. 17, the fabrication method may optionally include a second transfer step wherein the semiconductor structure 715 having a curved internal surface 720 is transferred from the elastic substrate to another substrate,

preferably a flexible substrate. This second transfer step may be achieved by bringing an exposed surface of the semiconductor structure 715 having a curved internal surface 720 in contact with a receiving surface of the other substrate that binds to the exposed surface of the semiconductor structure 715. Bonding to the other substrate may be accomplished by any means in the art including covalent bonds, bonding via van der Waals forces and the use of adhesives.

Stretchable semiconductor elements of the present invention may be effectively integrated into a large number functional devices and device components, such as transistors, diodes, lasers, MEMS, NEMS, LEDs and OLEDS. Stretchable semiconductor elements of the present invention have certain advantages over conventional rigid inorganic semiconductors. First, stretchable semiconductor elements may be flexible, and thus, less susceptible to structural damage induced by flexing, bending and/or deformation than conventional rigid inorganic semiconductors. Second, as a bent semiconductor structure may be in a slightly mechanically strained state to provide a curved internal surface, stretchable semiconductor elements of the present invention may exhibit higher intrinsic field effect mobilities than conventional unstrained inorganic semiconductors. Finally, stretchable semiconductor elements are likely to provide good thermal properties because they are capable of expanding and contracting freely upon device temperature cycling.

### Example 3: Methods of Making Printable Semiconductor Elements

The present invention provides methods of making printable semiconductor elements from a wide range of starting materials, including single crystalline wafers, silicon on substrate wafers, germanium wafers, thin films of polycrystalline silicon and ultra thin silicon wafers. Particularly, the present invention provides low cost methods of making large numbers of printable semiconductors in selected orientations and relative positions.

FIG. 18A shows an exemplary method for making printable semiconductor elements from a Si—Ge epi substrate. In this method, selective regions of a Si epi layer are masked by depositing a mask material, such as a thin film comprising a metal,  $\text{SiO}_2$  or  $\text{SiN}$ . This masking step defines shape and some of the physical dimensions (e.g. length and width for a ribbon) of the printable semiconductor elements to be fabricated. The exposed Si surface of the Si—Ge epi substrate is anisotropically etched by either dry or wet chemical etching methods. This generates relief features of silicon, preferably having smooth side walls, that can be effectively released from the Si—Ge epi substrate by lift off techniques, for example using selective SiGe wet etching provided by  $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  1:1:4 at 50° C. Optionally, source electrode, gain electrode, gate electrode, dielectric element or any combinations of these may be integrated into the semiconductor element prior to lift off. An advantage of this fabrication method is that the mother substrate can be cleaned and re-used.

FIG. 18B shows an exemplary method for fabricating printable semiconductor elements from a bulk silicon substrate, preferably a single crystalline silicon substrate. In this method, a silicon wafer is first dry oxidized, for example in a quartz tube furnace at a temperature selected from the range of about 800 degrees Celsius to about 1200 degrees Celsius. Next, a thin layer of gate material is deposited on the oxidized surface of the silicon wafer. Exemplary gate materials include metals or doped polycrystalline silicon.

The thin layer of gate material is selectively patterned with photoresist. This patterning step defines the shape and some of the physical dimensions (e.g. length and width for a ribbon) of the printable semiconductor elements to be fabricated. The thin layer of gate material and dielectric layer are anisotropically back etched, thereby generating relief features comprising a photoresist layer, gate material layer, dielectric layer and silicon layer and, preferably having smooth side walls. Next, the photoresist layer is reflowed, for example by annealing to a temperature selected from the range of about 100 degrees Celsius to about 130 degrees Celsius. Reflowing the photoresist transfers a portion of the photoresist to the side walls of the relief features. As shown in FIG. 18B, the exposed Si surface is isotropically etched using wet or dry etching methods, thereby releasing the relief features and generating composite printable semiconductor elements, preferably having smooth surfaces. Isotropic etching of the silicon may be achieved using a HNO<sub>3</sub>:NH<sub>4</sub>F:H<sub>2</sub>O 64:3:33 solution. Advantages of this fabrication method are the relatively low cost of the silicon substrate starting materials and the ability to reuse the mother substrate after planarization (ECMP).

FIG. 18C shows another exemplary method of fabricating printable semiconductor elements from a bulk silicon substrate, preferably a single crystalline silicon substrate. In this method, the external surface of a bulk silicon substrate is selectively patterned with photoresist. This patterning step defines the shape and some of the physical dimensions (e.g. length and width for a ribbon) of the printable semiconductor elements to be fabricated. The patterned substrate surface is anisotropically etched, preferably using dry etching methods such as reactive ion etching and inductive coupled plasma etching, thereby generating relief features, preferably relief features having smooth side walls. At least a portion of the side walls of the relief features are masked by depositing a masking material such as a thin layer of metal, SiO<sub>2</sub> or SiN. In one embodiment, masking material is applied to the side walls of relief features by angled evaporative or sputtering deposition techniques combined with sample rotation to ensure deposition all exposed side walls. As shown in FIG. 18C, the exposed Si surface is isotropically etched using wet or dry etching methods, thereby releasing the relief features and generating printable semiconductor elements, preferably having smooth surfaces. Isotropic etching of the silicon may be achieved using a HNO<sub>3</sub>:NH<sub>4</sub>F:H<sub>2</sub>O 64:3:33 solution. Advantages of this fabrication method are the relatively low cost of the silicon substrate starting materials and the ability to reuse the mother substrate after planarization (ECMP).

FIG. 18D shows yet another exemplary method of fabricating printable semiconductor elements from a bulk silicon substrate, preferably a single crystalline silicon substrate. In this method, the external surface of a bulk silicon substrate is selectively patterned with photoresist. The patterned substrate surface is anisotropically etched, thereby generating relief features. Next the silicon substrate is annealed, for example by annealing in a quartz furnace at a temperature of about 1100 degrees Celsius and in nitrogen. Next, the surface of the annealed silicon substrate is patterned by masking selected regions with photoresist. This patterning step defines the shape and some of the physical dimensions (e.g. length and width for a ribbon) of the printable semiconductor elements to be fabricated. As shown in FIG. 18D, the patterned surface of the annealed Si substrate is anisotropically etched using wet or dry etching methods, thereby generating printable semiconductor elements, preferably having smooth surfaces. Advantages of this fabrication

method are the relatively low cost of the silicon substrate starting materials, the ability to reuse the mother substrate after planarization (ECMP) and the ability to integrate source electrode, drain electrode, gate electrode and dielectric device components after the annealing step. In addition, wet etching may be used in the first etching step with a 110 silicon wafer.

FIG. 18E shows an exemplary method of fabricating printable semiconductor elements from an ultra thin silicon substrate. In this method, the external surface of an ultra thin silicon substrate is selectively patterned with photoresist. This patterning step defines the shape and some of the physical dimensions (e.g. length and width for a ribbon) of the printable semiconductor elements to be fabricated. The patterned substrate surface is anisotropically etched through thickness of the ultra thin silicon substrate, thereby printable semiconductor elements. Ultra thin silicon substrates having thicknesses selected from the range of about 10 microns to about 500 microns are preferred for some applications of this fabrication method. An advantage of this fabrication method is the relatively low cost of the ultra thin silicon substrate starting materials.

FIGS. 18F and 18G show exemplary methods for making printable semiconductor elements from thin films of polycrystalline silicon. In this method, a thin layer of polycrystalline silicon is deposited on a supporting substrate, such as glass or silicon substrate, having a sacrificial surface layers, such as a coating comprising SiN or SiO<sub>2</sub>. The polycrystalline thin film is then annealed, and selective regions of the exposed surface are selectively masked by depositing a mask material, such as a thin films comprising a metals, SiO<sub>2</sub> or SiN. This masking step defines shape and some of the physical dimensions (e.g. length and width for a ribbon) of the printable semiconductor elements to be fabricated. The patterned surface is anisotropically etched by either dry or wet chemical etching methods, generating relief features of silicon supported by the sacrificial layer, preferably relief features having smooth side walls. Isotropically etching the sacrificial layer releases the relief features, thereby generating printable semiconductor elements. An advantage of this fabrication method is that the supporting substrate can be cleaned and reused. Alternatively, a thin layer of polycrystalline silicon may be deposited directly on a SiO<sub>2</sub> substrate. As shown in FIG. 18G, similar annealing, patterning, anisotropic etching and lift off steps may be used to generate printable semiconductor elements. Optionally, source electrode, gain electrode, gate electrode, dielectric element or any combinations of these may be integrated into the semiconductor element prior to lift off in either of these methods.

FIGS. 18H(1) and 18H(2) illustrate a method for making single crystalline semiconductor films using printable semiconductor elements of the present invention. As shown in FIG. 18H(1), an amorphous or poly-crystalline semiconductor thin film is prepared on the surface of a substrate comprising an insulating material, such as SiO<sub>2</sub>. The thin amorphous or poly-crystalline semiconductor film may prepared by any means known in the art including, but not limited to, deposition techniques such as vapor deposition or sputtering deposition. Also referring to FIG. 18H(1), a printable semiconductor element comprising a single crystalline semiconductor structure is transferred onto the surface of the substrate covered with the thin amorphous or poly-crystalline semiconductor film. Use of a single crystalline semiconductor structure having one long lateral dimension is preferred for some applications of this method. The present invention also includes methods wherein the printable semiconductor element comprising a single crys-

talline semiconductor structure is transferred onto the substrate surface prior to deposition of the amorphous or poly-crystalline semiconductor thin film.

As shown in FIG. 18H(2), the thin amorphous or polycrystalline semiconductor film is annealed while in contact with the single crystalline semiconductor structure, for example by annealing at high temperatures such as temperatures greater than 1000 degrees Celsius. In this embodiment of the present invention, the single crystalline semiconductor structure acts as a seed promoting a phase transition throughout the thin film from an amorphous or polycrystalline state to a well organized single crystalline state. As shown in FIG. 18H(2), the phase transition follows a front of a high temperature gradient which moves across the entire surface of the wafer. Different high temperature furnaces or focused optical systems may be used to produce the temperature gradient necessary to obtain an efficient phase conversion of the semiconductor thin film. An advantage of this process is that it may significantly reduce the cost of producing single crystalline semiconductor thin films, such as single crystalline silicon or germanium films.

FIG. 18I shows an exemplary method of fabricating printable semiconductor elements comprising micro-wires from GaAs substrate. As shown in this figure, the exposed surface of the GaAs substrate is patterned with mask material, such as photoresist. Patterning may be achieved by microcontact or nanocontact printing or via conventional photolithography, as shown in FIG. 18E. The patterned surface is anisotropically etched using wet etching methods. In the example method shown, re-entrant profiles of side walls are obtained using a  $H_3PO_4$ — $H_2O_2$ — $H_2O$  solution, and the relief features formed are etched until they are released from the GaAs substrate, thereby generating GaAs micro-wires. As shown, the photoresist layer may be removed by washing with acetone and exposure to  $O_2$  reactive ion etching. An advantage of this technique is that the GaAs substrate may be reused after planarization (ECMP). This technique may also be used to fabricate micro-wires from an InP substrate.

FIG. 18J shows an alternative method for fabricating printable semiconductor elements comprising single crystalline silicon ribbons. The starting material in this method is a Si (110) wafer. As shown in FIG. 18J, an exterior surface of the Si (110) wafer is selected patterned with thin films of  $SiO_2$  which serves as a mask during processing. This masking step defines shape and some of the physical dimensions (e.g. length and width for a ribbon) of the printable semiconductor elements to be fabricated. The exposed (i.e. unmasked) surface of the Si (110) wafer is then isotropically etched by either dry or wet chemical etching methods. This processing step generates relief features of silicon, preferably having smooth side walls separated by a series of trench have a selected depth. The silicon relief features are then released from the Si (110) wafer by isotropic etching and liftoff processing, thereby generating printable semiconductor elements. Optionally, source electrode, gain electrode, gate electrode, dielectric element or any combinations of these may be integrated into the semiconductor element prior to lift off. An advantage of this fabrication method is that the mother substrate can be cleaned and re-used. FIG. 18J also shows SET micrographs of Si (110) at various points in the processing method.

FIG. 18K shows an alternative method for fabricating printable semiconductor elements comprising single crystalline silicon ribbons. The starting material in this method is a Si (111) wafer. The Si (111) wafer is selective isotropically etched for example using a combination of conven-

tional photolithography masking and wet etching methods. This processing step generates relief features of silicon. As shown in FIG. 18K, the side walls, surface or both of the silicon relief features are coated using a passivation process. Printable single crystalline silicon ribbons are released from the Si (111) wafer by isotropic etching and liftoff processing. FIG. 18J also shows SET micrograph of single crystalline silicon ribbons generated by this method just prior to liftoff.

Example 4: Methods of Making Semiconductor Nanowires and Microwires

It is a goal of the present invention to provide methods of making semiconductor nanowires and microwires having good mechanical and electrical properties allowing for their use in a wide variety of devices, device components and device settings. It is further a goal of the present invention to provide methods of assembling nanowires and microwires to construct selected single layer structures, multilayer structures and functional devices comprising these elements. To assess the utility of the methods of the present invention, nanowires and microwires of GaAs and InP were fabricated and evaluated with respect to their electrical conductivity and mechanical flexibility in a range of device configurations. In addition, the ability of the present methods to assemble large numbers of nanowires and microwires in well defined positions and orientations corresponding to large substrate surface areas was evaluated by fabricating a number of complex nano/microwire assemblies comprising single layer structures and multilayer structures. The present methods of making and assembling GaAs and InP nanowires and microwires were demonstrated to provide excellent control over wire width, length and spatial orientation. In addition, the GaAs and InP nanowires and microwires fabricated exhibited good mechanical and electrical properties when integrated into microelectronic devices.

FIG. 19 provides a schematic diagram illustrating the steps of an exemplary method of generating and transferring nanowire arrays of GaAs to a substrate, such as plastic substrate comprising poly(ethylene terephthalate) (PET) sheet coated with a thin layer of cured polyurethane (PU). As shown in FIG. 19, the process begins with a piece of GaAs wafer with its surface oriented along the (100) direction (American Xtal Technology, Fremont, Calif.). Defining a etch mask of  $SiO_2$  in the form of lines oriented along the (0 T T) direction prepares the structure for anisotropic etching using an aqueous solution of  $H_3PO_4$  and  $H_2O_2$  comprising  $H_3PO_4$  (85 wt %):  $H_2O_2$  (30 wt %):  $H_2O$  = 1:13:12 in volume (step i in FIG. 19). This etching chemistry, when applied in this fashion, exhibits high anisotropy, thereby generating sharply defined reverse mesa-shaped profiles of GaAs under the  $SiO_2$  mask stripes. For sufficient etching times, the two side walls of each reverse mesa intersect, resulting in the formation of a wire with triangular cross section. This triangular cross section is exemplified in the top inset of panel A (left side) of FIG. 19.

In one embodiment, the patterned  $SiO_2$  lines are surrounded by bulk  $SiO_2$  film, which results in both ends of each GaAs wire being connected to the mother wafer. This connection confines the wires and preserves the spatial orientation and layout as defined by the pattern of  $SiO_2$ . FIG. 20A provides a scanning electron micrograph of free-standing GaAs wires obtained from GaAs wafer patterned with isolated  $SiO_2$  lines. It is worthy of note that lateral undercutting of GaAs occurs along with the vertical etching,

resulting in the ability to decrease the width of resultant GaAs wires down to nanometer scale even with SiO<sub>2</sub> lines that have micron widths.

GaAs wire arrays prepared by the present methods may be transfer printed to plastic sheets with retention of the orientation and relative position of individual wires in the array. In the embodiment illustrate in FIG. 19, a conformable elastomeric transfer element, such as a flat piece of poly(dimethylsiloxane), or PDMS, Sylgard 184, A/B=1:10, (Dow Corning), is placed on the GaAs wafer to pick up the wires (as shown in step ii of FIG. 19). In this embodiment, relatively strong bonding between PDMS sheet and the SiO<sub>2</sub> mask layer is required to break the crystalline connections to the underlying substrate at the ends of wires.

Cleaning the PDMS stamp and GaAs wafer having the SiO<sub>2</sub> mask with a weak oxygen plasma promotes formation of covalent siloxane (Si—O—Si) bonds between PDMS and SiO<sub>2</sub> by a condensation reaction (see the middle inset of FIG. 19). The present invention includes methods, therefore, wherein the elastomeric transfer element, semiconductor wafer having the SiO<sub>2</sub> mask or both are exposed to a weak oxygen plasma to provide effective and mechanically strong transfer of the semiconductor wafer having the SiO<sub>2</sub> mask to the elastomeric transfer element. The density of bonds over the interface is proportional to the number of —O<sub>n</sub>Si(OH)<sub>4-n</sub> on the PDMS surface, which is highly dependent on the intensity of oxygen plasma and the treatment time. Treatment with a strong plasma for a long time can induce bonding that is too strong to release the wires from PDMS to the desired plastic substrates. Controlled experiments indicate that the PDMS and SiO<sub>2</sub> coated GaAs wafer treated by the plasma generated from O<sub>2</sub> at pressure of 10 mTorr, flow rate of 10 sccm, and power intensity of 10 W (Uniaxis 790, Plasma-Therm Reactive Ion Etching System) for 3 and 60 s, respectively, generated the best results. In these embodiments, the interaction between the e-beam evaporated SiO<sub>2</sub> mask layer and GaAs is strong enough to prevent delamination during the transfer process. Peeling the PDMS stamp away from the GaAs substrate after leaving it in contact with the GaAs wafer having the SiO<sub>2</sub> mask for ~2 hrs lifts off all of the wires (as illustrated in step iii of FIG. 19).

The present methods make the fabrication and assembly of large numbers of nanowires and/or microwires practically feasible. For example, the GaAs wafer after the transfer step (step iii of FIG. 19) can be polished to regenerate a flat surface for another run of wire fabrication (step iv of FIG. 19). The combination of wafer polishing with wire fabrication as described above makes it possible to generate a huge number of GaAs wires from a single piece of wafer. For example, one piece of GaAs wafer with diameter of 10 cm and thickness of 450 μm (commercially available from American Xtal Technology) can generate enough wires (~2.2 billions wires with widths of ~400 nm and lengths of 100 μm) to densely cover the entire surface of a plastic substrate with an area of 1.76 m<sup>2</sup> if one cycle of anisotropic etching and polishing consumes 2 μm GaAs in thickness. These conditions are typical of the results described in the present example. Accordingly, such repetitive application of wire fabrication followed by wafer polishing steps enables highly cost effective use of the bulk wafers.

As shown in steps v and vi of FIG. 19, the GaAs wires having SiO<sub>2</sub> mask elements can be effectively transferred to a substrate, such as a plastic substrate having an adhesive layer on its outer surface. In one embodiment, the PDMS stamp with bonded GaAs wires is exposed to ambient environment for one day or rinsed it with ethanol to recon-

stitute the PDMS surface to its native, hydrophobic status. This hydrophobic property of the PDMS surface substantially prevents the PDMS from strongly interacting with adhesives that are normally hydrophilic. When the recovered PDMS stamp is placed against an adhesive layer, such as a PU layer (obtained from Nolarland products, Cranbury, N.J.) spin-coated onto a plastic substrate (e.g., PET of ~175 μm in thickness, Mylar film, Southwall Technologies, Palo Alto, Calif.), only the GaAs wires attached to SiO<sub>2</sub> mask stripes are wettable to the adhesive. The thickness of PU layer can be varied from 1 to tens of microns by controlling the spin speed. Illuminating the sample with an ultraviolet lamp (Model B 100 AP, Black-Ray, Upland, Calif.) for 1 hr cures the PU layer and forms a strong bond between the cured PU and the GaAs wires and SiO<sub>2</sub> mask stripes and between the cured PU and the underlying PET sheet (step v in FIG. 19). Peeling away the PDMS stamp leaves the GaAs wires and SiO<sub>2</sub> stripes embedded in the matrix of cured PU with preservation of order and crystallographic orientation similar to those of wires prior to lift-off (step vi in FIG. 19). The separation of SiO<sub>2</sub> from PDMS stamp is enabled by two effects: i) moderate adhesion strength associated with sparse siloxane bonds at the interface between PDMS and SiO<sub>2</sub> which further weaken during the process of reconstituting PMDS surface; and ii) ultra-thin layer of SiO<sub>2</sub> (with thickness of several nanometers) that remains on the PDMS after cohesive failure of the SiO<sub>2</sub>, which can be amorphous, incompact and fragile. Immersing the plastic sheet in a solution of buffered oxide etchant (BOE, NH<sub>4</sub>F (40 wt %):HF (49 wt %)=10:1) for 15 min removes the SiO<sub>2</sub> mask stripes, leaving the clean (100) top surfaces of the GaAs nanowires (step vii of FIG. 19) facing out.

This simple ‘top down’ approach to the fabrication and dry printing of GaAs wire arrays offers many advantages. For example, the geometries (i.e., length, width and shape) of the wires and their spatial organization can be defined by the initial lithographic step to satisfy the design of the desired electronic or optical end application. The transfer printing technique can generate yield as high as 100% with preservation of the patterns defined by the lithography. The well oriented crystallographic facets of the transferred wires (i.e., the top (100) surface) on plastic substrates provide an extremely flat top surface (having a flatness similar to that of original wafer), which is very useful for device fabrication. Furthermore, the SiO<sub>2</sub> mask stripes prevent the top surfaces of GaAs wires from becoming contaminated by organics, such as PDMS, PU and solvents used in the processing. Embedding the GaAs wires in cured PU immobilizes them, thereby preventing them from moving in lateral or vertical directions, especially when the plastic substrates are bent or twisted. It is important to note that PU and PET are only examples of materials usable in the present invention. Accordingly, it will be understood by persons skilled in that art that other adhesives, for example NEA 155 (Norland®) and other types of plastic sheets, for example Kapton® or polyimide film, can be used in the methods of the present invention.

Unlike ‘bottom up’ approaches of the prior art, the ‘top down’ processes of the present invention can generate GaAs nanowires with uniform lengths from several microns up to tens of centimeters (i.e., the diameter of original wafers). FIG. 20A shows an SEM image of free-standing GaAs nanowires with widths of ~400 nm and lengths of 2 cm which were randomly assembled on a mother wafer. The long nanowires formed curved structures during drying process, indicating the high degree of flexibility that is afforded by their narrow widths. As shown in the lower inset

of FIG. 20A, the circled nanowire has a bend radius as small as ~20  $\mu\text{m}$ , which suggests that nanowires with width of ~400 nm could withstand strain of ~1.3%. The upper inset in FIG. 20A provides a scanning electron micrograph image of the cross section before a nanowire lift off, which clearly shows formation of inverse mesa profiles of GaAs and undercutting from anisotropic etching.

In one aspect of the present invention, the width of the GaAs wires is controlled by selectively adjusting the width of  $\text{SiO}_2$  mask lines, selectively adjusting the etching time or both. Widths between hundreds of microns and tens of nanometers are attainable using the present methods. Controlling etching time provides an easy way to generate nanowires from  $\text{SiO}_2$  patterns having micron widths. FIGS. 20B-E show scanning electron micrograph images of individual wires obtained by etching the GaAs wafer patterned with 2  $\mu\text{m}$  wide  $\text{SiO}_2$  lines. The wires were transferred to a PDMS surface using the procedures described above to measure precisely the average width of their top surfaces (referred to as  $\bar{w}_{\text{wires}}$ ). FIG. 20F provides a plot showing the dependence of the average width,  $\bar{w}_{\text{wires}}$ , of the top surfaces of wires fabricated by the present methods on etching time. This plot indicates that GaAs wires with widths down to 50 nm can be obtained using this embodiment of the present methods. The linear relationship between width and etching time is consistent with previous studies on etching kinetics of GaAs in  $\text{H}_3\text{PO}_4$ — $\text{H}_2\text{O}_2$ — $\text{H}_2\text{O}$  solution, i.e., the etching rate was proportional to etching time when the molar ratio between  $\text{H}_2\text{O}_2$  and  $\text{H}_3\text{PO}_4$  ( $n_{\text{H}_2\text{O}_2}/n_{\text{H}_3\text{PO}_4}$ ) was larger than 2.3 and the molar fraction of  $\text{H}_2\text{O}$  ( $r_{\text{H}_2\text{O}}$ ) was equal to or less than 0.9 ( $n_{\text{H}_2\text{O}_2}/n_{\text{H}_3\text{PO}_4}$  and  $r_{\text{H}_2\text{O}}$  of the etchant used in our experiments were 7.8 and 0.9, respectively). The statistical results show that the distributions of the widths of the wires (as determined by averaging along their lengths) was <9% for wires with widths of ~50 nm, which is somewhat narrower than the >14% variation in one type of ‘bottom up’ nanowires that has been reported to provide average widths of ~16.8 nm.

The scanning electron micrograph images shown in FIGS. 20B-D also show that the triangular cross sections of the wires is preserved during the thinning process, indicating the etching is highly anisotropic even for the free-standing GaAs wires. Close observations of the wires show that there is some roughness on their side walls. Much of this roughness comes directly from the lithographic procedures used to define the  $\text{SiO}_2$  mask stripes; some is induced by the misalignment of mask lines and etching itself. This roughness determines the width of the smallest continuous wires that we could obtain using this embodiment of the present invention. As shown in FIG. 20F, the ratio between the width variation along individual wires and average wire width ( $\sigma/\bar{w}$ ) was also highly dependent on the etching time. Continuous GaAs nanowires can be prepared when the ratio was less than 100%. The curve provided in FIG. 20F indicates that the width of nanowires obtained from application of this embodiment of the present invention can be decreased down to ~40 nm. Nanowires with different average widths exhibited essentially the same width variation along individual wires (i.e., ~40 nm), which was close to the width variation along individual  $\text{SiO}_2$  mask lines (i.e., ~36 nm). This comparison confirms that the roughness of wire side walls is mainly initiated by the rough edges of  $\text{SiO}_2$  mask stripes regardless of etching times. Accordingly, use of lithographic procedures that reduce the roughness of the mask stripes reduces the roughness on the edges of the wires. It is important to note that the transfer printing process described in this example exposes the pristine, ultraflat unetched top

surface of the wires for electrical connection and device fabrication on the final substrate (i.e. the PET of FIG. 19).

FIGS. 21A-G shows images of a variety of GaAs wire arrays printed on PDMS and PU/PET substrates. The wires in this case have widths of ~400 nm and lengths of ~100  $\mu\text{m}$ . The corresponding  $\text{SiO}_2$  mask lines had widths of 2  $\mu\text{m}$  and lengths of 100  $\mu\text{m}$  oriented along the (0 T T) direction on the (100) GaAs wafers. FIG. 21A is a scanning electron micrograph image taken from an GaAs wire array bonded to a flat 10 PDMS stamp via the  $\text{SiO}_2$  mask layer, indicating that the order of wires was preserved. The inset of FIG. 21A shows the ends of three wires with relatively higher magnification, clearly revealing the breakage at their ends. As shown in 15 FIG. 21B, peeling the PDMS stamp away from the cured PU left a smooth surface (as smooth as that of the PDMS) with the  $\text{SiO}_2$  mask stripes facing out. As shown in FIG. 21C, etching away the  $\text{SiO}_2$  layers with BOE exposes the pristine 20 top surfaces of GaAs wires. FIG. 21D presents an optical image collected from a PU/PET substrate with embedded 25 GaAs wires, indicating that large-area of wire arrays can be routinely printed on the PU/PET substrate using the method illustrated FIG. 19. GaAs wire arrays with other patterns (e.g., patches consisting of wires with different lengths) can also be transferred to PU/PET substrates.

The transfer process is repeated to print multiple layers of 30 GaAs wire arrays on the same PET substrate by spin-coating a new layer of PU. These methods provide important pathways to generating multilayer structures comprising 35 nanowires and/or microwires. FIGS. 21E and 21F give typical images of multilayer structures having double layers of GaAs wire arrays. In one embodiment, such multilayer structures are obtained by rotating the second layer with 40 different angles (~90° and ~45° for E and F, respectively) relative to the first layer. FIG. 21G provide images of 45 PU/PET substrates having three layers of GaAs wire array obtained by repeating the printing process on samples shown in FIGS. 21E and 21F. The thickness of the PU layer, which can be controlled by tuning the spin speed, controls the 50 spacing between the wire arrays. This type of multilayer capability does not, of course, require any form of epitaxial growth, and the PU insulates the arrays in different levels. This fabrication capability is useful for a large number of 55 device fabrication applications.

The wire fabrication and printing techniques of the present invention can be used to generate wire arrays of other 60 semiconductor materials on plastic substrates by using suitable anisotropic etchants. For example, InP wires with triangular cross sections are fabricated by etching an (100) InP wafer having  $\text{SiO}_2$  mask lines along (0 T T) direction in a 1% (v/v) methanol solution of  $\text{Br}_2$ . FIGS. 22A-C shows scanning electron micrograph images of an InP wire array on PMDS and PU/PET substrates. These wires were fabricated from an InP wafer patterned with  $\text{SiO}_2$  lines of 50  $\mu\text{m}$  in 65 length and 2  $\mu\text{m}$  in width. The wires shown have lengths and widths of ~35  $\mu\text{m}$  and ~1.7  $\mu\text{m}$ , respectively. The etching behavior of InP in methanol solution of  $\text{Br}_2$  is significantly 70 different from that of GaAs in aqueous solution of  $\text{H}_3\text{PO}_4$ — $\text{H}_2\text{O}_2$  in terms of profile of wire ends and lateral undercutting. For example, the etching process disconnected all the 75 ends of InP wires from the mother wafer even with an etch mask that was similar to the one used in fabrication of GaAs wires (FIG. 21). Furthermore, the degree of undercutting in InP is less than that in GaAs, indicating that InP wires with 80 small widths (less than 500 nm) can be more easily prepared by using narrow  $\text{SiO}_2$  stripes rather than by controlling the etching time.

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The mechanical flexibility of a simple two terminal diode device made with GaAs wire arrays (same as those shown in FIG. 21 which were fabricated from Si-doped n-GaAs wafer with carrier density of  $1.1\text{-}5.6 \times 10^{17} \text{ cm}^{-3}$ ) on a PU/PET substrate was evaluated by measuring the electrical properties as a function of bend radius. The structures were fabricated with GaAs wire arrays defined according to the methods of FIG. 19. Photolithography and metal deposition defined on these wires two Schottky contacts made of Ti/Au (5 nm/150 nm) and separated by 10  $\mu\text{m}$ . FIG. 23A provides a schematic diagram and image of an exemplary two terminal diode device comprising GaAs wire arrays. Dipping the substrate into a concentrated HCl solution for 10 min removed the native oxide layers on the surfaces of GaAs wires just before deposition of electrodes.

FIG. 23B shows the current-voltage (I-V) curves recorded at different bend radii. These curves all exhibit expected diode characteristics. The small differences among these curves suggest that almost no GaAs nanowires were broken even when the bend radius ( $R$ ) of substrate was 0.95 cm. The strain on the PET surface in this case was  $\sim 0.92\%$ , which is less than that estimated to exist in the free-standing GaAs nanowire shown in the inset of FIG. 20A. These results further confirm that GaAs nanowires generated by the present ‘top down’ fabrication methods are flexible and are able to be integrated with bendable plastic sheets. We note that the data show that when the substrate was relaxed after first bending it, the current was  $\sim 40\%$  smaller than that recorded from original device before bending. FIG. 23C shows the current-voltage (I-V) curves measured for the two terminal diode device after relaxation after bending at different bend radii. For the sake of comparison, the black curve in FIG. 23C shows the current-voltage curve corresponding to the device configuration prior to bending. The lack of variation in the I-V characteristics with bend radius and with multiple bending/unbending cycles after the first one suggest, however, that the one-time decrease in current might be caused by an initial variation in the properties at the interface between the electrodes and the wires.

The combined use of traditional photolithography and anisotropic chemical etching with bulk high quality single crystal wafers of these materials forms an attractive ‘top down’ route to micro and nanowires of GaAs and InP with triangular cross sections. The dimensions of the wires and their organization are selectively adjustable by appropriate selection of the lithography and etching conditions, for example etching time. The as-obtained wire arrays on the mother substrates are able to be effectively transfer printed with high fidelity to plastic substrates coated with a thin layer of adhesive in which the wires are embedded. The mother wafer is able to be re-used after polishing, which enables large numbers of wires to be generated from a single wafer. This “dry” transfer printing of ‘top down’ nanowires/micron wires represents a new class of transfer processes that offer many advantages over “wet” assembly of ‘bottom up’ nanowires in terms of preservation of order and crystallographic orientation of the wires as well the purity of their active surfaces. For macroelectronics applications in particular, where wires wider than 100-200 nm are useful, the “top down” fabrication methods of the present invention has many attractive features. The systems of wires on plastic substrates demonstrated here illustrate excellent bendability and significant potential for use in this class of application.

#### Example 5: Solution Printing Methods for Printable Semiconductor Elements

The present invention provides solution printing methods capable of transferring and assembling printable semicon-

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ductor elements over large areas of many substrates. This aspect of the present invention provides continuous, high speed fabrication methods applicable to a wide range of semiconductor devices and device components.

- 5 In one method of this aspect of the present invention, a printable semiconductor element is provided having a handle element. In the context of this description, the term “handle element” refers to a component that allows for controlled manipulation of the position and/or orientation of
- 10 a printable semiconductor element after solution phase delivery to a substrate surface. In one embodiment, a semiconductor element is provided having one or more handle elements each comprising a layer of material that is responsive to a magnetic field, electric field, or both. This aspect of
- 15 the present invention is useful for providing methods of aligning, positioning and/or orienting printable semiconductor elements on substrate surfaces using electrostatic forces, and/or magnetostatic forces. Alternatively, the present invention provides methods wherein a semiconductor ele-
- 20 ment is provided having one or more handle elements each comprising a layer of material that is responsive to laser induced momentum transfer processes. This aspect of the present invention is useful for providing methods of aligning, positioning and/or orienting printable semiconductor
- 25 elements on substrate surfaces by exposing the printable semiconductor element having one or more handle elements to a series of laser pulses (e.g. laser tweezers methods). Alternatively, the present invention provides methods wherein a semiconductor element is provided having one or
- 30 more handle elements each comprising a droplet that is response to forces generated by capillary action. The present invention includes methods and devices using printable semiconductor elements having one or more handle elements or one or more different types of handle element, such
- 35 as handle elements responsive to different types of fields. Handle elements may be provide in many types of printable semiconductor elements of the present invention including, but not limited to, microstructures, nanostructures, microwires, nanowires, microribbons and nanoribbons.
- 40 In this aspect of the present invention, one or more printable semiconductor elements each having one or more handle elements are dispersed into a solution or carrier fluid and delivered to a substrate surface. Delivery of the mixture of printable semiconductor elements and solution/carrier
- 45 fluid distributes the printable semiconductor elements randomly about the substrate surface. Next, the semiconductor elements randomly distributed on the substrate surface are concertedly moved into selected positions and orientations on the substrate surface by application of forces arising from
- 50 the presence of handle elements of the printable semiconductor elements. This aspect of the present invention is useful for aligning printable semiconductor elements having handle elements into well order arrays or into positions and orientations corresponding to a selected device or device component configuration. For example, printable semiconductor elements having one or more handle elements comprising a layer of magnetic material may be moved into selected positions and orientations on a substrate surface by application of a magnetic field having appropriate distributions of intensities and directions. In this embodiment, a magnetic field having selected distributions of intensities and directions may be applied by positioning one or more ferromagnetic elements or electromagnetic elements proximate to the substrate (such as positioned behind the substrate
- 55 surface, above the substrate surface and/or along side the substrate), thereby generating selected distributions of intensities and directions which correspond to a desired assembly,
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- 65

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pattern or structure of printable semiconductor elements or a selected device or device component configuration. In this aspect of the present invention, solvent, carrier fluid or both may be removed before, during or after selective positioning and orientation of printable semiconductor elements via manipulation of handle elements by any means known in the art, including by evaporation or by desorption methods.

FIG. 24 provides a schematic diagram illustrating an exemplary method of the present invention for solution printing printable semiconductor elements having handle elements comprising magnetic tags. As shown in FIG. 24, printable semiconductor elements are provided, each of which have a plurality of magnetic tags comprising thin nickel layers. In one embodiment, thin nickel layers are provided on the surface of a microsized or nanosized semiconductor structure. The use of nickel for handle elements in this example is only by way of example and any crystalline or amorphous ferromagnetic material may be used in these methods, including but not limited to, Co, Fe, Gd, Dy, MnAs, MnBi, MnSb, CrO<sub>2</sub>, MnOFe<sub>2</sub>O<sub>3</sub>, NiOFe<sub>2</sub>O<sub>3</sub>, CuOFe<sub>2</sub>O<sub>3</sub>, MgOFe<sub>2</sub>O<sub>3</sub> and amorphous ferrromagnetic alloys such as transition metal-metallloid alloys.

As shown in step I of the schematic diagram in FIG. 24, a plurality of printable semiconductor elements each having handle elements are dispersed into solution and cast onto the surface of a substrate. This step provides the printable semiconductor elements to the substrate surface in a random distribution of positions and orientations. As shown in step II of the schematic diagram in FIG. 24, a magnetic field is then applied to the printable semiconductor elements, preferably a magnetic field having selected distributions of intensities and directions. In the schematic shown in FIG. 24, a magnetic field having selected distributions of intensities and directions is applied by positioning the magnetic poles of one or more magnets on opposite sides of the substrate surface having printable semiconductors thereon. As a ferromagnetic material, interaction of the magnetic field and the nickel layers comprising the handle elements generates forces which move the printable semiconductors into desired positions and orientations on the substrate surface. In the embodiment shown in FIG. 24, a magnetic field is applied that orients the printable semiconductor elements into a well ordered array characterized by a substantially parallel alignment of the long sides of the printable semiconductor elements. As shown in step III of the schematic diagram in FIG. 24, electrical connections can be deposited on the ends of printable semiconductor elements comprising the ordered array in a manner establishing an electric connection and in a manner preserving the orientations prepared by application of the magnetic field.

FIG. 25 provides several optical images demonstrating the use of solution printing methods of the present invention to generate well order arrays of microstructures comprising printable semiconductor elements having handle elements comprising thin nickel layers. The optical images presented in the panels on the left of FIG. 25 correspond to a substrate surface having printable semiconductors dispersed on a substrate surface without the application of a magnetic field. As shown in these images, the printable semiconductor elements are randomly distributed on the substrate surface. The optical images presented in the panels on the right of FIG. 25 correspond to a substrate surface having printable semiconductors dispersed on a substrate surface upon the application of a magnetic field. In contrast to the images presented in the left panels, the optical images corresponding to conditions wherein a magnetic field is applied show that the printable semiconductor elements are provided in

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selected orientations and positions corresponding to a well ordered array. Comparison of the images presented in the left panels and right panels of FIG. 25 indicate that application of a magnetic field having selected distributions of intensities and directions is capable of generating forces that move individual printable semiconductor elements into selected positions and orientations.

As will be understood by persons of skill in the art of device fabrication, the positions and orientations of printable semiconductor elements in the right panels of FIG. 25 are but one example of orientations and positions achievable using the solution printing methods of the present invention. Selection of appropriate positions of handle elements on printable semiconductor elements and selection of appropriate magnetic fields having selected distributions of intensities and directions may be used to generate virtually any distribution of semiconductor element positions and orientations.

#### Example 6: Fabrication of High Performance Single Crystal Silicon Transistors on Flexible Plastic Substrates

It is a goal of the present invention to provide bendable macroelectronic, microelectronic and/or nanoelectronic devices and device components comprising printable, high quality semiconductor elements assembled on flexible substrates. In addition, it is a goal of the present invention to provide bendable electronic devices, such as bendable thin film transistors that exhibit field effect mobilities, on-off ratios and threshold voltages similar to or exceeding that of thin film transistors fabricated by convention high temperature processing methods. Finally, it is a goal of the present invention to provide bendable electronic devices compatible with efficient high throughput processing on large areas of flexible substrates at lower temperatures, such as room temperature processing on plastic substrates.

The ability of the present methods, devices and compositions to provide useful macroelectronic and/or microelectronic devices and device components exhibiting high device performance characterizing in bent and planar configurations was verified by experimental studies. The results of these measurements demonstrate that the present invention provides dry transfer contact printing techniques, exhibiting excellent registration capability, that are capable of assembling bendable thin film transistors by depositing a range of high quality semiconductors, including single crystal Si ribbons, Ga—As and InP wires and single-walled carbon nanotubes onto plastic substrates. For example, the results of these experimental studies indicate that bendable thin film type transistors comprising spatially well defined arrays of dry transferred printable single crystal silicon elements exhibit high device performance characteristics, such as average device effective mobilities, evaluated in the linear regime, of ~240 cm<sup>2</sup>/Vs, and threshold voltages near 0 V. Further, these studies show that the thin film transistors of the present invention exhibit bendability (i.e. strain at which failure occurs) comparable to devices made with organic semiconductors, and mechanical robustness and flexibility when subjected to frontward and backward bending.

High performance printed circuitry on large area flexible substrates represents a new form of electronics that has wide ranging applications in sensors, displays, medical devices and other areas. Fabricating the required transistors on plastic substrates represents a challenge to achieving these macroelectronic systems. Some approaches that have been

explored over the last several years are based on modified, low temperature versions of the types of process steps used to fabricate conventional silicon based thin film transistors (TFTs) on glass/quartz substrates. The high temperatures associated with the directional solidification processes developed for producing single-crystal silicon films (i.e., zone-melting recrystallization of Si films on  $\text{SiO}_2$  using a cw laser, a focused lamp, an electron beam, or a graphite-strip heater) make this approach unsuitable for use with plastic substrates. Laser based approaches have achieved some limited degree of success, although uniformity, throughput and use with low cost plastics poses significant continuing experimental challenges. Direct full wafer transfer of pre-formed circuits onto plastic substrates yield some useful devices, but this approach is difficult to scale to large areas and it does not retain printing type fabrication sequences that might be important for low cost, large area macroelectronics. Organic semiconductor materials provide an alternative pathway to flexible electronics; wherein the organic based electronic materials can be naturally integrated, via room temperature deposition, with a range of plastic substrates. The organic semiconductors materials currently known, however, enable only modest device mobilities. For example, even high quality single crystals of these materials have mobilities in the range of  $1\text{-}2 \text{ cm}^2/\text{Vs}$  and  $\sim 10\text{-}20 \text{ cm}^2/\text{Vs}$  for n and p-type devices, respectively.

Other fabrication techniques such as fluidic self assembly separate the high temperature steps for producing high mobility materials from the low temperature processing that is required for building devices on plastic substrates. These methods do not, however, allow efficient control of the organization or location of the deposited objects.

FIG. 26A illustrates the steps used to fabricate exemplary bendable thin film transistors devices of the present invention. First, photolithography defined a pattern of photoresist on the surface of a silicon-on-insulator wafer (Soitec unibond SOI with a 100 nm top Si layer and 145 nm buried oxide). This resist served as a mask for dry etching the top silicon layer of the SOI wafer with a  $\text{SF}_6$  plasma (Plasmatherm RIE system, 40 sccm  $\text{SF}_6$  flow with a chamber base pressure of 50 mTorr, 100 W RF power for 25 s). A concentrated HF solution etched the buried oxide and freed (but did not completely float off) the printable single crystal silicon semiconductor elements from their substrate. A flat piece of poly(dimethylsiloxane) (PDMS) was brought into conformal contact with the top surface of the wafer and then carefully peeled back to pickup the interconnected array of ribbons. The interaction between the photoresist and the PDMS was sufficient to bond the two together for removal, with good efficiency.

An Indium-Tin-Oxide (ITO; thickness  $\sim 100 \text{ nm}$ ) coated poly(ethyleneteraphthalate) (PET; thickness  $\sim 180 \mu\text{m}$ ) plastic sheet served as the device substrate. Washing it with acetone & isopropanol, rinsing it with deionized water and then drying it with a stream of nitrogen cleaned its surface. Treating the ITO with a short oxygen plasma (Plasmatherm RIE system, 20 sccm  $\text{O}_2$  flow with a chamber base pressure of 100 mTorr, 50 W RF power for 10 s) promotes adhesion between it and a spin cast dielectric layer of epoxy (3000 RPM for 30 s of Microchem SU8-5 diluted with 66% of SU8-2000 thinner). This photo sensitive epoxy was pre-cured at  $50^\circ\text{C}$ . on a hot plate during  $\sim 1 \text{ min}$ . Bringing the PDMS with a printable single crystal silicon semiconductor element on its surface into contact with the warm epoxy layer and then peeling back the PDMS led to the transfer of the printable single crystal silicon semiconductor element to the epoxy. This result suggests that the bonding forces

between the silicon and the soft epoxy layer (some of which are mechanical, due to the flow of epoxy around the edges of the printable single crystal silicon semiconductor elements) are stronger than those between the photoresist and the PDMS stamp. The epoxy layer was fully cured at  $100^\circ\text{C}$ . for 5 min, exposed to UV light from the back side of the transparent substrate for 10 s and then post baked at  $115^\circ\text{C}$ . for 5 min to crosslink the polymer. The photoresist mask (which, conveniently, prevents contamination of the top surface of the printable single crystal silicon semiconductor elements during the transfer steps) was dissolved with acetone and the sample was then abundantly rinsed with deionized water.

Source and drain electrodes were formed with Ti ( $\sim 70 \text{ nm}$ ; Temescal e-beam evaporator) deposited on the top surface of the printable single crystal silicon semiconductor elements. Etching (1:1:10 HF: $\text{H}_2\text{O}_2$ :DI for  $\sim 2 \text{ s}$ ) through a photoresist mask (Shipley S1818) patterned on the Ti defined the geometry of these electrodes. The last step of the fabrication involved dry etching ( $\text{SF}_6$  using the RIE parameters given above) through a photoresist mask to define islands of silicon at the locations of the devices. FIG. 26B presents a schematic illustration of the bottom gate device configuration of the thin film transistor together with high and low magnification optical images of part of the device array.

FIG. 27A presents current voltage characteristics of a bendable thin film transistor of the present invention that shows an effective device mobility of  $140 \text{ cm}^2/\text{Vs}$  in the saturation regime and  $260 \text{ cm}^2/\text{Vs}$  in the linear regime, as evaluated by application of standard field effect transistor models that ignore the effects of contacts. The high resistance ( $\sim 90 \Omega\text{cm}$ ) of the Schottky contacts in these devices, however, has a significant effect on the device response. FIG. 27B presents transfer characteristics of several devices, plotted on linear (left axis) and logarithmic (right axis) scales. The plot in the inset shows that the threshold voltages have a narrow distribution near 0 V. Small ( $<4\%$  in current for a  $\pm 10 \text{ V}$  cycle) hysteresis in the transfer characteristics indicates a low density of trapped charge at the interface between the silicon (with native oxide) and the epoxy dielectric. The small values ( $\leq 13 \text{ V}\cdot\text{nF}/\text{dec}\cdot\text{cm}^2$ ) of the normalized subthreshold slopes confirm the good quality of this interface, which may be governed primarily by the interface between the silicon and its native oxide. FIG. 27C shows the distribution of the linear effective mobilities of several bendable thin film transistors fabricate by the present methods. A Gaussian fit indicates a center value of  $240 \text{ cm}^2/\text{Vs}$  with a standard deviation of  $30 \text{ cm}^2/\text{Vs}$ . Some of the low values are associated with visible defects in the electrodes or other components of the devices. The uniformity of the epoxy dielectric was investigated by building, using the same substrate and methods used to prepare the transistor gate dielectric, an array of 256 ( $200\times 200 \mu\text{m}$ ) square capacitors. The inset in FIG. 27C shows the measured capacitance values. A Gaussian fit indicates a standard deviation lower than 2% confirming the excellent electrical and physical properties uniformity of the epoxy layer. Capacitance measurements carried out at various frequencies (between 1 kHz and 1 MHz) indicated a small ( $<3\%$ ) frequency-dependence of the dielectric constant.

The mechanical flexibility and robustness of the bendable thin film transistors of the present invention were investigated by performing frontward and backward bending tests. FIG. 28A presents a high-resolution scanning electron micrograph of solution cast ribbons (left inset) illustrating the remarkable flexibility of the printable single crystal

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silicon semiconductor elements. The right inset in FIG. 28A shows a picture of the experimental setup used to bend the bendable thin film transistors evaluated in this study. To maximize the strain induced in the thin film transistors when the plastic sheet is bent, a relatively thick (~180  $\mu\text{m}$ ) plastic substrate was used in these studies. FIG. 28B shows the small (~<1%) linear variation of the epoxy dielectric capacitance when subject to tensile and compressive strains (see top inset). The bending radius and strain values were computed using a finite element model of the buckling sheet. Comparisons of the bending profiles of the buckling sheet (for several bending radius) to the profiles obtained with the finite element method confirmed the accuracy of the simulations. The lower inset in FIG. 28B presents the variation of the saturation current of a device measured for a gate and drain bias voltages of both 4 V. The maximum value of the tensile strain at which the bendable thin film transistor can be operated seems to be limited by the failure of the ITO gate electrode (which fails a tensile strain value of ~-0.9%). The bendable thin film transistor operate well even at compressive strains as high as 1.4%. This level of bendability is comparable to that recently reported for organic transistors based on pentacene. Failure of the present bendable thin film transistors is likely to occur only at very high strains, as Takahiro et al. recently demonstrated that micron-sized single crystal silicon objects etched from the top layer of a SOI wafer can withstand remarkably high tensile stress (>6%) [T. Namazu, Y. Isom, and T. Tanaka J. MEMS 9, 450 (2000)]

The cause of the modest variation in output current with strain in our devices is not entirely known, as the known variation in mobility with strain contributes to, but does not fully account for, these changes. Devices of the type that we describe in this example enable new opportunities to investigate the charge transport in mechanically strained silicon at strain values not easily reached when bulk Si wafers are bent.

In summary, this Example demonstrates the high device performance and beneficial mechanical properties of bendable single crystal silicon transistors formed on plastic substrates by the simple and efficient parallel printing process for silicon provided by the present invention. To the best of our knowledge, the performance of these devices exceeds that of the best devices (silicon based or otherwise) exhibiting a similar degree of mechanical bendability. The top down control over the shapes, physical dimensions and composition (e.g. doped or not doped) of the printable silicon semiconductor elements, and the printing technique provide significant advantages compared to other approaches. In addition, the mechanical flexibility of the resulting devices is excellent. Further, these same general approaches are applicable to other inorganic semiconductors (e.g. GaAs, GaN, etc.) and can be used to fabricate a wide range of flexible microelectronic and macroelectronic devices and device components, such as solar cells, diodes, light emitting diodes, complementary logic circuits, information storage devices, bipolar junction transistors, and FET transistors. Therefore, the methods and device of the present invention are useful for an enormous range of fabrication applications for making flexible electronic products.

**Example 7: Printable Heterogeneous Semiconductor Elements and Devices Comprising Printable Heterogeneous Semiconductor Elements**

The present invention provides heterogeneous printable semiconductor elements comprising multimaterial elements,

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and related devices and device components. Printable heterogeneous semiconductor elements of this example comprise a semiconductor layer having a dopant with a selected spatial distribution, and provide enhanced functionality in a range of macroelectronic, microelectronic and/or nanoelectronic devices.

The ability of the present methods to fabricate heterogeneous printable semiconductor elements exhibiting useful electronic properties was verified by experimental studies. In addition, the applicability of the present methods to assembling printable elements into functional devices was demonstrated by fabrication of flexible thin film transistors comprising printable single crystal silicon semiconductor elements having integrated doped regions for contacts.

Large area, mechanically flexible electronic systems, known as macroelectronics, are attractive for a range of applications in consumer electronics, sensors, medical devices and other areas. A variety of organic, inorganic and organic/inorganic hybrid materials have been explored as semiconductors for these systems. Use of the present “top-down” technology approach for generating single crystal silicon micro/nanoelements (wires, ribbons, platelets, etc, which are refer to collectively as printable silicon semiconductor elements) is an alternative approach that has been demonstrated as useful for fabricating high performance thin film transistors on flexible substrates. This fabrication approach has also been demonstrated as applicable to other important semiconductor materials, such as GaAs, InP, GaN, and carbon nanotubes.

An important characteristic of the present approach is its use of high quality, wafer-based sources of semiconductor materials, which are grown and processed separately from subsequent device assembly steps. Separate semiconductor processing and assembly steps allow for device assembly at relatively low temperatures (e.g. room temperature  $\pm 30$  degrees Celsius) compatible with most flexible device substrates, such as plastic substrates. The present invention includes methods wherein high quality semiconductors are not only grown, but are also processes in other ways in fabrication steps independent from subsequent fabrication steps involving assembly of printable semiconductor elements on flexible substrates. In one embodiment, the present invention includes methods wherein dopants are introduced into the semiconductor during high temperature processing, and the resulting doped semiconductor material is subsequently used to generate printable heterogeneous semiconductor elements which can be assembled into a variety of useful electronic devices. Processing steps useful in for doping semiconductors include high temperature processing and processing wherein dopants are introduced in a manner providing control over their spatial distribution in one two or three dimensions (i.e. control over the area of implantation and depth of implantation). In one method, the semiconductor is selectively contact doped by spin on doping procedures performed at the wafer fabrication level in steps that are performed independently from the low temperature substrates. Contact doping provides precise control over the spatial distribution of dopant in the semiconductor material and, therefore, subsequent patterning and etching steps allow fabrication of high quality printable heterogeneous semiconductor elements having integrated doped regions. The solution printing and dry transfer contact printing methods are ideally suited for assembling these printable heterogeneous elements into devices, such as thin film transistors, exhibiting the excellent device performance and excellent bendability that can be achieved.

FIG. 29A presents a schematic representation of a fabrication process for generating transistors comprising printable heterogeneous semiconductor elements on a PET substrate. In this embodiment, the printable heterogeneous semiconductor element comprises crystal silicon with doped source (S) and drain (D) contacts. The approach illustrated in FIG. 29A uses a solution processable spin-on dopant (SOD) to dope selected regions of the top silicon layer of a silicon-on-insulator wafer (SOI; Soitec unibond with a 100 nm top Si layer and 200 nm buried oxide). Therefore, a spin-on dopant (SOD) provides the phosphorus dopant and a spin-on glass (SOG) serves as a mask to control where dopant diffuses into the silicon. This doped SOI provides the source of printable heterogeneous semiconductor elements.

To produce the printable heterogeneous semiconductor elements we first spin cast a spin-on glass (SOG) solution (Filmtronic) onto a SOI wafer and exposed it to rapid thermal annealing (RTA) at 700° C. for 4 minutes to form a uniform film (300 nm thickness). Etching (6:1 buffered oxide enhancet (BOE) for 50 seconds) through a lithographically patterned layer of photoresist (Shipley 1805) opened source and drain windows in the SOG. After stripping the resist, we uniformly deposited a phosphorous containing SOD (Filmtronic) by spin casting. RTA at 950° C. for 5 seconds caused the phosphorous from the SOD to diffuse through the lithographically defined openings in the SOG and into the underlying silicon. The SOG blocked diffusion in the other areas. The wafer was rapidly cooled to room temperature, immersed in BOE for 90 seconds to remove both the SOG and SOD and then thoroughly washed with DI water to complete the doping process.

The printable heterogeneous semiconductor elements were assembled onto plastic substrates of PET coated with indium tin oxide (ITO; 100 nm, gate electrode) and epoxy (SU8; 600 nm, gate dielectric) using the present methods. The epoxy not only provides the dielectric, but also facilitates the transfer printing of the printable heterogeneous semiconductor elements. Source and drain electrodes of Ti (100 nm) were formed on the doped contact regions by an aligned photolithography step followed by etch back. FIG. 29B shows optical images of several devices having heterogeneous printable semiconductor elements fabricated using the present techniques.

We estimated the doping levels and the contact resistances using a standard transfer line model (TLM). In particular, we measured resistances between Ti contact pads with separations (L) between 5 and 100 microns and widths (W) of 200 microns on printable heterogeneous semiconductor elements comprising uniformly doped crystalline silicon that were printed onto a plastic substrate were measured. The inset in FIG. 30A shows images of the arrangement of printable heterogeneous semiconductor elements and contact pads used to characterize the contact resistances. The linear current (I) vs. voltage curves (V) (not shown) indicate that the contacts are ohmic and that the doping level is high. The dependence of the resistance on L can be described by  $R_{total}=2R_c+(R_s/W)L$ , where  $R_{total}(=V/I)$  is the resistance between two contact pads,  $R_c$  is the contact resistance, and  $R_s$  is the sheet resistance. FIG. 30A shows a plot of the normalized resistance,  $R_{total}W$ , as a function of L. Linear fitting of  $R_{total}W$  gives  $R_s=228\pm 5 \Omega/\text{sq}$ , and  $R_cW=1.7\pm 0.05 \Omega\cdot\text{cm}$ . The value of normalized contact resistance  $R_cW$  is more than an order of magnitude lower than what we observed for undoped printable single crystal silicon semiconductor elements processed in a similar manner. The resistivity is about  $2.3\times 10^{-3} \Omega\cdot\text{cm}$ , which corresponds to a doping level of  $10^{19}/\text{cm}^3$  if we assume, for simplicity, that

the doping is uniform through the 100 nm doped printable silicon semiconductor element. FIG. 30B shows Time-of-Flight Secondary Ion Mass Spectroscopy (TOF-SIMS) measurements that show the use of patterned SOG as a diffusion barrier (See, Schematic in FIG. 29A) localizes the dopants to desired regions in the silicon. In the image shown in FIG. 30B, the bright red color indicates high phosphorous concentration.

FIGS. 31A-D shows measurements corresponding to transistors comprising printable contact doped silicon semiconductor elements on an epoxy/ITO/PET substrate. FIG. 31A plots the current-voltage characteristics of a device ( $L=7 \mu\text{m}$ ,  $W=200 \mu\text{m}$ ) of the present invention. The effective device mobility ( $\mu_{eff}$ ) is  $\sim 240 \text{ cm}^2/\text{Vs}$  in the linear regime and  $\sim 230 \text{ cm}^2/\text{Vs}$  in the saturation regime, as determined by application of standard field-effect transistor models. FIG. 31B shows transfer characteristics of devices of the present invention with channel lengths between  $2 \mu\text{m}$  and  $97 \mu\text{m}$  and channel widths of  $200 \mu\text{m}$ . The ON to OFF current ratios in all cases are  $\sim 10^4$ . The threshold voltages vary from  $\sim 2 \text{ V}$  to  $\sim 0 \text{ V}$ , monotonically from  $L=97 \mu\text{m}$  to  $2 \mu\text{m}$ . FIG. 31C presents the resistance of the devices measured in ON state ( $R_{on}$ ) at small drain voltages, and multiplied by W, as a function of L at different gate voltages. Linear fits of  $R_{on}W$  vs. L at each gate voltage provide information about both intrinsic device mobility and contact resistance. In this simple model,  $R_{on}$  consists of the series addition of the channel resistance (which is proportional to L) and the combined contact resistance  $R_c$  associated with the source and drain electrodes. FIG. 31C shows that  $R_c$ , as determined from the intercepts of linear fitting, is negligible compared to channel resistance for all channel lengths evaluated. The inset in FIG. 31C shows the variation of sheet conductance, as determined from the reciprocal of the slope of linear fitting in FIG. 31C, with gate voltage. The linear fit to these data, as shown in the inset of FIG. 31C, gives an intrinsic device mobility of  $\sim 270 \text{ cm}^2/\text{Vs}$ , and an intrinsic threshold voltage of  $\sim 2 \text{ V}$ .

FIG. 31D compares the effective mobilities,  $\mu_{eff}$ , of transistors having undoped and contact-doped printable single crystal silicon semiconductor elements evaluated directly from transfer characteristics measured in the linear regime (i.e. contact effects are not subtracted). For the undoped devices,  $\mu_{eff}$  decreases rapidly from  $200 \text{ cm}^2/\text{Vs}$  to  $50 \text{ cm}^2/\text{Vs}$  with decreasing the channel length L from 100 microns to 5 microns. The contacts begin to dominate device behavior at channel lengths below  $\sim 50$  microns. In the contact doped case, the mobilities are around  $270 \text{ cm}^2/\text{Vs}$ , with  $<20\%$  variation with channel length over this range, which is in consistent with the intrinsic device mobility determined from inset of FIG. 31C. These data provide additional evidence that these devices show negligible effects of contact resistance. We note that, in addition to the different mobilities, we notice that the devices with doped contacts are more stable, more uniform in their properties and less sensitive to processing conditions than those with undoped contacts.

Mechanical flexibility is an important characteristic of devices of this type. We performed systematic bending tests on the contact-doped  $\mu\text{-Si}$  transistors, with bending directions that place the devices in compression and in tension. We also carried out some fatigue tests. The details of the experimental set-up is provided in Example 6. FIG. 32A shows the change of the effective device mobility, normalized by the value in the unbent state,  $\mu_{0eff}$ , as a function of strain (or bending radius). Negative and positive strains correspond to tension and compression, respectively. For

this range of strains (corresponding to bend radii down to ~1 cm for the 200 micron thick substrate), we observed only small (<20% in most cases) changes in  $\mu_{eff}/\mu_{o,eff}$  the threshold voltage and the on/off ratio. This level of mechanical flexibility is comparable to that reported for organic and a-Si transistors on plastic substrates. FIG. 32B presents normalized effective mobilities  $\mu_{eff}/\mu_{o,eff}$  after several hundred bending cycles (to a radius of 9.2 mm) that cause compressive strain at the device to vary between 0 and 0.98%. Little change in the properties of the devices was observed; after 350 cycles, the  $\mu_{eff}/\mu_{o,eff}$  the threshold voltage and the on/off ratio change by less than 20%. These results indicate good fatigue stability of the present transistors comprising printable heterogeneous semiconductor elements.

This example demonstrates the usefulness of spin-on dopant processes for contact-doped printable single crystal silicon semiconductor elements in transistors on plastic substrates. Scaling analysis indicates that the present process yields devices that are not contact limited, which demonstrates the applicability of the present methods for fabricating high frequency silicon devices on plastic substrates. This feature, combined with the remarkably good mechanical flexibility and fatigue stability of the devices, make this contact doped printable heterogeneous semiconductor approach a valuable route to a wide variety of flexible macroelectronic, microelectronic and/or nanoelectronic systems.

The present invention also provides heterogeneous integration methods for integrating printable semiconductor elements into a range of devices and device configurations. This aspect of the present invention provides fabrication pathways for making a wide range of devices wherein disparate classes of materials are assembled and interconnected on the same platform. Heterogeneous integration methods of the present invention utilize solution printing and/or dry transfer contact printing to combining two or more different materials in a manner establishing their electrical, optical and/or mechanical interconnectivity. Printable semiconductor elements of the present invention may be integrated with different semiconductor materials or other classes of materials, including dielectrics, conductors, ceramics, glasses and polymeric materials.

In one embodiment of this concept, heterogeneous integration involves transferring and interconnecting a printable semiconductor element to a semiconductor chip having a different composition, for example to assemble a system on a chip type device. In another embodiment, a plurality free standing devices and/or device components are fabricated on different kinds of semiconductor wafers (e.g. silicon wafers and GaN wafers) and subsequently integrated together on the same receiving substrate, such as a receiving wafer. In yet another embodiment, heterogeneous integration involves introducing one or more printable semiconductor elements into preformed complex integrated circuits by assembling the printable elements in specific orientations and effectively interconnecting the printable elements with other components comprising the integrated circuit. Heterogeneous integration methods of the present invention may employ a large number of other techniques for assembling and interconnecting microscale and/or nanoscale printable semiconductor elements known in the art including, but not limited to, wafer bonding methods, use of adhesives and intermediate bonding layers, annealing steps (high and low temperature anneal), treatment to strip oxide outer coating, semiconductor doping techniques, photolithography and additive multilayer processing via successive thin film layer transfer.

FIG. 33 provides a SEM image a composite semiconductor structure comprising gallium nitride microstructures direct-bonded onto a silicon wafer (1 0 0) fabricated using a heterogeneous integration method of the present invention. To fabricate the composite semiconductor structure shown in FIG. 33, printable semiconductor elements comprising GaN were micromachined from a GaN on silicon (111) wafer using inductively coupled plasma etching and released from the silicon using an anisotropic wet etch in hot aqueous KOH (100 degrees Celsius). The printable GaN elements were removed from the mother chip and printed onto a receiving silicon chip by dry transfer contact printing using a PDMS stamp. Bonding between the printable GaN elements and the silicon chip is provided by attractive intermolecular forces does not require use of an adhesive layer. The SEM image provided in FIG. 33 shows that printable semiconductor elements and transfer printing assembly methods of the present invention are capable of heterogeneous integration of different semiconductor materials.

#### Example 8: Fabrication of High Performance Solar Cells Having Printable Semiconductor Elements

It is a goal of the present invention to provide methods of making solar cells, solar cell arrays and integrated electronic devices having solar cells on large areas of substrates having a range of compositions, including flexible plastic substrates. In addition, it is a goal of the present invention to provide heterogeneous printable semiconductor elements capable of providing P-N junctions in solar cells exhibiting photodiode responses comparable to solar cells fabricated by conventional high temperature processing methods.

The ability of printable semiconductor elements of the present invention to provide heterogeneous printable semiconductor elements comprising P-N junctions with high quality P-N layer interfaces in solar cells was verified by experimental studies. Solar cells were fabricated using two different fabrication pathways for making P-N junctions, and the photodiode responses of devices made by these pathways were evaluated. The experimental results provided in this example demonstrate that printable heterogeneous semiconductor elements and related assembly methods of the present invention are useful for providing high quality P-N junctions in solar cells.

FIG. 34A provides a process flow diagram schematically illustrating processing steps in a fabrication pathway for making a solar cell comprising a printable P-N junction. As shown in FIG. 34A, a high quality semiconductor material, such as a single crystalline silicon wafer, is provided and processed in a manner generating an N doped semiconductor region positioned directly adjacent to a P doped semiconductor region. Preferably for fabricating solar cells exhibiting good efficiencies, P and N regions are in physical contact and have an abrupt interface without undoped semiconductor present between them. The processed semiconductor material is subsequently patterned and etched to define the physical dimensions of a printable a P-N junction. Subsequent processing via lift-off techniques generates a monolithic structure comprising the printable P-N junction having a P doped layer directly adjacent to an N doped semiconductor layer. The printable P-N junction is then assembled onto a substrate using solution printing or dry transfer contact printing methods of the present invention. As shown in FIG. 34A, contacts (i.e. electrodes) on P and N doped semiconductor layers may be defined by deposition on to the monolithic structure prior to lift-off processing of the printable P-N junction or by deposition onto the printable P-N

junction after assembly on the substrate. In one embodiment, contacts are defined using vapor deposition of one or more metals.

FIG. 34B shows a schematic diagram of a solar cell device configuration generated by the fabrication pathway illustrated in FIG. 34A. A 5 micron thick P doped semiconductor layer having boron dopant is provided in direct contact with two N doped semiconductor layers having phosphorous dopant. Contacts are provided directly on the N doped layers and on two enriched P doped layers in contact with the P doped semiconductor layer forming the P-N junction. Introduction of phosphorous and boron doped contact regions overcomes the contact resistance of the system. FIG. 34C shows a plot of current versus bias showing the photodiode response observed upon illumination of a solar cell device having the configuration shown in FIG. 34B. As shown in FIG. 34C current is generated when the solar cell is illuminated and provided with a positive bias.

FIG. 35A provides a process flow diagram schematically illustrating processing steps in an alternative fabrication pathway for making a solar cell comprising independently printable P and N doped semiconductor layers. As shown in FIG. 35A, a high quality semiconductor material, such as a single crystalline silicon wafer, is provided and processed in a manner generating discrete N doped and P doped semiconductor regions. The processed semiconductor material is subsequently patterned and etched to define the physical dimensions of separate P doped and N doped layers. Subsequent processing via lift-off techniques generates a separately printable P doped semiconductor layer and/or a separately printable N doped semiconductor layer. A P-N junction is then assembled by printing a first doped semiconductor element (either P or N doped) onto a second doped semiconductor element having a different composition such that it is in contact with the first doped element. In one embodiment, the P-N junction is assembled by printing both P and N doped semiconductor layers, for example by printing a first doped semiconductor layer onto a substrate and subsequently printing a second doped semiconductor layer onto the first doped semiconductor layer. Alternatively, the PN junction may be assembled by printing a first doped semiconductor layer onto a substrate comprising a second doped semiconductor layer. Any orientation of P and N doped layers providing a good interface between these elements is usable in the present invention including, but not limited to, a orientation in which the first doped semiconductor element is contacted to the top of the second doped semiconductor element.

Joining N and P doped printable semiconductor elements may be accomplished via wafer bonding techniques well known in the art (See, e.g. "Materials Science and Engineering R" Jan Haisma and G. A. C. M. Spierings, 37 pp 1-60 (2002)). Optionally, P and N doped semiconductor layers are treated prior to, during or after printing to strip away any outer insulating layers on them, such as outer oxide layers, which can interfere with establishing a P-N junction having a high quality interface between P-N doped layers. Optionally, in some embodiments any water present on the doped semiconductor surfaces to be joined is eliminated, for example by heating, prior to contacting these elements to enhance the quality of the interface in the P-N junction. Assembly of the first and second doped semiconductor elements may be carried out using solution printing or dry transfer contact printing methods of the present invention. Optionally, the fabrication pathway of this aspect of the present invention may further comprise the step of annealing the P-N junction to establish a good interface

between P and N doped semiconductor layers. Annealing is preferably carried out at temperatures low enough so as not to significantly damage the substrate supporting the P-N junction, for example at temperatures less than about 200 degrees Celsius for P-N junctions assembled on plastic substrates. Alternatively, the P-N Junction may be annealed in processing steps separate from the substrate. In this embodiment, the annealed P-N junction is allowed to cool and subsequently assembled onto the substrate via solution printing or dry transfer contact printing methods. As shown in FIG. 35A, contacts (i.e. electrodes) on P and N doped semiconductor layers may be defined by deposition on to individual doped semiconductor layers prior to lift-off processing or by deposition onto the printable P-N junction after assembly on the substrate. In one embodiment, contacts are defined using vapor deposition of one or more metals.

FIG. 35B shows a schematic diagram of a solar cell device generated by printing a N doped semiconductor layer on top of a P doped semiconductor layer of a silicon wafer. The composite structure was annealed to a temperature of about 1000 degrees Celsius to generate a P-N junction having a high quality interface between N and P doped semiconductor layers. Electrical contacts were provided directly on top of each doped semiconductor layer via vapor deposition of aluminum layers. FIG. 35C shows a SEM image of a top view of the solar cell schematically depicted in FIG. 35B. The SEM image shows the N doped semiconductor layer positioned on top of the P doped semiconductor layer and also shows the aluminum contacts on top of each doped semiconductor layer. FIG. 35D provides a plot of current versus bias demonstrating the photodiode response of the solar cell shown in FIG. 35C. As shown in FIG. 35D current is generated when the solar cell is illuminated and provided with a positive bias. FIG. 35E provides a plot of photocurrent as a function of time observed upon illumination of the solar cell shown in FIG. 35C with different intensities of light.

The physical dimensions of printable heterogeneous semiconductor elements, such as printable doped semiconductor elements and printable P-N junctions, useful in solar cells of the present invention depend on a number of variables. First, the thickness must be large enough that appreciable fractions of the incident photons per area are absorbed by the P-N junction. Therefore, the thicknesses of P and N doped layers will depend, at least in part, on the optical properties of the underlying semiconductor material, such as its absorption coefficient. For some useful applications, thicknesses of printable silicon elements range from about 20 microns to about 100 microns and thicknesses of gallium arsenide elements range from about 1 micron to about 100 microns. Second, in some device applications the thickness of the printable elements must be small enough that they exhibit a useful degree of flexible for a particular device application. Use of thin (<100 microns) elements provides flexibility, even for brittle materials such as single crystalline semiconductors, and also lowers fabrication costs by requiring less raw materials. Third, the surface area of the printable elements should be large so as to capture a significant number of incident photons.

Dopants can be introduced into the semiconductor material by any process capable of providing well defined spatial distributions of high quality doped semiconductor materials, including methods using spin-on dopants (e.g., see Example 8). Exemplary methods of introducing dopant into semiconductor materials prove control in the spatial distribution of dopants in one, two or three dimensions (i.e. depth of implantation and area of a semiconductor layer implanted

with dopant). A significant advantage of the fabrication pathways shown in FIGS. 34A and 35A is that dopant implantation and activation may be separately carried out under clean room conditions and at high temperatures. Subsequent fabrication and assembly of printable doped semiconductor elements and/or P-N junctions, however, may be carried out at lower temperatures and in non-clean room conditions, thereby allowing high throughput fabrication of solar cells on a variety of substrate materials.

**Example 9: Fabrication of Stretchable Circuits and Electronic Devices**

The present invention provides stretchable electrical circuits, devices and device arrays capable of good performance when stretched, flexed or deformed. Similar to the stretchable semiconductor elements described in Example 2, the present invention provides stretchable circuits and electronic devices comprising a flexible substrate having a supporting surface in contact with a device, device array or circuit having a curved internal surface, such as a curved internal surface exhibiting a wave structure. In this structural arrangement, at least a portion of the curved internal surface of the device, device array or circuit structure is bonded to the supporting surface of the flexible substrate. In contrast to the stretchable semiconductors in Example 2, however, the device, device array or circuit of this aspect of the present invention is a multicomponent element comprising a plurality of integrated device components, such as semiconductors, dielectrics, electrodes, doped semiconductors and conductors. In an exemplary embodiment, flexible circuits, devices and device arrays having a net thickness less than about 10 microns comprise a plurality of integrated device components at least a portion of which have a periodic wave curved structure.

In a useful embodiment of the present invention, a free standing electrical circuit or device comprising a plurality of interconnected components is provided. An internal surface of the electrical circuit or device is contacted and at least partially bonded to a prestrained elastic substrate in an expanded state. Prestraining can be achieved by any means known in the art including, but not limited to, roll pressing and/or prebending the elastic substrate, and the elastic substrate may be prestrained by expansion along a single axis or by expansion along a plurality of axes. Bonding may be achieved directly by covalent bonding or van der Waals forces between at least a portion of the internal surface of the electrical circuit or device and the prestrained elastic substrate, or by using adhesive or an intermediate bonding layer. After binding the prestrained elastic substrate and the electrical circuit or device, the elastic substrate is allowed to relax at least partially to a relaxed state, which bends the internal surface of the printable semiconductor structure. Bending of the internal surface of the electrical circuit or device generates a curved internal surface which in some useful embodiments has a periodic or aperiodic wave configuration. The present invention includes embodiments wherein all the components comprising the electrical device or circuit are present in a periodic or aperiodic wave configuration.

Periodic or aperiodic wave configurations of stretchable electrical circuits, devices and device arrays allow them to conform to stretch or bent configurations without generating large strains on individual components of the circuits or devices. This aspect of the present invention provides useful electrical behavior of stretchable electrical circuits, devices and device arrays when present in bent, stretched or

deformed states. The period of periodic wave configurations formed by the present methods may vary with (i) the net thickness of the collection of integrated components comprising the circuit or device and (ii) the mechanical properties, such as Young's modulus and flexural rigidity, of the materials comprising integrated device components.

FIG. 36A shows a process flow diagram illustrating an exemplary method of making an array of stretchable thin film transistors. As shown in FIG. 36A, an array of free standing printable thin film transistors is provided using the techniques of the present invention. The array of thin film transistors is transferred to a PDMS substrate via dry transfer contact printing methods in a manner which exposes internal surfaces of the transistors. The exposed internal surfaces are next contacted with a room temperature cured prestrained PDMS layer present in an expanded state. Subsequent full curing of the prestrained PDMS layer bonds the internal surfaces of the transistors to the prestrained PDMS layer. The prestrained PDMS layer is allowed to cool and assume an at least partially relaxed state. Relaxation of PDMS layers introduces a periodic wave structure to the transistors in the array, thereby making them stretchable. The inset in FIG. 36A provides an atomic force micrograph of an array of stretchable thin film transistors made by the present methods. The atomic force micrograph shows the periodic wave structure that provides for good electrical performance in stretched or deformed states.

FIG. 36B shows optical micrographs of an array of stretchable thin film transistors in relaxed and stretched configurations. Stretching the array in a manner generating a net strain of about 20% on the array did not fracture or damage the thin film transistors. The transition from a relax configuration to a strain configuration was observed to be a reversible process. FIG. 36B also provides a plot of drain current versus drain voltage for several potentials applied to the gate electrode showing that the stretchable thin film transistors exhibit good performance in both relaxed and stretched configurations.

**Example 10: Large Area, Selective Transfer of Printable Microstructured Silicon ( $\mu$ -Si): A Printing-Based Approach to High Performance Thin Film Transistors Supported on Flexible Substrates**

The methods, devices and device components of the present invention provide a new printing-based fabrication platform for making high performance integrated microelectronic devices and device arrays. Advantages of the present approach to macroelectronic and microelectronic technologies over conventional processing methods include compatibility with a wide range of substrate materials, physical dimensions and surface morphologies. In addition, the present printing-based approach enables a low cost, high efficiency fabrication pathway for making integrated microelectronic devices and device arrays on large areas of substrates that is compatible with pre-existing high throughput printing instrumentation and techniques.

The advanced information technologies that shape the structure of modern society depend critically on the use of microelectronic devices, ones that involve ever increasing higher densities of integration. From the initial circuits (ICs) of the late 1950's, ones that incorporated fewer than 4 transistors, current state of the art ICs now integrate millions of transistors in an essentially equivalent sized package. There has been an increased interest, however, in developing new device form factors, ones in which the capabilities of semiconductor devices are embedded in structures involving

either large area and/or flexible materials supports using fabrication method that serve to in an attempt to decrease costs while maintaining high device performance levels. Such devices technologies could find wide application as active matrix pixel display drivers and components of RF identification tags. Recent reports detail the use of solution processing methods to construct models of such circuits, notably ones based on semiconductor nanowires (NWs) or networked nanotubes. Although functional devices prepared in this way are promising, they are generally characterized by significantly lower levels of device performance compared to conventional high temperature semiconductor processing approaches. For example, field effective mobilities ranging from ~2 cm<sup>2</sup>/Vs and ~40 cm<sup>2</sup>/Vs are reported for thin film transistors (TFTs) prepared using solution processing methods.

In one aspect, the present invention provides a “top down” fabrication strategy using microstructured single-crystalline silicon ( $\mu$ s-Si) ribbons harvested from silicon-on insulator wafers for use in ultra-high performance TFTs. This fabrication technique is compatible with respect to a range of useful semiconductor materials, and has been successfully adapted to other industrially useful semiconductor materials that include GaN, InP and GaAs.

In this example we demonstrate a number of important processing steps useful in the implementation of this technology, including fabrication methods which allow the selective transfer and accurate registration of silicon ribbons across large substrate areas, and versatile printing procedures applicable to both rigid (i.e. glass) and flexible plastic substrates. We specifically report here two methods that can be used to selectively remove  $\mu$ s-Si from an SOI wafer and subsequently transfer them in patterned forms onto a plastic substrate. The processes, for convenience referred to have as Method I (FIG. 37A) and Method II (FIG. 37B), use different mechanisms of adhesive bonding to affect the printing-based pattern transfer of the  $\mu$ s-Si. Method I exploits physical bonding between a molded Sylgard 3600 poly(dimethylsiloxane) (PDMS) stamp (a new experimental, high modulus PDMS product provided by the Dow Corning Corp.) and  $\mu$ s-Si objects. Method II uses a recently developed masterless soft-lithography technique to chemically bond the  $\mu$ s-Si to a PDMS coated substrate.

FIG. 37A provides a schematic diagram showing a processing method of the present invention (Method I) for patterning  $\mu$ s-Si elements onto a plastic substrate. In the present example, the plastic substrate comprised a poly(ethyleneterephthalate) (PET) sheet. A peanut shaped photoresist pattern is developed on top of a SOI substrate using standard photolithography techniques. Plasma etching, followed by resist stripping, yields  $\mu$ s-Si “peanuts” that are supported on top of a buried oxide layer. The sample is then etched incompletely using HF to give undercut peanuts held only by a residual oxide layer present at the dumbbell ends of the  $\mu$ s-Si. The SOI wafer is then laminated with a hard 3600 PDMS stamp molded with features corresponding to the latent image of the desired pattern transfer. The raised features of the stamp correspond to regions where  $\mu$ s-Si is removed selectively from the SOI surface due to strong autoadhesion to the PDMS. The stamp, after peeling it away from the SOI wafer, is then placed in contact with a poly(ethyleneterephthalate) (PET) sheet coated with polyurethane (PU) that had been partially cured using a UV lamp. A bar coating technique is used to deposit the PU adhesion level to ensure a uniform coating thickness over the large area of the (600 cm<sup>2</sup>) plastic substrate. The  $\mu$ s-Si on the stamp is then placed in contact with the PU coated side of

the plastic sheet, a second UV/Ozone exposure is then preformed from the PET side of the sandwich to fully cure the PU and enhance its bonding to the  $\mu$ s-Si. Pealing the stamp from the plastic substrate results in the detachment of the microstructured silicon from the PDMS, thus completing the transfer to the PU coated substrate.

FIG. 37B provides a schematic diagram illustrating an alternative processing method of the present invention (Method II) for patterning  $\mu$ s-Si elements onto a plastic substrate. In the present example, the plastic substrate comprised a poly(ethyleneterephthalate) (PET) sheet. This recently reported Decal Transfer Lithography (DTL) technique effects the pattern transfer using a flat, unmolded PDMS slab that is photochemically treated to provide spatially modulated strengths of adhesion. An UV/Ozone (UVO) treatment is patterned across the surface of a slab of conventional Sylgard 184 PDMS using a microreactor photomask to pattern the UVO modification with high spatial resolution. After exposure, the photochemically modified PDMS coated PET is placed in contact with a peanut presenting SOI wafer and heated to 70° C. for 30 minutes. The fabrication of the peanut shapes on the SOI wafer followed the same procedures of Method I (see FIG. 37A), with the addition of evaporating a thin film of SiO<sub>2</sub> (5 nm) onto the surface after the HF etching step. This layer facilitates strong chemical bonding to the PDMS. After heating, the PDMS is peeled from the SOI, giving a patterned transfer of  $\mu$ s-Si to the UVO modified regions of the PDMS.

FIG. 38A shows the design of the so-called peanut shaped  $\mu$ s-Si objects used in methods of the present invention. Inset optical image in FIG. 38A shows the optimized HF etching condition where the buried oxide under the channel is removed while a sacrificial SiO<sub>2</sub> portion remains. The peanut shape is particularly beneficial because its ends are slightly wider than the body of the structure. Upon etching the underlying oxide layer in an HF solution, the timing can be optimized such that the oxide layer under the center is completely removed while a sacrificial portion of SiO<sub>2</sub> still remains at either end (the dumbbell region seen in the inset image of FIG. 38A). It is this residual SiO<sub>2</sub> layer that holds the  $\mu$ s-Si in its original position. Without this oxide bridge layer, the order of the  $\mu$ s-Si created on the SOI wafer by photolithography is susceptible to lost. FIG. 38B shows an example of lost of this order when the Si objects are overetched in HF solution. As shown in FIG. 38B, Si objects start to float in the HF solution when the sample was over etched in HF solution. When the  $\mu$ s-Si is removed from the SOI wafer by either Method I or II, fracture occurs at the edges of the sacrificial region.

FIGS. 38C, 38D, 38E and 38F shows a series of micrographs that depicts the progression of each step of the  $\mu$ s-Si transfer as effected using Method I. FIG. 38C shows the  $\mu$ s-Si on the SOI wafer after optimized undercut HF etching. FIG. 38D shows the SOI wafer after the PDMS stamp removed a portion of the  $\mu$ s-Si. As shown in FIG. 38D, the PDMS stamp removes a portion of the  $\mu$ s-Si, thereby leaving the neighboring regions intact on the SOI. Since the unused microstructured silicon objects on the SOI wafer are retained at their original positions, they can be picked up by a stamp and transferred in subsequent printing steps (as discussed below). FIG. 38E shows  $\mu$ s-Si structures transferred onto the PDMS stamp. The missing center of each end of the  $\mu$ s-Si ribbons reveals the pattern of the fracture occurs during the transfer of the microstructured silicon from the SOI to PDMS stamp. FIG. 38F shows a representative result for a second transfer of the  $\mu$ s-Si (this time from the PDMS stamp

to the PU coated plastic substrate) wherein the  $\mu$ -Si that adhered to the PU support on the plastic.

Multiple transfers are possible from a small PDMS stamp to a larger plastic surface. FIGS. 39A and 39B provide optical images of the selective transfer of the  $\mu$ -Si onto PU/PET sheet by 3600 PDMS stamp. As shown in FIG. 39A, a large area ( $15 \times 15$  cm) transfer where the  $\mu$ -Si was sparsely transferred onto a plastic substrate by multiple transfers using a  $8 \times 8$  cm stamp. Each pixel in the image is of the same configuration as that shown in FIG. 38F and follows the same protocol described for FIGS. 38C-38E. The inset of FIG. 39B shows a more complex molded form, a “DARPA macroE” lettering composed of peanut  $\mu$ -Si objects smaller in size than those highlighted in FIGS. 38C-38E. The high pattern fidelity of the transfer is illustrated by the qualities of the objects defining the letter “A” (circle of inset image) as shown in FIG. 39B. These data demonstrate that only those areas directly touched by the stamp ultimately transfer to the plastic substrate. We note that this transfer is more difficult using conventional Sylgard 184 PDMS for two reasons. First, the Sylgard 184 sags when the separation distances between features exceeds twenty times the feature height. The examples shown here embrace such design rules and thus precludes high-fidelity transfers using the lower modulus polymer. Second, we also found that the Sylgard 184 sometimes does not have enough adhesive force to pickup every  $\mu$ -Si peanut from the SOI wafer and defects are observed in some applications using stamps prepared from this polymer. The 3600 PDMS from Dow Corning does not sag appreciably even at an aspect ratios of 1:200 and, perhaps more importantly, its adhesion to the  $\mu$ -Si objects is stronger than that of the 184 PDMS.

An example of a  $\mu$ -Si transfer carried out using Method II is shown in FIGS. 39C and 29D. FIG. 39C is an optical micrograph of a section of a Sylgard 184 coated PET substrate to which the  $\mu$ -Si has been chemically bonded and subsequently transferred. A higher magnification image of the  $\mu$ -Si transferred in this way is shown in FIG. 39D. It should be noted that the dimensions of the peanuts used in this demonstration are relatively small with ribbon widths of  $25 \mu\text{m}$ . We found, interestingly, that these smaller features have a different fracture point when they are removed from the SOI wafer. In the blowup of FIG. 39D, one also notes that the PDMS surface is also no longer flat. The reason for this is because of the fact that sections of the PDMS are in fact reciprocally transferred to the SOI, being ripped out of the bulk in contacting regions activated by the patterned UVO treatment, regions where the PDMS sagged and touched the wafer surface between the peanuts.

FIG. 40A illustrates an exemplary device geometry of a device fabricated using the peanut shaped  $\mu$ -Si based on a transfer using Method I. To construct these devices an Indium-Tin-Oxide (ITO) coated PET sheet is used as the substrate. The ITO served as the gate electrode and diluted SU-8 5 (measured capacitance= $5.77 \text{nF/cm}^2$ ) is employed as a gate dielectric. FIG. 40B provides I-V curves of  $\mu$ -Si TFTs at a range of gate voltage ( $V_g = -2.5 \text{ V}$  to  $20 \text{ V}$ ). As shown in FIG. 40B, these plastic supported, peanut shaped  $\mu$ -Si TFTs show an accumulation mode n-channel transistor behavior. The channel length of the device, as shown in the inset image of FIG. 40C, is  $100 \mu\text{m}$  and the width of the device is  $400 \mu\text{m}$ . FIG. 40C shows the transfer characteristics, measured at a constant source-drain voltage ( $V_{sd}=1\text{V}$ ), indicated the effective mobility was  $173 \text{ cm}^2/\text{Vs}$ . The inset in FIG. 40C shows an optical micrograph of actual device of the present invention. The transfer characteristics indicated that the threshold voltage ( $V_{th}$ ) is  $-2.5 \text{ V}$  with an effective

mobility was  $173 \text{ cm}^2/\text{Vs}$ . These values are consistent with the performance characteristics expected for a  $100 \text{ nm}$  thick bottom gate structure of this type.

The selective transfer methods described in this example provide an efficient route for transferring microstructured silicon from a SOI wafer to a flexible, macroelectronic system. Using these techniques, and in contrast with conventional solution casting methods, the microstructured silicon objects can be transferred from an SOI mother wafer with precise registration and utilized in ways that minimize waste. The mechanical properties of the new 3600 PDMS investigated in this work demonstrates that it has a number of important advantages as compared to the commercial Sylgard 184 PDMS resin, notably its dimensional stability and higher surface adhesion properties. The printing techniques also proved to be compatible with the construction of macroelectronic systems that incorporate high performance  $\mu$ -Si thin film transistors.

#### Experimental

##### Method I

The fabrication of the  $\mu$ -Si objects was carried out using a commercial SOI wafer (SOITEC, p-type, top Si thickness= $100 \text{ nm}$ , resistivity= $13.5-22.5 \text{ ohm}\cdot\text{cm}$ ,  $145 \text{ nm}$  buried oxide layer). Photolithography (Shipley 1805 resist) was used to pattern the SOI wafer into the desired peanut-shaped geometry (mid-section length:  $200 \mu\text{m}$ , width:  $25 \mu\text{m}$ , diameter of peanut:  $50 \mu\text{m}$ ). Dry etching (Plasmatherm RIE system, SF<sub>6</sub> flow,  $40 \text{ sccm}$ ,  $50 \text{ mTorr}$ , RF power= $100 \text{ W}$ ,  $45 \text{ sec}$ ) was then used to remove the exposed silicon. The underlying SiO<sub>2</sub> was then etched for  $80 \text{ seconds}$  in an HF (49%) solution. For the 3600 PDMS stamp of Method I, a specialty PDMS (Dow Corning, 3600, elastic modulus= $8 \text{ MPa}$ ) and Sylgard 184 (Dow corning, elastic modulus= $1.8 \text{ MPa}$ ) was mixed in a one to one ratio and cured using standard soft-lithographic patterning methods. A UV source (ozone active mercury lamp,  $173 \mu\text{W/cm}^2$ ) was used to cure the PU thin film adhesion layer (Norland optical adhesive, No. 73). These latter films were coated onto a PET substrate ( $180 \mu\text{m}$  in thickness, Mylar film, Southwall technologies) using a bar coating procedure (Meyer bar, RD specialties).

##### Method II

For Method II, the sizes of the peanut shapes used were smaller than the ones used in Method I (mid-section length:  $10 \mu\text{m}$ , width:  $2 \mu\text{m}$ , diameter of ends:  $5 \mu\text{m}$ ). A similar fabrication protocol was used to produce these structures with the exception that the RIE etching time was reduced to  $25 \text{ seconds}$  (to minimize sidewall etching) and the buried oxide layer was etched for  $30 \text{ seconds}$  in a concentrated (49%) HF solution. After the latter etching step, the sample was rinsed in a water bath and dried in an oven at  $70^\circ \text{C}$ . for  $5 \text{ minutes}$ . A  $50 \text{ \AA}$  SiO<sub>2</sub> layer was then evaporated on top of the sample (Temescal FC-1800 Electron Beam Evaporator). To bind a thin layer of PDMS onto the PET substrate, a layer of PU was first cast by spinning onto the PET at  $1000 \text{ rpm}$  for  $30 \text{ seconds}$  and exposed to UVO ( $173 \mu\text{W/cm}^2$ ) for  $4 \text{ minutes}$ . A film of PDMS was then spin-cast at  $1000 \text{ rpm}$  for  $30 \text{ seconds}$  onto the PU a cured thermally at  $65^\circ \text{C}$ . for three hours.

The selective area soft lithographic patterning procedure comprised placing the unpatterned PDMS side of the coated PET substrate in contact with the patterned side of the UVO photomask. The fabrication of this microreactor mask followed procedures described by Childs et. al. The pattern consisted of two interlocking rectangular arrays ( $1.2 \times 0.6 \text{ mm}$ ). The PDMS was then irradiated through the UVO photomask for  $3 \text{ minutes}$  at a distance of  $\sim 3 \text{ cm}$  from a mercury bulb (UVOCS T10x10/OES). After exposure, the

PDMS stamp was peeled away from the UV-O photomask, and the exposed PDMS face was placed into contact with the peanut-bearing SOI wafer. After heating at 70° C. for 30 minutes, tweezers were used to slowly peel the PDMS away, removing segments of the  $\mu$ -Si in registry with the areas of irradiation.

#### Device Fabrication

SU-8 5 with 66% (v) SU-8 2000 thinner was spun onto the ITO side of a coated PET sample at 3000 rpm for 30 seconds. The SU-8 epoxy was then precured at 60° C. on a hot plate for ~1 minute. The PDMS stamp (Method I) with the  $\mu$ -Si on its surface was then brought into contact with the epoxy layer for 30 seconds and peeled back to transfer the  $\mu$ -Si to the epoxy. The SU-8 dielectric was then fully cured at 115° C. for 2 minutes, exposed to UV for 10 seconds, and postbaked at 115° C. for 2 minutes. Metal for titanium contacts (40 nm) was then added by e-beam evaporation, with the source-drain area patterned using standard photolithographic methods in conjunction with etching using a 1% HF solution.

#### Example 11: Bendable GaAs Metal-Semiconductor Field Effect Transistors Formed with Printed GaAs Wire Arrays on Plastic Substrates

The fabrication methods of the present invention are versatility with respect to the materials that can be assembled and integrated into useful functional devices and device components. Particularly, the present methods are applicable to fabrication of semiconductor based microelectronic and macroelectronic devices using a range of high quality semiconductor materials, including non-silicon materials. To demonstrate this capability of the present methods bendable metal-semiconductor field-effect-transistors (MESFETs) having GaAs microwires were fabricated by present methods and evaluated with respect to their electrical and mechanical attributes.

Field effect transistors formed with high quality, single crystalline semiconductor nano- and microstructures on large area, mechanically flexible plastic substrates are of great interest for a wide range of applications in displays, sensors, medical devices and other systems. A number of approaches have been demonstrated to transfer high quality semiconductor materials (e.g., Si nanowires, microribbons, platelets, etc.) onto plastic substrates for mechanically flexible metal-oxide-semiconductor field-effect-transistors (MOSFETs). The methods of the present invention are useful for fabricating bendable metal-semiconductor field-effect-transistors (MESFETs) on plastic substrates using GaAs microwires (a class of material that we refer to as microstructured GaAs, or  $\mu$ -GaAs) that have integrated ohmic source/drain contacts. In these methods, high quality bulk GaAs wafers provide the starting material for ‘top down’ fabrication procedures to form the micro/nanowires. In addition, transfer printing techniques using elastomeric stamps integrate well ordered arrays of these wires with plastic substrates. Electrical and mechanical measurements of MESFETs formed in this way demonstrate that good performance and excellent bendability is achievable using the present methods.

FIG. 41 provides a schematic illustration of the major steps for fabricating, on flexible plastic substrates (poly (ethylene terephthalate) (PET)), MESFETs that use arrays of single crystalline GaAs wires with epitaxial n-type channel layers, and integrated ohmic contacts of AuGe/Ni/Au. A (100) semi-insulating GaAs (SI—GaAs) wafer with an epitaxial Si-doped n-type GaAs layer (concentration of

$4.0 \times 10^{17}/\text{cm}^3$ , IQE Inc., Bethlehem, Pa.) provides the source material for generating the microwires. Photolithography and metallization via electron-beam (and/or thermal) evaporation generates arrays of narrow metal stripes (with width of 2  $\mu\text{m}$  and spacing of 13  $\mu\text{m}$ ) comprising conventional multilayer stacks, i.e., AuGe (120 nm)/Ni (20 nm)/Au (120 nm) for ohmic contacts. Annealing the wafer at elevated temperature (i.e., 450° C. for 1 min) in a quartz tube with flowing N<sub>2</sub> forms ohmic contacts to the n-GaAs.

Defining the metal stripes along the (0 1 1) crystalline orientation of GaAs enables microwires (with integrated ohmic contacts) to be generated using a top down fabrication approach. As shown in processing step i in FIG. 41, a pattern of photoresist is defined on top of the metal stripes (3  $\mu\text{m}$  widths); the openings between these lines lie between adjacent metal stripes. These openings allow etchant (H<sub>3</sub>PO<sub>4</sub> (85 wt %):H<sub>2</sub>O<sub>2</sub> (30 wt %):H<sub>2</sub>O=1:13:12 in volume) to diffuse to the GaAs surface to etch GaAs anisotropically. The photoresist protects the interface between ohmic stripes and GaAs from exposure. The anisotropic etching generates reverse mesas and undercuts along the surface of GaAs, resulting in the formation of GaAs wires with triangular cross section and narrow width released from mother wafer. The undercut yields GaAs wires with widths down to micrometer and/or nanometer length scales by controlling the geometry of the resist and the etching time. Each wire has two ohmic stripes separated by a gap that defines the channel length of the resultant MESFET. As shown in processing step ii in FIG. 41, contacting a flat, elastomeric stamp of poly(dimethylsiloxane) (PDMS) to the photoresist coated GaAs wires forms a van der Waals bond between the hydrophobic surfaces of the PDMS and the photoresist. As shown in processing step iii in FIG. 41, this interaction enables removal of all of the GaAs wires from the wafer to the surface of the PDMS when the stamp is peeled back from the mother wafer. This transfer process preserves the lithographically defined spatial organization (i.e. aligned arrays) of the wires. The PDMS stamp with GaAs wires is then laminated against a PET sheet covered with a thin layer of liquid polyurethane (PU, NEA 121, Norland Products Inc., Cranbury, N.J.), a kind of photocurable polymer.

As shown in processing step iv in FIG. 41, curing the PU, peeling off the PDMS stamp and removing the photoresist by O<sub>2</sub> reactive ion etching (RIE, Unaxis 790, Plasma-Therm Reaction Ion Etching System) leaves the ordered GaAs wires with exposed ohmic stripes embedded on the surface of the PU/PET substrate. In the transfer printing process, the photoresist serves not only as an adhesive layer but also as a protective film to prevent the surfaces of the GaAs wires and ohmic contacts from being contaminated. As shown in processing step v in FIG. 41, further lithographic processing on the PU/PET substrate defines electrodes (250 nm Au) that connect the ohmic stripes to form the source and drain, and for gate electrodes (Ti (150 nm)/Au (150 nm)). The resultant arrays of MESFETs are mechanically flexible due to the bendability of PU/PET sheet (thickness of ~200  $\mu\text{m}$ ) and the GaAs wires (widths and thicknesses less than 5  $\mu\text{m}$ ).

FIG. 42A presents a schematic showing a cross section view of the geometry of a GaAs wire based MESFET on a plastic substrate (PU/PET). The source/drain electrodes form ohmic contacts to the n-GaAs layer. The gate electrode forms a Schottky contact to this layer. The strong interaction between the cured PU and the side walls of the GaAs wires bonds the wires to the PU/PET substrate. In this geometry and with the processing approach described previously, the active n-GaAs layer (i.e., the transistor channel) never contacts any polymeric materials other than photoresist. The

Ti/Au gate electrode forms a Schottky contact with the n-GaAs surface; the barrier allows one to apply a relatively negative voltage (i.e., <0.5 V) to modulate the flow of current between the source and drain electrodes, as in a conventional MESFET. FIG. 42B shows a representative image of two GaAs wire based MESFETs on plastic each of which uses an array of ten GaAs wires, fabricated according to the process flow diagram of FIG. 41. The wires have well-aligned orientation and uniform widths of ~1.8  $\mu\text{m}$ . Au pads with widths of 150  $\mu\text{m}$  and lengths of 250  $\mu\text{m}$  connect the ohmic stripes on ten GaAs wires to form source and drain electrodes for each individual MESFET. A Ti/Au stripe with width of 15  $\mu\text{m}$  and deposited in the 50- $\mu\text{m}$  gap (transistor channel) between source and drain electrodes provides the gate electrode. These stripes connect to a larger metal pad for probing. The contrast difference between the metal on the wires and that on the plastic is likely due to surface roughness on the PU generated during RIE etching of the photoresist. FIG. 42C shows the image of a 2 cm $\times$ 2 cm PET sheet with hundreds of transistors, clearly demonstrating its flexibility. Multiple printing steps and/or wire fabrication runs may be used to generate large numbers of wires patterned over large areas on plastic substrates. Various parameters, such as the widths of the GaAs wires, the widths of the source/drain electrodes, the channel and gate lengths are adjusted easily to yield MESFETs with a range of desired output characteristics.

The DC performance of the transistors was characterized to evaluate their electrical and mechanical properties. FIGS. 43A, 43B and 43C present results from a GaAs MESFET with a channel length of 50  $\mu\text{m}$ , a gate length of 15  $\mu\text{m}$ , similar to the one shown in FIG. 42B. FIG. 43A shows the current-voltage (between drain and source electrodes) curves at gate voltages between 0.5 to -2.0 V with steps of 0.5 V. The  $I_{DS}$ - $V_{DS}$  characteristics are comparable to conventional wafer based MESFETs built with n-type GaAs layer and standard techniques, i.e.,  $I_{DS}$  saturates in the regions of high  $V_{DS}$  and  $I_{DS}$  decreases with decrease of gate voltage. In the linear region, the channel resistance at  $V_{GS}=0$  V is  $R_{channel}=6.4 \text{ k}\Omega$ . FIG. 43B shows the transfer characteristics (i.e.,  $I_{DS}$  vs.  $V_{GS}$ ) of a GaAs MESFET of the present invention measured at different  $V_{DS}$ . All of the curves have minima at the same gate voltage, i.e., -2.65 V. The drop of  $I_{DS}$  at high positive gate voltages is due to the leakage current from gate to source that develops through the Schottky contact in this regime. FIG. 43C shows the transfer curve at  $V_{DS}=4$  V, plotted as  $(I_{DS})^{1/2}$  vs.  $V_{GS}$ , clearly showing a linear relationship as expected for a MESFET. The pinch-off voltage and transconductance at  $I_{DS}=0.19 \text{ mA}$  and  $V_{DS}=4 \text{ V}$  are  $V_p=2.65 \text{ V}$  and  $g_m=168 \mu\text{S}$ , respectively. These characteristics indicate that the transistors fabricated on PET substrates resemble the behavior of typical GaAs MESFETs fabricated on wafers by traditional approach.

Mechanical flexibility represents an important parameter of devices on plastic substrates for many of the target applications that are being considered. We tested the transistors by bending the supporting PET sheet. FIGS. 44A and 44B show gate-modulated current-voltage characteristics of a GaAs wire based MESFET on a flexible PET substrate (A) before bending; (B) after bending to a bend radius of 8.4 mm. These figures compare the performance of a transistor before and after the substrate was bent to a radius of 8.4 mm, i.e., corresponding surface strain of 1.2% (tensile in this case) for the 200  $\mu\text{m}$  thick substrate. The results indicate that the transistor can withstand these high strains without failure. In fact, the saturated current at  $V_{GS}=0 \text{ V}$ , increases by ~20% in this case. FIG. 44C shows the gate-modulated current-

voltage characteristics of the GaAs wire based MESFET after relaxing the bent substrate to its flat, unbent state. A comparison of FIG. 44C and FIG. 44A indicates that after releasing the strain, i.e., such that the substrate becomes flat again, the transistor recovers the performance of its original state. FIG. 44D shows the variation of  $I_{DS}$  at  $V_{DS}=4 \text{ V}$  and  $V_{GS}=0 \text{ V}$  in 3 cycles in terms of bending (with different surface strains)/unbending, indicating that these MESFETs survive multiple bending cycles that cause the tensile strain at the device to vary between 0% and 1.2%, without significant change of their performance (<20%). The systematic changes observed with strain may be related to the fact that mechanical strain causes displacement of crystalline lattice of GaAs wires and their distribution of energy levels.

This example describes an approach that involves (i) generation of ohmic contacts by high temperature annealing on GaAs wafers, (ii) production of GaAs micowires with these integrated ohmic contacts by anisotropic chemical etching, (iii) dry transfer printing of these wires onto plastic substrates with an elastomeric stamp, and (iv) fabrication of high quality MESFETs by low temperature processing of these wires on plastics, to yield the flexible GaAs MESFETs on plastic substrates. The intrinsic properties of GaAs (e.g. high mobilities), the ability to make the MESFETs with short gate lengths and the straightforward paths for integrating these devices into complex circuits (potentially with other transistors built using similar approaches but with other semiconductors) indicate a use for achieving high frequency response for advanced communication, space and other systems. These advantages as well as the remarkably good mechanical flexibility of these devices make GaAs wire MESFETs interesting for flexible macroelectronic systems.

In summary, Micro/nanowires of GaAs with integrated ohmic contacts have been prepared from bulk wafers by metal deposition and patterning, high temperature annealing and anisotropic chemical etching. These wires provide a unique type of material for high performance devices that can be built directly on a wide range of unusual device substrates, such as plastic or paper. In particular, transfer printing organized arrays of these wires at low temperatures onto plastic substrates yield high quality, bendable metal-semiconductor field effect transistors (MESFETs). Electrical and mechanical characterization of devices on poly(ethylene terephthalate) illustrates the level performance that can be achieved. These results indicate promise for this approach to high speed flexible circuits for emerging applications in consumer and military electronic systems.

#### Example 12: Device Configurations Using Printable Semiconductor Elements

FIG. 45 provides a schematic diagram illustrating an exemplary device configuration of the present invention for a P type bottom gate thin film transistor on a plastic substrate. As shown in FIG. 45, the P type bottom gate thin film transistor comprises a silicon printable semiconductor element with doped contact regions, an indium tin oxide bottom gate electrode, an epoxy dielectric layer and source and drain electrodes. The plastic substrate is a poly(ethylene terephthalate) (PET) sheet. Also provided in FIG. 45 are current-voltage characteristics typical of these devices for a range of gate voltages.

FIG. 46 provides a schematic diagram illustrating an exemplary device configuration of the present invention for a complementary logic gate on a plastic substrate. As shown in FIG. 46, the complementary logic gate comprises a P-type

thin film transistor and a N-type thin film transistor, each having printable semiconductor elements and provided on a poly(ethylene terephthalate) (PET) sheet.

FIG. 47 provides a schematic diagram illustrating an exemplary device configuration of the present invention for a top gate thin film transistor on a plastic substrate. As shown in FIG. 45, the top gate thin film transistor comprises a silicon printable semiconductor element with doped contact regions, a SiO<sub>2</sub> dielectric layer and gate, source and drain electrodes. The plastic substrate is a poly(ethylene terephthalate) (PET) sheet having a thin epoxy layer to facilitate transfer and assembly of the thin film transistors and components thereof. Also provided in FIG. 47 are current-voltage characteristics typical of these devices for a range of gate voltages.

We claim:

1. A wafer of printable light emitting diodes, the wafer comprising:

a substrate native to a plurality of printable light emitting diodes; and

the plurality of printable light emitting diodes, each light emitting diode of the plurality of printable light emitting diodes disposed on the native substrate and partially released from the substrate such that each light emitting diode is connected to the substrate via a partially etched sacrificial layer, wherein the plurality of printable light emitting diodes are in contact with a transfer device, and wherein a remaining portion of the partially etched sacrificial layer connecting each light emitting diode to the substrate provides an alignment maintaining element that is breakable when the transfer device moves away from the substrate.

2. The wafer of claim 1, wherein the partially etched sacrificial layer is located between the substrate and the plurality of printable light emitting diodes.

3. The wafer of claim 2, wherein the partially etched sacrificial layer comprises SiN.

4. The wafer of claim 2, wherein the partially etched sacrificial layer comprises SiO<sub>2</sub>.

5. The wafer of claim 1, wherein the printable light emitting diode comprises an inorganic semiconductor structure.

6. The wafer of claim 1, wherein the wafer is a member selected from the group consisting of a single crystalline silicon wafer, a silicon on insulator wafer, a polycrystalline silicon wafer, a GaAs wafer, a silicon on substrate wafer, a germanium wafer, a thin film, polycrystalline silicon wafer, and an ultra thin silicon wafer.

7. The wafer of claim 1, wherein the plurality of printable light emitting diodes form an array of light emitting diodes.

8. The wafer of claim 1, wherein the substrate is a member selected from the group consisting of gallium arsenide, gallium nitride, silicon, and germanium.

9. The wafer of claim 1, wherein each printable light emitting diode comprises a top surface coated with a release layer that facilitates bonding of the printable light emitting diode to a contact surface of the transfer device and subsequent release.

10. The wafer of claim 9, wherein the release layer comprises a photoresist.

11. The wafer of claim 1, wherein each printable light emitting diode comprises at least one smooth surface exhibiting deviations from an average surface position of less than 10 nm.

12. The wafer of claim 1, wherein each printable light emitting diode has a field effect mobility greater than or equal to 300 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>.

13. The wafer of claim 1, wherein each printable light emitting diode comprises an N-doped semiconductor region positioned directly adjacent to a P-doped semiconductor region.

14. The wafer of claim 1, wherein each printable light emitting diode of the plurality of light emitting diodes has a thickness between 10 nm to 100 microns.

15. The wafer of claim 14, wherein each printable light emitting diode of the plurality of light emitting diodes has a width from 100 nm to 1 millimeter.

16. The wafer of claim 15, wherein each printable light emitting diode of the plurality of light emitting diodes has a length from 1 micron to 1 millimeter.

17. A wafer of printable light emitting diodes, the wafer comprising:

a substrate native to a plurality of printable light emitting diodes; and

the plurality of printable light emitting diodes, each light emitting diode of the plurality of printable light emitting diodes disposed on the native substrate and partially released from the substrate such that each light emitting diode is connected to the substrate via a partially etched sacrificial layer, wherein the plurality of printable light emitting diodes are in contact with a transfer device, and wherein a remaining portion of the partially etched sacrificial layer connecting each light emitting diode to the substrate provides an alignment maintaining element that is breakable when the transfer device moves away from the substrate; and wherein each printable light emitting diode comprises a top surface coated with a release layer that facilitates bonding of the printable light emitting diode to a contact surface of a transfer device and subsequent release.

18. The wafer of claim 17, wherein the release layer comprises a photoresist.

19. A wafer of printable light emitting diodes, the wafer comprising:

a substrate native to a plurality of printable light emitting diodes; and

the plurality of printable light emitting diodes, each light emitting diode of the plurality of printable light emitting diodes disposed on the native substrate and partially released from the substrate such that each light emitting diode is connected to the substrate via a partially etched sacrificial layer, wherein a remaining portion of the partially etched sacrificial layer connecting each light emitting diode to the substrate breaks when a transfer device moves away from the substrate; wherein

the partially etched sacrificial layer comprises SiN or SiO<sub>2</sub>.

20. A wafer of printable light emitting diodes, the wafer comprising:

a substrate native to a plurality of printable light emitting diodes; and

the plurality of printable light emitting diodes, each light emitting diode of the plurality of printable light emitting diodes disposed on the native substrate and partially released from the substrate such that each light emitting diode is connected to the substrate via a partially etched sacrificial layer, wherein a remaining portion of the partially etched sacrificial layer connecting each light emitting diode to the substrate breaks when a transfer device moves away from the substrate; wherein

the wafer is a member selected from the group consisting of a single crystalline silicon wafer, a silicon on insu-

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lator wafer, a polycrystalline silicon wafer, a GaAs wafer, a silicon on substrate wafer, a germanium wafer, a thin film, polycrystalline silicon wafer, and an ultra thin silicon wafer.

**21.** A wafer of printable light emitting diodes, the wafer comprising:

a substrate native to a plurality of printable light emitting diodes; and

the plurality of printable light emitting diodes, each light emitting diode of the plurality of printable light emitting diodes disposed on the native substrate and partially released from the substrate such that each light emitting diode is connected to the substrate via a partially etched sacrificial layer, wherein a remaining portion of the partially etched sacrificial layer connecting each light emitting diode to the substrate breaks when a transfer device moves away from the substrate; wherein

the substrate is a member selected from the group consisting of gallium arsenide, gallium nitride, silicon, and germanium.

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**22.** A wafer of printable light emitting diodes, the wafer comprising:

a substrate native to a plurality of printable light emitting diodes; and

the plurality of printable light emitting diodes, each light emitting diode of the plurality of printable light emitting diodes disposed on the native substrate and partially released from the substrate such that each light emitting diode is connected to the substrate via a partially etched sacrificial layer, wherein a remaining portion of the partially etched sacrificial layer connecting each light emitting diode to the substrate breaks when a transfer device moves away from the substrate; wherein

each printable light emitting diode comprises an N-doped semiconductor region positioned directly adjacent to a P-doped semiconductor region.

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