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Advanced system design using HDL
Project-2

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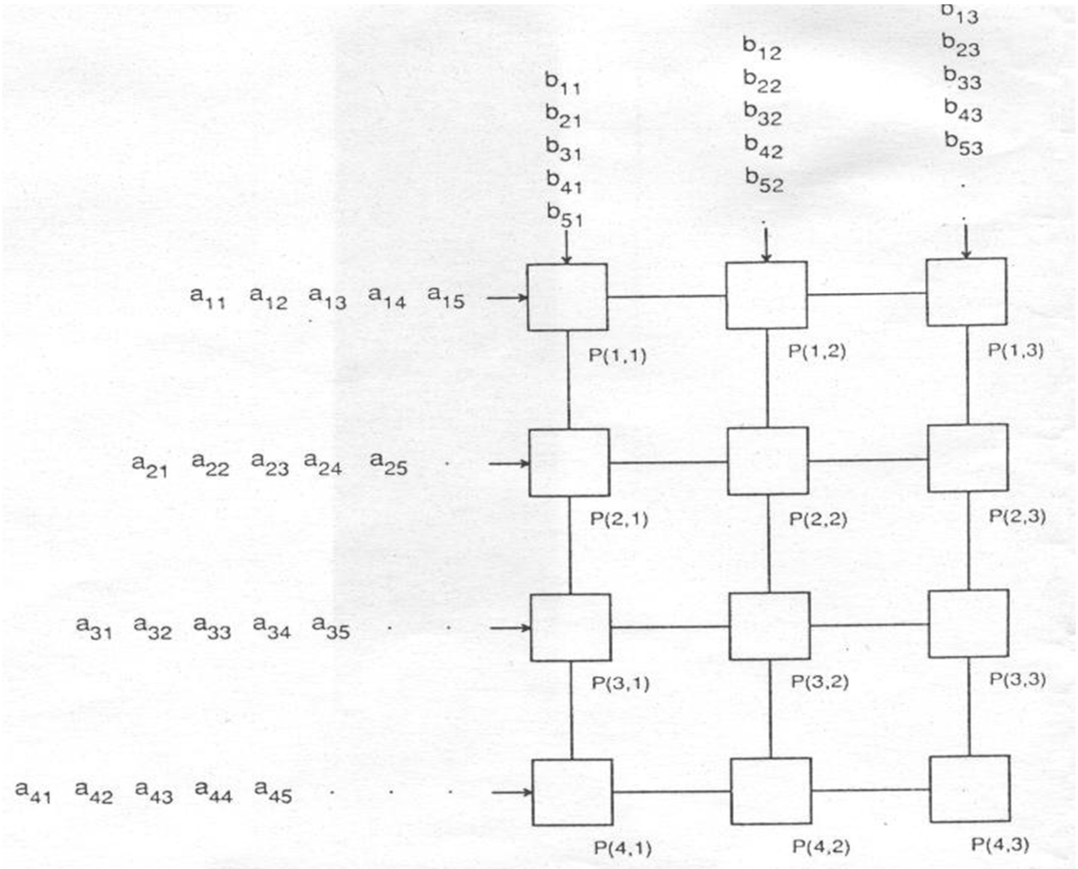
Parallel and Pipeline implementation of a matrix multiplier

Report:

The schematic of parallel and pipeline implementation of a matrix multiplier is shown below. In the schematic, each block is a MAC unit. In this project we make all the MAC's along anti-diagonal to be computed in parallel and in turn, those entire MAC's in a pipeline fashion. The size of the matrix A is 4 X 5 and that of B is 5 X 3.

During the first clock cycle, only the block, P(1,1) is executed and inputs to that block are, a11 and b11. In the next clock cycle, the block p(1,2) and p(2,1) is executed and inputs to that block are a11, b12 and a21,b11. If noticed, the inputs that are coming from the left hand side are getting shifted to the right. Similarly, the inputs that are coming from the top are getting shifted down. This process continues and all the blocks are executed in anti-diagonal fashion. We get the first output after 5 clock cycles, and the last output after 10th clock cycle.

I have created 3 files in modelsim. One named mac_unit, performs the multiplication and accumulation (MAC operation). Next, mat_mul that performs matrix multiplication by calling the mac_unit 12 times. This is called in such a fashion that, MAC operation is performed in parallel and in pipelined fashion. First, p(1,1) is called, next p(1,2) and p(2,1) next p(1,3), p(2,1) and p(2,2) and so on. This structure continues to give us a parallel combination. The last file is test_trial2 which is basically a test bench for the above operation.


b11 b21 b31 b41 b51
b12 b22 b32 b42 b52 .
b13 b23 b33 b43 b53 . .
a11 a12 a13 a14 a15
a21 a22 a23 a24 a25 .
a31 a32 a33 a34 a35 . .
a41 a42 a43 a44 a45 . . .
P(1,1)
P(1,2)
P(1,3)
P(2,1)
P(2,2)
P(2,3)
P(3,1)
P(3,2)
P(3,3)
P(4,1)
P(4,2)
P(4,3)