



# Welcome to The Logic Design Lab!

Fall 2021

## Lab 2: Advanced Gate-Level Verilog

Prof. Chun-Yi Lee

Department of Computer Science  
National Tsing Hua University

# Agenda

- Lab 2 Outline
- Lab 2 Basic Questions
- Lab 2 Advanced Questions



# Lab 2 Outline

- Basic questions (1.5%)
  - Individual assignment
  - Due on **10/7/2021 (Thu). In class.**
  - Only demonstration is necessary. Nothing to submit.
    - Please **draw the circuits of question 1, and explain the differences between the adders of question 3 in your report.**
- Advanced questions (5%)
  - Group assignment
  - eeclass submission due on **10/14/2021 (Thu). 23:59:59.**
  - Demonstration on your FPGA board (**In class**)
  - Assignment submission (**Submit to eeclass**)
    - Source codes and testbenches
    - Lab report in PDF

# Lab 2 Rules

- Only gate-level description is permitted
  - Only basic logic gates are ALLOWED (AND, OR, NAND, NOR, NOT)
  - Sorry, no xor & xnor
- Please **AVOID** using
  - Continuous assignment (e.g., **assign =**, **wire =**) and conditional operators (e.g., **: ?**)
  - Behavioral operators (e.g., **=**, **!**, **%**, **&**, **\***, **+**, **/**, **<**, **>**, **^**, **|**, **~**)

# Lab 2 Submission Requirements

- Source codes and testbenches
  - Please follow the templates **EXACTLY**
  - We will test your codes by TAs' testbenches
- Lab 2 report
  - Please submit your report in a single **PDF** file
  - Please **draw** the gate-level circuits of your designs (**please use computer softwares to draw your figures**)
  - Please **explain** your designs in detail
  - Please **list** the contributions of each team member clearly
  - **Please explain how you test your design**
  - What you have **learned** from Lab 2

# Agenda

- Lab 2 Outline
- **Lab 2 Basic Questions**
- Lab 2 Advanced Questions



# Basic Questions

- Individual assignment
- Verilog questions (due on **10/7/2021 (Thu). In class.**)
  - (Gate Level) NAND gate only
  - (Gate Level) 3-input majority gate
  - (Gate Level) 1-bit full adder & half adder
- Demonstrate your work by **waveforms**

# Verilog Basic Question 1

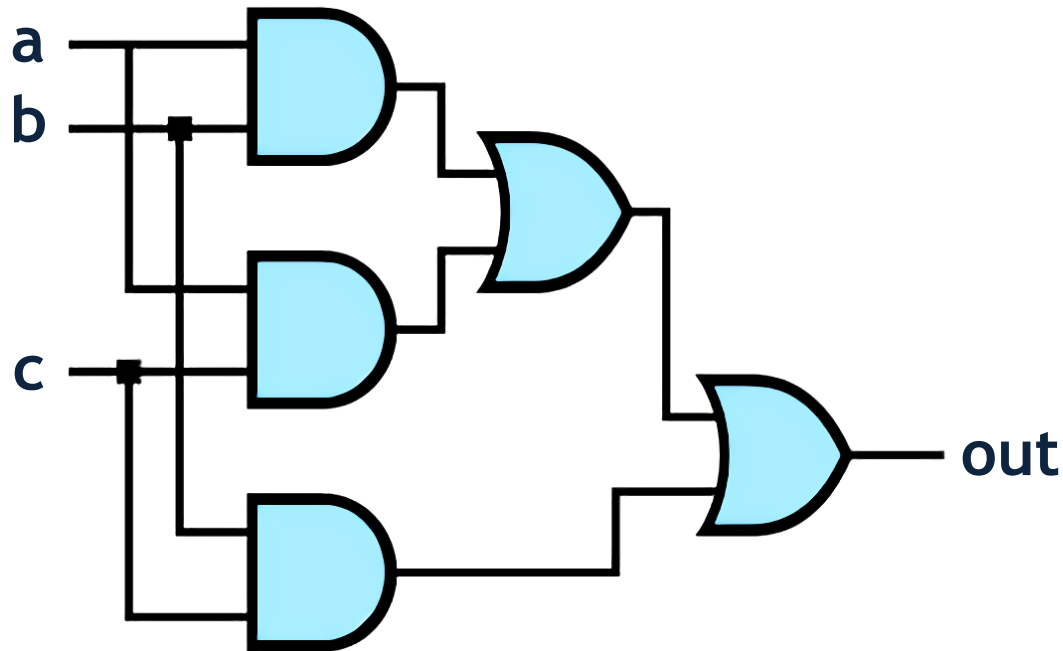
- (Gate Level) NAND gates only
  - Use **NAND gates only** to realize the following functions
  - **NOT, NOR, AND, OR, XOR, XNOR, NAND**
  - Input/Output: a (1bit), b (1bit), sel (3 bits), out (1 bit)
  - Please **draw your circuits** in your report

sel [2:0]	out
000	out = a <b>nand</b> b
001	out = a <b>and</b> b
010	out = a <b>or</b> b
011	out = a <b>nor</b> b
100	out = a <b>xor</b> b
101	out = a <b>xnor</b> b
110 & 111	out = <b>!</b> a



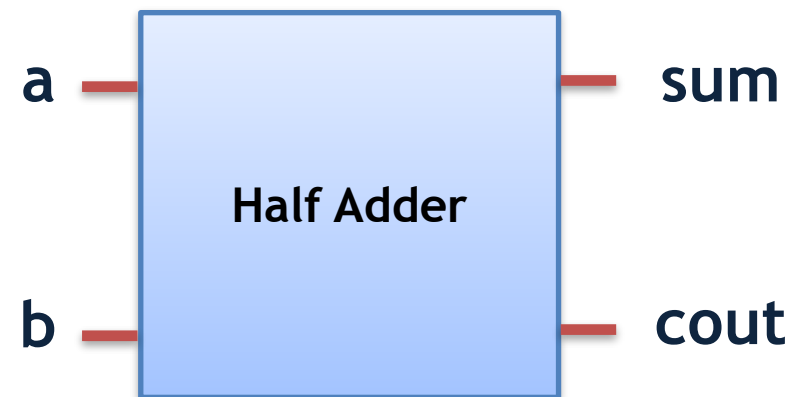
# Verilog Basic Question 2

- (Gate Level) 3-input majority gate
  - Use **NAND gates only** to realize the following circuit
  - Please reuse the modules implemented in Question 1
  - Input/Output: a (1bit), b (1bit), c (1 bit), out (1 bit)



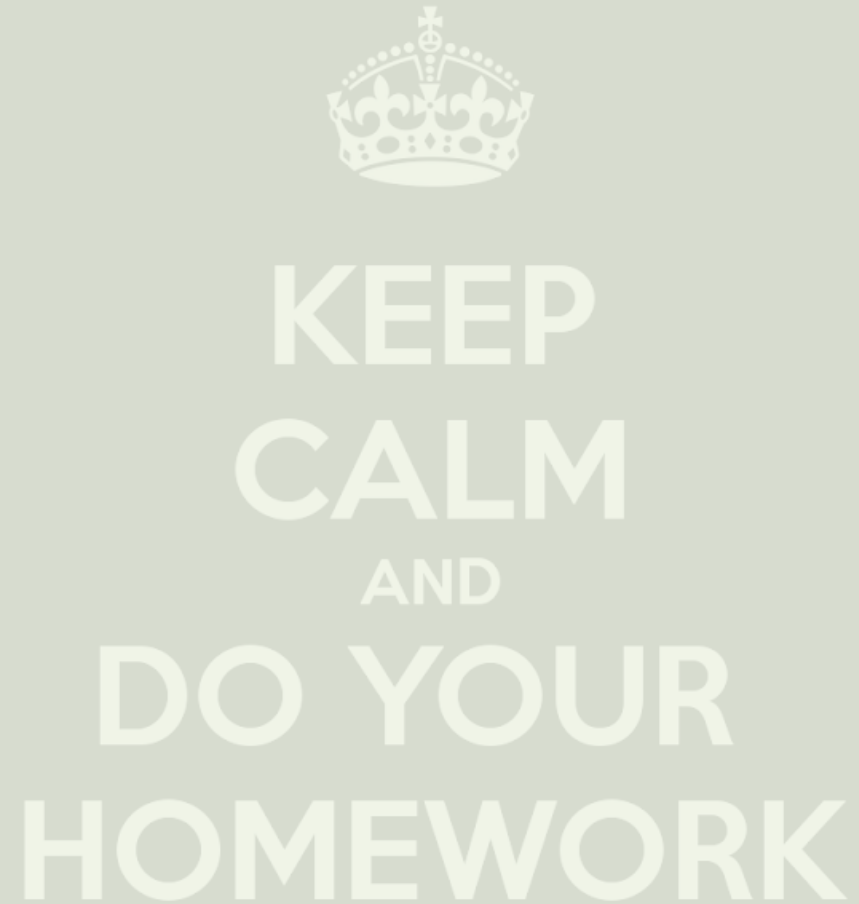
# Verilog Basic Question 3

- (Gate Level) 1-bit full adder & half adder
- Please design two modules: one for a 1-bit full adder and one for a 1-bit half adder, use **NAND gates only**
- Please reuse the module of your majority gate for the 1-bit full adder design
- Please **explain** the difference between these two adders in your **report**.



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- Lab 2 Basic Questions
- Lab 2 Advanced Questions

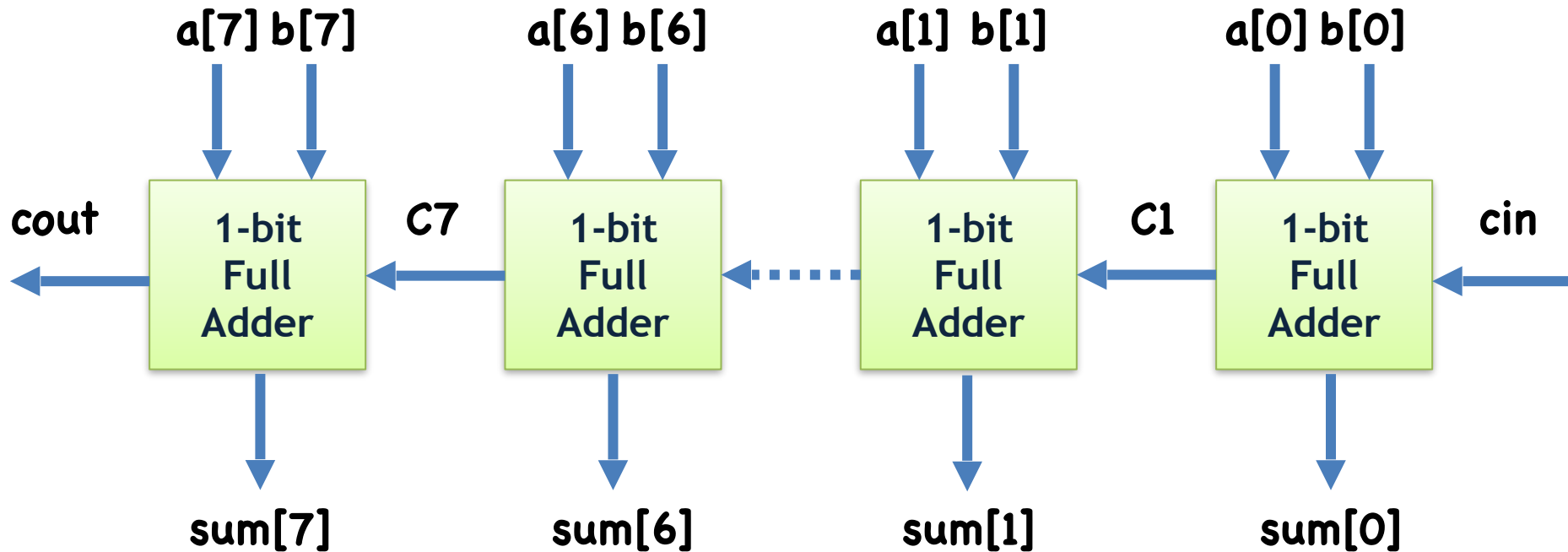


# Advanced Questions

- Group assignment
- Verilog questions (due on 10/14/2021 (Thu). 23:59:59.)
  - (Gate Level) 8-bit ripple carry adder (RCA)
  - (Gate Level) Decode and execute
  - (Gate Level) 8-bit carry-lookahead (CLA) Adder
  - (Gate Level) 4-bit multiplier
  - (Gate-level) An exhausted testbench design
- FPGA demonstration (due on 10/14/2021. In class.)
  - (Gate Level) Decode and execute

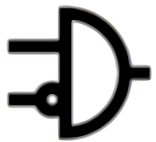
# Verilog Advanced Question 1

- (Gate-level) 8-bit ripple-carry adder (RCA)
- Instantiate the 1-bit full adder module from the Basic Question 3



# Verilog Advanced Question 2

- (Gate Level) Decode and execute
  - Please use the universal gate depicted on the bottom left corner only to implement the basic logic gates listed below.
    - Please draw your circuits of your basic logic gates (AND, OR, NOT ...) in your report
    - Implement your universal gate in Universal\_Gate.v and instantiate it in your design, do not submit this file and ensure that your design uses no primitive logic gates.
  - Use your own basic logic gate modules to realize the following functions specified in the table defined on the bottom-right corner
  - Input/Output: rs (4 bits), rt (4 bits), sel (3 bits), rd (4 bits)

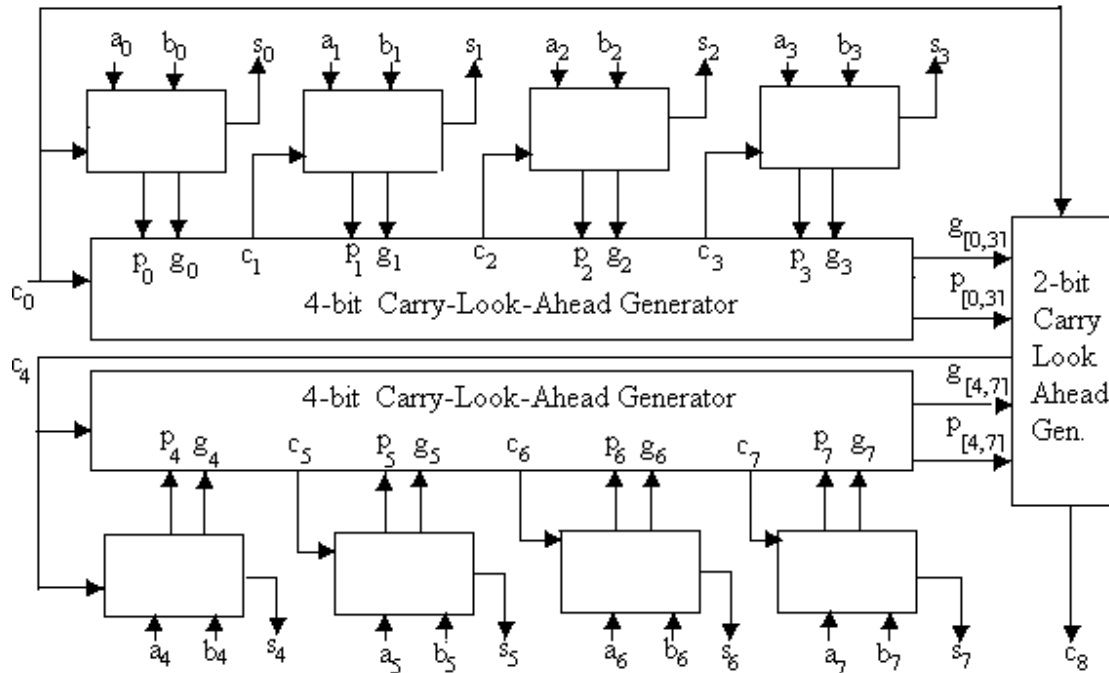


The universal gate  
to be used

Instruction	OP_Code	Function
ADD	000	$rd = rs + rt$
SUB	001	$rd = rs - rt$ (hint: two's complement)
BITWISE AND	010	$rd = rs$ (bitwise AND) $rt$
BITWISE OR	011	$rd = rs$ (bitwise OR) $rt$
RS CIR. LEFT SHIFT	100	$rd = \{rs[2:0], rs[3]\}$
RT ARI. RIGHT SHIFT	101	$rd = \{rt[3], rt[3:1]\}$
COMPARE EQ	110	$rd = \{3'b111, rs == rt\}$
COMPARE GT	111	$rd = \{3'b101, rs > rt\}$

# Verilog Advanced Question 3

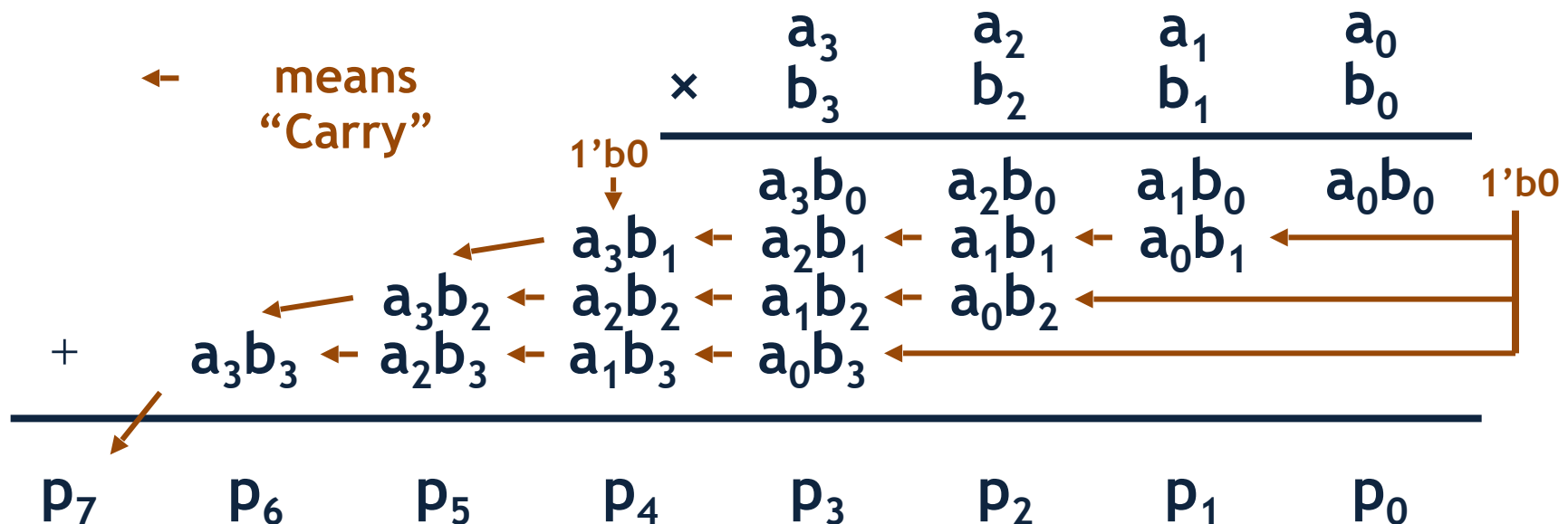
- (Gate Level) 8-bit carry-lookahead (CLA) adder
  - Using **NAND** gates only
  - Please design your CLA using **hierarchical modules**
  - Please explain **the circuit of CLA**, the **benefits of it**, and **how it works in your report**
  - Please draw your 4-bit CLA generator design **in your report**
- Go to Wikipedia to check out the details of it
  - [https://en.wikipedia.org/wiki/Carry-lookahead\\_adder](https://en.wikipedia.org/wiki/Carry-lookahead_adder)



- **Adder inputs:**
  - The operands:  $[7:0]$   $a$  (8 bits),  $[7:0]$   $b$  (8 bits)
  - The carry in:  $c_0$  (1 bit)
- **Adder outputs:**
  - The sum:  $[7:0]$   $s$  (8 bits)
  - The carry out:  $c_8$  (1 bit)

# Verilog Advanced Question 4

- (Gate Level) 4-bit multiplier
  - Design a 4-bit unsigned multiplier using **your full adder and half adder**
  - Using **NAND** gates only
  - Please explain how it works
  - Please draw your block diagram using your **adders** and **logic gates**
- **Inputs:**  $a[3:0]$  and  $b[3:0]$ ; **Output:**  $p[7:0]$





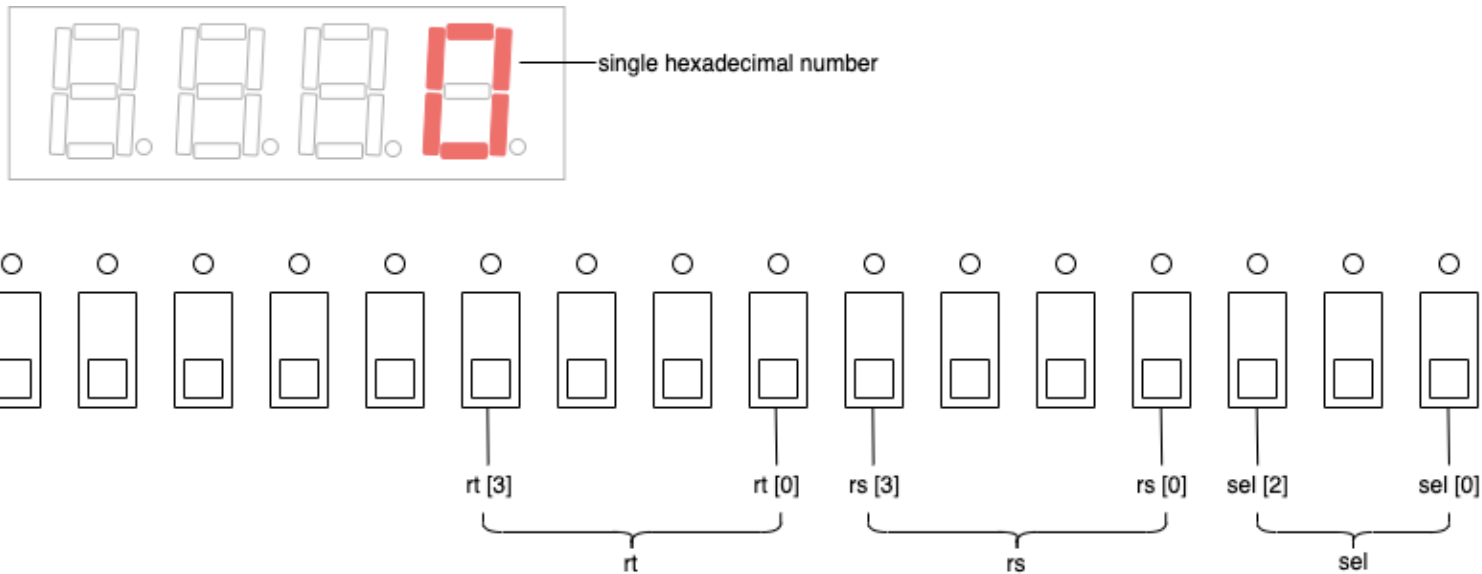
# Verilog Advanced Question 5

- (Test Bench) An exhausted testbench design
  - In this question, please design a testbench for a 4-bit adder circuit
  - We will use faulty designs to check if your test bench can find the intentionally inserted errors
  - We will check whether all the input patterns are covered
- Testbench requirements
  - Please follow the template for your test bench I/Os, which have two additional pins: **error** and **done**.
  - Please change input to the test instance every five nanoseconds.
  - One nanosecond after the inputs are given, set **error** to 1'b1 if an error is detected.
  - Set **done** to 1'b1 five nanoseconds after testing is finished.

# Advanced Questions

- Group assignment
- Verilog questions (due on 10/14/2021 (Thu). 23:59:59.)
  - (Gate Level) Decode and execute
  - (Gate Level) 8-bit carry-lookahead (CLA) Adder
  - (Gate Level) 4-bit multiplier
  - (Gate-level) An exhausted testbench design
- FPGA demonstration (due on 10/14/2021 (Thu). In class.)
  - (Gate Level) Decode and execute

# FPGA Demonstration 1



- (Gate Level) Decode and execute
- Implement the decode and execute module in **Advanced Question 2** onto your FPGA, and represent the output signal **rd** in a **single hexadecimal number**
- Please assign your inputs/outputs as:
  - **SW[2:0]** stands for '**sel**', **SW[6:3]** stands for '**rs**', **SW[10:7]** stands for '**rt**'
  - Use the **rightmost 7-segment display** to show your **rd**



# Thank you for your attention!



\*Yosemite Valley view taken at Glacier Point, Yosemite National Park, CA.  
This picture is taken by Chun-Yi Lee himself, who is also a fan of photography