Lab Review

10/12/2021

Lab1 & Lab2 Basic

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Agenda

Lab1 Issues

Lab2 Basic Issues

Grading

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Lab1 Issues

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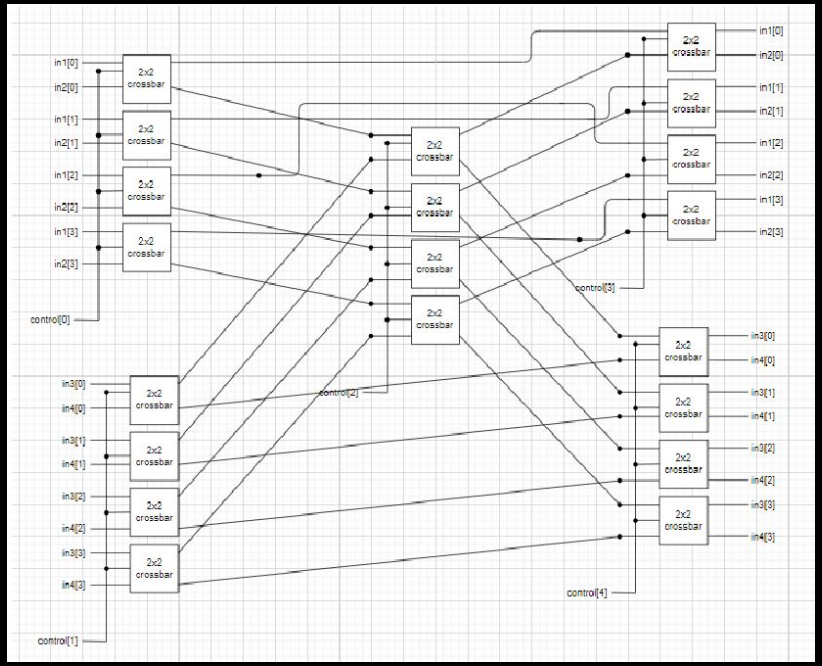
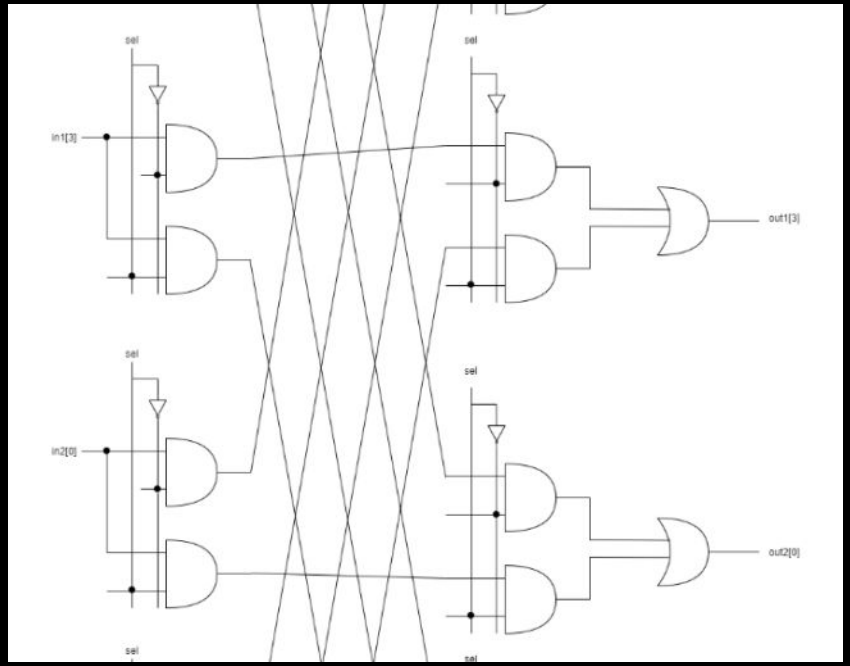
Lab1 Issues (1/3) - Schematic Graphs

- No open circuit.
- No Diagnal running wires - wires should have 90 degree turns.
- Please export the graph, don’t just take screenshots.
- Do **not** paste TA’s picture in the report, draw it on yourself.

Lab1 Issues (1/3) - Schematic Graphs





Lab1 Issues (2/3) - Terminology

- Modules are “instantiated”, not “called”.
- Wires are just conducting wires, they can’t “store” any signal.
- Module inputs are not “argument”, since module isn’t function.

  They are input signals.

Lab1 Issues (3/3) - Other Report Related

- Do **not** paste all your code.
- Remember to explain your design. Don’t just paste pictures to us.
- Clear & Detailed. There is no ambiguity in your description.
- Please organize your report by separating it into sections of different lab questions.

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Lab2 Basic Issues (1/1)

- Do **not** flatten your code!
- Declare your internal signal first.
- Meaningless signal name is not preferable.

```
nand and12(o2,ab5,ab5);
wire nabc5,nabc6;
nand and13(nabc5,na,sel[1],nc);
nand and14(nabc6,nabc5,nabc5);
wire ab6,ab7,ab8;
nand or1(ab6,a,a);
nand or2(ab7,b,b);
nand or3(ab8,ab6,ab7);
wire fin2;
nand and15(fin2,ab8,nabc6);
nand and16(o3,fin2,fin2);

wire nabc7,nabc8;
nand and17(nabc7,sel[0],sel[1],nc);
nand and18(nabc8,nabc7,nabc7);
wire ab9,ab10,ab11,ab12;
nand nor1(ab9,a,a);
nand nor2(ab10,b,b);
nand nor3(ab11,ab9,ab10);
nand nor4(ab12,ab11,ab11);
wire fin3;
nand and19(fin3,ab12,nabc8);
nand and20(o4,fin3,fin3);

wire nabc9,nabc10;
nand and21(nabc9,na,nb,sel[2]);
nand and22(nabc10,nabc9,nabc9);
wire ab13,ab14,ab15,ab16,a17;
```

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- Advanced Question Code: 10% each
- Report: 10% for each question (A1, A2, A3, A4, FPGA)
- FPGA Demo: 5%
- What have you learned: 5%

Q&A