Technical Article

Learn Analog Circuits: Types and Applications of Current Mirrors

April 03, 2019 by [Dr. Sergio Franco]

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Learn more about analog design in this introduction to the current mirror, including how this circuit is implemented in analog ICs.

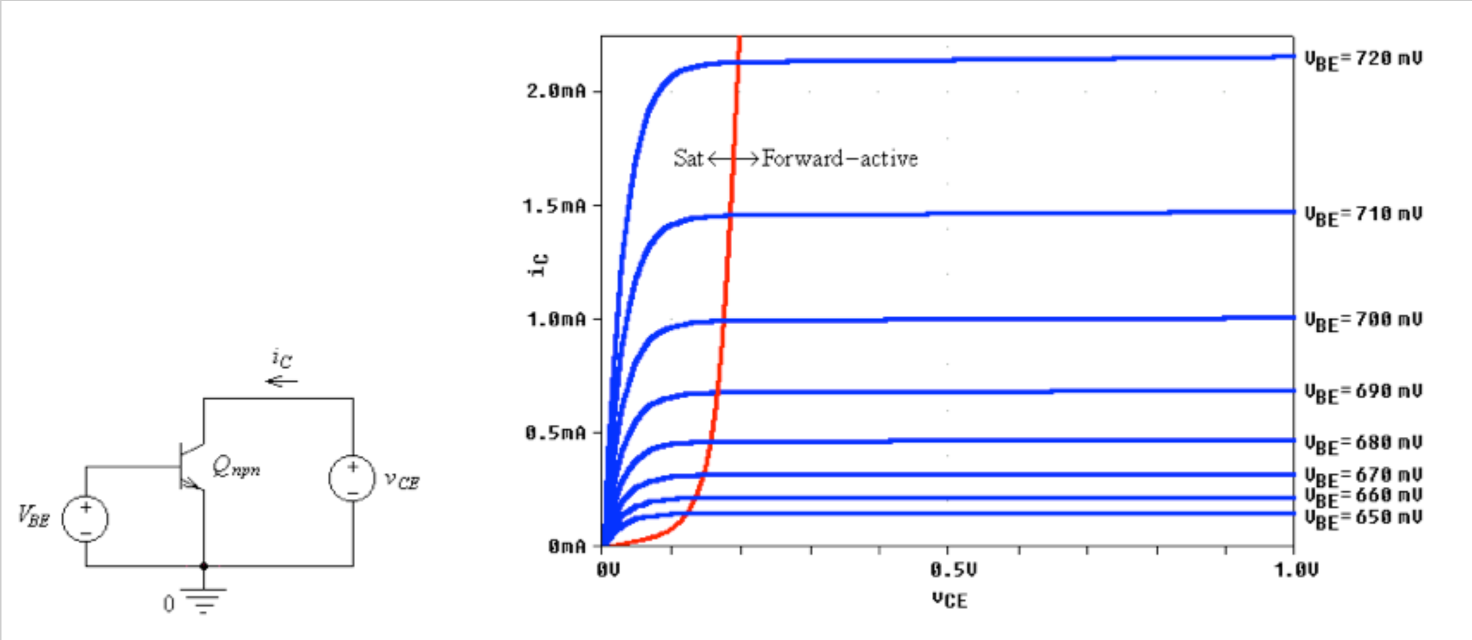
The current mirror is an important analog building block that finds application in such diverse areas as DC biasing and current-mode signal processing. This block comes in various incarnations, which we will investigate below:

- Basic mirror
- Mirror with beta helper
- Widlar current source
- Wilson mirror

We'll begin by looking at some basic characteristics of a bipolar junction transistor (BJT).

Background: BJT Characteristics

To set the background, consider Figure *1*, which shows the i_C-v_{CE} characteristics of an *NPN* BJT for different base-emitter voltage drives V_{BE}.



(a) *(b)*

Figure 1. Using PSpice to display the i_C-v_{CE} characteristics of an NPN BJT. For $v_{CE} < 0.2$ V the BJT is in saturation (Sat), whereas for $v_{CE} \geq 0.2$ V it is operating in the forward-active (FA) region.

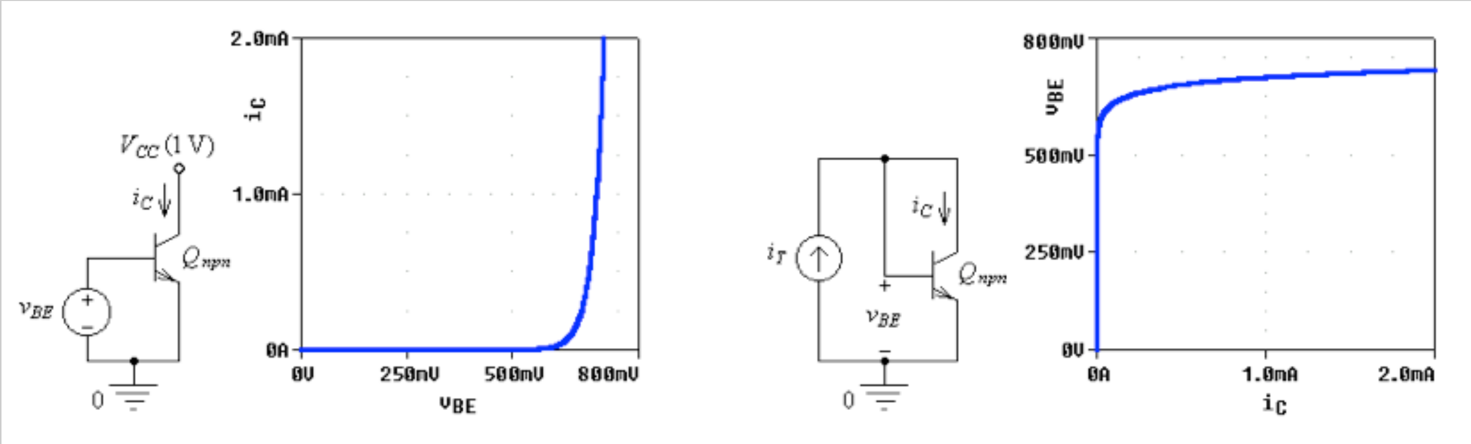
We observe that, for $v_{CE} \geq 0.2$ V, all curves are essentially flat, indicating the BJT's ability to sink current independently of the collector voltage (so long as this voltage is prevented from dropping below about 0.2 V). Even though V_{BE} is incremented in equal 10 mV steps, i_C increases in geometric fashion. In fact, in the forward-active (FA) region, i_C is related to v_{BE} exponentially as

$$i_C = I_s e^{v_{BE}/V_T}$$

Equation 1

where I_s is a scaling factor called the *saturation current*, and V_T is another scaling factor called the *thermal voltage* because it is proportional to absolute temperature T. For a low-power BJT, I_s is typically in the femtoampere range (1 fA = 10^{-15} A).

Moreover, V_T = 26 mV at room temperature. Figure *2a* shows the PSpice plot of Equation (1) for a BJT with I_s = 2 fA (this value has been chosen so that with v_{BE} = 700 mV the BJT gives exactly i_C = 1.0 mA).



(a) ***(b)***

Figure 2. Using PSpice to plot (a) i_C vs. v_{BE} and (b) v_{BE} vs. i_C.

The inverse of Equation (1) is

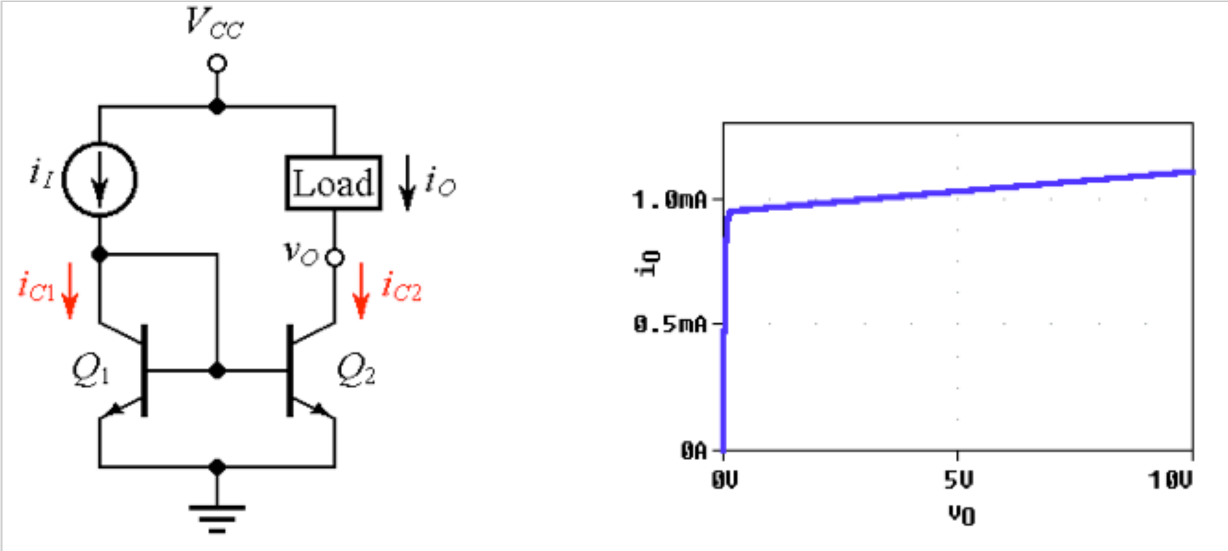
$$v_{BE} = V_T \ln(i_C / I_s)$$

Equation 2

To plot v_{BE} as a function of i_C via PSpice, we connect the base and collector terminals together to operate the BJT in what is called the *diode mode*, and then we apply a test current i_T, as shown in Figure *2b*.

Basic Current Mirror

The basic mirror, shown in Figure *3a*, consists of a pair of *matched* BJTs fabricated (or mounted) in close proximity to each other so that their characteristics (I_s and V_T) *track* each other with temperature and time.



(a) *(b)*

Figure 3. (a) Basic current mirror, and (b) its i_O vs. v_O characteristic for i_I = 1 mA and V_{CC} = 10 V.

Assuming negligible base currents, we note that diode-connected Q_1 responds to the input current i_I by developing a voltage drop v_{BE} according to Equation (2) shown above.

Since Q_2 is experiencing the *same* v_{BE} as Q_1, we must have $i_{C2} = i_{C1}$, by Equation (1), so Q_2 *mirrors* Q_1. Assuming negligible base currents, we thus have $i_O = i_I$.

Compared to Figure *1b*, the expanded view of Figure *3b* indicates that the curve in the FA region exhibits a nonzero slope. This stems from the so-called *Early Effect* [1], as a consequence of which the projections of all curves meet at a common point on the negative axis called the *Early Voltage* V_A, as shown in Figure 4.

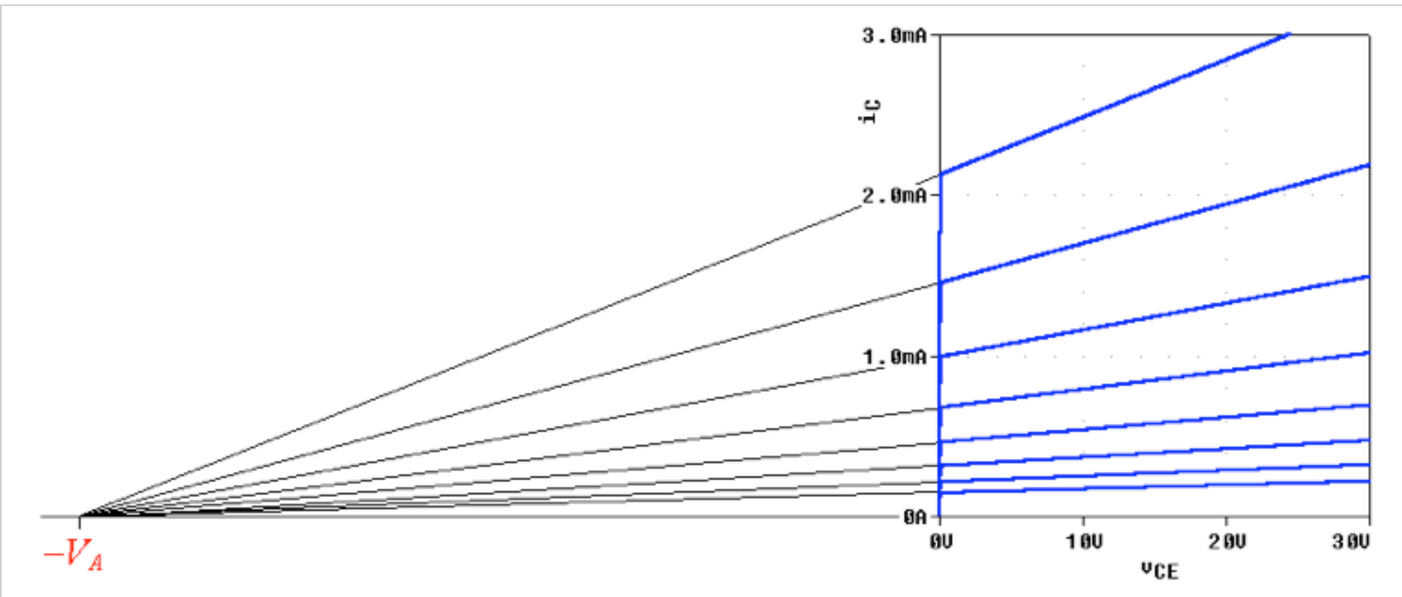


Figure 4. Expanded view of Figure 1b, illustrating the consequences of the Early Effect.

The slope of an i_C curve in the FA region is denoted as $1/r_o$, the reciprocal of resistance. Applying simple geometric reasoning to Figure 4, we have the slope (= $1/r_o$) ≈ I_C / V_A, or

$$r_o \cong \frac{V_A}{I_C}$$

Equation 3

where I_C represents the current at the left edge of the FA region.

The PSpice example shown uses V_A = 60 V, so for I_C = 1 mA we have $r_o \approx 60/10^{-3}$ = 60 kΩ. This means that the Norton equivalent seen by the load is a 1 mA current sink with a parallel resistance of 60 kΩ. For every volt increase in v_O, r_o is responsible for an increase in i_O of (1 V)/(60 kΩ) = 16.7 μA.

Current Mirror with Beta Helper

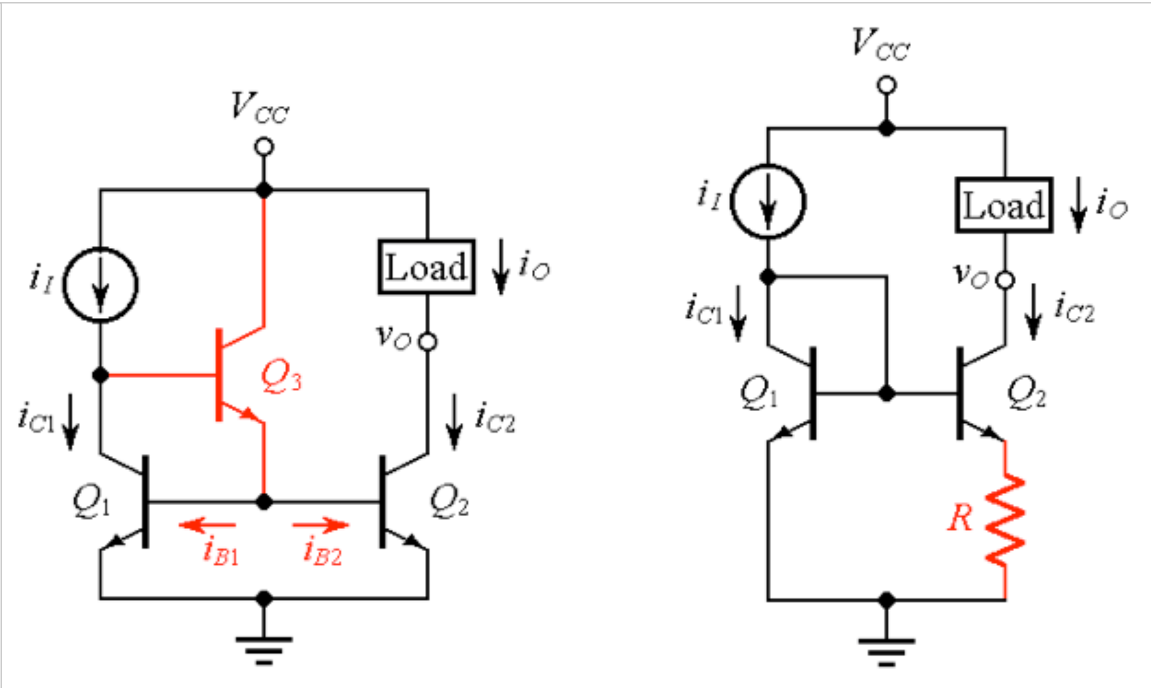
We now wish to take a closer look at the base currents of the basic mirror of Figure *3a*. It is well known that a BJT's base current i_B is related to the collector current i_C as $i_B = i_C / \beta$, where β is the BJT's *current gain*. Typically, $\beta \approx 100$, though integrated-circuit BJTs may have $\beta \approx 250$. With reference to Figure *3a*, KCL at Q_1's collector node implies $i_I = i_{C1} + i_{B1}$ +

$i_{B2} \approx i_{C1} + 2i_{B1} = i_{C1} + 2i_{C1}/\beta = i_{C1}(1 + 2/\beta)$, or

$$i_{C1} \cong \frac{i_I}{1+2/\beta} \cong i_I\left(1-\frac{2}{\beta}\right)$$

Equation 4

indicating that i_{C1} (and hence i_{C2}, by mirror action) will be a bit *less* than i_I. For instance, with $\beta = 100$, i_{C1} and thus also i_O ($= i_{C2} = i_{C1}$) will be about 98% of i_I. Should this error be intolerable, we can enlist the help of a third BJT Q_3 to supply i_{B1} and i_{B2} in the manner of Figure *5a*.



(a) ***(b)***

Figure 5. (a) Current mirror with beta helper, and (b) Widlar current source.

This reduces the error current at Q_1's collector node by a factor of about β, so Equation (4) still holds, but with β replaced by β^2.

Widlar Current Source

In DC biasing applications it is often necessary to synthesize a current $i_O << i_I$. The circuit of Figure *5b*, named for its inventor Bob Widlar, achieves this goal by means of a resistor R in *series* with Q_2 to reduce Q_2's base-emitter voltage drop as

$$v_{BE2} = v_{BE1} - Ri_O$$

Equation 5

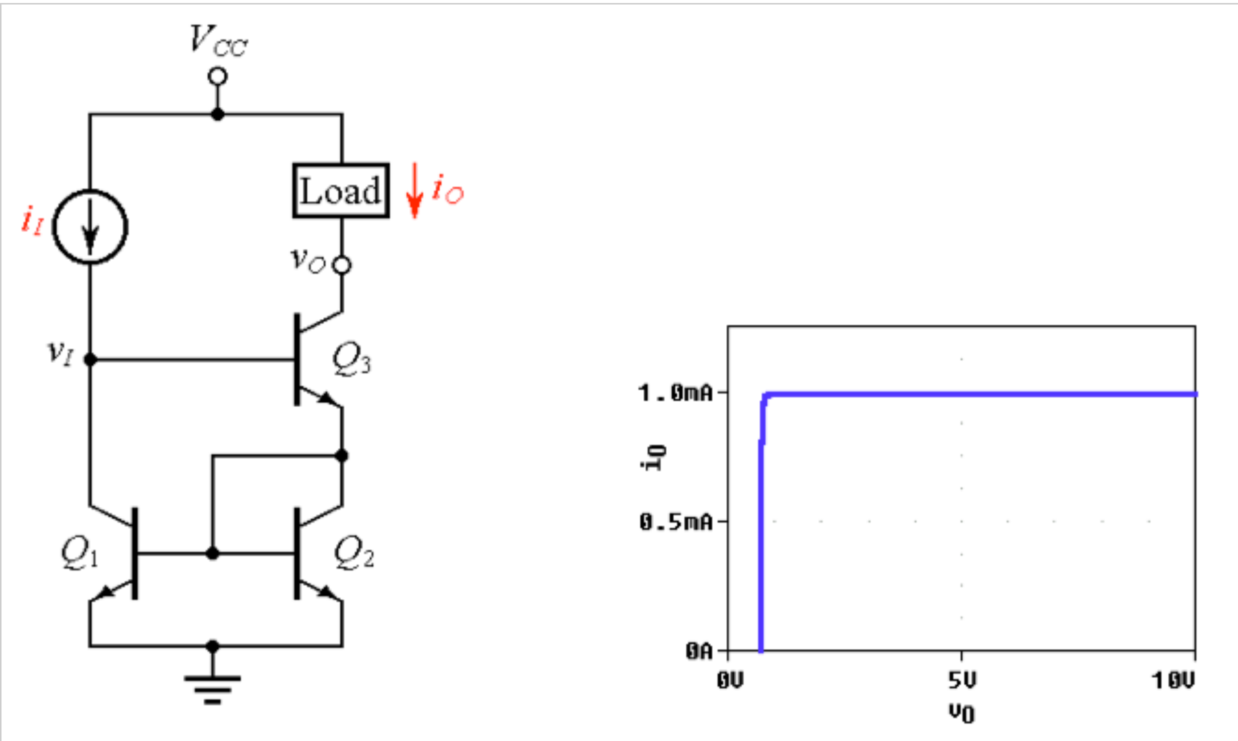
In this connection, it helps to remember the following *rules of thumb* so dear to practicing engineers:

- To raise (lower) i_C by an *octave*, you need to raise (lower) v_{BE} by 18 mV (because $e^{\pm 18/26} \approx 2^{\pm 1}$).
- To raise (lower) i_C by a *decade*, you need to raise (lower) v_{BE} by 60 mV (because $e^{\pm 60/26} \approx 10^{\pm 1}$).

As an example, suppose we have i_I = 1 mA (= 1,000 μA) and we want i_O = 20 μA. We can think of 20 as the result of dividing 1,000 by 10 to get 100, dividing 100 by 10 to get 10, and then multiplying 10 by 2 to get 20. So, R must drop (60 + 60 –18) mV = 102 mV. Then, R = (102 mV)/(20 μA) = 5.1 kΩ.

Wilson Current Mirror

There are applications in which it is desirable that a current mirror (*a*) be exempt from the beta-error of Equation (4), and (*b*) exhibit a much higher output resistance than the r_o of Equation (3), so that it can closely approximate an *ideal current source* or *sink*. The mirror of Figure *6a*, named for its inventor G. R. Wilson, achieves both objectives with just one additional transistor Q_3 (two birds with one stone). This elegant circuit can be analyzed systematically [1], but here we shall limit ourselves to an intuitive discussion.



(a) ***(b)***

Figure 6. (a) Wilson current mirror, and (b) its i_O vs. v_O characteristic for i_I = 1 mA and V_{CC} = 10 V.

We note that Q_3 carries the same current as Q_2 because they are in series, and Q_1, in turn, mirrors the current of Q_2, so, the left and right halves of the circuit carry *identical* currents. This is corroborated by the fact the Q_3 draws its base current from the left half, whereas Q_1 draws its base current from the right half, in a give-and-take fashion. (A systematic analysis [1] predicts an error of the type of the beta helper.)

Now, if we attempt to raise v_O by, say, 1 V, the Early Effect would cause i_{C3} to increase by (1 V)/r_o. This would cause an increase in v_{BE2}, by Equation (2), and this, in turn, would cause an increase in i_{C1}, by Equation (1). Having become a bit more conductive, Q_1 would be letting less base current into Q_3, forcing the latter to conduct a bit less. In words, any attempt to raise i_{C3} is met by a reaction that tends to nullify such an attempt. In fact, this is negative feedback! (A systematic analysis [1] predicts a Norton resistance of about $\beta r_o/2$.) The flatness of the i_O curve of Figure *6b* confirms the excellent characteristic of the Wilson mirror!

Current Mirrors at Work

It can be fun to look at integrated-circuit schematics and identify the presence and purpose of current mirrors (CMs). For instance, turning to the 741 op-amp of Figure 7, we identify the following CMs:

- The trio Q_5 - Q_6 - Q_7 is a basic CM with beta helper. This CM forms an *active load* for the differential input stage made up of the left half (Q_1 - Q_3) and right half (Q_2 - Q_4). Ideally, the two halves should be perfectly matched, but in practice there may be some mismatch, resulting in an input offset voltage V_{OS}. The emitters of Q_5 and Q_6 are equipped with 1 kΩ resistors to allow for the creation of an externally induced imbalance equal but opposite to the imbalance of the left and right halves, so as to null V_{OS}. (For the procedure to null the offset voltage V_{OS}, please refer to the fifth figure of this page in the AAC textbook.)
- The pair Q_{10} - Q_{11} is a Widlar current sink. The bias current for diode-connected Q_{11} is established by R_5, which is actually a dual-purpose component because it also biases diode-connected Q_{12}.
- The basic CM Q_{12} - Q_{13} is designed to source *two* currents independently, one to provide an *active load* function for common-emitter amplifier Q_{17}, and the other to *bias* the circuitry of the output stage. The current entering Q_{13}'s emitter is steered separately by Q_{13}'s two collectors, in percentages determined by the collector areas.
- The pair Q_8 - Q_9 forms yet another basic CM, which, in connection with the Widlar sink Q_{10} - Q_{11}, is designed to provide the DC bias current for the two halves of the input stage.
- Can you identify other CMs? Yes indeed, it's the pair Q_{23} - Q_{24}. Under normal operating conditions, these BJTs are off because Q_{21} is off. However, should an overload condition arise at the output, Q_{21} will go on, turning on also Q_{24}. By mirror action, Q_{23} will go on and starve Q_{16} of base current to limit the power dissipated by the output stage.

Figure 7. Circuit schematic of the 741 op-amp (courtesy of Fairchild Semiconductor Corporation).

Next, let us look at the CFA of Figure 8.

Figure 8. Circuit schematic of a current-feedback amplifier (CFA).

This circuit uses a pair of Wilson CMs, Q_5 - Q_6 - Q_7 and Q_8 - Q_9 - Q_{10}, to replicate, respectively, the collector currents of Q_1 and Q_2 and provide their difference at the common base terminals of Q_{13} and Q_{14}. In a way, the upper CM acts as an *active load* for the lower CM, just as the lower CM acts as an active load for the upper CM. Furthermore, the DC biasing circuitry consists of the current sources I_3 and I_{13}, and the current sinks I_4 and I_{14}, which are shown in symbolic form for simplicity. But, if we were to look at a more detailed schematic, we would find that also these sources and sinks are implemented in CM form.

Conclusion

This article briefly reviewed BJT operation, then it explored four types of BJT current mirrors: the basic mirror, the mirror with beta helper, the Widlar current source, and the Wilson mirror. In the final section, we saw some examples of how current mirrors are incorporated into analog integrated circuits.

Current mirrors can also be implemented using CMOS technology. AAC's article entitled [The Basic MOSFET Constant-Current Source]() is a good place to start if you want to learn about the CMOS version of the current mirror.

References

[1] http://online.sfsu.edu/sfranco/BookAnalog/AnalogJacket.pdf

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