Using Pspice to analyze amplifier loop stability (Part 1 of 2)

planetanalog.com/using-pspice-to-analyze-amplifier-loop-stability-part-1-of-2/

Planet Analog January 8, 2011

PLANET ANALOG

Abstract

While it may be relatively straight forward to look over a simple amplifier, at relatively lower frequencies, to determine its stability, the task of evaluating the stability (or lack thereof) of a more-complicated circuit configuration may be significantly more challenging. This article uses readily available Pspice Macromodels in conjunction with simple circuit techniques to enhance the designer's ability to ensure that his designs are functional and stable.

What makes an amplifier unstable?

A closed-loop system is stable as long as loop gain does not turn into positive feedback at any frequency that matters. Loop gain is a phasor (which means it has both magnitude *and* phase properties); the most common culprit for instability is additional phase shift around the loop turning a perfectly good negative feedback into a positive one. What constitutes a frequency where the loop gain phase “matters” is where loop gain is 0dB or above.

Looking at the amplifier circuit shown in **Figure 1** , one could estimate how stable it is by determining the phase shift encountered when the signal goes around the loop one time, while the loop is broken. The following example demonstrates one way this can be accomplished by using simulation software, Op Amp Macromodel, and employing the ideal components offered in Pspice.

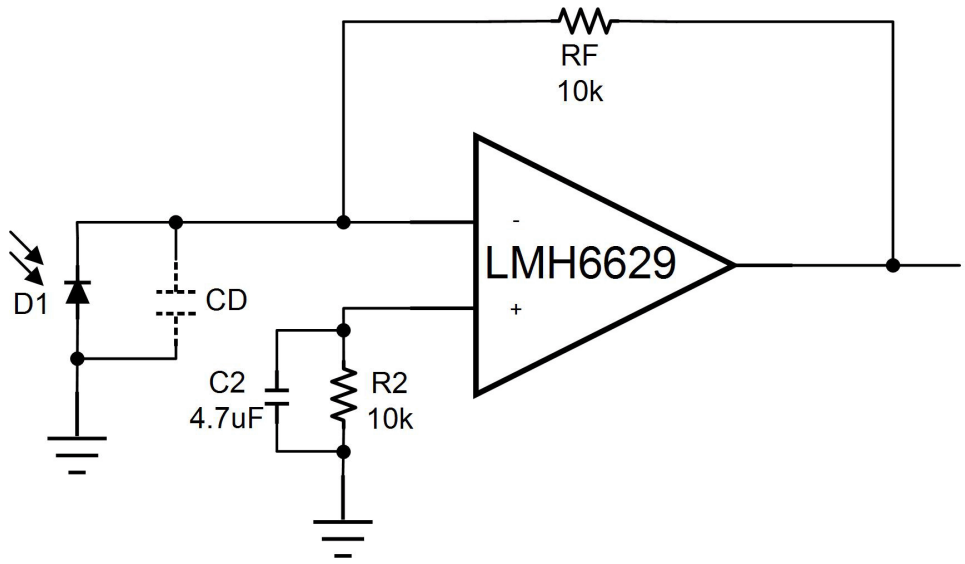

Figure 1: Transimpedance Amplifier

High-speed low-noise transimpedance amplifier (TIA) stability example:

Let's use a transimpedance amplifier (TIA) as an example and explore its stability to demonstrate the technique we are about to propose. TIA's have many industrial and consumer uses, such as LIDAR (Light Detection And Ranging), barcode scanner, factory automation, etc. Some of the challenges facing the designer are to maximize SNR and to achieve the speed/bandwidth necessary to pass the intended signal without attenuation or degradation.

Figure 1 is one such design using the LMH6629, a very high-speed (GBWP= 4GHz) low-noise device (0.69nV/rtHz) with a minimum stable gain of +10V/V (with COMP pin tied to VCC). The LMH6629's compensation (COMP) input can be tied to VEE to lower the minimum stable gain to 4V/V. For maximum slew rate and bandwidth (small and large signal), in this example the COMP pin is tied to VCC. The attainable bandwidth is directly related to the amplifier GBWP and inversely proportional to the Transimpedance gain (R_F) and the photodiode inherent parasitic capacitance.

A convenient method of deciding what feedback resistor (R_F) to use for a given amplifier is to refer to the plot of **Figure 2** , where the total equivalent input current noise density "i_{ni} " is plotted against R_F when using the LMH6629. In this plot, "i_n " is the LMH6629 input noise current, "e_n " is the LMH6629 input noise voltage, "k" is the Boltzmann constant, and "T" is absolute temperature in ºC.

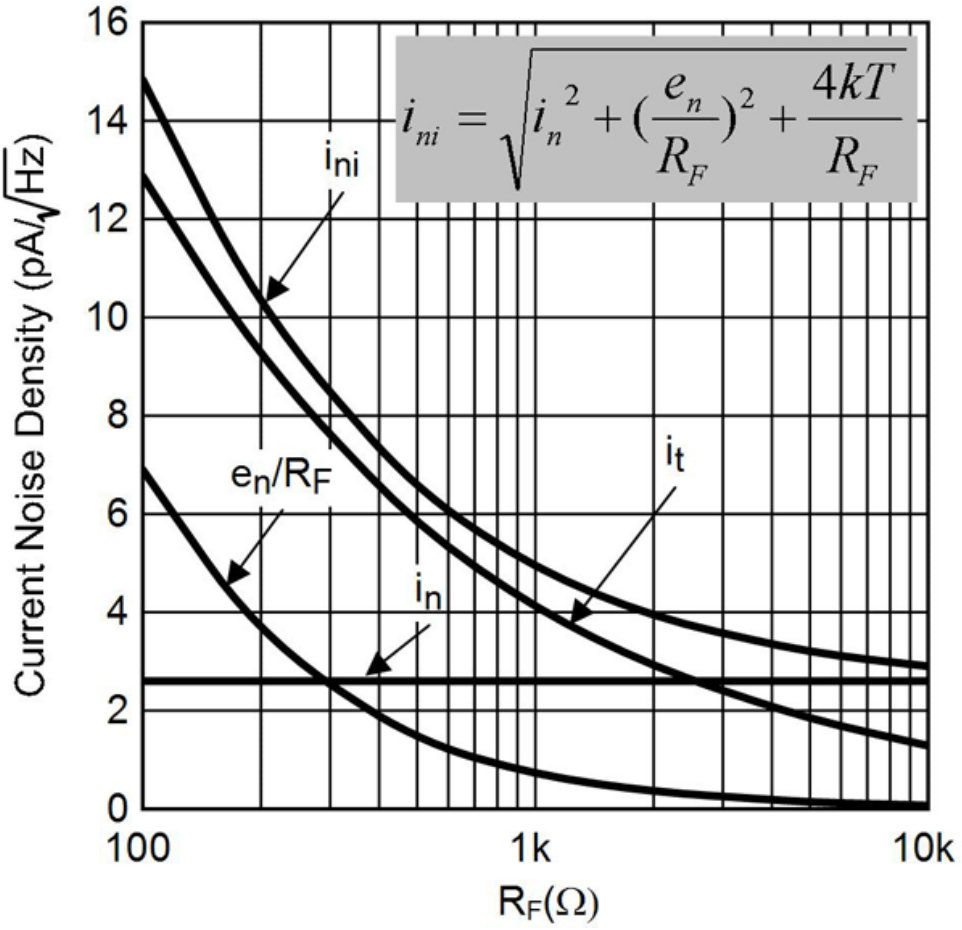

Figure 2: Total Equivalent Noise Density vs. Feedback Resistance

As evident from Figure 2, for the LMH6629, setting R_F to 10k W ensures the minimum total equivalent input current noise density, i_{ni} , and thus the highest SNR. Any further increase in R_F reduces the attainable speed with no discernable improvement in SNR.

A major factor which makes stability analysis complicated for a seemingly simple circuit is the effect of parasitic components. In the circuit of Figure 1, there is very little that hints that the circuit may be close to instability. The parasitic component "C_D " shown is the photodiode intrinsic capacitance which scales according to the photodiode area and its sensitivity. R2 is used to cancel the offset error due to the LMH6629's input bias current flow and C2 eliminates R2's noise.

Assuming a nominal photodiode capacitance (C_D) of 10pF, the simulated response of the circuit of Figure 1 is shown in **Figure 3** and is indicative that the circuit is unstable; this is evident by the large and sharp peaking in the frequency response. In the frequency domain, stability can be determined by knowing the phase margin (PM) of the circuit. For simulation purposes, the simplified equivalent circuit of a photodiode is a current source.

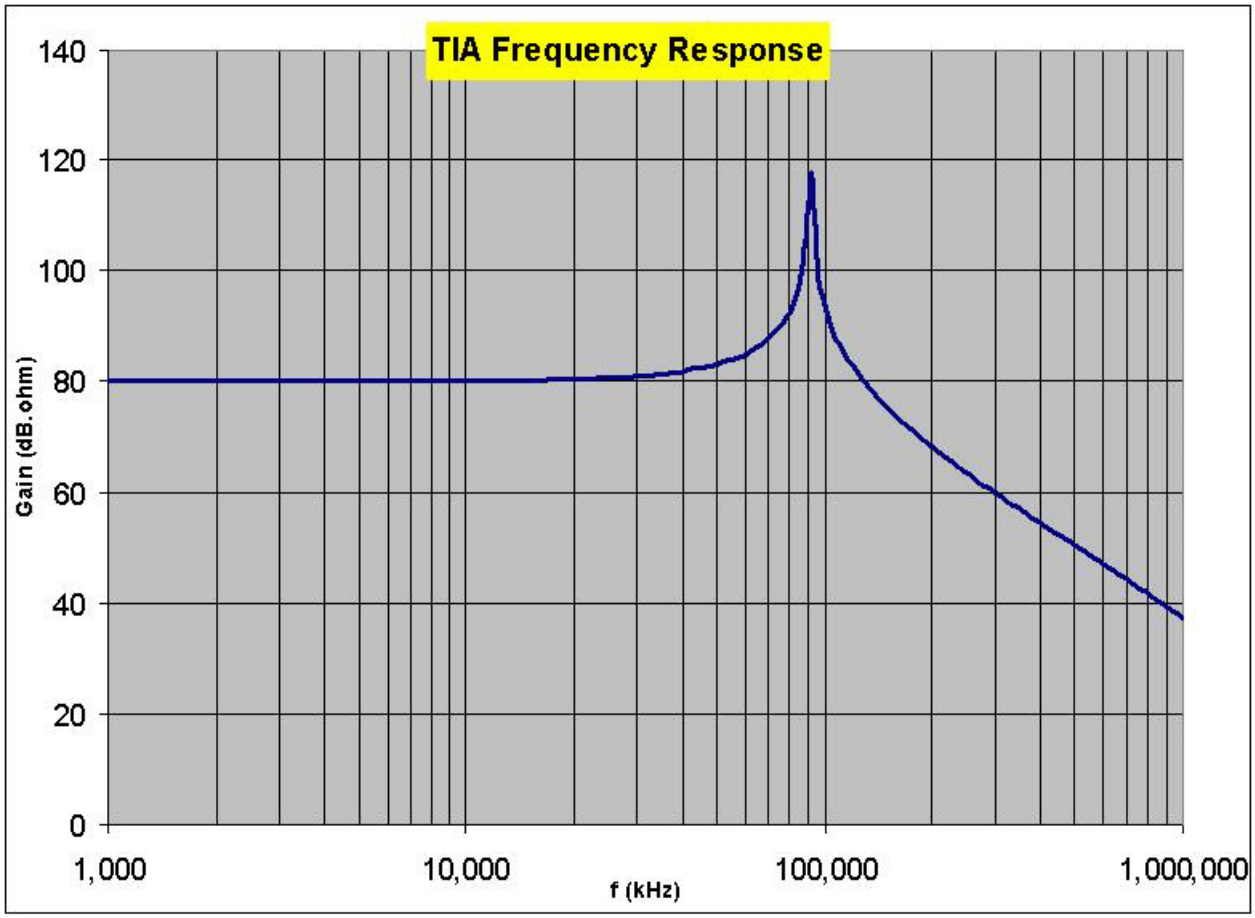

Figure 3 : TIA Frequency Response Indicates Instability

To an experienced user, the lack of stability with a relatively large feedback resistor, R_F , might be evidence that R_F "looking" into the parasitic capacitance of the inverting Op Amp input is the reason for ringing and overshoot. This can be called "excessive phase shift" around the loop. The inverting input parasitic capacitance is composed of the photodiode capacitance and the LMH6629's input capacitance. The LMH6629's wide bandwidth exacerbates the problem by lowering the total input capacitance that is enough to cause excessive phase shift. The most effective method in remedying the situation is to insert a capacitor (C_F) of proper value across R_F .

Barring a full blown pen-and-pencil analysis to look for the cause of low phase margin responsible for this behavior, one is left with little choice but trial and error in choosing compensation components to improve stability. A more rigorous method, which is considerably faster than the pen-and-pencil approach, is to use simulation to gain more insight about the loop behavior over frequency without the hassles of complex arithmetic and the possibilities of computation error.

What is needed is to be able to observe the circuit in "open loop" configuration so that the loop gain (LG) magnitude and phase can be studied. Simulation provides an opportunity to do just that since it arms the user with a variety of ideal components that can do the job effectively.

In the simulation circuit of **Figure 4** , the loop has been opened in terms of AC (where phase margin matters) while retaining the DC closed loop so that the operating point is properly established. This is accomplished by a large value series inductance (L1) and a large value shunt capacitor (C1) at the output.

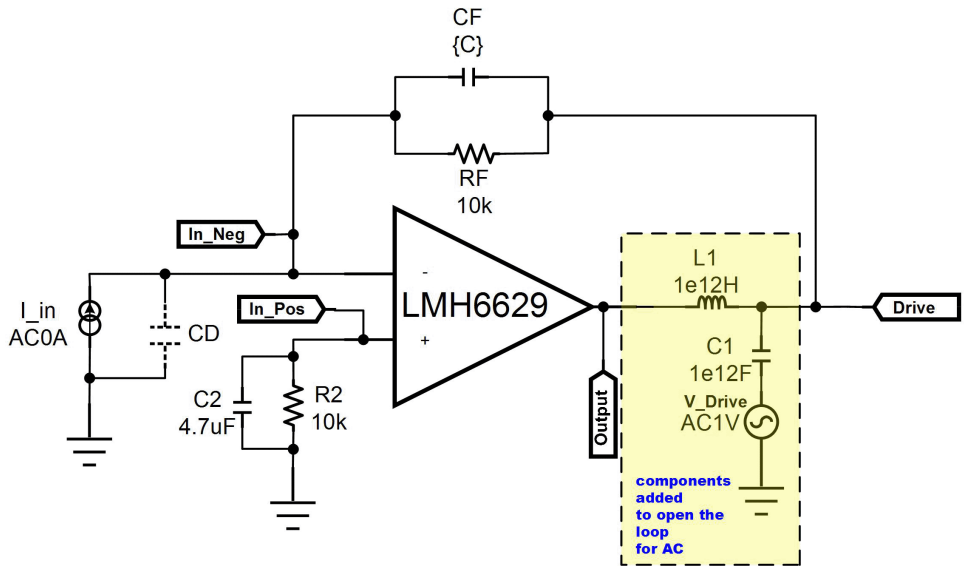

Figure 4 : Insert Large "L" and Large "C" to Open the Loop at AC for Simulation

The AC source driving the large capacitor (V_Drive) can be set to 1V and the simulated response at the device output is the LG function as shown in **Figure 5** .The low phase margin of ~0º in Figure 5 confirms the excessive closed loop frequency response peaking seen in Figure 3. A figure of merit used is that phase margin should be bigger than 45º for stability.

Notes:

1. Make sure the input current source (in place of the photodiode) is set to "AC 0" before starting the frequency response simulation

2. Results shown are with C_F set to 0pF

3. Magnitude is shown as solid line and phase angle as dashed line in Figure 5

4. Phase margin is the phase angle of the "LG Function" when it crosses 0dB

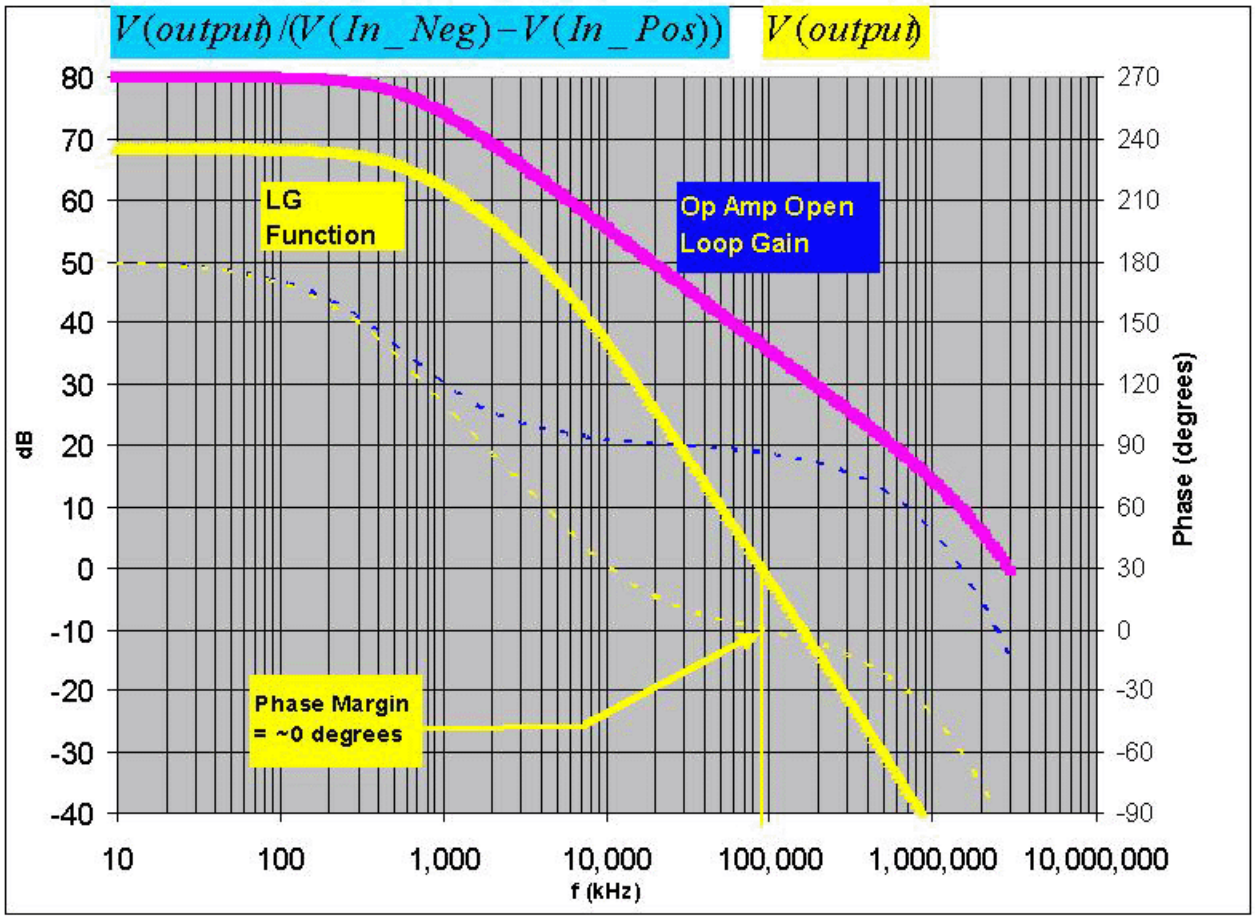

Figure 5 : Open Loop Plot Shows Insufficient Phase Margin

In an effort to find the proper compensation capacitor value to improve phase margin, one could plot Noise Gain for various values of C_F (in the circuit of Figure 4) along with the LMH6629 Open Loop Gain plot together, as shown in **Figure 6** . Noise Gain is V(Drive)/V(In_Neg). Note that the simulated low frequency value of LG is higher than 0dB; that's because the LMH6629's Macromodel also models its differential input resistance.

Most Pspice simulators allow the use of the ".STEP PARAM" statement shown in Figure 6 to run multiple simulations and display all results superimposed. Other simulators may have dedicated commands to allow this type of simultaneous simulations. The optimum C_F value is one which places a pole on the Noise Gain function at the frequency where it intercepts the LMH6629's Open Loop Gain plot. From Figure 6, that would be C_F = 0.25pF in this example.

Any higher C_F value, and there will be a bandwidth penalty and any lower value, there will not be enough phase margin. If C_F is high enough (e.g. 7pF in this example), the Noise Gain plot may intercept the Open Loop plot below 20dB, which is the minimum stable gain of the LMH6629; this situation would again be unstable or the amplifier could have excess frequency response peaking. So, there is a region of stability and an optimum value.

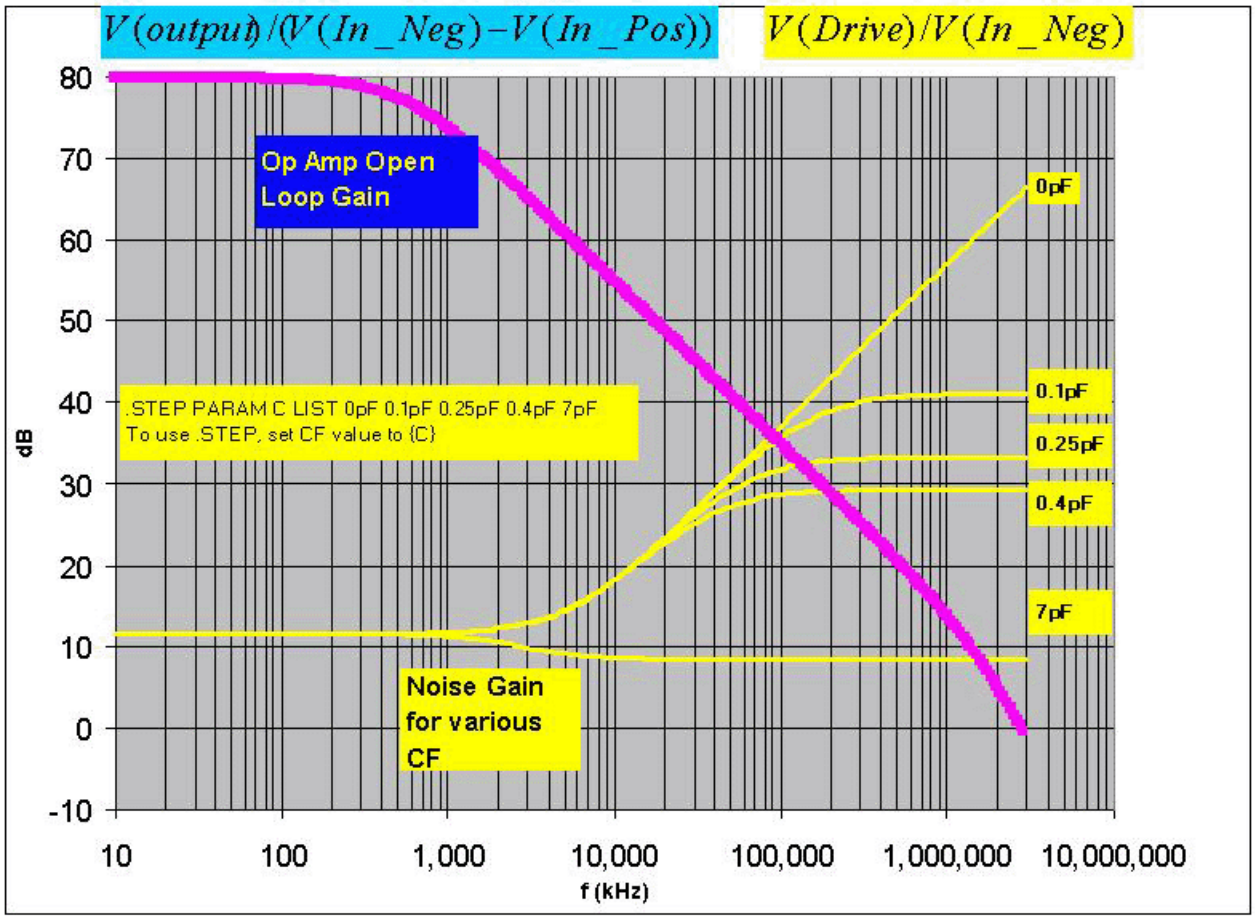

Figure 6 : Noise Gain Plots for C_F Optimization

Figure 7 shows the resulting plot of LG as a function of frequency with C_F =0.25pF to confirm that the Phase Margin has increased to 61º from the original 0º without C_F .

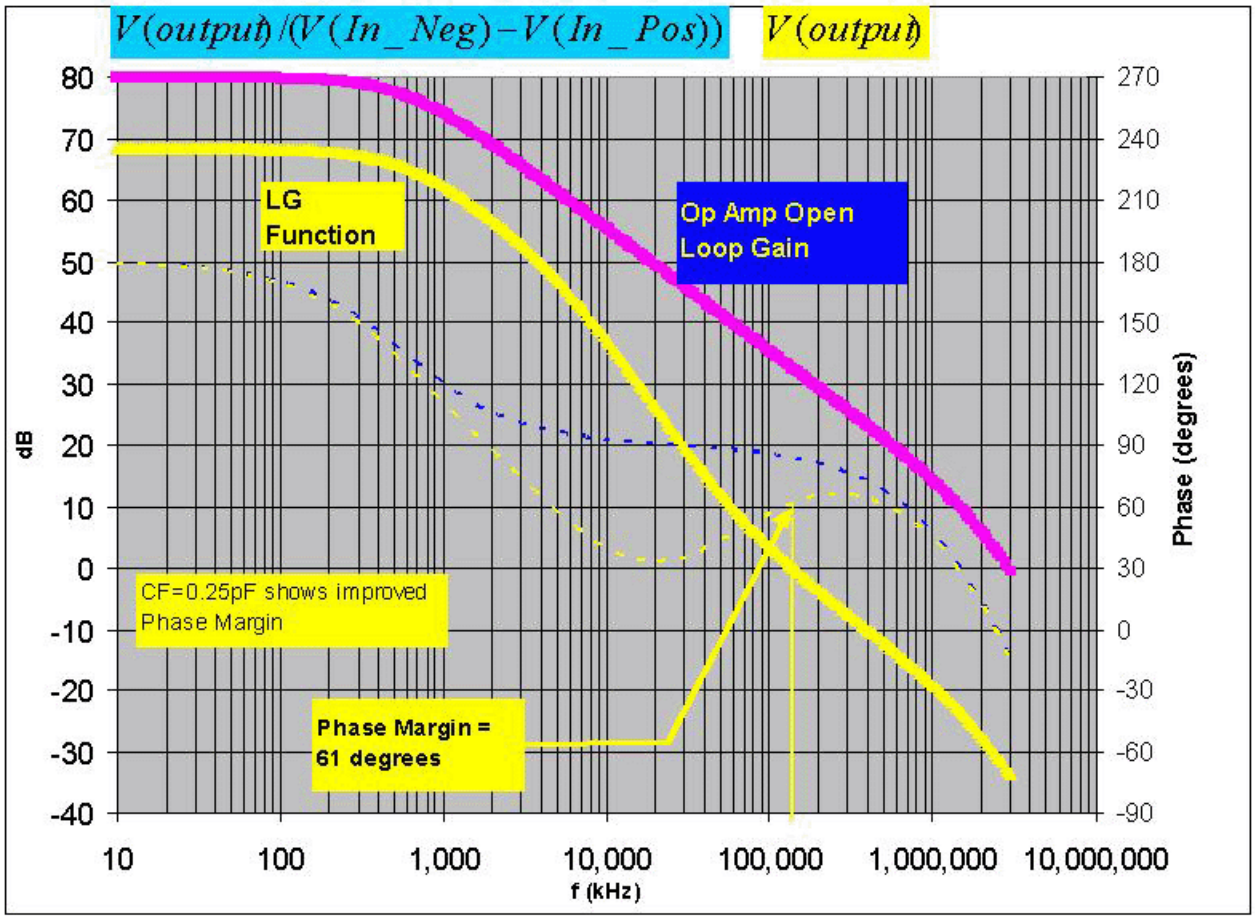

Figure 7 : Open Loop Plot to Confirm Phase Margin Improvement due to C_F

Having found the optimum value of C_F , one could go back to the original closed loop configuration (without the large L and C which were added to investigate LG and NG) and obtain the step response with optimum C_F value (0.25pF in this case) included. **Figure 8** is this plot for various C_F to confirm that either larger or smaller C_F values could be unstable or could have long ringing and settling times while optimum C_F results in a nice step response with minimal ringing.

Obviously, 0pF and 7pF are completely unstable. Not that the oscillation frequency with 7pF is much higher than that of 0pF due to the higher frequency of intercept between Noise Gain and amplifier open loop gain plot, as predicted by Figure 6.

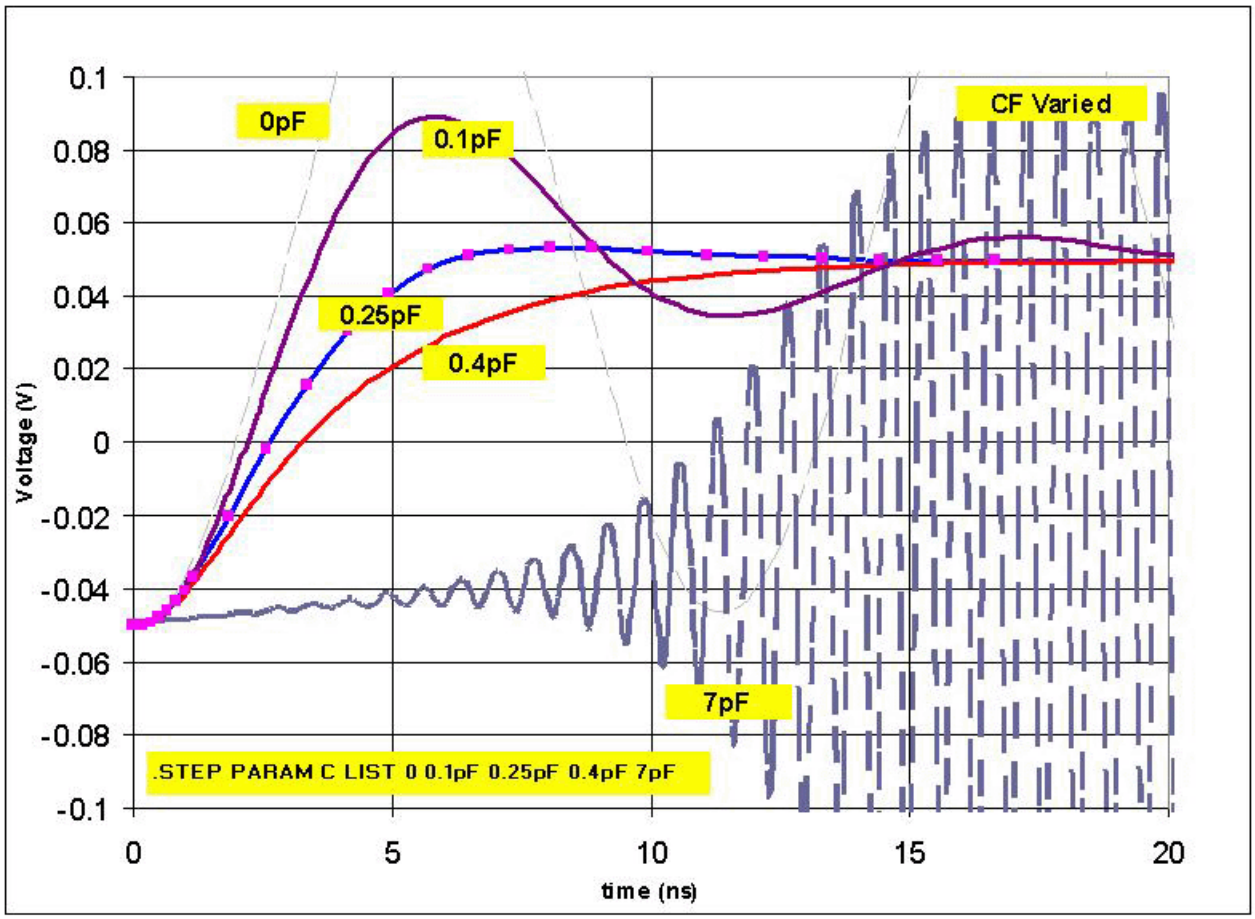

Figure 8 : Closed Loop Step Response for Various C_F

(End of *Part 1* ; *Part 2* will look at practical considerations and bench results comparison.)

About the author

Hooman Hashem i is an application engineer who joined National Semiconductor Corp in 1995. He has an MSEE from Santa Clara University (1989) and a BSEE from San Jose State University (1983). He currently works in National's High Speed Signal Path group.