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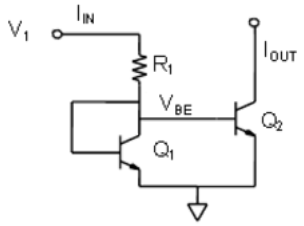
Chapter 11: The Current Mirror



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11.1 Basic principles

The implementation of the current mirror circuit may seem simple but there is a lot going on. The simple two transistor implementation of the current mirror is based on the fundamental relationsl that two equal size transistors at the same temperature with the same V_{GS} for a MOS or V_{BE} for a BJT have the same drain or collector current. To best understand this important circuit building block and how it makes use of this relationship we need to deconstruct the circuit into input and output sections and examine each in turn.

A current mirror is a circuit block which functions to produce a copy of the current flowing into or out of an input terminal by replicating the current in an output terminal. An important feature of current mirror is a relatively high output resistance which helps to keep the output current constant regardless of load conditions. Another feature of the current mirror is a relatively low input resist which helps to keep the input current constant regardless of drive conditions. The current being 'copied' can be, and often is, a varying signal current. The current mirror is often used to provide bia currents and active loads in amplifier stages.

The ideal block level concept of the current mirror is shown in figure 11.1. Given a current source as the input, the input section of the current mirror looks like a virtual short circuit and reflects (sw the direction of flow) this current to produce a current sink (the current exiting the mirror); as a result, we obtain a current sink (figure 11.1a). Conversely, given a current sink as the input, the currer mirror reflects this current to control current source (figure 11.1b); as a result, now we obtain a current source. We can generalize this basic current mirror structure with this first observation: A curr mirror consists of a low impedance input stage connected to a high impedance output current stage.

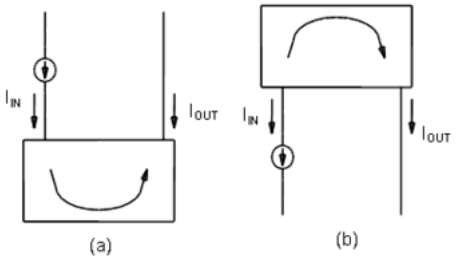

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Figure 11.1, Current Mirror (a) Sink (b) Source

Conceptually, an ideal current mirror is simply an ideal current amplifier with a gain of -1. In Chapter 8 we explored the transistor and you should recall that the BJT device is a current amplifier of (current controlled current source) in that the collector current is β times the base current. The problem with using this feature directly is that β is not a well controlled value from device to device an vary with changes in temperature. Accurate current amplifiers are difficult to directly implement using conventional transistor amplifier configurations which are typically voltage amplifiers. For exar

the MOS transistor is generally modeled as a voltage controlled current source and can not be used directly as a current amplifier. The use of feedback and the current to voltage relationship of two terminal elements such as a resistor are most often used when manipulating currents as signals. Because in a current mirror the input and output are currents, it is easier to convert the input to a volt first and then convert a voltage back to a current at the output.

It should be noted that these two stages of the current mirror may have a linear relationship (for example where $V(volt)_{OUT} = I_{IN}R$ and $I_{OUT} = V(volt)_{IN}/R$) like a resistor. In figure 11.1.1 we see t classic operational amplifier implementation of the current to voltage converter explored back in Chapter 4 section 2. The virtual ground at the negative input of the op-amp provides a very low inp resistance. These circuits use the linear relationship between the current in resistor R1 and the voltage across the resistor. However, this linear relationship is not necessarily required. Any element or combination of elements could be used such as the $V(volt)_{BE}$ or $V(volt)_{GS}$ of a transistor as in (b) if the output voltage was taken at the gate of M1 (output of the op-amp).

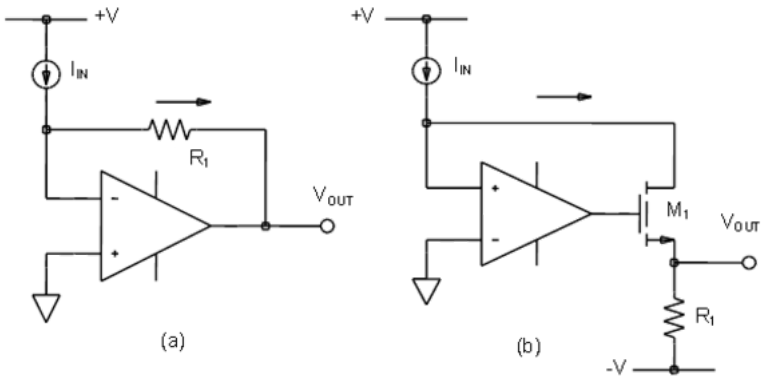

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Figure 11.1.1 Linear Current to Voltage converter (from Chapter 4)

Similarly, as an output stage we have the operational amplifier implementation of the voltage to current converter from section 1 of Chapter 4 in figure 1.1.2. Here the input voltage is forced across resistor R1 such that the resulting current in R1 flows through transistor M1.

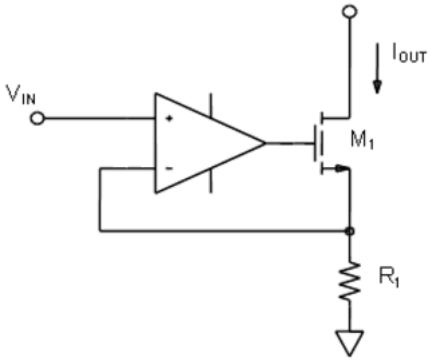

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Figure 11.1.2 Linear Voltage to Current converter (from Chapter 4)

Implementing the block diagram of the current mirror shown in figure 11.1 follows directly from these voltage / current converter stages from Chapter 4, if we connect the output of the I to V (volt converter in figure 11.1.1(b) to the input of the V (volt) to I converter in figure 11.1.2. With the two resistors being equal, I_{OUT} would be the mirror image of I_{IN}. Note that the second op-amp is not actually necessary because the gates of the two NMOS transistors can be tied directly to each other with the same result. Remember that two equal size transistors at the same temperature with the $V(volt)_{GS}$ (or $V(volt)_{BE}$ for a BJT) have the same drain current. This is an important simplification of the current mirror concept.

The converters might consist of non-linear devices having whatever I to V (volt) characteristics that may include another physical quantity (such as temperature); the only requirement is that the characteristics be the inverse of each other. For example, if the input I to V (volt) stage implements a function v = f(i) and the output stage implements the inverse function i = f -1(v) the total input to output transfer function is v = f(i) = f(f -1(v)) . We can make a second observation: A current mirror consists of two connected stages with inverse transfer functions of each other.

The converter circuits in figures 11.1.1 and 11.1.2 are rather complicated and require as many as two operational amplifiers. A much simpler implementation would be better.

11.2 An input stage to convert current to voltage

We would like a simple configuration where the active element, a single transistor, serves as the desired current-to-voltage converter. However, the transistor is a unidirectional device, where for the B the base emitter voltage controls the collector current or for the FET the gate source voltage controls the drain current. Producing the opposite where the collector current controls the $V(volt)_{BE}$ is n possible in the conventional use of the device as a common emitter amplifier. Referring back to Figure 11.1.1, the solution is to incorporate negative feedback. In this case that means making the tra adjust its base emitter or gate source voltage, $V(volt)_{BE}$ or $V(volt)_{GS}$, so that the collector or drain current is $I_{IN} = (V(volt)_1 - V(volt)_{BE})/R$. For this purpose, we simply connect the collector to the ba gate to drain or "diode connect" the transistor. This classic "diode" connection results in 100% parallel negative feedback (figure 11.2). As a result, with this diode connected transistor, the collector current serves as the input quantity while the base-emitter voltage $V(volt)_{BE}$ serves as the output quantity with the logarithmic transfer function of the base emitter junction. Similarly, a diode conne enhancement mode MOS FET (gate tied to drain) will serve as a similar current to voltage converter with $V(volt)_{GS}$ as the output quantity rather than $V(volt)_{BE}$.

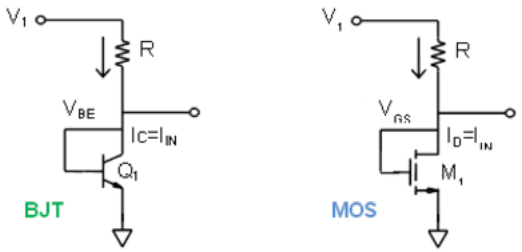

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Figure 11.2, Current to Voltage Converter

ADALM1000 BJT as a diode lab activity (/university/courses/alm1k/alm-lab-3)
ADALM1000 MOS as a diode lab activity (/university/courses/alm1k/alm-lab-3m)
ADALM2000 BJT as a diode lab activity (/university/courses/electronics/electronics-lab-3)
ADALM2000 MOS as a diode lab activity (/university/courses/electronics/electronics-lab-3m)

11.3 An output stage to convert voltage to current

A bipolar transistor can be driven by a voltage or by a current. If we consider the base emitter voltage, V (volt)$_{BE}$, as the input and the collector current, I_C, as the output (figure 11.3), we can think o transistor as a non-linear voltage-to-current converter having an exponential characteristic. The base can be directly driven by the voltage output of the I-to-V (volt) converter we just discussed. The collector provides the output terminal of our simple current mirror: The output V (volt) to I converter stage of the simple current mirror is just a transistor acting as a non-linear (exponential for BJT voltage-to-current converter. Again if a MOS transistor were used for the input stage the output stage would be a MOS transistor with the gate serving as the voltage input and the drain as the curre output.

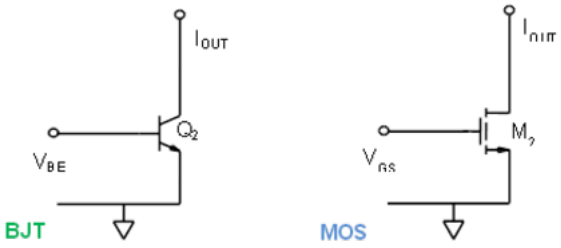

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Figure 11.3, Voltage to Current Converter

11.4 Assembling the complete circuit

The final step is to connect the output of the input stage (the base emitter junction of Q_1) to the input of the output stage (the base emitter junction of Q_2) to build the basic BJT current mirror circ (figure 11.4). At this point we will concentrate on the issues involved with the BJT current mirror and pick back up with the MOS current mirror in section 11.6.

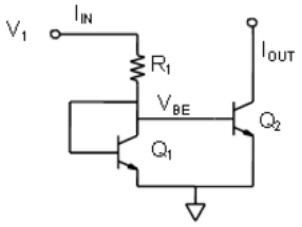

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Figure 11.4, BJT Current Mirror

11.4.1 Mirror Gain other than 1

If transistors Q_1 and Q_2 in figure 11.4 are identical (that is have the same size emitter and thus equal I_S) the input current to output current ratio or gain is ideally 1. There are often occasions when gain other than one is required. When building circuits from discrete devices only simple integer ratios are possible while in microelectronic integrated circuits it is possible to make transistors with arbitrary emitter areas, A. However, even in integrated circuits the best design practice is to use identical unit size transistors when making current mirrors.

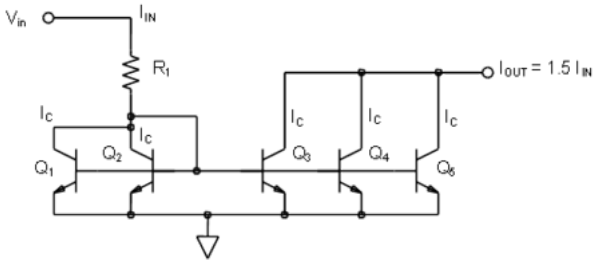

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Figure 11.4.1, Current Mirror with non-unary gain ratio

If on the input side of the mirror we connect N identical devices in parallel and connect M (mega (prefix, as in Mbps, MHz)) devices in parallel on the output side, the gain of the mirror will be M (m (prefix, as in Mbps, MHz))/N. In figure 11.4.1 we see an example where 2 (N=2) devices are connected together on the input and 3 (M (mega (prefix, as in Mbps, MHz))=3) devices are connected to on the output. The mirror gain will thus be 3/2 or 1.5. Since all five transistors share the same V (volt)$_{BE}$voltage, their collector currents, I_C, will all be equal. The input current I_{IN} splits equally in Q Q_2 such that:

$$I_C = \frac{I_{IN}}{2}$$

,

$$I_{OUT} = 3 I_C$$

or $\left(\frac{3}{2}\right) I_{IN}$

11.5 Imperfections of the simple mirror

There are three primary error sources that make the simple 2 transistor mirror less than ideal. The first is the mirror gain. Ideally I_{OUT} should exactly equal I_{IN}. There are systematic and random fa that make this not the case. The second is the incremental output resistance, which determines how much the output current varies with the voltage seen at the mirror output. The third limitation is minimum voltage drop across the output leg of the mirror necessary to maintain the desired output current. This minimum voltage, called output compliance, is determined by the need to keep the output transistor of the mirror in the active region. There are also a number of secondary performance issues with mirrors, for example, temperature stability and frequency response.

11.5.1 Gain Errors

An error source in this simple BJT based current mirror is that the transistors Q_1 and Q_2 (figure 11.4) each remove a base current I_B from the input current I_{IN}. As a result, the output current is sma than the input current:

$$I_{OUT} = I_{IN} - 2 I_B$$

As was already discussed, current mirrors can just as easily be made from MOS FET transistors. The I-to-V (volt) and V (volt)-to-I functions are different but of course are still the inverse of each otl significant advantage of the MOS current mirror is the lack of base current induced error that BJT current mirrors suffer. There are methods to correct or compensate for the base current in BJT c mirrors which will be discussed in detail in later sections of this chapter.

11.5.2 Compliance voltage

It is necessary to keep the output (BJT) transistor out of saturation, V (volt)$_{CB}$ = 0 V (volt). Or from another perspective, not allow the collector base junction to forward bias. That means the lowest output voltage that results in the correct output current, the compliance voltage, is V (volt)$_{OUT}$ = V (volt)$_{CV}$ = V (volt)$_{BE}$ under bias conditions with the output transistor at the output current level I_C with V (volt)$_{CB}$ = 0 V (volt) or, restating the V (volt)$_{BE}$relation from earlier:

$$V_{CV} = V_T \ln\left(\frac{I_C}{I_S}\right)$$

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Where V (volt)$_T$ is the thermal voltage and I_S is the reverse saturation current.

11.5.3 Output resistance

The V (volt)$_{CB}$ of Q_1 in the mirror is zero. If V (volt)$_{CB}$ is greater than zero in the output transistor Q_2, the collector current in Q_2 will be somewhat larger than Q_1 due to the Early effect. In other the mirror has a finite output resistance given by the r_O of the output transistor, namely:

$$R_N = r_O = \frac{V_{CB} + V_A}{I_C}$$

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Where:
V (volt)$_A$ is the Early voltage
V (volt)$_{CB}$ is the collector-to-base voltage

As we learned in an earlier chapter, the inclusion of emitter degeneration resistors (R_{E1} and R_{E2} in figure 11.5) can increase the effective collector impedance seen at the mirror output. In order for t mirror gain to remain equal to 1, R_{E1} must of course equal R_{E2}. The added voltage drop across the emitter resistor R_{E2} (I_{OUT} x R_{E2}) adds to the minimum allowable output voltage (see section 11.

While resistors could also be added to the sources in an MOS based mirror, it is often more effective to simple increase the channel length, L, of the transistors. The longer the channel the less it is a by the channel length modulation due to the increasing drain voltage.

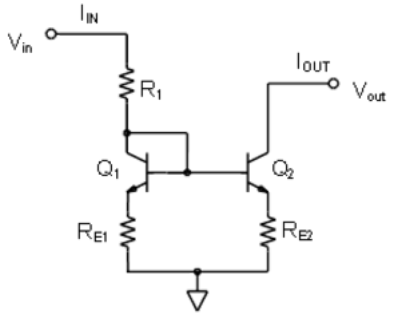

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Figure 11.5, Emitter degeneration included to boot output resistance.

It is important to note that the inclusion of emitter resistors does not reduce the reduction in the output current I_{OUT} caused by the finite beta of Q_1 and Q_2. A compensating voltage can be inserted including resistor R_B, of the correct value, as shown in figure 11.6.

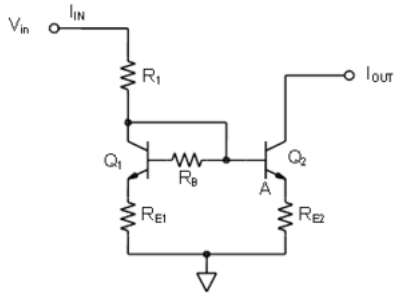

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Figure 11.6, Adding a resistor in the base of Q_1 tends to compensate for the finite beta of Q_2

For V (volt)$_{CB}$ close to zero (that is, neglecting base-width modulation errors) the necessary value for R_B is:

$$R_B = \frac{\beta+1}{\beta-A}(1+A)(r_E + R_{E1})$$

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For example, using A = 2 (a mirror gain of 2), I_{IN} = 1mA, so r_E = 26Ω and R_{E1} = 500Ω (introducing about 500mV of degeneration) R_B should be 1578Ω if β is enough larger than A so that facto be ignored, or 1626Ω if it is included and beta is 100. Clearly, this compensation method becomes unpredictable when β is small and is comparable to A and will never be precise because β_1 and β_2 not in general equal. However, this technique can be of practical utility in many cases.

11.6 Basic MOSFET current mirror

The simple current mirror can, obviously, also be implemented using MOSFET transistors, as shown in figure 11.7. We know that transistor M (mega (prefix, as in Mbps, MHz))$_1$ is operating in the saturation region because V (volt)$_{DS}$ is greater than or equal to V (volt)$_{GS}$. Transistor M (mega (prefix, as in Mbps, MHz))$_2$will also be in saturation so long as the output voltage is larger than its satu voltage. In this simple configuration, the output current I_{OUT} is directly related to I_{IN}.

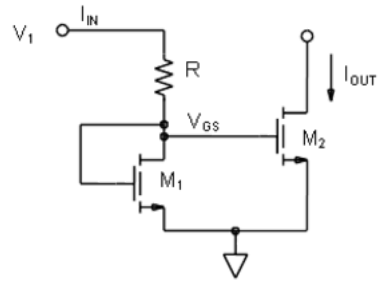

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Figure 11.7 Simple MOS current mirror

The drain current of a MOSFET I_D is a function of both the gate to source voltage and the drain to gate voltage of the MOSFET given by I_D = f (V (volt)$_{GS}$, V (volt)$_{DG}$), a relationship derived fro functionality of the MOSFET device. In the case of transistor M (mega (prefix, as in Mbps, MHz))$_1$ of the mirror, $I_D = I_{IN}$. Input current I_{IN} is a known current, and can be provided by a resistor a shown in the figure, or by a threshold-referenced or self-biased current source to ensure that it is constant, independent of voltage supply variations.

Using V (volt)$_{DG}$=0 for transistor M (mega (prefix, as in Mbps, MHz))$_1$, the drain current in M (mega (prefix, as in Mbps, MHz))$_1$ is I_D = f (V (volt)$_{GS}$,V (volt)$_{DG}$=0), so we find: f (V (volt)$_{GS}$, 0) = I_I implicitly determining the value of V (volt)$_{GS}$. Thus I_{IN} sets the value of V (volt)$_{GS}$. The circuit in the diagram forces the same V (volt)$_{GS}$ to apply to transistor M (mega (prefix, as in Mbps, MHz))$_2$. (mega (prefix, as in Mbps, MHz))$_2$ also is biased with zero V (volt)$_{DG}$ and provided transistors M (mega (prefix, as in Mbps, MHz))$_1$ and M (mega (prefix, as in Mbps, MHz))$_2$ have good matching of properties, such as channel length, width, threshold voltage etc., the relationship I_{OUT} = f (V (volt)$_{GS}$,V (volt)$_{DG}$=0) applies, thus setting $I_{OUT} = I_{IN}$; that is, the output current is the same as the inp current when V (volt)$_{DG}$=0 for the output transistor, and both transistors are matched.

The drain-to-source voltage can be expressed as V (volt)$_{DS}$=V (volt)$_{DG}$ + V (volt)$_{GS}$. With this substitution, the Shichman-Hodges model provides an approximate form for function f(V (volt)$_{GS}$,V (volt)$_{DG}$):

$$I_D = f\left(V_{GS}, V_{DG}\right) = \frac{1}{2} K_p \left(\frac{W}{L}\right)\left(V_{GS} - V_{th}\right)^2 \left(1 + \lambda V_{DS}\right)$$

$$I_D = \frac{1}{2} K_p \left(\frac{W}{L}\right)\left(V_{GS} - V_{th}\right)^2 \left(1 + \lambda \left(V_{DG} + V_{GS}\right)\right)$$

Where:
Kp is a technology related constant associated with the transistor,
W/L is the width to length ratio of the transistor,
V (volt)$_{GS}$ is the gate-source voltage, V (volt)$_{th}$ is the threshold voltage, V (volt)$_{DS}$ is the drain-source voltage
λ is the channel length modulation constant

Output resistance

Because of channel-length modulation, the mirror has a finite output resistance given by the *ro* of the output transistor, namely:

$$R_N = r_O = \frac{1/\lambda + V_{DS}}{I_D}$$

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Where:
λ = channel-length modulation parameter
V (volt)$_{DS}$ = drain-to-source bias.

Compliance voltage

To keep the output transistor resistance high, V (volt)$_{DG}$ = 0 V (volt). That means the lowest output voltage that results in correct mirror behavior, the compliance voltage, is V (volt)$_{OUT}$ = V (volt)$_{CV}$ (volt)$_{GS}$ for the output transistor at the output current level with V (volt)$_{DG}$ = 0 V (volt), or using the inverse of the f- function, f^{-1}:

$$V_{CV} = V_{GS}(\text{for } I_D \text{ at } V_{DG} = 0V) = f^{-1}(I_D) \text{ with } V_{DG} = 0$$

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For the Shichman-Hodges model, f^{-1} is approximately a square-root function.

11.7 Improved current mirrors

11.7.1 Buffered Feedback current mirror

Figure 11.8 shows a mirror where the simple wire connecting the collector of Q_1 to its base is replaced by an emitter follower buffer. This improvement to the simple current mirror is referred to as a emitter follower augmented mirror. The current gain ($ß_{Q3}$) of the emitter follower buffer stage (Q_3) greatly reduces the gain error caused by the finite base currents of Q_1 and Q_2.

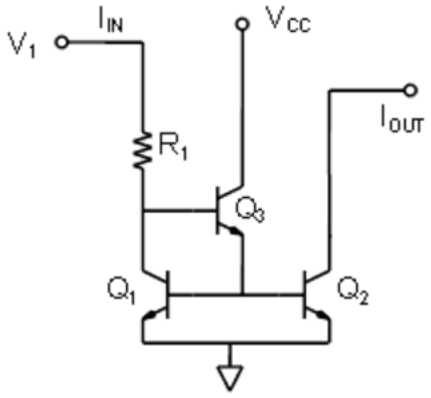

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Figure 11.8 Buffered Feedback current mirror.

One thing to note that is different in this mirror configuration vs. the simple two transistor mirror is that the Collector-Base voltage, V (volt)$_{CB}$, of Q_1 is no longer zero. It is equal to the V (volt)$_{BE}$ of Given the effect of the finite output resistance (Early effect) the output current I_{OUT} in Q_2 will most closely match I_{IN} when the collector voltage of Q_2 is the same as that of Q_1 which is $2XV_{BE}$ ab the common voltage. Also note that when driven by a resistor, like R_1, I_{IN} will now be (V (volt)$_1$-V (volt)$_{BE1}$-V (volt)$_{BE2}$)/R_1.

Another consequence of adding the emitter follower buffer is, in general, a loss in the frequency response of the mirror. Transistor Q_3 is potentially operating at a very small current of $2I_B$. If there to be a significant capacitance to ground at the base connection common to Q_1 and Q_2 the current available to discharge this current will also be small equal to $2I_B$. But the current available to cha this node is potentially equal to $ß_{Q3}I_{IN}$ which is very much larger than $2I_B$. This asymmetry in the charging vs. discharging current available for this node in the current mirror can lead to very undesirable response to fast changes to I_{IN}.

11.7.2 The Wilson current mirror

A Wilson current mirror or Wilson current source, named after George Wilson, is an improved mirror circuit configuration designed to provide a more constant current source or sink. It provides a more accurate input to output current gain. The structure is shown in figure 11.9.

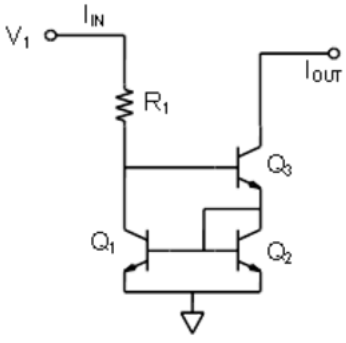

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Figure 11.9 The Wilson Current Mirror

We will be making the following two assumptions. First, all transistors have the same current gain ß. Second, Q_1 and $Q_2$are matched, so their collector currents are equal. Therefore, $I_{C1} = I_{C2} (= I_C)$ $I_{B1} = I_{B2} (= I_B)$.

The base current of Q_3 is given by,

$$I_{B3} = \frac{I_{C3}}{\beta}$$

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The emitter of Q_3 current by,

$$I_{E3} = (\frac{\beta+1}{\beta})I_{C3}$$

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Looking at figure 11.9, it can be seen that $_{IE3} = I_{C2} + I_{B1} + I_{B2}$ Substituting for I_{C2}, I_{B1} and I_{B2}, $I_{E3} = I_C + 2I_B$

so,

$$I_{E3} = (1 + \frac{2}{\beta})I_C$$

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Substituting for I_{E3}

$$(\frac{\beta+1}{\beta})I_{C3} = (1 + \frac{2}{\beta})I_C$$

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rearranging,

$$I_C = (\frac{\beta+1}{\beta+2})I_{C3}$$

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The current through R_1 is given by, $I_{R1} = I_{C1} + I_{B3}$

But, $I_{C1} = I_{C2} = I_C$

Substituting for I_C and since $I_{B3} = \frac{I_{C3}}{\beta}$ (/_detail/university/courses/electronics/text/chptr11-e7.png?id=university%3Acourses%3Aelectronics%3Atext%3Achapter-11) we get,

$$I_{R1} = (\frac{\beta+1}{\beta+2})I_{C3} + \frac{I_{C3}}{\beta}$$

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Therefore,

$$I_{R1} = (\frac{\beta+1}{\beta+2} + \frac{1}{\beta})I_{C3}$$

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And finally,

$$I_{C3} = \frac{I_{R1}}{1 + \frac{2}{\beta(\beta+2)}}$$

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From the above equation we can see that if

$$\frac{2}{\beta(\beta+2)} << 1, I_{C3} \approx I_{R1}$$

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And the output current (assuming the base-emitter voltage of all transistors to be 0.7 V (volt)) is calculated as,

$$I_{C3} \approx I_{R1} = \frac{V_1 - V_{BE2} - V_{BE3}}{R_1}$$

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Note that the output current is equal to the input current I_{R1} which in turn is dependent on V (volt)$_1$ and R_1. If V (volt)$_1$ is not stable, the output current will not be stable. Thus the circuit does not a
a regulated constant current source.

In order for it to work as a constant current source, R_1 must be replaced with a constant current source.

Advantages over other configurations

This circuit has the advantage of virtually eliminating the base current mismatch of the conventional BJT current mirror thereby ensuring that the output current I_{C3} is almost equal to the reference
input current I_{R1}. It also has a very high output impedance due to the negative feedback through Q_1 back to the base of Q_3.

11.7.3 Further improvement (full Wilson Mirror)

Adding a fourth transistor to the simple Wilson current mirror in figure 11.10, we have the modified or improved Wilson mirror. The improved input to output current accuracy is accomplished by
equalizing the collector voltages of Q_1 and Q_2 at 1 V (volt)$_{BE}$. This leaves the finite ß and voltage differences of each of Q_1 and Q_2 as the remaining unbalancing influences in the mirror.

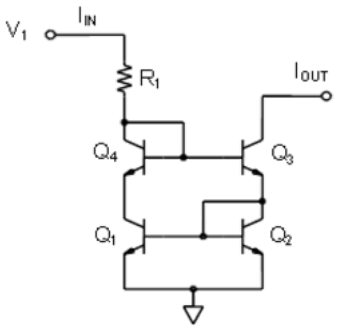

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Figure 11.10 The improved Wilson Current Mirror

11.8 Widlar current source

A Widlar current source is a modification of the basic two-transistor current mirror that incorporates an emitter degeneration resistor for only the output transistor, enabling the current source to ge
low currents using only moderate resistor values. This circuit is named for its inventor, Robert Widlar, and was patented in 1967.

The Widlar circuit may be used with bipolar transistors or MOS transistors. An example application is in the now famous uA741 operational amplifier, and Widlar used the circuit in many of his de

11.8.1 Analysis

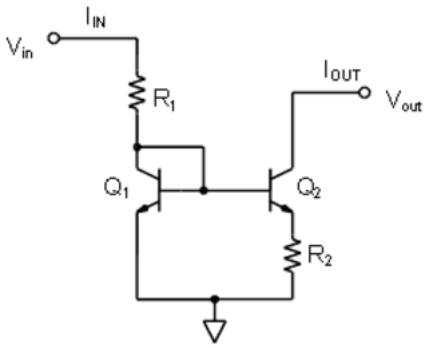

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Figure 11.11 A version of the Widlar current source using bipolar transistors.

Figure 11.11 is an example Widlar current source using bipolar transistors, where the emitter resistor R_2 is connected in series with the emitter of output transistor Q_2, and has the effect of reducing
current in Q_2 relative to Q_1. The key to this circuit is that the voltage drop across the resistor R_2 subtracts from the base-emitter voltage of transistor Q_2, thereby reducing the collector current comp
to transistor Q_1. A simulation plot showing this reduction in I_{C2} is presented in figure 11.12.

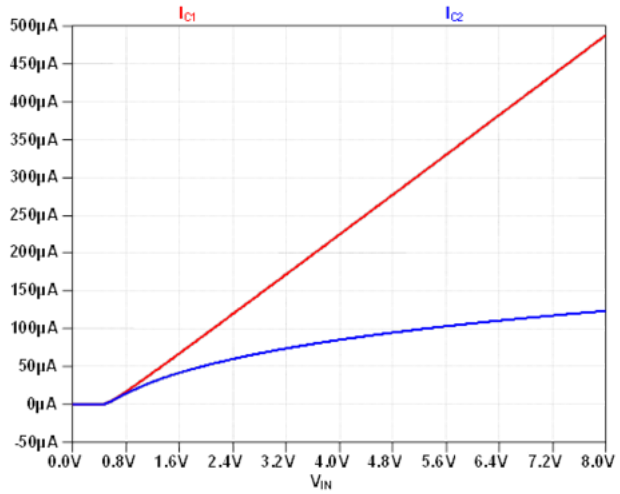

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Figure 11.12 Plot of the collector current of Q_1 and Q_2 R_1 = 15KΩ, R_2 = 300

This observation is expressed by using KVL around the base emitter loop of the circuit in Figure 11.11 as:

$$V_{BE1} = V_{BE2} + I_{E2}R_2 = V_{BE2} + (\beta_2 + 1)I_{B2}R_2$$

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Where $ß_2$ is the beta of the output transistor, which may not be the same as that of the input transistor, in part because the currents in the two transistors are very different. The variable I_{B2} is the ba current of the output transistor, V (volt)$_{BE}$ refers to base-emitter voltage. If we neglect the effect of finite ß and use the V (volt)$_{BE}$ equation we can obtain a useful formula for the output current:

$$I_{OUT}R_2 = V_T \ln \frac{I_{IN}}{I_{OUT}}$$

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where V (volt)$_T$ is the thermal voltage, $I_{IN} = I_{C1}$ and $I_{OUT} = I_{C2}$.

Suppose we want to create a 100uA output current from a 300uA input current as in the simulation plot of figure 11.12. V (volt)$_T$ is 26mV times ln(3) is 28.5mV. 28.5mV divided by 100uA is 285 oh This equation makes the approximation that the currents are both much larger than the saturation currents I_{S1}, I_{S2}, an approximation valid except for very low current levels. In the following the distinction between the two scale currents is dropped, although the difference can be important, for example, if the two transistors are designed with different emitter areas.

11.8.2 Output impedance

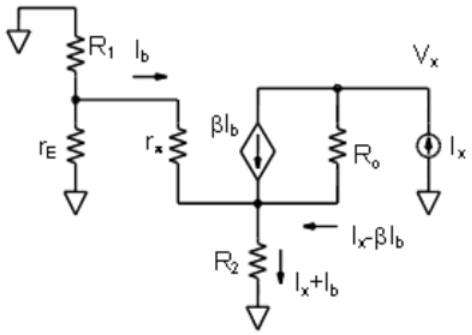

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Figure 11.13 Small-signal circuit for finding output resistance of the Widlar source shown in figure 11.11.

A test current $I/_x$ is applied at the output, and the output resistance is then R_O = V (volt)$_x$ / I_x.

An important property of a current source is its small signal incremental output impedance, which should ideally be infinite. The emitter degeneration resistance introduces local current feedback fo transistor Q_2. Any increase in the current in Q_2 increases the voltage drop across R_2, reducing the V (volt)$_{BE}$ for Q_2, thereby countering the increase in current. This feedback means the output impedance of the circuit is increased, because the feedback involving R_2 forces use of a larger voltage to drive a given current.

Output resistance is found using a small-signal model for the circuit, shown in Figure 11.13. The transistor Q_1 is replaced by its small-signal emitter resistance r_E because it is diode connected. In a d connected transistor the collector is short-circuited to the base, so the transistor collector-base junction has no time-varying voltage across it. As a result, the transistor behaves like the base-emitter di which at low frequencies has a small-signal circuit that is simply the resistor r_E = V (volt)$_T$ / I_E, with I_E the DC Q-point emitter current. The transistor Q_2 is replaced with its hybrid-pi model. A test current I_x is attached at the output.

Using the figure, the output resistance is determined using Kirchhoff's laws. Using Kirchhoff's voltage law from the ground on the left to the ground connection of R_2:

$$I_b((R_1 \parallel r_E) + r_\pi) + (I_x + I_b)R_2 = 0\ .$$

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Rearranging:

$$I_b = -I_x \frac{R_2}{(R_1 \parallel r_E) + r_\pi + R_2} \ .$$

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Using Kirchhoff's voltage law from the ground connection of R_2 to the ground of the test current:

$$V_x = I_x(r_O + R_2) + I_b(R_2 - \beta r_O) \ ,$$

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or, substituting for I_b:

Eq. 4

$$R_O = \frac{V_x}{I_x} = r_O \left(1 + \frac{\beta R_2}{(R_1 \parallel r_E) + r_\pi + R_2}\right)$$ (/_detail/university/courses/electronics/text/chptr11-e22.png?id=university%3Acourses%3Aelectronics%3Atext%3Achapter-11)

$$+ R_2 \left(\frac{(R_1 \parallel r_E) + r_\pi}{(R_1 \parallel r_E) + r_\pi + R_2}\right) \ .$$ (/_detail/university/courses/electronics/text/chptr11-e23.png?id=university%3Acourses%3Aelectronics%3Atext%3Achapter-11)

According to Eq. 4, the output resistance of the Widlar current source is increased over that of the output transistor itself (which is r_O) so long as R_2 is large enough compared to the r_p of the output transistor. (Large resistances R_2 make the factor multiplying r_O approach the value (ß +1).) The output transistor carries a low current, making r_p large, and increase in R_2 tends to reduce this current further, causing a correlated increase in r_p. Therefore, a goal of $R_2 \gg r_p$ can be unrealistic, and further discussion is provided below. The resistance R_1 / r_E usually is small because the emitter resistance usually is only a few ohms.

ADALM1000 Lab Activity 6, BJT Current Mirror (/university/courses/alm1k/alm-lab-6)
ADALM1000 Lab Activity 6M, MOS Current Mirror (/university/courses/alm1k/alm-lab-6m)

ADALM2000 Lab Activity 6, BJT Current Mirror (/university/courses/electronics/electronics-lab-6)
ADALM2000 Lab Activity 6M, MOS Current Mirror (/university/courses/electronics/electronics-lab-6m)

11.9. The Zero Gain Amplifier

When designing a circuit it is important to take into account the wide variation in certain device values from one to another. A central objective of the designer is to desensitize the circuit to these variations to produce a circuit which meets the specifications across all possible conditions. One aspect of design which is common to nearly all circuits is the establishment of stable bias or operating levels. This seemingly minor portion of a design can provide the most challenging and interesting circuit problems. Many bias generators are centered around the generation of currents to operate the core of the circuit. Current generated from simple resistors and diodes or diode connected transistors connected across the power supply will vary approximately proportional to the variation of the supply voltage. This variation in the resulting bias current is frequently undesirable.

This is to introduce another kind of current mirror, actually a stabilized current source, which has an output which had been desensitized to variation in input current. To understand this configuration is helpful to examine the behavior of a zero gain amplifier. A NMOS version is shown in figure 11.14 but PMOS, NPN or PNP transistors will just as well function in this configuration

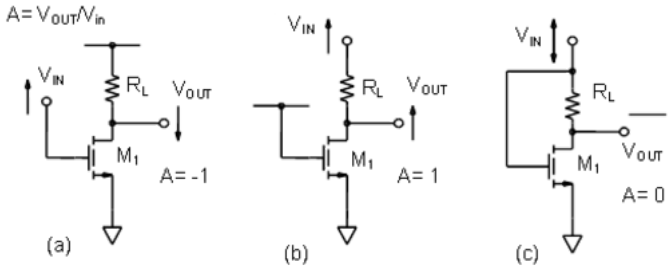

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Figure 11.14 NMOS Zero Gain Amplifier

Remembering back to the previous explanation of the common emitter/source amplifier (figure 11.14(a)), the gain is a function of the drain (or collector) current and the load resistor. For a given drain current, if the drain resistor R_L is set equal to r_s then the gain A will be minus 1.

Alternatively. if the gate is held fixed at the same DC bias level which produces an identical drain current as in (a) and an input signal is applied to the top of load resistor R_L (figure 11.14(b)), then the gain will be plus 1. That is if the drain/source output impedance of the transistor is neglected. If we now connect the gate to the top of resistor R_L as in figure 11.14©, the net gain superimposing both paths will be 1 - 1 = 0.

In figure 11.15 we have an NPN transistor biased into conduction with a collector voltage V (volt)$_C$ which is less than the base voltage V (volt)$_{BE}$ by the thermal voltage V (volt)$_T$= kT/q, (equal to Ic R_L) and is essentially constant with input voltage changes applied from V (volt)$_{IN}$. The voltages seen at V (volt)$_{BE}$ and V (volt)$_C$ are plotted vs. the applied voltage at V (volt)$_{IN}$ in figure 11.14. As we can see while V (volt)$_{BE}$ continues to rise, V (volt)$_C$ remains much more constant and actually decreases above a certain level of V (volt)$_{IN}$.

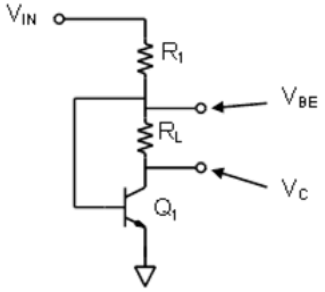

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Figure 11.15 NPN Zero Gain Amplifier

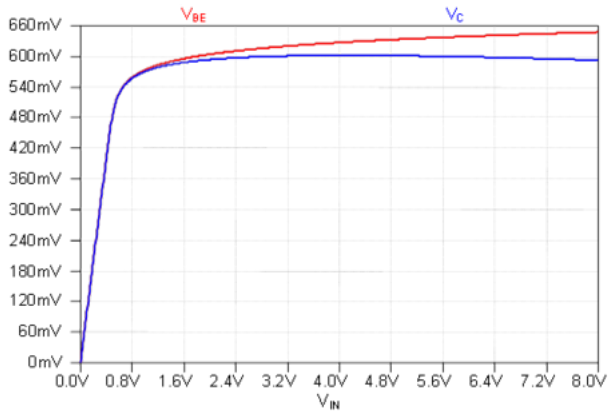

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Figure 11.16 Plot of V (volt)$_{BE}$ and V (volt)$_C$ vs V (volt)$_{IN}$ for R1 = 10KΩ and R_L=75Ω

A zero gain amplifier made using an enhancement mode NMOS 2N7000 transistor was simulated where the small signal AC gain and phase was calculated as the drain current was swept. As can b in figure 11.17 there is a sharp null or dip in the gain curve at around 345uA. This also occurs at the point where the phase makes a sharp transition from 0 degrees to 180 degrees.

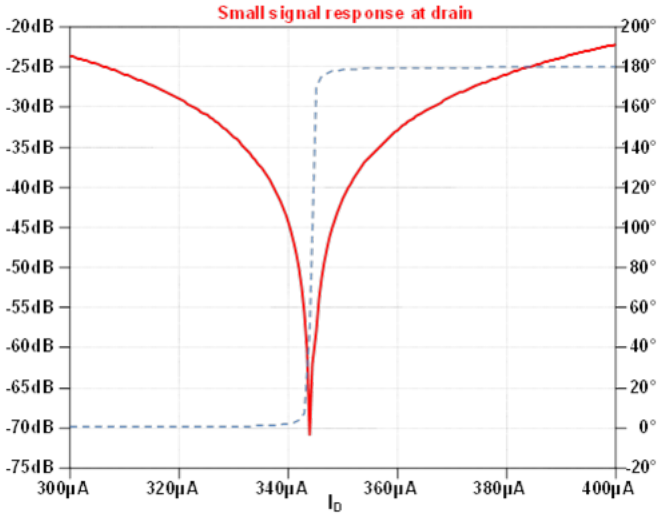

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Figure 11.17 Small signal gain/phase plot of zero gain amplifier vs. I_D

ADALM1000 Lab Activity 7, BJT Zero Gain Amplifier (/university/courses/alm1k/alm-lab-7)
ADALM1000 Lab Activity 7m, NMOS Zero Gain Amplifier (/university/courses/alm1k/alm-lab-7m)

ADALM2000 Lab Activity 7, BJT Zero Gain Amplifier (/university/courses/electronics/electronics-lab-7)
ADALM2000 Lab Activity 7m, NMOS Zero Gain Amplifier (/university/courses/electronics/electronics-lab-7m)

11.10 Stabilized Current Source

Now that we understand the concept of the zero gain amplifier, the objective is to investigate its use to produce an output current which is stabilized (less sensitive) to variations of the input current I This current source configuration, figure 11.17, is also sometimes called a Peaking Current Source or g (gravity)$_{m\ (milli\ (prefix,\ as\ in\ mW,\ mA,\ mV,\ ms))}$-compensated mirror. Because the collector voltage V of transistor Q_1 is now more constant with changes in the input supply voltage as represented by V (volt)$_{IN}$, it can be used as the base voltage of Q_2 to produce a much more constant collector curre transistor Q_2.

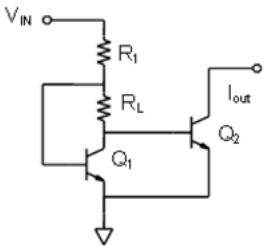

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Figure 11.18 Stabilized (Peaking) current source (g (gravity)$_{m\ (milli\ (prefix,\ as\ in\ mW,\ mA,\ mV,\ ms))}$-compensated mirror)

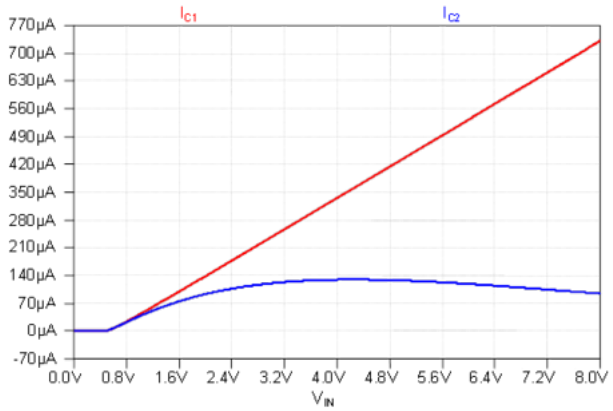

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Figure 11.19 Plot of the collector current of Q_1 and Q_2 $R_1 = R_2 = 10K\Omega$, $R_L = 75\Omega$

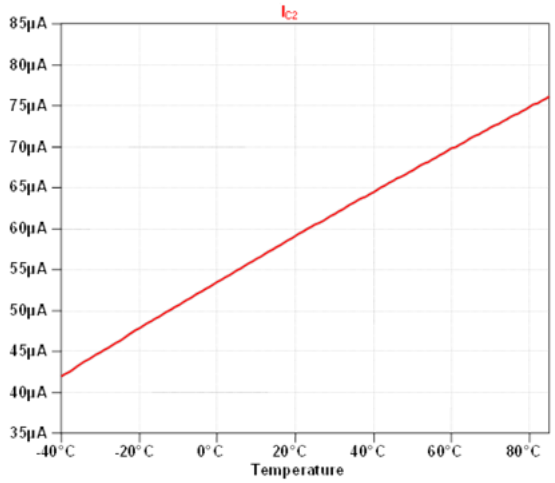

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Figure 11.20 PTAT current plot of Peaking Current Source

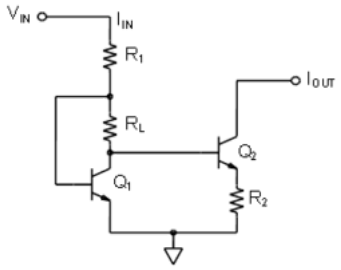

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Figure 11.21 A combination of the Widlar mirror and peaking current source provides further improvement in the regulation of a variable input current.

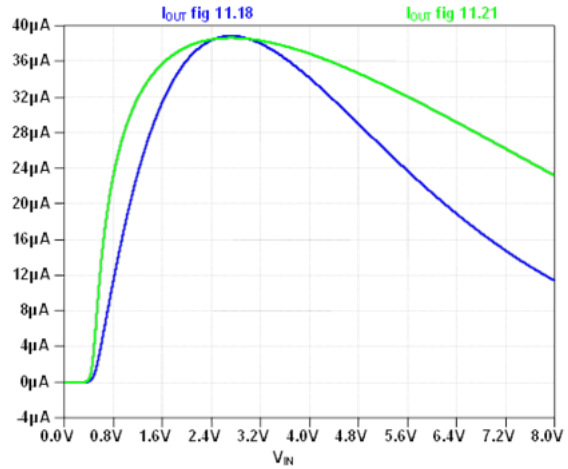

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Figure 11.22 Simulation of circuit in figures 11.18 and 11.21 with R_1 = 20KΩ, R_L= 250Ω and R_2= 1.2KΩ

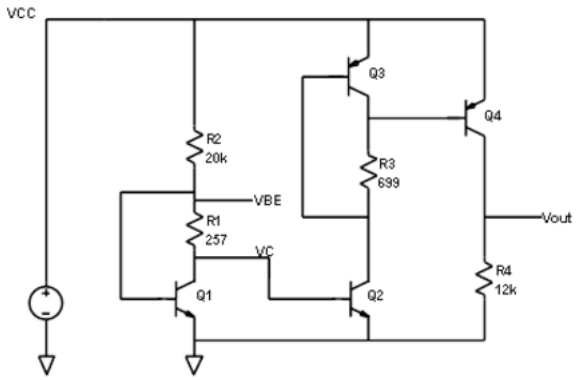

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Figure 11.23 cascade of NPN and PNP peaking current sources

ADALM1000 Lab Activity 8, BJT Stabilized current source (/university/courses/alm1k/alm-lab-8)
ADALM1000 Lab Activity 8m, NMOS Stabilized current source (/university/courses/alm1k/alm-lab-8m)

ADALM2000 Lab Activity 8, BJT Stabilized current source (/university/courses/electronics/electronics-lab-8)
ADALM2000 Lab Activity 8m, MOS Stabilized current source (/university/courses/electronics/electronics-lab-8m)

More background on current mirrors can be found in this Wikipedia page [https://en.wikipedia.org/wiki/Current_mirror]

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