Home

Current projects

Where TMC really shines: a novel transimpedance stage (TIS).

Note: This page will be updated from time to time (and press F5).

Introduction

The objective of this project is the realisation of a simple low cost yet symmetrical and ultra low distortion front-end suitable to drive high-end audio output stages (for example this one). In addition, providing a high PSRR and a (near) rail to rail ouput swing, which makes an elevated and heavily filtered supply voltage for the front-end unnecessary. Low distortion is obtained by using so called 'Baxandall super pairs' as well as Transitional Miller Compensation.
It should be noted that results are based on simulation using Micro-Cap. Also schematics, plots and other drawing were created with Micro-Cap.

Acronyms

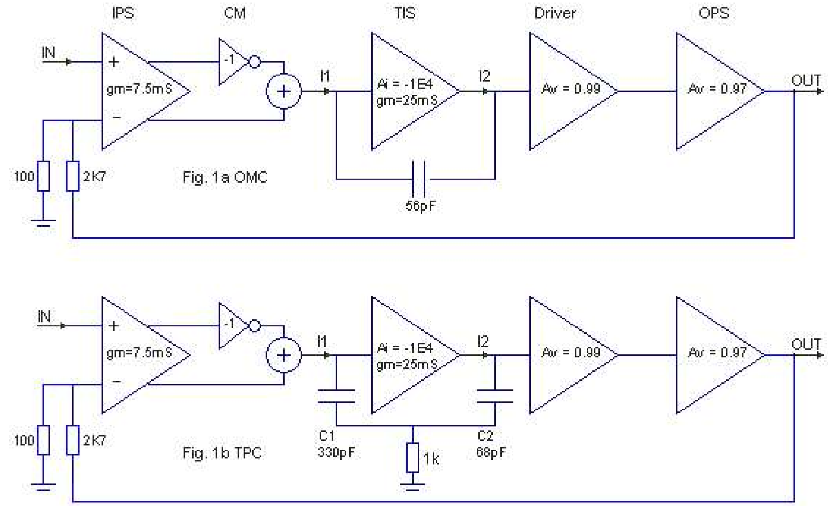
Ai: Current gain
Av: Voltage gain
Cdom: Dominant pole compensation capacitor or Miller capacitor
CMCL: Common Mode Control Loop
gm: (mutual) Transconductance
IIC: Input Inclusive Compensation
IPS: Input Stage
LTP: Long tailed Pair
OMC Ordinary Miller Compensation
OPS: Output Stage
PLIL Phase Lead, Input Lag (compensation)
PSRR Power Supply Rejection Ratio
SR: Slew Rate
TIS Trans-impedance Stage (also called VAS)
TMC Transitional Miller Compensation
TPC Two Pole (Miller) Compensation
ULGF Unity Loop Gain Frequency
VAS Voltage Amplification Stage (also called TIS)

OMC versus TPC versus TMC

A common way to explain the improvement from TPC or TMC over OMC is to look at the increased loop gain. The higher the loop gain, the lower the distortion. As simply as that. In case of TPC, all stages (IPS, VAS, Driver & OPS) are exposed to the increased loop gain, while in case of TMC the IPS doesn't benefit from the increase loop gain. So, one might conclude that TPC is superior over TMC. Theoretically, yes. Practically, certainly not in every case, as has been revealed by simulation of practical circuits. These seemingly contradictory results have led to a heated debate on DIY Audio Forum, which started here and continues there.

Clearly more factors are involved than just loop gain. Hence, a different approach is needed to fully explain the effects of TPC and

TMC on distortion. So, let's have a look at the *load* on the output of the IPS and VAS, because the lighter the load, the less distortion. Again, as simple as that. In the next simulations (of a typical mainstream amp) the load is expressed as AC current at a constant sine input signal of 1V. Four cases were investigated: OMC, TMC and two versions of TPC. I1 is the IPS output current and I2 is the VAS output current. See fig.1.



What we see, as expected, is that I1 is much lower in case of TPC, while in case of TMC, I1 is about the same or slightly higher compared to OMC. So far so good and in accordance with the textbooks. I2 however, shines a different light on these compensation schemes. See fig.2, bottom graphs. Now it is TMC that reduces the VAS loading by almost an order of magnitude, While TPC, if correct implemented (fig.1b), slightly increases the loading. However, if C1 and C2 are swapped (TPC-wrong), the VAS loading increases by an order of magnitude, resulting in much higher distortion. Needless to say that the latter is not recommended.

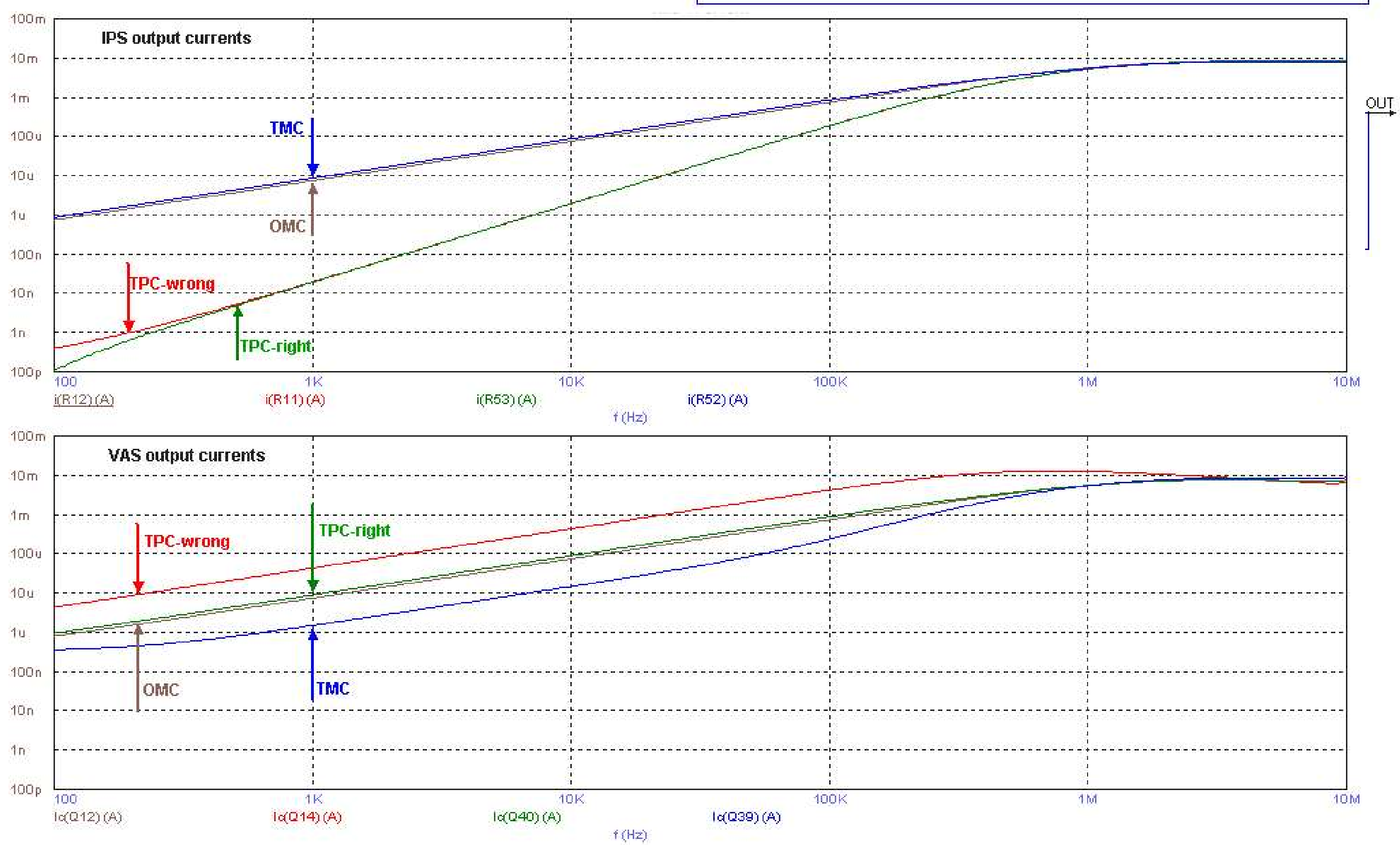


Fig. 2. AC currents as function of frequency seen at the output of the input stage and VAS output for different compensation schemes.

Pros and Cons in Summary

TPC reduces distortion of IPS, TIS and OPS as well, though it puts a higher load on the TIS output.
TMC only reduces the distortion of the TIS and OPS. However it decreases the load on the TIS output.
As both techniques have their pros and cons, practical implementations in power amps will yield similar improvements and there's no clear winner.

How to get rid of the cons and keep the pros of both techniques

We can improve the performance in two ways: either by decreasing the load on the VAS in case of TPC, or by decreasing the load on the IPS in case of TMC . Let's start with TPC. This can be realized by using the emitter of the (pre-) driver as take-off point for the Miller compensation, together with a small load on the VAS output itself, similar as depicted by fig.3b. But there's another (minor) issue with TPC not previously discussed here. Inherently to *this* kind of second order compensation, the step response suffers from a noticeable amount of overshoot. Although it can be remedied by an additional lead-lag compensation as has been shown by [Megajocke](), yet there are two more problems with complementary TISes: The stability of VAS quiescent current and the so called *fighting VAS* issue. These can be remedied by a common mode control loop (CMCL). However, the added complexity makes this route less attractive. So let's see what TMC has to offer.

As said before, in this case the load on the IPS has to be decreased, which can be realized by applying a so called 'Input Inclusive Compensation'. Instead of connecting the Miller cap C1 to the TIS input, just tie it to the inverting input of the IPS. Now, the IPS has far less work to do: Only supplying current to the TIS instead of supplying to the compensation capacitor as well, which is normally one order higher. See fig.4, upper curves, OMC versusTMC-2.

However, this not without consequence. Not only the Miller ULGF becomes way too high, but also the phase shift from the IPS adds to the Miller loop beyond an acceptable level. To maintain sufficient stability a redistribution of gain stages is required This is done by:

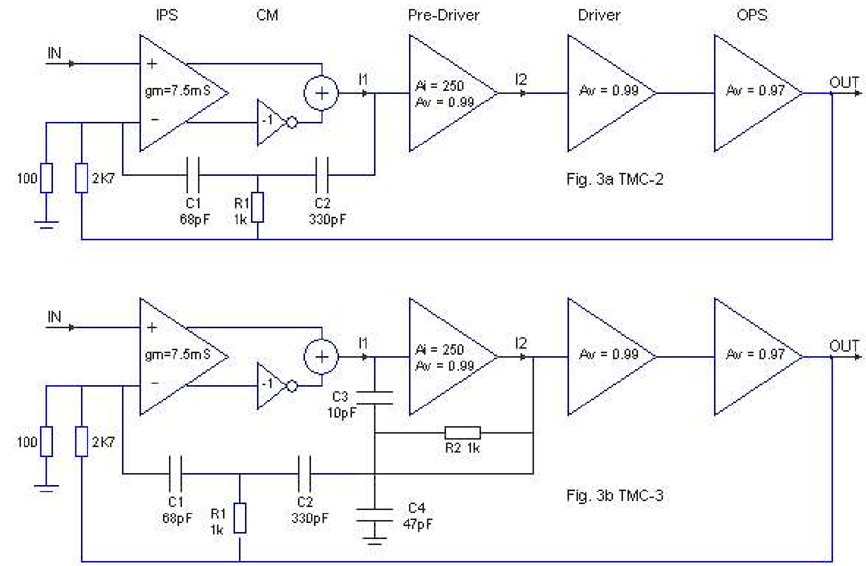
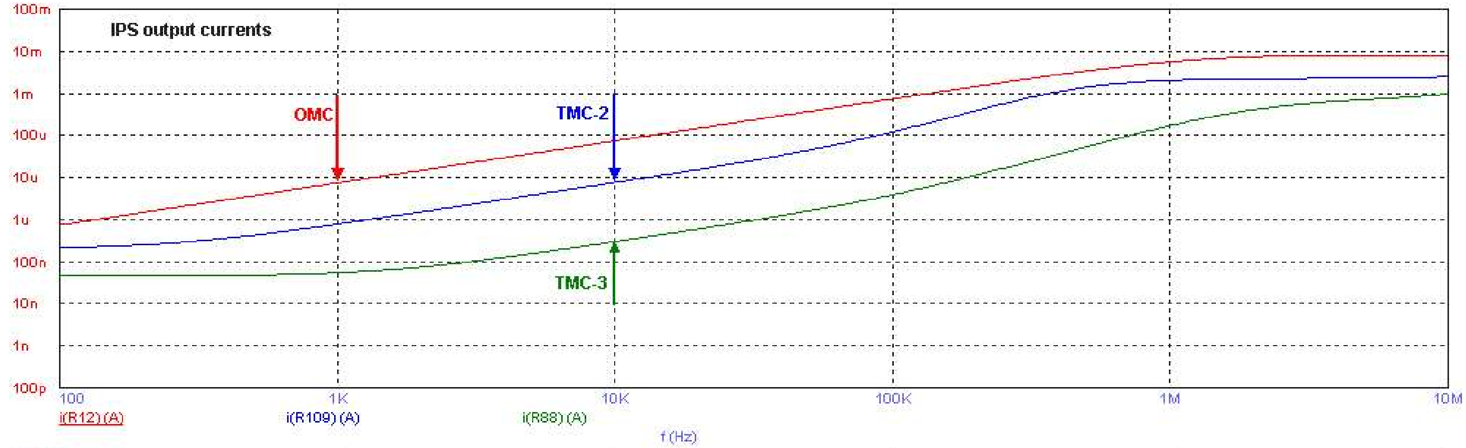


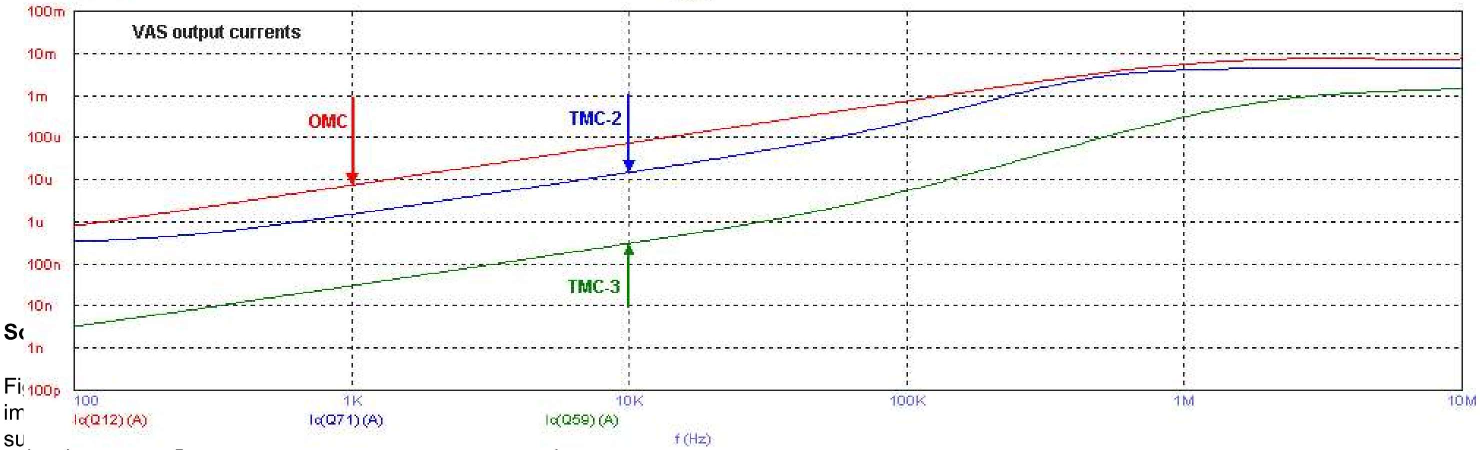
Fig.3a. Modified Transitional Miller Compensation enclosing the input stage.
Fig.3b. Ditto, enclosing the pre-driver as well.

1. Replacing the ubiquitous VAS (with a gain of beta or even beta^2) by a cascode (with a current gain of 1x) which is directly connected to the current mirror,
2. Putting a pre-driver after the cascode, which restores the gain of the whole chain, see fig.3a.

The cascode comprises not just a single transistor, rather a Baxandall super pair. As a result, the distortion caused by the nonlinear Cob and Early effect been almost completely eliminated. See Dimitri Danyuk and Malcom Hawksford for more information.

A futher improvement can be obtained by tying the compensation capacitor C2 to the output of the next stage, i.e. the pre-driver, see fig.3b. In this way, IPS and TIS output currents are reduced by almost three orders of magnitude, see fig.4 TMC-3.





pairs, the low distortion of the IPS would have been completely swamped by the distortion of them.

Although the current gain of the TIS is just 0dB, the gain-bandwidth-product of the stages enclosed by the Miller loop is still too high. Therefore, a so called PLIL compensation (C1 & R7) is added to stabilize the Miller loop. See John Ellis for more information on this subject.

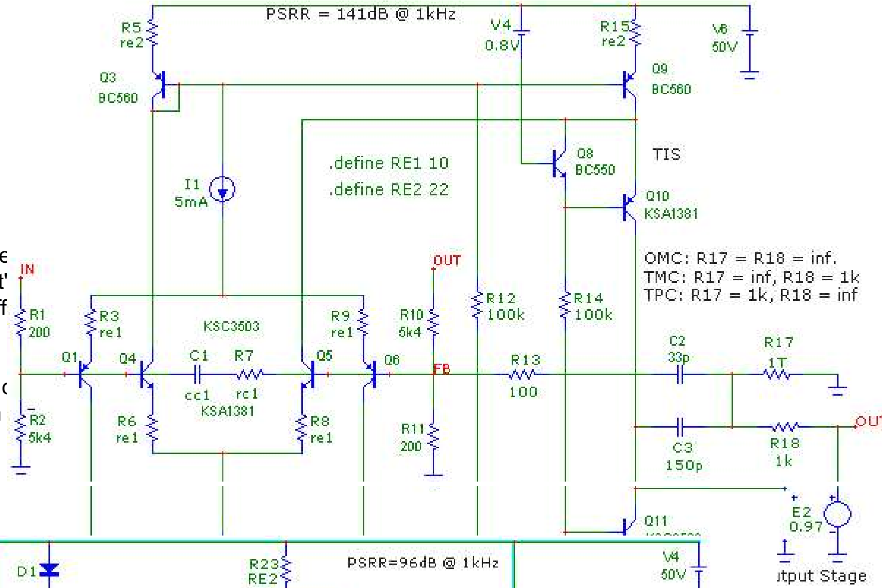
By the way, many other configurations also need additional compensation to tame the Miller loop.

Since the VAS has been replaced by a cascode having a current gain of just 1x, another problem arises: Any load (including C2) at the output of the TIS will also been 'seen' by the IPS. At first sight not much seems to be gained by this circuit. But... this is where TMC comes into play (and **shines!**), as it moves the capacitive load from the TIS to the OPS, well, at least at frequencies of interest. In this way (differential) collector currents of the IPS are greatly reduced. Compared to TPC at 20kHz by a factor of about 20 and compared to OMC by a factor of about 4 (of course, depending on circuit details).

For the same reason THD20k is much lower with TMC: 51ppb, leaving TPC (C2 & C3 not swapped) in the dust

with an embarrassing 1.3ppm.

It should be noticed that the current gain and gm are still rather low. Ignoring second order effects (finite beta, etc.) they are approximately: gm ~= 2 / (RE + VT / Ic) = 2 / (10 + 26 / 2.5) = 98 mA/V (simulated: 94 mA/V)
Iout / Ifb ~= Rfb*gm = 200*0.098 = 19.6 (simulated: 17.4).
Therefore, it's highly recommended to compensate for the lack of gain by means of a pre-driver.



A welcome side effect of a TIS gain of just 1x is that you don't ne
Instead, it's defined by the tail current of the IPS. More precisely, it'
On the other hand, the limited gain has a marked effect on the eff
increasing the loop gain, it is only effective if there is enough gain
lowered by means of TMC.
Another point of concern is an increase in THD when the inputs c
and R1=400 then THD20k = 123ppb. These issues will be remedied in

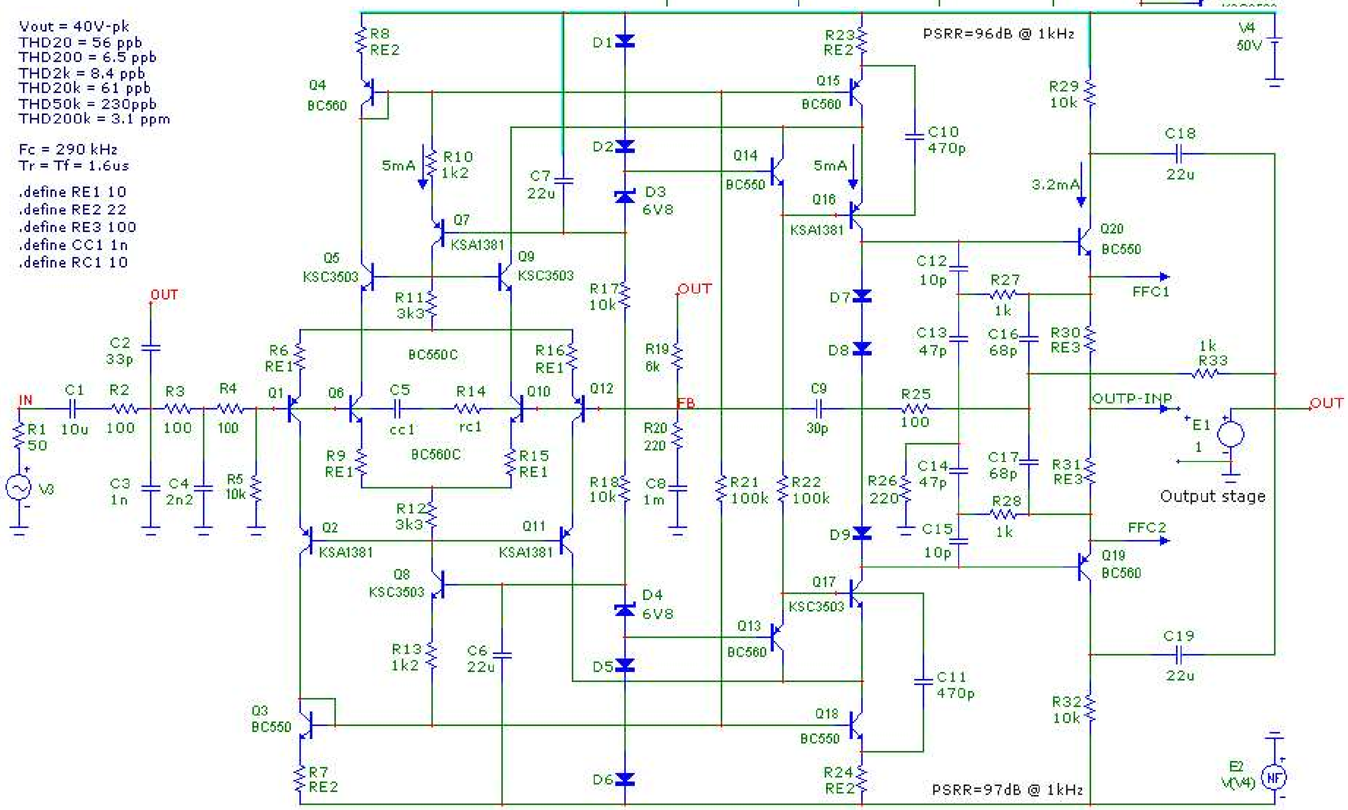


Fig. 6 Implementation of the Super TIS including input LP filter, cascodes and pre-drivers.

Circuit Description

Why cascodes

Under perfectly balanced conditions of the IPS the Early effect and nonlinear Cob don't affect the performance. In that case there is no need for cascodes. However, we do not always know the output impedance of the pre-amp to which this circuit is connected and if we know, it's a bit cumbersome to adjust R1 to the right value. Keeping Vce constant by means of cascodes avoid these issues.Opposed to the first circuit, varying R1 from zero to 400 Ohms has hardly any effect on the distortion.

Bias Q13 & Q14

Q13 and Q14 need some bias current, of course. This current, defined by R22, not only depends on the supply voltage, but it also subtracts from the TIS standing current. It's the latter we don't want. Therefore R21 is added to compensate for this dependence. Now, any current substracted from the TIS is at the same time added to the TIS via the current mirrors, giving a net result of zero deviation.

Taming the super pair

Due to positive feedback of the base currents, Baxandall super pairs tend to be unstable. This becomes apparent by some peaking of the gain at tens of MHz when the TIS output isn't loaded by any shunt compensation. Capacitors C10 and C11 diminish the amount of positive feedback to a safe level and prevent oscillations at high frequencies. With the shunt compensation in place however, the peaking has also gone. Nevertheless, I have kept C10 & C11 to be on the safe side.

Input Low Pass Filter

The objective of this filter is twofold: Preventing HF ingress and limiting the slew rate. As this front-end is intended to drive a MOSFET OPS some caution is in order. The higher the SR, the higher the gate currents and the higher the stress on the drivers. So reducing the SR from 500V/us to 50V/us (that's more than adequate for an audio amp) will also reduce the peak current of the drivers by a factor of ten. As a result, one can use smaller (and faster) drivers. A second-order filter is used as this one, in contrast to a first-order filter, limits the SR far better at the onset of a large and steep impulse. Since this is the moment where Vce of the drivers is at it highest, such filter does a better job of limiting the current as well as the power dissipation (courtesy of Andy Connor).

TMC

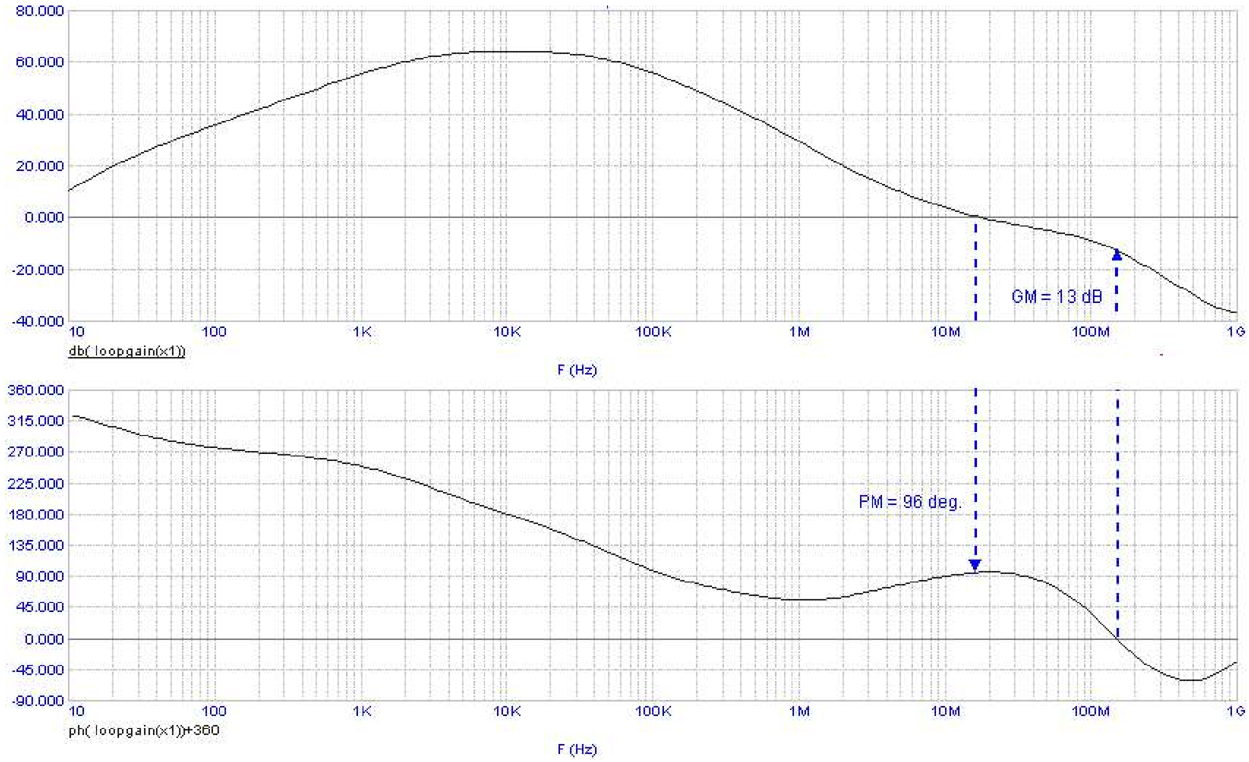
As the first circuit lacks some Miller loop gain, this has been remedied in the second circuit by including the pre-drivers into the Miller loop. See C16 and C17 which are connected to the emitters of Q19 and Q20. But leaving the TIS output unterminated (with a capacitive load) is not a good idea, as the HF response will be ill-defined (mainly by parasitic stray capacitances). In order to define and limit the gain at HF, the TIS output has to be terminated by some capacitve load, in effect shunt compensation. However, a simple (first-order) shunt compensation would decrease the loop gain at audio frequencies too much again. So I have opted for a second-order compensation. At HF the compensation is defined by C12 ... C15 & R26, while at AF it has hardly any effect, as the whole network is bootstrapped by the pre-driver emitters via R27 & R28.

Bootstrapped collectors of the pre-drivers

Since the TIS exhibits an extreme high output impedance (that is, without frequency compensation), it is very sensitive to the nonlinear Cob of the pre-drivers. As a matter of fact, it would put the whole project in peril. This can be avoided simply by bootstrapping the collectors of the pre-drivers, see C18 & C19.

Some Specifications

THD20k at Vi = 1.47V-pk: 61ppb, mostly 2nd and 3rd harmonics and independent of Ri (within certain limits, of course).
THD200k at Vi = 1.47V-pk: 3.1ppm.
Slew Rate without input filter: max. 500V/us.
With input filter: Tr = Tf = 1.6 us (slew rate is meaningless).
Filter cut-off frequency: 290kHz.
Max. output voltage at node out: +/- 47.5V;
Max. voltage at node A: +49V. Thus almost rail to rail.
BTW, the front-end of Bob Cordell's EC amplifier, a non-complementary design of the same complexity, distorts 1ppm at 20kHz.



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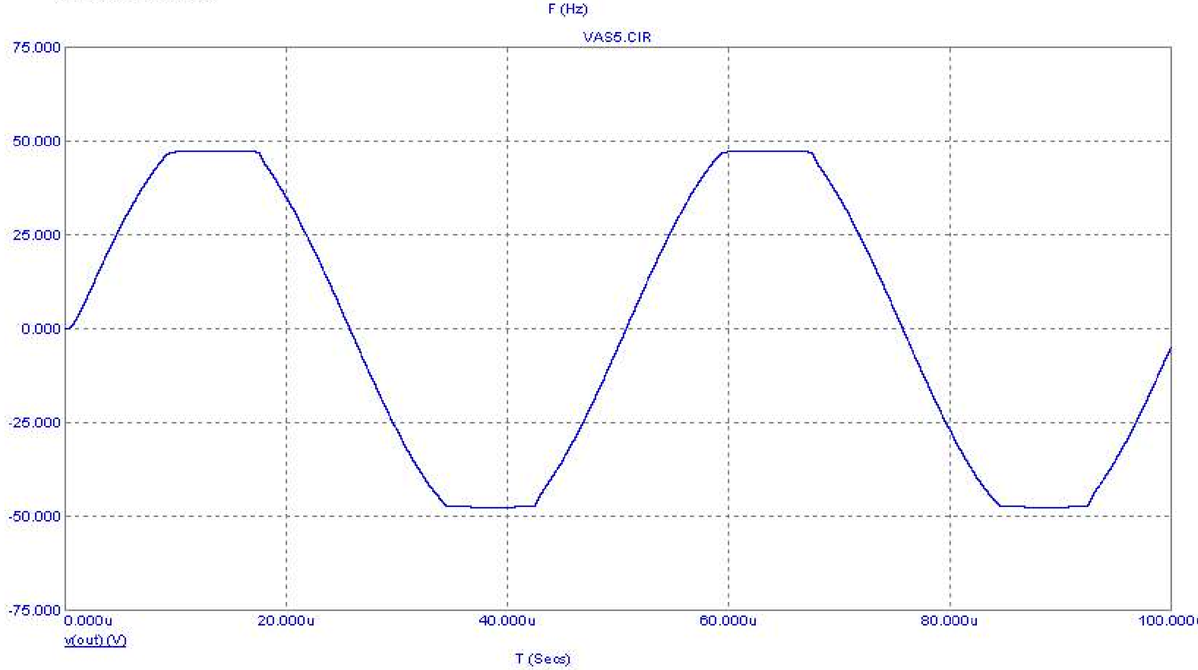


Fig.8. Clipping behavior at 20kHz from amp fig.6.

How it should not be done, way too complex:

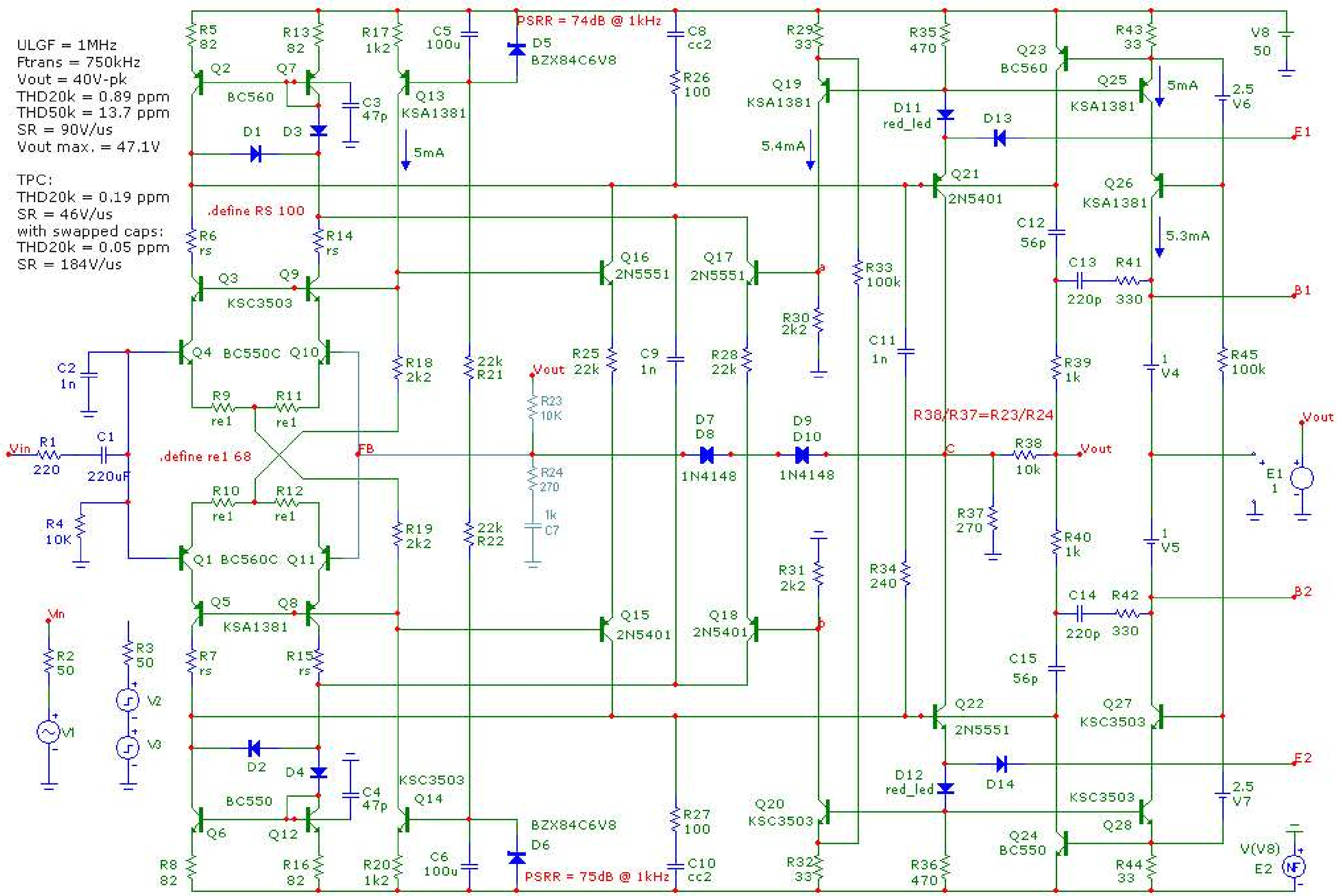


Fig.9. A fully symmetrical front-end using more traditional techniques and complemented with a CMCL to stabilize the VAS current. By now **totally obsolete!**

What we have gained

One may ask what we have gained with the Super TIS. Well, a lot. Let's compare it to a more traditional approach of a full fledged symmetrical front-end, i.e. one with IPS- and VAS-cascodes, a CMCL, protection of the VAS and provisions for an active clamp, see above, fig.9.

First, it uses almost twice as much components. Second, the performance lags far behind. Using TMC, the distortion at 20kHz is more than ten times higher and the maximum slew rate five times lower.

Using TPC with the same capacitors (fig.10) THD figures do improve, though not to the same level as the Super TIS. The slew rate however, dropped to 46V/us and the step response looks ugly.

With swapped TPC capacitors (fig.11, courtesy of Harry Dymond) THD figures come close to the performance of the Super TIS, though the slew rate still lags behind with 184V/us versus 500V/us of the Super TIS.
By the way, who says that the TPC capacitor ratio (C21:C13) is totally irrelevant?

While the circuit of fig.9 needs VAS protection (by means of Q23 & Q24), the Super TIS doesn't need that, as it's self-limiting (governed by the LTP current sources).

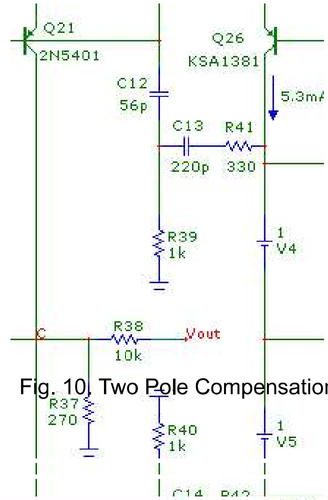


Fig. 10. Two Pole Compensation (TPC)

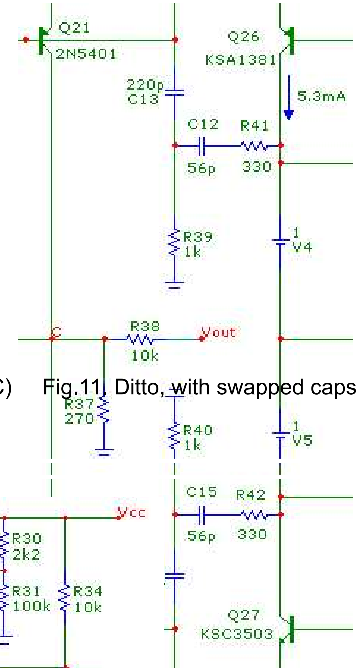
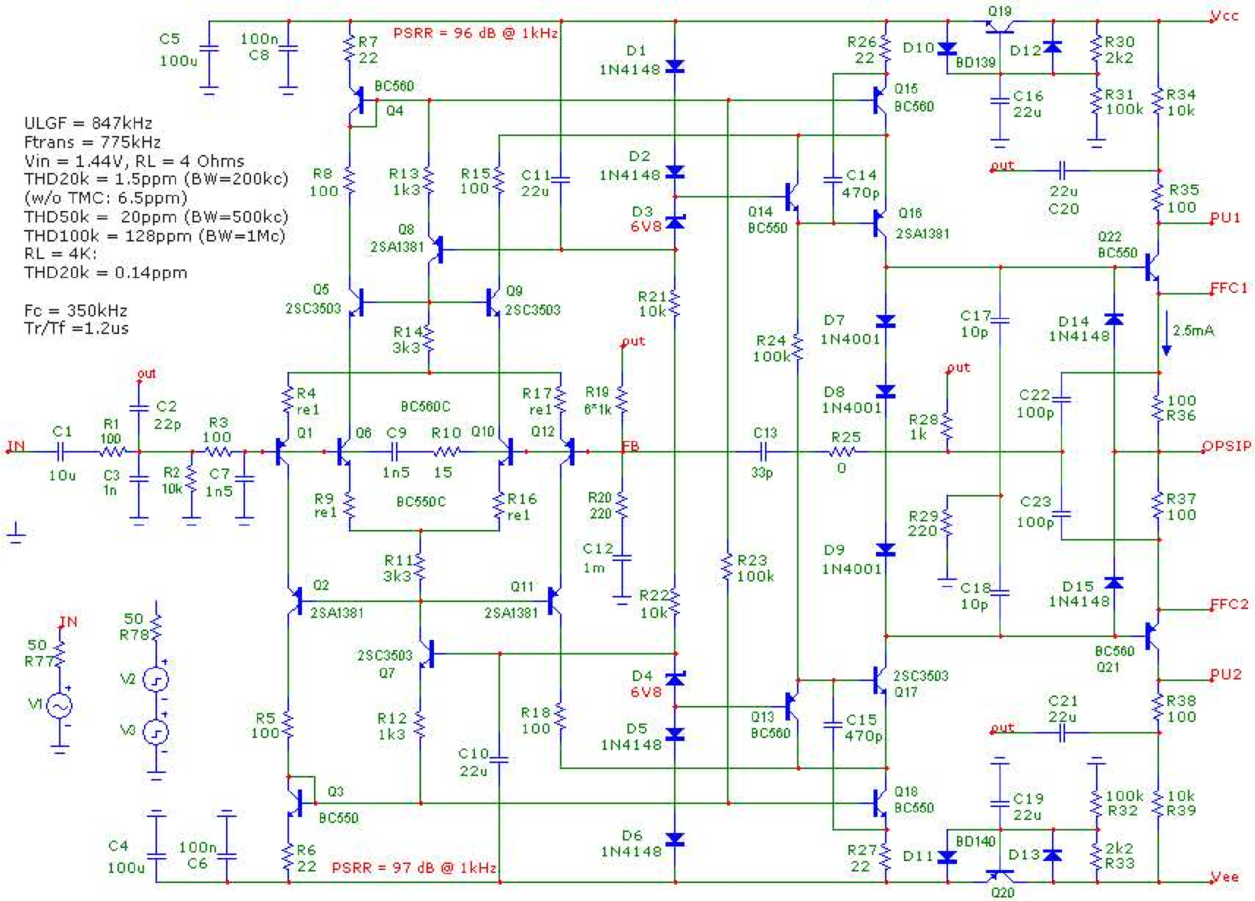
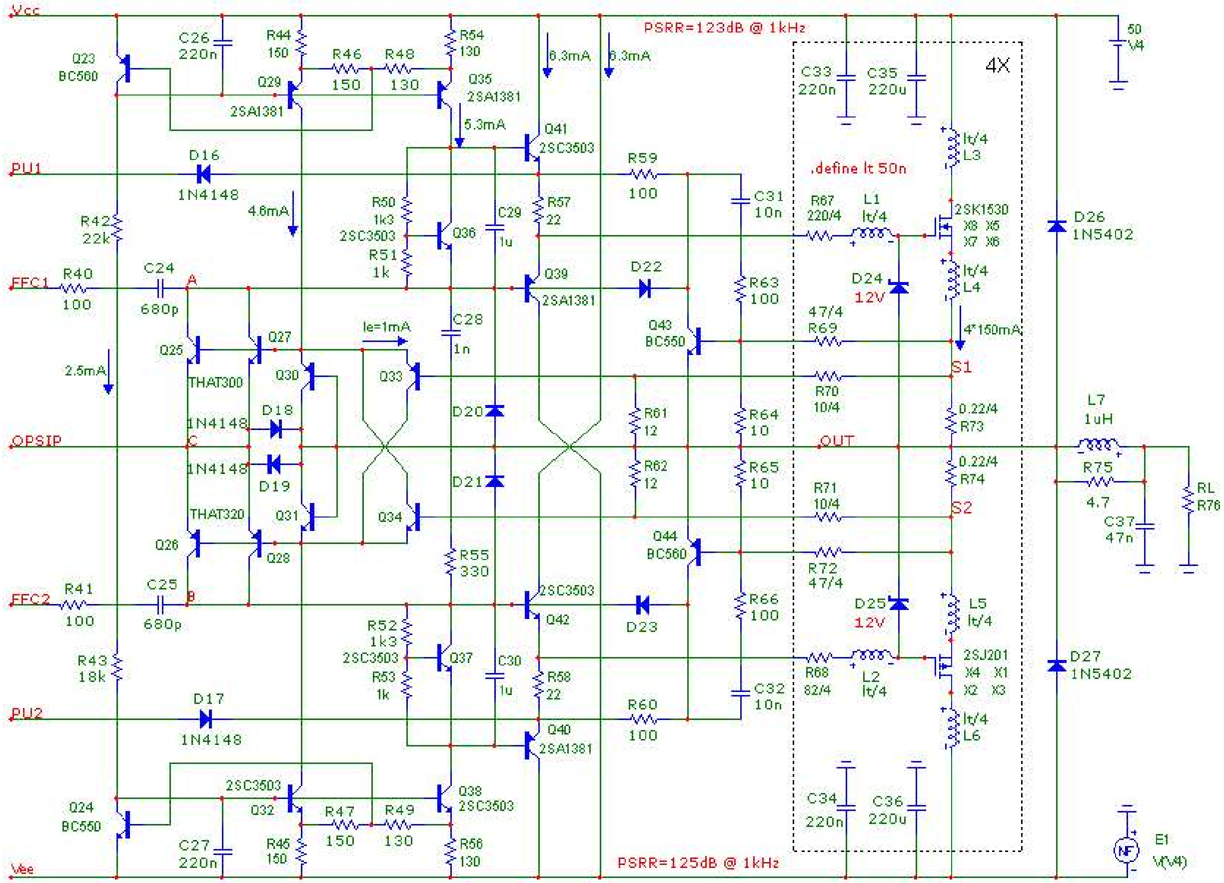


Fig.11. Ditto, with swapped caps




PSRR=123dB @ 1kHz
PSRR=125dB @ 1kHz
4X
.define lt 50n
Vcc
Vee
PU1
PU2
FFC1
FFC2
OPSIP
OUT
6.3mA
5.3mA
4.6mA
2.5mA
Ie=1mA
4*150mA
S1
S2
A
B
C

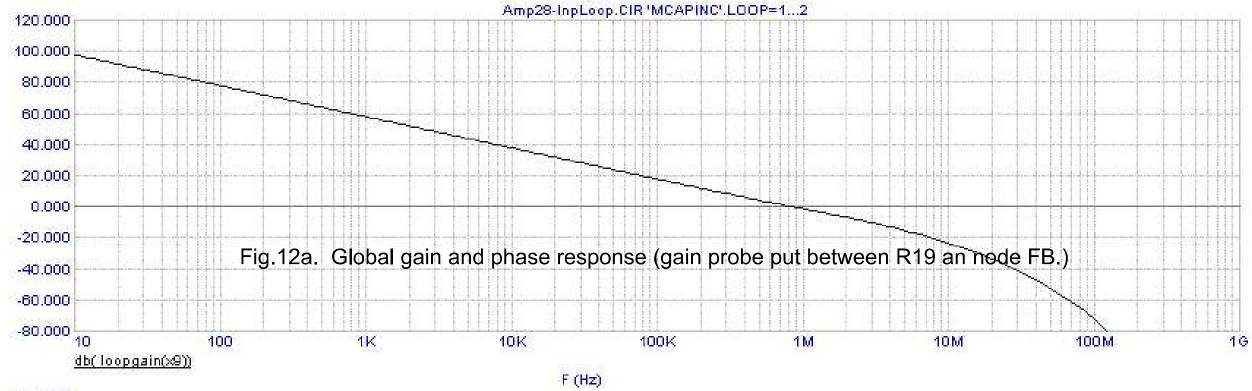


Fig.12a. Global gain and phase response (gain probe put between R19 an node FB.)

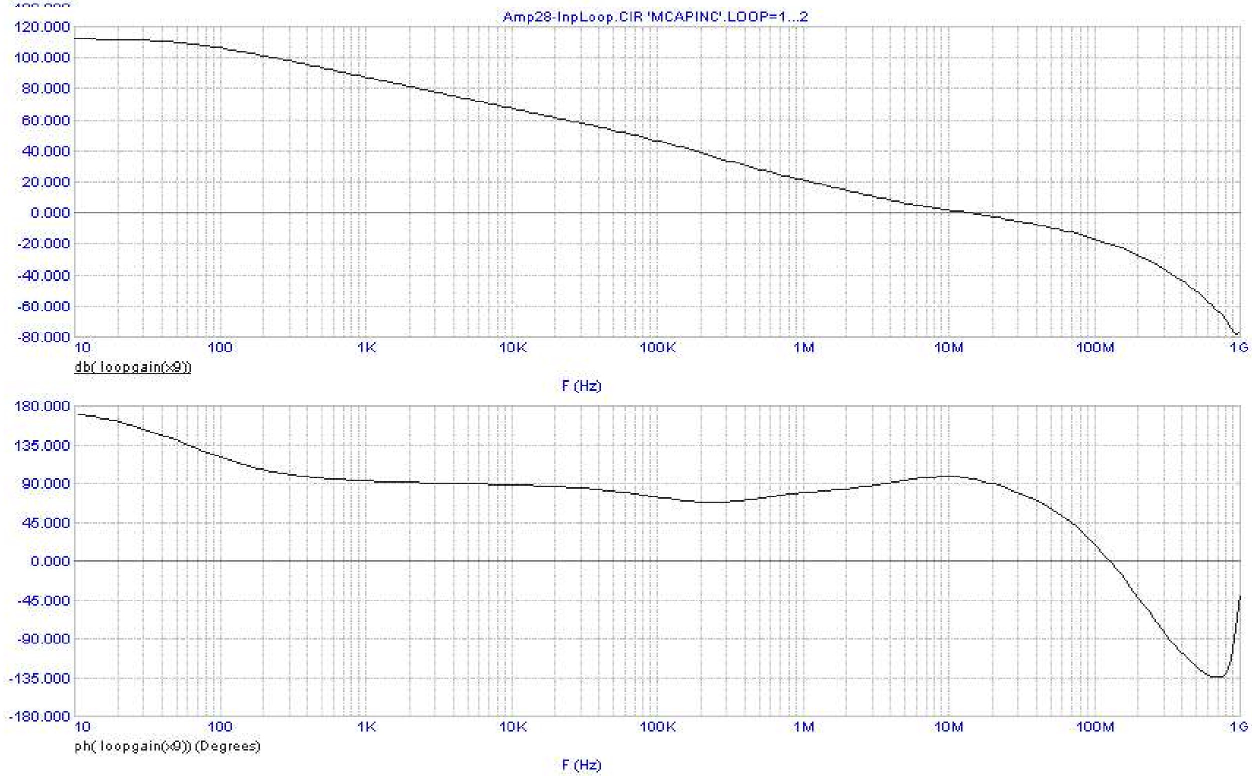
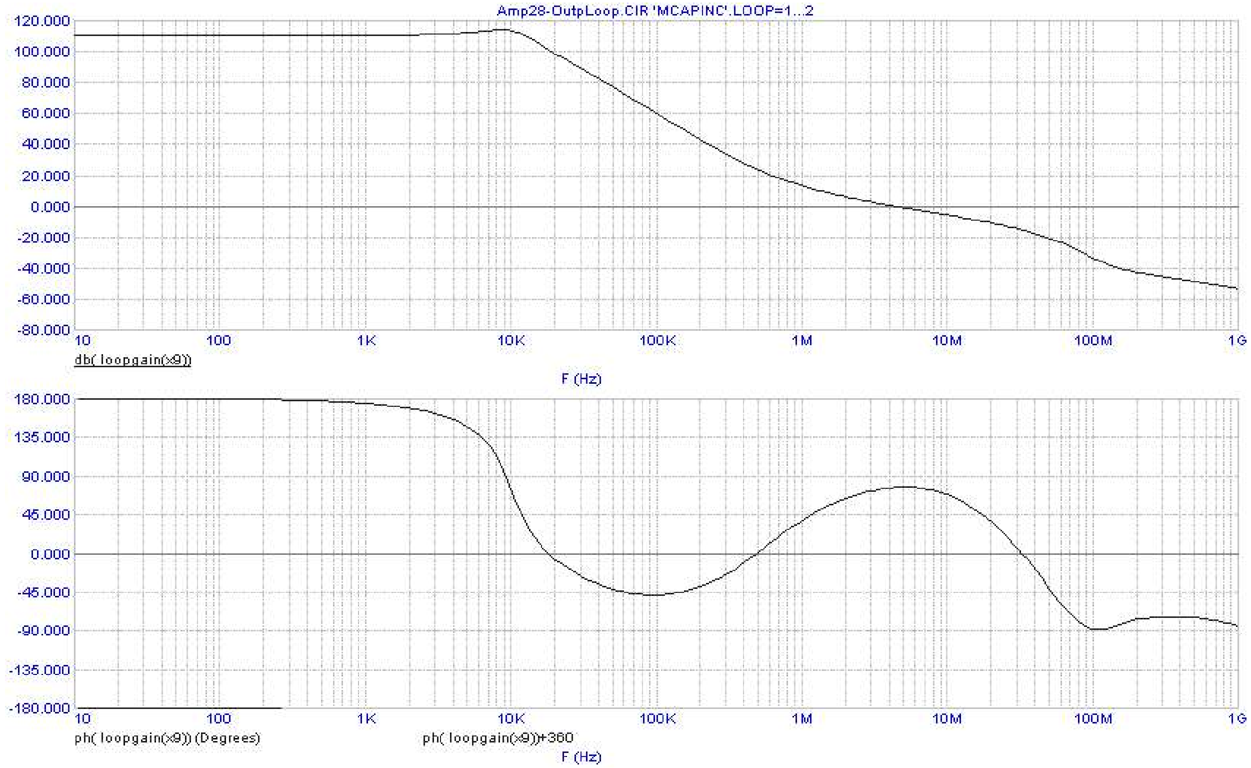


Fig.12b. Input gain and phase response (gain probe put between base of Q12 and node FB)


Amp28-OutpLoop.CIR 'MCAPINC'.LOOP=1...2
120.000
100.000
80.000
60.000
40.000
20.000
0.000
-20.000
-40.000
-60.000
-80.000
10
100
1K
10K
100K
1M
10M
100M
1G
db(loopgain(x9))
F (Hz)
180.000
135.000
90.000
45.000
0.000
-45.000
-90.000
-135.000
-180.000
ph(loopgain(x9)) (Degrees)
ph(loopgain(x9))+360
F (Hz)

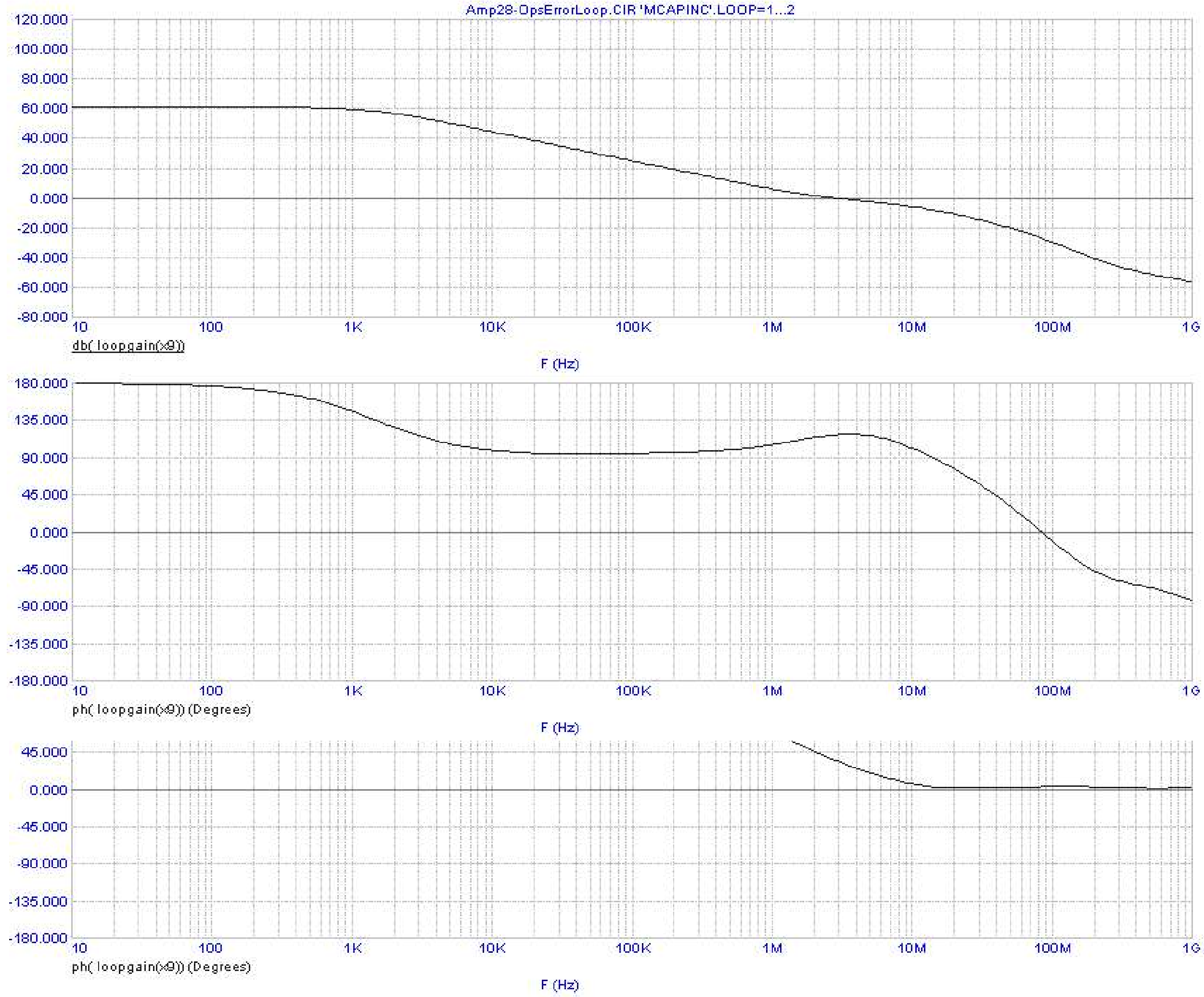


Fig.12e. Auto bias common mode gain and phase response (gain probe put between R63 and R72)
This loop controls the quiescent current of the output stage.

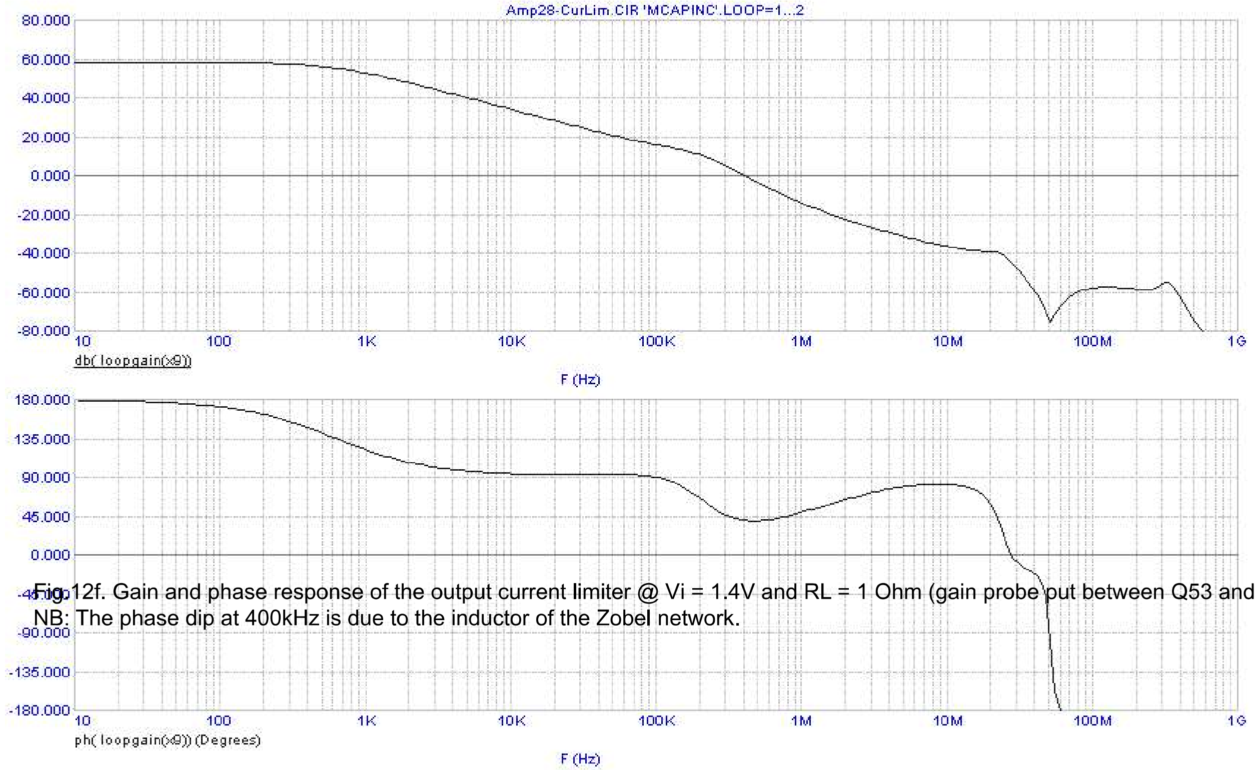


Fig.12f. Gain and phase response of the output current limiter @ Vi = 1.4V and RL = 1 Ohm (gain probe put between Q53 and R71)
NB: The phase dip at 400kHz is due to the inductor of the Zobel network.

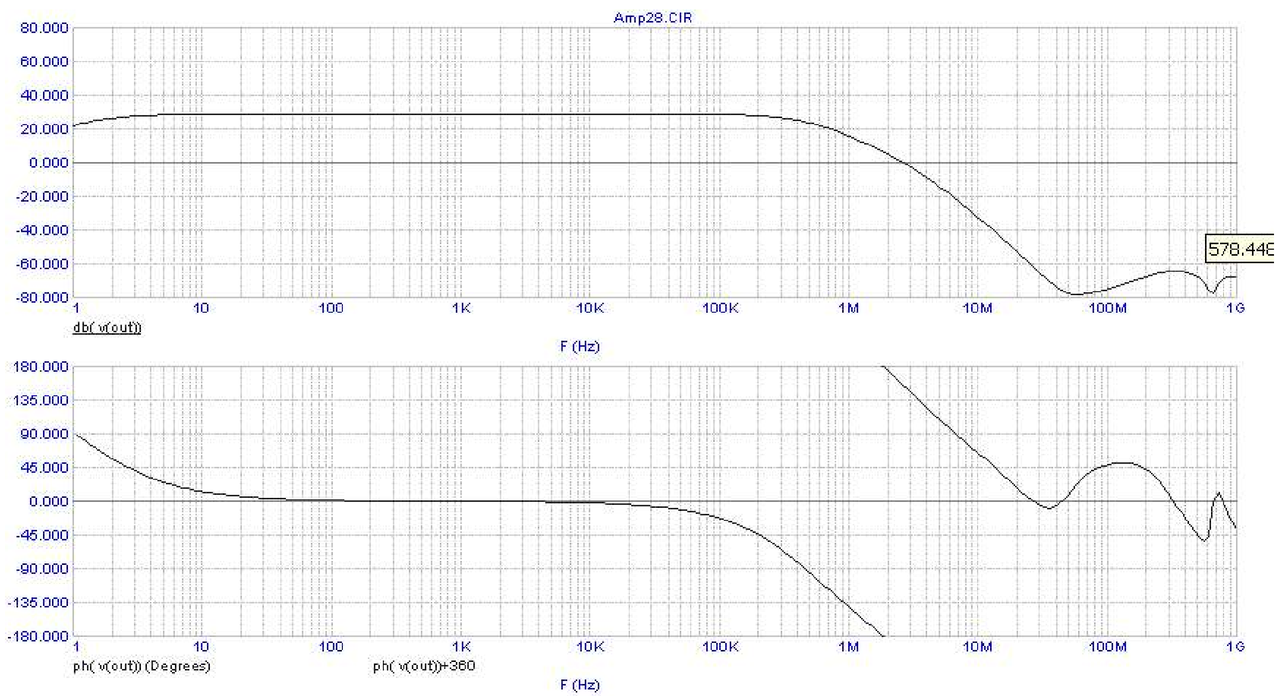


Fig.12g. Closed loop gain and phase response simulated before the Zobel network.

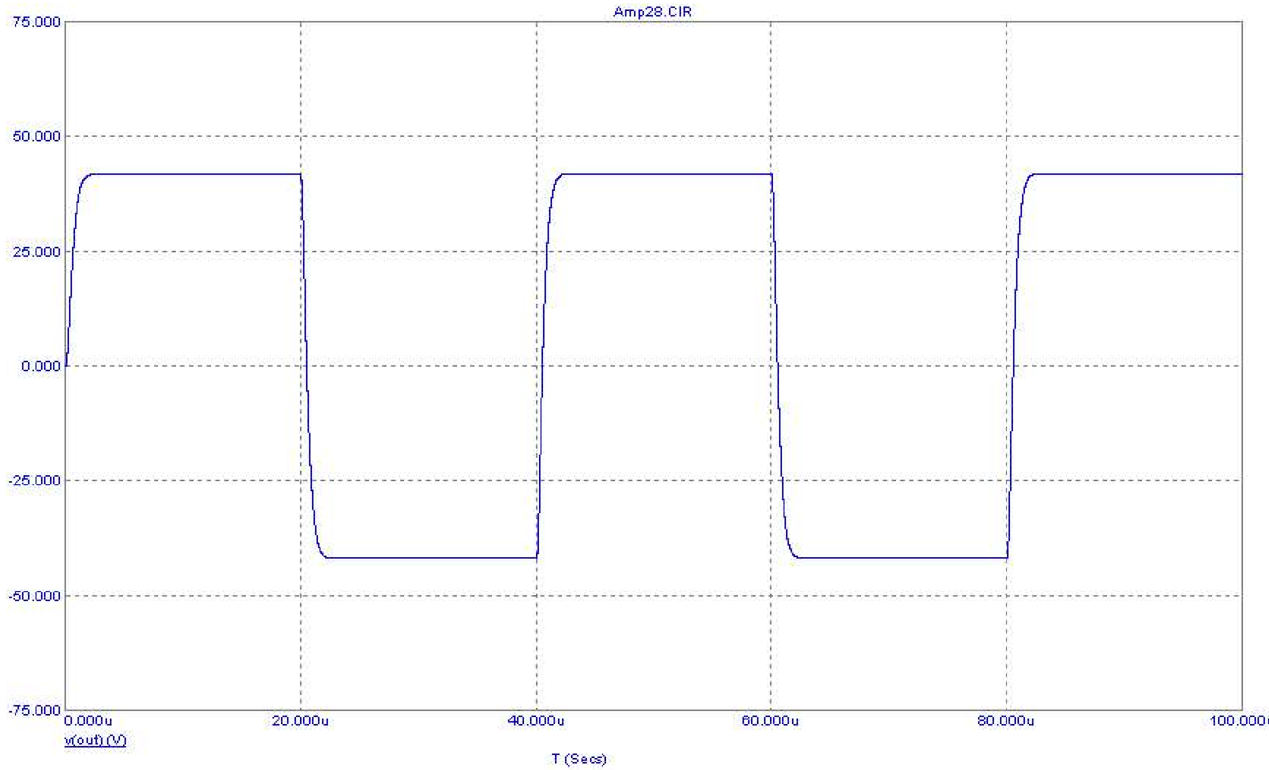


Fig.12h. Closed loop step response simulatd before the Zobel network.

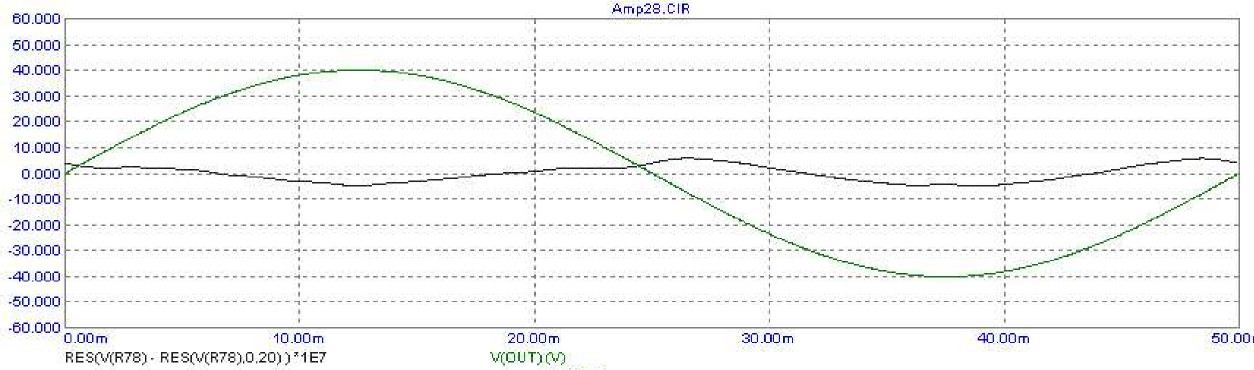
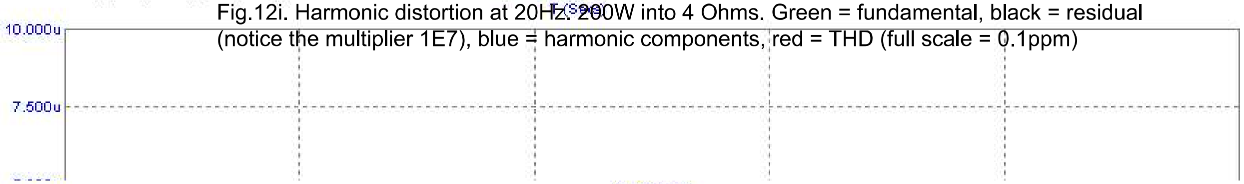


Fig.12i. Harmonic distortion at 20Hz. 200W into 4 Ohms. Green = fundamental, black = residual (notice the multiplier 1E7), blue = harmonic components, red = THD (full scale = 0.1ppm)



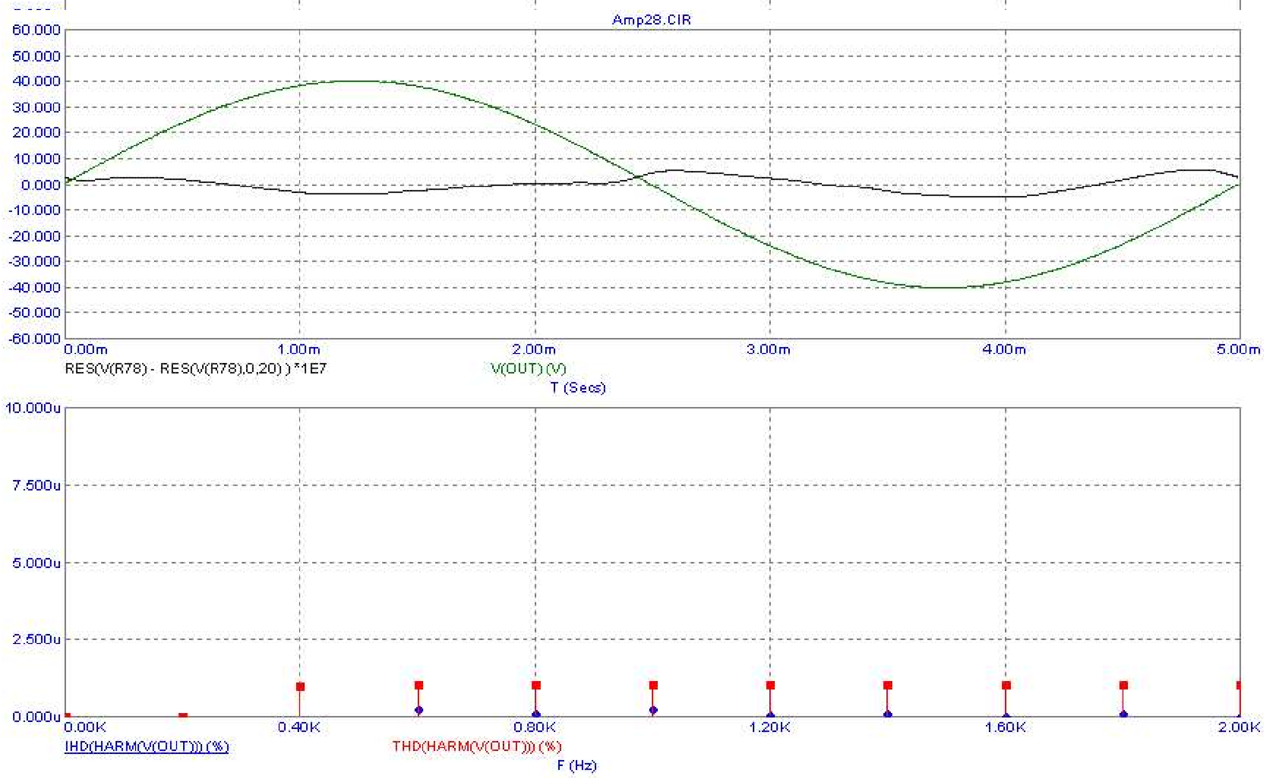


Fig.12j. Harmonic distortion at 200Hz. 200W into 4 Ohms. Green = fundamental, black = residual (notice the multiplier 1E7), blue = harmonic components, red = THD (full scale = 0.1ppm)

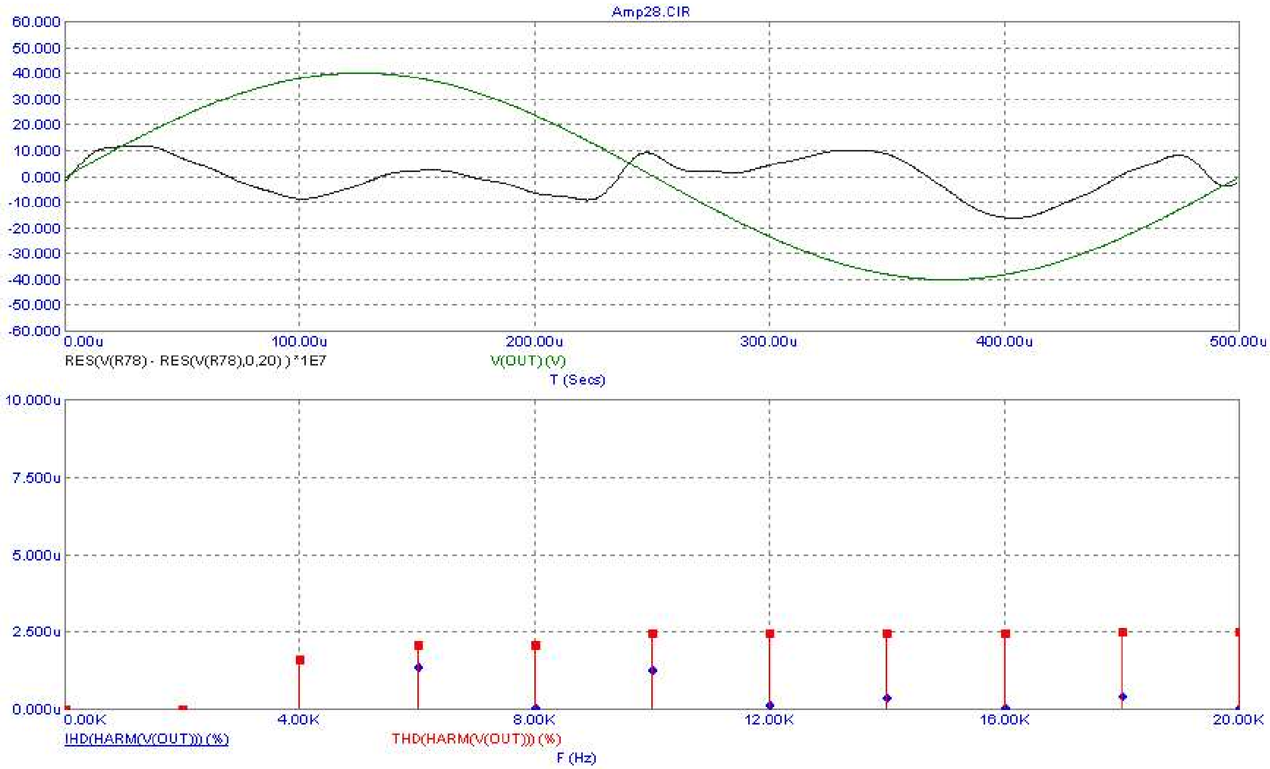
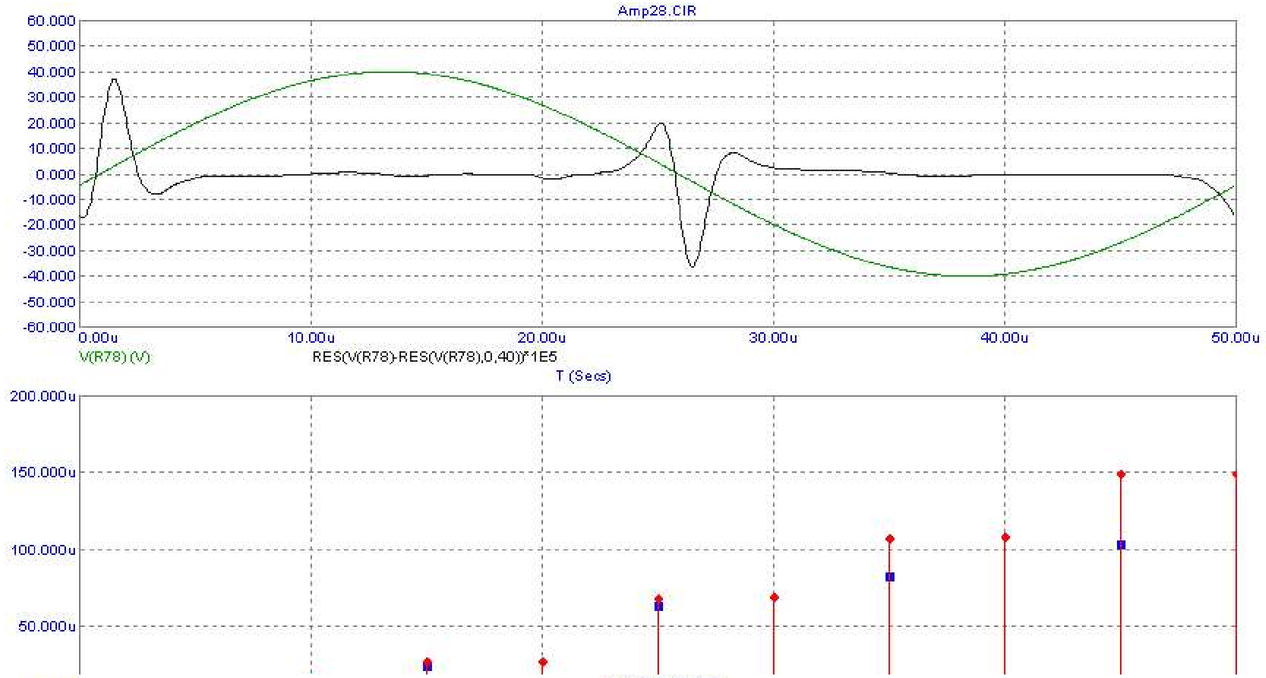


Fig.12k. Harmonic distortion at 2kHz. 200W into 4 Ohms. Green = fundamental, black = residual (notice the multiplier 1E7), blue = harmonic components, red = THD (full scale = 0.1ppm)


Amp28.CIR
V(R78) (V)
RES(V(R78)-RES(V(R78),0,40))*1E5
T (Secs)

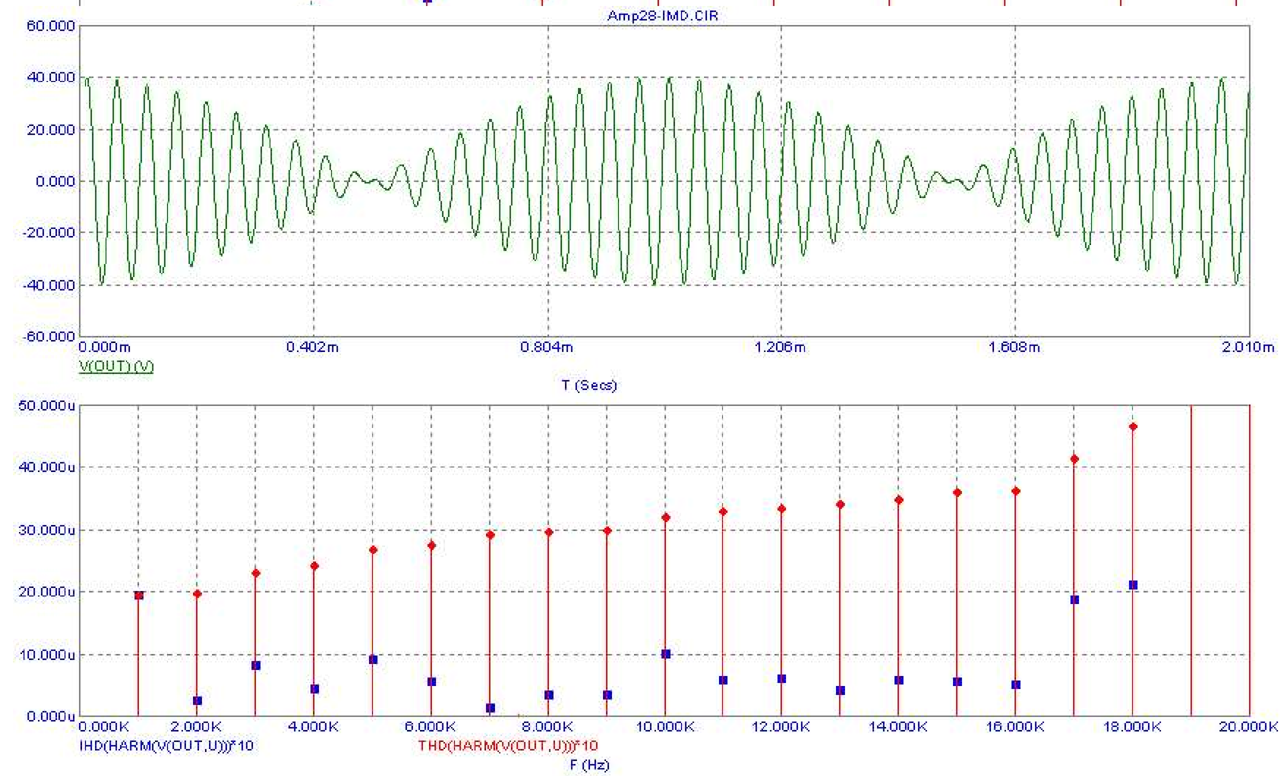

Amp28-IMD.CIR
V(OUT) (V)
T (Secs)
IHD(HARM(V(OUT,U)))*10
THD(HARM(V(OUT,U)))*10
F (Hz)

Fig.12m. ITU-R intermodulation test with two sine waves of 19 and 20kHz (green). Blue = individual IM products, blue = RMS value of IM products. Total IMD = 0.047ppm at BW = 18kHz (full scale is 0.05ppm).

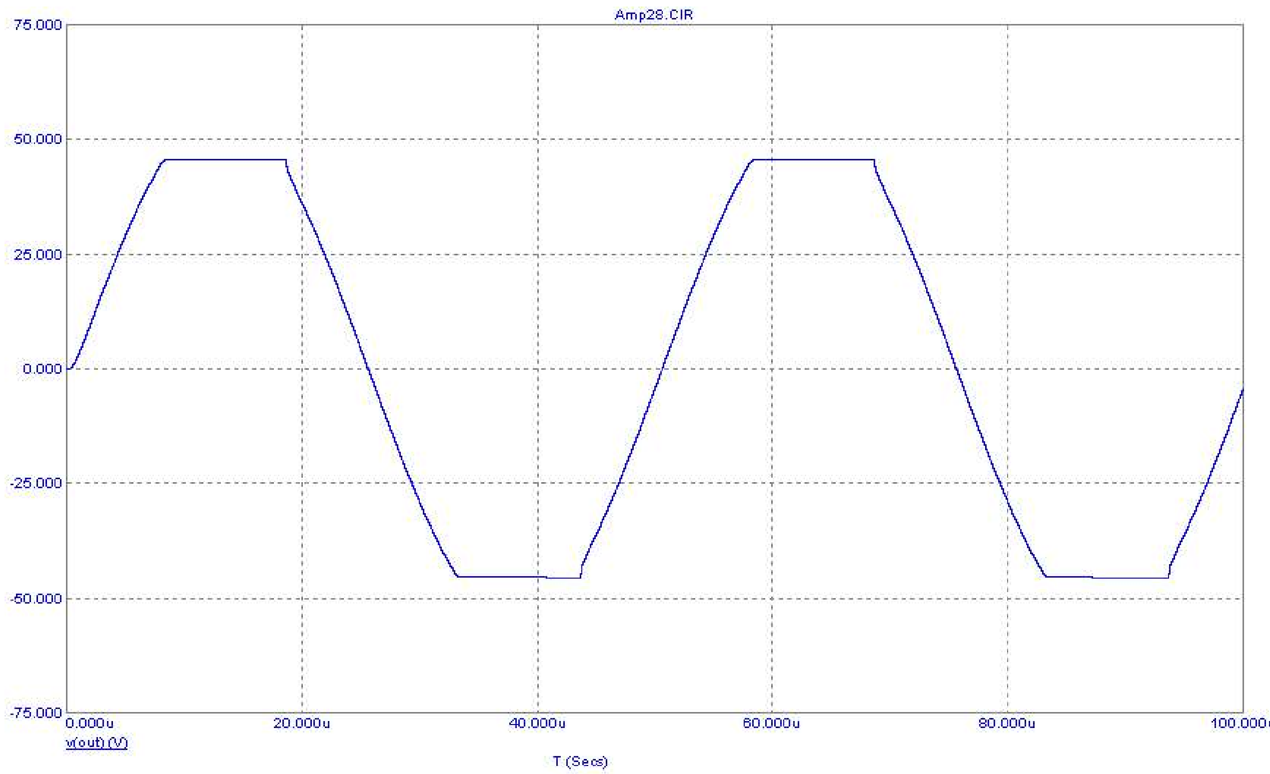


Fig.12n. Clipping behavior at Vi = 2V and f = 20kHz. Since no provisions are made to limit the output voltage to a predetermined value (for example by means of a Baker clamp), some 'sticking' is visible.

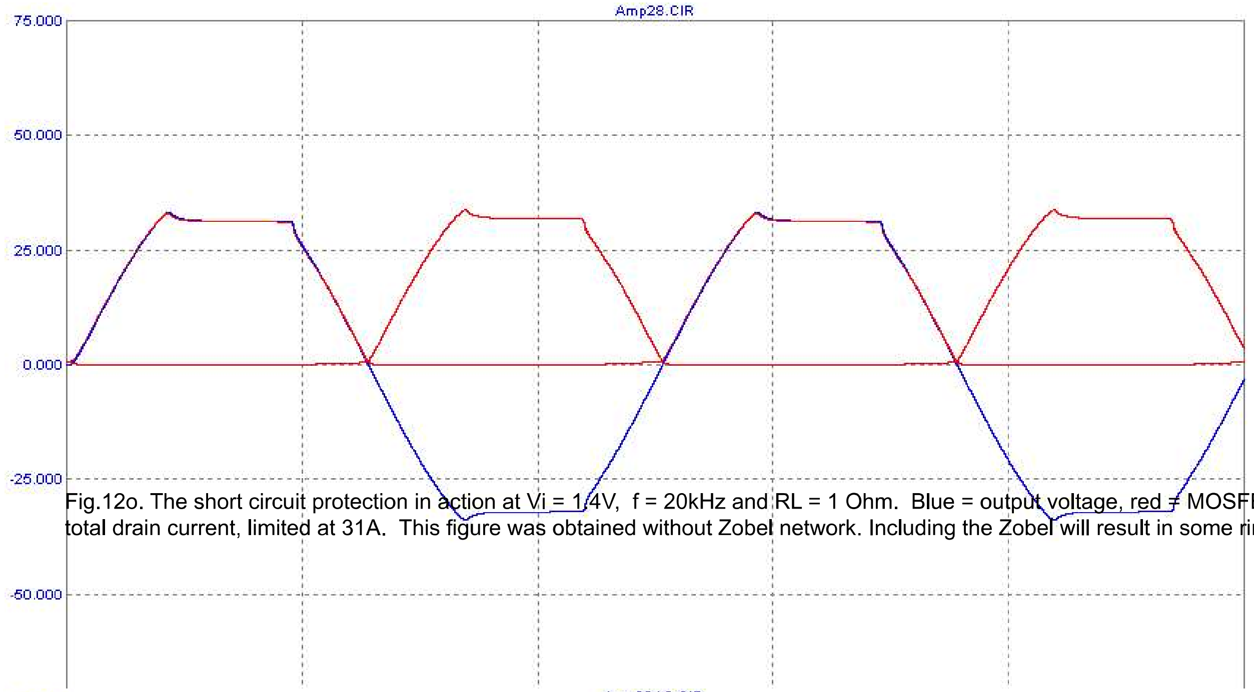


Fig.12o. The short circuit protection in action at Vi = 1.4V, f = 20kHz and RL = 1 Ohm. Blue = output voltage, red = MOSFET total drain current, limited at 31A. This figure was obtained without Zobel network. Including the Zobel will result in some ringing.

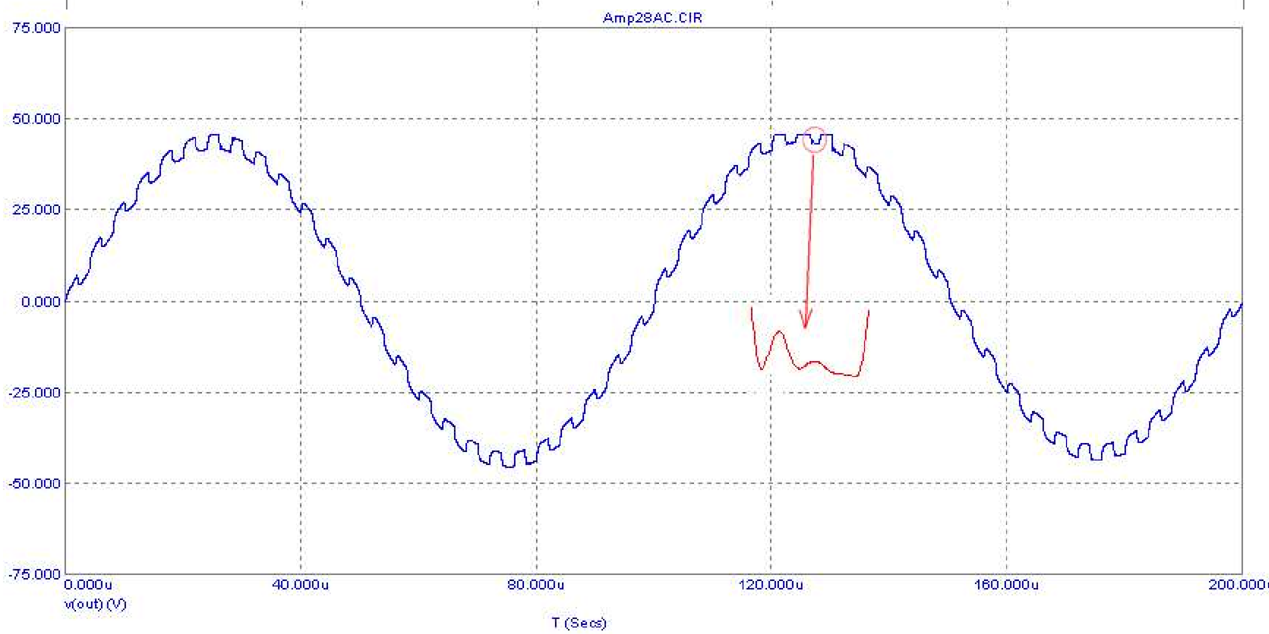


Fig.12p. The 'R.C. Bowes stability test'. A small 250kHz square wave is superimposed on a large 10kHz sine wave. In this away instabilities at many different output levels are easily detected. Near clipping some ringing occurs, see red detail. Notice that for this test the input filter has been disabled.

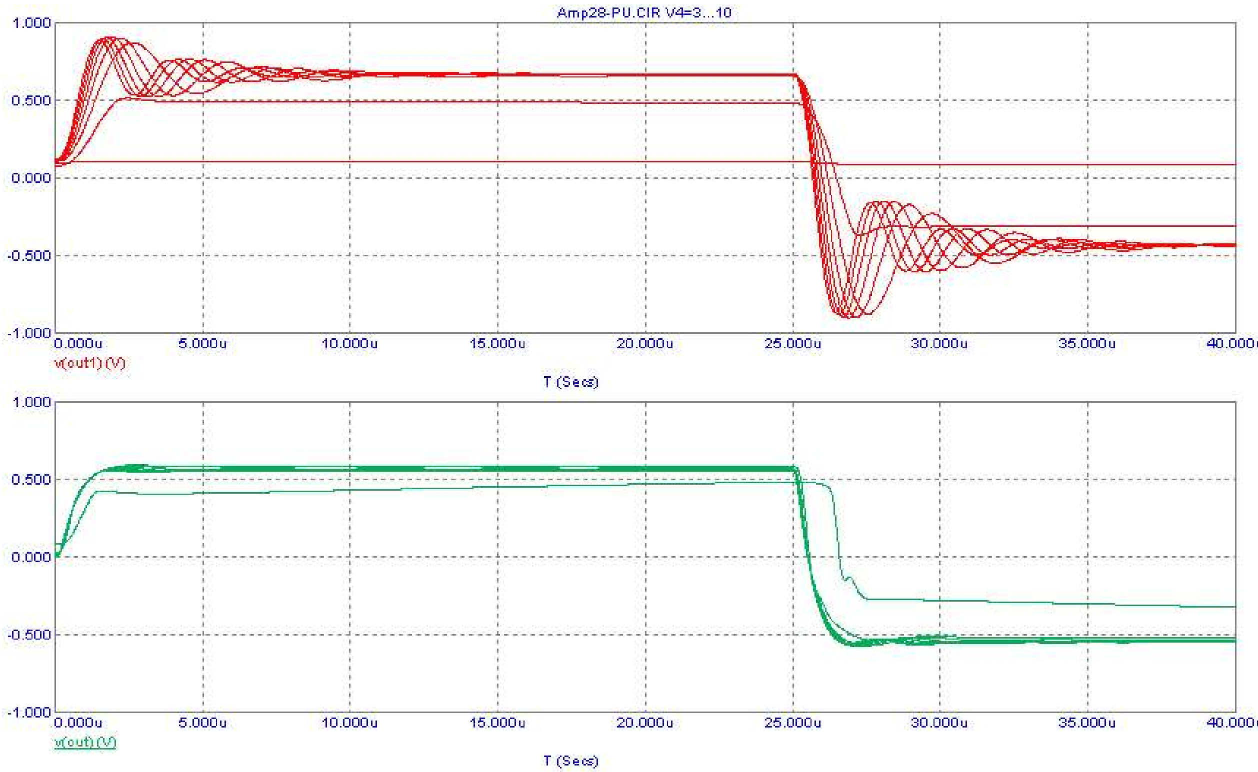
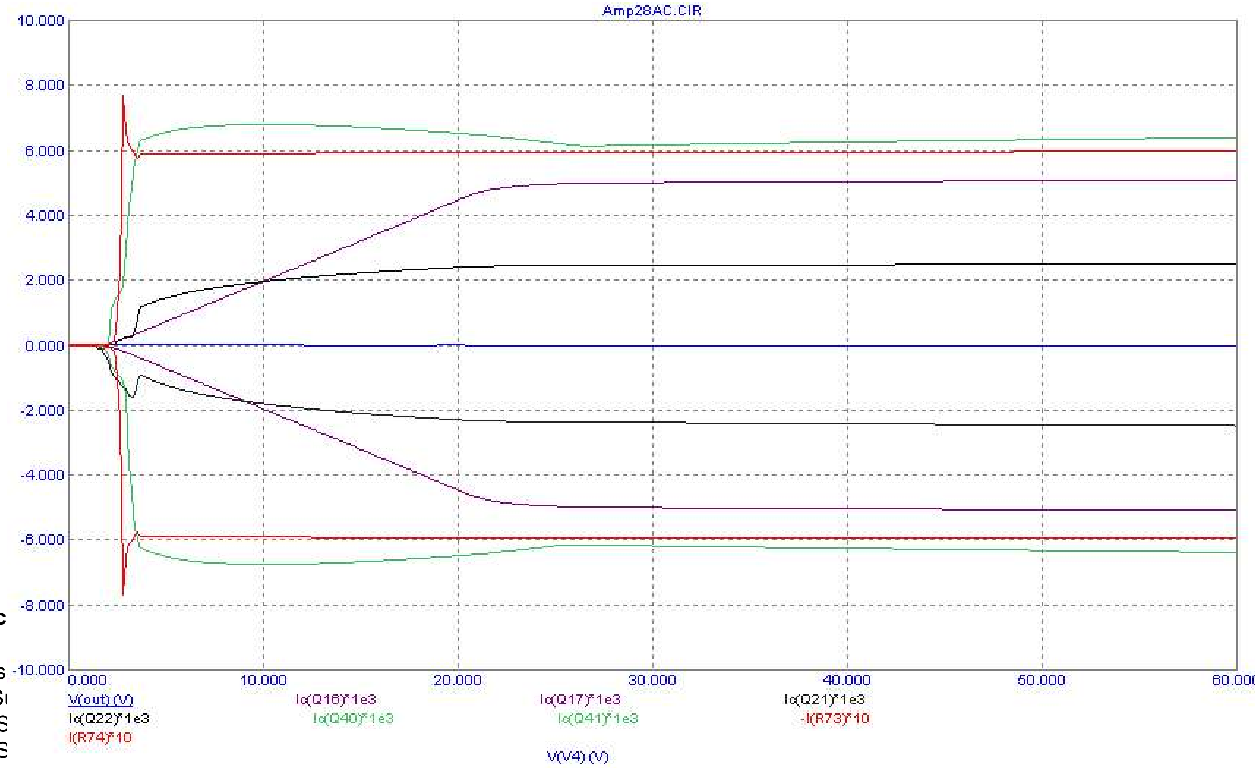


Fig.12q. Stability test during the power-on phase. Supply voltage was stepped from 3 to 10V. Input signal was a 20mV 20kHz square wave. The upper graphs show serious ringing, caused by saturation of the pre-driver transistors Q21 & Q22 at low supply voltages. Bootstrapping the collectors by means of D16 & D17 cured the instability, see lower graphs.



ain
so
to

Effec

It is s … r this claim holds
for the S…
1. A S…
2. A S…
3. The front-end of Bob Cordell's HEC MOSFET amp with a BJT input stage.
4. The front-end of Bob Cordell's HEC MOSFET amp with a JFET input stage.

First, an AM demodulation test was performed using a 1V 10MHz carrier, modulated by a 20kHz sine with a modulation depth of 70%. The 20kHz component at the output of the front-end was then 'measured' by means of an FFT.

Next, a 10MHz sine also of 1V amplitude was superimposed on an AF signal of 1V and 20kHz. This was done to figure out how much the HF signal contributes to distortion of the AF sine. Since a strong HF signal not necessarily will lead to AM detection, it may nevertheless push the audio signal into a nonlinear region. As a result, compression of the audio signal will take place. Hence a 'compression test' has been included as well.

Front-end:	SuperTIS-BJT	SuperTIS-JFET	HEC-BJT	HEC-JFET
Demodulated AM signal:	0.73mV	10.1mV	1.52V	1.27V
THD20k without HF carrier:	0.028ppm	0.071ppm	0.19ppm	0.76ppm*
THD20k with HF carrier:	0.656ppm	457ppm	161ppm	156ppm
THD20k increase:	0.628ppm	457ppm	160ppm	155ppm

These figures clearly indicate that the SuperTIS will not benefit from JFETs in the input stage.
Needless to say that in every respect the BJT version of the SuperTIS is the winner.

After a second thought, above enormous discrepancies between BJT and JFET results made me suspicious. So I decided to repeat the simulations with a smaller HF signal. This time of 100mV instead of 1V. Now we get a totally different picture:

Front-end:	SuperTIS-BJT	SuperTIS-JFET	HEC-BJT	HEC-JFET
Demodulated AM signal:	5.4uV	1.26mV	0.35mV	0.82mV
THD20k without HF carrier:	0.028ppm	0.071ppm	0.19ppm	0.76ppm*
THD20k with HF carrier:	0.030ppm	0.072ppm	0.24ppm	26.3ppm
THD20k increase:	0.002ppm	0.001ppm	0.05ppm	25.5ppm

These differences are far less extreme. Still, BJTs yield better results in both cases and the SuperTIS still outperforms the other front-end. For further reading on this topic look here, here, here and here at the diyAudio forum.

* This figure reduces from 0.76ppm to 0.23ppm if the input cascode (Q2 & Q6) is bootstrapped.

Below are the test circuits for RFI simulations.

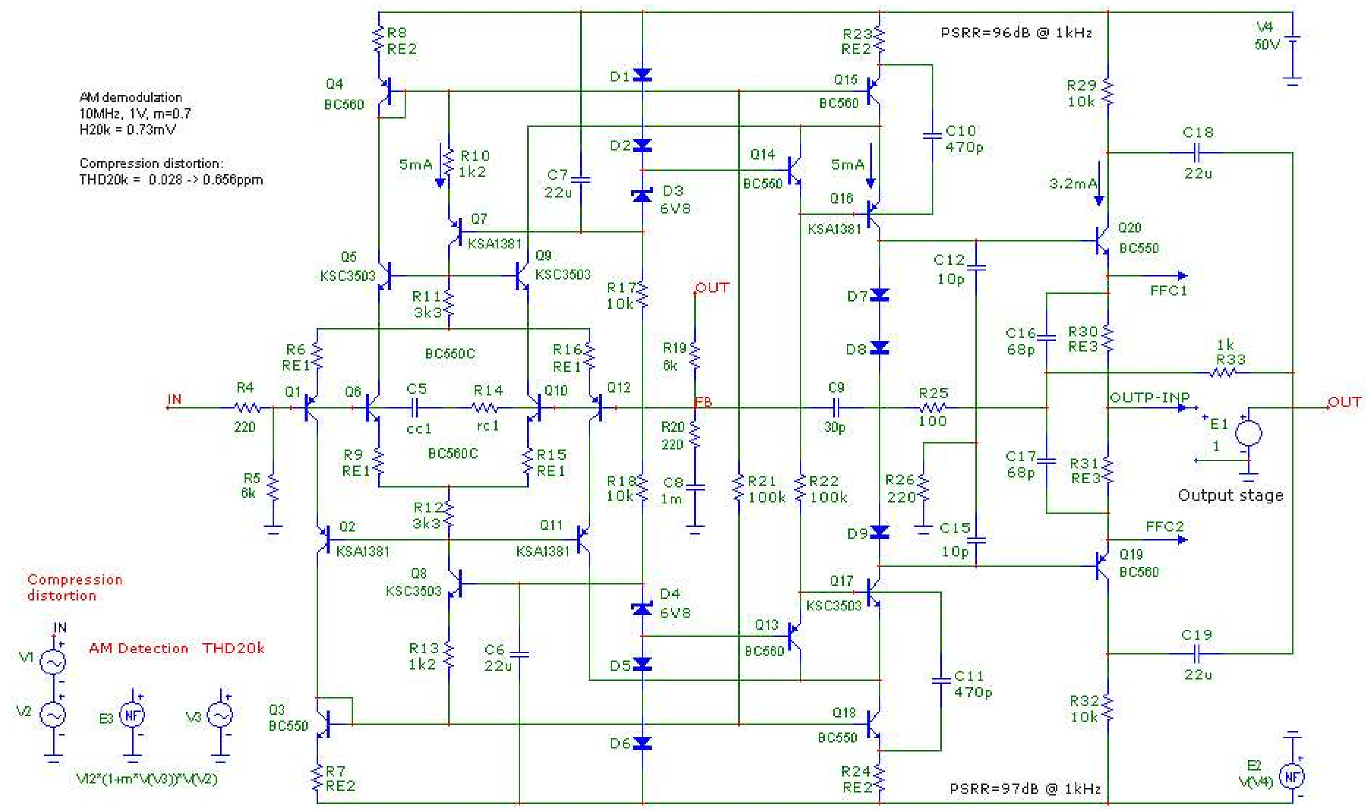


Fig.13. RFI test circuit of SuperTIS plus BJT input stage.

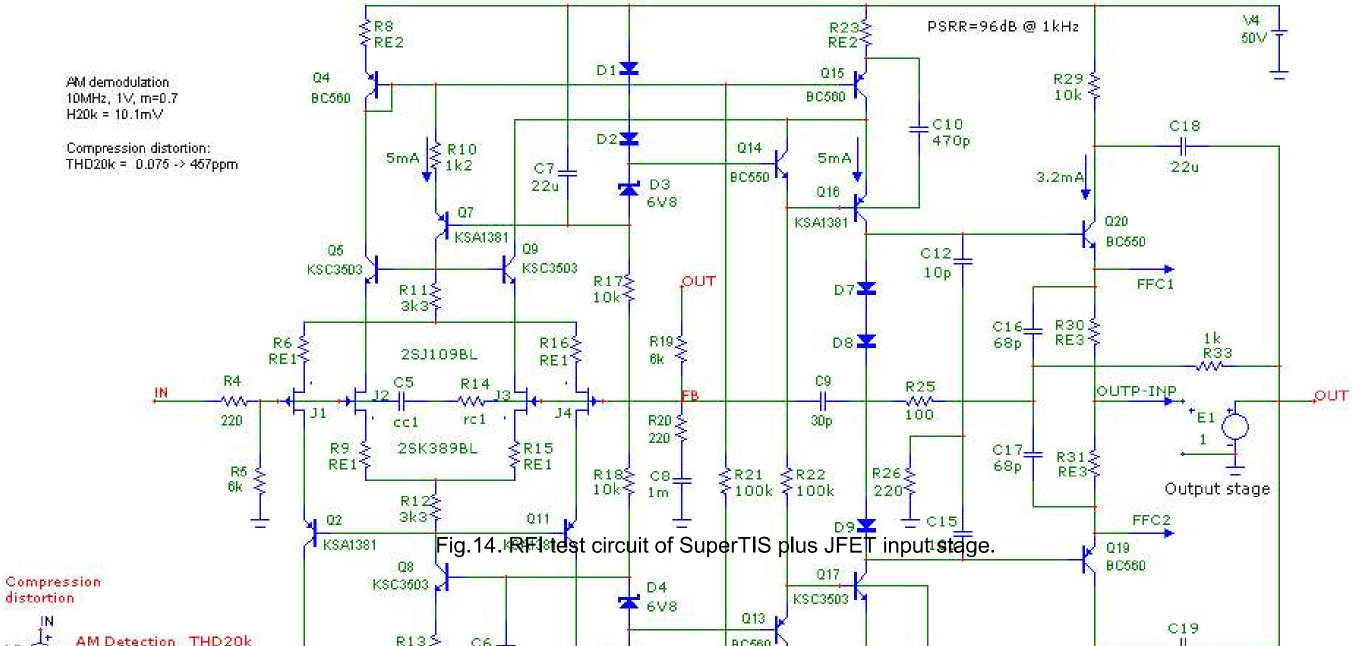


Fig.14. RFI test circuit of SuperTIS plus JFET input stage.

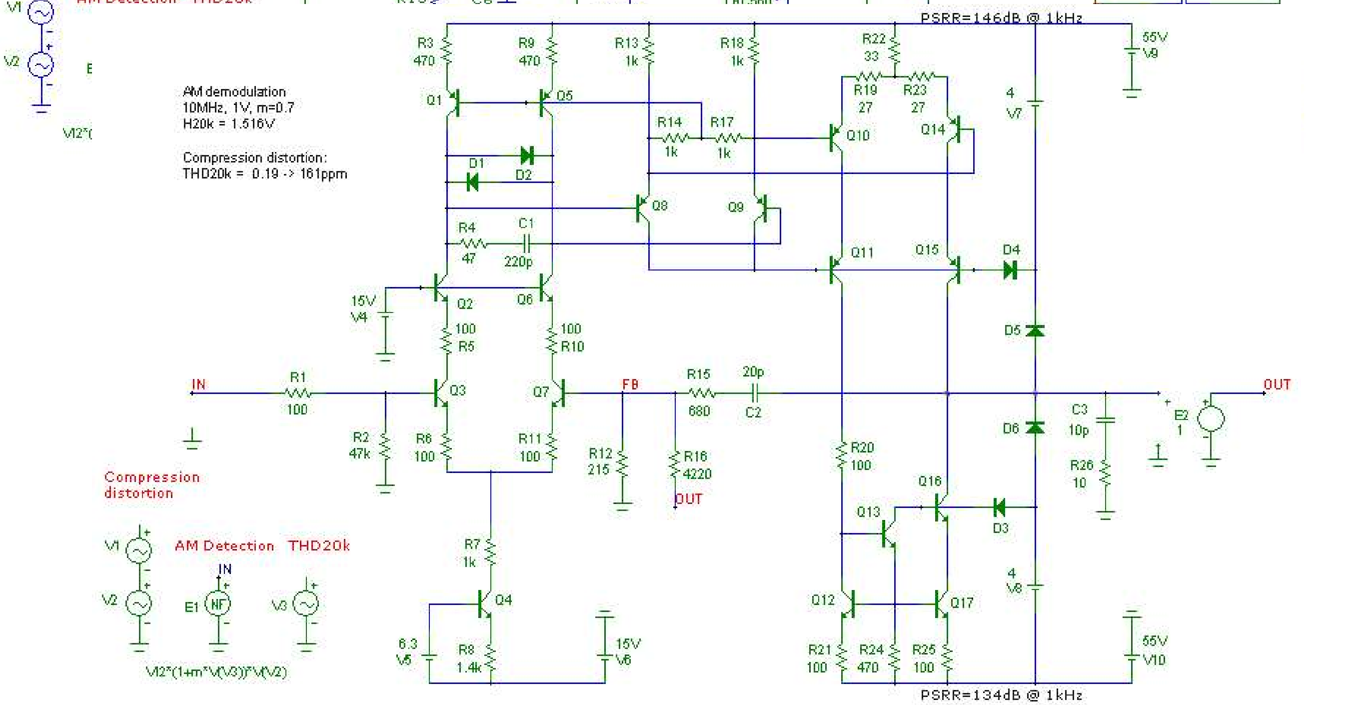


Fig.15. RFI test circuit of Cordell's HEC-MOSFET amp plus BJT input stage.

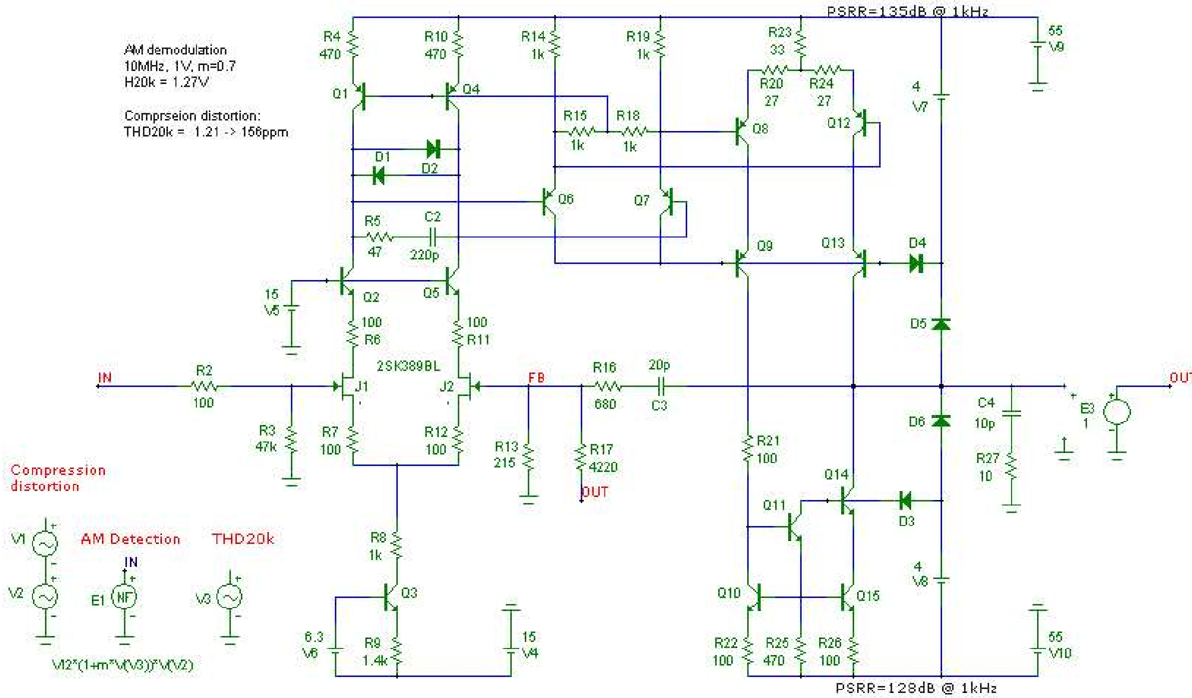
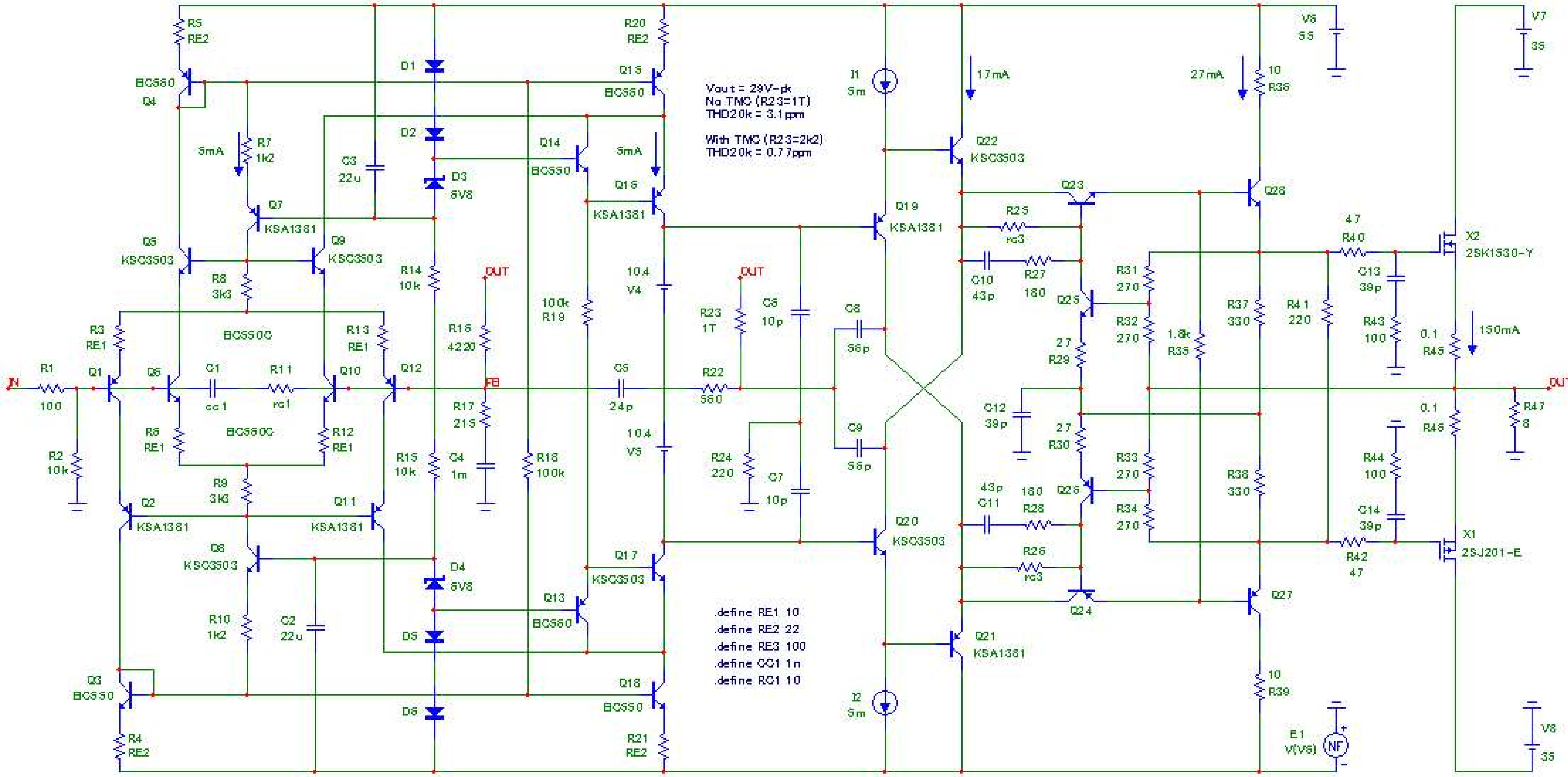


Fig.16. RFI test circuit of Cordell's HEC-MOSFET amp plus JFET input stage.



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