

# The Ovation e-Amp: A 180 W High-Fidelity Audio Power Amplifier



A high performance audio power amplifier featuring an Emitter Follower Triple output stage with jumper selectable compensation for MC or TMC and jumper selectable open loop gain and frequency bandwidth characteristics. A 5 pair EFT output stage allows this design to deliver short term current peaks approaching 40 A

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June 2012

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## 1. Introduction

The e-Amp is a 180 Watt RMS (conservatively rated into  $8\ \Omega$ ) fully balanced symmetrical ('FBS') amplifier featuring an emitter follower triple (EFT) bipolar output stage and beta enhanced VAS stage.

The amplifier can be configured using jumpers for TMC (Transitional Miller Compensation) or straight Miller compensation (MC). The VAS can be lightly loaded to reduce the overall loop gain, but increase the open loop -3 dB bandwidth to 40 kHz also using a jumper. I have called this compensation option 'Wide Band' or WB. This allows four compensation schemes to be selected – MC, TMC, WB-MC and WB-TMC. With the e-Amp, by simply inserting or removing a few jumpers it can be flipped from one compensation design another – how it is ultimately tuned, and how it sounds, is up to personal choice.

A microprocessor based protection board takes care of transformer in-rush current limiting at power-up, speaker muting (unusually, using low  $R_{ds(on)}$  Trench mosfets), over temperature, DC offsets and output short current protection.

Subjectively the e-Amp produces great imaging, a very smooth, open mid and top end with plenty of bass depth and slam. I personally doubt you could ask for anything more from a power amplifier.

I hope you enjoy reading about the Ovation e-Amp as much as I enjoyed designing, constructing and writing about it.

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## 2.Ovation e-Amp Specifications

All specifications at  $\pm 68$  V supply rail at 25 °C ambient unless otherwise stated.

Parameter	Specification	Conditions
Output Power	200 W RMS into 8Ω	20 Hz to 20 kHz; <0.1% distortion
	350 W RMS into 4Ω	20 Hz to 20 kHz; <0.3% distortion
	420 W RMS into 2Ω	20 Hz to 20 kHz; <0.4% distortion (short term capability)
	Peak $I^2R$ capability limited by power supply >> 1 KW	
Output Drive Capability	3 Ω at 60 degrees to 400 W for short periods	
	8 Ω Resistive to 200 W for extended period with specified power supply and heatsink	
Peak output Current	~40 A for <=50 ms	
Protection	Supply rails fused with 10 A fuses. MCU based protection board provides:-	
	DC offset protection; over temperature protection, over current protection; transformer in-rush limiting and speaker muting and on/off pushbutton control	
Distortion	TBC c. 30 ppm	180 W into 8Ω 20 Hz to 20 kHz
	TBC c. 15 ppm	180 W into 8Ω at 1 kHz
	TBC c. 10 ppm	100 W into 8Ω 20 Hz to 20 kHz

The above figures are with HIGH LOOP GAIN and TMC selected. With standard MC and HIGH LOOP GAIN, distortion figures are higher.

<0.01%	180W into 8Ω 20 Hz – 20 kHz
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The above figure with wide band OLG and standard MC selected

Signal to Noise Ratio	>105 dB	Ref full power output
Damping Factor	>300	1 kHz into 8 Ω
Slew Rate	155 V/ μs symmetrical	10% to 90% pos and neg; input filter disabled
Rise/Fall time (with FE filter)	<1.2 μs symmetrical	10% to 90% into 8 Ω
Frequency response	20 Hz to 20 kHz ± 0.1 dB	8 Ω, 100 W
	20 Hz to 20 kHz ± 0.2 dB	4 Ω, 200 W
	2 Hz to 350 kHz -3 dB	1 W into 8 Ω
Input Impedance at 1 kHz	10 k Ω//(470 Ω + 1 nF)	
Gain	51 x (34 dB)	1 kHz into 8 Ω
Input Sensitivity	1.27 V for full power output	
Phase/Gain Margin	MC >80 degrees p.m.; Gain margin > 35 dB; TMC >60 degrees p.m.; 20 dB gain margin	
	Stable into 2 Ω//2 μF; stable into any capacitance from 0 pF to 2 μF (2 μF was test limit)	

### 3. The e-Amp Circuit Description

Refer to Fig 1. The input (via J4) is low pass filtered through R68 and C24 and feeds into a fully balanced differential long tailed pair (LTP) consisting of the non-inverting input pair Q10 and Q13 and the inverting input pair Q9 and Q14. R61 through R63 and R65 (100 Ω resistors) provide degeneration and each NPN and PNP LTP is fed with a constant current source derived from Q4 and Q15 (PNP LTP current source) and Q3 and Q11 (NPN LTP pair current source) along with associated components. Both current sources are set for 10 mA. R6 and C22, and their mirrors R5 and C3, provide ripple and noise filtering to ensure the current sources remain very quiet and do not allow any noise into the front end through the power supply rails.

The output current from the non-inverting input pair (Q10 and Q13) feeds into the VAS stage via cascode transistors Q32 and then to R72 for the positive signal side and Q33 and then to R71 for the negative signal side. R41, R83 and C31 and C32 form base stopper networks, designed to prevent HF oscillation, which you can read about here: [Cascode-Oscillation-in-Audio-Amplifiers1.pdf](#). The inverting input transistor pair (Q9 and Q14) collector output currents connect via cascode transistors Q33 and Q34 to the VAS emitter degeneration resistors R59 and R69, a technique that helps to improve distortion performance.

In this design, the feedback is capacitively coupled via C7 and C23. The offset with this configuration is typically around 2 ~ 3 mV if you match the front-end LTP transistor hFEs to within 10% and when unmatched, you can expect an offset of around 10 ~ 15 mV. One of the reasons for cascading the front end is to allow the use of low voltage, high gain transistors for the front end LTP's, which helps to keep bias current induced offset voltage low due to the high LTP tail current of 10 mA and reduce power dissipation in the LTPs. Q9, Q10, Q13, and Q14 are high gain BC547C/557C devices (hFE spread 450 to 800) that are selected for a 10% hFE match. D2 and D6 (8.2 V 250 mW Zeners) provide the base reference voltage for the cascode transistors (Q31-Q34), and also provide the offset set adjustment reference for R80, with C27 simply ensuring that no Zener noise is injected into the inverting input. C29 and C30 provide additional decoupling of the Zeners.

The VAS stage consists of Q8 and Q29 for the negative signal side, Q16, and Q30 for the positive signal side. Q8 and Q16 are beta enhancement transistors that raise the local VAS loop gain and buffer the front end diff amp output current developed across R71 and R72. The VAS output transistors (Q29 and Q30) are the most critical active devices in the e-Amp, and generally in any high power voltage feedback audio amplifier. C10, C11 and C20 and C21 are the primary loop compensation capacitors and are the most critical passive components in a voltage feedback amplifier.

J7 and J8, when linked with jumpers, configure the e-Amp for TMC compensation. When removed, the amplifier uses conventional Cdom Miller compensation. R30 and R31 (33 k) are connected across the VAS, and when J6 (LG) is jumpered, lightly load the VAS stage to lower, flatten and extend the amplifier

loop gain. Through the use of these jumpers, the Ovation e-Amp can be set up for any of four compensation schemes. The e-Amp compensation design is covered in detail in Section 8.

D10 and D11 are very fast switching, low reverse capacitance BAV21 diodes configured as Baker clamps to prevent rail sticking when the e-Amp is driven into clipping – this will be discussed in some more detail in the ‘Design’ discussion later in this document under Section 7.6

Interposed between the two VAS output devices is the Vbe amplifier consisting of Q7 and Q12. Q7 is the temperature sensor and is tightly thermally coupled to the output devices, and Q12 is the shunt transistor that conducts most of the VAS standing current. R7 (1 k 22 turn potentiometer) provides output quiescent current adjustment. R75 (10 k NTC), R76 and R77 provide additional temperature compensation at the higher end of the heat sink operating temperature range. The VAS is decoupled by C12 and keeps the shunt impedance low at high frequencies while C13 provides compensation for the Vbe multiplier, ensuring it remains stable. Note that both the pre-drivers and the drivers are mounted on the same heatsink as the output devices. See Section 7.9 for more details.

The VAS output is taken off from either side of the Vbe multiplier and fed into the pre-driver transistors Q25 and Q28. I’ve used the same devices here as in the VAS simply for convenience – low Cob is not really needed for this function, but the devices are relatively inexpensive and the pre-driver power requirements are modest. The pre-drivers (along with the driver stage) run in class A for all output loads, with a nominal standing current of 16 mA and dissipate around 1.1 W each. It is important that the pre-driver and driver stages remain in class A under worst case drive conditions – this is assured by the high gain in the driver and output stages. R66 + C15, R3, R33 and C9, along with R73 form a stopper network for Q25 and Q24, designed to prevent parasitic oscillation – something EF triples are prone to if precautions are not taken. The mirror components on the negative side of the amplifier form the same function for Q27 and Q28. The driver stage (Q24 and Q27) also runs in class A with a standing current of 33 mA for a device dissipation of 2.3 W per device on 70 V rails set by the value of R23 and R24.

The e-Amp uses ‘sustained beta’ NJW3281 (Q20-Q23 and Q6) and NJW1302 (Q13 ~ Q16 plus Q5) devices, each fed from the driver stage output via 1% 4.7 Ω base stopper resistors – again, to ensure there is no HF parasitic oscillation. These transistors have very good Safe Operating Area (SOA) specifications, and importantly, their gain is quite flat across a wide collector current range. This translates into less loading of the driver and pre-driver stages, and as a result, lowers distortion. The output devices are coupled to the output rail (this is the point where the 8 x 0.33 Ω output device emitter resistors all join together) by means of 0.33 W low inductance 4 W wire wound resistors. These resistors provide local feedback and aid in linearizing the output transfer function. Secondly, they also aid in stabilizing the quiescent current in conjunction with the Vbe multiplier discussed earlier.

D1 and D2 are flyback diodes connected between the output rail and the supply rails and are designed to route inductive dump currents around the output devices.

The output rail is connected to the output terminal via L1 (1  $\mu$ H) and R8 and is designed to isolate the amplifier from capacitive loads which can cause instability (covered in more depth in the ‘Discussion’ section). A Zobel network (R9 and C19) is connected between the output rail back to the system ground via a dedicated terminal called ‘ZR’. Feedback is from the output rail to the inverting input (Q9 and Q14) via R11, R12 and R82 (15 k  $\Omega$ ) with R67 (100  $\Omega$ ) forming the lower part of the feedback divider network. Thermal distortion due to  $I^2R$  heating in the feedback resistors is a concern because under full power output conditions, they will dissipate 1 W. For this reason, the feedback resistors consist of three parallel 0.5 W devices that feature very low voltage coefficients and low thermal drift.

C7 and C23 provide DC blocking (so the e-Amp’s DC gain is unity). A large value 1000  $\mu$ F capacitor keeps low frequency distortion mechanisms to a minimum. C23 is a .1  $\mu$ F poly device that has very good high frequency characteristics, and ensures that the ESL and ESR effects from C7 is bypassed at higher frequencies.

If the ground return for the decoupling capacitors finds its way back to the star ground through the ground connection on J4, noise and hum are likely. R49 (3.3  $\Omega$ ) prevents this by isolating the front end ground from the rest of the amplifier ground.

The e-Amp uses simple current limiting protection. U4 is an AC opto isolator that just measures the voltage across R52 and R53, turning on when the current exceeds about 40 A. The opto output feeds into a separate protection board which will disengage the output load when triggered. The e-Amp uses a mosfet based SSR to handle speaker muting and DC protection and the protection circuit response time to a gross overload is under 50  $\mu$ s. F1 and F2, 10 A fuses provide last-ditch protection in the event of a catastrophic system fault. U6, an LM60 temperature sensor, is mounted in close proximity to Q18, and senses the general heatsink and output device temperature. This feeds into the control board, where the trip temperature is set to 70 °C. D5 and D6 provide reverse bias protection in the event that either of the supply rail fuses opens, clamping the associated rail to 0.6 V.

J10 allows the feedback loop to be routed from the pre-driver so that during initial assembly (or repair), the front end can be tested independently before the power devices are fitted.

Finally, Q1, R1, R42 and C1 and Q2 along with R4, R43 and C2 form ‘ripple eater’ circuits and filter the main power supply rails before feeding the front end circuit.

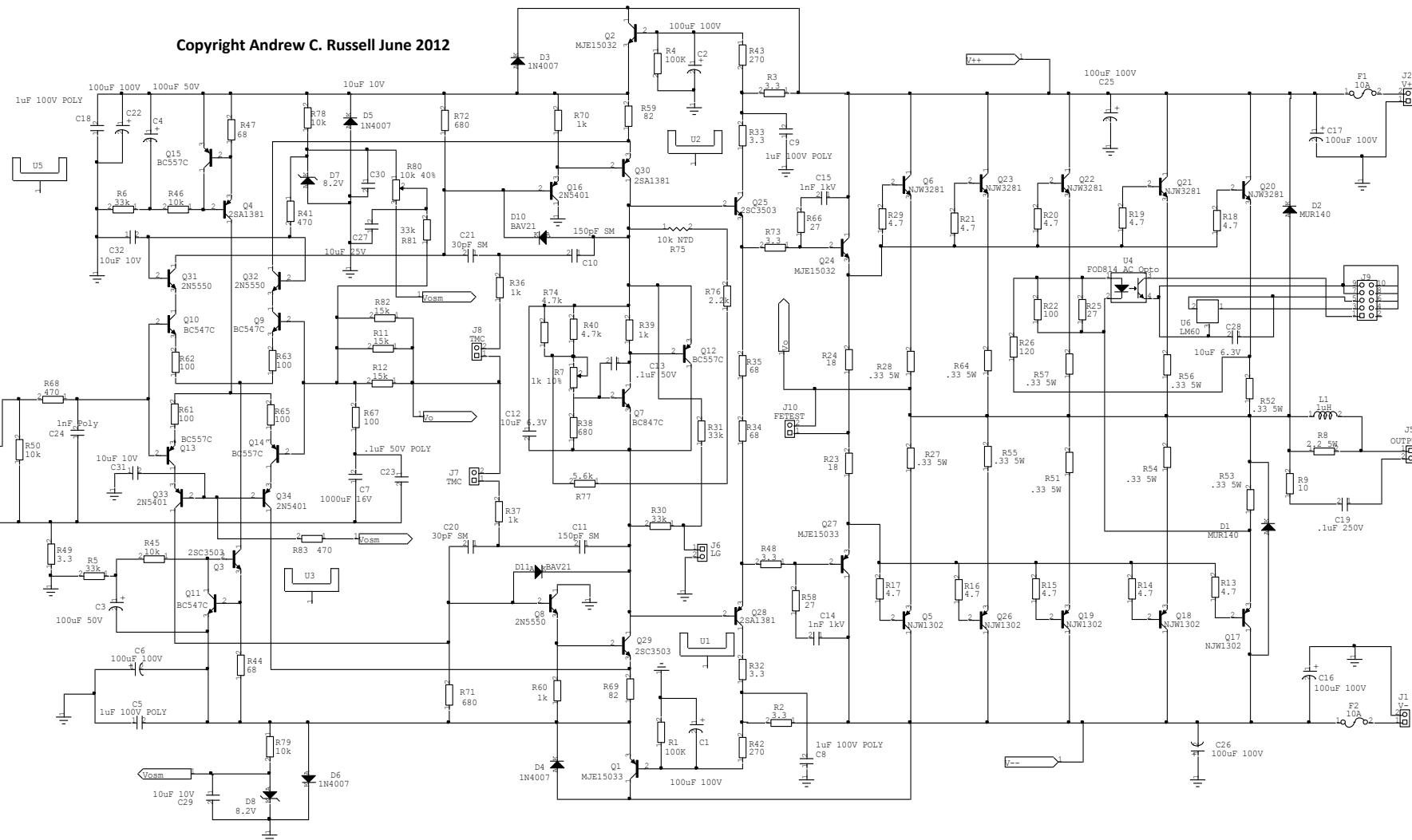


Figure 1 - e-Amp Circuit Diagram

## 4. Component Selection

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For high voltage small signal devices, I used ON Semi 150 V 2N5550 and 2N5401 devices, and for the low voltage high gain devices, BC547C and BC557C types. Q29 and Q30, the VAS transistors are critical and must have low Cob and high Early voltage. The 2SA1381 and 2SC3503 are ideal devices for this function.

For leaded electrolytic capacitors, I generally like to use Panasonic from Digikey because they are well specified and the quality is very good. There are a few 10  $\mu\text{F}$  25 V MLCC<sup>1</sup> SMD ceramic devices used for low voltage DC rail decoupling on the board, again, I usually stick with Panasonic as well. For the high voltage 1  $\mu\text{F}$  stacked foil devices (always great for HF decoupling), I use BIC Vero polyester types from Mouser. Cdom capacitors C20 and C21 (and TMC comp caps C10 and C11) are critical components with few really good options outside of silver mica. The damping network capacitors C9 and C14 (1 nF Polyester) are critical as well. On the original prototype, I used 1000 V ceramic capacitors. During routine debugging and development work, I was driving the amplifier and these capacitors would ‘sing’ at about 30 V pk to pk voltage swing and above at the test frequency. Simply clamping the devices between thumb and forefinger silenced them. Moving to the poly caps completely solved the problem. Bottom line: don’t use general purpose ceramics in anything but DC decoupling in audio<sup>2</sup>.

For resistors, I have mostly used Vishay CFP metal film devices from Mouser (the leaded resistor selection at Digikey is really lacking for some reason). Critical devices are the feedback network, LTP degeneration resistors, LTP load resistors and input bias and filter network. These need to be good quality, low noise, low TCR and low voltage coefficient components. Assuming the use of good quality metal film resistors in the first place, I am not going to comment on the ‘sonics’ of resistors; I read a lot of commentary about this subject - some of it no doubt valid, much of it not.

For the heatsink, at least 0.3 K/W is required for reliable long-term operation, with 0.25 K/W even better. Good options here that I looked at were a [Fischer Elektronik](#) case with integrated heatsinks and a 5U Modushop case. The [Modushop](#) products from Italy are not quite as well finished as the Fischer products, but they are not as expensive. The Fischer cases do not have a 10 mm front panel thickness option which Modushop do - a 10 mm front plate looks cool, a 3 mm front plate does not. Fischer cases are difficult to purchase (they use local reps) which is not the case with Modushop who run an efficient web shop, accept PayPal (and recently announced debit card transactions) and will ship anywhere in the world. Andrea Bettazoni at Modushop also offers drilling and tapping services but it is not inexpensive and English is not his first language.

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<sup>1</sup> ...but special care is needed in selection: [whats-the-capacitance-of-your-mlcc](#)

<sup>2</sup> I used 1 kV 1 nF Panasonic ceramic caps in the Ovation 250 driver snubbers and did not suffer from this problem. The problem devices on the e-Amp proto were 1 kV 1 nF 10% types Vishay PT# B102K25X7RN63J5R. With respect to audio, X7R and especially Y5R are *very problematic* dielectrics with capacitance strongly dependent upon voltage and they are known to have piezo effects as demonstrated in this case. KEMET 630 V Polypropylene film capacitors (PT# PFR5102J630J11L4) were used in the final design and they have none of these problems.

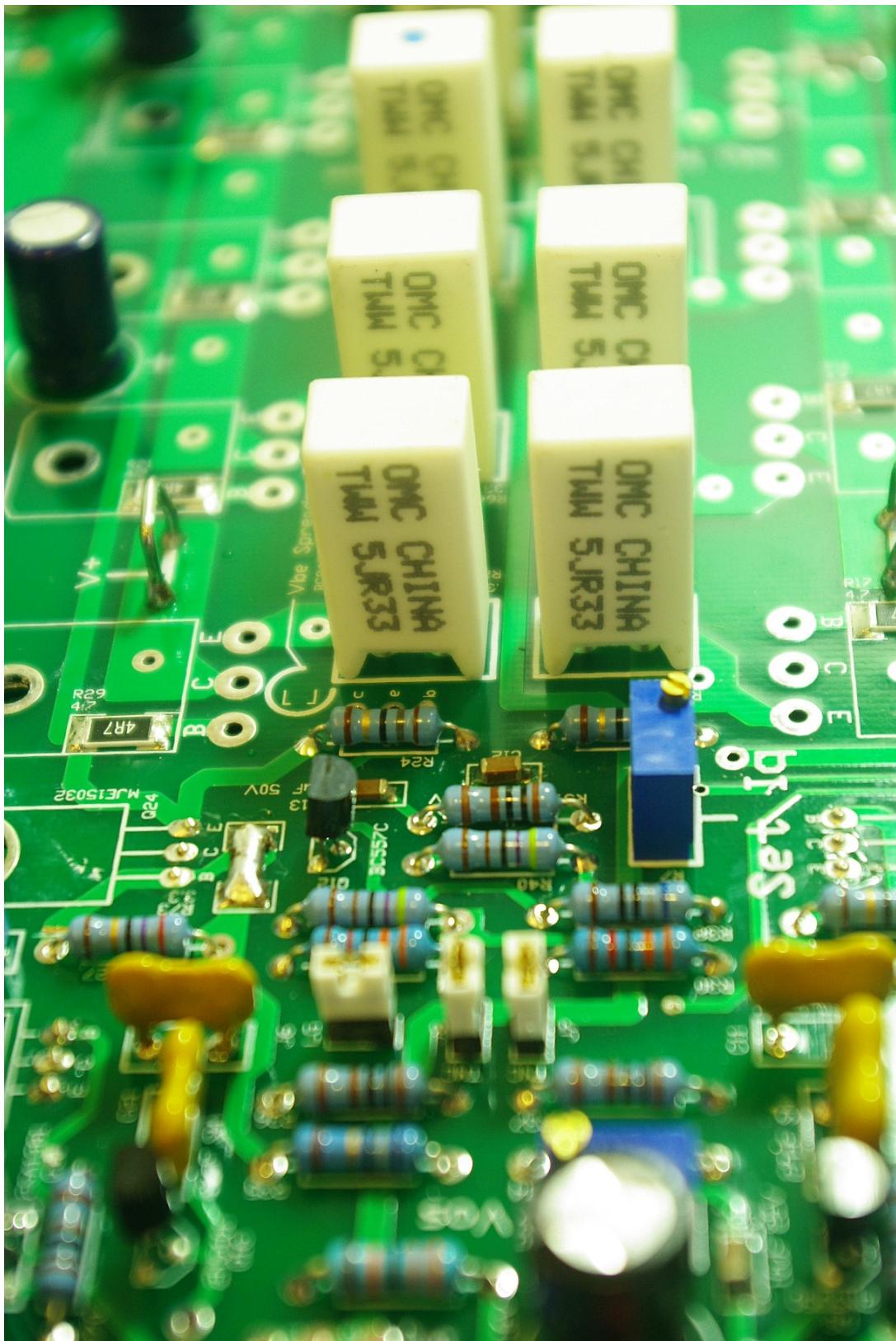


Photo 1 - Small Signal Section

## 5. Power Supply

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For a big amplifier like this, there are a few options for the power supply. A monobloc construction would require two completely separate supplies. This option is usually applied on the notion that channel separation and dynamic power performance is improved. The other would be to have a single transformer feeding a common capacitor bank which would then feed both amplifier channels and this is the most common and cost effective power supply configuration. In the Ovation e-Amp, I used a common transformer that feeds to separate rectifiers and capacitor banks. This configuration provides very good channel separation and avoids the use of a second, heavy, and expensive power transformer.

For the main filter capacitors, I used 10 x 8.2 mF (8200 micro Farads) 80 V devices, giving 41 mF per rail per amplifier channel – more than adequate for the job - and one 35 A bridge rectifier per channel. Diodes generate RFI burst noise as they come out of conduction and this can couple into the sensitive circuit nodes (conducted and EM coupling) on the amplifier and affect the performance. To overcome this, each diode in the two bridge rectifiers is decoupled using a snubber<sup>3</sup> and the bridges and associated wiring are shielded.

The capacitor filter banks are implemented on 70 µm thick DSTHP PCBs (as are the amplifier module PCBs). The charging, amplifier supply feeds, and ground returns are separated in this PCB design to minimize common impedance coupling noise through both the wiring and PCB traces, and the capacitor ESR/ESL as shown in Fig 2. Further, the order in which the amplifier ground return signals are made is also very important. The e-Amp does not use a star ground design, but a 'T' grounding scheme. The Zobel is placed closest to the capacitor bank charge return star ground (A in Figure 2) followed by the speaker return, the decoupling ground and finally the signal ground which goes all the way to the amplifier input stage, and is separated from the decoupling ground by a 3.3 Ω resistor on the amplifier PCB. All of these signal related grounds are tee'd off by about 20 cm from the charging ground return. If the order of these connections is swapped – say the Speaker Return is swapped with the Decouple GND, this places a noise voltage source (speaker current x the trace impedance) in series with Decouple GND, which then couples up through the amplifier decoupling capacitors onto the supply rails. Trace and cabling inductances exacerbate the effect at HF and on fast rise time signals.

There are two Decouple GND connections per channel. This is needed because the ground return of decoupling capacitors on the amplifier boards are also routed separately back to the supply and not joined on the amplifier PCB board. Firstly, in class AB amplifiers, the output signal current is reflected on the supply rails as half wave rectified pulses at the signal frequency plus associated harmonics. When one half of the output stage is conducting, and the supply rails are tightly coupled (e.g. through twisting the wires together) it can couple wide band hash into the amplifier front end through the non-conducting power supply rail. For this reason, in class AB amplifiers, the + and - supply rails and their associated ground return should be separated and then routed back to the power supply common

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<sup>3</sup> See <http://www.hagtech.com/pdf/snubber> for an excellent discussion on snubbers.

connection point. These layout guidelines are probably easier to do on a single PCB and I did toy with the idea of mounting filter capacitor bank on the amplifier PCBs. However, I decided due to space constraints and to ease design and development to keep them separate.

For this amplifier, I ended up using a 1 kVA Triad toroidal transformer from Mouser that cost \$140 excl. shipping. The [Ovation 250 Watt](#) per channel amp power transformer (2 kVA, 18 kg) was wound by Airlink Transformers in the UK specifically for audio and cost me about \$450 in 2006. That was a big investment, but it is exceedingly quiet – in fact I'd say completely inaudible with no buzzing or humming of any description. When building a high quality amplifier, the transformer and power supply quality cannot be over-emphasized. However, I am pleased to say that the Triad transformer is also very good, with no buzzing or humming, and it runs cool as well.

Avel-Lindberg, Plitron and Amveco in the USA would also have been good choices. Plitron, specifically, have a range of torroids designed for high-end audio and they claim low inrush currents and substantially lower noise. These transformers run at about \$350 Canadian for a 750 VA component whereas the standard transformer costs about \$140 Canadian. Tellingly, the standard Plitron 750 VA weighs in at about 5 kg, whilst the audio specified one comes in at 15 kg for the same power rating. On the face of it, the Plitron high end transformers look like excellent value for money.

The completed power supply assembly (transformer, capacitor filter banks and brace onto which all the components are mounted weights 13 kgs. For reference, the power supply on the Ovation 250 weighs about 24 kg (18 kg transformer and 6 kg brace and capacitor filter bank).

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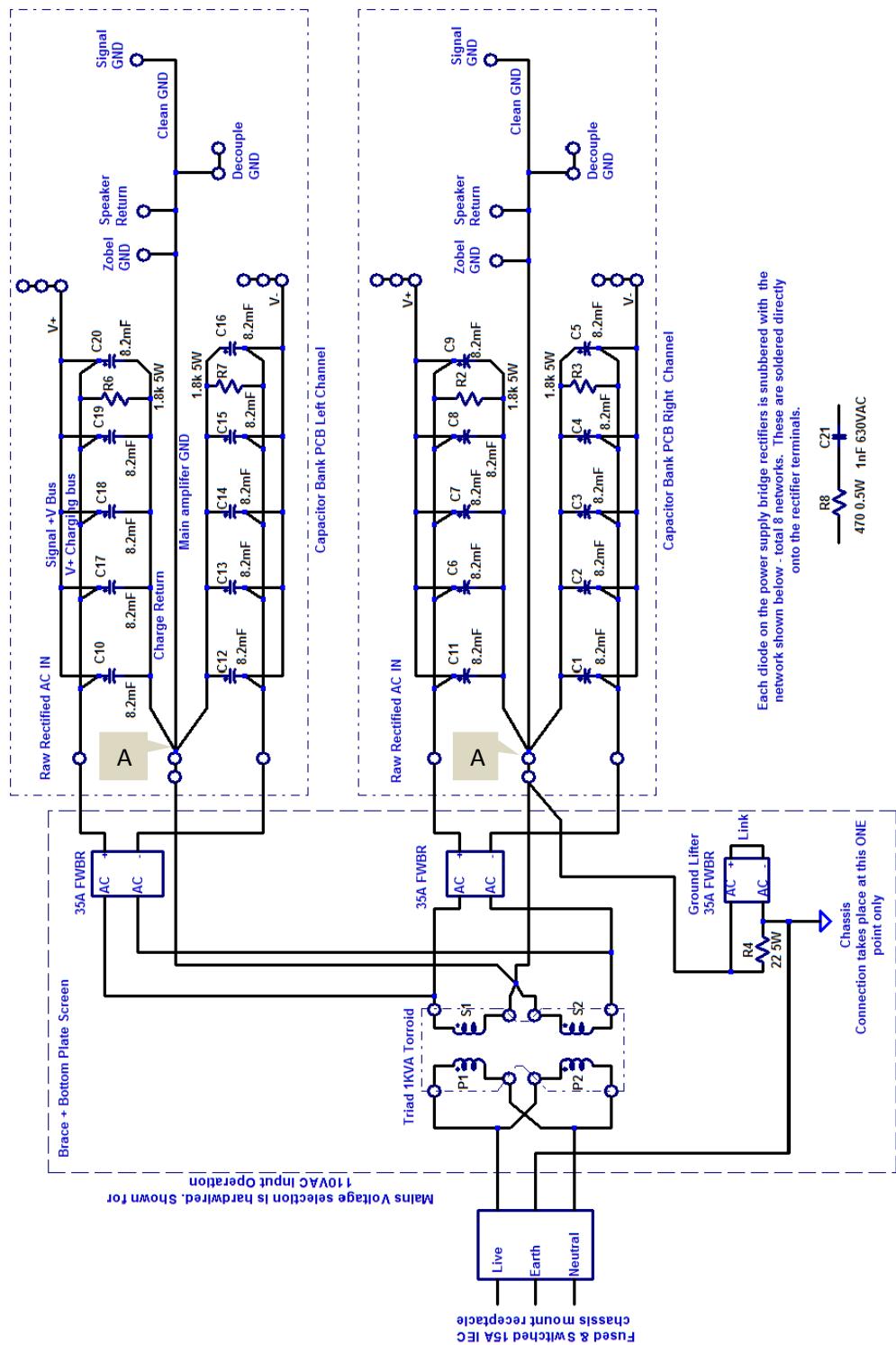


Figure 2 - PSU Board Circuit Diagram. The layout of the PCB and the order in which the ground returns from the amplifier modules are connected is important in order to achieve low noise and hum.

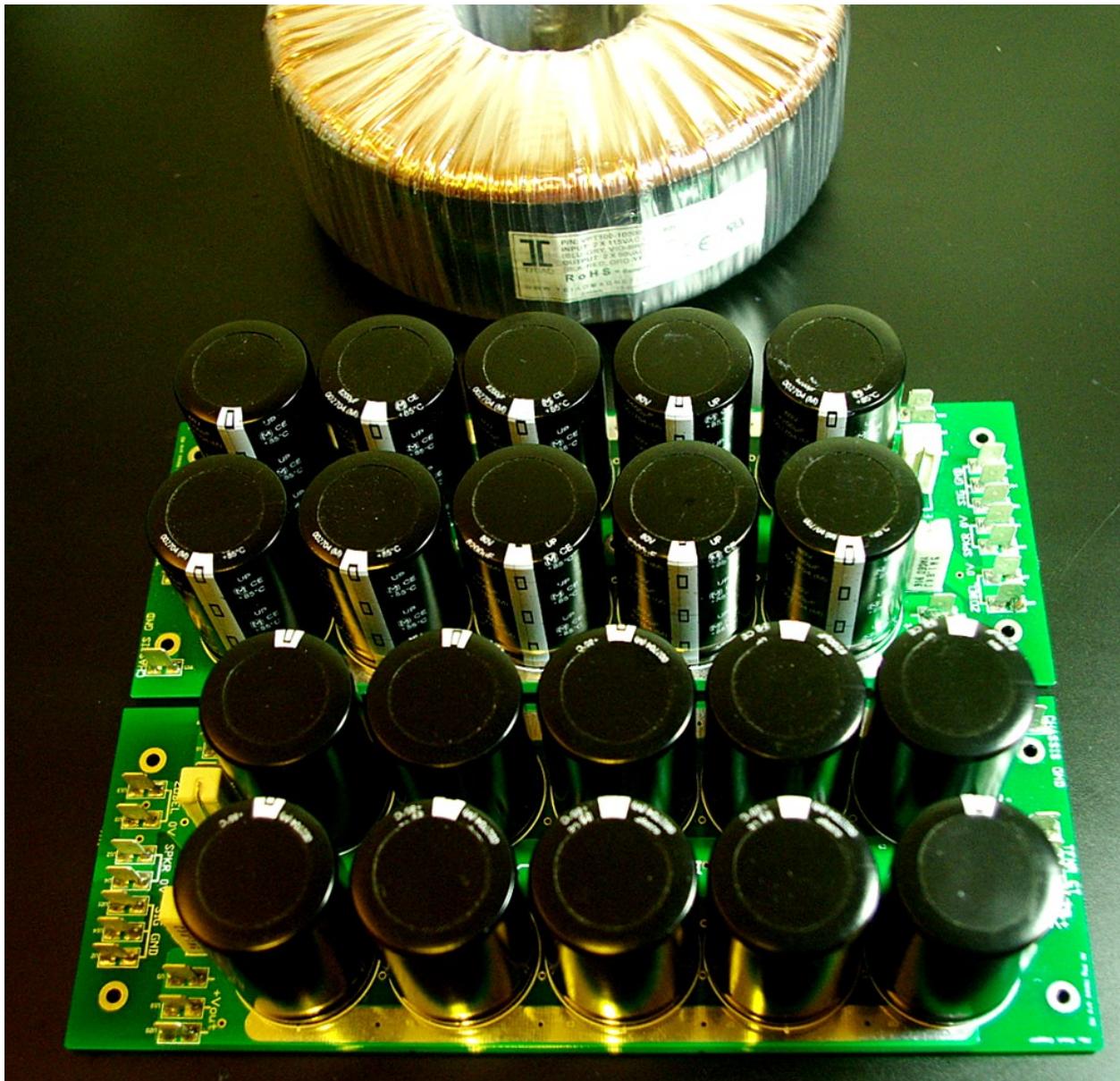


Photo 2 - e-Amp PSU Components

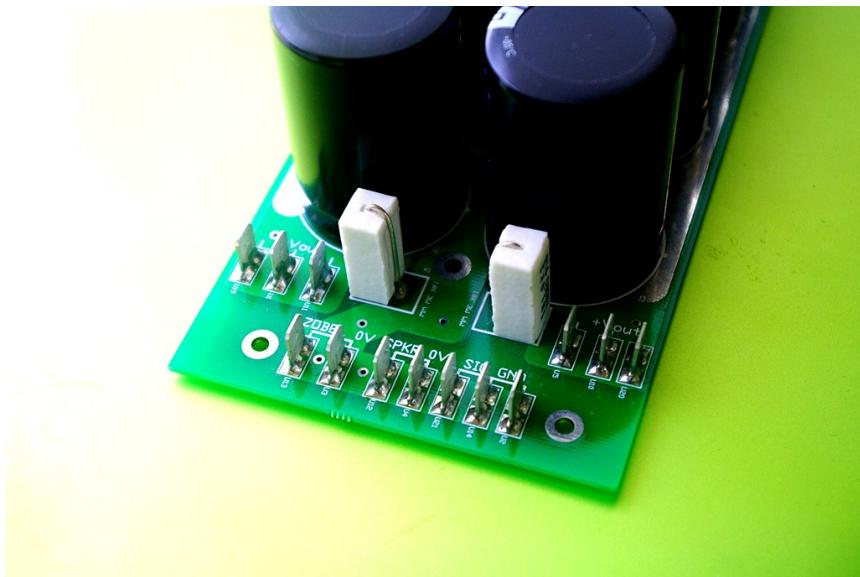


Photo 3 – Connections to the Amplifier Module are ordered for Minimum Noise

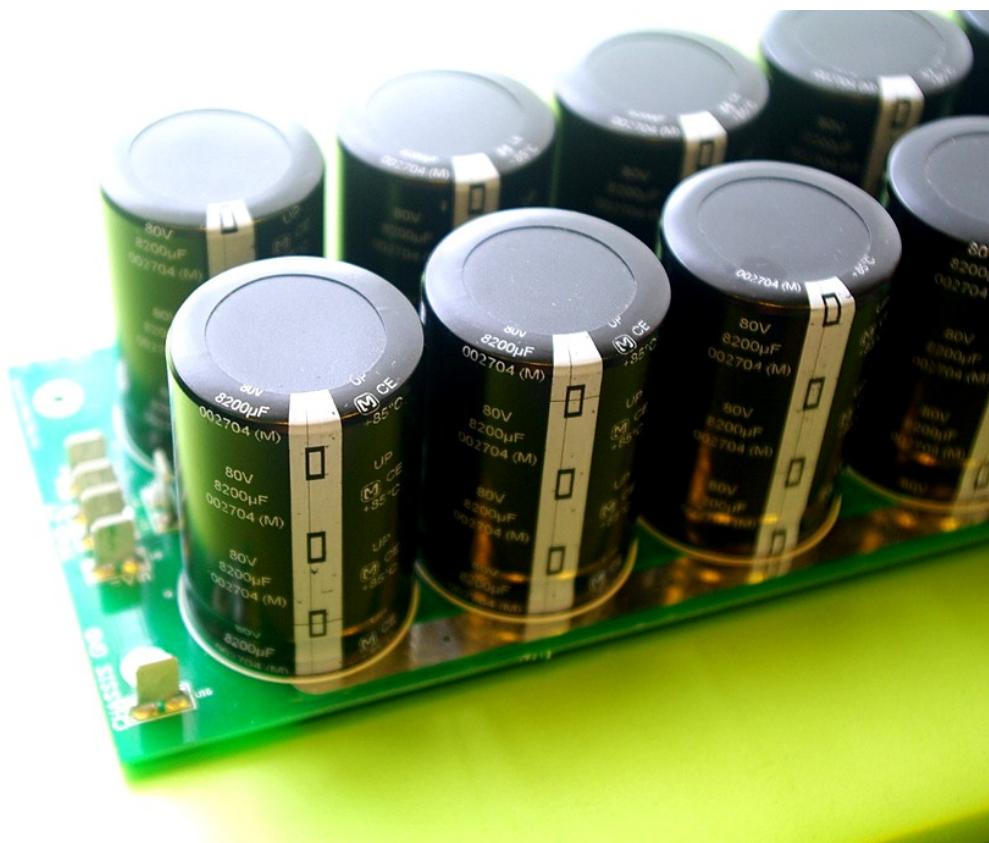


Photo 4 - e-Amp PSU Board

## 6. Construction

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Fig 3 details the wiring. I typically use 10 to 12 AWG (that's about 2 mm to 2.6 mm copper cross section diameter) multi-strand cable for the heavy current cabling. For the signal wiring from the RCA sockets to the PCB, I used a screened cable and made sure it had a proper screen. A lot of the cheap stuff simply bundles some multi-strand alongside the inner core – the screen has to surround the inner core to work properly and it should ideally be of the woven type.

The input signal RCA connectors have to be thoroughly isolated from the chassis - if not, the amplifier will hum. Input sockets and wiring have to be kept well away from the AC mains inputs and from the amplifier power supply wiring. The Ovation e-Amp PCB layout facilitates this, but it is of course always easy in the thick of a construction project to overlook these matters.

Rod Elliot has an excellent general discussion on [grounding/earthing](#) and [PSU wiring](#). On a project like this, involving mains voltages and all metal chassis, construction and safety are paramount. For the mains input, Rod Elliot recommends an IEC mains socket with integrated power switch and fuse holder, which is what I used as well. I needed to do some major drilling and filing, but it was the safest and most attractive looking solution. Chassis earthing is critical for safety. In the power supply circuit, I have shown a ground lifter circuit (D2 and R5) which allows the amplifier 0 V to be earthed (i.e. connected to the chassis) without causing any earth loop hum. This leaves the amplifiers floating within  $\pm 1.4$  V of earth potential, which is enough in almost all cases to eliminate ground loops. Under fault conditions, the diodes simply clamp the fault current to earth, ensuring safety. Note the important link between + and – as shown in Fig 2 on D2 (red box on the diagram). I used a 35 A bridge (which can handle repetitive surge currents of >200 A) for this function for safety reasons, and on similar projects would not recommend anything less.

The PC utilizes a ‘sandwich’ construction technique whereby the output devices are placed between the PCB and the heatsink. Although this means the PCB is larger than designs that do not use this approach, it makes for a robust, neat looking final board. As an added bonus, the PCB acts as the washer and torque spreader, reducing any chances of cracking the power devices due to over tightening.

The Modushop ‘Dissipante’ 5U housing base cover plate and internal mounting plate are not built to handle the heavy transformer and capacitor bank and flex by 3 ~ 4 mm under the weight. This problem is easily solved however. I had a 2 mm thick ‘U’ shaped brace fabricated with a 10 mm flange on each side. When this is bolted onto the base plate assembly, it provides a significant amount of reinforcing and with 12 kg of transformer and capacitor bank, the base plate shows no flexing. I used a similar approach on my earlier Ovation 250 design (but there I use 3 mm thick material because the transformer is considerably heavier) and can vouch for its effectiveness; further the brace provides very effective screening of transformer magnetic fields and is a convenient place upon which to mount the capacitor banks, as shown in Photo 5 below.



Photo 5 – Brace Assembly

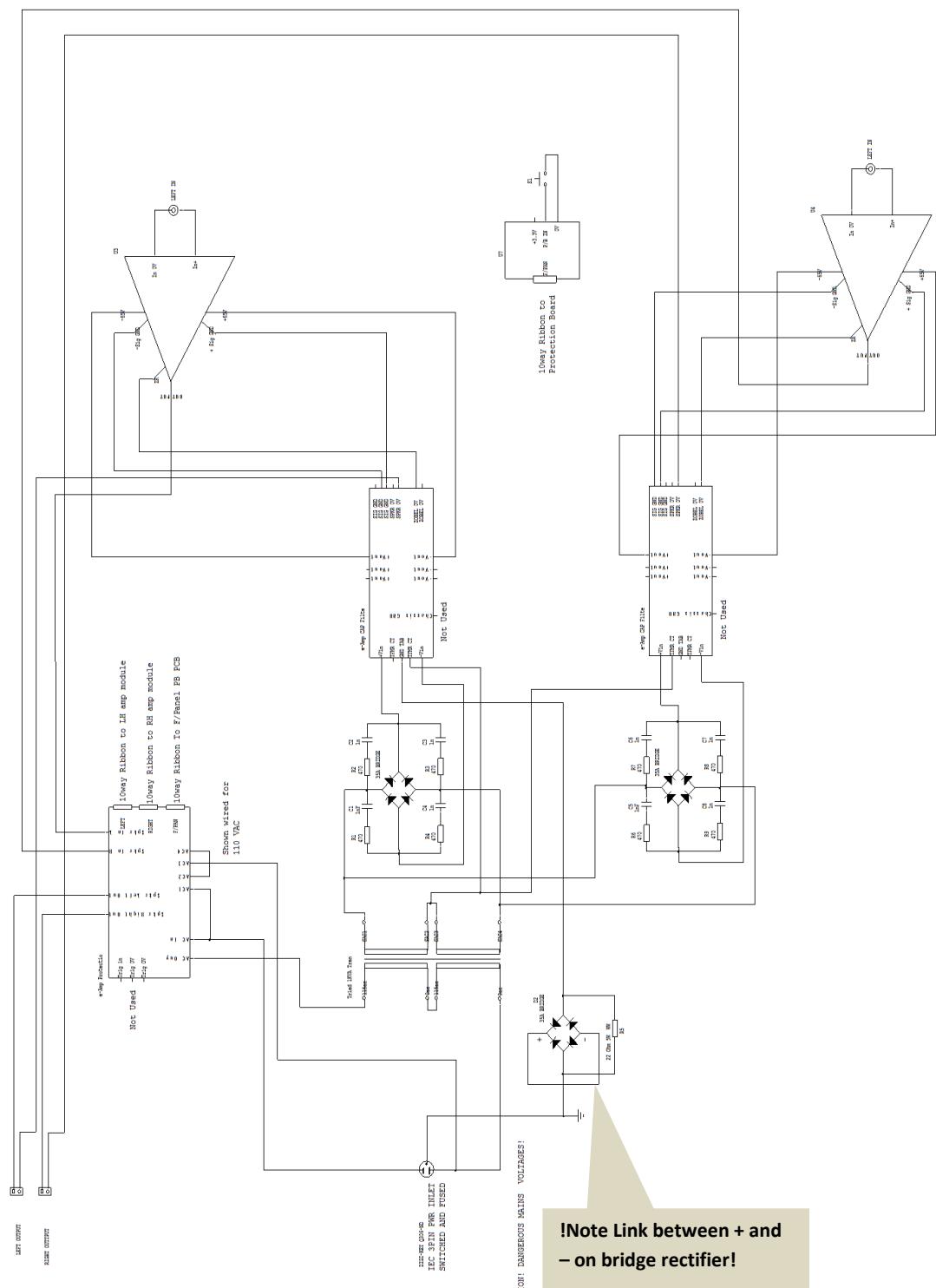


Figure 3 - e-Amp Wiring Plan

## 7. Design Discussion

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Although the relationships between key circuit performance parameters are well understood<sup>4</sup>, there is no universal approach or methodology to designing audio amplifiers. You either get taught in engineering school how do it in very general terms, you stick with it and adapt it over time, or you work out your own methodology. Of course, there are now some very good books on the specific subject as well. I use [LTSpice](#) very extensively in the design process, since even though you can calculate the required component values to quickly arrive at the initial 1<sup>st</sup> round nominal values, there is a lot of fine tuning required to get a really good, high performance design, and that's even before we start to think about the critical PCB layout and wiring issues. To be sure, what is seen in the circuit model on a computer does not always reflect what is measured or observed on the prototype in the detail, but its close enough to help understand what's going on in the prototype, and to make sensible tweaks. A major reason for the discrepancy is to do with the accuracy of the models in the simulator to prototype direction, but there are also problems going from the prototype to the model because the prototype real world components with parametric spreads and parasitics (e.g. capacitors, trace inductances and so on) result in behavior you don't see at first on your computer, and a typical example is the behavior of EF triples and cascodes (you can read about my cascode experience [here](#)) in the presence of PCB trace inductance. Further, there are a few cases where modeling and simulation are problematic, a good example being the FBS topology with mirror loaded LTP (to be discussed a bit further on), which simulates perfectly, but is not DC stable in the real world, rendering it useless in a practical amplifier without some form of VAS DC common mode current control circuit.

### 7.1 e-Amp Topology: 'Fully Balanced Symmetrical' (FBS)<sup>5</sup>

The choice facing the designer of any power voltage feedback amplifier is to go with either a Lin (so called because it was HC Lin of Bell Labs who first proposed the topology in the 1950's) or FBS topology or some derivative (and there are many) of either. Like the feedback debate, there are those that swear by the Lin topology (popularized by Douglas Self who used it as the demonstrator of his now famous 'blameless' amplifier concept) and others that say the FBS can do no wrong. The criticisms from some quarters leveled at the Lin topology stem from the fact that the VAS is not symmetrical and therefore the drive to the output stage is not symmetrical since you have a buffered common emitter stage usually loaded with a current source. The common emitter VAS amplifier can provide substantial currents into the output stage, but the current source limits the drive on the other half of the waveform. As a result, the slew rate (SR) is also not symmetrical, and when Self's efforts to mitigate this problem are studied, one quickly concludes it is a hopeless cause. Balanced designs suffer none of these drawbacks, offer an additional 6 dB of loop gain, and neatly cancel 2<sup>nd</sup> harmonic distortion, although some practitioners don't like this, citing the resultant missing, or lower level, even order harmonic distortion spectra as a negative influence on amplifier sound. There are well known

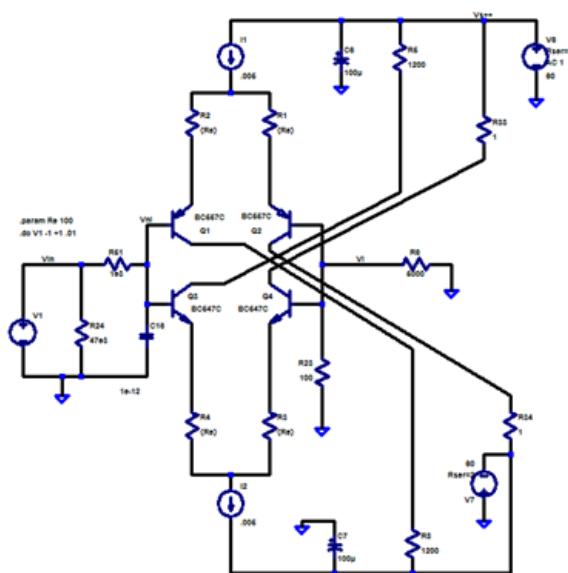
<sup>4</sup> See Marshal Leach: [Amplifier Tutorial](#) which covers the fundamentals of voltage amplifier design.

<sup>5</sup> FBS – Fully Balanced input stage feeding a Symmetrical VAS stage

techniques to convert a standard single ended LTP to a balanced drive VAS in which the drive and slew rates are symmetrical. The earliest single ended LTP input to balanced drive VAS I have been able to identify was in Bart Locanthi's<sup>6</sup> design from 1966 while he was at JBL. Subsequently this was used to good effect by a number of manufacturers, and popularized by Hitachi Semiconductor in their mosfet applications data handbook from the very early 1980s, but I don't know if they got it from Locanthi, or if it was developed independently. Robert Cordell<sup>7</sup> used a standard single ended LTP to balanced VAS stage topology in his amplifier with mosfet output and error correction, also from the early 1980s. In the FBS topology, originally developed by John Curl, and his subsequent derivative utilizing a folded cascode, SR's and drive to the output stage is symmetrical and VAS output current drive capability is substantial. However, the FBS small signal stages are generally more complex, and compared to the Lin topology, there is a \$ cost penalty (albeit small) and the PCB layout also takes a bit more effort. The Lin topology is simpler, lower cost and still achieves remarkably good results as evidenced by Self's work. In terms of output stage drive capability, if one uses an EF3 or CFP output stage, the drive issues with the Lin can be reduced substantially, though you cannot readily overcome the differences in positive and negative SR's. Given some of the shortcomings of the Lin, and I have to say my positive experience with the FBS topology in the Ovation 250 amplifier, the FBS was also selected for the e-Amp. The penalty is slightly higher cost and complexity for the small signal components (maybe around \$4 on a one off like this), but I think for a high performance amplifier this is a small price to pay for symmetrical drive of the output stage and an additional 6 dB of open loop gain. I would add at this point that if designing an amplifier for high volume commercial applications, the Lin topology would be my first choice because of its simplicity and cost effectiveness. But, like the Ovation 250, the Ovation e-Amp has definitely not been designed to a price point.

## 7.2 Front End Design

Figure 4 - Front End Model



A general discussion about input device technology, Re, SR, Input Overload, Tail Current and Input Filter

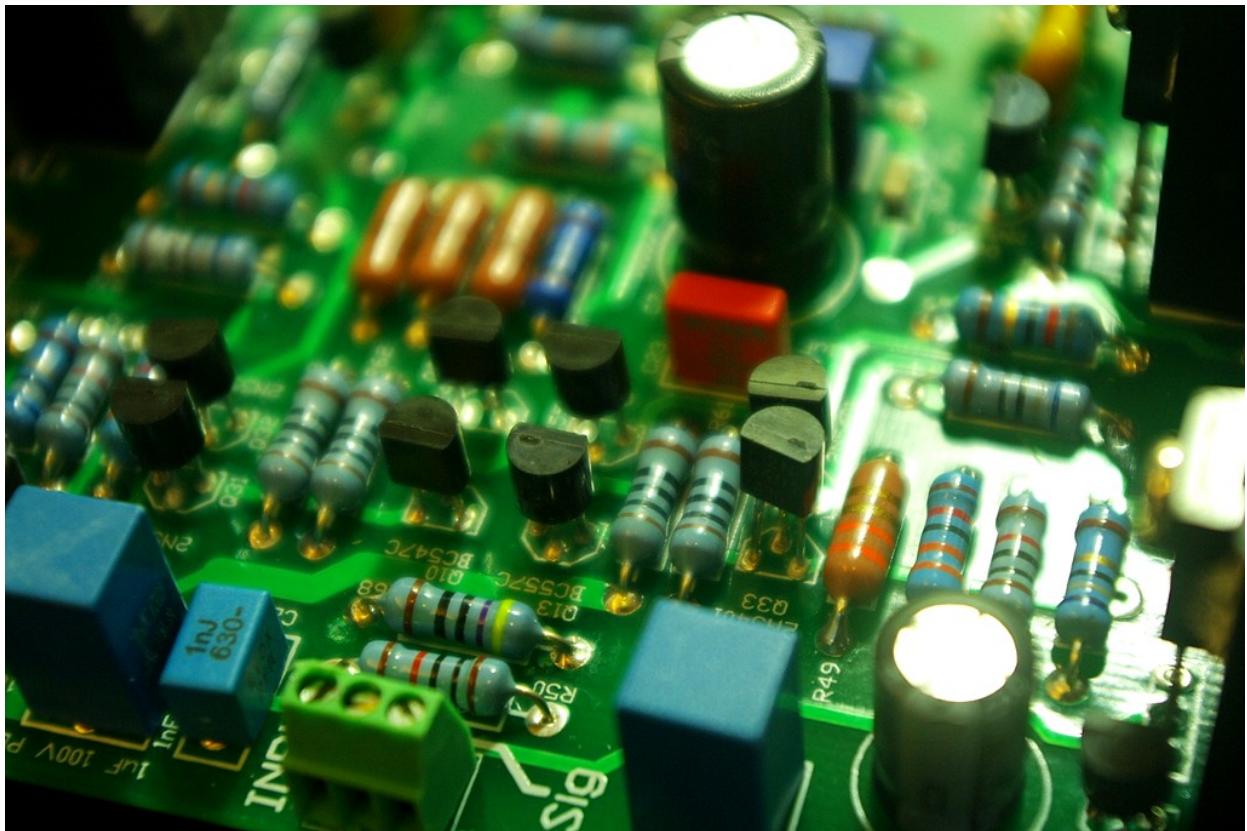
### JFETs or Bipolar?

Solid state amplifier designers have a choice of 2 basic device technologies for the input stage: bipolar or JFET. Some idiosyncratic designs use mosfets, but I will not cover these here. The  $gm$  of JFETs is much lower than un-degenerated bipolar devices, and in VFAs using conventional Cdom compensation, this translates into higher slew rates for a given

<sup>6</sup> Read about Bart Locanthi here: [http://en.wikipedia.org/wiki/Bart\\_N.\\_Locanthi](http://en.wikipedia.org/wiki/Bart_N._Locanthi)

<sup>7</sup> see <http://www.cordellaudio.com/papers/mosfet>

tail current, ergo less chance slewing related



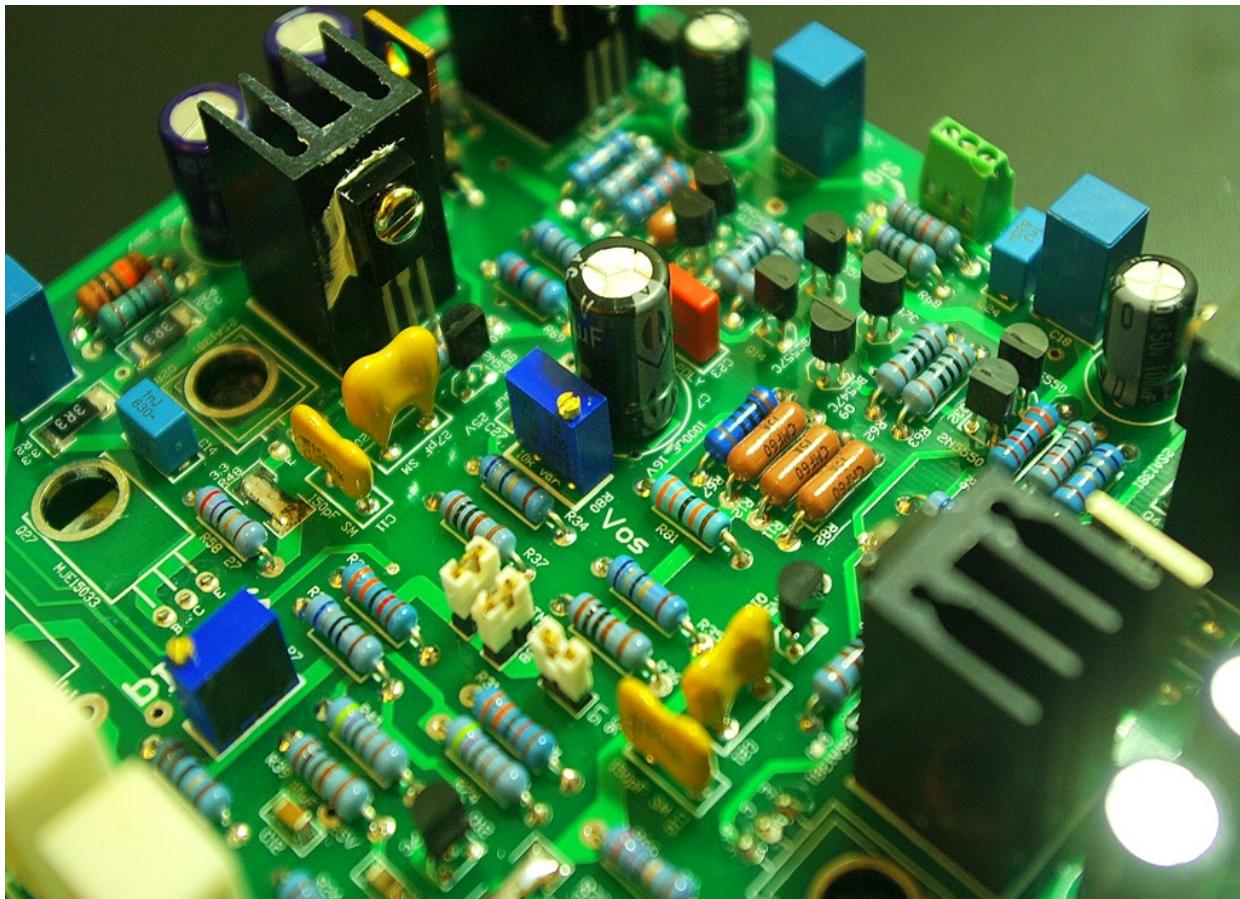
**Photo 6 - e-Amp Small Signal Stages**

distortion mechanisms. JFETs can offer improved RFI immunity over un-degenerated bipolar devices, and some designers claim they are more linear than bipolar devices, but this has been contested. They are unmatched in applications requiring high input resistance (great for condenser mic preamps or photo-diode amplifiers for example) and their very low noise current makes them ideal for things like MM cartridges, or any other high impedance sources. These are all very strong points in favour of the JFET. John Curl, the designer of Parasound amplifiers, carved out a name for himself as the foremost proponent of JFET front ends in audio power amplifiers. Nelson Pass, a class A, ultra simple signal path exponent is also a JFET fan, as is Charles Hansen of Ayre. However, JFETs are not without their problems. Firstly, in FBS topology designs, quite some effort is required to match  $I_{dss}$  and  $V_{gs}$  vs  $I_d$  characteristics to minimize distortion and DC offsets. In both JFET and bipolar designs, balance between the LTP two halves is critical for lowest distortion - however matching JFETs is much more difficult because the device parameters are somewhat 'looser' than bipolar devices. Discrete designs using this approach will require a servo to correct for both initial offset and temperature drift<sup>8</sup>. Input capacitance in JFETs is high and very non-linear with respect to the gate drain voltage, causing distortion. One way of getting around this is to cascode the diff amp devices so that  $V_{ds}$  is fixed. In bipolar designs the front end LTP stages are often cascaded (as is the case with this design) so that small signal, high hFE devices can be used, since

<sup>8</sup> Even using an electrolytic feedback network coupling cap, FBS discrete JFET front end amplifiers are likely to have many 10s or even 100s of mV of DC offset on the output. Offset over operating temperature can approach many mVs. Thus the servo in JFET front end power amplifiers is a necessity – the desire to avoid the electrolytic coupling cap in the feedback network is of secondary importance and a happy coincidence.

high voltage high hFE transistors are not readily available. Cascoding bipolar devices also aids in PSRR and improves linearity by mitigating Cob effects. In JFETs, the lower  $gm$  also translates into lower overall open loop gain, if this is an important design goal (some designers prefer lower loop gain), the lower inherent  $gm$  is not a problem, but a virtue.

Modern bipolar power amplifier designs are almost *never* configured without input stage degeneration – this in order to improve slew rates and avoid the now extremely well understood TIM mechanism. This also immediately mitigates RFI ingress (an objection often raised by designers who prefer JFETs) but the penalty is additional noise contribution from the degeneration resistors – however the levels are low enough so that they are of no concern in a power amplifier. Of course,  $gm$  is also lowered, but the designer has a bit more flexibility as to how much. The input capacitance in bipolar devices is lower, and when the degeneration is factored in, linearity easily matches or exceeds JFETs. Input bias currents are of course higher, and if the tail current is high (which is what I tend to do in my designs to enable high SR's with standard MC), the feedback and bias resistors need to be low to minimize any resultant offset. However, high input capacitances in JFET designs also mean there is a practical upper limit to the feedback resistor values in those designs as well, to say nothing of the noise contribution. Bipolar input stages are much more DC stable than JFET discrete stages – typically on a well designed power amp using high beta devices 10 ~ 15 mV of offset without hFE matching, and temperature drift of under 10  $\mu$ V/C. This allows the feedback network to be capacitively coupled (more on this point later), and a simple pot adjustment for offset voltage suffices. Unlike JFETs, good small signal bipolar devices are ubiquitous, and devices from the same batch are remarkably well matched – Vbe of <2 mV and hFE to within 20% is quite typical. Tighter matching by hand is therefore an absolute cinch, and on BC547C/557C you can easily match devices from the same batch to within 2 ~ 3% at hFE = 500+. The golden age of the JFET is long passed, and some of the best devices ever developed for audio (especially Toshiba) have been EOLED (End Of Life - semiconductor industry parlance for end of production and no longer available). There is quite some niche JFET industry in audio sourcing NOS, faking devices and generating ‘vapor ware’ - i.e. promises of matching N and P channel JFETs on roadmaps that never materialize. No doubt, the very fact that these devices are no longer in production has driven up prices and allowed all sorts of magical audio properties to be attributed to them . . .



**Photo 7 - VAS and Small Signal Stages Showing the Feedback Option Jumpers**

There are as many bipolar front end solid state amplifiers in the Stereophile 'A' grade category as JFET and Tube designs. Clearly, overall execution and technical expertise enables designers to avoid the cons and exploit the pros of their chosen devices to deliver top class results. For all of the reasons outlined above, and like the Ovation 250 design, the Ovation e-Amp also uses an all bipolar front end.

#### Slew Rate, Tail Current, Front End Overload and Input Filter

In order to avoid TIM, Leach describes succinctly the requirements to ensure that the input overload capability is not exceeded. The input stage must remain operating in its linear region with the maximum expected input signal dynamic both in terms of magnitude and rise/fall time. Linked to this, the LTP tail current must be able to charge and discharge Cdom<sup>9</sup> quickly enough to ensure that the peak

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<sup>9</sup> Note that in the e-Amp for standard MC, Cdom is made up of 30pF in series with 150pF which is effectively 25pF



Figure 5 - Input Stage Linearity Range

resistively loaded LTP's (and use of Cdom or TMC compensation), I like to run my front end diff amps stage 'rich' with a tail current of about 10 mA (so 5 mA per side) and  $R_E$  at about  $100 \Omega$  as this meets a nominal 0.5 V maximum input signal capability while still keeping the loop gain reasonably high. Because the LTP is resistively loaded, under worst case slew conditions when either Q10 or Q13 are turned on hard and providing the maximum amount of current into Cdom (C10 and C11), a large portion of the tail current is still shunted away from charging Cdom through R71 and R72. In mirror loaded LTP's, all of the tail current under these circumstances is diverted into charging Cdom, so for the same slew rate, you can get away with half the tail current. The second important reason for running the tail current high, as in the Ovation e-Amp front-end configuration, is in order to achieve high slew rates using standard MC. This translates directly into modest input filter requirements (-3 dB circa 350 kHz) which would otherwise have to be set at a much lower cutoff frequency to ensure there would be no transient overload on the input stage. Due to the compensation design on the e-Amp (to be covered more fully later), a low value for Cdom is used (effectively 25 pF), which results in a slew rate of  $\sim 155 \text{ V}/\mu\text{s}$  (front end filter disabled). This high slew rate is as a direct result of the high tail current and heavy front end degeneration<sup>10</sup>. Fig 5 shows the output of the model where the input voltage is plotted against the LTP collector currents. The linear range is about  $\pm 0.6 \text{ V}$ . For higher values of  $R_{EM}$  and/or tail current<sup>11</sup>, the input linear operating range increases, but this has to be paid for with a reduction in  $gm$ .

differential voltage between the non-inverting and inverting inputs to the amplifier do not exceed the maximum linear operating region of the input stage. If either of these two conditions is not met, TIM can occur. Fig. 4 shows the model I used to check for input stage overload capability. The tail currents,  $I_1$  and  $I_2$  along with the value of  $R_E$  determine the max input voltage input the stage can handle whilst still remaining linear. Because of the

<sup>10</sup> See Cordell 'Designing Audio Power Amplifiers' page 94 ~ 95

<sup>11</sup> The tail current also sets up the bias point of the VAS amplifier stage. Therefore, if  $R_E$  is held constant and the tail current is doubled, the LTP load resistor has to be halved to keep the VAS bias point voltage, resulting in this example in a halving of the input stage gain.

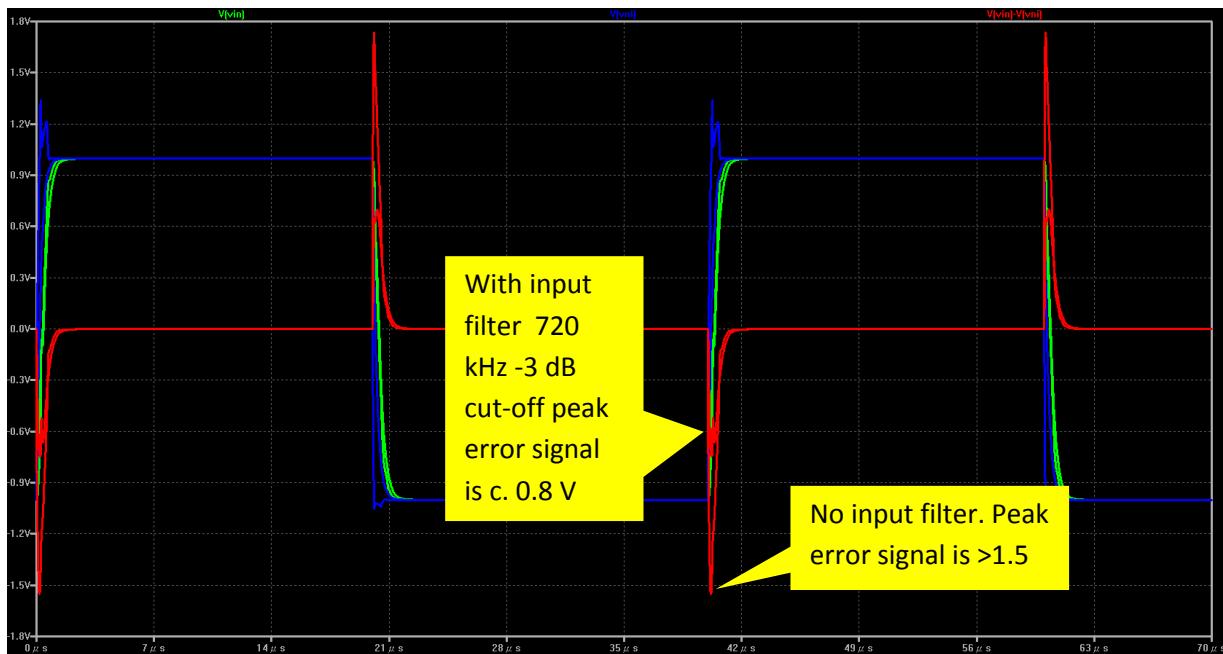


Figure 6 - Input LTP Transient Overload

If this difference voltage exceeds the linear input operating voltage as shown in Fig. 5 (which is just under  $\pm 0.6$  V), the amplifier cannot be guaranteed free of TIM distortion. Fig. 6 plots the error signal as the delta between the non-inverting input and the inverting input. To simulate this error plot, I fed in a square wave of 25 kHz at  $\pm 1$  V pk-pk with a rise time of 100 ns. This is an implausibly fast rise and fall time, but clearly shows the absolute limits of the front end overload capability. If the input stage saturates, there is no feedback – the amplifier is running open loop until the loop recovers. As a result, the output it is likely to end up stuck at one of the supply rails until the loop can gain control again – a very messy situation indeed. However, the cure is simple - either lower the input filter cut off frequency and/or reduce the input stage  $gm$  by increasing  $Re$  until the difference voltage falls below the maximum linear operating range per Fig. 5.

The front end design and value selected for Cdom therefore ensures that the e-Amp will never run into TIM. Fig. 6 shows the result with no input filter (capacitor value set to 0 pF) and the peak error signal (red trace) is  $> 1.5$  V. With the Input filter -3 dB cut-off set to 720 kHz, the peak error signal is the lower red trace at about 0.8 V, while with a 2  $\mu$ s rise/fall time signal (far more realistic), the peak error signal is 0.3 V – well within the overload capability of the front end. Connecting each channel of a wideband dual channel scope to the inverting and non-inverting input and subtracting the two will directly display the difference waveform and something very similar to that which can be seen in Fig 6. Use a fast rise time square wave input signal for this test – 100 ns is about right – with the front-end filter in situ.

In the final design, I lowered the input -3 dB cut off frequency to circa 350 kHz (R68 and C24) as a precaution against RF ingress.

The front end design goals can be summarized as follows:-

1. Ensure that under absolute maximum input drive conditions (i.e., just prior to clipping) the input stage remains linear, as shown in Fig 5 and Fig 6. Use 2  $\mu$ s rise/fall times for this design step. Increase RE and/or the LTP tail current to ensure this condition is met. Do not provide any more headroom on the front end stage than is necessary, since this has to be paid for by a reduction in loop gain and ultimately increased distortion.
2. For conventionally Miller Compensated configurations like the e-Amp, run the LTP current high (so 5 ~ 10 mA) in resistively loaded designs to ensure high slew rates and sufficient current to charge and discharge Cdom whilst at the same time providing the current demanded by the LTP collector load resistors.
3. With regard to the input filter, adjust the cut off frequency on the final prototype by looking at the output into an 8  $\Omega$  load, and making sure there is no overshoot, being careful not to be too aggressive. An input filter -3 dB of between 300 and 500 kHz is about right for design like the e-Amp. For this design step, use a fast rise time of about 100 ns.
4. Cdom, Re, tail current and the input filter are selected based on a set of tradeoff's which in turn are highly dependent upon output device Ft.

Section 8 covers the e-Amp compensation design more fully.

### 7.3 LTP Current Source

I spent some time deciding whether to go for active current sources or to use the legacy technique (Marshal Leach and Bart Locanthi designs are good examples) which is to derive the LTP tail currents from a Zener + resistor reference. For the active current sources, one can use the classic transistor+diode reference, the two back-to-back transistor variant or even a current mirror, where the attraction is that a single resistor can set both +ve and -ve tail currents, albeit with some additional complexity over the other options.

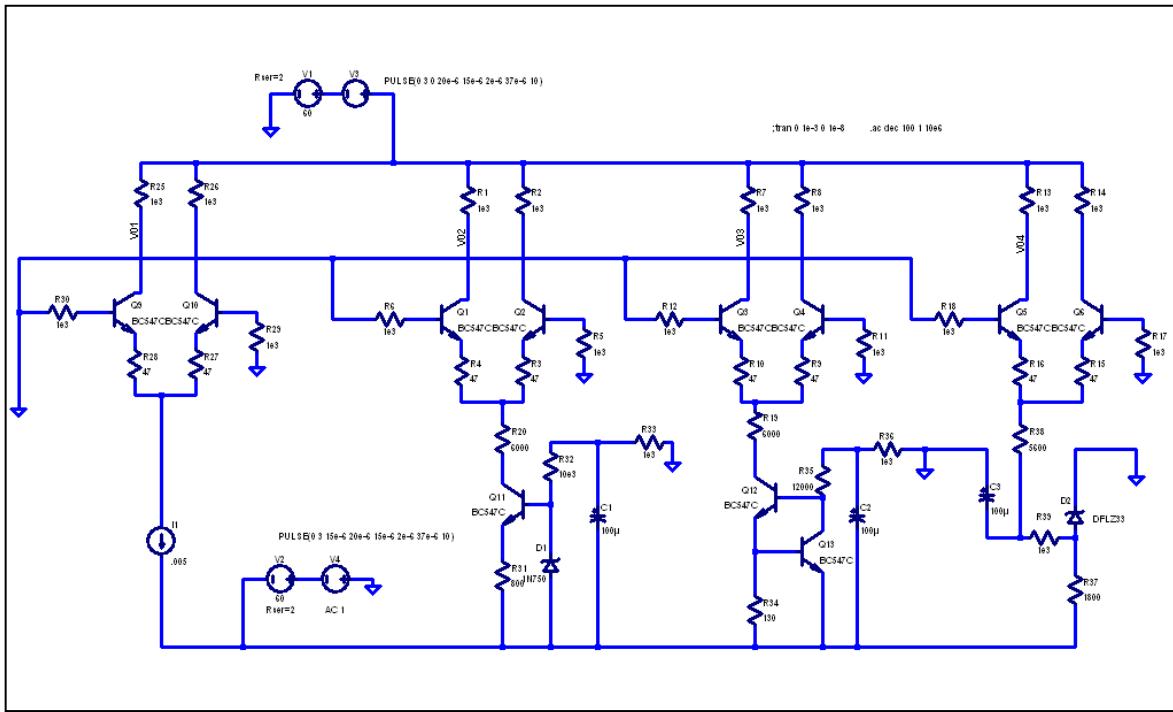


Figure 7 - e-Amp LTP Current Source Options

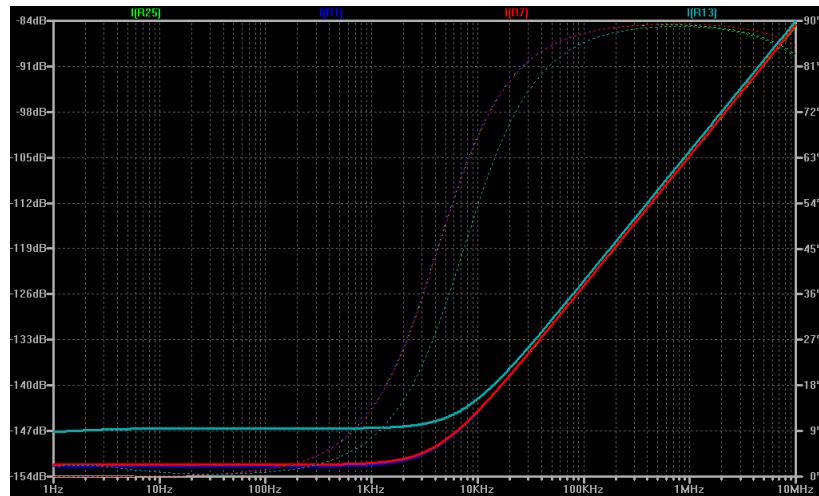


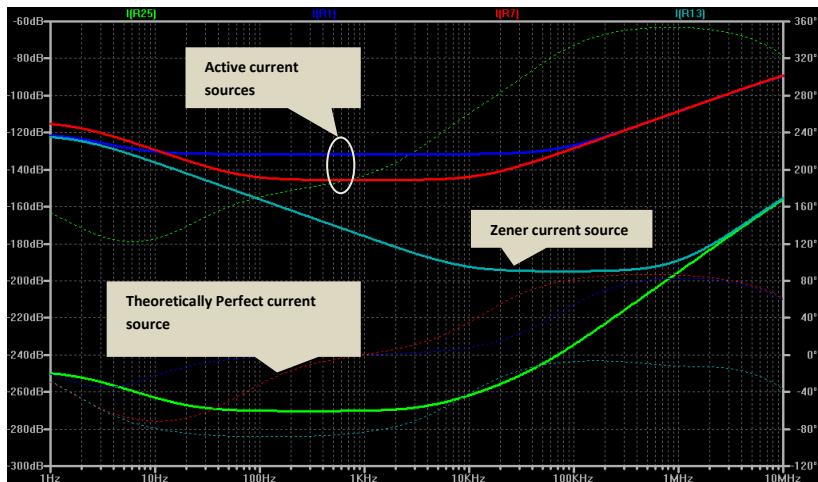
Figure 8 - Positive Supply Rejection of Current Source Options 1Hz to 10MHz for the 3 Current Source Designs

little worse at lower frequencies at -147 dB vs 154 dB for the active types and the theoretically perfect current source. The major limitation of the +ve supply rejection is due to the coupling of the +ve rail noise signal through to the bases of the LTP transistors via Cob. Here we see that one of the benefits of cascading the LTP transistors is to reduce this effect and improve PSRR, although at -126 dB there may be a temptation to concede that it is good enough without it.

Fig. 9 details the -ve rail rejection performance. The green trace is the ideal theoretical current source which is the reference. In both the active types, -ve rail rejection performance falls off (i.e. stops

Figure 8 details the options looked at and from left to right they are an ideal theoretical current source with infinite output impedance (for reference), the standard Vref based current source, the popular two transistor type and finally, the Zener derived source. On the output side of the LTP's (i.e. the diff amp collector load resistors) all of the current sources perform well in terms of +ve supply rejection (see Fig. 8). However, the Zener reference rejection is a

improving) between about 10 Hz and 200 Hz, whilst the Zener derived reference only levels off at 20 kHz and remains considerably better than the other practical options right up to the simulated limit of 10MHz. On the active types, you can cascode the current source transistor, or use a three transistor variant, to get better performance, but the Zener reference performance still cannot be matched.



**Figure 9 - LTP Current Source Performance -ve Supply Rail Rejection.**  
Green trace is the reference based on an ideal current source, dark blue and red the active current sources, and the light blue trace is the Zener + resistor source.

and tested. The Zener reference offers advantages at HF that are clearly evident from the simulation above, but you then have to worry about matching the diodes, and using some big decoupling and filtering capacitors. During prototype development, I consistently got readings across the 1% current sense resistors (R44 and R47 in Fig. 1) of within 2 mV of each other - a 0.6% current source match *without* any selection. This is considerably better than any of the other current source options.

## 7.4 LTP Load Options

For good performance, the tail current must be shared equally between the two transistors in each LTP (same applies to single ended designs as well). Simulation shows that only a small imbalance can lead to appreciable distortion. Traditionally, audio power amplifier designers have used either resistive load or a current mirror. With a current mirror, you get very good balancing between the transistors in the LTP pair and very high gain. Additionally, as discussed in section 7.2, the SR is doubled over that of resistive loading because all of the input stage tail current can be steered to charge Cdom - none of it is wasted flowing into the collector resistive load (see OR and OR in Fig 10). On the face of it, a current mirror load looks like a great solution – and it is on single ended designs like the Lin. However, in the FBS topology, current mirror LTP loads are not DC stable and the amplifier output drifts towards one of the supply rails and remains locked up there – a conventional DC servo won't help either - and as a result, you have to add a common mode current loop (CMCL) balancing circuit to keep the amplifier output centered<sup>12</sup>.

Further complications with the mirror load are that the amplifier loop gain is much higher and the designer has to wrestle with additional work on amplifier recovery after overload (clipping).

<sup>12</sup> See <http://www.synaesthesia.ca/front-end.html> for an example by Edmond Stuart and Ovidiu Popa on the challenges of designing and building a sub 1ppm distortion amplifier along with the DC balancing technique developed to address FBS mirror loaded LTP's.

The resistive load LTP was chosen for the e-Amp:- it is simple, there are no DC balance issues, ‘sticky rail’ occurs only in the VAS stage and as we will see a bit later, is easily remedied – and distortion performance is still outstanding. Regarding the requirement to balance tail current, this is set by the input voltage required by the VAS buffer and VAS output transistor  $V_{be}$ 's plus the voltage drop across the VAS emitter degeneration resistor. The easiest way to do this in practice is to calculate the initial resistor value, check it on a simulator and then tweak the final LTP collector load resistor on the prototype for lowest distortion. The process is simply to take 2  $V_{be}$  (since the VAS uses a two transistor follower configuration), allow for a further circa 1 ~ 1.5 V drop across the VAS amplifier emitter degeneration resistor (this is R27 and R69 in Fig 1) giving around 3 V. The load resistor is then calculated based on  $0.5 \times$  the LTP tail current which is 5 mA. In the e-Amp this gives a collector load resistor value of  $680\ \Omega$ . In the final design, I checked the value to ensure good balance and thus lowest distortion. This value will repeatedly give the lowest distortion across any number of amplifier replicas. Of course, a mirror load with well matched transistors will give better amplifier to amplifier LTP current balancing, but this comes at the expense of the CM balance issues discussed above. Separately, the other aspect investigated on the e-Amp was the effect of unbalanced currents between the two LTPs. Differences of up to 5% have only a minute effect on distortion – in the order of 2 ~ 3ppm. It is the balance between each half of the individual LTPs that is critical for low distortion, and this of course applies to both single ended and FBS topologies.

## 7.5 Feedback Network Coupling

There is a lot of commentary on the web (and in books) about the impact of electrolytic capacitors on amplifier sound and feedback network capacitive coupling. When you pass an audio signal through a *suitably sized, quality* electrolytic, the AP distortion analyzer shows zero (0) distortion – which, as Self points out in ‘Small Signal Analog Design’ intuitively it should do because it is a short at AC<sup>13</sup>. DA and DF are usually put forward as having detrimental sonic effects, but no concrete evidence to this effect has been shown. The usual solution to get around using an electrolytic capacitor is to use an opamp based servo. However, servo's are not without their problems, and one has to question whether or not the additional complexity really does bring real sonic benefits. Cordell has pointed out that servos are inside the amplifier feedback loop (as is the coupling cap), and this could also impart a sonic signature. Further, under overload conditions (severe clipping), or situations where there is a lot of very low frequency program material, servos can misbehave, and some sort of DC offset protection is needed for back-up. For this design, I capacitively coupled the feedback network using C7 and C23 to the inverting input of the amplifier. C7 is a large 1000  $\mu F$  16 V electrolytic device which is deliberately oversized in order to get around low frequency electrolytic distortion – a problem Cyril Bateman documented about 20 years ago. Provided you keep the AC voltage across an electrolytic to mV levels, this form of distortion can be eliminated. At HF (so ~ 1 MHz and above), the construction and lead inductance of electrolytic capacitors can cause impedance peaking, which will cause a dip in gain, and this is addressed by C23, a 0.1  $\mu F$  poly capacitor which simply bypasses the electrolytic. The input transistors are matched for hfe to within 10%

<sup>13</sup> If the AC voltage across an electrolytic is less than about 50 mVRMS, the distortion contribution is extremely low and can effectively be disregarded. The PGP amplifier (referenced elsewhere in this document), used an electrolytic coupling capacitor in the feedback network and achieved *under 1ppm* distortion at 20 kHz at high power levels.

and this gave offsets of <5 mV in two prototypes and in the two final boards. This design does not use a servo and therefore provides output offset adjustment facility by means of R80. Offset drift due to shifts in temperature from c. 25 °C to 65 °C is less than 1 mV and therefore well below any level that need be of concern.

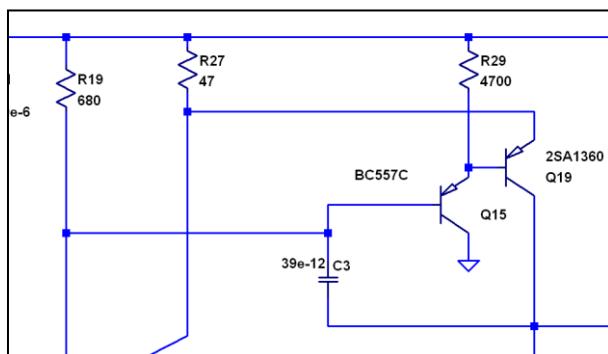
## 7.6 The VAS

In a conventional Miller Compensated (MC) voltage feedback amplifier, the VAS is in the form of an integrator, with the integrator capacitor formed by Cdom, and the input current provided from the LTP stage collector current. In the closed loop condition, the VAS stage thus has a critical task in converting what is a small signal current of a few micro amps (closed loop condition with normal program material) into a voltage that may swing 100 Vpk-pk or more on a reasonably high power amplifier.

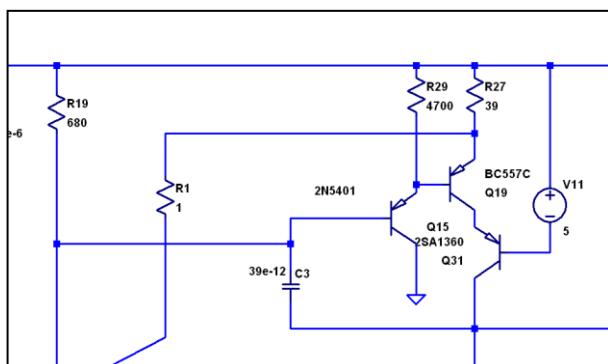
Critical design goals for any VFA VAS can be summarized as follows:-

- Convert small input currents from the front end LTP stage into large output voltages – this is therefore a high gain stage
- Highly linear - closed loop input LTP and VAS distortion should be in low single digit ppm range
- Provide adequate current drive to the output stages – the VAS standing current should therefore be much higher than the expected typical drive current to the output stages, including the usual buffer under worst-case conditions. It goes without saying then that this must be operated well into the class A region under *all* load conditions

Figure 9 - Standard beta enhanced VAS



- Swing to within a few volts of the supply rails ideally – so, maximize the potential power from the supply rails
- No ‘rail sticking’ – come out of clipping cleanly and with no parasitics
- Be tolerant of supply rail noise



For a VFA, there are many VAS variants but I will stick to conventional options which are the common emitter, Hawksford, cascode and folded cascode. It is important that the VAS local loop gain (i.e. the amplification stage enclosed by Cdom) is high in order to ensure maximum linearity and for this reason the VAS (Q29 and Q30 in Fig1)

Figure 10 - Cascoded VAS

transistors are preceded by ‘beta enhancement’ transistors Q8 and Q16. Without these transistors, the LF open loop gain (when the amp is configured for conventional Miller compensation) is reduced by about 12 dB (from 83 dB to 71 dB), and this has an important impact on the distortion performance of the amplifier across all frequencies. The collector output of the VAS can either drive the Vbe multiplier directly or use some form of cascode. Cascoding (See Fig 10) is usually used to enable the use of low voltage, high hfe small signal transistors for the VAS amplifier. Cascoding also increases the local VAS loop gain. It is very important that the VAS amplifier transistor, or if a cascode is being used the cascode transistor, has low Cob – and this means in the 2 pF to 3 pF region. The base collector voltage modulates Cob as it swings with the applied input signal, and this is a significant source of distortion in the VAS. Cascode transistors are typically biased at about 3 ~ 5 volts off their associated rails as shown in Fig 10. In general, the approach shown in Fig 9 is sufficient (20 ppm ~ 30 ppm open loop distortion at 20 kHz) although the Fig 10 variant will show about half that due to the reduction of Early effect in Q19.

Another interesting VAS design, is the Hawksford Cascode<sup>14</sup> shown in Fig 11, which achieves reductions in stage distortion an order of magnitude lower than conventional designs whether cascaded or not. In the Hawksford cascode, the cascode base current (an error term) is cancelled by drawing the base current through the emitter degeneration resistor (R27 in Fig 17) and returning it to the collector current of the same transistor (also known as ‘re-circulating’).

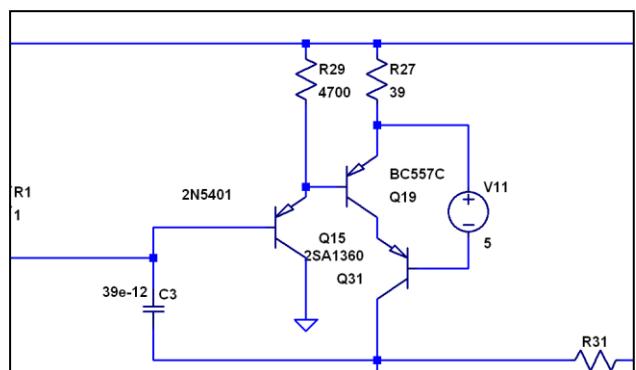


Figure 11 - Hawksford VAS

voltage swing is maximized – no auxiliary boost supply is required for the front end which is often required with cascode VAS stages (and often seen on mosfet amplifiers to meet the higher Vgs threshold). In simulation, the e-Amp VAS stage + pre-driver will swing 200 Ω load to 100 Vpk to pk at 20 kHz with less than 0.2% distortion, and with a load of 10 k, the figure is in the region of 6 ppm. Given the simplicity, this is good performance indeed.

Due to the high LTP current of 10 mA, when the e-Amp VAS transistor is driven into saturation, there is significant base charge storage in the main VAS transistors, which manifests itself as 3 ~ 4 µs of overhang or ‘stickiness’ on both the positive and negative peaks. At 20 kHz, this results in a truly horrible looking output waveform (see Fig 12 below) and a rapid and dangerous increase in amplifier supply current. The cure here is to use a Baker clamp which shunts base current away from the VAS transistor under overdrive conditions. I used BAV21 diodes (D10 and D11 in Fig. 1) because of their fast switching (c. 50 ns), and very importantly, reverse bias capacitance, which is typically in the region of about 1.2 pF at low reverse voltages. As a result, the Ovation e-Amp comes out of clipping very cleanly and there is little distortion contribution from the modulation of the diode reverse capacitance with VAS output voltage –

<sup>14</sup> REDUCTION OF TRANSISTOR SLOPE DISTORTION IN LARGE SIGNAL AMPLIFIERS, M.O.J. Hawksford, JAES, vol.36, no.4, pp.213 ~ 222, April 1988. A copy can be downloaded at [http://www.essex.ac.uk/csee/research/audio\\_lab/malcolms\\_publications.html](http://www.essex.ac.uk/csee/research/audio_lab/malcolms_publications.html)

in the region of low single digit ppm and swamped by other mechanisms in a practical amplifier such as this.

In designs driving mosfet output stages which have high input capacitance, rail sticking exacerbates local parasitic ringing in of the VAS as it exits clipping. This is caused by dynamic short term changes in device parameters (VAS and the mosfets input capacitance) with the changing signal voltage. The amplifier feedback loop tries to correct for this and the result is ringing. Focusing on trying to fix this problem with loop compensation will not work. In all cases, a decent VAS transistor (avoid MJE340/350 types for example) and a Baker clamp will clean things up. Bottom line: sticky rail has to be avoided at all costs.

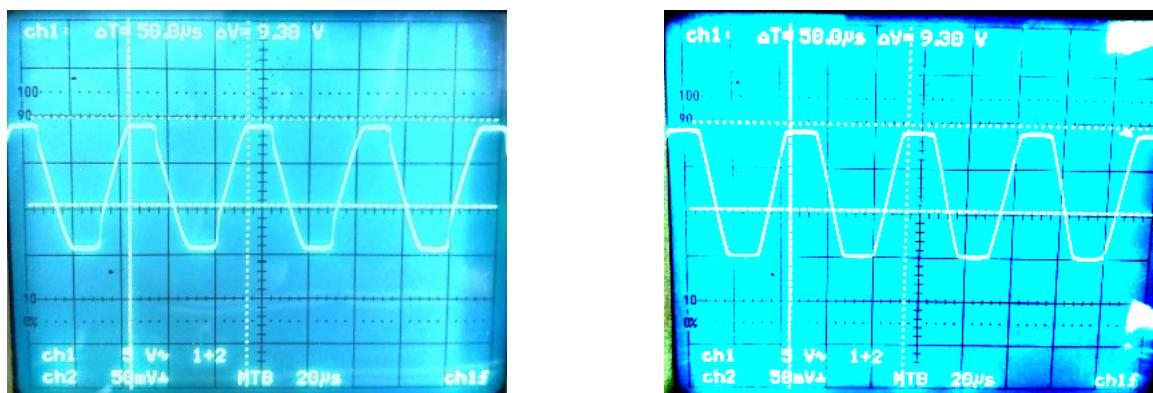


Figure 12 - Waveforms Without Baker Clamp (L) and with Baker Clamp (R). Waveforms captured at emitter of the driver stage. Vertical Scale is 50 V/division.

Some designs (e.g. John Curl's HCA-3500) and the earlier Krell amplifiers used mosfets configured in common source or folded cascode in the VAS stage. These designs will typically not suffer from rail sticking (the base charge storage mechanism in mosfets is different to bipolar devices and related to gate capacitance), and the saturation voltage is very low allowing the full rail of the amplifier to be exploited. Further, the front-end stage can be run at a higher gain (ratio of Rdegen to LTP collector load resistor) because the threshold voltage of the mosfets is higher than bipolars, allowing the use of a higher value LTP load resistor. However, the input capacitance of mosfets is both high and very non-linear; for this reason, it makes more sense to use MIC with these topologies and not MC. Additionally the PSRR in folded cascode designs is not as good as the common source variant, so these designs also benefit from capacitance multiplier techniques in the small signal and VAS supply rails. For now, this probably a topology I will reserve for further investigation in the future.

## 7.7 Keeping Things Quiet – Ripple Eater

The e-Amp employs ripple eater circuits (Q1, Q2, and associated components) to remove rail noise. Although the front-end current sources are heavily filtered and the LTPs are cascaded, if you are really looking for the best possible noise performance, a ripple eater is an invaluable circuit technique. The photo below shows the supply rail noise at 150 W into 8 Ω and - the upper trace is the mains ripple measured at V+ and superimposed on that the output signal. The bottom trace shows the noise on the supply rails to the front end after the ripple eater and it is well over 30 dB down. When this is coupled to the supply rail rejection afforded by the LTP pairs (through the action of feedback), hum and noise performance is very good – total wideband noise measured at the output is well under 1 mV into 8 Ω.

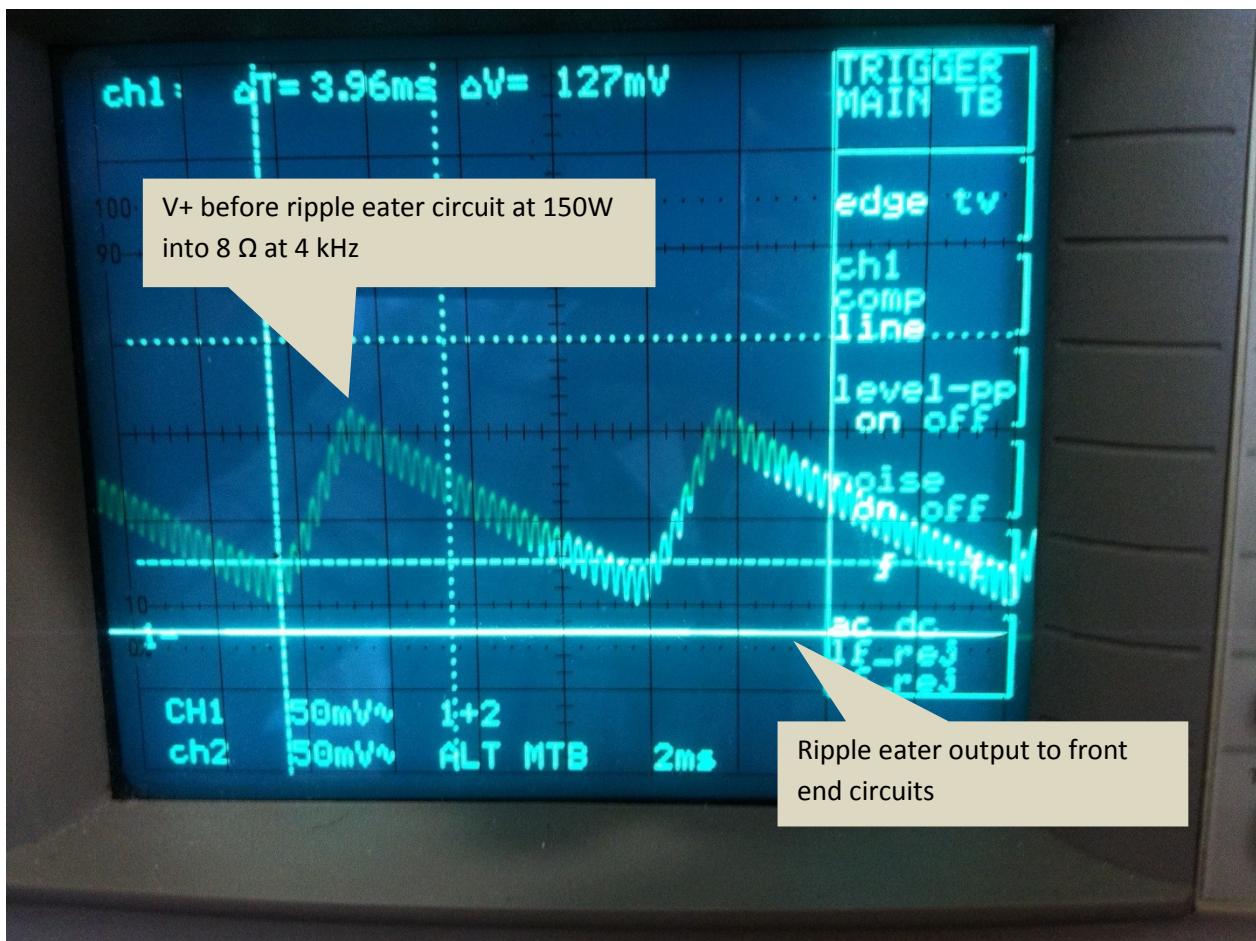


Photo 8 - Ripple Eater Performance (note: Upper trace scope probe switched to 10x)

Note also that the output signal appears as a half wave rectified replica on the supply rails. When playing music, the rails are ‘loaded’ with wideband hash from the rectified output signal (fundamental and harmonics to many hundreds of kHz) and this can feed into the front end and affect performance – and especially so at higher frequencies. Cascoding helps by preventing HF feed through via the collector base capacitance of the LTP pairs, and the e-Amp of course uses both techniques.

## 7.8 Output Stage

Mosfets (lateral and vertical types) have some very useful properties, chief amongst them are the lower drive requirements at audio frequencies and lack of secondary breakdown – simple current limiting is ample. Lateral mosfets are much more rugged than bipolar devices and can handle higher peak currents. Mosfets have a much higher  $F_t$  than bipolar devices (300 MHz is quite common), so compensation can be easier while more feedback can be applied if that is your persuasion, although you still have to look out for parasitic output stage instability – the solution is the same as for bipolar devices: use a gate stopper (=base stopper for bipolar) but the value is usually about 10x to 20x higher at  $30 \sim 100 \Omega$ . Simple buffering of the VAS is all that is required – usually no need for a double or triple follower. But, mosfets need to be reasonably matched if multiple pairs are going to be used in a linear application like a power amplifier. Thermal stability on lateral types is also good, however it usually comes at the expense of quite high drain current (to achieve the zero TC bias point) compared to bipolars.

Self showed that in mosfet output stages, the  $gm$  variation in the cross over region is substantially worse than in bipolar designs, and it is very difficult to get anything remotely like smooth signal handoff across the two halves of the output stage – a trick bipolar output stages are much better at. That said, Cordell and a few other designers have made the case that Self's mosfet models are inaccurate, and the  $gm$  cross over discontinuities nothing like as bad in the real world. However, if you want to reduce the cross over non-linearities to manageable levels, then the output quiescent current has to be set quite high – typically 120 mA to 150 mA per pair, and I have seen figures of 200 mA in some designs. On a big amplifier, this might entail 4 pairs totaling out at 600 mA to 800 mA on  $\pm 65$  V rails: - thus, you already have an output stage standing dissipation of 78 W to 104 W. This is about twice as much as an equivalent 4 pair bipolar output stage with  $0.33 \Omega$  output emitter degeneration resistors, although some designers would argue you may be able to get away with just 3 pairs of mosfets for the same rated power, which is a point I might concede.

Hawksford's seminal output stage error correction circuit<sup>15</sup> (HEC) addressed mosfet output stage non-linearity, with an early practical demonstration by Robert Cordell. Using this technique, he demonstrated a [mosfet](#) amplifier that surpassed bipolar output stage designs in performance terms. More recently, the 'Pretty Good Poweramp' or PGP, designed by Edmond Stuart and Ovidiu Popa used HEC and an advanced mirror loaded FBS front end design using nested feedback techniques to demonstrate full power 20 kHz THD of *under 1ppm* into  $8 \Omega^{16}$ .

Bipolar devices are easy to apply (although they need VI protection, or very generously designed output stages) and are currently about 30% ~ 40% less expensive per pair. However, for a high quality amp, you do have to factor in the additional driver stage and protection costs, and this means that output stage costs at a systems level probably favour mosfets. If the emitter degeneration resistor on bipolar designs is a reasonable value e.g. 0.27 to  $0.33 \Omega$ , matching of output devices, other than ensuring that they are from the same tube, is not required for good current sharing and distortion performance. On two

<sup>15</sup> See [http://www.essex.ac.uk/csee/research/audio\\_lab/malcolm\\_spudocs/J3\\_Distortion](http://www.essex.ac.uk/csee/research/audio_lab/malcolm_spudocs/J3_Distortion)

<sup>16</sup> See Edmond Stuart and Ovidiu Popa's design at <http://www.synesthesia.ca/PGP.html>

Ovation e-Amp prototypes, I measured a worst case spread across pairs of emitter degeneration resistors of 6 mA and 4 mA – i.e. under 8%. It should be noted in the design presented here that the output emitter degeneration resistors are *not* matched and are 5% types. Modern high power 200 W 15 A bipolar devices have  $F_t$ 's up at 30 MHz. While this is not as good as mosfets, it nevertheless facilitates designs with respectable amounts of feedback at 20 kHz – far removed from the days when power device  $F_t$ 's were in the order of 2 MHz. Since the hard turn on threshold voltage of bipolar devices is about 3 ~ 4 times lower than mosfets (0.65 V vs. 2 to 2.5 V), higher supply rails to the driver and VAS stages are not required in order to maximize the output device supply rail power delivery. The disadvantages of course are a more complex drive circuit.

The better open loop linearity – a correctly biased EF3 typically produces about 0.1% open loop distortion at mid power loads, rising to about 0.8% at full power - lower output stage quiescent current requirements in Class AB, and easier matching requirements were the reasons I chose to go with a bipolar output stage.

The output stage configuration used is a ‘triple follower’ based on the Locanthi ‘T’ circuit, developed in the 1960’s by Bart Locanthi (see [Locanthi Triple](#)) It was, and remains, the breakthrough bipolar amplifier output stage configuration and still the best choice if you are looking to maximize the gain bandwidth of a class AB output stage. Like the CFP output configuration however, you still have to take care of emitter follower parasitic oscillation. Topologies like the CFP or Darlington, might respectively give a bit more output swing, or load the VAS a little less, but the ‘T’ is the best overall solution where supply rail voltages are not a restriction, which is the case in the Ovation e-Amp.

For the ‘T’ the designer can employ either an EF2 (i.e. two transistor emitter follower) or an EF3 (three transistor emitter follower, also sometimes just called a ‘triple’ or EFT). I did some Spice simulations that showed that a triple has about an order of magnitude lower distortion in a closed loop amplifier compared to the double. Furthermore, insofar as distortion is concerned, the double shows little tolerance for changes in output load – just the kind of thing to be expected when driving a speaker where the impedance can vary between 2.5 to 16  $\Omega$  over the audio band. By contrast, when the amplifier uses the triple output stage, it shows under 10 ppm increase in distortion going from 8 to 4  $\Omega$  resistive load, this being mostly due to the increased loading of the VAS stage, especially at higher frequencies.

In the ‘T’ configuration, only the output stage (i.e. the NJW3281 and NJW1302 devices) halves switch in class AB – everything else is operated in class A. Running the pre-drivers and the drivers heavily in class A affords the opportunity to reduce the output distortion arising from switching artifacts that come about as one half of the output stage turns off and the other turns on, and avoid the use of any speed-up capacitors across the pre and driver stage emitter-emitter resistors.

EF3s (and to some extent EF2s) can suffer from high frequency parasitic oscillation, usually in the 10s of MHz range. This oscillation is brought about by the parasitic inductances in the transistor leads and PCB traces. When these inductive components are factored into the practical output circuit of an EF3, they form a Colpitts oscillator structure. Unless specific measures are taken to disassociate the parasitic elements from the active devices, its highly likely that the output stage will be unstable. On the Ovation

e-Amp, there are 2 ‘stopper’ networks per positive and negative output halves used for this purpose. I will only cover the top half here. They are R73, R66 and C15 in the base of the driver transistor Q24, and in the collector circuit of Q25, the pre-driver, R3, R33 and C9. These networks effectively swamp (or damp) the lead and trace inductances, breaking the formation of any Colpitts structures, ensuring that the e-Amp EF3 output stage remains stable under all conditions. The additional complexity may be questioned, however, the benefits of the EF3 are much lower load on the VAS stage, improving VAS linearity and effectively raising the open loop gain, and importantly, allowing this amplifier to drive short term loads as low as  $2\ \Omega$  with less than 50 ppm additional distortion. Few other output stage configurations or device technologies can deliver this type of performance.

## 7.9 Output Device Protection: The Tradeoff Game

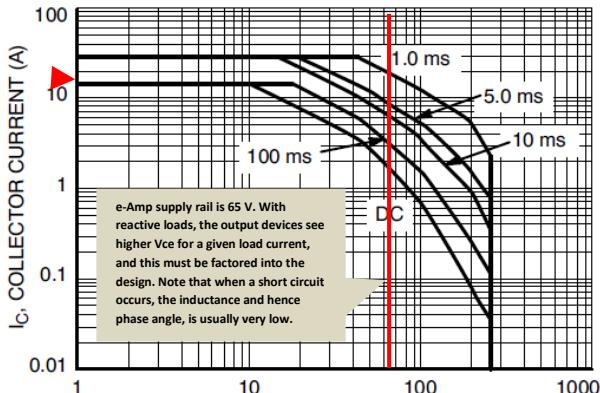


Figure 13 – NJW3281/1302 SOA. The 65 V Vce 1ms Ic capability is 18A (note: rating shown for 25 °C - at higher temperatures the curves are derated)

For commercial and industrial grade applications, protection is necessary, since you can never be sure of the operating environment, and typically will include SOA limiting on bipolar technology output stages, and simple current limiting on mosfet designs. In the Ovation 250, I used 3-slope SOA protection, but later concluded it was too aggressive and intruded on the amplifier sound. On the e-Amp, LTSpice investigation showed that even with very benign protection, driving a 3 Ω 60 degree load (which is an exceedingly heavy worst case scenario), distortion performance was compromised, and to get around this, protection eventually had to be backed off so much it was ineffective, or, the number of output devices had to be increased significantly. In order to be able to handle difficult low impedance and reactive loads (and reduce distortion), the e-Amp employs 5 output devices per rail on ± 65 V rails. In the e-Amp, only simple current limiting is used by measuring the  $I^2R$  voltage drop across one pair of emitter degen resistors (R52 and R53) using an opto-isolator which feeds into a separate MCU based control board. In a practical hi-fi application, the typical load impedance between about 80 Hz and 1 kHz will be in the 3 ~ 4 Ω region, with dips down to 2 Ω at certain frequencies (speaker model dependent of course). Above about 1 kHz, the impedance starts to increase, while at below about 100 Hz, it increases rapidly as the speaker LF resonance peak is approached. Further below this, the speaker DC coil resistance dominates. 10 A fuses provide back stop protection and these are mounted on the main amplifier PCB. Using this simple protection scheme, the Ovation e-Amp can deliver over 30 A for short periods (50 ms) without any protection circuitry affecting the sonics. In the event of a dead short circuit (so >>40 A with the full supply rail across the output devices), the SSR protection scheme on the control board disengages the speaker in under 50 μs, protecting the amplifier. From the SOA curves in Fig. 13, assuming worst-case ± 65 V supply rail (resistive load – a highly reactive load is another matter entirely), the output device capability is bounded by the 1 ms curve above – i.e. about 18 A, or 90 A for the total amplifier with 5 output pairs.

## 7.10 Vbe Spreader and Thermal Compensation

The Vbe multiplier (bias spreader) circuit consists of two transistors (Q7 is the temperature sensor transistor and Q12 is the spreader shunt transistor in Fig. 1) in a CFP arrangement. With the standard Lin topology (aka Douglas Self's 'Blameless'), the VAS standing current is pretty much fixed by the current source load under normal operating conditions<sup>17</sup>. In the Ovation e-Amp and other designs that employ

<sup>17</sup> Lin topology amps have non-symmetrical drive capability, so the VAS transistor in this topology can conduct higher currents than that set by its current source load, especially in current limit or high output current drive situations.

this topology, the VAS standing current can change under heavy load conditions in which the output protection circuit activates. It is important therefore to ensure that the Vbe multiplier remains well regulated so that the output stage standing currents are tightly controlled, hence the requirement for a high gain two transistor circuit. There are other techniques using a single transistor with some slope compensation using a resistor, but these have a higher shunt impedance than the variant used in this design.

Initial set up is accomplished by adjusting the bias potentiometer so that you measure a volt drop across any pair of output emitter resistors ( $2 \times 0.33 \Omega = 0.66 \Omega$ ) of 52 mV. The figure of 52 mV (or 26 mV across a single emitter resistor) is the optimum emitter resistor volt drop in class AB amplifiers for minimum distortion. Note in this design, that the pre-drivers are also mounted on the main heatsink. In a triple, my approach is to try to keep the output stage devices iso-thermal – more easily said than done in practice (I measured 5 to 7 °C delta between devices using a hand held IR gun type thermometer). In competing designs that mount the pre-drivers on separate heatsinks, care has to be taken where the sensing device is mounted. If for example, the pre-drivers run hot, but you are sensing the output device temperature, you are going to get big shifts in quiescent current during warm up. In this type of layout, you need to sense the pre-driver temperature – both Self and Cordell discuss this in their books.

My preferred technique for temperature sensing is to use a small SMD (Q7) device which I closely locate to one of the output device collector leads (easy to do with PCB mount TO247/264 style packages) and then tightly couple this thermally by the application of a small amount of thermal grease over the SMD device and the output device collector lead. Because the SMD device has a low thermal mass, it can respond rapidly to the output device temperature changes, although I have to admit, never as quickly as a co-packaged sensor like the ON NJL1302 and NJL3281 devices (see the data sheet here [NJL3281](#)). However, in a triple, the output device Vbe shift with temperature is only 1/3<sup>rd</sup> of the temp comp problem. The temperature slope of the sensor transistor can be adjusted somewhat by altering the collector current of Q7 between about -1.95 mV per °C and up to about -2.2 mV per °C, which is how I arrived at the 1 k Ω collector load resistor (R39) you see in the circuit (Fig. 1). However, in triples, fast, accurate thermal compensation with just a simple CFP spreader can be difficult and in the Ovation e-Amp, I use a two-point temperature compensation with the aid of a 10 k NTC (R75). R75 is mounted close to one of the output transistor collectors on the component side of the PCB. To calibrate the temperature compensation circuit, R76 + R77 PCB locations are bridged with a 20 k potentiometer - set initially to 10 k - and R7 adjusted for the correct output stage Iq about 1 minute after power up (which is the time it takes to stabilize after switch on). Iq compensation is then accurate to within 10% up until about 50 °C, after which Iq rapidly diverges (increases) from the ideal value. Once the heatsink temperature reaches 65 °C, the 20 k potentiometer is adjusted to get the correct Iq level again (52 mV as measured across a pair of output stage 0.33 Ω degeneration resistors). The potentiometer is removed and R76 and R77 are then installed with a total value which is the same as the potentiometer setting. This is a one time calibration cycle and is fixed for the mechanical and electrical design of the amplifier. This calibration method starts out by setting Iq at ambient (assumed to be 22 ~ 27 °C) and then readjusting it at a second, higher temperature point (65°C). When R76 and R77 are set to the correct value, this moves the original ambient calibration point down in temperature, effectively spreading the two calibration points apart by 10 to 15 °C (the 65°C cal point is fixed and does not move),

such that the effective calibration points are 12 to 17 °C ('adjusted' ambient) and 65 °C. Using this technique, the output stage  $I_q$  variation is better than  $\pm 10$  mA around the nominal 78 mA value for all output power levels and ambient temperature conditions after allowing for a few 10s of seconds recovery period after a high power music burst. Temperature compensating EF2s is easy compared to triples, and I have to admit that some of the linearity gains made in moving from an EF2 to an EF3 are lost in the short-term dynamic variation of  $I_q$  with program material. However, in designs like this that have moderate loop gains (especially with the loaded VAS and WB-TMC discussed under Compensation later on), you are still well ahead with the triple. The only way to get open loop 0.01% output stage distortion, considering both temperature and load, is to provide some form of error correction. However, HEC as applied to bipolar output stages is problematic, requiring elevated driver supply rails and additional power dissipation. For now, I think the Ovation e-Amp output stage and associated temperature compensation performance for the level of complexity involved is very good.

Fig. 14 and Fig. 15 graphs below help to visualize the thermal compensation approach.

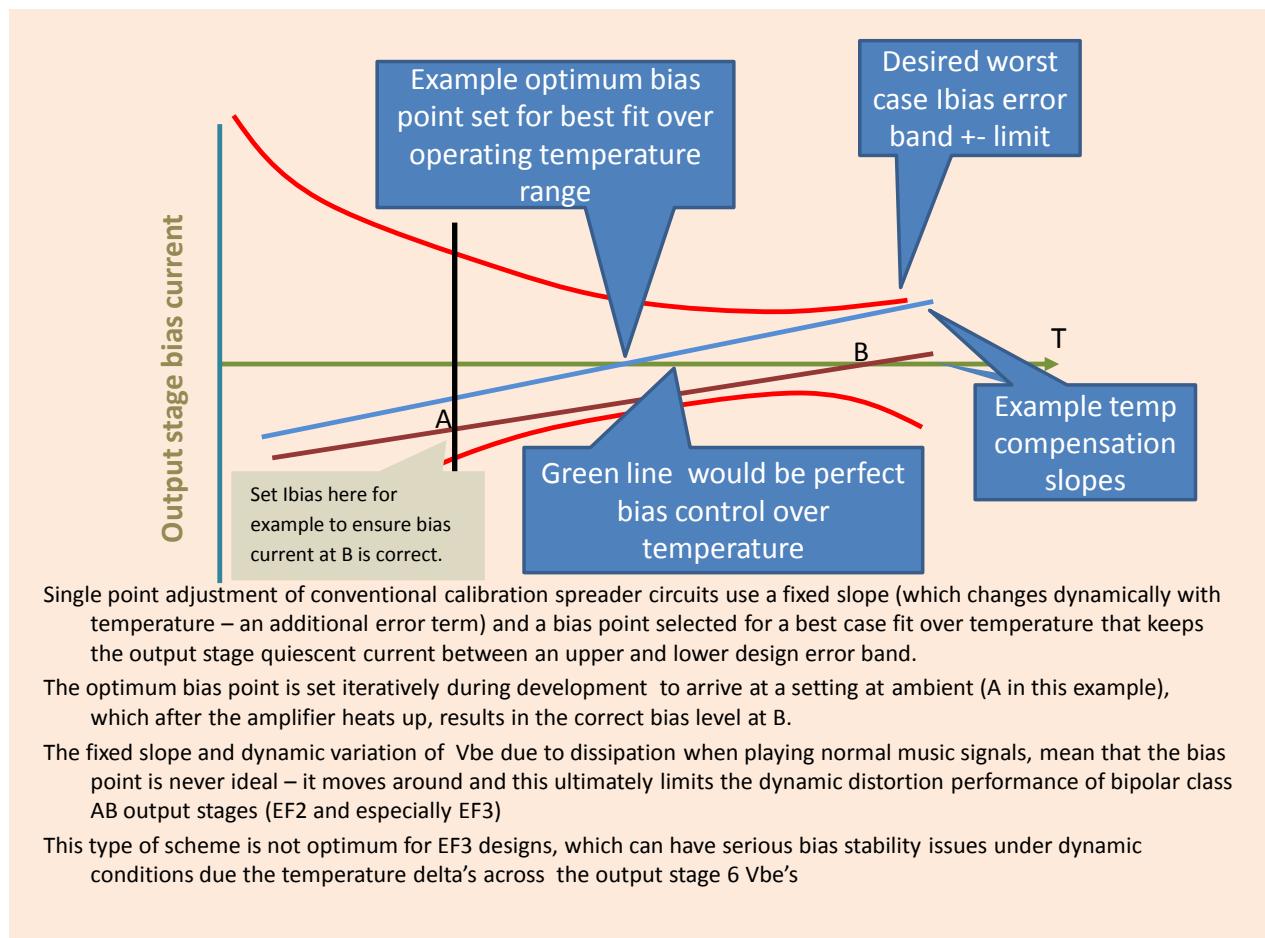


Figure 14 – Conventional Single Point Thermal Compensation

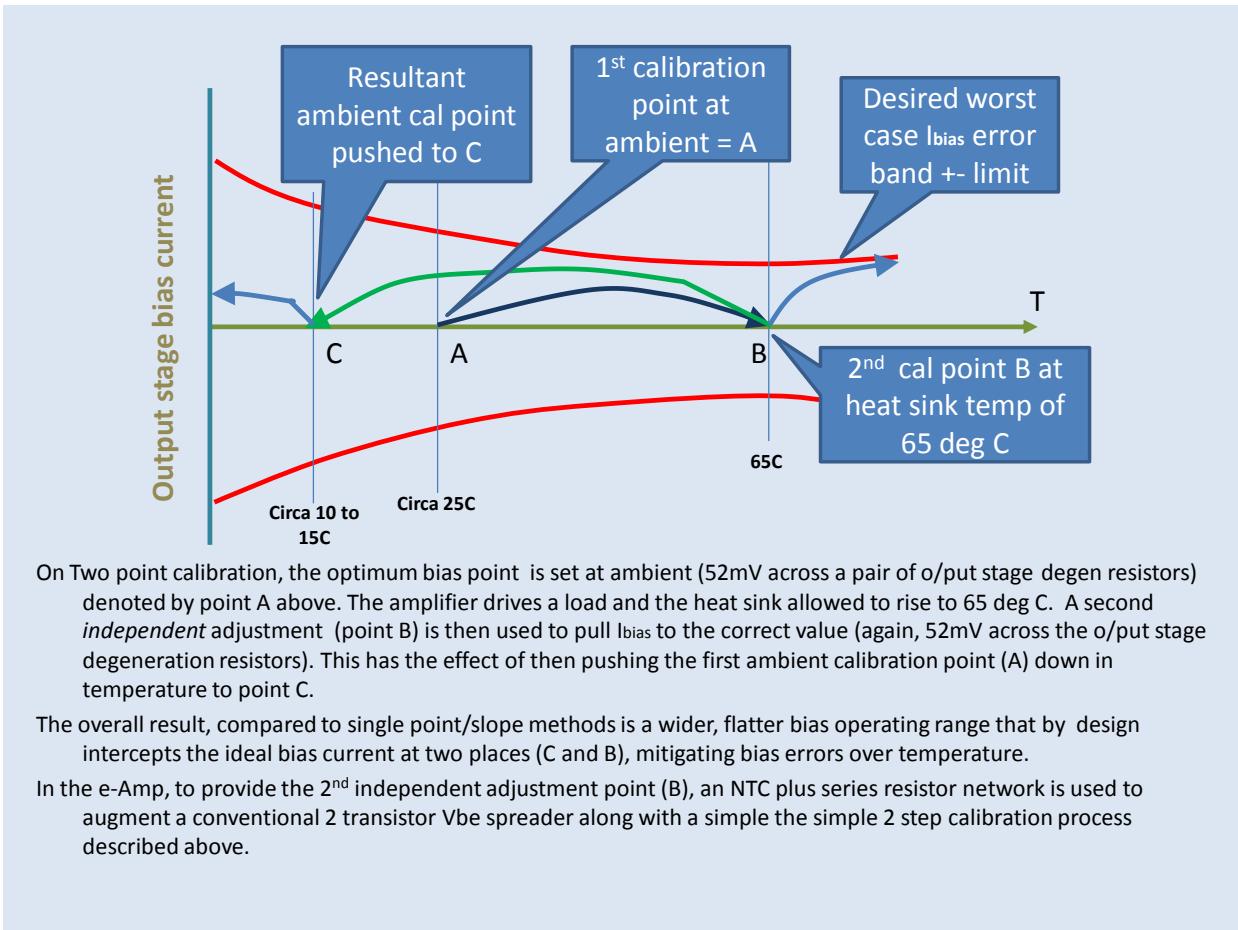
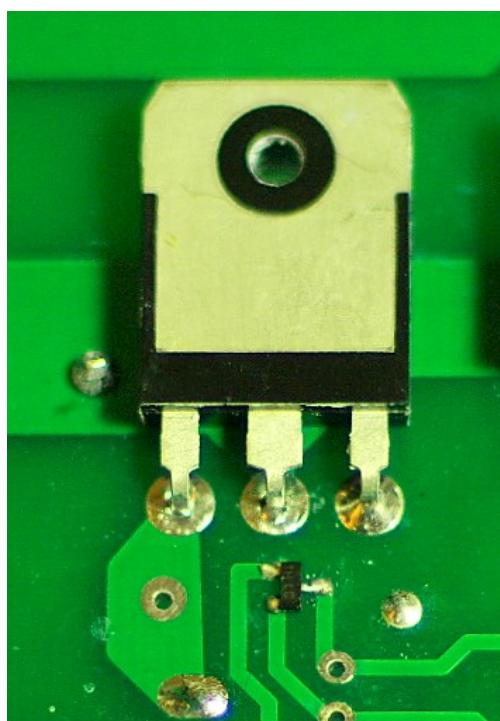


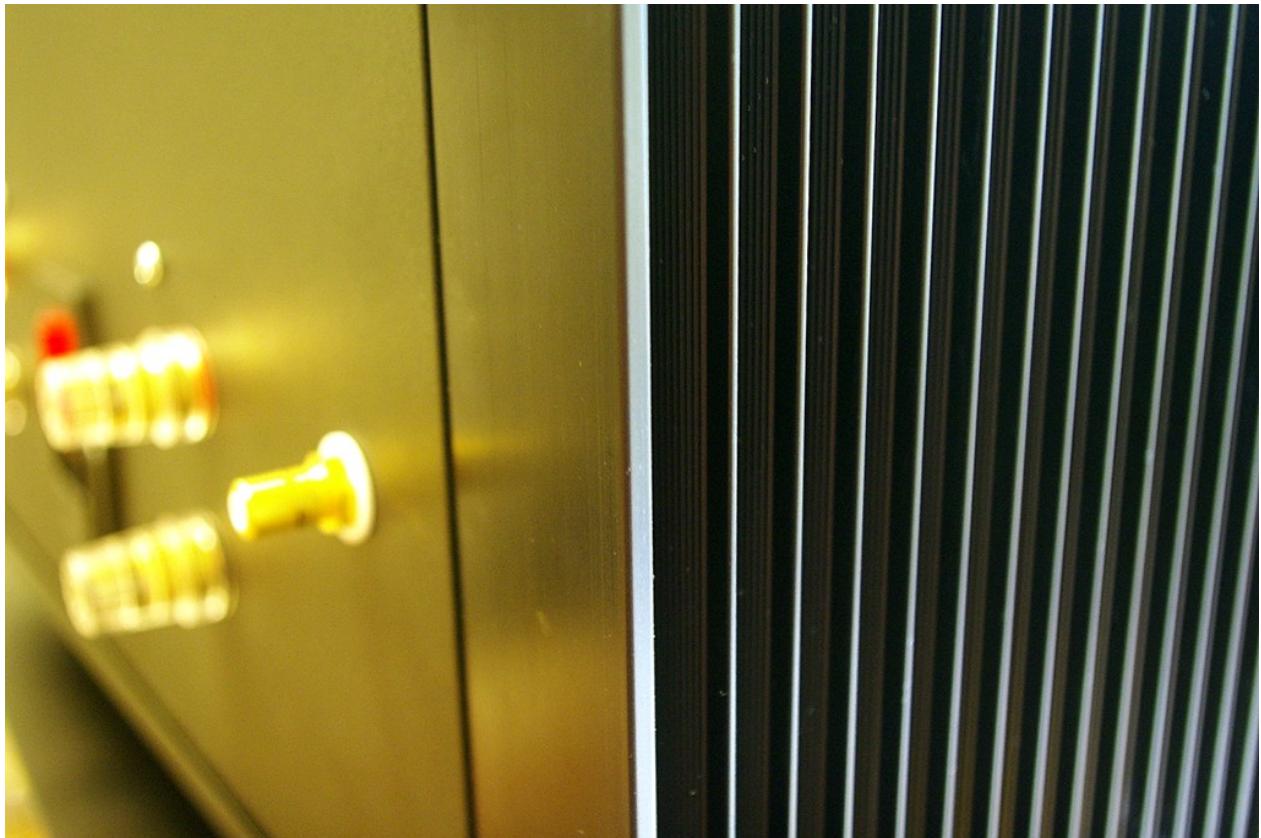
Figure 15 - Two Point Thermal Compensation as used on the e-Amp



The picture on the left shows the temperature sense transistor Q7 (BC847C) located in close proximity to Q6, one of the output devices prior to the application of a small amount to thermal grease between the two devices to improve coupling.

The tab and die header temperature of the power transistor are within a few °C of each other and respond quickly to changes in power dissipation. The collector lead (which is part of the header) therefore makes an ideal place to sense temperature.

Photo 9 - Temperature Sensing Technique



## 8. Feedback and Compensation

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There still remains quite some debate within the audio design community on the sonic benefits of wide open loop bandwidth (but lower open loop gain) vs. low open loop bandwidth (but high open loop gain), centering around the causes of PIMD (Phase Inter-Modulation Distortion). And this is before we have even begun to consider Zero Global Feedback vs. Global Feedback debate. With regard to PIMD, the finger of blame has been pointed at the modulation of the loop gain corner frequency in voltage feedback amplifiers. The protagonists have different views on the audibility, the level of PIMD in feedback amplifiers and the cure. Some claim that having the loop gain corner frequency well above 20 kHz may mitigate the problem, since PIM primarily affects signals above the corner frequency.

Techniques include the creation of a 2<sup>nd</sup> nested feedback loop with feedback coming off the VAS itself back to the inverting input (Miller Inclusive Compensation, or MIC), or even resistive feedback around the VAS, as Self has shown. Cordell has written a concise paper ([phase\\_intermodulation\\_distortion.pdf](#)) on the subject, and in his view, negative feedback all but completely removes the problem.

In the Ovation e-Amp, different compensation modes can be selected by installing or removing PCB jumpers. I originally thought about fitting relays actuated by a front panel switch to accomplish this, but a line has to be drawn somewhere in terms of complexity. The current iteration of this design does not include MIC in the available options, but that will be the subject of a future design. Using simple VAS loading allows loop gain right across the audio band to be reduced, allowing room to experiment more freely on the audibility or not of PIMD, and the general ‘sound’ of the amplifier. Here’s what I target with compensation in my designs:-

1. Through the action of feedback, reduce distortion across the audio band
2. Ensure adequate gain and phase margins - therefore the amplifier must remain stable into all real world loads.
3. The amplifier must display zero oscillation, zero amplifier ringing/overshoot into resistive loads when driving a load without a series output inductor
4. Be highly tolerant of capacitive loads covering all practical possibilities when the load is driven through a 1-2 µH inductor in series with the output
5. Accept any real world input signal and not suffer from TIM/SID distortion phenomena

For general, simple feedback systems like amplifiers, the easiest and most convenient method to analyze and compensate an amplifier is to use Bode analysis in a simulator. It then becomes a simple matter to adjust values to optimize the performance because as a designer, you are able to ask ‘what if’, then make the change in the simulator, and then observe the results and then try it out on the physical prototype. As part of an iterative design process, this gets one going in the right direction, and the final, optimal compensation component values can quickly be converged upon.

## 8.1 Standard Miller Compensation (MC)

To kick off, a first guess at Cdom is needed, and that entails some thought about the unity gain bandwidth (UGBW) frequency of the loop. In a typical modern bipolar power audio amplifier with 30 MHz GBW output transistors (the GBW frequency varying markedly with collector current by the way) like the ones used in this design, the UGBW of the loop is set between about 0.5 and 1.5 MHz, the upper value limited by the high frequency poles in the amplifier output stages. For amplifiers using legacy transistors like the 2N3055/2955, the UGBW loop frequency had to be set well below 500 kHz, which amongst other things is why these old designs were doing well at 0.1% THD. The *UGBW loop frequency is fixed* as part of the design – you cannot simply decide to raise it in order to increase the amount of feedback at lower frequencies because the result will be instability as the HF pole(s) gains rise above unity before the higher UG cross over frequency. Assuming a -20 dB/decade loop roll-off in response, the upper loop UGBW limit is set by the amount of phase shift in the overall system loop, and the lower limit is then fixed by the 20 dB/decade roll-off response. If the -3 dB corner frequency is assumed to be somewhere below 2 ~ 3 kHz (a very reasonable assumption in an amplifier that uses MC like this design), then a GBW of 2 MHz would imply 40 dB of loop gain at 20 kHz, and 60 dB at 2 kHz. Likewise, if the loop UGBW were set at 1 MHz, then the amount of feedback at the frequencies mentioned above would be about 6 dB lower. At this stage, the exact value is not critical because you have to fine tune the compensation design on the bench. To kick this exercise off, the initial UGBW value will be set at 1 MHz – a practical, value for this design. The value of Cdom is then calculated from

$$C_{dom} = 1/[2*\pi*fx*Acl*2*(R_{degen}+r_e')]^{18}$$

Where fx = the UGBW frequency – set initially to 1 MHz

Acl = is the closed loop gain magnitude below the -3 db roll off point – i.e. low frequency gain – set to 35

Rdegen is the LTP emitter degeneration resistor which is 100 Ω in this design

r<sub>e</sub> is the internal emitter resistance of the LTP transistors from [0.026/(2\*LTP tail current)]

Rdegen is selected independently selected as described in section 7.2 to ensure that the front-end stage remains linear, and for a resistively loaded LTP, assuming a 350 kHz -3 dB input filter, a voltage drop across Rdegen of about 0.5 V is a good value. For a standing LTP current of 5 mA (so half of the 10 mA LTP current source), this gives a value of 100 Ω.

Using the above, we arrive at a value of 30 pF for Cdom. Slew rate (SR) can be independently adjusted by adjusting the LTP tail current (there is also a small influence from r<sub>e</sub>', but the approximation is good enough for our purposes at the kind of tail currents we are talking about here) and for the values given above, excluding the effect of the front-end filter, this is 155 V/ μs. If the LTP was mirror loaded, the slew rate would be double this figure. The SR can also be increased by increasing Rdegen, but in order to maintain the same UGBW frequency, Cdom would have to be decreased, since there is no point in lowering the UGBW it as this sacrifices OLG. It should again be stressed that the front end filter discussed

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<sup>18</sup> This formula is referenced from many texts - Self, Cordell and Marshal Leach amongst others

earlier in section 7.2 forms an important part of the overall compensation of the amplifier – the high slew rate + the 150 kHz front end filter cut off frequency ensure that the e-Amp will never suffer from TIM problems.

For the e-Amp, I used the Michael Tian et al<sup>19</sup> technique for extracting the *loop gain and phase data* as given in the examples folder of LTSpiceIV in the file called ‘Loop2’.

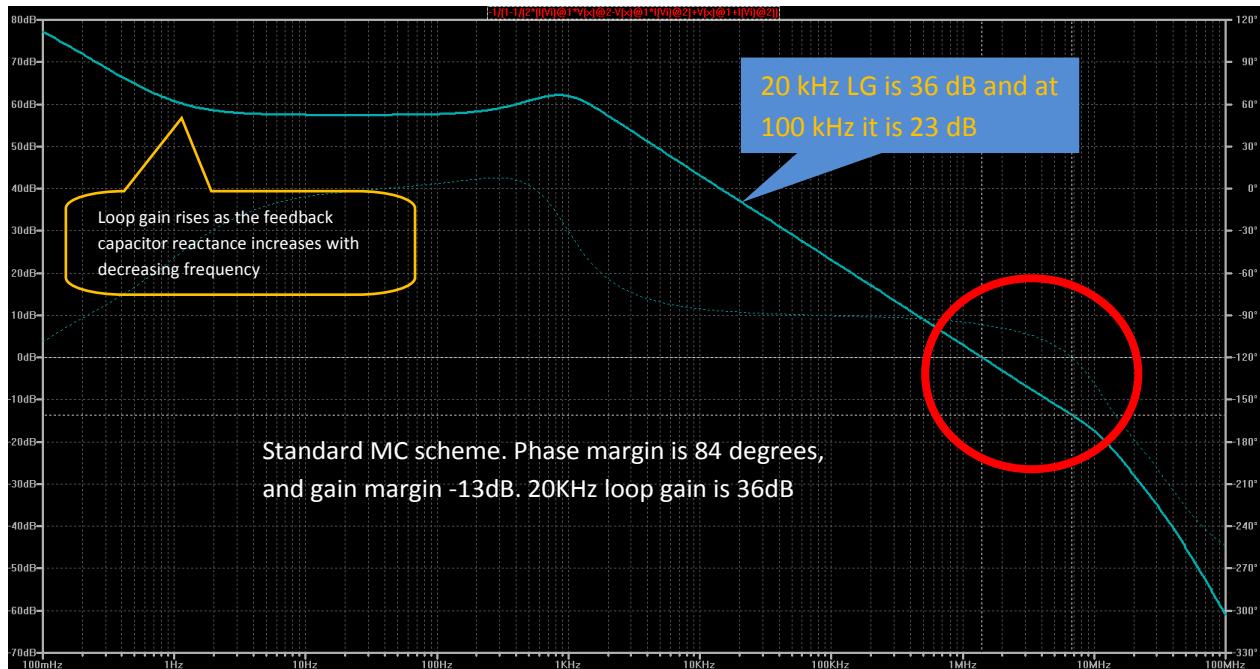


Figure 16 - e-Amp Loop Gain and Phase Plot – Standard MC

Fig. 16 details the standard MC loop gain and phase plot for the e-Amp. The phase margin at the UGBW frequency of 1.3 MHz is 84 degrees (180 - 96), and the gain margin is -13 dB. The recommended *minimum* phase margin for an audio amplifier is 45 degrees, and gain margin is 6 dB. However, I decided to keep this significant phase and gain margin in hand in order to be able to apply TMC more easily and still have plenty of gain and phase latitude, which will be covered a little further on.

The final test has to be done on the bench where the amplifier must be loaded with an 8 Ω resistor before the output inductor and driven with a 10 kHz square wave of about 2 V pk to pk, with a rise time of about 2 μs (no point in faster rise times, and rise time should also not be much slower than this). The output should not show any signs of overshoot or ringing into a purely resistive load. The next step is to apply a range of capacitive loads across the load resistor connected in the normal fashion after the output inductor, typically from about 100 pF all the way up to 2 μF – half decade values (so 100 pF, 500 pF, 1 nF, 5 nF etc) will normally be sufficient. The final tests must entail the amplifier driving a 2 to 22 Ω range load with the different parallel capacitance values discussed above, varying the square wave frequency between about 3 kHz and 100 kHz to look for potential problems. Note that when driving a

<sup>19</sup> [1] Michael Tian, V. Visvanathan, Jeffrey Hantgan, and Kenneth Kundert,

"Striving for Small-Signal Stability", IEEE Circuits and Devices Magazine, vol. 17, no. 1, pp. 31 ~ 41, January 2001.

capacitive load, you will get ringing as the output inductor forms a tank circuit with the load capacitance at a frequency of  $1/[2\pi\sqrt{LC}]$  – this ringing has nothing to do with amplifier stability and is quite normal.

On a bipolar output stage power amplifier, loop instability will typically show up as oscillation between about 50 kHz up to 1 MHz. Values much beyond this would indicate possible parasitic oscillation, and that is a separate problem from loop stability, and will normally entail a different set of cures. In the tests described above, there must be no indication of any instability.

It is during this bench testing process that the designer can elect to push the UGBW frequency up in order to maximize feedback. In this design, if  $C_{dom}$  were reduced to 10 pF, it would move the UGBW to 3 MHz and the loop gain at 20 kHz from 36 dB to 46 dB. But, with this small value of  $C_{dom}$ , the phase margin rapidly decreases (and here we are *definitely* on the slippery slope of device to device parametric spreads, layout etc) and the gain margin also declines. If you load an amplifier like this with a worst case real world load, even with the output inductor, the phase margin deteriorates very rapidly. There are techniques, like lead compensation across the feedback resistor, that will allow you to claw back some of the gain and phase margin, but then you have to contend with RF ingress and you still have to deal with component spreads and so forth from unit to unit. What is important is that the final compensation design leaves *plenty of leeway* for driving capacitive loads. There are too many designs (some published in popular electronics magazines), where in the mistaken notion of chasing the lowest possible distortion, the final result is more often than not a marginally stable amplifier that breaks into oscillation, or rings, with real world loads. I also know from my own amplifier construction experience that stable amplifiers sound better than ones optimized for low distortion at the expense of stability margin. Stability should always take priority over shooting for the lowest distortion.

## 8.2 Transitional Miller Compensation (TMC)<sup>20</sup>

In the e-Amp, invoking TMC requires fitting jumpers J7 and J8 which connect an additional set of capacitors and resistors into the compensation network. TMC works by enclosing the output stage within the  $C_{dom}$  local feedback loop, and then transitioning the output stage out of the  $C_{dom}$ -VAS loop at HF where output stage phase shifts become troublesome. This contrasts markedly with MC, where the output stage is never included in the  $C_{dom}$ -VAS loop, and in order to maintain stability, feedback is actually curtailed ('thrown away') at HF to ensure that the output stage poles fall below the unity gain cross over frequency. In TMC, the typical transition frequency depends upon the output devices but a figure of between 500 kHz and 1 MHz appears to give the best results with the output stage devices used in this design. In the Ovation e-Amp, with a 26 degree phase margin impact (and this is why the MC phase margin was left at 84 degrees), TMC improves the available feedback at 20 kHz from 36 dB in the standard MC configuration, to around 51 dB. This delivers a 5x reduction in THD at 20 kHz – a very

<sup>20</sup> Independently developed and brought into the audio mainstream over the last few years by Edmond Stuart. See <http://www.data-odyssey.nl/> for in depth discussions around some of the latest amplifier design and compensation techniques. Peter Baxandall also appears to have been thinking about TMC compensation shortly before he died in the 1990's - see [here](#)

significant improvement for the cost of 2 resistors and 2 capacitors<sup>21</sup>. I tested TMC extensively on my other design, the Ovation 250, and can confirm that it is very reliable and if implemented correctly with a reasonable transition frequency and does not suffer from any tendencies to oscillate or ring. Fig. 18 shows the TMC loop gain and phase performance.

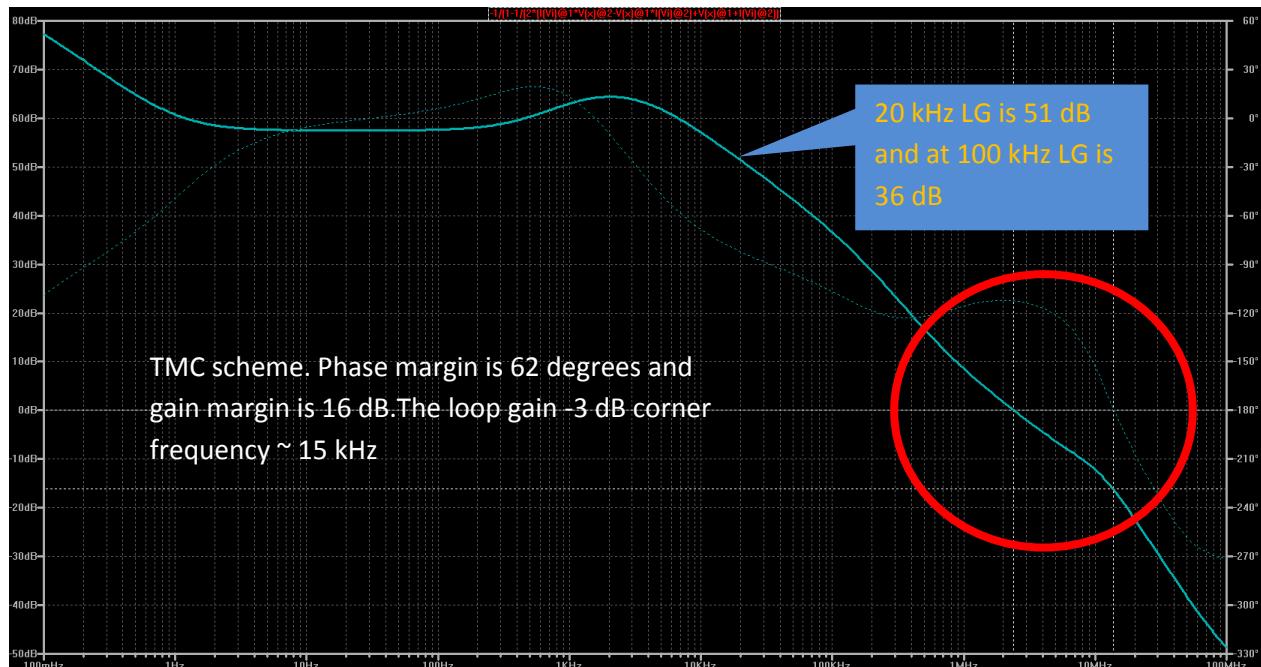


Figure 17 - e-Amp with TMC Compensation

### 8.3 Hybrid Wide Band Feedback (WBF) + TMC

The next e-Amp compensation configuration to explore is a hybrid ‘Wide Band Feedback’ or WBF+TMC (see Fig. 18). Here, TMC is combined with light VAS stage loading to push the loop gain -3 dB point up to about 40 kHz, to ensure the feedback factor (i.e. loop gain) is constant across the audio band. Recall from earlier discussions that some designers believe that PIMD is caused primarily by the loop gain corner frequency lying within the audio band – and for conventional MC on the Ovation e-amp, this is about 2 kHz (see Fig. 17). The corner frequency is modulated by changes in input stage  $gm$  as the input signal varies. By loading the VAS (insert jumper J6), the loop gain is flattened, but with the help of the TMC loop, still maintained at a reasonable level, such that at 20 kHz there is 46 dB of feedback. Again, as with the previous two compensation schemes, there is enough gain and phase margin, and the amplifier remains unconditionally stable.

<sup>21</sup> On a Lin topology amplifier, it would take only 1 extra resistor and capacitor

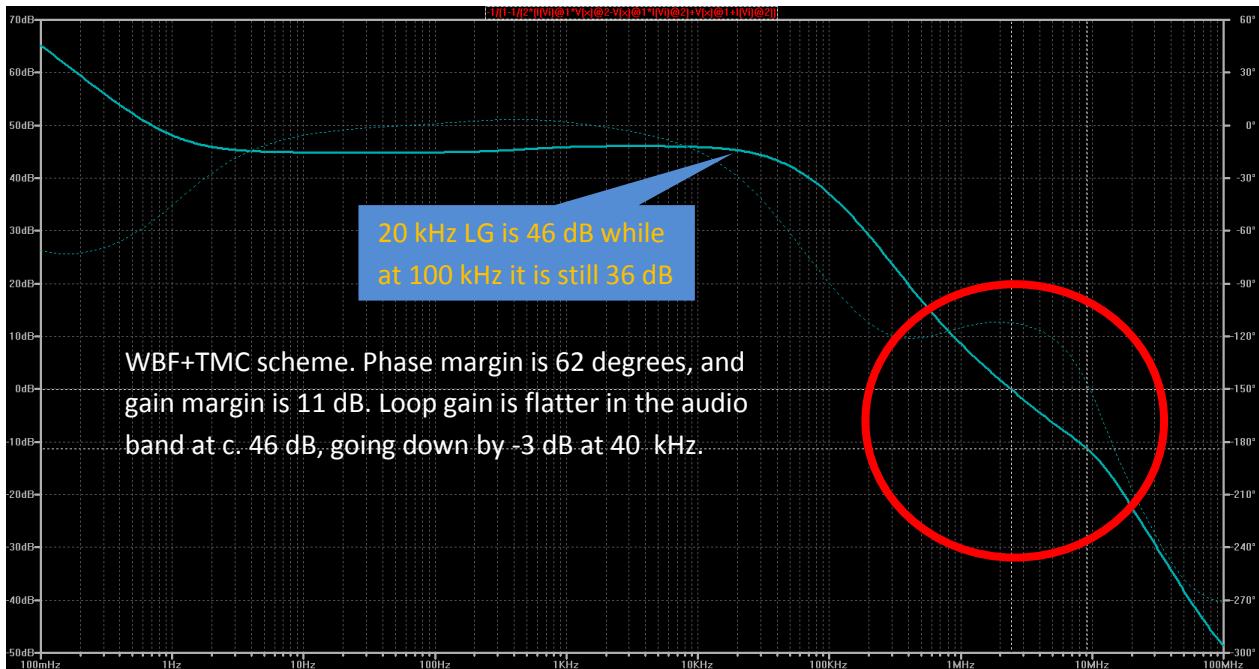


Figure 18 - WBF + TMC Compensation

## 8.4 Alternative Compensation Strategies

The Ovation e-Amp compensation schemes use Miller, TMC and loop gain reduction (through VAS loading) for loop gain bandwidth spreading and some combinations of these. There are alternative strategies which offer increased slew rates. The e-Amp standard MC slew rate is in the region of 155 V/ $\mu$ s. Dispensing with Cdom MC and using MIC would allow this to be dramatically increased<sup>22</sup>. With MIC, Cdom is returned not to the VAS stage input, but to the amplifier inverting input, enclosing the input and VAS stages at HF and then enclosing the output stage in a separate, global feedback loop via the normal feedback resistor network. Since the Cdom plus input stage  $gm$  integrator structure essential to conventional MC is removed, this breaks the  $it=CV$  slew rate limit (i.e. they are '*non-slewing*'), and using this approach, Cordell's mosfet amplifier from the early eighties featured a SR of c. 300 V/ $\mu$ s. Similarly, John Curl's HCA-3500 featuring an all JFET complimentary input stage also used MIC to achieve very high SR's. MIC usually requires some additional compensation of the input stages – typically an RC network across the LTP collector load resistors or mirror, or VAS shunt loading to ground – to ensure stability of the front end stage plus VAS loop.

Still other MC strategies include the (pre) driver stage in the main Cdom loop. I experimented with these approaches and on the simulator, was easily able to achieve single digit ppm distortion levels at full power, but in practice stability was a big issue. On one of the Ovation e-Amp prototypes, I included the pre-drivers in the feedback loop, and got HF burst oscillation between 5 and 8 MHz. The only cure was an additional frequency transition compensation network, and I decided for reasons of practicality, to draw a line in the sand and abandoned the idea. That said, by virtue of the fact that you are able to put

<sup>22</sup> See Cordell 'Designing Audio Power Amplifiers' Chapter 9 and E. Stuart et al at diyAudio.com for some in depth examples of these techniques

about 15 dB more feedback around the output stage at HF, TMC does a really excellent job of reducing overall amplifier distortion without any stability issues.

## 8.5 Output Inductor and Zobel Network

When an amplifier (and this includes op-amps and discrete small signal amplifiers as well by the way) drives a capacitive load, *high frequency poles* in the output stage devices that lie above the unity gain cross over frequency (and therefore have gains of <1) move downward in frequency, such that these poles then end up with gains of > unity. The additional phase shift therefore taking place before the unity gain cross over frequency, leads to instability or oscillation. Output inductors to ensure *unconditional stability* on modern amplifiers are in the region of 0.5 to 1  $\mu\text{H}$ , this lower range of inductance values primarily as a result of fast, high  $F_t$  output devices<sup>23</sup> and a better understanding of compensation in the general amplifier design community. Output inductors in the region of 0.5 to 1  $\mu\text{H}$  have little sonic effect in the audio band or on the damping factor because at higher frequencies, the speaker cable and cross-over network inductances dominate (straight cable inductance is  $\sim 1 \mu\text{H}$  per meter). On a typical audio installation, cabling inductances are as much as  $3 \sim 5 \mu\text{H}$ , and the speaker and cross over network inductances will be many times this value ( $2 \sim 4 \text{ mH}$ ), but they are also damped by the speaker coil resistance. Cable, crossover and speaker capacitances can range from a few tens of nF, all the way up to  $1 \sim 2 \mu\text{F}$  for an electrostatic speaker load.

It is quite possible to configure amplifiers to exclude the output inductors, and there are a number of designers of commercial equipment that have taken this approach – for example John Curl (Parasound) and Charles Hansen (Ayre). For this to work reliably, the gain and phase margins have to be sufficient under worst case conditions, or, as in the case of Ayre, the amplifier has to run with zero global feedback. In a feedback design, this might typically entail running at lower loop gains, using high(er) speed output devices like the ones used in the Ovation e-Amp, with a small amount of lead compensation (which can add another 6 dB or more of gain margin if appropriately sized). The e-Amp includes an output inductor of  $1 \mu\text{H}$ . Along with the generous gain and phase margins, this makes the e-Amp an unconditionally stable design – it will therefore drive any capacitive load up to  $2 \mu\text{F}$  in parallel with any resistive load of  $2 \Omega$  and higher. The additional gain and phase margin afforded by the output inductor can also be traded for about 6 dB more loop gain, which of course can bring distortion reduction benefits if you choose to do this, but my earlier comments in this regard should be noted. As mentioned before, it is better to err on the side of caution with regard to compensation, and concede some distortion performance in the interests of absolute stability.

A Zobel network<sup>24</sup> – R9 and C19 - is connected between the output rail and the filter capacitor 0 V junction. The Zobel network connected before the output inductor presents decreasing impedance as frequency increases, and therefore partially cancels the inductive load impedance increase of the speaker and associated cable. The net result is that the amplifier load looks essentially resistive. This improves stability and amplifier settling time. Some designs take the Zobel from the speaker side of the inductor, where it can compensate for increasing speaker and cabling impedance at higher frequencies,

<sup>23</sup> The MJL1302/1381 have an  $F_t$  of 30MHz, while the legacy MJ802/4502 had an  $F_t$  of just 2Mhz.

<sup>24</sup> Also called a Beaucherot Cell

while I have also seen designs with Zobel networks both before and after the output inductor. To re-iterate the point made earlier, it is important that the Zobel network ground is returned separately to the main filter capacitors 0 V junction directly and *not* simply tacked onto the local PCB ground return - this to avoid injecting high frequency currents into the local ground which would then couple up onto the supply rails and into the front end small signal chain, causing distortion and possible instability.

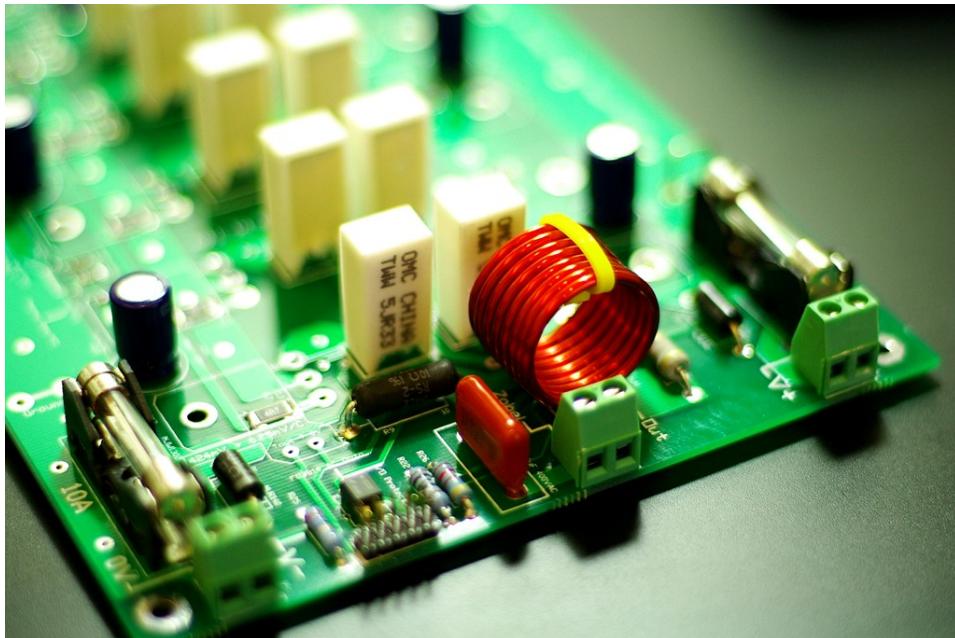


Photo 10 - Output Coil. Wire Diameter is 2 mm



Photo 11 - WBT Style Speaker Connectors

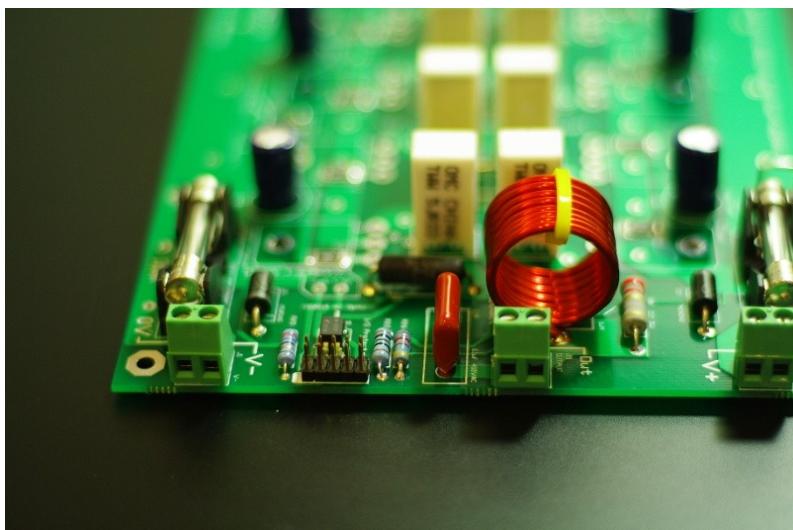
## 9. Protection

Amplifier protection is provided by separate board based on an 8 bit NXP 89LPC922 MCU (U12 in Fig. 19) and associated circuitry. This covers heatsink over temperature sensing and shutdown, speaker mute, transformer inrush current limiting, output short circuit and DC offset detection and shutdown, and ON/OFF control via a push button switch. Each amplifier board is connected to the controller board via a 10 way IDC ribbon cable (J3 and J4), while a 3<sup>rd</sup> ribbon cable (J2) connects to the front panel LED's (Power which is green and Error which is red) and pushbutton switch.

The speaker connections come in via J1 and J8 – note that pin 1 has to be connected to the amplifier output while pin 2 has to go to the speaker HOT side because the amplifier DC detect is taken off pin 1. The speaker muting function is implemented using a solid-state loudspeaker relay (SSLR) with two off back-to-back connected 150 V TO220 Trench FET technology devices (Q1 through Q4) from Fairchild (part # FDP083N15A). These feature a typical R<sub>ds(on)</sub> of around six mΩ, for a total relay end-to-end resistance of less than 15 mΩ. These devices can handle peak currents when ON of c. 100 A. The mosfets are driven by parallel connected photo-couplers (U6, U7, U9 and U13), which improves the switching speed significantly and this is done in order to keep within the mosfet switch devices SOA – even so, the 1 ms current capability at 70 V is still around 6 A, while the 100 μs capability is 100 A. Therefore, if you switch them quickly at under 100 μs, these devices can make or break enormous load currents. Further, the R<sub>ds(on)</sub> changes little with currents below about 50 A when the devices are turned on hard (so V<sub>gs</sub> is 10 to 12 V) and this translates into very low distortion which I sim'd at about 1 ppm, and AP measurements taken by other designers using a similar topology confirmed these figures. The total end to end SSLR resistance is significantly lower than any readily available electromechanical relay, and the SSLR solution can take some serious abuse – for example like cleanly switching fault currents as high as 40 A in <200 μs in this specific design (for an even faster, but non-isolated SSLR design, see [Solid-State-Loudspeaker-Relay-V1.0.pdf](#)). Further, since there is no contact wear out mechanism there are no long term reliability issues to contend with. Provided the operating envelope remains within the maximum thermal and electrical specifications of the mosfets, these devices can switch these huge fault loads day in and day out, year after year. There are no relays with equal or lower contact resistance that can do that at reasonable cost or similar speed.

The LIVE mains feed to the main power transformer is taken via J7. For power ON/OFF and in-rush (or 'soft start') current limiting, standard 16 A Tyco relays are used - unlike the speaker muting function described above, this is where a relay solution is a good fit - and this prevents mains switch-on voltage dips (and mains ECB trips) by limiting the transformer magnetizing in-rush current, as well as limiting the smoothing capacitor initial charge-up currents. U8 and associated circuit handles Power ON/OFF, while U10 takes care of the inrush current (the soft start time is set to about 5 seconds), which is limited by 3 x 7 W 47 Ω resistors in parallel (R19 through R21). Without soft start current limiting, the peak currents through the rectifier and associated wiring can be as high as 250 A and take up to 5 to 10 mains cycles before settling at the normal running peak currents which are in the region of 20 to 30 A in this design.

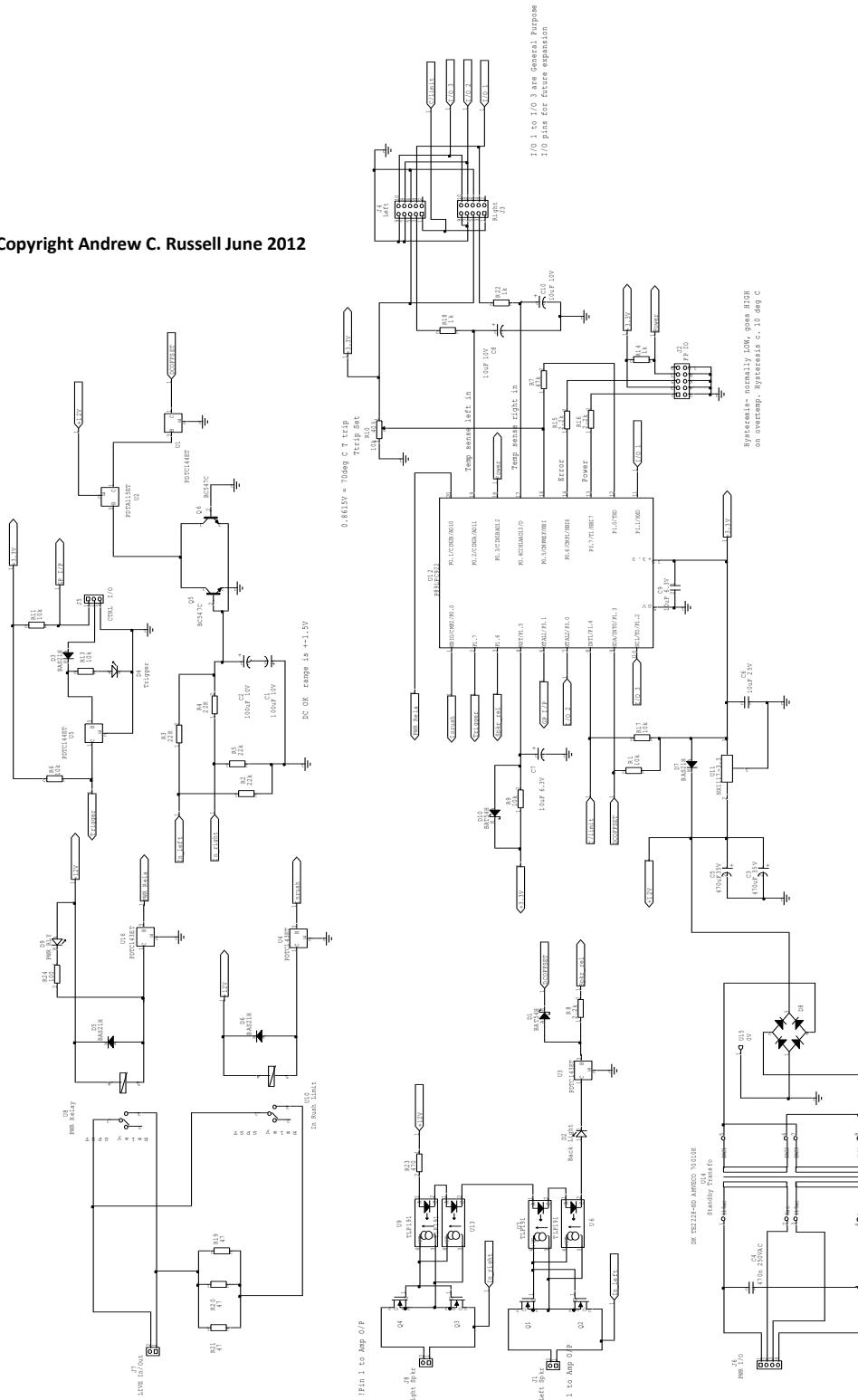
Heatsink temperature sensing is accomplished with SMD mount LM60 temperature sensors which are located near the collector lead of one of the output devices on each amplifier board and thermally coupled using some silicon grease. The sensor outputs feed into the control board via J3 and J4 pin 3, with pin 5 providing the necessary 3.3 V to power them up. The trip temperature is set to 70 °C by adjusting VR1 on the protection board for a reading of 0.8615 V on pin 14 of the MCU (comparator external reference input). The sensors feed into the comparator inputs pins 19 and 17 on the MCU. 6 °C hysteresis is provided by turning open drain port P1.0 LOW, which in turn pulls the comparator reference down by c. 45 mV via R7. Note that both the temperature sensors and the over current detect opto-isolator circuits on the amplifier boards are completely floating in order to prevent ground loops or any possible noise problems.



**Photo 12 - Connector to Current Sense and Temp Sensor**

Output DC fault detection (circa  $\pm 1$  V) uses a standard low pass signal averaging filter (R2 through R5 and C1 and C2) feeding a two transistor DC detect circuit (Q5 and Q6) which is buffered, inverted (U2 and U1 RET devices) and directly drives the SSLR driver RET transistor U3 OFF via D1. The DC Offset signal from U1 also feeds into the MCU INTO (level triggered) input on port P1.2. This direct drive configuration from the output of U1 to the SSLR driver transistor U3 provides some fail safety in the event of an MCU hang-up ensuring that on a serious DC fault condition the SSLR is turned off directly with the MCU effectively bypassed. The MCU job is then to latch the SSLR OFF and monitor the amplifier output to see if the DC offset condition abates after which it will turn the amplifier output back on again subsequent to doing a few further housekeeping checks. However, the DC detect circuit always takes priority over the MCU for this fault condition, since what we ultimately want to do is provide the highest level of protection to the loudspeakers. The response time from detection of a gross DC fault in which the speaker is shorted to one of the 68 V rails to the SSLR turning OFF is under 8 ms and dominated the filter RC time constant. During a DC fault condition, the red Error LED flashes at about 1 Hz.

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**Figure 19 - Amplifier Protection board**

Output stage over current is detected with an opto-isolator connected across a pair of emitter degeneration resistors on the amplifier board. The opto open collector output comes in from each amplifier board on pin 1 of J3 and J4, where they are wire or'd and connected to INT1 (also set for level triggering) of the MCU with R17 providing the pull up current. In the case of over current detection due to a short circuit on the output, the amplifier output is immediately disconnected from the speaker via the speaker relay and powered down. The response time to a hard short circuit, detect to SSLR OFF condition is under 50 uS. The red Error LED will remain illuminated (no flashing), indicating a fault condition in the speaker wiring. The amplifier has to be unplugged from the wall socket and powered up again. If the fault is still present when the SSLR turns on, it will simply go into shutdown, and the above cycle will repeat again.

A Trigger input (active HIGH: 0 V = OFF and +12 V = ON) is provided through J5 pin 2 and U5. During each watchdog service cycle, the trigger input on the MCU (P1.7) is checked, and if changed from the previous status, the amplifier power status is updated accordingly. The system is set up such that it is always the latest change of state on either the Trigger input or the front panel ON/OFF pushbutton that is actioned. I ended up not providing a trigger input on the e-Amp – however, the option to add it is always there.

Three general-purpose I/O lines are provided, P1.1, P1.2 and P3.0, along with a GP active low input via J5 pin 1 into P3.1. These are intended to provide additional features for future high power audio projects and for the e-Amp project are simply grounded on the amplifier module side through the ribbon cables

All of the protection functions are interrupt driven, such that once a task is completed, the MCU goes into sleep mode with the clock halted to minimize any EMI generation, waking up again as soon as an interrupt condition is detected. The internal 1 second MCU watchdog ensures that if a software latch-up occurs, a reset is generated and the amplifier automatically powers OFF. The code was written in C (Keil) and when compiled, requiring about 1 Kbyte of memory. The protection board is powered up whenever the amplifier is plugged into the wall socket, and the rear panel IEC socket mains switch is ON. When in the standby condition (so, amplifier turned off), the power consumption is around 300 mW. Mains to the control board is fed in via J6, where there is provision for wiring up for 110 or 220 VAC.

Finally, in terms of general safety and damage minimization under a worst case fault condition (e.g. MCU board fail and both N and P dives fail short circuit), a last stop protection mechanism is provided by the 10 A rail fuses on the amplifier boards. On the mains side, a switched 3 pin IEC socket is used which includes an integral 5 A 5x20 fuse and this provides fire hazard safety in the case of a mains fault inside the amplifier.

## 10. Final Thoughts

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Douglas Self and Robert Cordell's books, and some lively interaction on a number of DIY audio forums (particularly [diyaudio.com](http://diyaudio.com)), have improved the understanding of key amplifier distortion mechanisms and how to mitigate them. At 150 W RMS into 8 Ω at 20 kHz and using TMC, the e-Amp targets less than 10 ppm distortion, and using standard MC, around 40 ppm. These are good performance figures (both MC and TMC), and they are achieved with moderate amounts of feedback – loop gain at 20 kHz with WBF-TMC is 46 dB and is essentially flat from LF through to about 40 kHz, while on MC its around 36 dB at 20 kHz. Certainly the use of modeling (LTSpice) with a fair amount of iterative fine tuning and the focus on the linearity performance of each of the main stages (LTP, VAS and output stage) also played an important role in attaining the e-Amp's performance. The performance of the Ovation e-Amp is better than the Ovation 250 (standard MC and TMC). I put this down to better optimization of the output stage design, VAS + pre-driver and fine-tuning of the front end LTP stages, where I made better tradeoff's between LTP degeneration, Cdom and the input filter cut-off frequency.

The e-Amp design is slightly less complex than the Ovation 250 that preceded it by about 4 years. In that design, I made a different set of tradeoffs, but in the e-Amp, the tradeoffs viz-a-viz complexity and performance are better nuanced, and this simply comes through gaining experience and confidence in a particular topology – in this case FBS.

Compared to the Ovation 250, the SOA protection is gone, that I now believe was overly aggressive (careful listening tests with it enabled and disabled convinced me of this), replaced with simple, fast current limiting and an oversized output stage for the stated 180 W RMS 8 Ω power rating; the separate high voltage, Zener regulated supply to the front end in the Ovation 250 added complexity for sonic benefits and marginal power increases that were questionable. The Ovation e-Amp design focuses more successfully than the Ovation 250 on the key design aspects that determine measured and sonic performance. In my view these are open loop linearity, PCB and wiring layout, and compensation design. If you do not get these close to 100% right in an amplifier design, you cannot get good performance no matter what else you do. During the work on the e-Amp, I was also more attuned to some of the possible component selection issues that are discussed in the books I have mentioned above, but also highlighted other well known practitioners in the field.

Greater effort was put into the power supply and PCB layout on the Ovation e-Amp. The capacitor filter bank was carefully laid out to keep capacitor charging currents separate from amplifier supply lines (I use a double sided PCB). Further, the use of a ripple eater filter stage is both simple and very effective in removing ripple noise and program material harmonics from the front-end power rails – something that is a significant issue in all class AB designs. On the PCB, the decoupling capacitor ground returns have been split between the + and – rails, and run separately back to the star ground point.

I retained the EF3 output topology, but used very much faster 30 MHz Ft output devices (NJW1302/3281) and therefore spent some effort (testing and adjusting values to determine the range

of effectiveness) on the optimization of the stopper networks. In the Ovation 250 I used slow MJE21192/21194 devices and a simple L-pad between the pre-driver emitters and the driver bases was sufficient. In the Ovation e-Amp I have settled for a damper ( $27\ \Omega$  and  $1\ nF$ ) in the driver base circuit, and then enhanced rail decoupling between the pre-driver and driver circuits.

The VAS and pre-driver stages run at lower currents than the Ovation 250. In that design, I ended up with a VAS standing current of about 32 mA and the pre-driver stage at around 28 mA. The e-Amp VAS runs at 15 mA and the pre-driver stage at 20 mA, while the driver stage current has been reduced from over 90 mA to 38 mA. The e-Amp pre-driver and driver stages are therefore equipped to potentially deliver over 800 W (i.e. much higher than the amplifier rating) and still remain in class A.

A lot of experimental effort went into optimizing the thermal compensation. In EFTs, time lags are the designers enemy with regard to bias stability (and, by implication, less than optimum output stage bias and higher short term distortion), and the use of an NTC to augment the Vbe spreader along with two point compensation during the design phase play a key role in the measured bias stability.

The recent popularization of TMC have meant it has now entered the audio design mainstream as judged by the chatter about the subject on the net. The Ovation 250 was modified in July 2011 for TMC and has proven very stable. Importantly, I have not been able to detect any deleterious effects on the sound. The potential to reduce distortion dramatically at HF without the requirement to increase overall loop gain is one of the reasons I like this compensation scheme – it makes much more effective use of the available loop gain than competing compensation techniques. Allowing the compensation scheme to be jumper selectable between MC and TMC on the Ovation e-Amp leaves plenty of room for long term listening experiments. I may end up selecting one over the other – only time will tell. I hope at a later date to be able to document my findings and share them with you on [www.hifisonix.com](http://www.hifisonix.com).



**A**

Amplifier protection · 50  
 Amveco · 12  
 AP distortion analyzer · 29  
 Avel-Lindberg · 12  
 Ayre · 21, 48

**B**

balanced differential input · 5  
 Bart Locanthi · 20, 26, 35  
 base stopper · 6, 34  
 bias spreader · 37  
 bipolar · 34, 35  
 Bode · 42  
 Bode analysis · 42

**C**

capacitive load · 7  
 capacitively coupled · 5, 22  
 cascode · 21, 28, 30, 31  
 Cdom · 5, 9, 23, 24, 25, 26, 28, 30, 43, 45, 47, 54  
 CFP · 9, 20, 35, 37  
 Charles Hansen · 21, 48  
 chassis · 16  
 class A · 6, 35  
 class AB · 35, 38, 54  
 CMCL · 28  
 Cob · 6, 9, 27, 31  
 Colpitt's oscillator structure · 35  
 common emitter stage · 19  
 common mode current loop · 28  
 compensation · 6, 34, 48  
 contact wear out mechanism · 50  
 cross over discontinuities · 34  
 cross-over network · 48  
 current source · 5, 27, 28, 37  
 Cyril Bateman · 7

**D**

damping factor · 48  
 Damping Factor

damping factor · 4  
 Darlington · 35  
 DC offset detection · 50  
 degeneration · 22  
 device temperature · 38  
 Digikey · 9  
 dissipation · 6, 34  
 distortion · 4, 5, 6, 7, 25, 28, 29, 30, 31, 34, 38, 49  
 Distortion  
     distortion · 34  
 Douglas Self · 7, 19, 37  
 driver stage · 6

**E**

Early effect · 31  
 earth · 16  
 Edmond Stuart · 28, 34, 45  
 electrolytic · 9  
 electrolytic feedback network coupling cap · 21  
 emitter degeneration · 5, 31, 34  
 EOL · 22  
 error correction · 20  
 ESL · 7  
 ESR · 7

**F**

FBS · 19, 28  
 feedback · 5, 6, 7, 9, 19, 30, 34  
 feedback network capacitive coupling · 29  
 filter capacitors · 11, 49  
 fire hazard safety · 53  
 flyback diodes · 6  
 folded cascode · 20, 30  
 Frequency response · 4  
 Front End Design · 20  
 ft · 48  
 fully balanced · 5  
 Fully Balanced Symmetrical · 19

**G**

Global Feedback · 42  
 gm · 22, 25, 46  
 ground · 7, 16, 49

---

**H**

harmonics · 54  
 Hawksford · 30, 31, 34  
 HC Lin · 19  
 heatsink · 9, 16  
 heatsink over temperature sensing · 50  
 Heatsink temperature sensing · 51  
 HEC as applied to bipolar output stages · 39  
 HF decoupling · 9  
 Hfe · 22  
 Hitachi · 20  
 Hybrid Wide Band Feedback' · 46

---

Michael Tian · 44  
 Miller · 3, 5, 26, 30, 31, 42, 43, 45, 47  
 Miller compensation · 3  
 Miller Inclusive Compensation · 42, 47  
 Miller Inclusive Compensation, or MIC · 42  
 MJ802  
     MJ4502 · 48  
 MJL1302 · 6, 35, 48  
 MJL1381 · 6, 35  
 Modushop · 9  
 mosfet · 20, 34  
 mosfets  
     lateral and vertical · 34  
 Mouser · 9, 12

---

**I**

Idss · 21  
 IEC socket · 16  
 inductive dump · 6  
 inductive dump currents · 6  
 Input Impedance · 4  
 in-rush · 50  
 interrupt driven · 53

---

**J**

JFET · 20, 22, 47  
 John Curl · 21, 48

---

**L**

Leach · 19, 23, 26  
 lead and trace inductances · 36  
 Lin · 19, 28, 37  
 LM60 temperature sensors · 51  
 Locanthy · 20  
 Locanthy T · 35  
 long tailed pair · 5  
*loop gain and phase* · 44  
 loop gain · 24, 28, 30, 31  
 low TCR · 9  
 LTP · 5, 19, 20, 24, 26, 27, 28, 29, 30

---

**M**

Marshal Leach · 19  
 MCU watchdog · 53  
 MIC · 47

---

**N**

Nelson Pass · 21  
 NJL1302 · 38  
 NJL1381 · 38  
**noise** · 5, 9, 12, 27  
 noise filtering · 5  
 non-linearity · 5, 34  
*non-slewing* · 47  
 NOS · 22  
 NTC · 55  
 NTD · 38

---

**O**

open loop gain · 31  
 Output DC fault detection · 51  
 Output Device Protection · 37  
 Output Devices · 33, 34  
 Output Drive Capability · 4  
 Output inductors  
     output inductors · 48  
 Output Power · 4  
 output rail · 6, 7, 48  
 output shortcircuit · 50  
 Output stage over current · 53  
 Ovation  
     Ovation 250 · 37, 46, 54  
 Ovation 250 · 9, 20, 23, 54, 55  
 Ovidiu Popa · 28, 34

---

**P**

Panasonic · 9

---

parasitic oscillation · 6, 35

parasitics · 35

Parasound · 21, 48

PCB · 16, 20, 38, 49

**Phase Inter-Modulation**

distortion · 42

**Phase Margin**

Gain Margin · 4

PIM ·

polyester · 9

pre-drivers · 6, 35, 38, 47

Pretty Good Poweramp' or PGP · 34

soft start' · 50

software latch · 53

solid state loudspeaker relay (SSLR) · 50

speaker cable · 48

speaker mute · 50

speaker muting function · 50

Spice · 35

*stability* · 48

stacked foil · 7, 9

standing current · 6, 37

Stereophile · 23

stopper networks · 36

sustained beta · 6

## Q

Quad slope VI Limiting · 4

## R

rail fuses · 53

RCA connectors · 16

*Rdegen* · 43

resistive load LTP · 29

RFI · 21, 22

RFI burst noise · 11

RFI ingress · 22

ripple eater · 7, 33, 54

Rise/Fall time

fall time · 4

Robert Cordell · 20, 34, 42

Rod Elliot · 16

## S

Safe Operating Area · 6

screened cable · 16

Self · 19, 29, 34, 42, 54

servo · 19, 28

shunt impedance · 6

Single Point Thermal Compensation · 39

Slew rate · 43

Slew Rate · 4

Small Signal Analog Design · 29

small signal stages · 20

SMD · 9, 38

snubber · 11

snubbers · 11

SOA · 6

**SOA protection** · 37

## T

tail current · 5, 21, 22, 23, 24, 26, 28, 29, 43

temperature · 6, 38

temperature compensation · 6, 38

temperature drift · 22

Thermal Compensation · 37

threshold voltage · 35

TIM · 23, 25

TMC · 3, 4, 5, 39, 45, 46, 47, 48, 54, 55

Topology · 19

transformer · 3, 4, 12

transformer inrush current limiting · 50

transformer magnetizing current · 50

Transitional Miller Compensation · 3, 45

TMC · 3

Trench FET technology · 50

Trigger input · 53

trip temperature · 51

triple · 20, 34, 35, 38, 39

two point temperature · 38

Two Point Thermal Compensation · 41

## U

UGBW · 43, 44, 45

## V

vapour ware · 22

VAS · 5, 6, 19, 24, 29, 30, 31, 34, 35, 37

local loop gain · 30

Vbe multiplier · 6, 31, 37

**Vbe Multiplier** · 37

Vgs · 21

Vishay · 9  
Voltage Amplification Stage · 5  
voltage feedback · 42

---

**W**

WBF+TMC · 46  
wideband hash · 33  
wiring layout · 54

---

**Z**

zener reference diode · 5  
Zero Global Feedback · 42  
Zobel · 7, 48

## Notes

---

### Ovation e-Amp Document History

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June 6 2012	Initial Release
June 11 2012	Corrected with minor updates and clarifications to page 39 and 45; JFET Offset levels clarified on page 22 footnote; Corrected Ovation PSU assembly weight; June 11 2012 added copyright notices to circuits and corrected grammatical errors
July 5th 2012	Corrections to SI units usage, spelling and grammar. My thanks to Dr. Harry Dymond for his feedback on the document