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AN-394
APPLICATION NOTE

An Outboard Digital-to-Analog Converter for Digital Audio Sources

by Hank Zumbahlen

INTRODUCTION

This application note describes an AES/EBU receiver and outboard digital-to-analog converter (DAC) for use with digital audio sources. Due to the use of the AD1891 Asynchronous Sample Rate Converter (ASRC), which is at the heart of the design, the sample rate of the input signal can vary from 24 kSPS to 48 kSPS. The interpolation filter is implemented using the ADSP-2115 Digital Signal Processor (DSP). Great care has also been taken in the design of the analog section and power supplies. The block diagram of the complete system is shown in Figure 1.

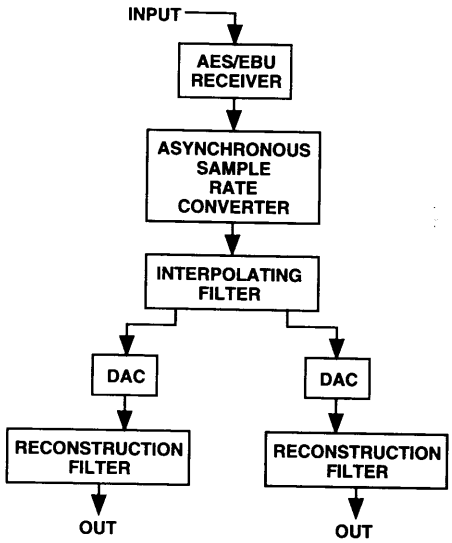


Figure 1. Block Diagram

BACKGROUND

As the performance level of CD players has improved over the years, we have seen the separation of the transport and the conversion functions into two physically separate units. Separate DAC converters first appeared as performance enhancements to commercial CD players, the idea being that the analog section in most CD player designs were limited in some manner, usually by cost constraints. The external DAC would also free from the power supply modulation resulting from the electromechanical demands of the positioning systems on the power supply in the CD or DAT transport.

The use of the AD1891 ASRC chip in this design yields several benefits. First, it allows the optimization of the reconstruction filter. Since the sample rate of the output is fixed, regardless of the sample rate of the input, the reconstruction filter design need not accommodate a range of output sample rates. Secondly, the sample rate conversion process reduces the jitter on the digital signals applied to the D/A converter chip.

This outboard DAC is implemented on three boards. The first board contains the digital functions, which include the AES receiver and the interpolation filter. The second board contains the analog functions, the D/A converter chip, reconstruction filters and balanced output drivers. The power supply occupies the third board. By separating the analog function from the digital function, we effectively isolate the analog ground from the digital ground, reducing coupled noise.

THE DIGITAL BOARD

The AES/EBU Receiver

The first section of the outboard DAC converter is the AES/EBU (Audio Engineering Society/ European Broadcast Union) receiver. The AES/EBU interface has been adopted as the standard interface linking the digital inputs and outputs of audio components.

The AES/EBU interface is primarily intended for professional applications. A very similar standard is the S/P DIF (Sony/Philips Digital Interface Format) which is primarily intended for consumer applications. There are some small differences in the channel status bits, but the main difference is that the AES/EBU interface is balanced (RS-422 compatible) and the S/P DIF is single ended. Impedance levels and signal amplitudes are also different.

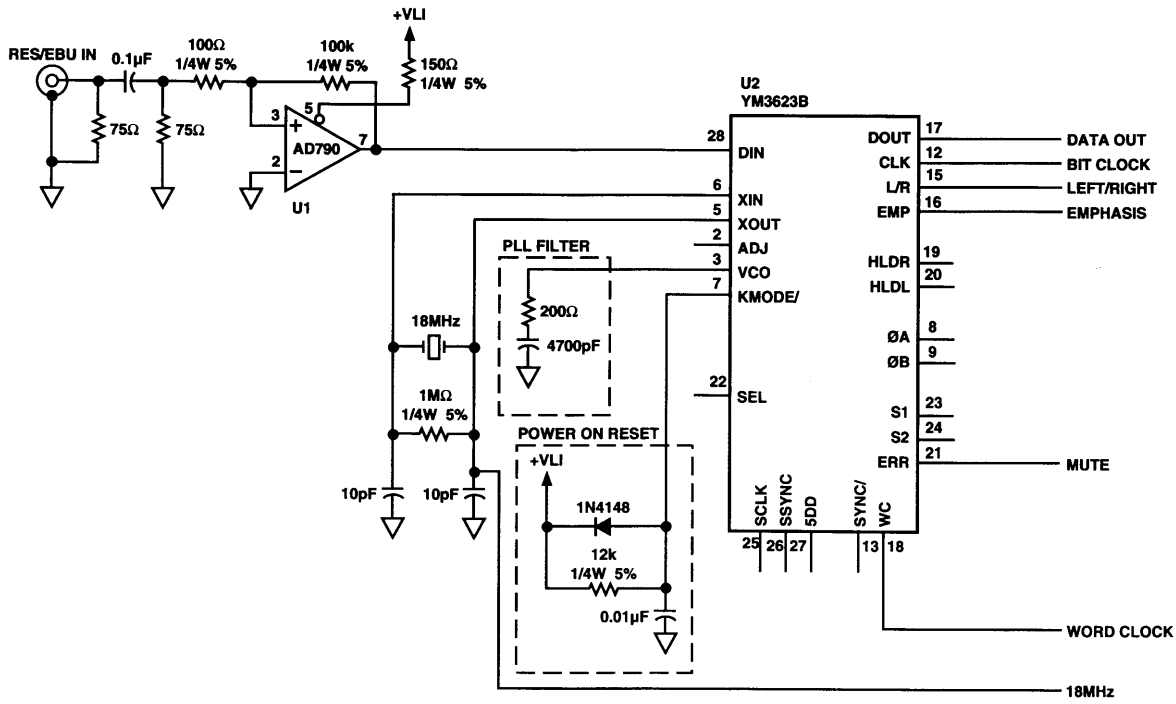


Figure 2.

The standard digital audio format consists of four signals. They are the output data, which alternates between left and right channels, a bit clock, a left/right channel identification signal and a word sync (frame sync) signal. For convenience of transmission, these four signals are encoded into one composite signal and the composite signal is transmitted asynchronously down a single wire or optical conductor. The receiver takes this composite signal and through the use of a phase lock loop (PLL) separates the four signals back out.

It is this reconstruction of the clock signal in the PLL that is one source of jitter in the recovered signal. Jitter of the word clock is a source of one form of sonic degradation. Simply stated: the correct signal at the wrong time is the wrong signal. Jitter can cause spurious tones by mixing in a nonlinear fashion with the sample rate which could produce tones in the audio band. This is a form of intermodulation distortion (IMD). Much discussion has taken place on the audibility of jitter.[1, 2, 3, 4]

The receiver is implemented in a single LSI chip (U2 of Figure 2). The main function of this chip is to implement the PLL for clock and data recovery. It also strips off the header information and provides a mute signal if an error is detected. A crystal oscillator provides a signal for the PLL to lock onto in the absence of an input.

A preamplifier function is provided to amplify the input signal to the TTL levels required by the receiver chip. This function is implemented with a comparator (U1 of Figure 2) rather than the usual CMOS gate as an attempt to minimize the jitter of the signal.

ASYNCHRONOUS SAMPLE RATE CONVERSION

The next section of the design is the block made up of the AD1891 Asynchronous Sample Rate Converter (ASRC). This block serves two major purposes: it provides for sample rate conversion and also de-jitters the output. The AD1891 was chosen over the AD1890 because we assume that the input data word is a fixed 16-bit length and the sample rate would not be variable short term. The AD1890 allows for variable length and variable rate.

There are several standard sample rates in the audio world. The most common is undoubtedly the 44.1 kHz sample rate used by the Compact Disk (CD). Other standards include 48 kHz used in Digital Audio Tape (DAT) and the 32 kHz used in film and direct digital satellite broadcast.

The output data rate in this design is set to 48 kHz. This allows a little more room for the transition band of the reconstruction filter. An output rate of 48 kHz allows an input range of 24 kHz to 48 kHz. If the input rate were to be over 48 kHz (the maximum allowable rate is 60 kHz), the AD1891 would adjust the bandwidth of the FIR filters downward to avoid aliasing effects.

The AD1891 takes the standard four signal set (data, bit and word clocks, and the L/$\overline{R}$ signal) from the AES/EBU receiver as its input. On the output side are a new bit clock, word clock and L/$\overline{R}$ signals that are generated by a crystal oscillator and a divider string. Note that there is no requirement for the input and output signals to have

any particular phase relationship. They are completely independent. This is also why the sample rate conversion process is said to be asynchronous. Note that the only output of the AD1891 is the data out, all other signals are inputs.

The process of sample rate conversion is most easily thought of as asynchronous resampling of the data. In this process the input data stream is interpolated to a very high sample rate. The data is then passed through a FIR filter to limit the bandwidth so that the resampling will not produce aliases. The data stream would then be resampled at the output data rate. By using a high effective interpolation rate (65,536) and a high number of taps and filter coefficients (approximately 4 million) insures that the distortion in the audio band is kept below the 16-bit level. A visual representation of this process is shown in Figure 3.

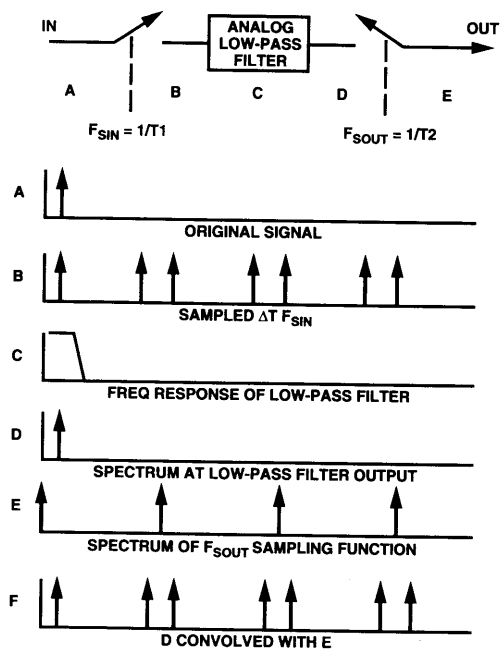


Figure 3. Two Samplers with Analog Filter

This model is an oversimplification. If we assume a 48 kSPS sample rate and a 65,536 times oversample rate, the required clock rate would be over 3 GHz, which is beyond the operating frequency of the DSP engine.

A more correct model (see Figure 4) is one of a bank of filters with uniform amplitude response and incrementally different group delays. Flat amplitude response with a fixed group delay is a characteristic of the all pass filter. Each filter has a different fixed delay. The larger the time difference between input and output samples the shorter the delay added by the filter used (see Figure 5). The group delay of each of these filters is uniform so that the resulting response has the desirable feature of linear phase across the audio band. There are the equivalent of 65,356 of these filters in the AD1891, each with nominally 64 taps for a total of approximately 4 Meg words of 22 bits of coefficients for the FIR filters. We can therefore model the ASRC as a digital filter where the filter coefficients change on a sample by sample basis. This lowers the required clock rate of the ASRC to the tens of MHz, which is much more practical.

For a more complete description of the polyphase model, please refer to the AD1890/AD1891 data sheet and the references in the bibliography.[5, 6, 7]

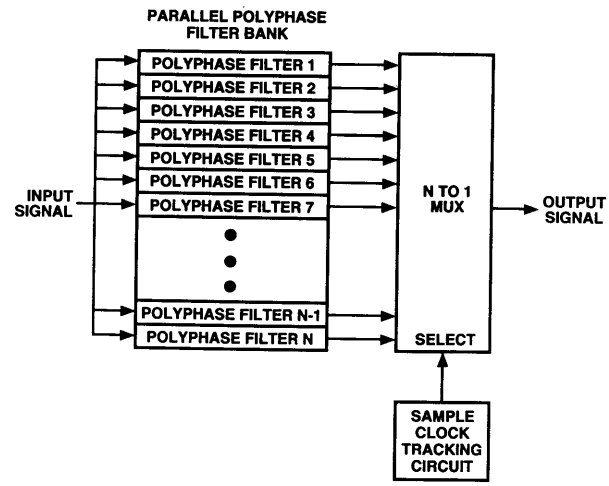


Figure 4. Polyphase Filter Bank Model–Conceptual Block Diagram

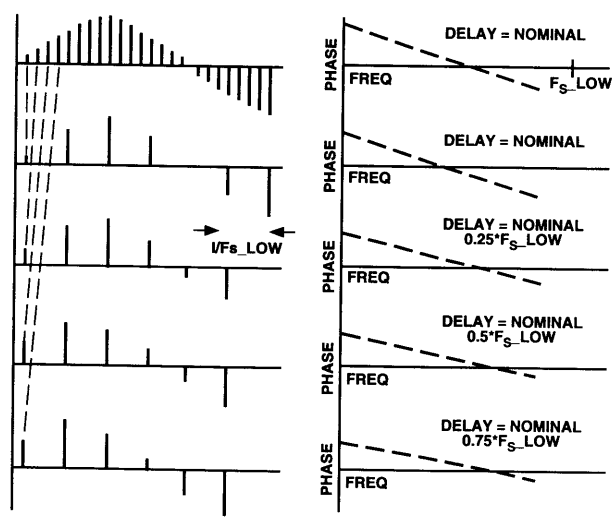


Figure 5. Subfilters Realigned with Coarse Time Grid

There is an unexpected side benefit from this process. Since the output data rate is determined by an external crystal oscillator, there is a very low jitter in the output clock. The jitter being only the inherent jitter of the oscillator and the jitter of the divider string, which will be almost nonexistent. Of course, to take advantage of this jitter reduction, care must be taken to minimize the amount of circuitry the clocks, especially the word clock, pass through. The word clock is most critical since it controls the updating of the D/A converter. There is also a digital servoing in the clock circuit that reduces jitter of the internal clock. This circuit determines the ratio between the input and output clocks and therefore the appropriate set of filter coefficients. The block diagram of the AD1890/AD1891 is shown if Figure 6.

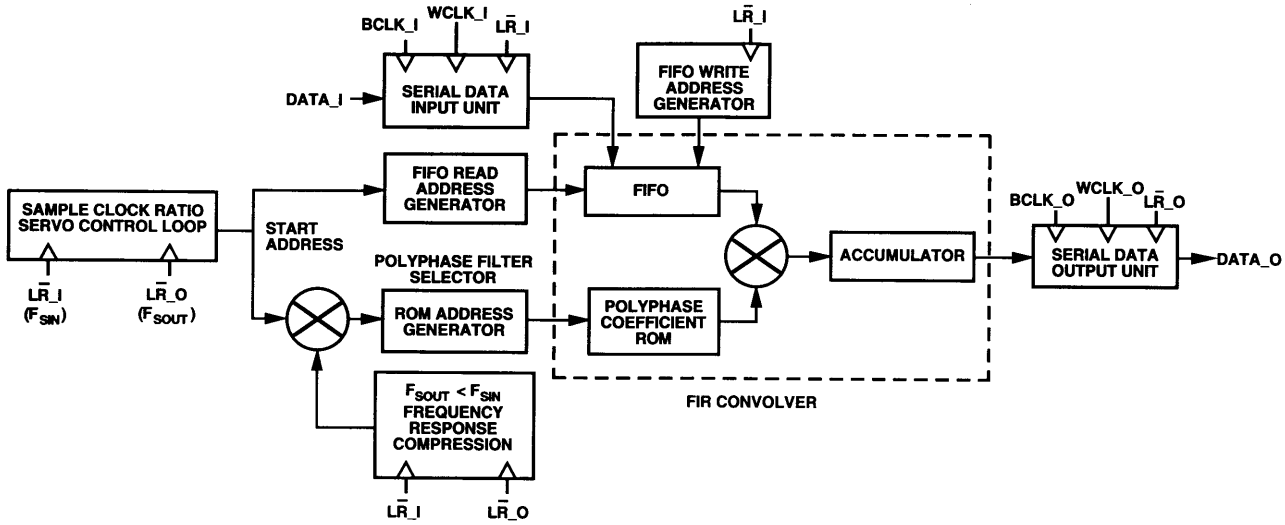


Figure 6. AD1890/AD1891 Functional Block Diagram

The audio performance of the AD1891 is consistent with high quality audio reproduction. The passband ripple of the polyphase filters is less than .01 dB. The transition band is 4.1 kHz at a 44.1 kHz sample rate. The stopband attenuation is greater than 110 dB. The dynamic range of the filter (referred to full scale using a –60 dB input) is 96 dB. The THD+N is a minimum of 96 dB below full scale (108 dB typical at 1 kHz). The amplitude of the distortion and noise components scale with input amplitude, being 20 dB down for an input signal that is 20 dB down. Typical performance is shown if Figures 7 through 9. The internal accumulator is 27 bits, which is important in maintaining the audio performance of the system.

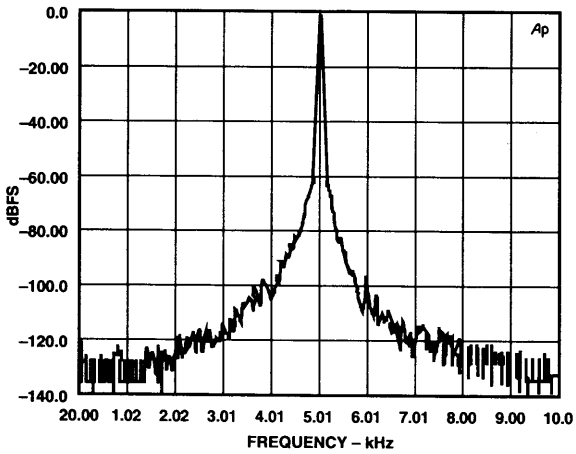


Figure 7. AD1890/AD1891–5 kHz Tone at 0 dB FS with 100 ns p-p Binomial Jitter on L/R̄ Clocks, Fast Settling Mode, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, 16 K-Point FFT, BH4 Window

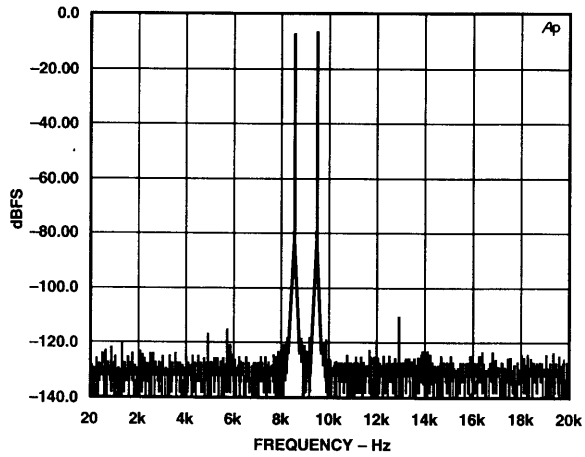


Figure 8. AD1891–Twintone, 10 kHz and 11 kHz, 44.1 kHz Input Sample Frequency, 48 kHz Output Sample Frequency, 16 K-Point FFT, BH4 Window

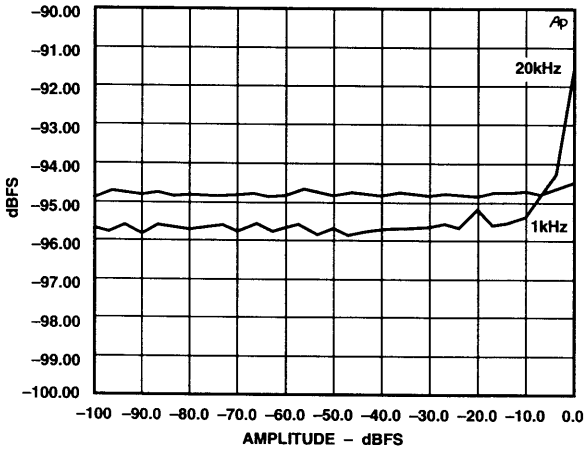


Figure 9. AD1891–THD+N vs. Input Amplitude, 44.1 kHz Input Sample Frequency, 48 kHz Output Sample Frequency, 1 kHz and 20 kHz Tones

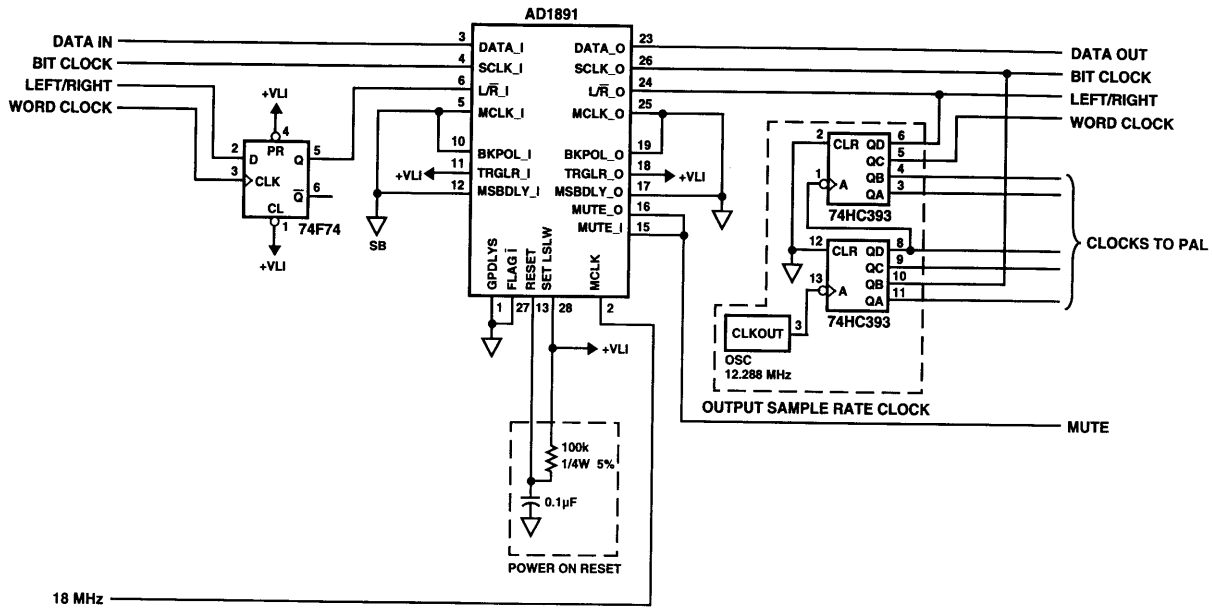


Figure 10. Asynchronous Sample Rate Converter

Even though the input data word length is 16 bits, the word length is 32 bit clocks, for a total of 64 bit times for the combined left and right channels. This allows for higher resolution data streams in the AES/EBU interface along with header information such as whether the emphasis is on or off and an indication of the sample rate. The interface between the AES/EBU receiver and the AD1891 is complicated slightly by the fact that the receiver right justifies the data and the AD1891 expects to see left justified data. To get around this, the word clock is used to delay the L/$\overline{R}$ signal. This delays the L/R signal by 1/4 of the word time which in effect left justifies the data. The schematic for the AD1891 block is shown in Figure 10.

INTERPOLATION FILTER

It has become accepted procedure in the design of CD players and DAT recorders to use interpolation, which is effectively oversampling the output data. The reason we would want to use oversampling is to increase the transition band and, in turn, reduce the required order, of the output reconstruction filters. There is the added benefit that through the averaging effects of the interpolation filter the resolution of the output can be increased. In this case we are going to a 20-bit, 4× oversampled system.

A 20 MHz ADSP-2115 digital signal processor is used as the DSP engine. A complete schematic is shown in Figure 11.

The primary purpose of the DSP engine is to provide the interpolation of the data word to the oversampling rate. It also provide the FIR (Finite Impulse Response) filtering function to band limit the resultant output to 20 kHz. The averaging of the data by the filter also allows us to increase the resolution of data stream. An FIR filter is used so that the filter can have a linear phase response. This means that the group delay is uniform across the audio band. This preserves the phase relationship of the audio signal components.

A 4× oversample rate was chosen as the highest practical rate. It is desirable to move the sample rate as far out in frequency as possible to reduce the requirements of the analog reconstruction filter. The upper limit is set by the number of instruction cycles between output samples at the 4× rate and the number of taps in the filter. The number of taps in the filter in turn determines the width of the transition band and the minimum stopband attenuation.

Several other features were incorporated into the digital filter.

First, we provide for digital dither. Dither is adding a low level random signal to the output word. This signal randomizes the roundoff error of the digital filter which produces as apparent improvement in low level linearity with a slight decrease in S/N ratio. Subjectively, the increased noise level is less objectionable than the harmonic distortion of the roundoff error and therefore is a reasonable tradeoff for the increased linearity.

A calibration signal is also provided to facilitate adjustment of the low level linearity trim of the AD1862 DAC. This signal is a low level sine wave which allows trimming the MSB transition of the AD1862. This also improves the low level linearity.

Another control line allows for polarity inversion of the signal. The audibility of absolute polarity is still widely discussed in the audio world. It is especially hard to prove or disprove since little source material is available that takes polarity into account. This function is provided for those instances where it is useful.

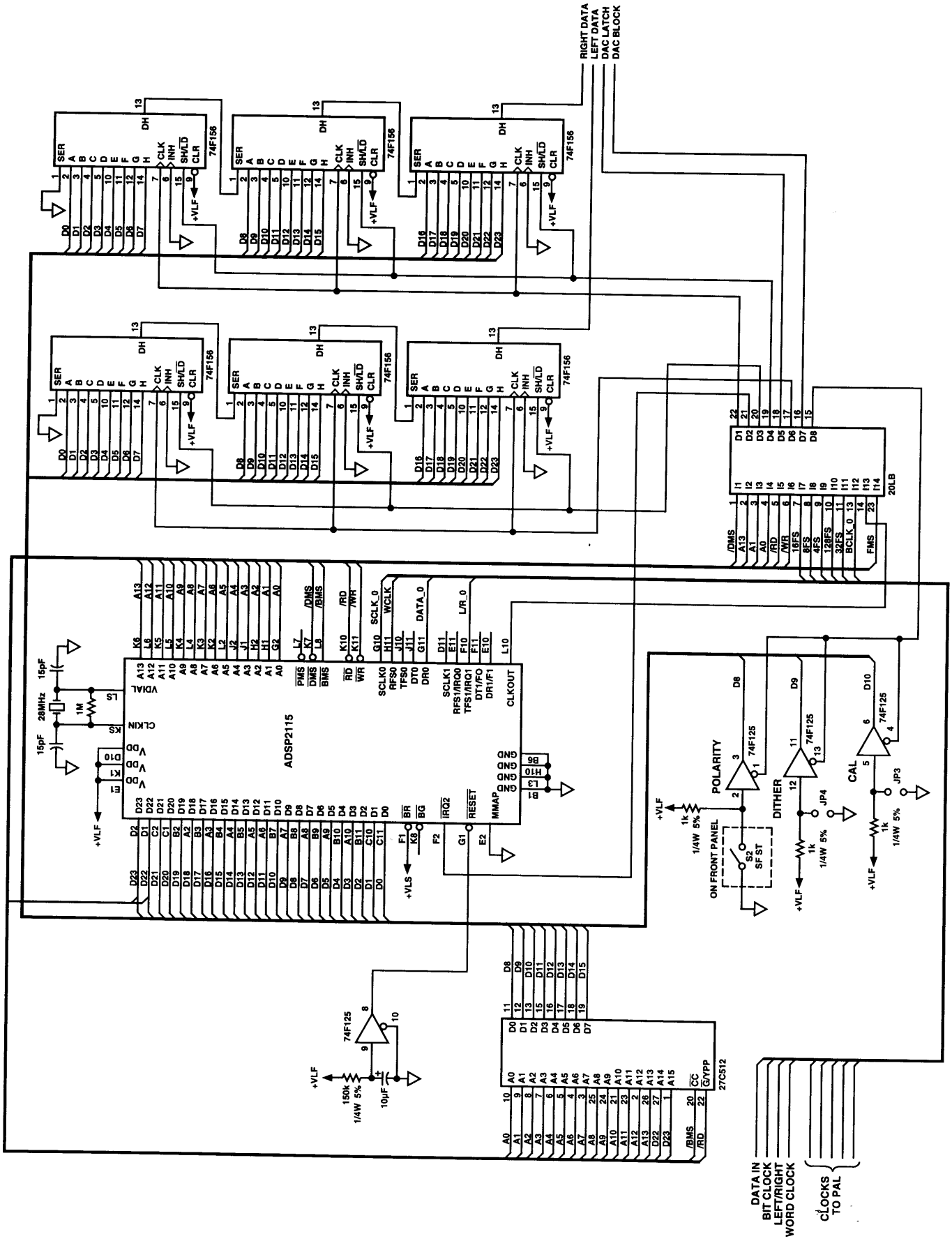

RIGHT DATA
LEFT DATA
DAC LATCH
DAC BLOCK
74F156
20LB
ADSP2115
28MHz
15pF
1M
+VLF
+VLS
74F125
POLARITY
DITHER
CAL
ON FRONT PANEL
S2
SF ST
JP3
JP4
1k
1/4W 5%
150k
10µF
27C512
DATA IN
BIT CLOCK
LEFT/RIGHT
WORD CLOCK
CLOCKS
TO PAL

Figure 11.

The output of the DSP chip connects to the D/A converters. The data out of the ADSP-2115 is parallel instead of serial due to bandwidth limitations of the serial port.

It is much easier for the DSP to work with word lengths that are binary numbers. Therefore, a 20 bit word will be rounded up to 32 bits. Left channel data + right channel data equals 64 bits. At 4× oversampling at 48 kSPS we then need a serial clock of 12.288 MHz. This does not allow much time for the overhead required to run the serial port. Also, we would still have to synchronize the serial port to the operation of the filter since we are outputting two words. And we need to gate off the clock after the 20th bit so as not to overflow the input shift register of the D/A. We have to count the clock pulses into the D/A converter and limit them to 20 or the MSB will clock past the D/A converter's shift register. The counter string also forms the word clock pulse, generating a pulse at the 20th bit. Since the input word is 16 bits at 48 kSPS we use the serial port for the data input. A programmable logic device (PAL) is used to generate all the gating pulses. The PAL programming is available on the Analog Devices BBS (617) 461-4258.

THE ANALOG BOARD

Digital-to-Analog Conversion

The next section of the design is the analog section, which is contained on a separate board. It is comprised of the digital to analog converter (DAC) chip, a de-emphasis circuit, reconstruction filters and output drivers. The purpose of the reconstruction filter is to smooth the output of the DAC by band limiting the signal. This turns the stairstep output of the D/A converter to a smoothly varying analog waveform.

The D/A converter used is the AD1862. It is a conventional multibit 20-bit converter. Although the current trend in consumer audio is toward single bit converters, they don't seem to provide top of the line performance.[10] While they have theoretically perfect linearity, they seem to be lacking in noise and transient performance.

The AD1862 uses a digital offset technique to minimize the nonlinearity at center scale. An adjustment for further optimizing the low level linearity (commonly referred to as the MSB trim) is provided.

The I/V converter IC has been set up to allow a variety of op amps. Space for compensation caps and feedback resistors have been provided which allow for just about any single amplifier (with the standard pinout) to be accommodated. Suggested op amps are the AD797, AD829 or the AD811. Note that this includes both voltage feedback and current feedback (transimpedance) types. See Figure 12. NOTE: Not all passive components used for all op amps.

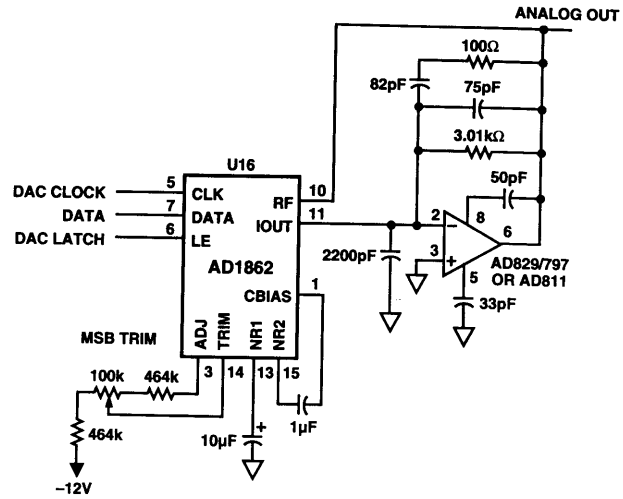


Figure 12.

RECONSTRUCTION FILTER

The next amplifier section (see Figure 13) has a dual purpose. First, it provides compensation for the passband rolloff of the Bessel or Equiripple reconstruction filter. This is about 1 dB at 20 kHz, assuming a cutoff frequency of 30 kHz. The second is to provide a complementary de-emphasis function for the emphasis which is an option in the CD format. The de-emphasis curve is shown in Figure 14. An LED is provided for indication of the activation of this circuit.

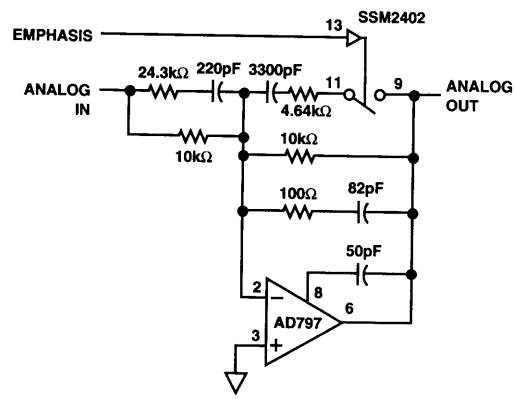


Figure 13.

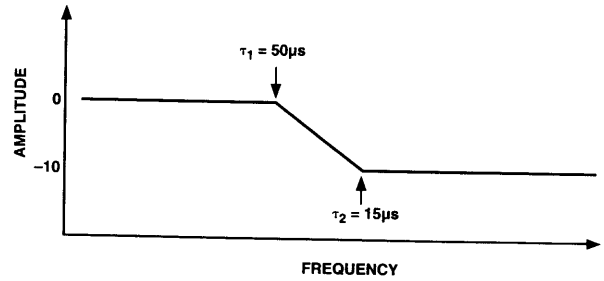


Figure 14. De-Emphasis Curve

It is common practice in most CD systems for the complexity of the output filter to be three poles, usually of the Bessel type. While this does a reasonable job of attenuating the undesirable spectral components, it does not really go far enough.

Let us look at the graphs of attenuation vs. frequency (Figure 15). Using an oversample rate of 4 and a sample rate of 48 kSPS (kilo-samples per second) the DAC's data rate is 192 kSPS. If we assume that 30 kHz is the edge of the passband of the filter, this equates to Ω of 6.4. We use 30 kHz as the passband edge to minimize the attenuation of the filter at 20 kHz and to insure the flat phase response extends well past the audible frequency range.

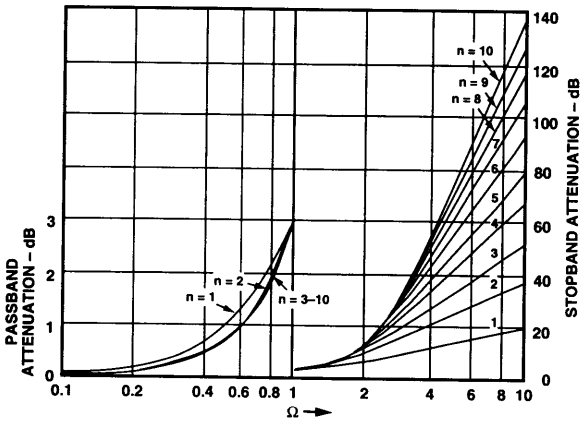


Figure 15. Attenuation Characteristics for Maximally Flat Delay (Bessel) Filters (Used with Permission John Wiley & Co.)

Since we are trying to develop a high quality system with better than 16 bit performance, the spurs should be attenuated by more than 96 dB. We also want Bessel response since it has flat group delay, which will insure that we maintain the phase integrity of the signal. The standard three-pole Bessel filter will be in the area of 40 dB–45 dB attenuation at Ω of 6.4 (Ω = frequency/cutoff frequency). Seven pole Bessel filters will approach 90 dB, eight poles will surpass it. On further investigation we find that an equiripple filter gives almost equivalent performance in the passband but improved attenuation in the stopband. A seventh order Equiripple filter will give us the desired response (see Figure 16).

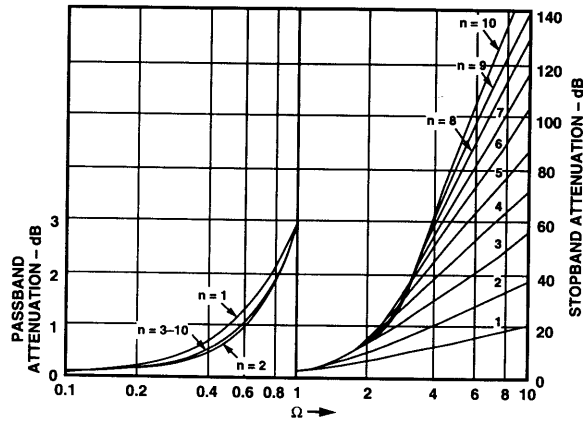


Figure 16. Attenuation Characteristics for Linear Phase with Equiripple Error Filter (Phase Error = 0.05°) (Used with Permission John Wiley & Co.)

Now that we have chosen the type of filter that we are going to build, we must choose the topology of the filter. We choose the FDNR (Frequency Dependent Negative Resistor) topology for several reasons. First, the FDNR has become popular in the audio world because the signal does not pass directly through an op amp. The attractiveness of not passing a signal through an active device is based on the assumption that any active device will distort the signal and, therefore, should be avoided. Secondly, although it does increase the number of components, the sensitivity of the filter response to the accuracy of the component value is decreased. The design of the filter section appears in Appendix A. The schematic of the filter section is shown in Figure 17.

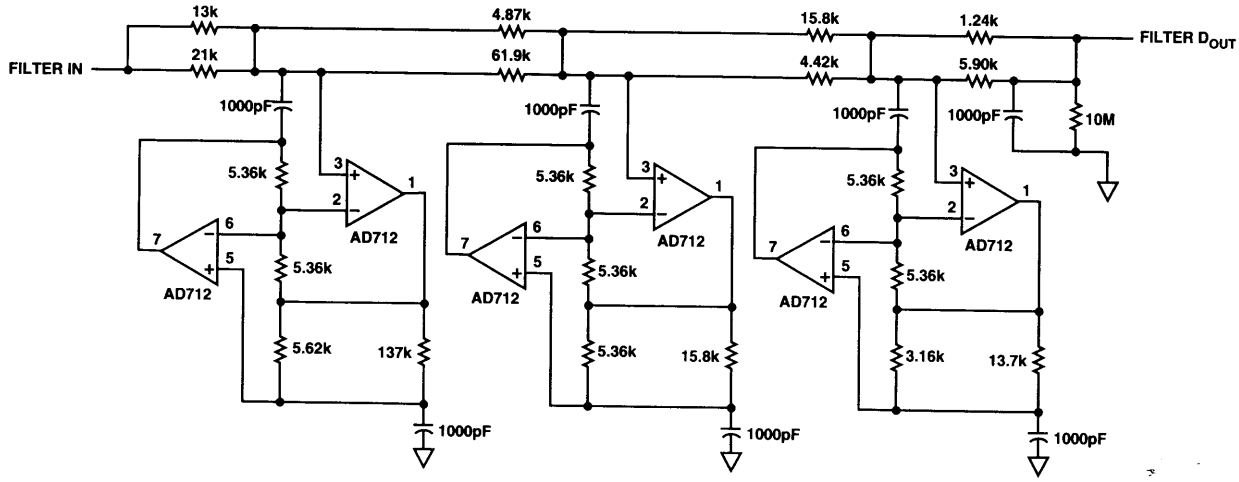


Figure 17.

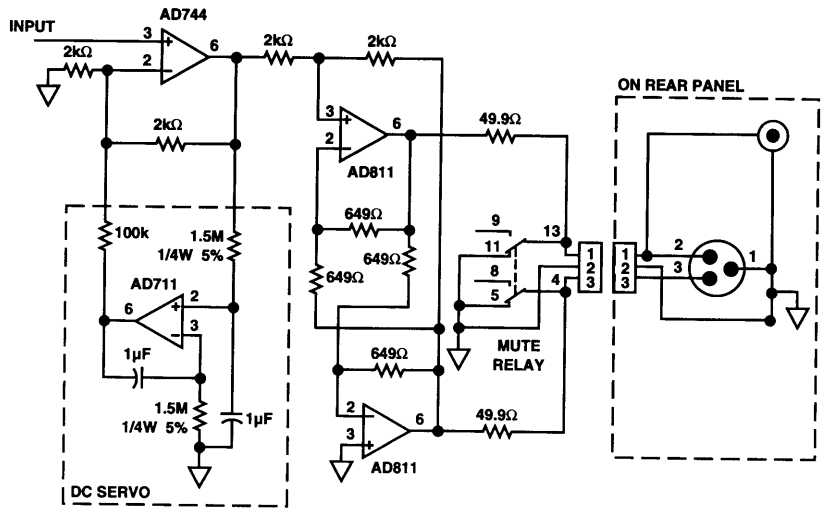


Figure 18.

The AD712 op amp was chosen for use in this circuit for two reasons. First, since it is a FET input device, its high input impedance will not load down the rest of the circuit. Also the high input impedance means that the input bias currents are low, which will also reduce errors. The second reason for using the AD712 is that by virtue of the fact that it is a dual monolithic device the inputs will be inherently well matched, which will improve the performance of the circuit.

OUTPUT DRIVERS

The output of the unit is available as either balanced or single ended signals. The balanced format is preferable in that it minimizes ground loops between stereo components. It also has the potential of providing a cleaner signal because the signal is not referred to the local ground but to the inverse of itself. Single-ended outputs are provided simply by using only one side of the balanced output. Single ended are used simply because the vast majority of audio systems will be set up for this type of output. The output of the driver circuit is shorted to ground by the mute relay at power up and anytime an error is detected by the AES receiver or the sample rate converter. The schematic of the output section is shown in Figure 18.

APPENDIX A FILTER DESIGN

We choose to use a Bessel type filter for the reconstruction filter because of it's superiority in the time domain. As stated earlier we actually use an equiripple filter that has slightly better attenuation but with still good transient response. The price we pay is for slightly greater, although still flat, group delay. Figure 19 compares the Equiripple filter response to Bessel and Butterworth filter responses. The reason we give up the better attenuation of the Butterworth filter types is for the transient performance and flat phase response, as demonstrated by the Impulse and step responses. Figures 20 and 21 show the transient response of Equiripple filter compared to Bessel and Butterworth response filters.

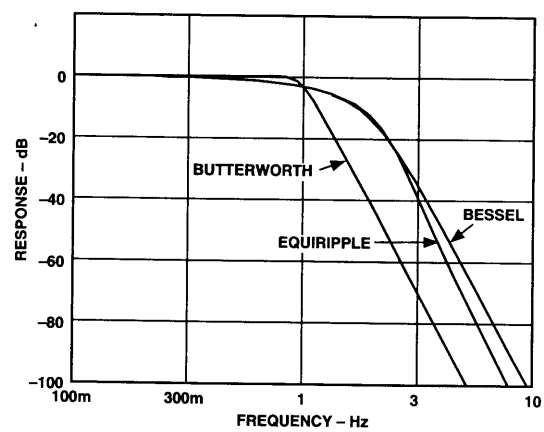


Figure 19. Normalized Filter Comparison Frequency Response

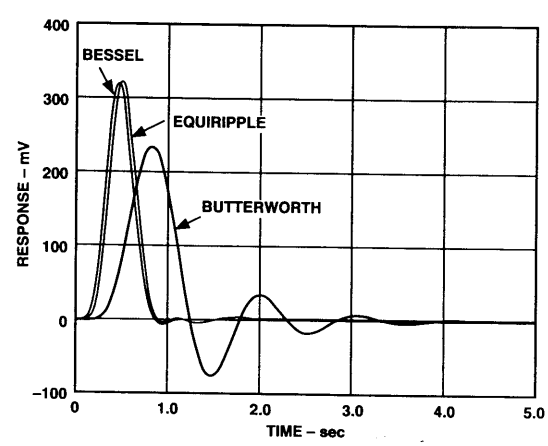


Figure 20. Normalized Filter Comparison Impulse Response

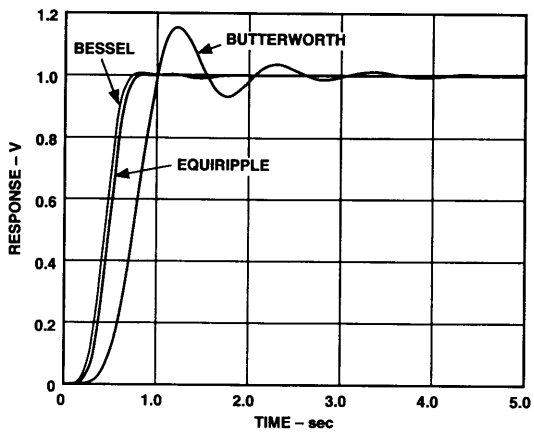


Figure 21. Normalized Filter Comparison Step Response

We choose the single terminated ($R_S = 0$) version of the filter rather than the double terminated so that we eliminate a capacitor in the signal path. Going to the charts[11] we get the following values:

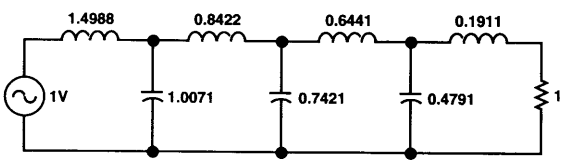


Figure 22. Normalized Filter Prototype

We now perform the transformation by s to transform the filter into the Frequency Dependent Negative Resistor (FDNR) form.

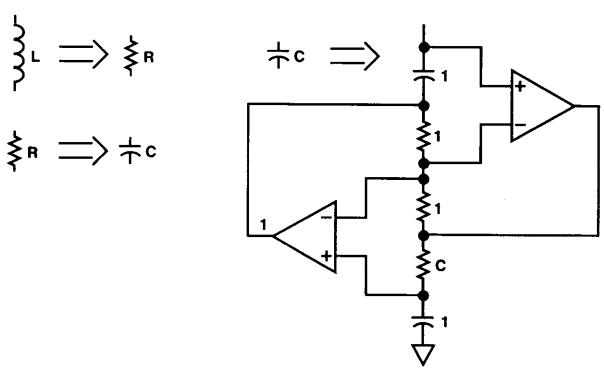


Figure 23. Frequency Dependent Negative Resistor 1/S Impedance Transformation

We now must denormalize the filter by frequency and impedance. We have chosen a cutoff frequency of 30 kHz. Therefore we define a frequency scaling factor (FS) of $2\ F_C = 1.884 \times 10^{-5}$. Next we choose a normalized capacitor value of 1000 pF. This allows us to then define a impedance normalizing factor of $Z = C/(FS\ C')$. All capacitor values are then multiplied by $Z \times FS$. All resistors are then multiplied by Z. When calculating the values of the resistors in the filter we find that they do not fall on a standard value. We now modify the center frequency to allow for a standard value for the 5.305 kΩ resistor that shows up twice in each section. The standard value is 5.36 kΩ. This results in a center frequency of 29.693 kHz. For the rest of the resistor values we parallel two values to allow us to get an accurate response as possible. The frequency and group delay of the filter are shown in Figure 24 and Figure 25.

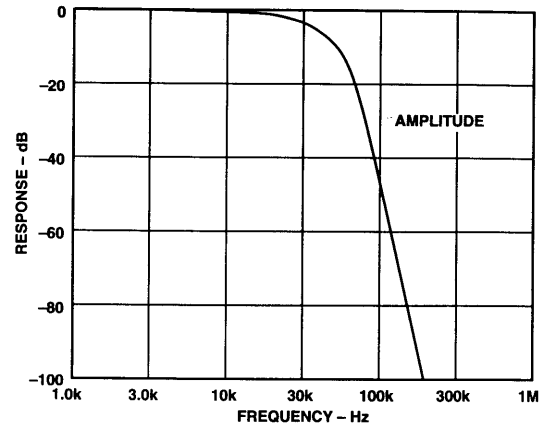
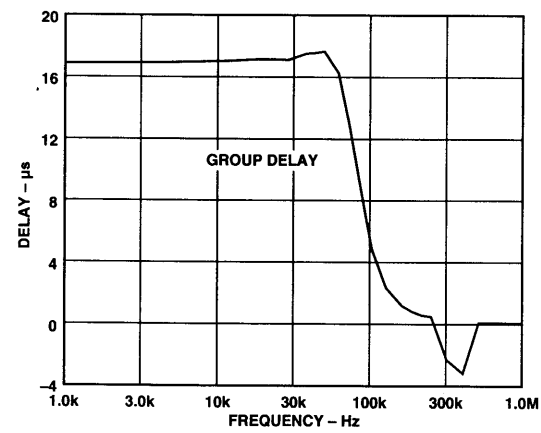


Figure 24. Reconstruction Filter



Filter 25. Reconstruction Filter

APPENDIX B POWER SUPPLIES

One of the most overlooked aspects of audio design is the power supply. It is an essential part of the circuit. If there is noise on the power supplies to an op amp, it will be passed on to the rest of the circuit. All op amps have a power supply rejection ratio (PSRR) specified. Although the PSRR is generally large at low frequency, it falls as the frequency is increased. Therefore, we use decoupling capacitors to shunt high frequency noise from the circuit. As has been discussed many time in the literature, these decoupling caps must have good high frequency performance (low ESR, etc.) and must be located as close to the amplifiers as possible.

We also can improve the voltage regulator that we use to provide the power. Standard regulators, such as the LM78XX series, do a good job of stabilizing the voltage at dc, their output impedance rises with frequency. This is because they are based on an amplifier with limited gain bandwidth product. We can make significant improvements in the performance of the system as a

whole by designing a regulator using more modern amplifiers with higher gain-bandwidth products. The circuit simple amplifies the difference between the reference, which is provided by a Zener diode and its own output, buffered by a pass transistor. A complete schematic of the regulator is provided in Figure 26. In addition high speed soft recovery diodes are used as rectifiers in the power supply. This results in reduced RFI.[13]

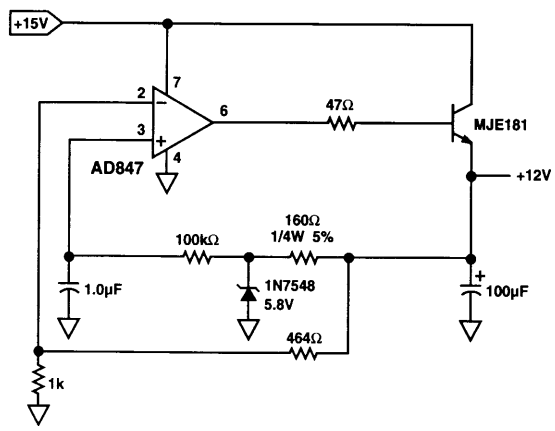


Figure 26. Positive Regulator

CONCLUSION

We have presented a complete, state of the art outboard DAC. Full schematics, copies of the PAL program and copies of the Gerber files for the project are available on the Analog Devices DSP BBS (617) 461-4258.

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