THE SAFE OPERATING AREA (SOA) PROTECTION OF LINEAR AUDIO POWER AMPLIFIERS

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Introduction

The desirability, or lack thereof, of over-voltage and over-current protection for power semiconductors in audio power amplifiers remains a point of contention in the field[1]. For example, some designers[2] appear to recommend multiple-transistor complementary output stages, as often mandated by high-power class-A operation, to circumvent the need for SOA protection of bipolar devices, while others[3] suggest that such voltage-current (*alias* V-I) limiters may be dispensed with altogether by merely adopting enhancement-mode power MOSFETs (hereinafter e-MOSFET).

These views appear to be rather more widely accepted than they should, and constitute a charter for near heroic unreliability in amplifiers so designed, as even a momentary short to ground can destroy an expensive output stage. The zener diode-clamping of the gate-source voltage of e-MOSFETs is thought by some[4,5] to be all that is required in regard to protection. While the zener diodes are mandatory (ideally with $10V < V_{zener} < 20V$ to prevent premature clamping) they only serve to protect the e-MOSFET's gate oxide insulation from over-voltage destruction[6], and do nothing whatever to protect the device from accidental short circuits and forbidden voltage-current combinations that may occur when the amplifier is called upon to drive reactive loads.

The positive temperature coefficient of on-resistance[7] (and therefore *negative* temperature coefficient of drain current) enjoyed by e-MOSFETs eliminates the secondary breakdown phenomenon which is the bane of bipolar transistors, but does not constitute licence for wilful violation of power dissipation limits in linear audio-frequency applications. This is in contrast to ultrasonic switching usage, where e-MOSFET dissipation bounds may be blissfully ignored, and adherence to drain current and drain-source voltage limits will suffice.

All output stage semiconductors used in complementary or quasi-complementary (full or half bridge) linear audio power amplifiers, without exception, require SOA protection for reliable operation. However, such circuitry must be carefully designed to prevent premature activation during normal amplifier operation.

Single slope linear foldback limiting

Many low to medium-power (sub-200W into 8Ω) commercial audio amplifiers incorporate a single slope linear foldback voltage-current protection circuit (**fig. 1**) attributed to **S.G.S. Fairchild Ltd.** by Dr A.R. Bailey[8]. In practice, the complimentary output transistors T_{O1} and T_{O2} may each consist of a compound arrangement of at least two transistors in series.

The instantaneous collector-emitter voltage v_{ce} across T_{O1} is sensed by **R1**, **R2** and **R3**, while the output current, expressed as a voltage across emitter resistor R_e, is simultaneously monitored by **R2** and **R3**. Thus these voltages are summed algebraically at the base of protection transistor T_{P1} which is driven into conduction shunting voltage drive to T_{O1} in the event of an over-voltage, over-current or simultaneous occurrence of both conditions in the output device.
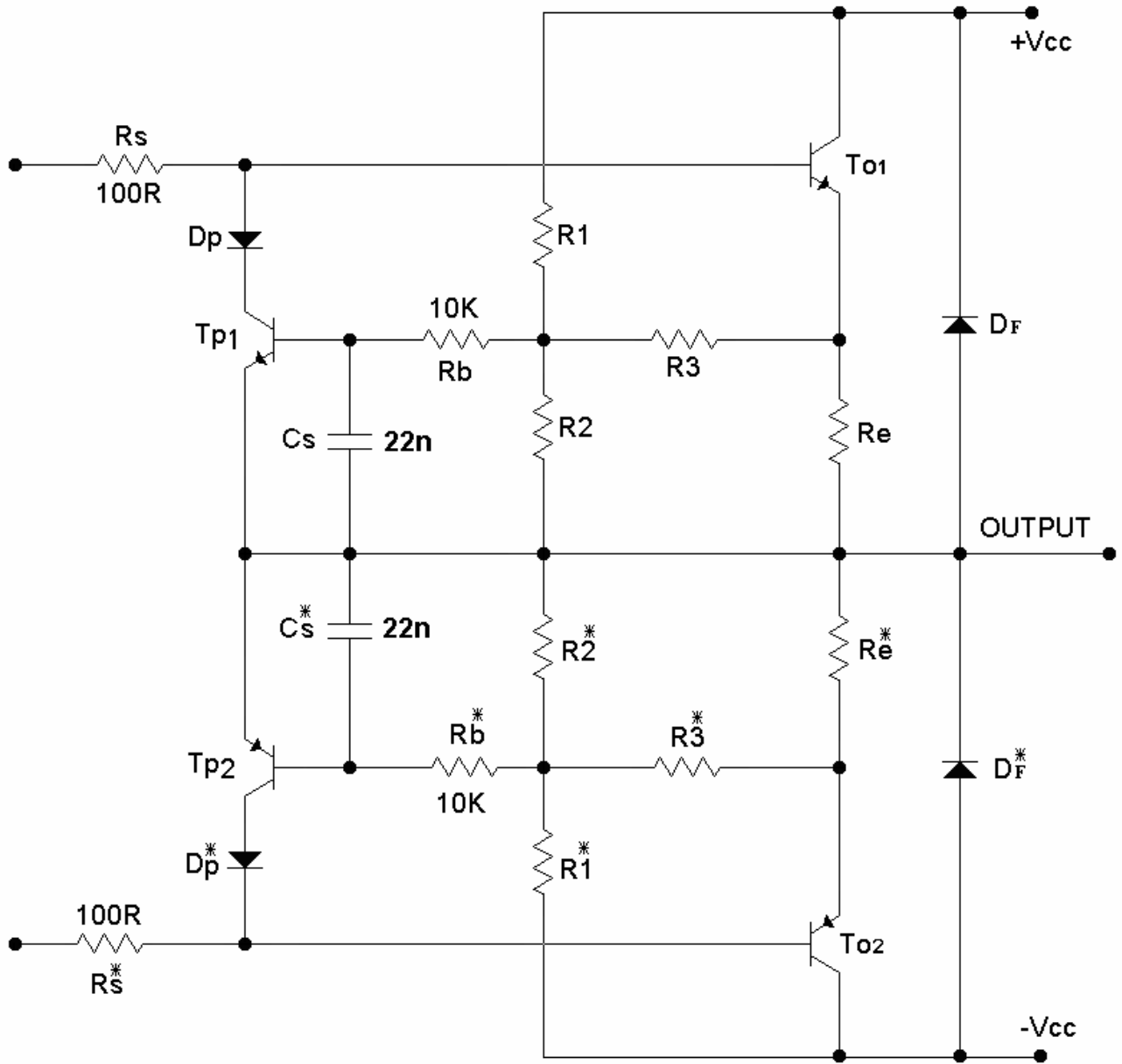
Fig. 1. Improved version of Fairchild's single slope linear foldback protection circuit applied to a complementary output stage.

The series resistor R_S (typically $100R \leq R_S \leq 2K2$) expedites this process by limiting the current required by T_{P1} to shunt voltage drive to T_{O1}. The freewheeling diode D_F protects the output device from excessive base-emitter reverse bias[9], due to beyond-rail voltage spikes generated when SOA protection is invoked with inductive loads, while D_P performs the same function for the small-signal protection transistor T_{P1} by preventing its base-collector junction from being forward biased[5].

If the amplifier's output approaches the negative supply rail while driving a sufficiently low impedance, the current sunk by T_{O2} generates an appreciable voltage drop across its emitter resistor R_e^*; the output is then at an appreciably higher potential than the common input to the complementary output stage. Consequently, transistor T_{O1} is reverse biased and T_{P1}'s base-collector junction, in the absence of its collector diode D_P, would be forward biased causing current to flow from emitter to collector.

Diode D_P prevents this form of spurious inverse-active mode limiter activation by decoupling T_{P1}'s collector as T_{O1}'s base-emitter junction is reverse biased. The potential at T_{O1}'s emitter is then equal to the output voltage since T_{O1} is non-conducting and, contrary to Duncan[10], only negligible leakage current flows through its emitter resistor R_e. By symmetry the explanation above also applies to the negative half of the circuit.

A small-value capacitor is sometimes connected across the base-collector junction of each protection transistor[1] with a view to eliminating oscillation that occurs in the network during the limiting process. These capacitors appear in parallel at AC and are entirely unsatisfactory, as they create an ill-defined and therefore undesirable feedfoward path around the output stage, shunting it out of the global feedback loop at high audio frequencies-precisely where the amplifier is most vulnerable with respect to non-linearity.

Such vulnerability is due to a necessarily diminished feedback factor at high audio frequencies in the interest of Nyquist stability. Connecting the capacitor across the base-emitter junction of each protection transistor is the preferred solution.

Series base resistors R_b and R_b^* (of the order of $10K$) are also recommended for each protection transistor. These base ballast resistors make for better controlled activation of the protection transistors by damping anomalous voltage spikes otherwise provoked by these transistors being overdriven.

Additionally, the single pole low-pass filters comprising ballast resistors R_b, R_b^* and shunt capacitors C_S, C_S^* prevent activation of the protection transistors at ultra-sonic frequencies where such protection is unnecessary. For typical values, the source impedance of the protection circuit (referred to the base of each protection BJT) may be deemed negligible compared to the value of the ballast resistor. For brevity, diodes D_F, D_F^*, D_P, D_P^*, base-emitter shunt capacitors C_S, C_S^* and ballast resistors R_b, R_b^* are omitted in all subsequent figures.

The values of R_b and C_S shown in **figure 1** provide 6dB of attenuation at approximately 1Khz. This is roughly equivalent to doubling the permissible power dissipation per output device at this frequency.

The filter's nominal time constant may not exceed **500µS** with bipolar output transistors, as the filter is required to partially damp the oscillation that occurs during limiting and not completely eliminate it. This is because this oscillation is intrinsic to the circuit's operation.

For instance, if the amplifier's output swings positive during persistent SOA overload (such as a continuous short-circuit to ground or negative supply rail), protection transistor T_{P1} is driven forward-active, cutting off output transistor T_{O1}. The fault is therefore removed with respect to T_{O1} and protection transistor T_{P1} is promptly disabled. This in turn causes the instantaneous recurrence of the overload condition and attendant reactivation of T_{P1}. The on-off action of the protection transistor in these circumstances appears as persistent local high frequency oscillation which, contrary to popular opinion, has nothing to do with the stability of the protection circuit or, indeed, the amplifier's major feedback loop.

The resistor values for the arrangement of **figure 1** are obtained by drawing the desired protection locus on a *linear-linear* scale graph of the output transistor's DC safe operating area (**fig. 2**). One of the three resistors (usually **R3**) is assigned an arbitrary value (typically $100R \leq R3 \leq 1K$), and the two remaining resistors evaluated from simultaneous equations developed from two convenient points on the protection locus.
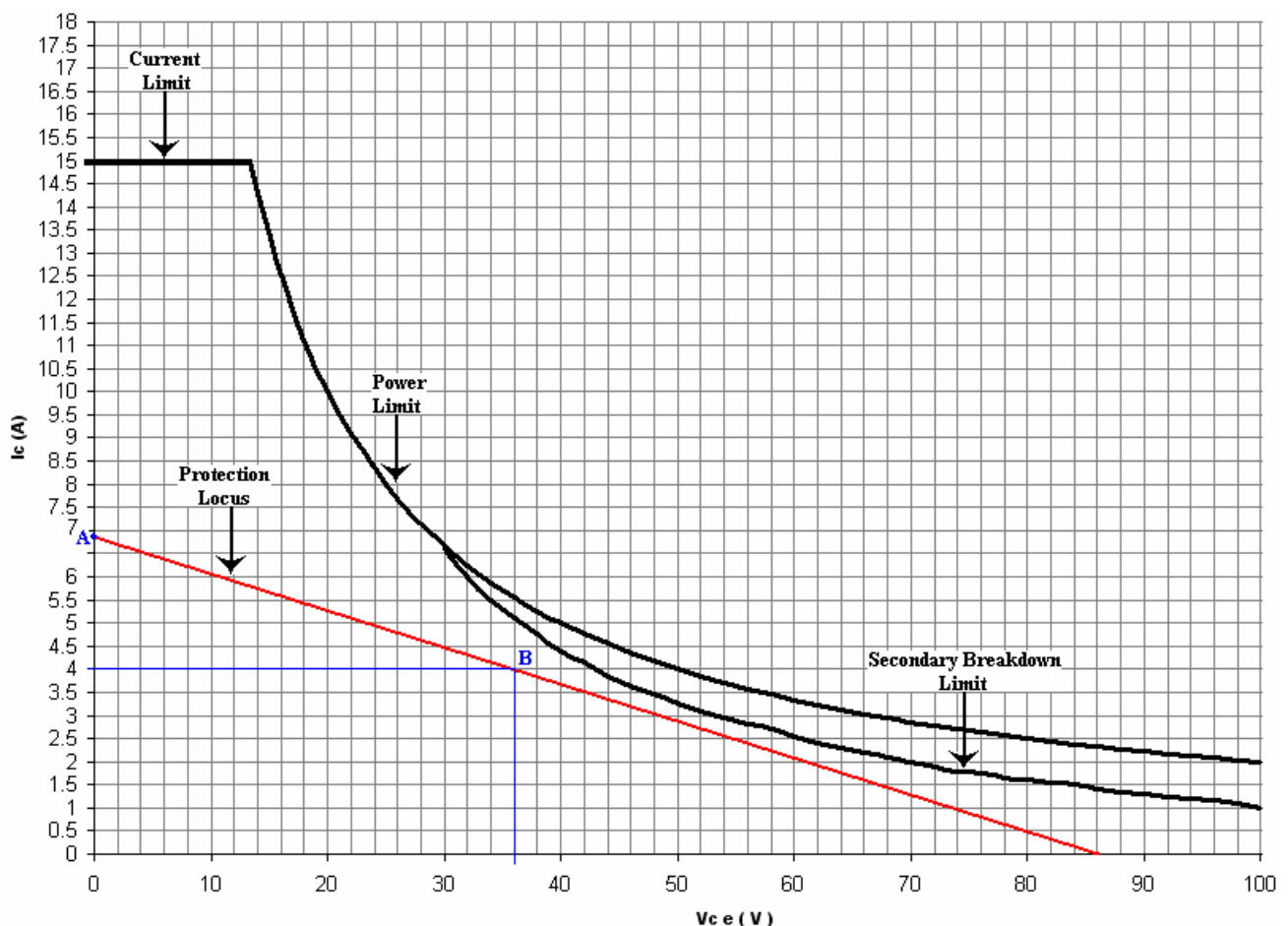

Fig. 2. Safe operating area of On Semiconductor®'s MJL3281A; the single slope linear foldback protection locus is drawn to intersect the Vce-axis at a value greater than $2|V_{cc}|$ to prevent premature limiting.

With this arrangement, it is essential that the linear protection locus intersect the SOA's **Vce** axis at a value greater than the sum of the moduli of the amplifier's voltage supplies; otherwise $\mathbf{T_{P1}}$ turns on under normal loading when the output swings negative, even with the output open-circuit. Similarly, $\mathbf{T_{P2}}$ would be activated under normal output loading when the output swings positive. This effectively short-circuits the "small signal" circuit preceding the output stage directly to the output, causing gross distortion.

Failure to adhere to the above condition appears to have caused some designers to erroneously abandon electronic SOA protection of any form altogether[1,12]. However, this requirement presents a significant impediment to the efficient utilisation of the comparatively large SOA in the low-**Vce** region of the graph. This is especially true of amplifiers with relatively high supply-rail voltages where in the case of bipolar transistors secondary-breakdown severely curtails flexibility in optimal placement of the protection locus.

This is graphically illustrated in **figure 2** for an amplifier with nominal ±40V supply rails, and using **On Semiconductor®'s** excellent[13] 200W **MJL3281A-MJL1302A** complementary power transistors. Note that although the datasheet SOA of 200W for these devices is used here for brevity, this is specified at a device case temperature $\mathbf{T_C} = 25^{\circ}\mathbf{C}$. The later is only achievable with an improbable heat sink of infinite dimensions. In practice, the datasheet SOA should be adjusted (*viz.* "derated") to accommodate the transistor's steady state case temperature with the designer's selected heat sink.

Only the positive half of the circuit of **figure 1** need be used to calculate the required passive component values (**fig. 3**). Ideal active devices are assumed, with infinite input impedance, zero saturation voltage and zero ohmic resistance. The error thus accrued is negligible, provided small-signal transistors of high current-gain $(\beta \geq 100)$ are used. Let $\mathbf{V_{be}}$=0V6, $\mathbf{R_3}$=220R and **Re**=0R22.

Taking two arbitrary points **A** and **B** on the locus where at point **A** Ic=6.85A, **Vce**=0V, and at point **B** Ic=4A, **Vce**=36V, it follows from **figure 3**:

$$0.6 = \frac{1.507\mathbf{R}_2}{\mathbf{R}_2 + \mathbf{R}_1 220/(\mathbf{R}_1 + 220)} \tag{1}$$

With reference to **figure 4** and noting that the contribution of $\mathbf{I}_3$ to the current in $\mathbf{R_e}$ is negligible:

$$\mathbf{I}_2 = \mathbf{I}_1 + \mathbf{I}_3 \tag{2}$$

$\Rightarrow$

$$0.6/\mathbf{R}_2 = (40 - 3.72)/\mathbf{R}_1 + (4 - 3.72)/\mathbf{R}_3$$

$\Rightarrow$

$$0.6 = \mathbf{R}_2(36.28/\mathbf{R}_1 + 0.28/220) \tag{3}$$

Solving **(1)** and **(3)** simultaneously gives $\mathbf{R}_1 \approx 12\text{K}4$ and $\mathbf{R}_2 \approx 143\text{R}0$. For enhanced accuracy it is recommended that these values be made up from series or parallel combinations of 1% resistors where necessary.

When the output swings to -40V, then 80V appears across $\mathbf{R}_1$ in series with $\mathbf{R}_2 \text{//} \mathbf{R}_3$ to a good first approximation. Thus, the voltage present at the base of the protection transistor $\mathbf{T}_{P1}$ is given by:

$$V_{be} \approx \frac{80(\mathbf{R}_2 \text{//} \mathbf{R}_3)}{(\mathbf{R}_2 \text{//} \mathbf{R}_3) + \mathbf{R}_1} \approx 0V55$$

Therefore, it follows that spurious activation of $\mathbf{T}_{P1}$ cannot occur if instantaneous collector current i_c is less than the maximum permissible collector current $I_{C(MAX)}$ at $v_{ce} \approx 2|V_{cc}|$. A general expression that facilitates the rapid verification of the compliance of any amplifier using single slope linear foldback limiting may be developed:

$$\left| \frac{2\mathbf{V}_{cc}(\mathbf{R}_2 \text{//} \mathbf{R}_3)}{\{(\mathbf{R}_2 \text{//} \mathbf{R}_3) + \mathbf{R}_1\}} \right| < \mathbf{V}_{be}$$

$\Rightarrow$

$$\boxed{\left| \frac{2\mathbf{V}_{cc}\mathbf{R}_2\mathbf{R}_3}{(\mathbf{R}_2\mathbf{R}_3 + \mathbf{R}_1\mathbf{R}_2 + \mathbf{R}_1\mathbf{R}_3)} \right|_{T_A=25^o C} < 0V6} \tag{4}$$

Equation 4 is true only at an ambient temperature $\mathbf{T}_A$ of $25^o\mathbf{C}$ as the threshold voltage of the protection transistors may be expected to drop roughly 2mV per degree Celsius increase in temperature. Further equation 4 is valid subject to the following condition:

$$i_C < I_{C(MAX)}\big|_{v_{ce} \approx 2|V_{cc}|} \tag{5}$$

This condition is invariably fulfilled during normal operation, as no practical loudspeaker system would demand that the output transistor sustain $v_{ce} \approx 2|V_{cc}|$ while providing any appreciable current.
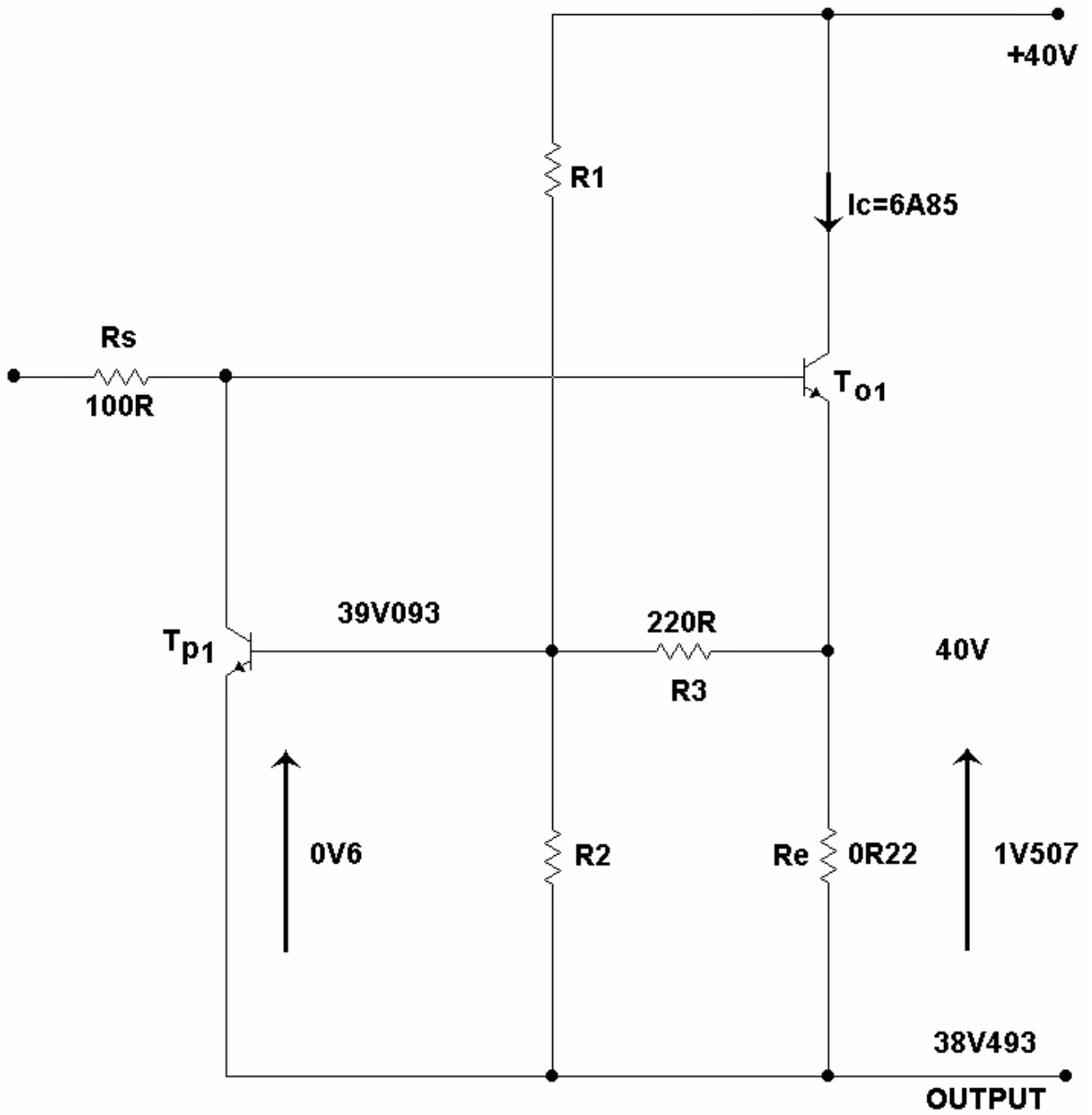
Fig. 3. Output conditions at point A on the protection locus of figure 2.
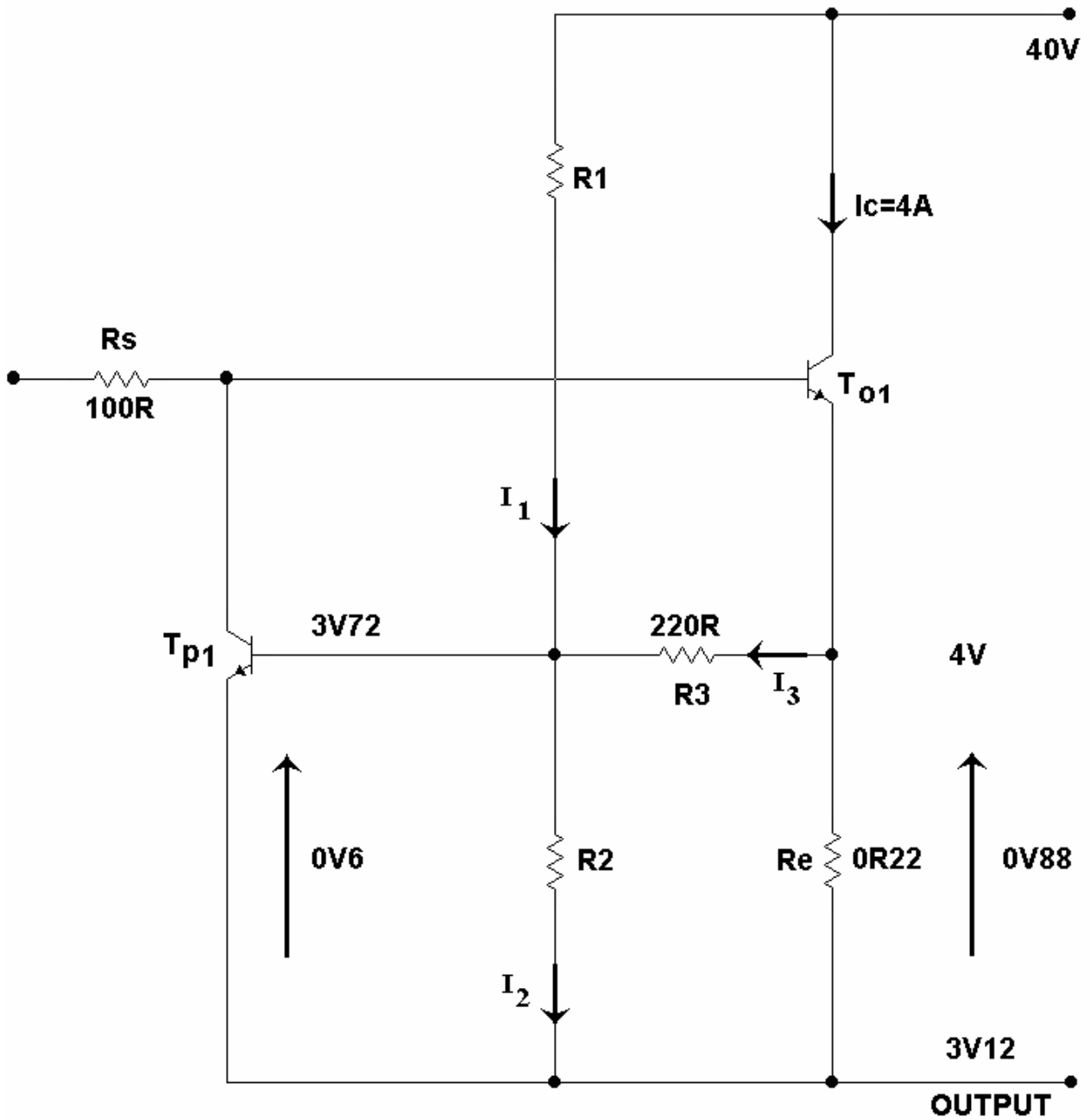
Fig. 4. Output conditions at point B on the protection locus of figure 2. The contribution of I_3 to the current in Re is negligible.

Figure 5 shows a common variation[10,11,13,14] on the single slope linear foldback limiter of **figure 1**, with resistor $\mathbf{R}_2$ excised so that from **equation 4**:

$$\left| \frac{2\mathbf{V}_{cc}\mathbf{R}_3}{\{\mathbf{R}_3 + \mathbf{R}_1 + (\mathbf{R}_1\mathbf{R}_3/\mathbf{R}_2)\}} \right| < 0\mathbf{V}6$$

Since $\mathbf{R}_2 \to \infty$, then:

$$\left| \frac{2\mathbf{V}_{cc}\mathbf{R}_3}{(\mathbf{R}_3 + \mathbf{R}_1)} \right|_{\mathbf{T}_A = 25^\circ\mathbf{C}} < 0\mathbf{V}6$$

The optimal protection locus for this network (**fig. 6**) must be plotted so that calculated resistor values comply with the above condition. This scheme is atrociously inefficient, as for a nominal $\mathbf{V}_{ce} \approx 0\mathbf{V}$ and **Re**=0R22, resistors $\mathbf{R}_1$ and $\mathbf{R}_3$ are in parallel and, of necessity, the collector current i_c is prematurely limited to $\left\{\mathbf{I}_c\big|_{\mathbf{V}_{ce}\approx 0\mathbf{V}} < (\mathbf{V}_{be}/\mathbf{R}_e \approx 2\mathbf{A}7)\right\}$.

A value of **Re**=0R1 gives a modest improvement, with $\left\{\mathbf{I}_c\big|_{\mathbf{V}_{ce}\approx 0\mathbf{V}} < (\mathbf{V}_{be}/\mathbf{R}_e \approx 6\mathbf{A}0)\right\}$. Clearly claims[13] of "load-invariant" drive capability made for power amplifiers using this scheme are rather premature.

The protection locus is realised by deriving output stage conditions (**fig. 7**) at a single arbitrary point **B** on the locus subject to $\left\{0 < \mathbf{V}_{ce} < 2|\mathbf{V}_{cc}|\right\}$. With $\mathbf{V}_{cc} = 40\mathbf{V}$, **Re** = 0R22, $\mathbf{R}_3$=220R and noting that $\mathbf{R}_1$ and $\mathbf{R}_3$ constitute a simple voltage divider, then:

$$\mathbf{R}_1 \approx \frac{(40 + 39.4)}{(-39.4 + 39.78)/220\mathbf{R}} \approx 46\mathbf{K}$$

This unwarranted dependence on the value of **Re** is unacceptable as in some applications, such as output stages comprising paralleled complementary e-MOSFET pairs, $(0\mathbf{R}1 < \mathbf{R}_e \leq 1\mathbf{R}0)$ may be required to guarantee equable current sharing.
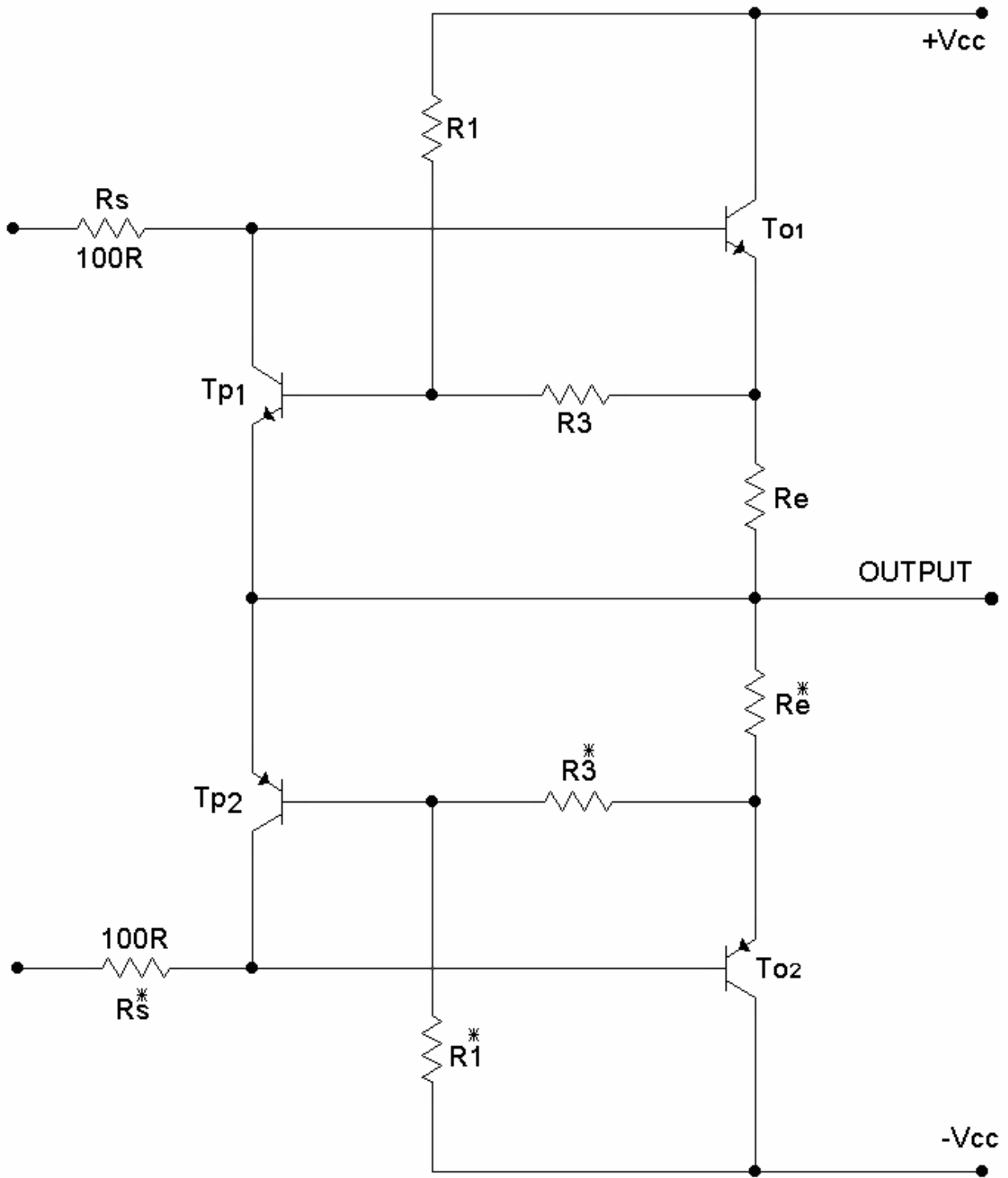
Fig. 5. Compromised single slope linear foldback scheme gives grossly inefficient SOA utilisation.
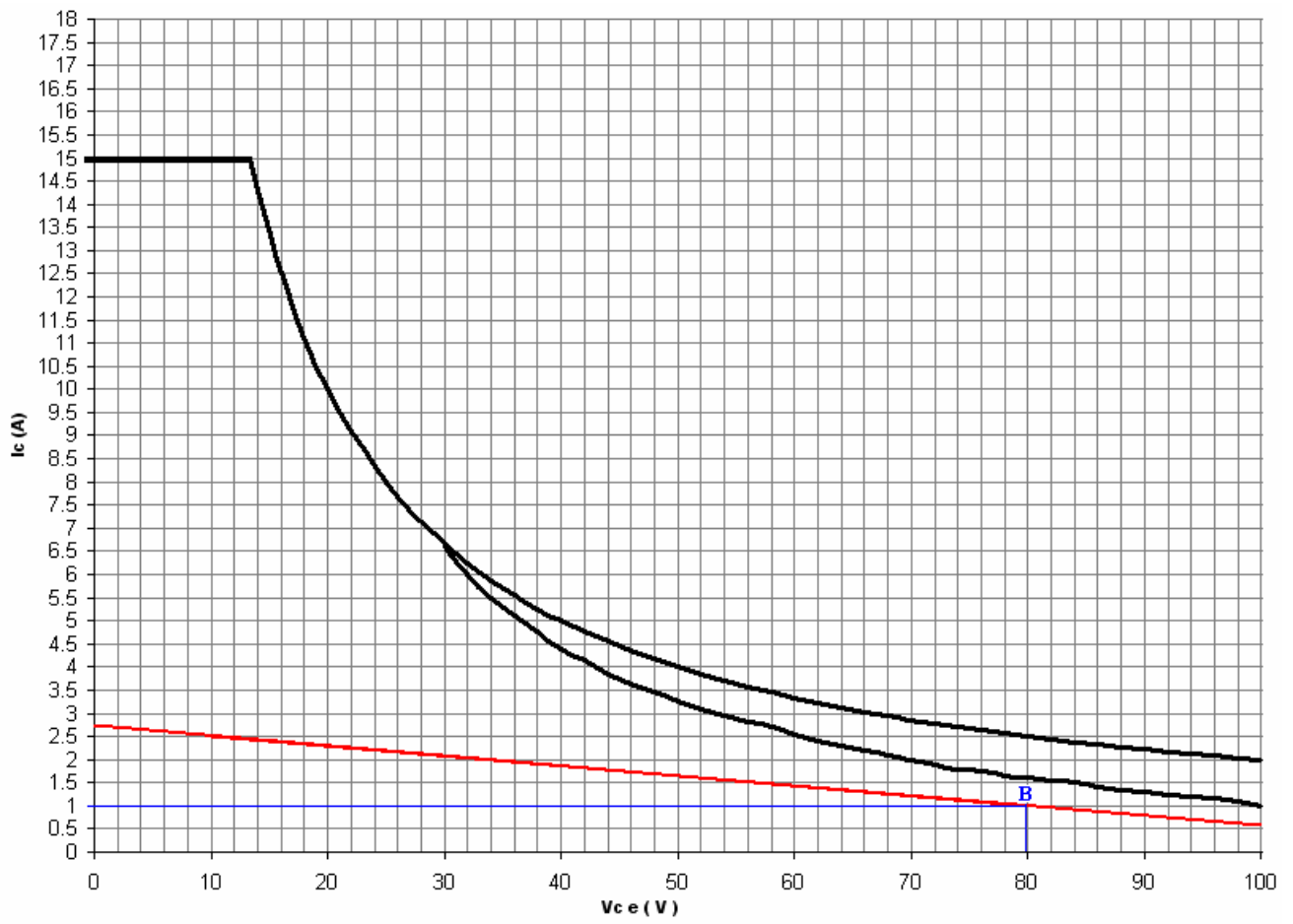
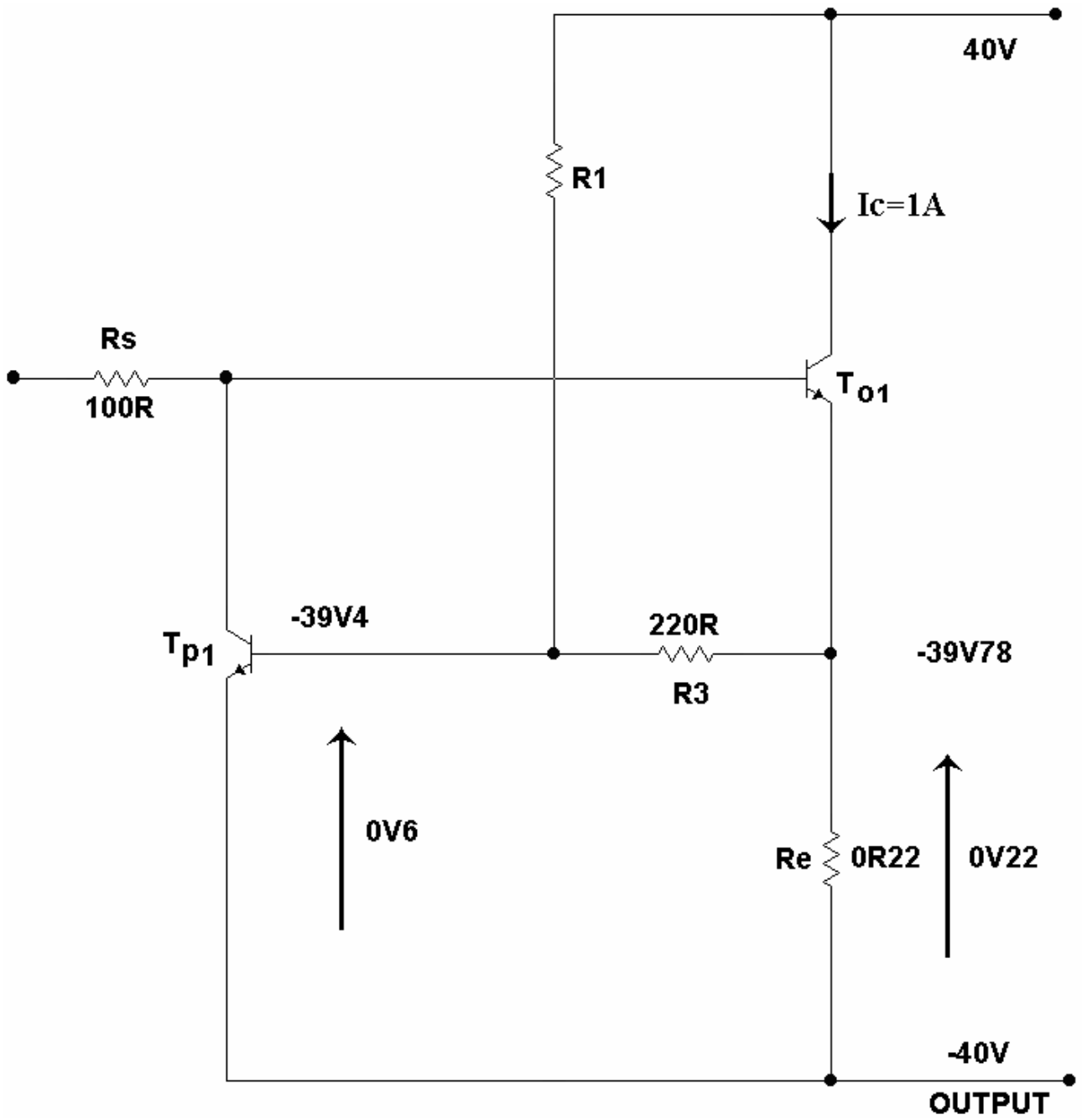**Fig. 6. Linear protection locus clearly shows the inflexibility of the scheme of figure 5.**

Fig. 7. Output conditions at point B on the protection locus of figure 6.

<u>**Driving reactive loads**</u>

A clear appreciation of the nature of the amplifier's load is required to establish the bounds within which the SOA limiter must remain inactive. **Figure 8** shows an ideal complementary emitter follower (in Electronics Workbench's **Multisim Professional®** SPICE simulator[15]) used to drive the *de facto* standard $(8\Omega\angle0^{0})$ test load to ±40V supply rails.

The plots obtained in **figure 9** show that the voltage v_{ce} across $\mathbf{T_{O1}}$ is precisely 180^{0} out of phase with the current i_{c} it is required to source; the voltage across the device is a minimum when its collector current is at a maximum and conversely. Instantaneous power dissipation is merely the product of instantaneous device voltage and current; peak transistor dissipation $\mathbf{p_{d(max)}} \approx 50\mathbf{W}$ occurs twice in $\mathbf{T_{O1}}$'s conducting half-cycle, at half the peak load voltage $(v_{out}/2 \approx V_{cc}/2)$ and half the peak load current $i_{c(peak)}/2$.
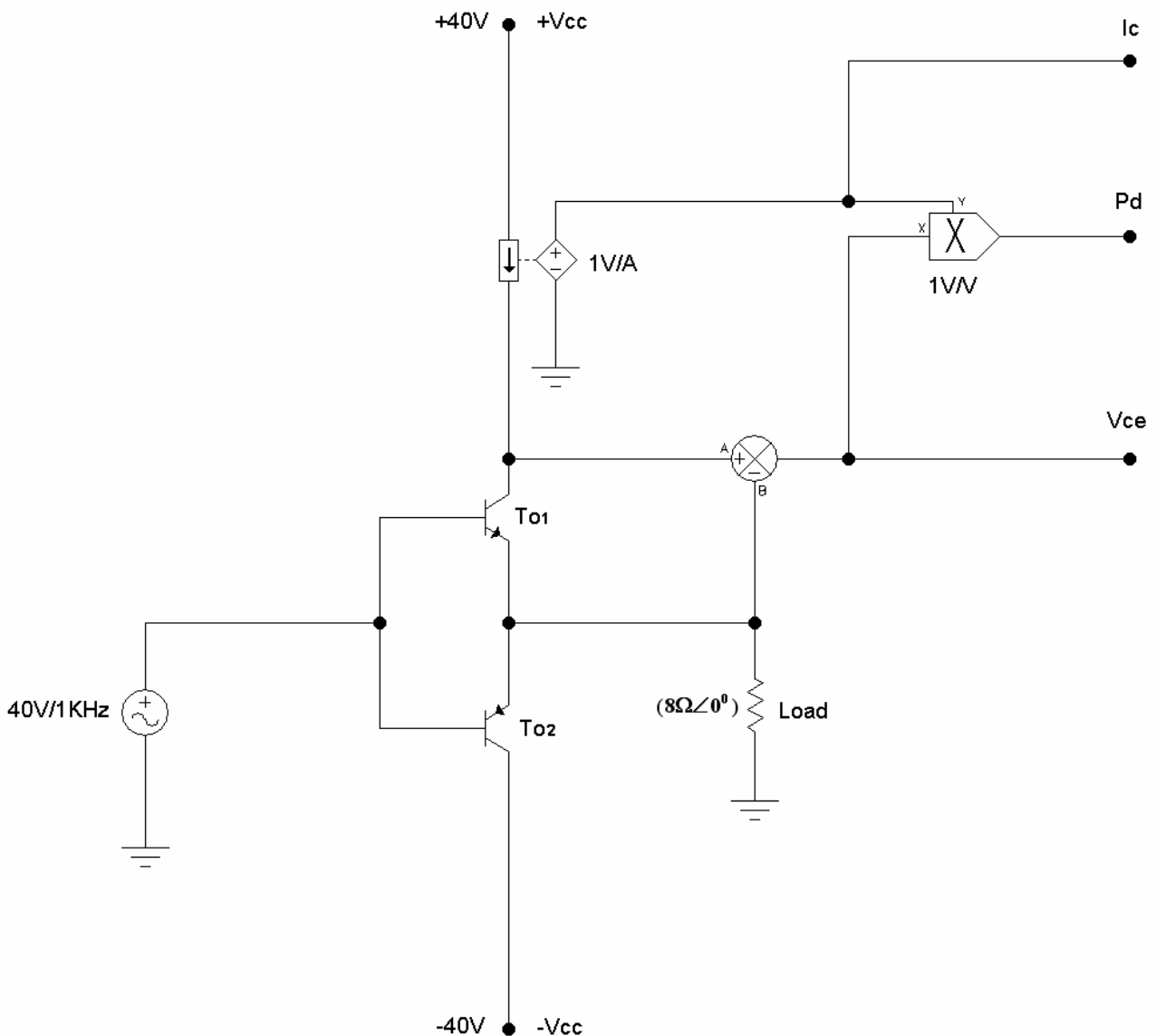
Fig. 8. Ideal emitter follower used to determine instantaneous collector current i_{C}, collector-emitter voltage v_{ce} and device dissipation P_{d}.
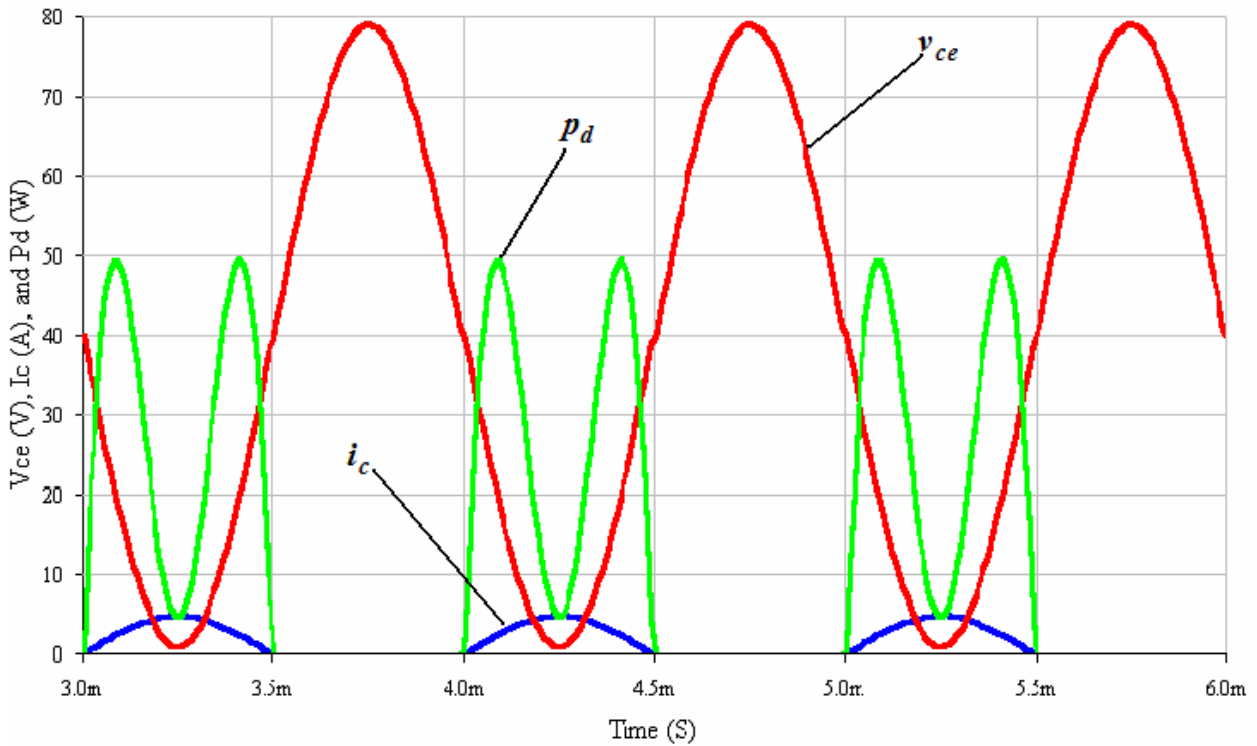
Fig. 9. Instantaneous v_{ce}, i_C and P_d in sourcing output transistor while driving roughly 39V across an $(8\Omega \angle 0^0)$ load.

Since the $(8\Omega \angle 0^0)$ load line resides well below the linear protection locus of **figure 10** (reproduced from **fig. 2**), it is clear that a single pair of **MJL3281A-MJL1302A** power transistors operating from ±40V rails will comfortably drive an 8Ω dummy load to clipping without invoking protection; however, this will certainly not be the case with loudspeaker loads, which are invariably reactive[16,17]. An amplifier with "high-fidelity" aspirations, intended to drive full-range multiple-transducer loudspeaker systems, including electrostatics, should at least be capable of driving a $(4\Omega \angle \pm 60^0)$ impedance without invoking SOA-protection.

A $(4\Omega \angle -60^0)$ impedance was devised in SPICE by driving a 2Ω0 resistor in series with a 45μ9441 capacitor at 1Khz with the ideal complementary emitter follower of **figure 8**. The traces thus obtained (**fig. 11**) were used to plot the $(4\Omega \angle \pm 60^0)$ load line in **figure 10**. Peak transistor dissipation $\mathbf{p_{d(max)}} \approx 362\mathbf{W}$ (with $\sim 39V_{(Peak)}$ across the load) occurs at $v_{ce} \approx 46.9V$ and $\mathbf{i_c} \approx 7.7\mathbf{A.}$

In other words (**fig. 12**), because current leads voltage in a capacitive impedance, transistor $\mathbf{T_{O1}}$ (**fig. 8**) is required to source $\boldsymbol{i_c} \approx 7.7\boldsymbol{A}$ when the output swings *away* from the negative supply rail to $\mathbf{v_{out}} \approx -6\mathbf{V.}$ Similarly, transistor $\mathbf{T_{O2}}$ must sink $\boldsymbol{i_c} \approx 7.7\boldsymbol{A}$ when the output swings from +Vcc to $\mathbf{v_{out}} \approx +6\mathbf{V.}$ Note that the crossover discontinuity in the output voltage characteristic (at $\left| v_{out} \right| \approx 35V$) now precedes zero voltage crossing by 60^0 (**fig. 12**); this is contrary to the popular view that the crossover discontinuity is coincident with zero voltage crossing regardless of the nature of the load.

With a $(4\Omega \angle +60^0)$ inductive impedance, in which current lags voltage, the output conditions are reversed, with the load demanding $\boldsymbol{i_c} \approx 7.7A$ from $\mathbf{T_{O1}}$ when the output swings from the positive supply to $\mathbf{v_{out}} \approx -6\mathbf{V.}$ Regardless of the nature of the load, however, device voltage v_{ce} and load voltage v_{out} are always 180^0 out of phase and of course, being a voltage follower, the input voltage is always in phase with v_{out} at the frequencies of interest.
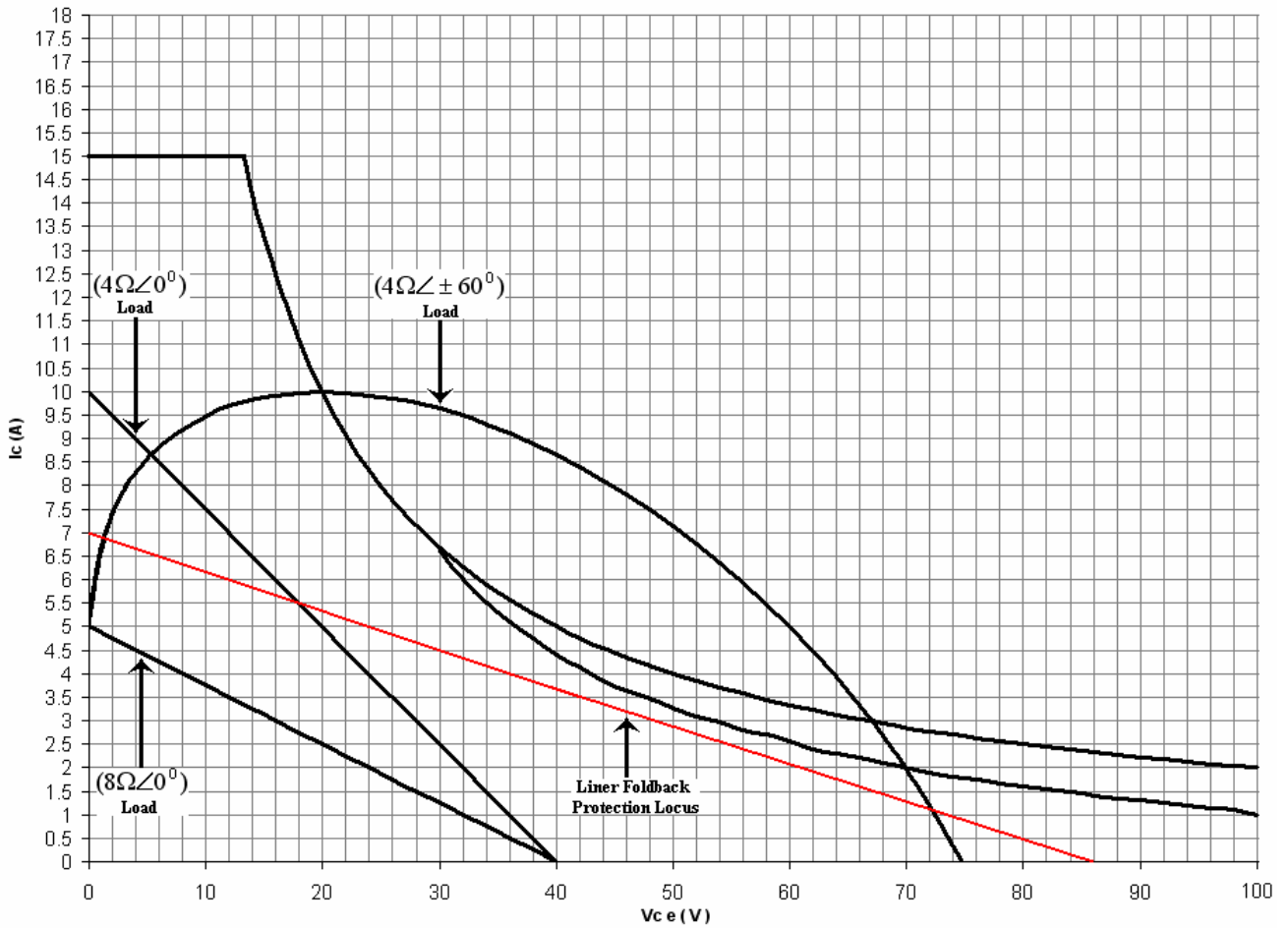
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Fig. 10. The reactive load gives an elliptical characteristic which causes more than seven times greater peak device dissipation than for the $(8\Omega\angle 0^0)$ case.
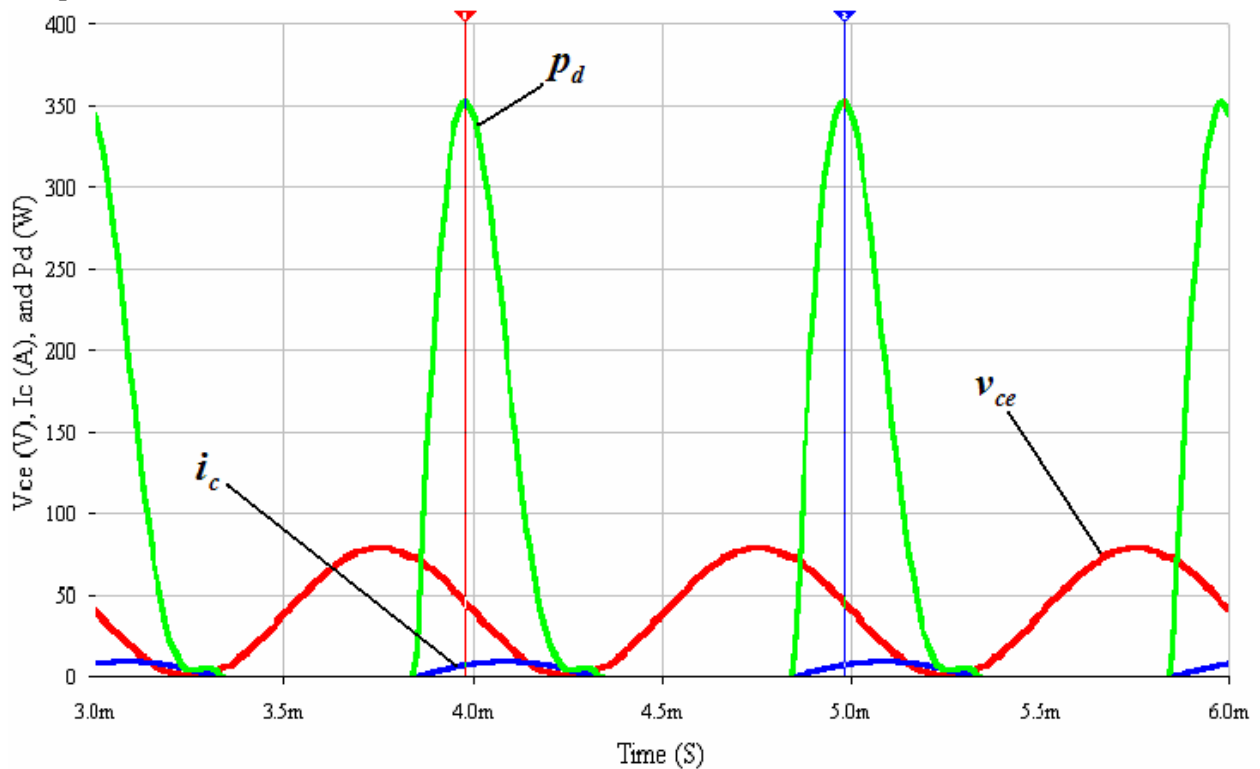

Fig. 11. Instantaneous v_{ce}, i_C and P_d in sourcing output transistor T_{O1} obtained by driving a $(4\Omega\angle -60^0)$ load to a little under $40V_{(Peak)}$.

The linear foldback protection locus (**fig. 10**) only permits 3A at **Vce**=46.9V; therefore a minimum of three output pairs are required to drive a notional ($4\Omega\angle\pm60^{0}$) loudspeaker system from $\pm40V$ supply rails without intrusive limiter activation. Note that this may need to be "derated" to four transistor pairs to accommodate realistic device case temperatures. On this basis, and using other established techniques[11,18], including mandatory DC offset and thermal overload protection systems, a reliable and versatile low distortion amplifier may be constructed.

As the cost of power transistors is significant, there is a compelling financial incentive to minimise the number of devices used by utilising the SOA as efficiently as possible. To this end, it has been suggested[10] that, ideally, the protection locus should closely match the bounds of the SOA. This is unnecessary, as reactive load drive primarily requires that current delivery in the $\left|V_{cc}\right|\le v_{ce}<2\left|V_{cc}\right|$ region be maximized without violating suitably derated DC safe operating limits. In general, as shall be demonstrated, an optimally located nonlinear protection locus with at least one breakpoint should suffice.
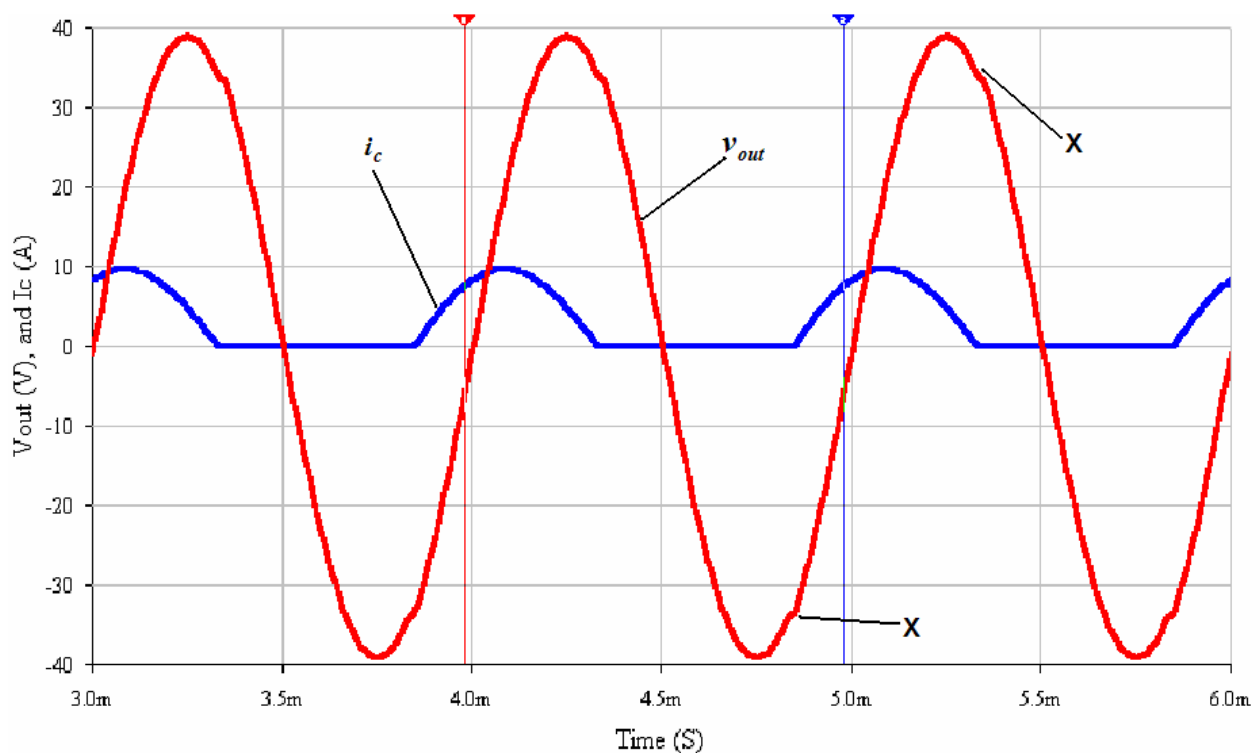

Fig. 12. Transistor T_{O1} delivers 7.7A to the $(4\Omega\angle-60^{0})$ load when the output voltage swings away from -Vcc to -6V. The crossover discontinuity marked X now precedes zero voltage crossing by 60^{0}.

Single slope single breakpoint non-linear foldback limiting

Introducing a zero-gradient segment at some optimal point in the protection locus permits an increase in current delivery at the low-**Vce** end of the SOA without significantly compromising available current at higher device voltages (**fig. 13**). The single slope linear foldback protocol (**equation 4**) is made redundant as the protection locus does not cross the Vce-axis at any point.

The zero-slope segment **BC** is realised by splitting R_1 in **figure 1** into R_{1A}, R_{1B} and clamping the voltage across R_{1B} and R_2 with zener diode D_1 (**fig. 14**) when $\{64V \leq v_{ce} < (2|V_{cc}| = 80V)\}$. When $(0V \leq v_{ce} < 64V)$, segment **AB**, the diode is off (virtually open-circuit) and the circuit reverts to a single slope linear foldback regime. This scheme was apparently introduced by Ruehs[20], but the algebra used to establish component values was incorrect.
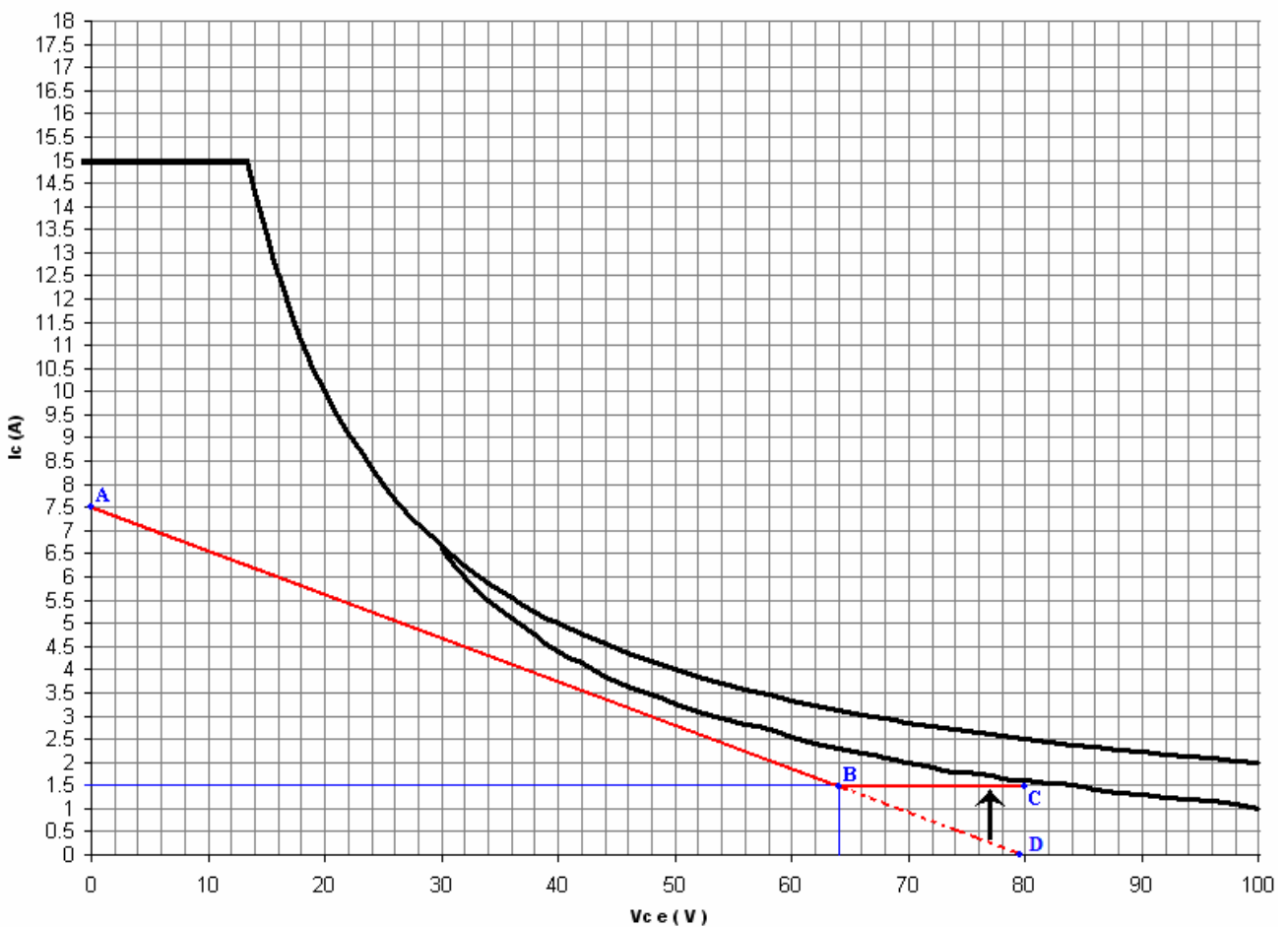
Fig.13. Single slope single breakpoint non-linear foldback protection locus.

The zener diode is disconnected and resistors R_{1A} and R_{1B} amalgamated into one resistor R_1 (**fig. 15**). As was the case with the circuit of **figure 1**, component values are then established for the single-slope locus **ABD** at arbitrarily selected points **A** and **B** where at point **A**, **Ic=7.5A**, **Vce=0V**, and at point **B**, **Ic=1.5A**, **Vce=64V**.

With reference to **figure 15** and selecting $R_1 = 100R$:

$$0.6 = \frac{1.65R_2}{R_2 + R_1 100 / (R_1 + 100)} \tag{6}$$

From **figure 16** and noting that the contribution of I_3 to the current in R_e is negligible:

$$I_2 = I_1 - I_3$$

$\Rightarrow$

$$0.6/R_2 = (40 + 23.73)/R_1 - (-23.73 + 24)/R_3$$

$\Rightarrow$

$$0.6 = R_2 (63.73/R_1 - 0.27/100) \tag{7}$$

Solving (**6**) and (**7**) simultaneously gives $R_1 \approx 4K8$ and $R_2 \approx 56R$.

The zener diode, with an arbitrarily selected zener voltage $V_Z = 10V$, is now introduced and resistor R_1 split into resistors R_{1A} and R_{1B} (**fig. 17**). At point **B** in the protection locus of **figure 13** the diode is at the threshold of conduction and the voltage across it is its zener voltage V_Z. However the current through the diode at this point is still negligible compared to the current through R_{1A} and R_{1B}.

Thus from **figure 17**:

$$I_1 = I_2 + I_3$$

$\Rightarrow$

$$I_1 = \frac{0.6}{56} + \frac{(-23.73 + 24)}{100} = 13.42\text{mA}$$

$\Rightarrow$

$$R_{1B} = \frac{(-14.33 + 23.73)}{13.42\text{mA}} = 700R4$$

$\Rightarrow$

$$R_{1A} = R_1 - R_{1B} = 4K8 - 700R4 \approx 4K1$$

As is the case with the linear foldback locus of **figure 2**, a minimum of three output pairs is required to drive a $(4\Omega\angle\pm60^0)$ load, since available current at $v_{ce}\approx45\text{V}97$ remains unchanged at $i_C\approx3\text{A}1$.

However, with the protection locus of **figure 13**, available current per output pair at $\textbf{Vce}\approx4\text{V}$ increases from 6A4 to 7A1 and the current at $v_{ce}\approx2|V_{cc}|$ increases from 0A5 to just under 1A5 per output pair.

Since the locus is non-linear, caution must be exercised to ensure that while pursuing the secondary objective of enhancing current delivery in the low-Vce region of the SOA, available current in the critical higher device voltage region $(|V_{cc}|\leq v_{ce}<2|V_{cc}|)$ is not simultaneously compromised by the location of the breakpoint.
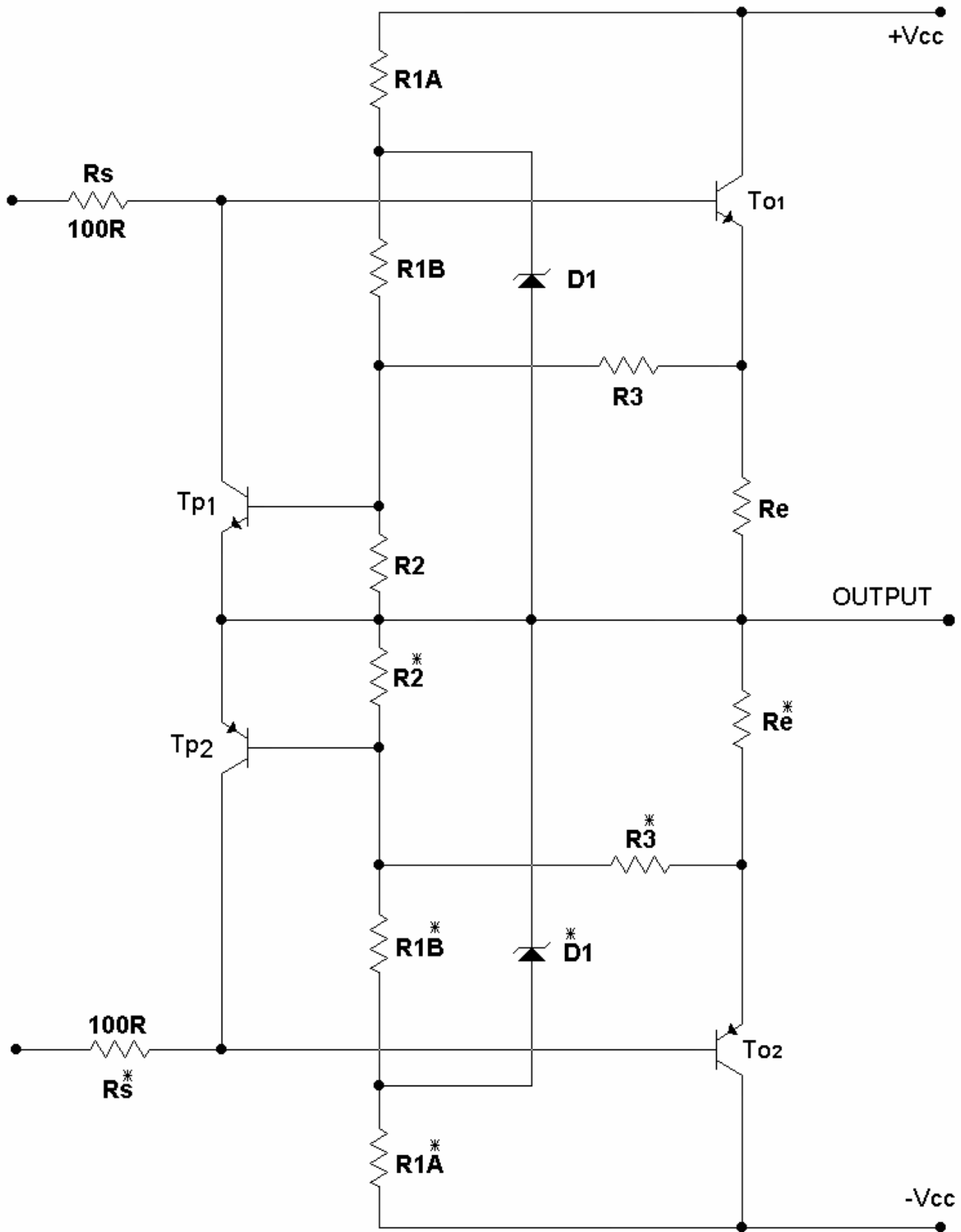
Fig.14. Single slope single breakpoint non-linear foldback protection cell applied to a complementary emitter follower.
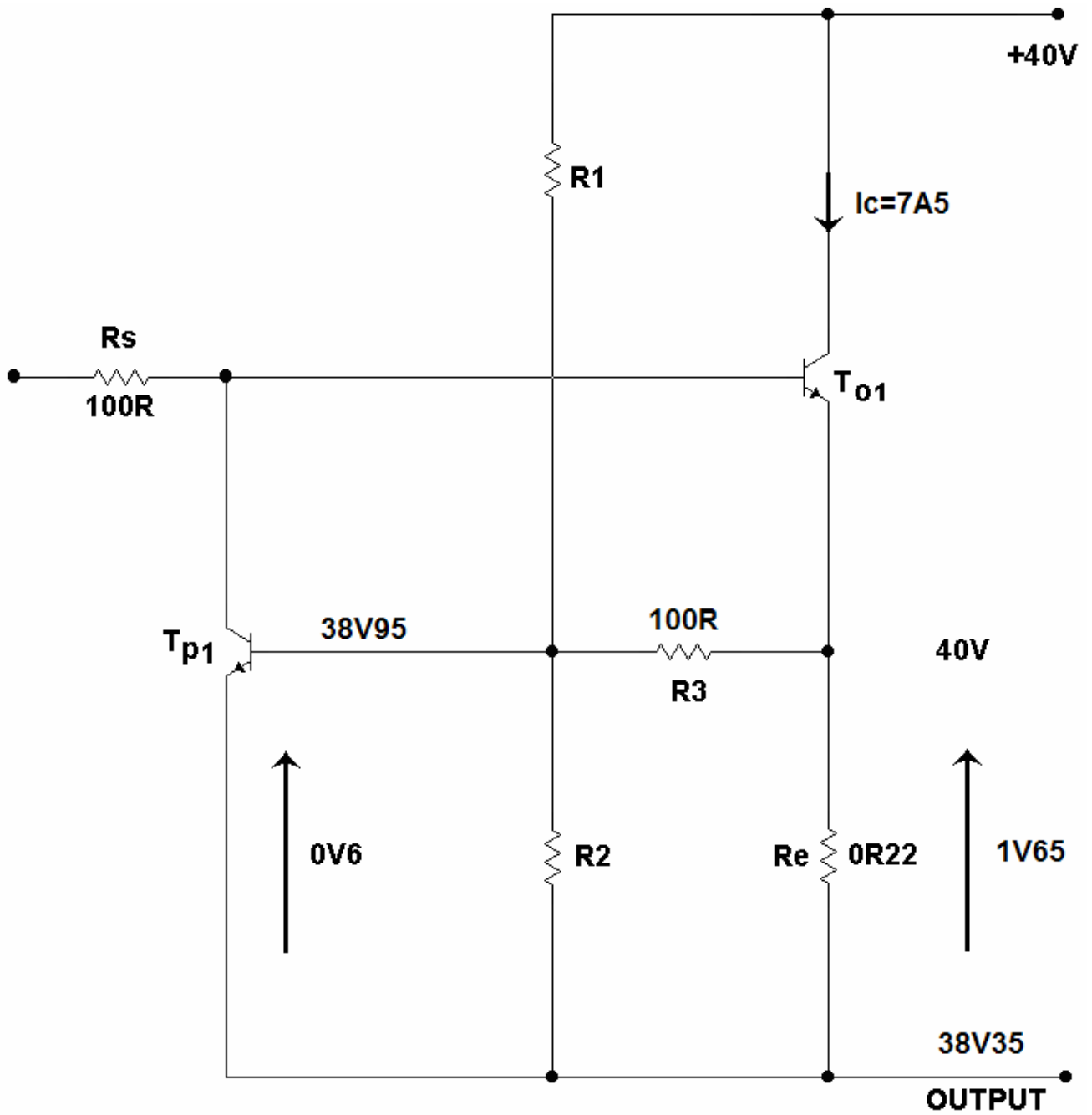
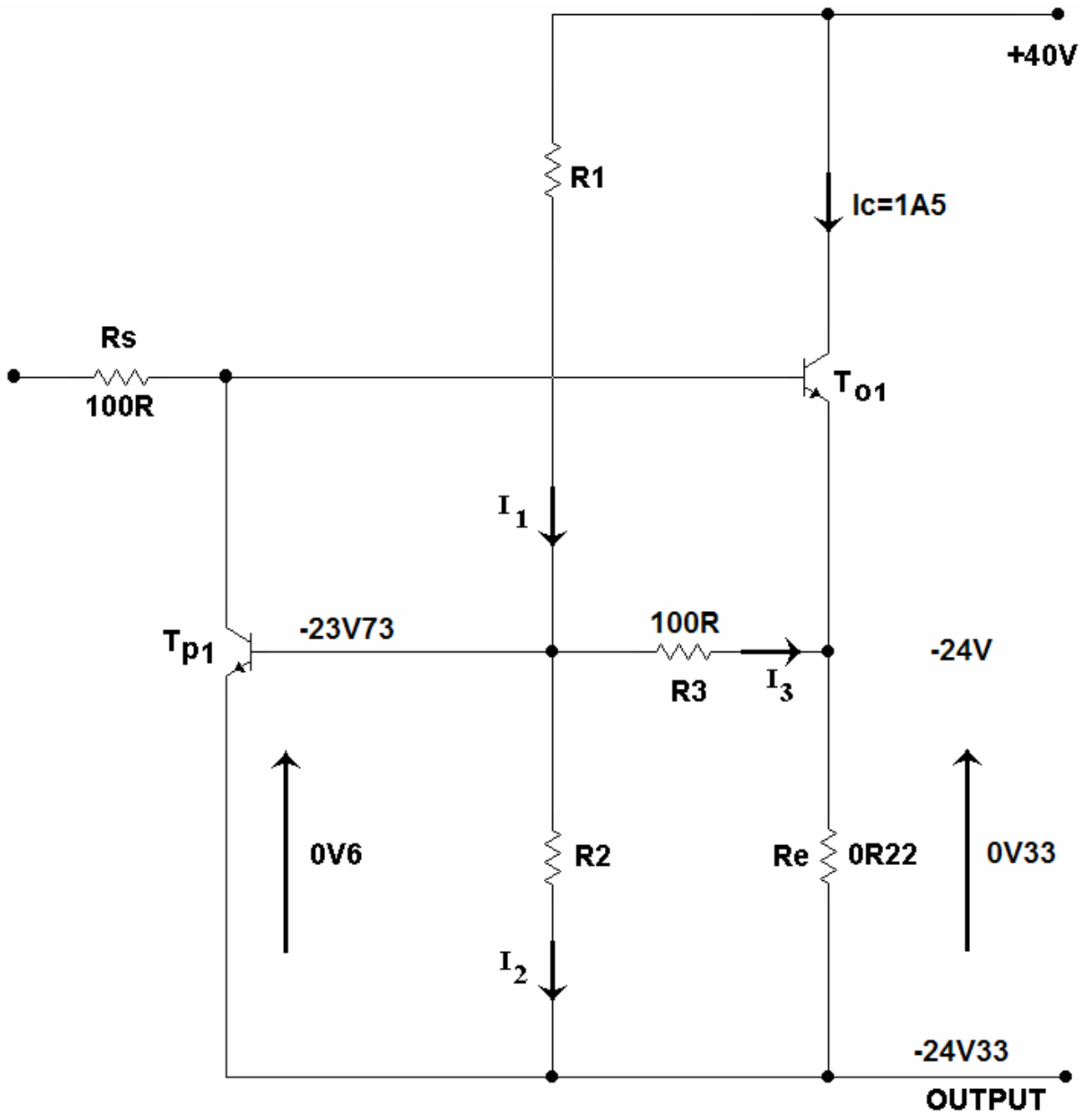**Fig.15. Output conditions at point A on the protection locus of figure 13.**

Fig. 16. Output conditions at point B on the protection locus of figure 13. The contribution of I_3 to the current in Re is negligible.
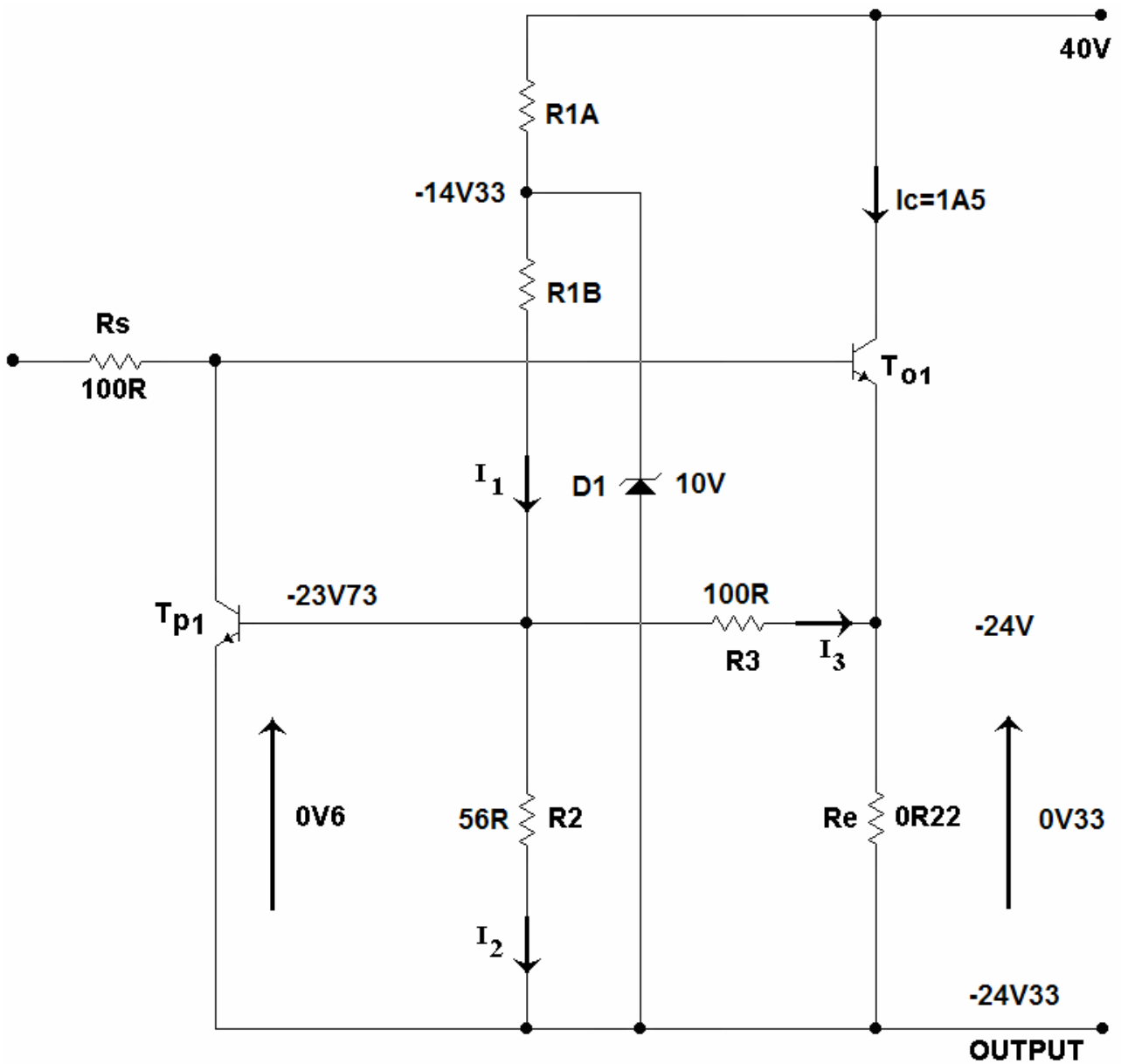
Fig. 17. Output conditions at point B on the protection locus of figure 13 with D1 in situ and R1 split into two. The contribution of I_3 to the current in Re is deemed negligible.

The circuits of **figures 18** and **19** are frequently used[5,19,21] to realise single slope single breakpoint non-linear foldback protection. The small signal diode in **figure 18** is used to establish the flat portion of the locus. Unfortunately simulation reveals that this arrangement gives a soft and grossly ill-defined breakpoint.

Alternatively the small signal diode (**fig. 19**) is used to effect a single slope single breakpoint regime by means of a simple voltage polarity-dependent divider[23]. However, this scheme (beloved of North American manufacturers) is unsatisfactory with respect to flexibility in breakpoint placement. This is because diode commutation can only occur at $v_{out} \approx 0V$ (i.e. $v_{ce} \approx |V_{cc}|$) so that the nominally zero-slope portion of the locus is solely defined by the voltage drop across **Re** being equal to the protection transistor's base-emitter voltage.

The locus of **figure 21** requires a nominal **Re**=0R47; this more than doubles gain-step distortion[11,pg.256.] generated by a class-AB output stage compared to the circuit of **figure 14**, for which **Re**=0R22. A smaller value of **Re** cannot be employed as this would result in a commensurate and necessarily unsafe vertical displacement of segment **BC**. Thus, segment **BC** is fixed for $|\mathbf{V_{cc}}| = 40\mathbf{V}$, and gives even more inefficient SOA usage in the crucial $|V_{cc}| \leq v_{ce} < 2|V_{cc}|$ region than the compromised single slope linear foldback arrangement of **figure 5**.

Further, using a fixed reference voltage (zero volts in this case), independent of the floating collector-emitter voltage v_{ce}, as the basis for SOA protection is rather optimistic as it presumes equally invariant supply rails that do not sag under load. For example, a nominal 40V supply rail that sags by 5V under load would effect a 5V horizontal displacement of segment **AB** to **DE** (**fig. 21**). Conversely, a primary supply surge could cause a potentially disastrous horizontal translocation along **BC** of segment **AB** into and perhaps well beyond the transistor's SOA limits

Since the diodes in **figure 19** are, in theory, never forward biased simultaneously, the modification in **figure 20** is often adopted[18] in what may at first appear to be an elegant simplification. The excision of one of the resistors in this fashion is, alas, a false economy at best, as the performance of the circuit is now significantly compromised by the finite reverse recovery time of the diodes, with minority carrier storage causing the diodes to conduct briefly when reverse biased. This causes minute intermittent zero-crossing oscillation at the output, which may easily be misdiagnosed as a class-B crossover anomaly.

Since segment **BC** is established by merely selecting **Re**=0R47, only point **A** on locus **ABC** (**fig. 21**) is required to obtain a solution. Let $\mathbf{R_1} = 220\mathbf{R}$ and $\mathbf{V_{cc}} = 40\mathbf{V}$ (**fig. 22**):

$$\mathbf{I_2} \approx \mathbf{I_1}$$

Where

$$\mathbf{I_1} = (40 - 34.02)/220\mathbf{R} \approx 27.18\mathbf{mA}$$

With $\mathbf{V_f} \approx 0\mathbf{V}7$ at 27mA

$$\mathbf{R_2} = \mathbf{V_{R2}}/\mathbf{I_2} \approx (34.02 - 0.7)/27.18\mathbf{mA} \approx 1\mathbf{K}2$$

The circuit in **figure 19** is capable of modest improvement however, and therefore merits closer scrutiny.
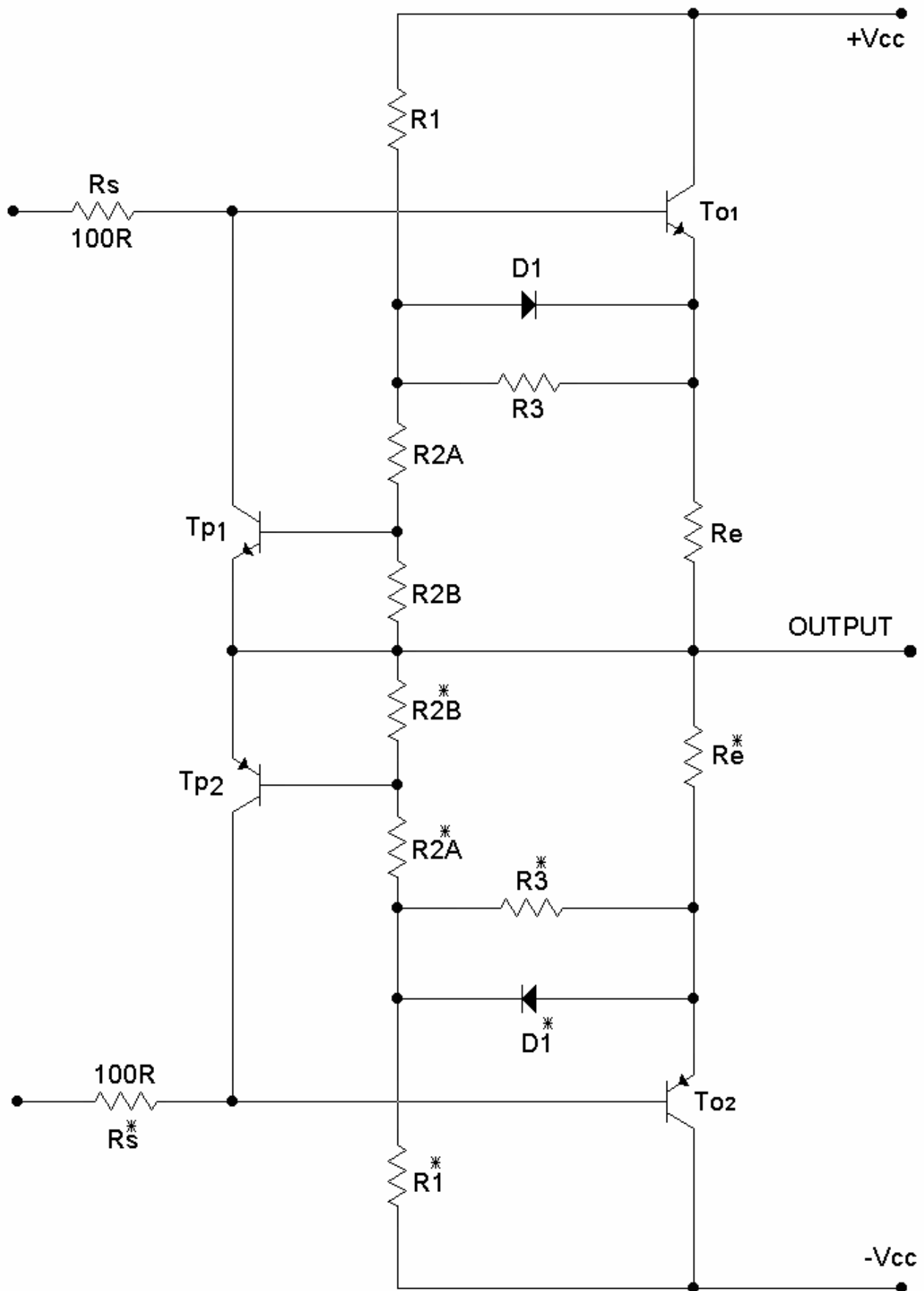
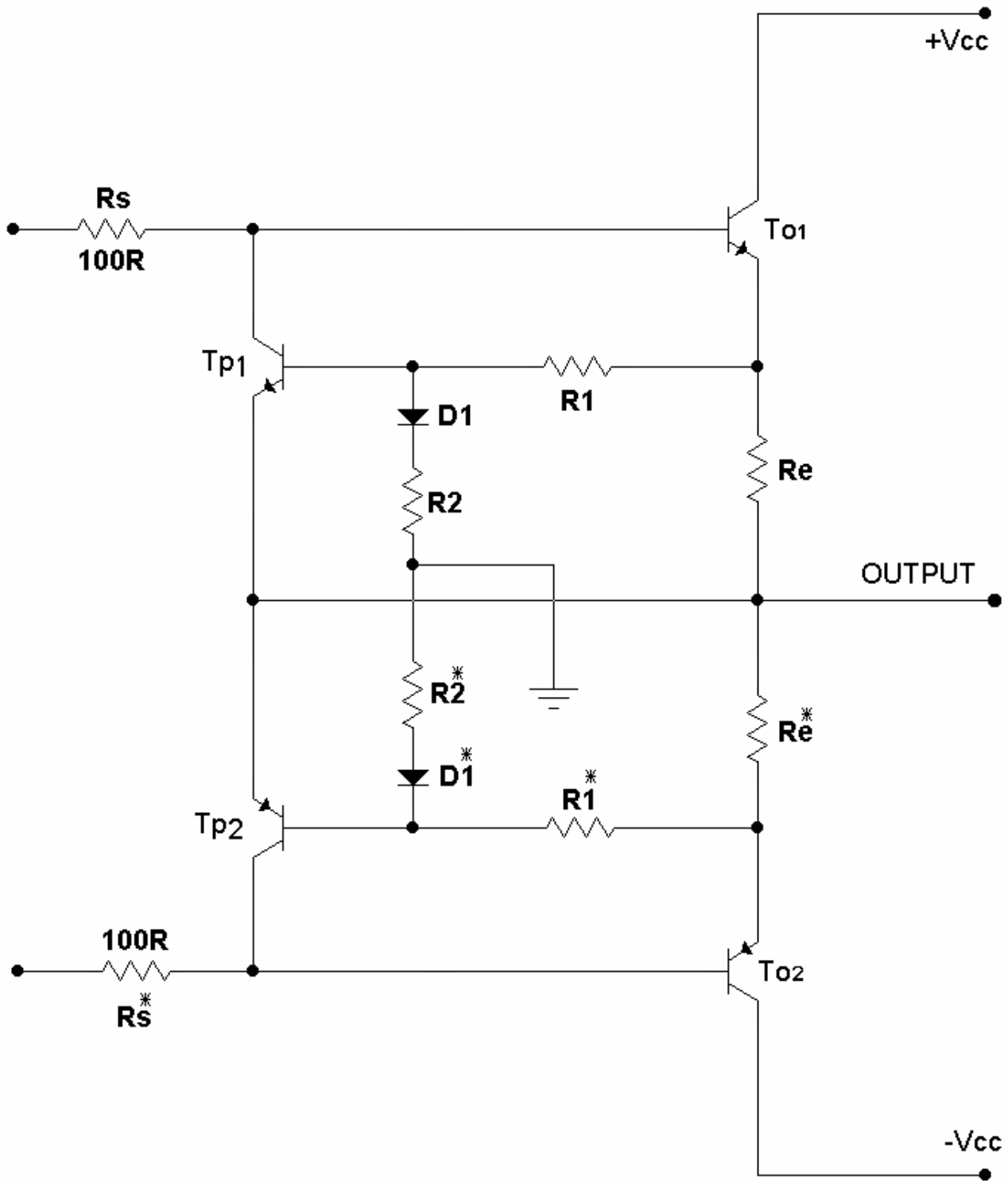**Fig. 18. Small signal diode-based single slope single breakpoint non-linear foldback limiter.**

Fig. 19. Polarity-dependent voltage divider used to introduce a single breakpoint in an otherwise linear-slope locus.
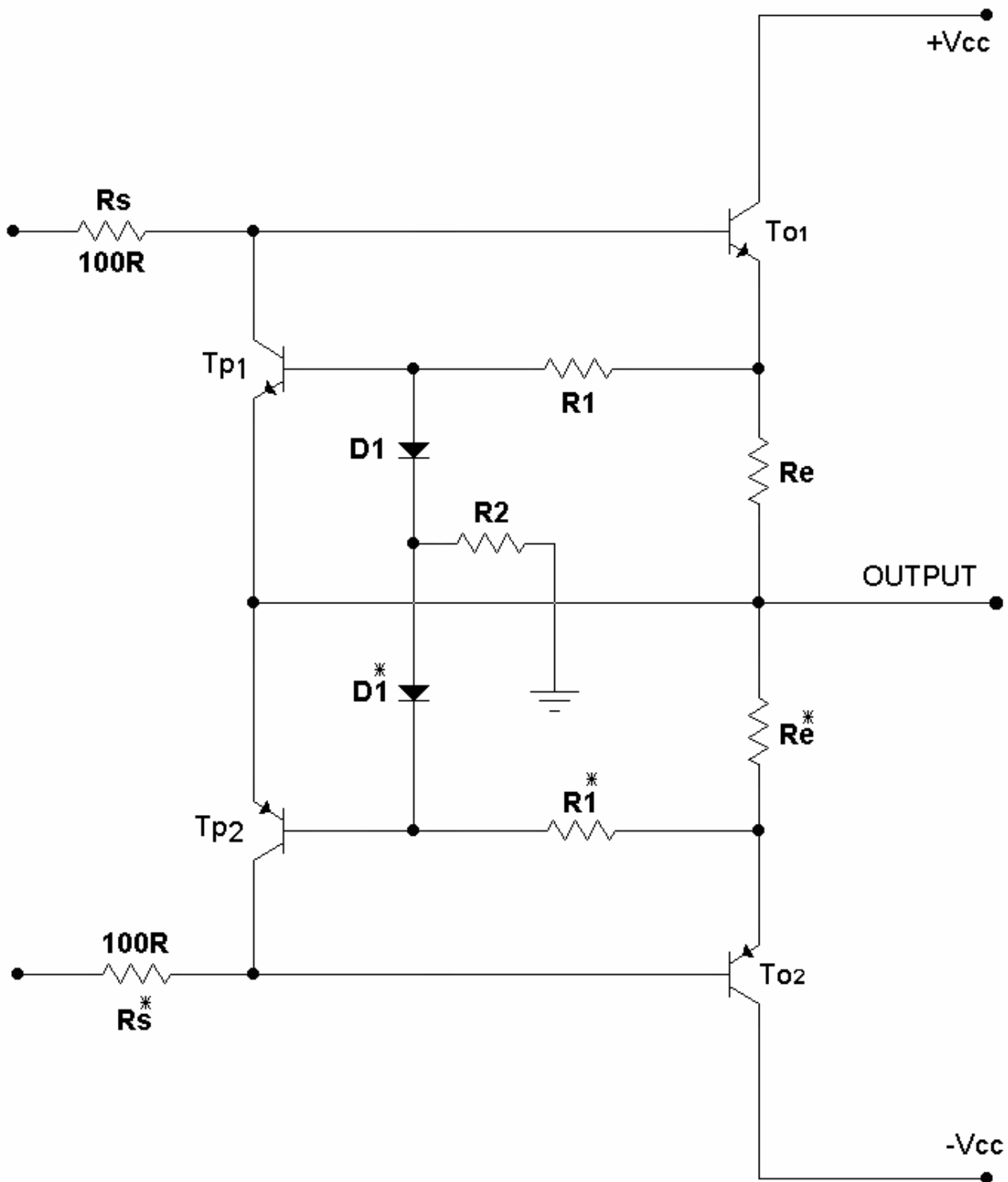
Fig. 20. A common variation in figure 18 which gives inferior performance due to the finite reverse recovery time of the diodes.
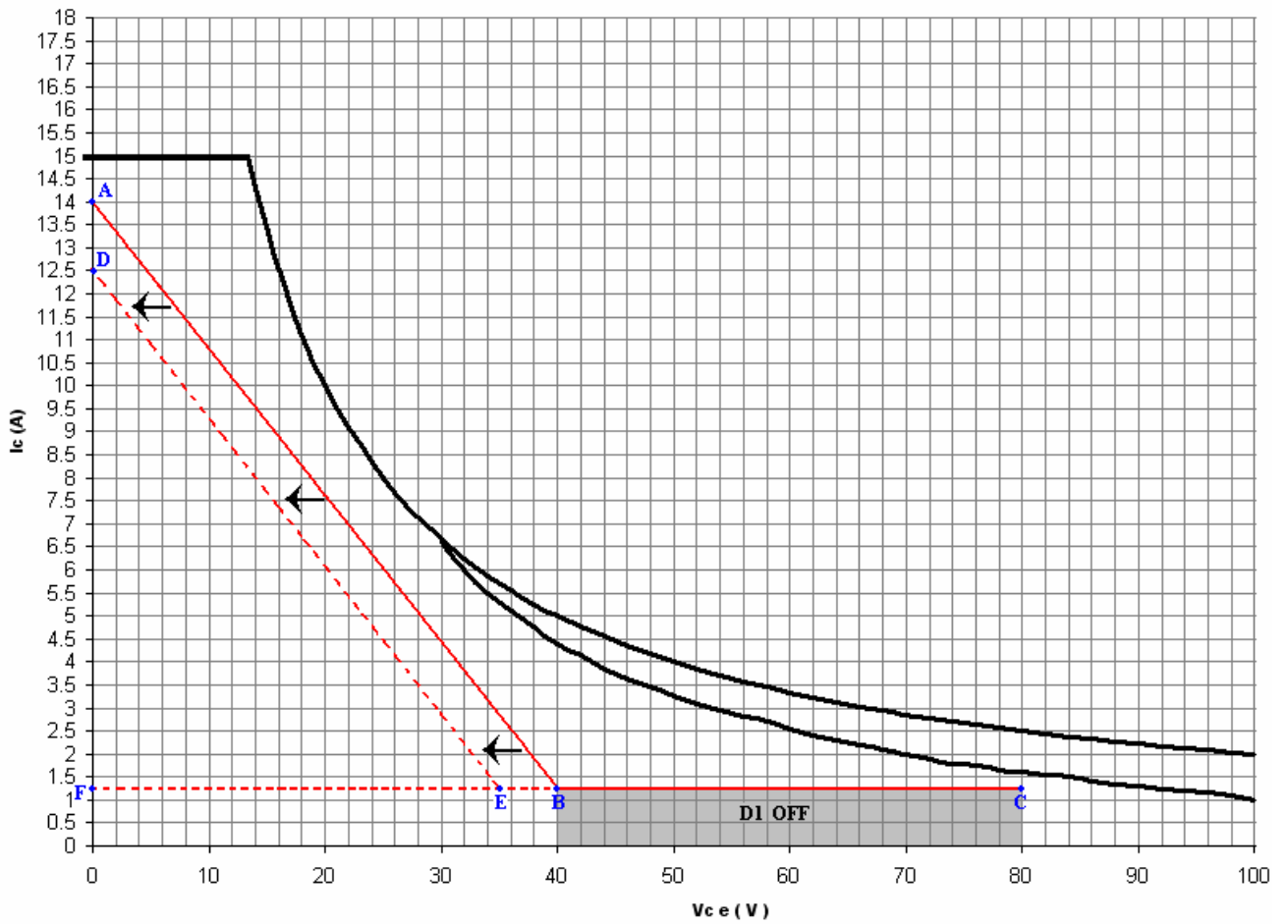
Fig. 21. Single slope single breakpoint non-linear protection locus described by network of figure 19. A notional 5V drop in the supply rail causes an equivalent horizontal translation of segment AB to DE.
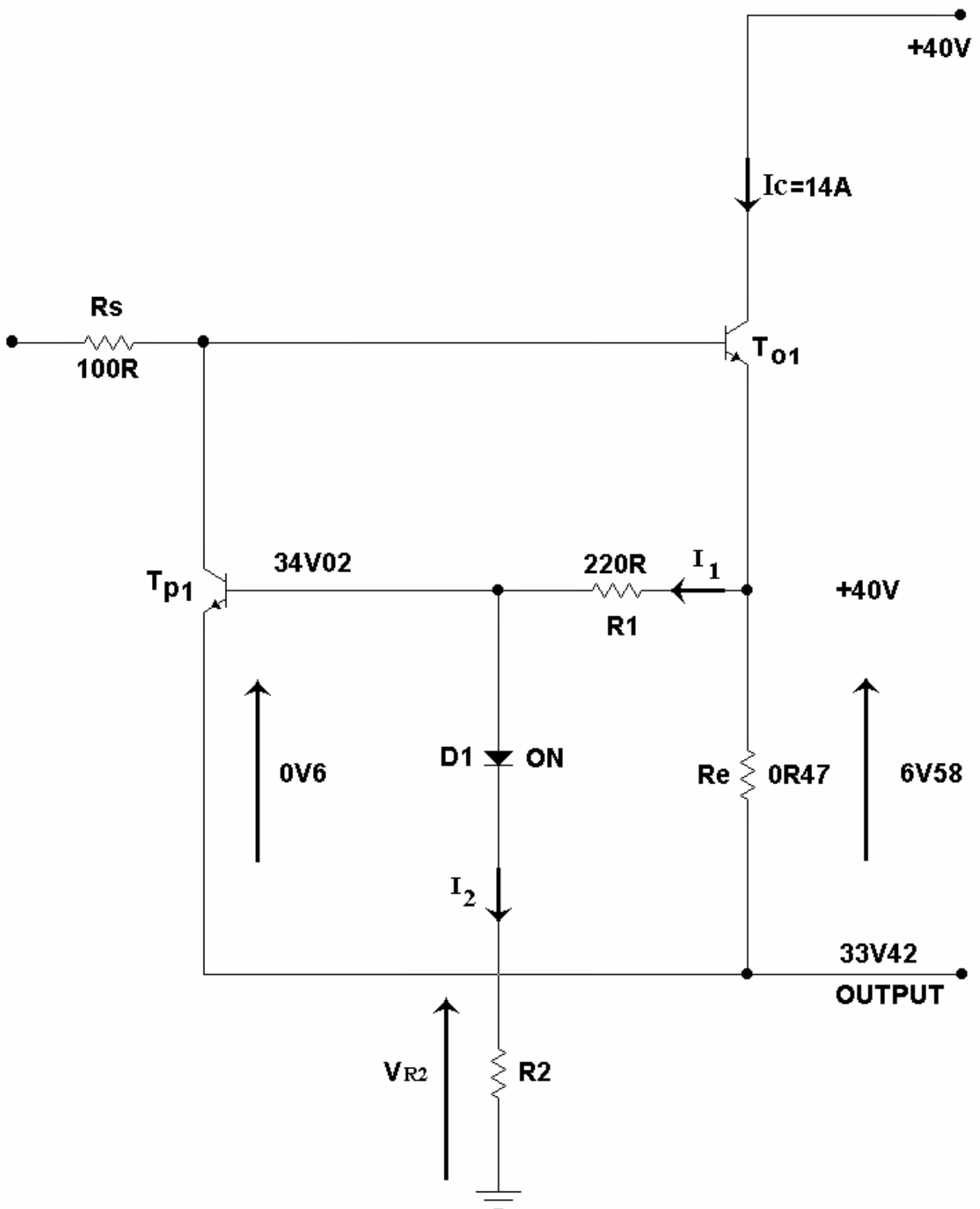
Fig. 22. Output conditions at point A on the protection locus of figure 21.

This scheme can be made more efficient (**fig. 23**) by changing the voltage divider's fixed reference voltage from zero to two arbitrary voltages $\mathbf{V_{Ref1}}$ and $\mathbf{V_{Ref2}}$ of equal magnitude but opposite polarity, such that $\left\{0\mathbf{V} < \left(\left|\mathbf{V_{Ref1}}\right| = \left|\mathbf{V_{Ref2}}\right|\right) < \left|\mathbf{V_{cc}}\right|\right\}$; nominal 40V rails are assumed. This enhances the flexibility of the circuit, as the breakpoint can now be freely located along **CF** (**fig. 24**) giving rise to a more efficient locus **BEF**.

The reference voltage is equal in magnitude to the output voltage $\mathbf{v_{out}}$ at the breakpoint in locus **BEF** (**fig. 25**); i.e. $\left|\mathbf{V_{Ref1}}\right| = \left|\mathbf{V_{Ref2}}\right| = \left|\mathbf{V_{out}}\right|_{\mathbf{V_{ce}}=60\mathbf{V}} = 20\mathbf{V}6$, with $\mathbf{V_{Ref1}} = -20\mathbf{V}6$ and $\mathbf{V_{Ref2}} = +20\mathbf{V}6$; this calls for a nominal 60V6 zener diode. It is recommended that the required voltage drop be realized with multiple low-voltage devices $\left(6\mathbf{V} \leq \mathbf{V_Z} \leq 12\mathbf{V}\right)$ as these possess a significantly lower series impedance than may be obtained with single device [22]. In practice, therefore, each of $\mathbf{Z_1}$ and $\mathbf{Z_2}$ may, for example, consist of six **On Semiconductor® 1N5240B** 10V zeners in series with a forward biased **1N4448** diode, all biased at a nominal 25mA by $\mathbf{R_Z}$ and $\mathbf{R_Z^*}$.

Crucially, in **figure 23**, the cathode of diode $\mathbf{Z_1}$ is connected directly to $+\mathbf{V_{cc}}$, effectively bootstraping $\mathbf{V_{Ref1}}$ to the supply rail, so that any anomalies on the supply are directly impressed on the reference voltage. This effectively eliminates the potentially fatal tendency of segment **BE** to migrate back and forth along **CF** with non-ideal supply rail fluctuations. Similarly, $\mathbf{V_{Ref2}}$ is bootstrapped to the supply rail by connecting the anode of $\mathbf{Z_2}$ to $-\mathbf{V_{cc}}$.

Let $\mathbf{R_1} = 220\mathbf{R}$ and $\left|\pm\mathbf{V_{cc}}\right| = 40\mathbf{V}$ (**fig. 26**):

$$\mathbf{I_2} \approx \mathbf{I_1}$$

Where

$$\mathbf{I_1} = \left(40 - 35.9\right)/220\mathbf{R} \approx 18.64\mathbf{mA}$$

With $\mathbf{V_f} \approx 0\mathbf{V}7$ at 20mA,

$$\mathbf{R_2} = \mathbf{V_{R2}}/\mathbf{I_2} \approx \left(35.9 - 0.7 + 20.6\right)/18.64\mathbf{mA} \approx 3\mathbf{K}0$$

The dependence of segment **EF** (**fig. 24**) on the value of **Re** for the circuit in **figure 23** remains its achilles' heel. The singular advantage of the network of **figure 14** is that it permits the arbitrary location of a breakpoint in the protection locus without undue reference to the value of **Re**.

Moreover because the entire network of **figure 14** floats between the output and supply rails the position of the locus in the SOA remains resolutely invariant in the face of deviant power supply behaviour, without recourse to a bootstrapped voltage reference.
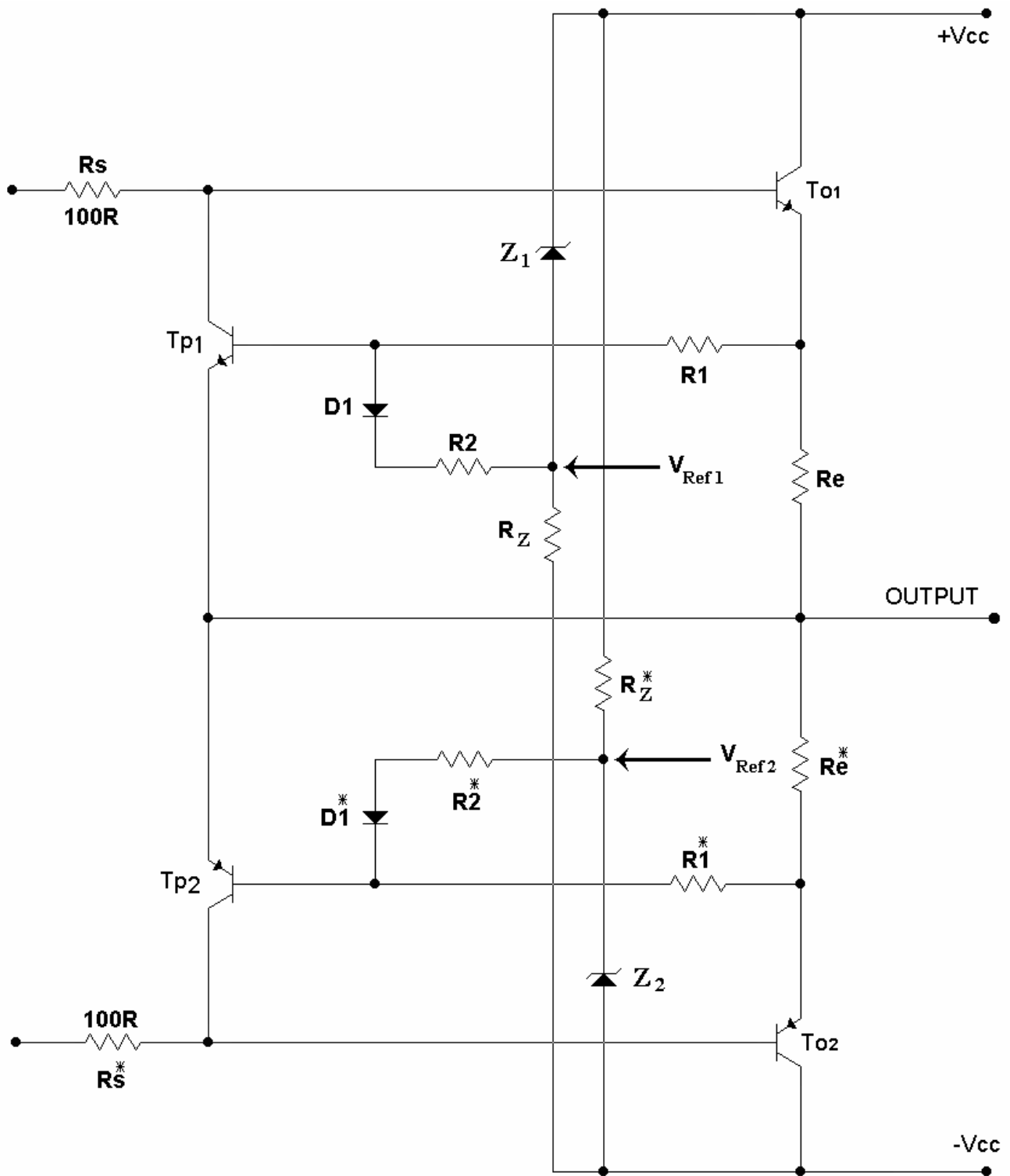
Fig. 23. The use of arbitrary voltage references of equal magnitude makes for a worthwhile improvement in efficiency compared to the arrangement of figure 19.
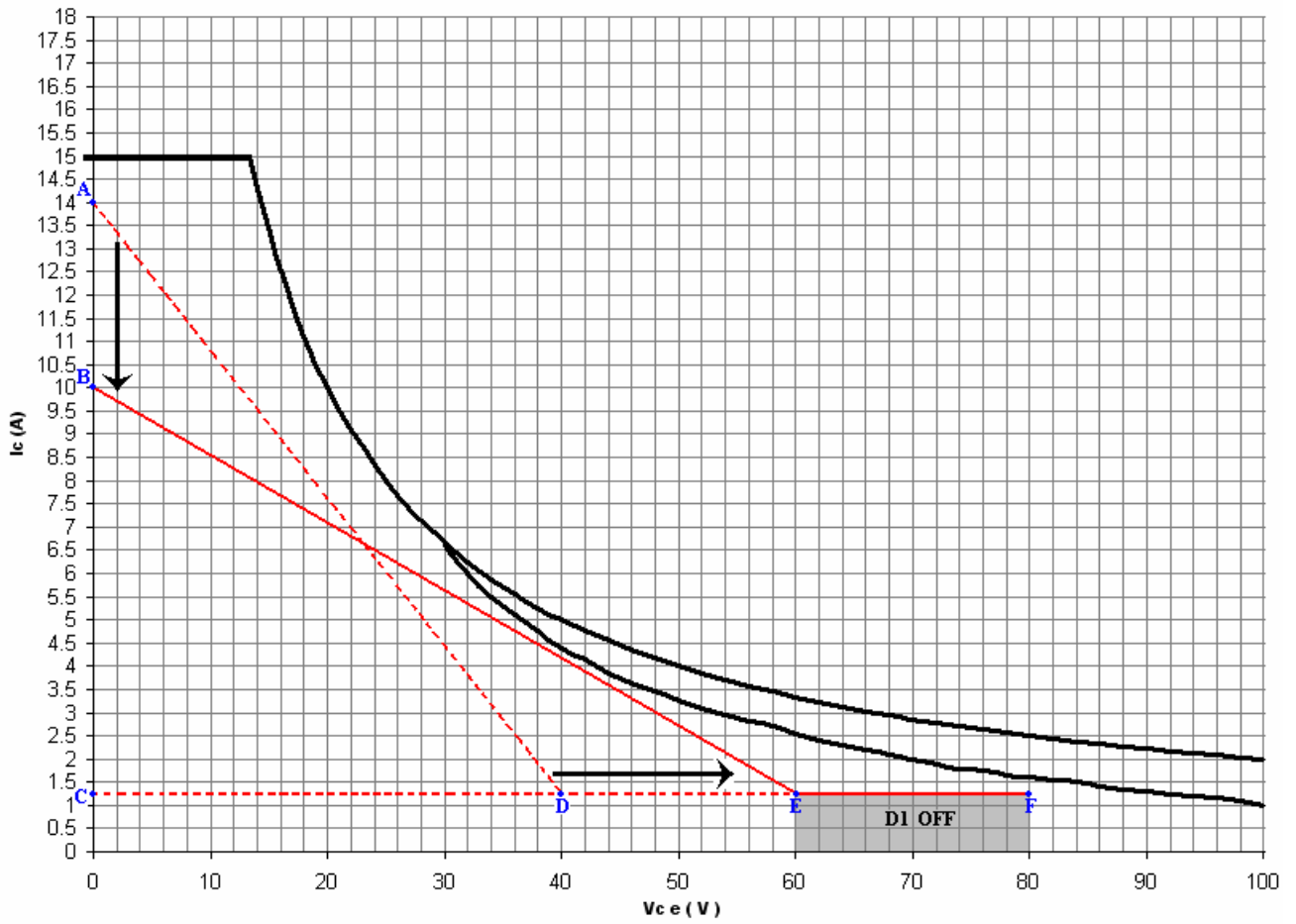
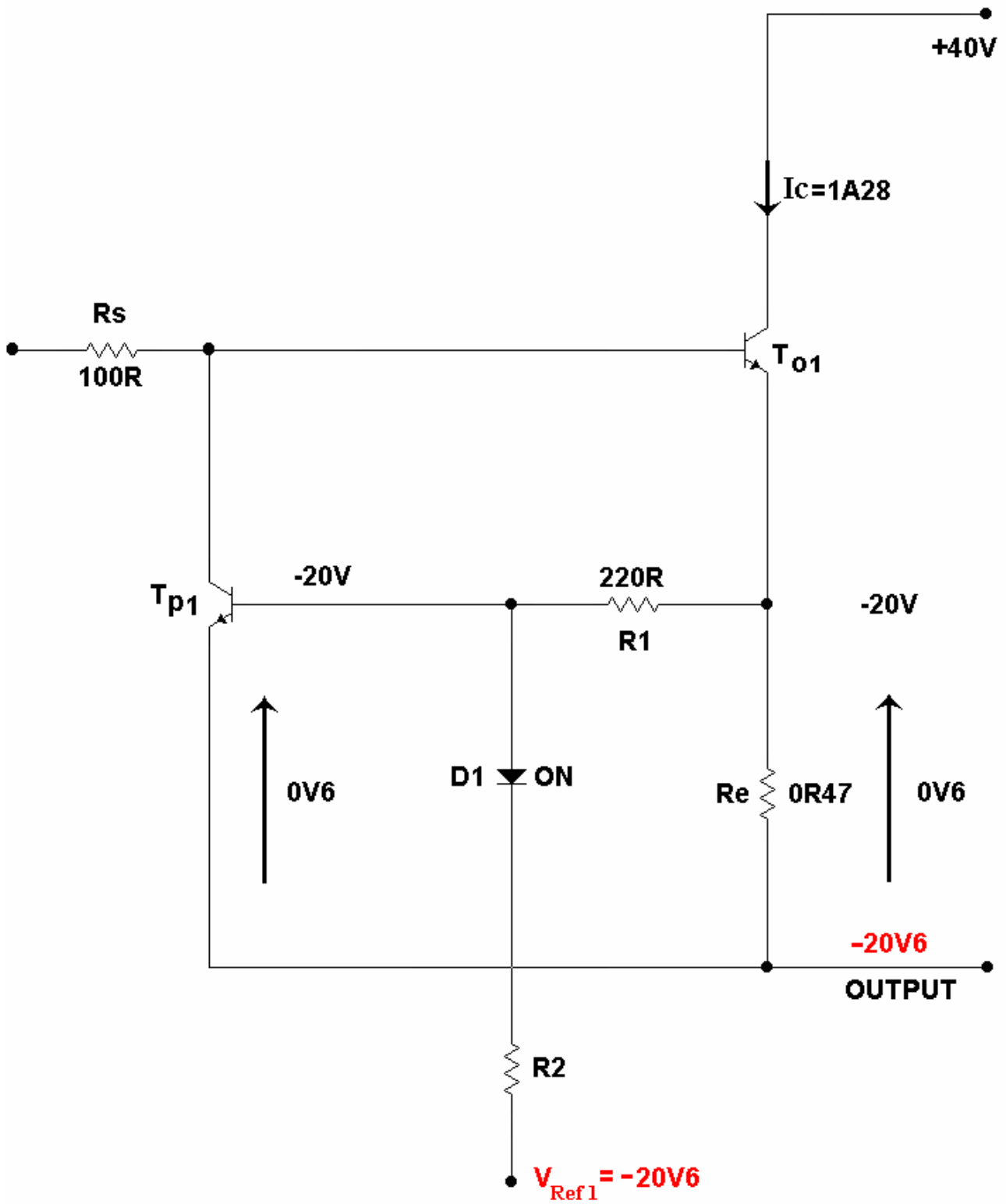**Fig. 24. Improved single slope single breakpoint locus BEF realised by using an arbitrary voltage reference.**

Fig. 25. The reference voltage is made equal in magnitude to the output voltage at the breakpoint (i.e. when Vce=60V); the diode is then at the threshold of conduction.
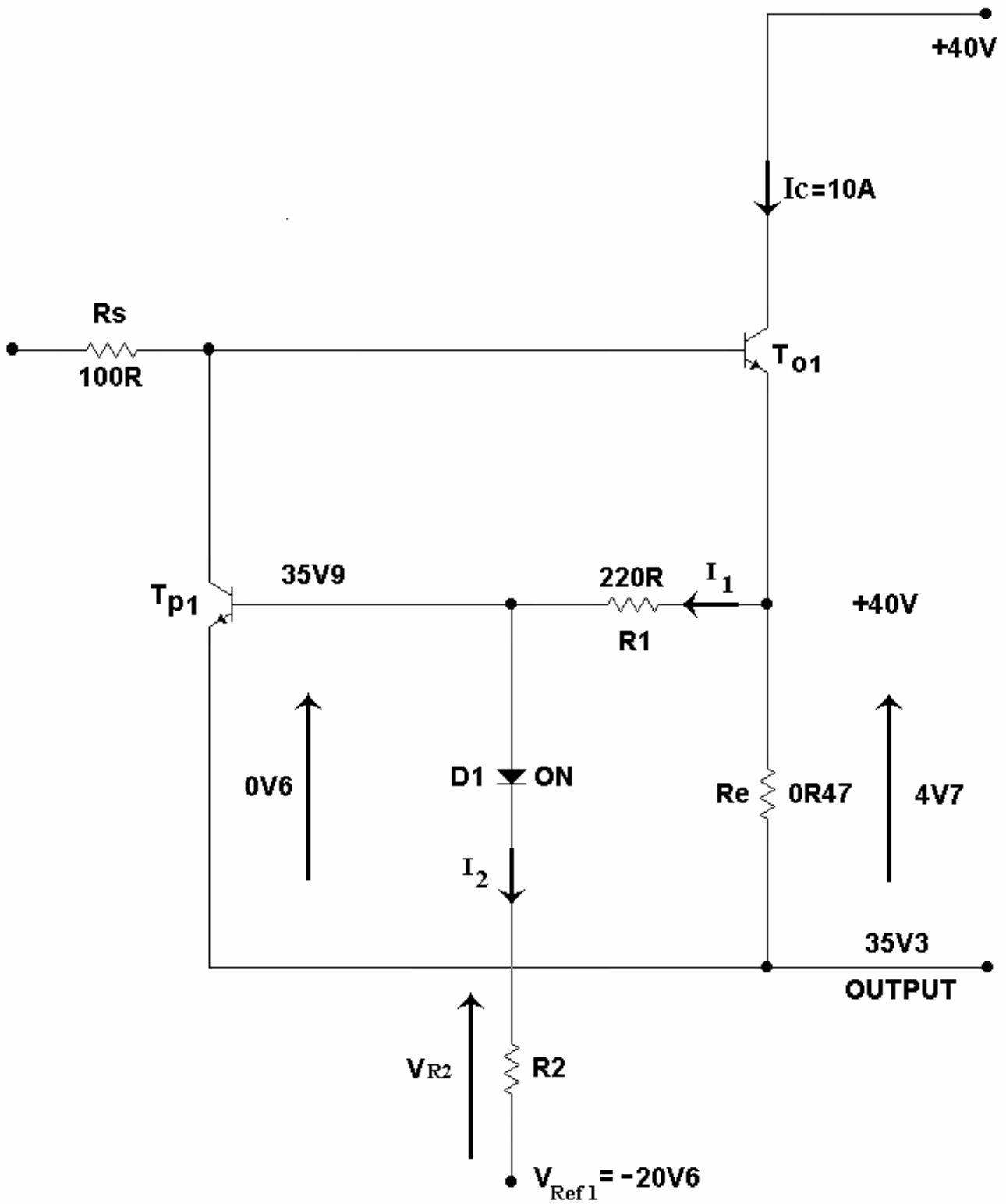
Fig. 26. Output conditions at point B on the protection locus in figure 24.

Dual slope single breakpoint non-linear foldback limiting

Introducing a resistor R_d in series with diode D_1 (**fig. 28**) causes the voltage drop across the series combination to increase linearly above the diode's conduction threshold. This effectively induces a net linear increase in potential across resistors R_{1B} and R_2 for i_C and v_{ce} combinations in the $v_{ce} \geq 36V$ region of the SOA (**fig. 27**). The gradient of segment **BD** in the protection locus can now be varied linearly[11] with R_d about point **B** which gives vastly greater flexibility with regard to optimal placement of the breakpoint.
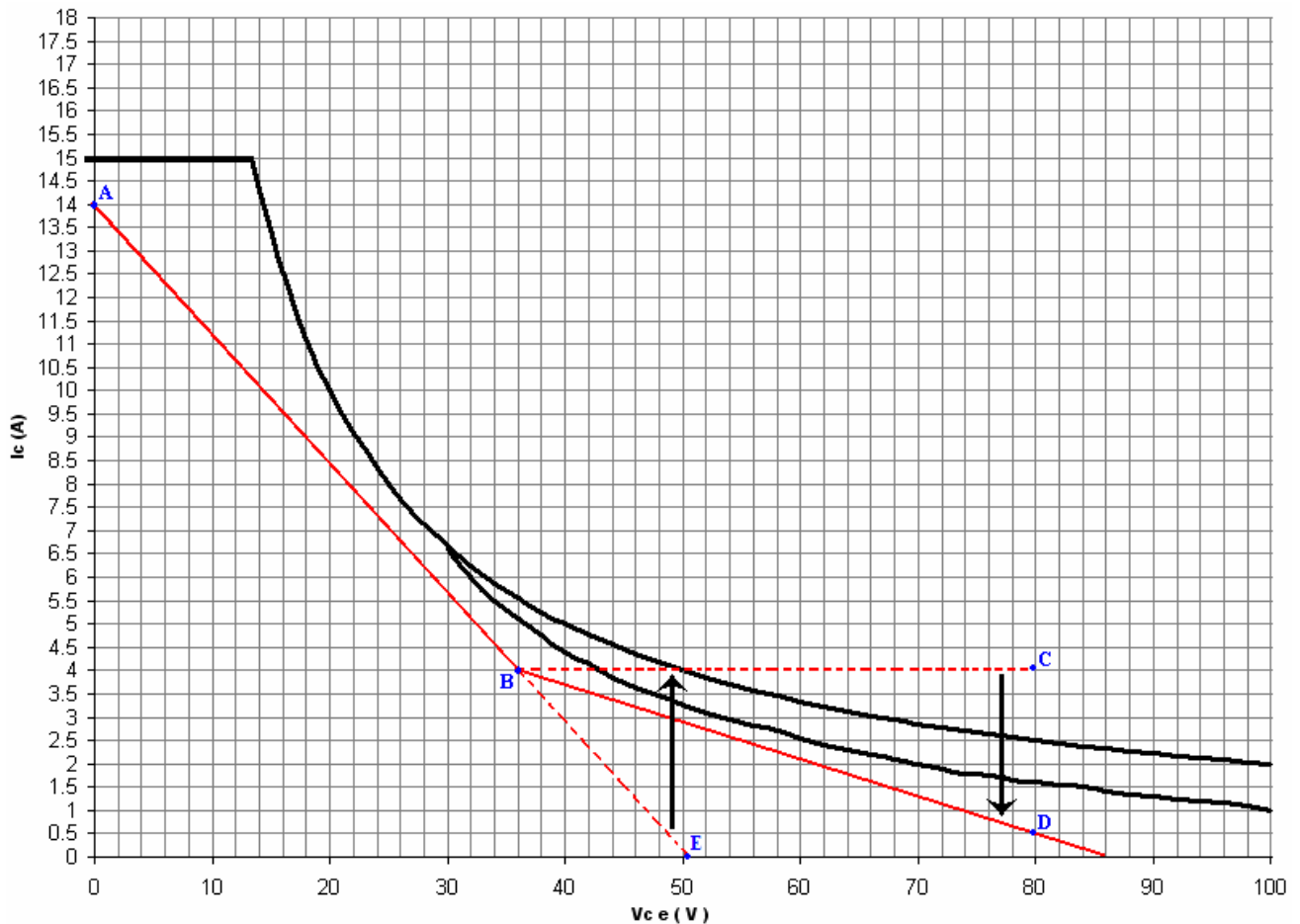

Fig.27. Dual slope single breakpoint non-linear foldback protection locus.

As is the case with single slope linear foldback SOA limiting, segment **BD** must intersect the SOA's **Vce** axis at a value greater than the sum of the moduli of the supply rails if spurious limiter activation is to be prevented. Available current per output pair at $\mathbf{Vce} \approx 4V$ is further increased to 12A8 compared to 7A1 for the locus of **figure 13**.
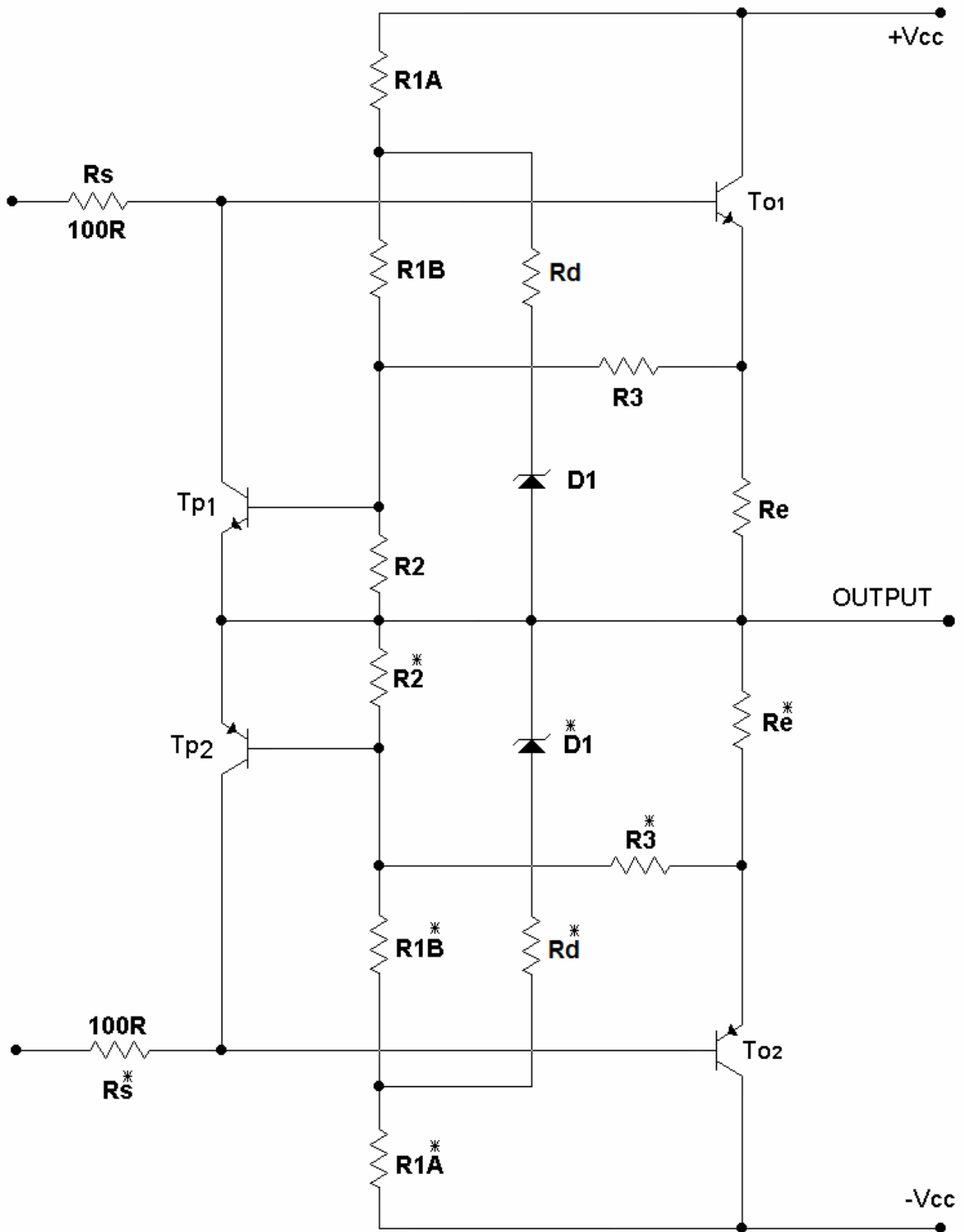
Fig.28. Dual slope single breakpoint non-linear foldback limiter.

Initially, as previously established, resistor values are calculated for the single slope segment **ABE** (**fig. 27**) in the absence of the zener diode and resistor R_d. Additionally, resistors R_{1A} and R_{1B} are combined into a single resistor R_1.

Arbitrarily selecting $R_3 = 100R$ and points **A** and **B** where at point **A** $I_c = 14A$, $V_{ce} = 0V$ and at point **B** $I_c = 4A$, $V_{ce} = 36V$, it follows from **figure 29**:

$$0.6 = \frac{3.08 R_2}{R_2 + R_1 100 / (R_1 + 100)} \tag{8}$$

From **figure 30**:

$$I_2 = I_1 + I_3$$

$\Rightarrow$

$$0.6 / R_2 = (40 - 3.72) / R_1 + (4 - 3.72) / 100$$

$\Rightarrow$

$$0.6 = R_2 (36.28 / R_1 - 0.28 / 100) \tag{9}$$

Solving (**8**) and (**9**) simultaneously gives $R_1 \approx 1K5$ and $R_2 \approx 22R7$.

The zener diode (arbitrary $V_Z = 10V$) is now introduced and resistor R_1 split into R_{1A} and R_{1B} (**fig. 31**):

$$I_1 = I_2 - I_3$$

$\Rightarrow$

$$I_1 = \frac{0.6}{22.7} - \frac{(4 - 3.72)}{100} = 23.6 \text{mA}$$

$\Rightarrow$

$$R_{1B} = \frac{(13.12 - 3.72)}{23.6 \text{mA}} = 398R$$

$\Rightarrow$

$$R_{1A} = R_1 - R_{1B} = 1K5 - 398R \approx 1K1$$

Resistor **Rd** is now introduced and its value established by consideration of the circuit conditions at point **D** ($I_c = 0.5A$, $V_{ce} = 79.89V$) on the locus of **figure 27**.

Thus from **figure 32**:

$$\mathbf{I_{1B} = I_2 + I_3}$$

$\Rightarrow$

$$\mathbf{I_{1B}} = \frac{0.6}{22.7} + \frac{(-39.4 + 39.89)}{100} = 31.3\mathbf{mA}$$

$\Rightarrow$

$$\mathbf{V_x} = -39.4 + \mathbf{I_{1B}R_{1B}} \approx -26.9\mathbf{V}$$

$\Rightarrow$

$$\mathbf{I_d = I_{1A} - I_{1B}} = \frac{(40 + 26.9)}{\mathbf{1K1}} - 31.3\mathbf{mA} \approx 27.5\mathbf{mA}$$

$\Rightarrow$

$$\mathbf{R_d} = \frac{(\mathbf{V_x} + 30)}{\mathbf{I_d}} \approx 111\mathbf{R5}$$
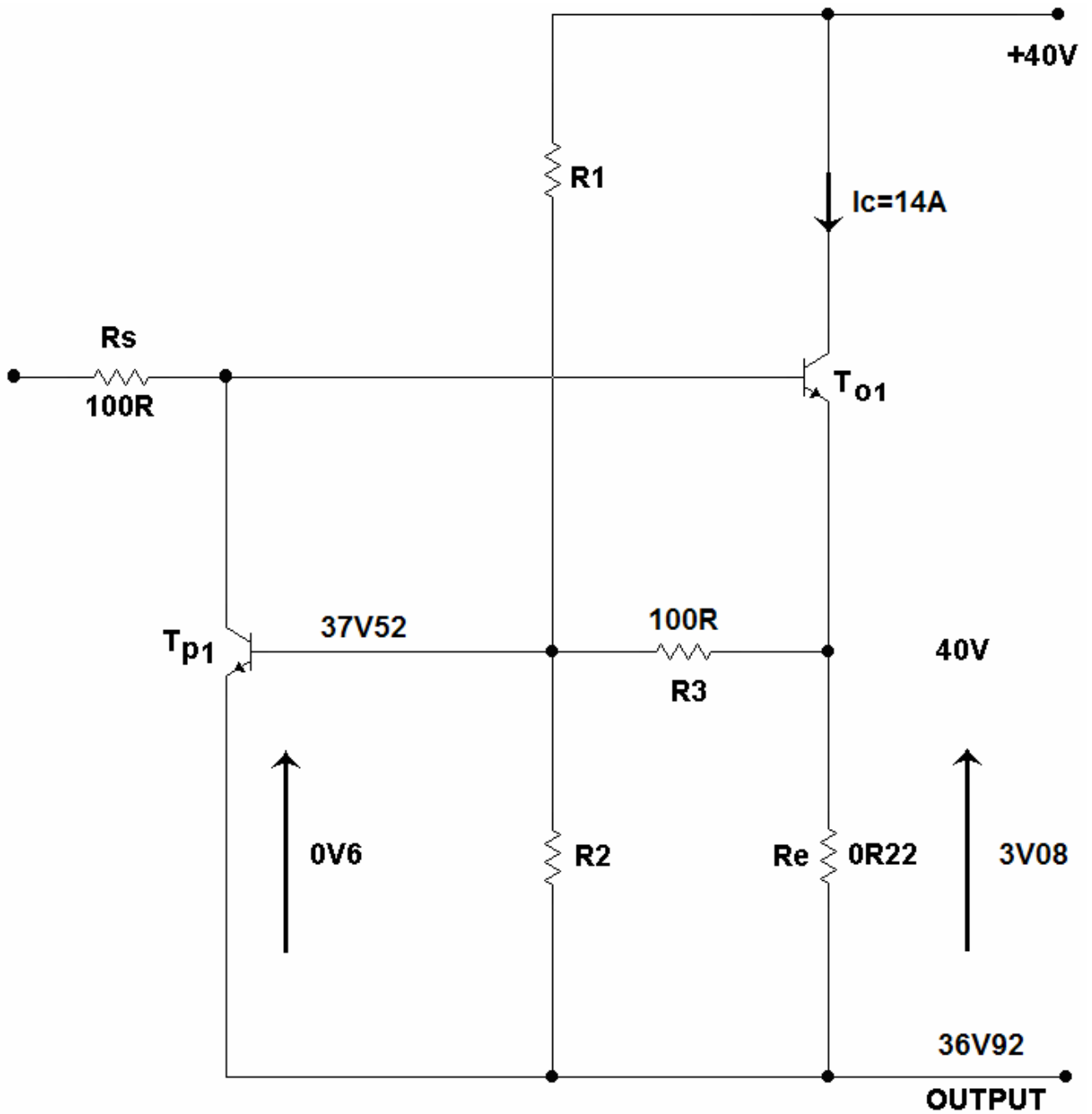
Fig. 29. Output conditions at point A on the protection locus of figure 27 in the absence of the zener diode and resistor Rd.
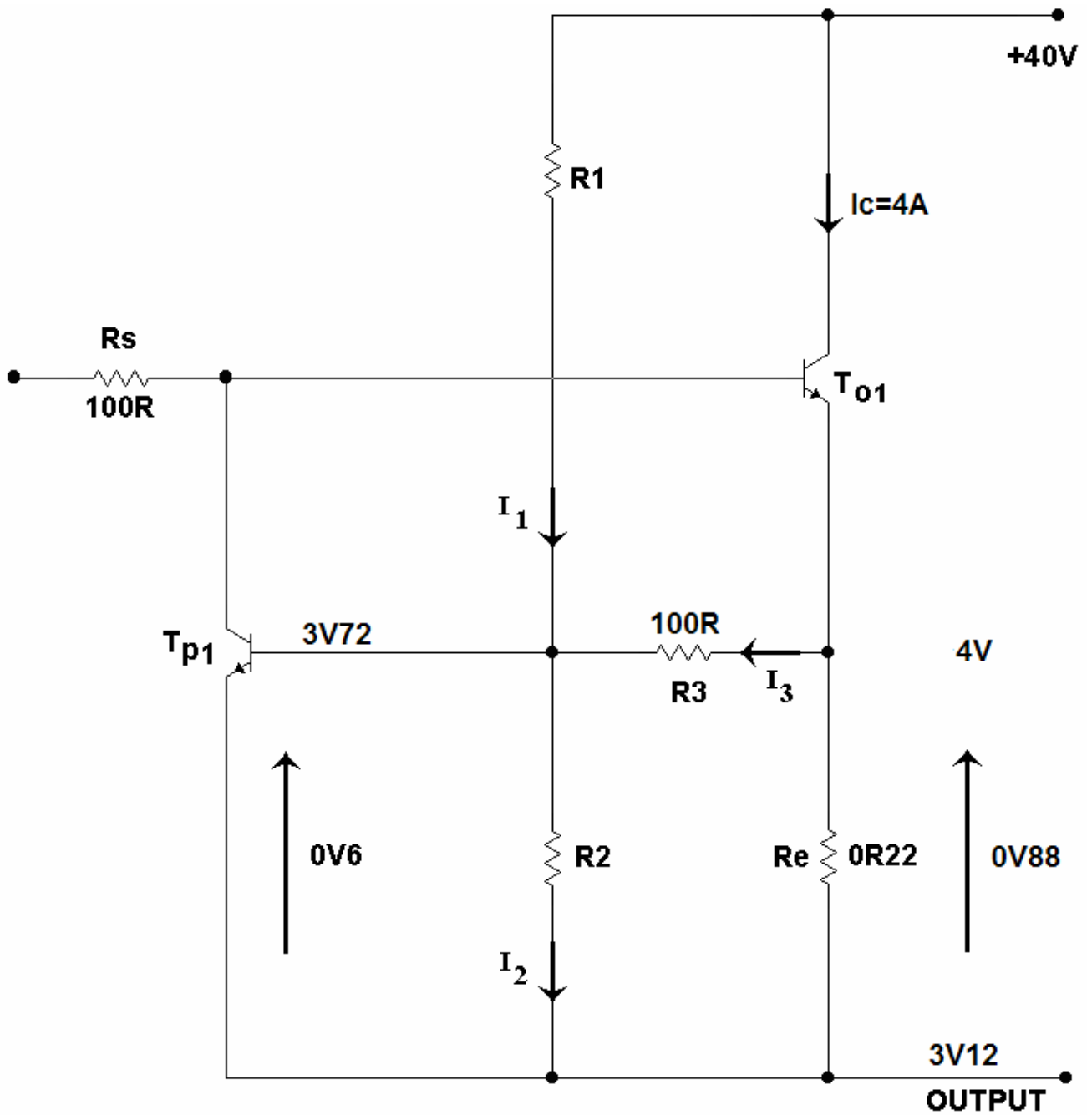
Fig. 30. Output conditions at point B on the locus of figure 27 in the absence of the zener diode and resistor Rd.
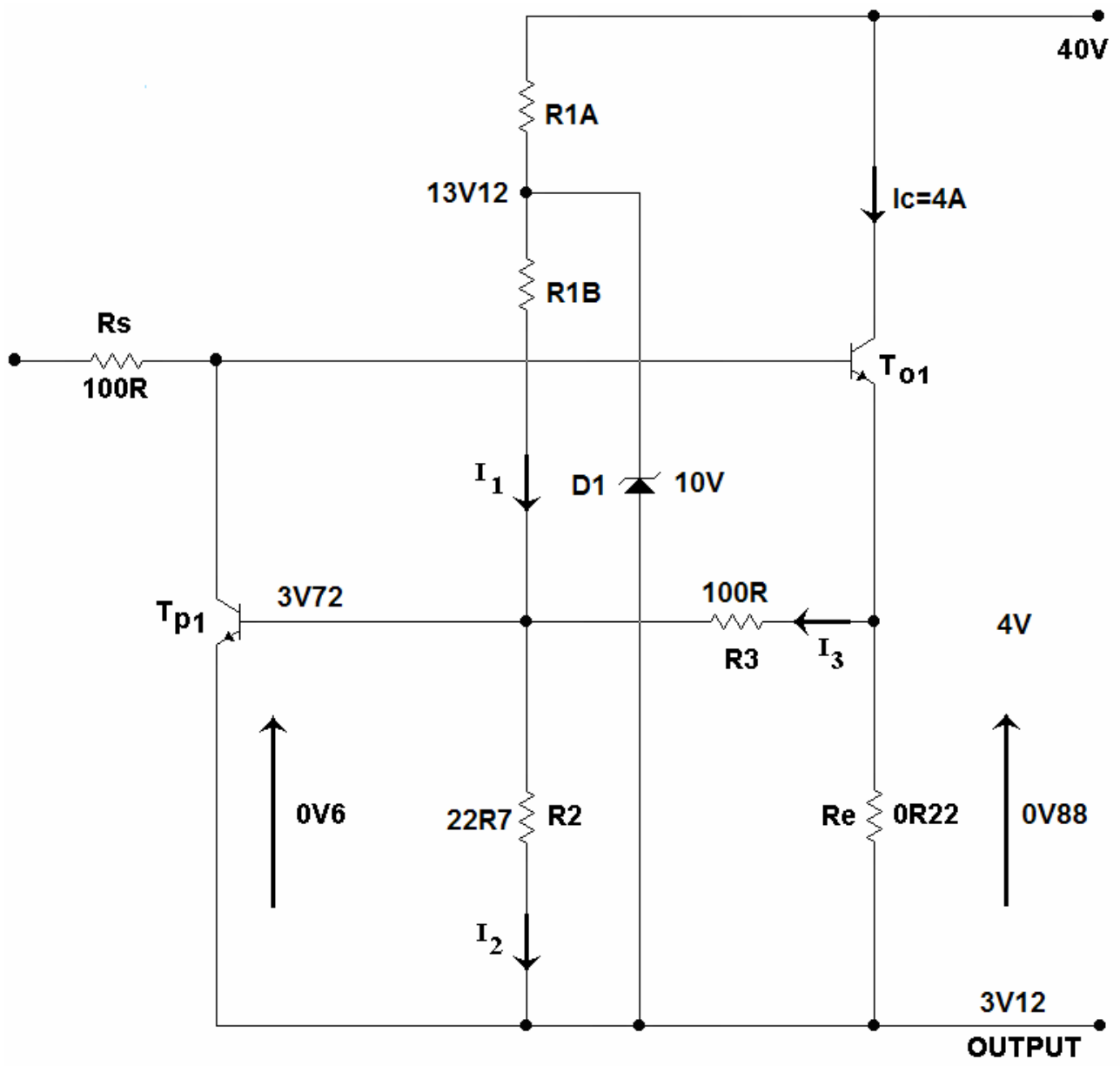
Fig. 31. Output conditions at point B on the locus of figure 27 with the zener diode included and R1 split in two.
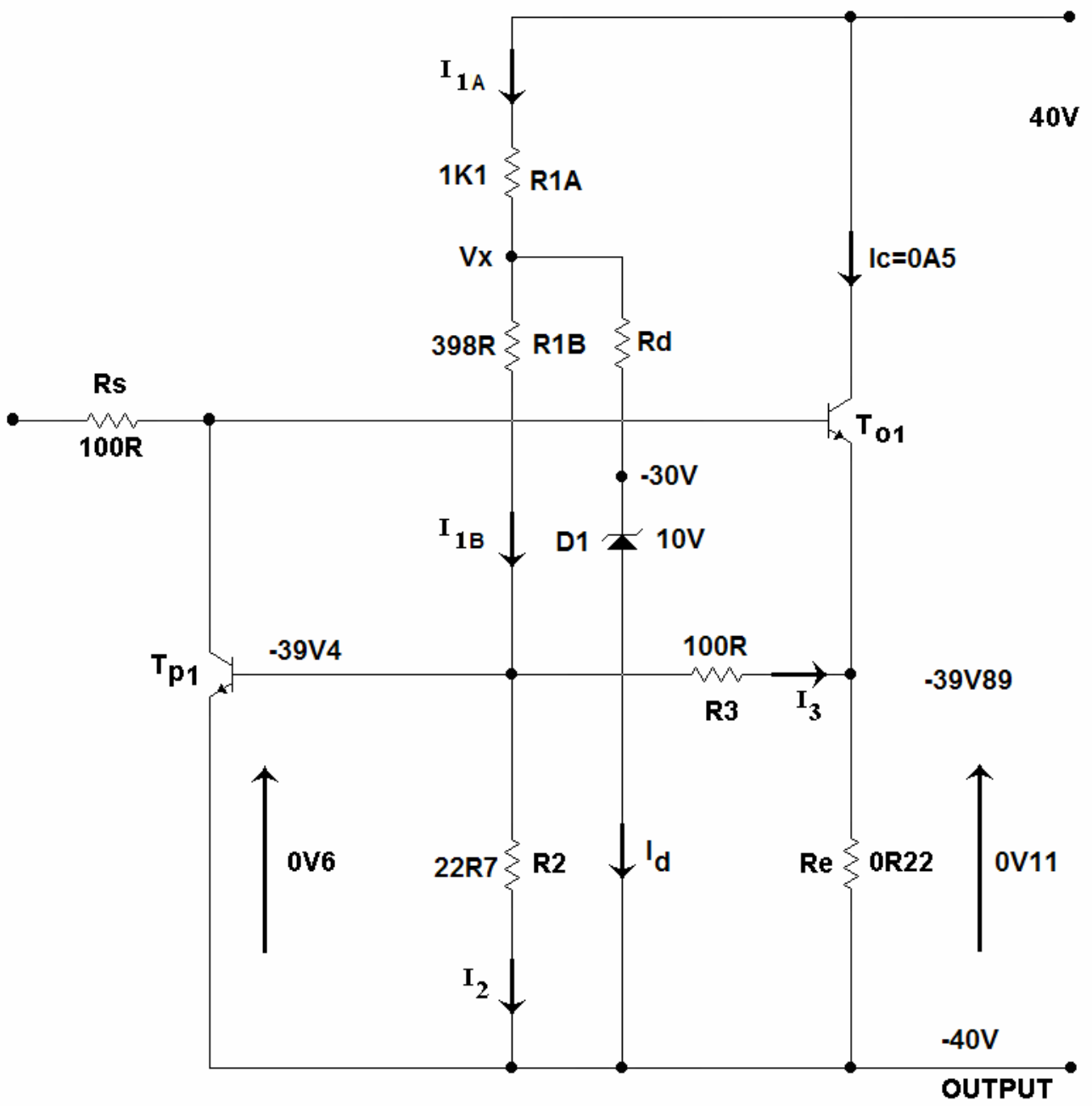
Fig. 32. Output conditions at point D on the locus of figure 27 with the resistor Rd introduced.

The dual slope single breakpoint scheme of **figure 33**, sometimes erroneously [10] described as "treble slope" [*sic*], is an amalgam of the circuits of **figures 5** and **19**. As in **figure 19**, the breakpoint occurs at $v_{out} \approx 0V$ (i.e. $v_{ce} \approx |V_{cc}|$) giving locus **ADEF** (**fig. 34**). However, segment **DEF**, being part of **CDEF**, is established by R_1 and R_3, and its efficacy is therefore as dependent on the value of **Re** as the network of **figure 5**.

Resistor R_2 merely pulls the base of the protection transistor low as required for $\{0V \leq v_{ce} < 40V\}$; this gives segment **AD** whose position in the SOA is ill-defined for non-ideal supply rails due to the use of an invariant voltage reference. Since the breakpoint for this arrangement is fixed at $v_{ce} \approx |V_{cc}|$, only points **A** and **F** on locus **ADEF** are required to obtain a solution.

With reference to **figure 35**, let $R_3 = 220R$ and $|\pm V_{cc}| = 40V$:

$$I_1 \approx I_3$$

Where

$$I_3 = (-39.4 + 39.78)/220R \approx 1.73\text{mA}$$

$\Rightarrow$

$$R_1 = (40 + 39.4)/1.73\text{mA} \approx 46\text{K}$$

With reference to **figure 36**:

$$I_2 \approx (40 - 37.52)/(R_1 // R_3) = 2.48/219R \approx 11.33\text{mA}$$

With $V_f \approx 0V7$ at 11mA:

$$R_2 = V_{R2}/I_2 = (37.52 - 0.7)/11.33\text{mA} \approx 3\text{K}3$$

Clearly, this scheme's indecent dependence on the value of **Re** makes it inferior to the standard linear foldback arrangement of **figure 1**. Consequently, given **Re=0R22**, the protection locus of **figure 34** permits the delivery of only 1A5 at $\text{Vce} \approx 45V97$, requiring a minimum of *six* output pairs for unimpeded drive into a $(4\Omega \angle \pm 60^0)$ load from ±40V supply rails.
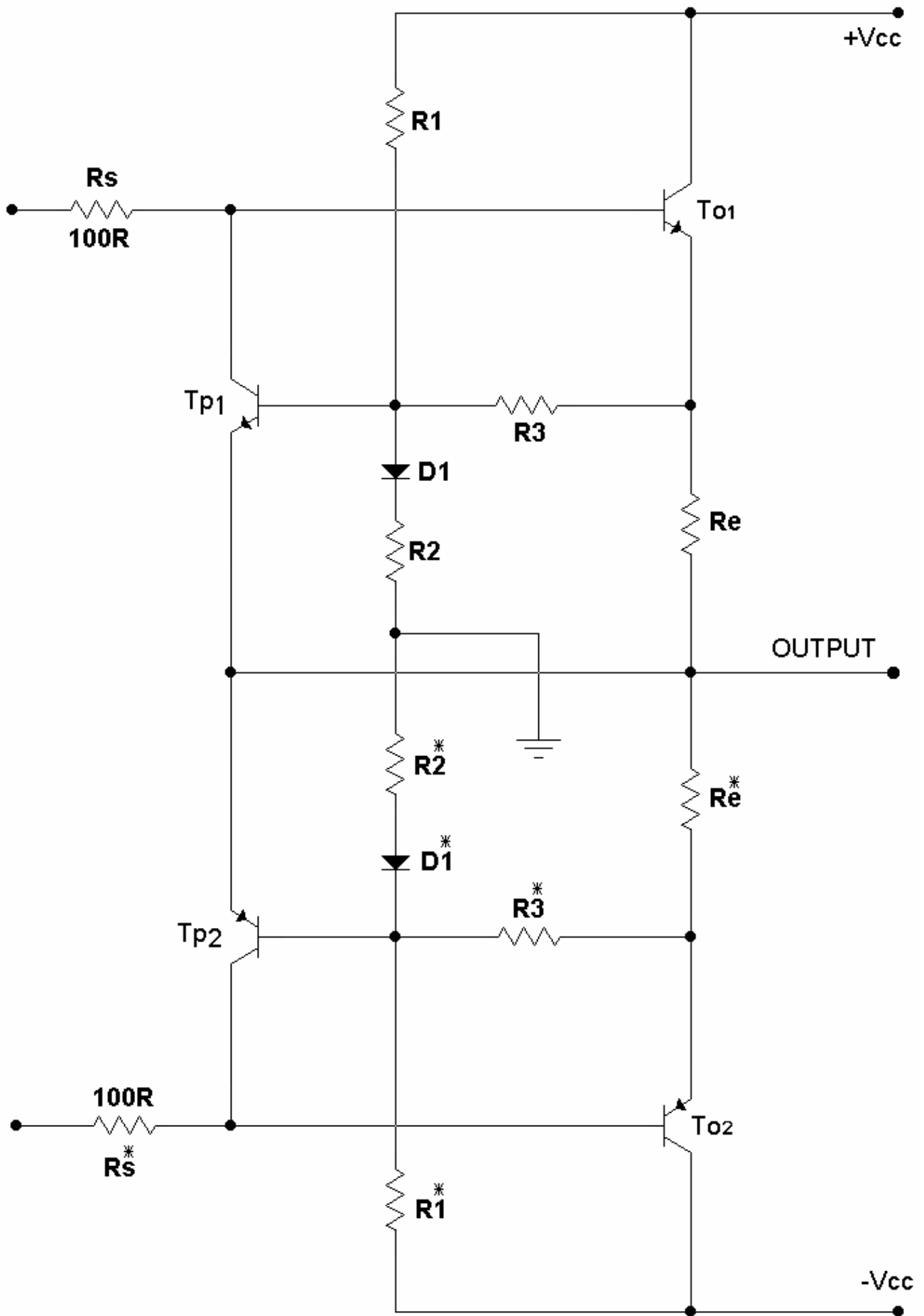
Fig. 33. This dual slope single breakpoint scheme is a logical development of the circuits of figures 5 and 19.
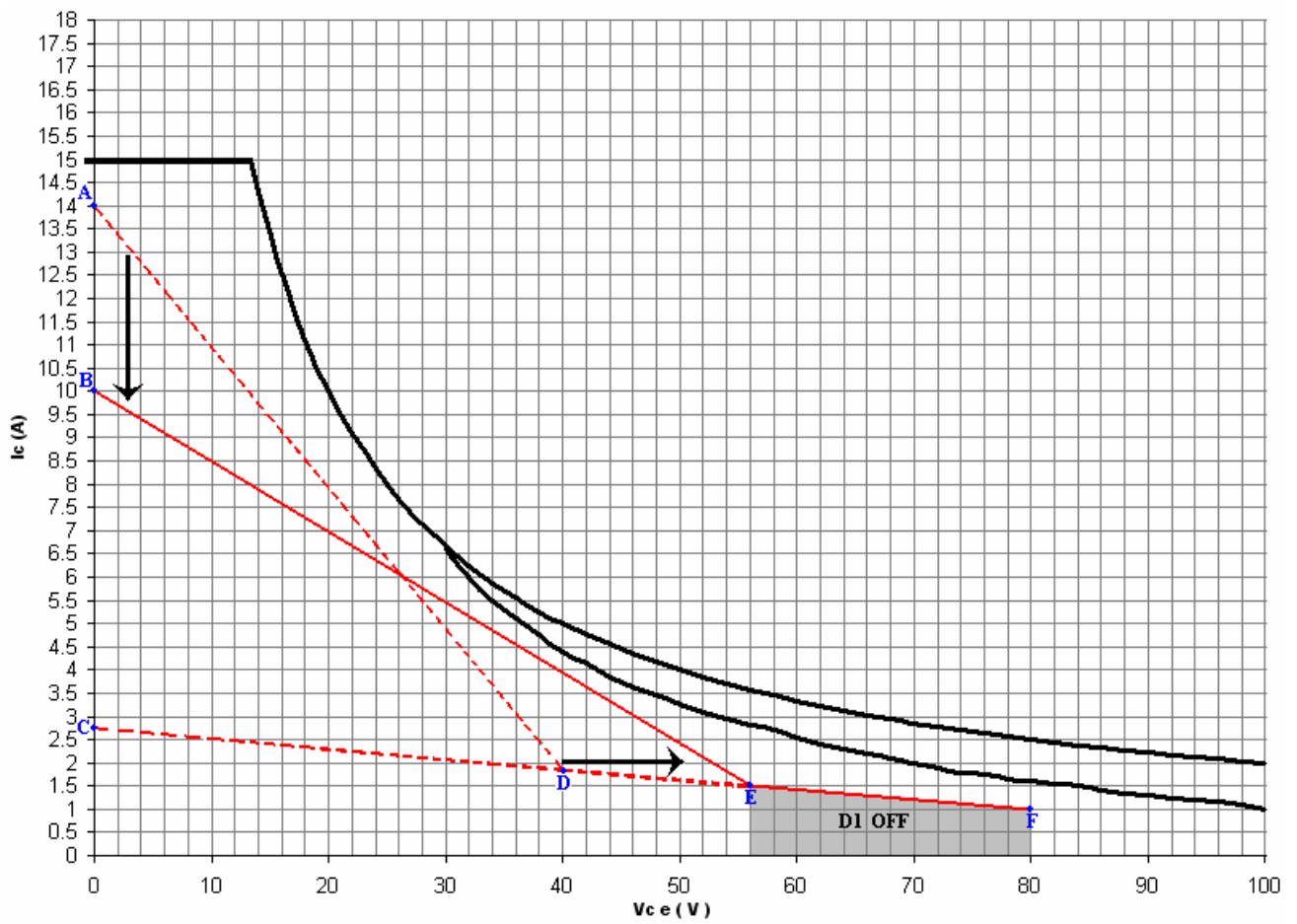
Fig. 34. Dual slope single breakpoint loci described by the circuits of figure 33 and 37.
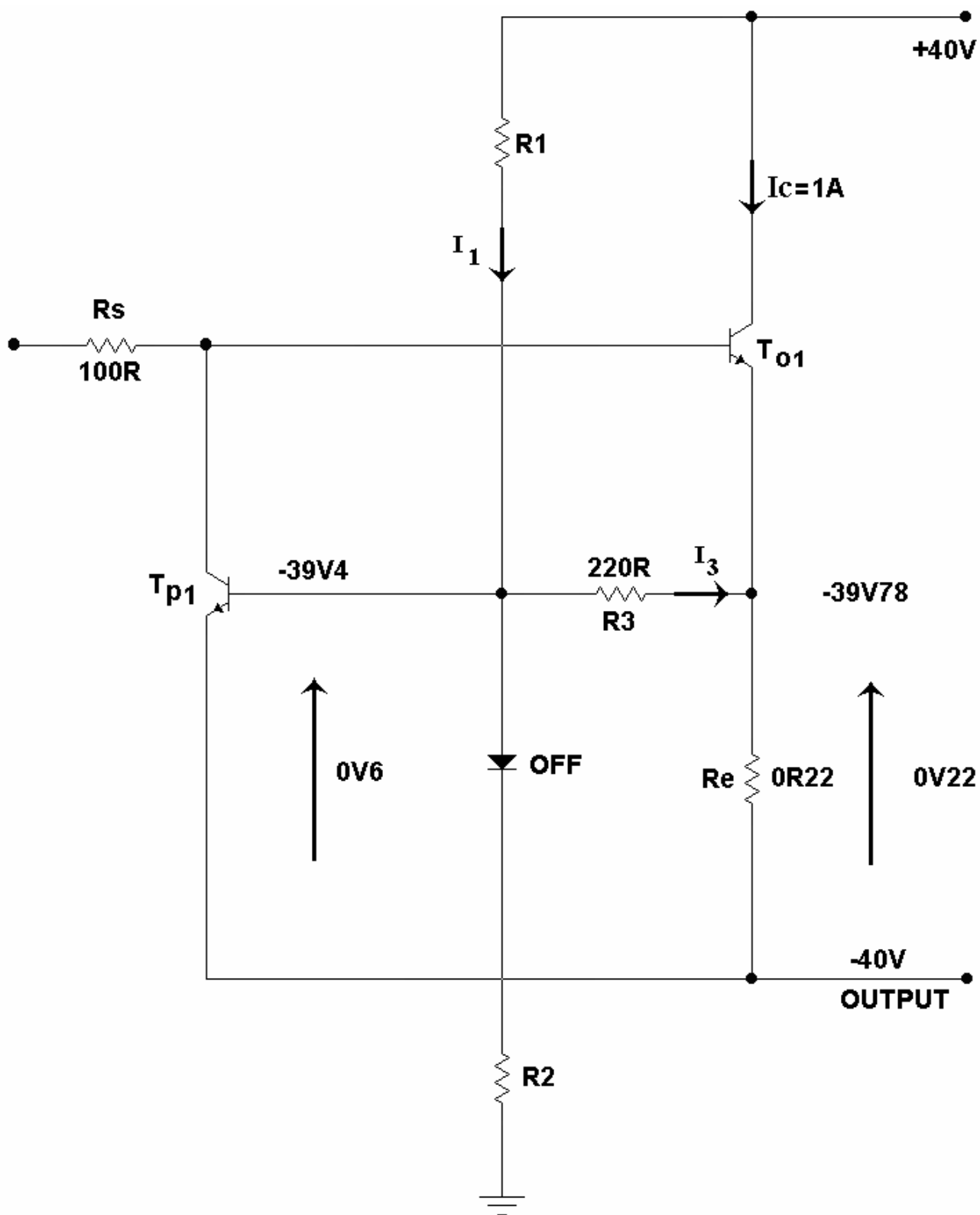
Fig. 35. Output conditions at point F on locus ADEF of figure 34.
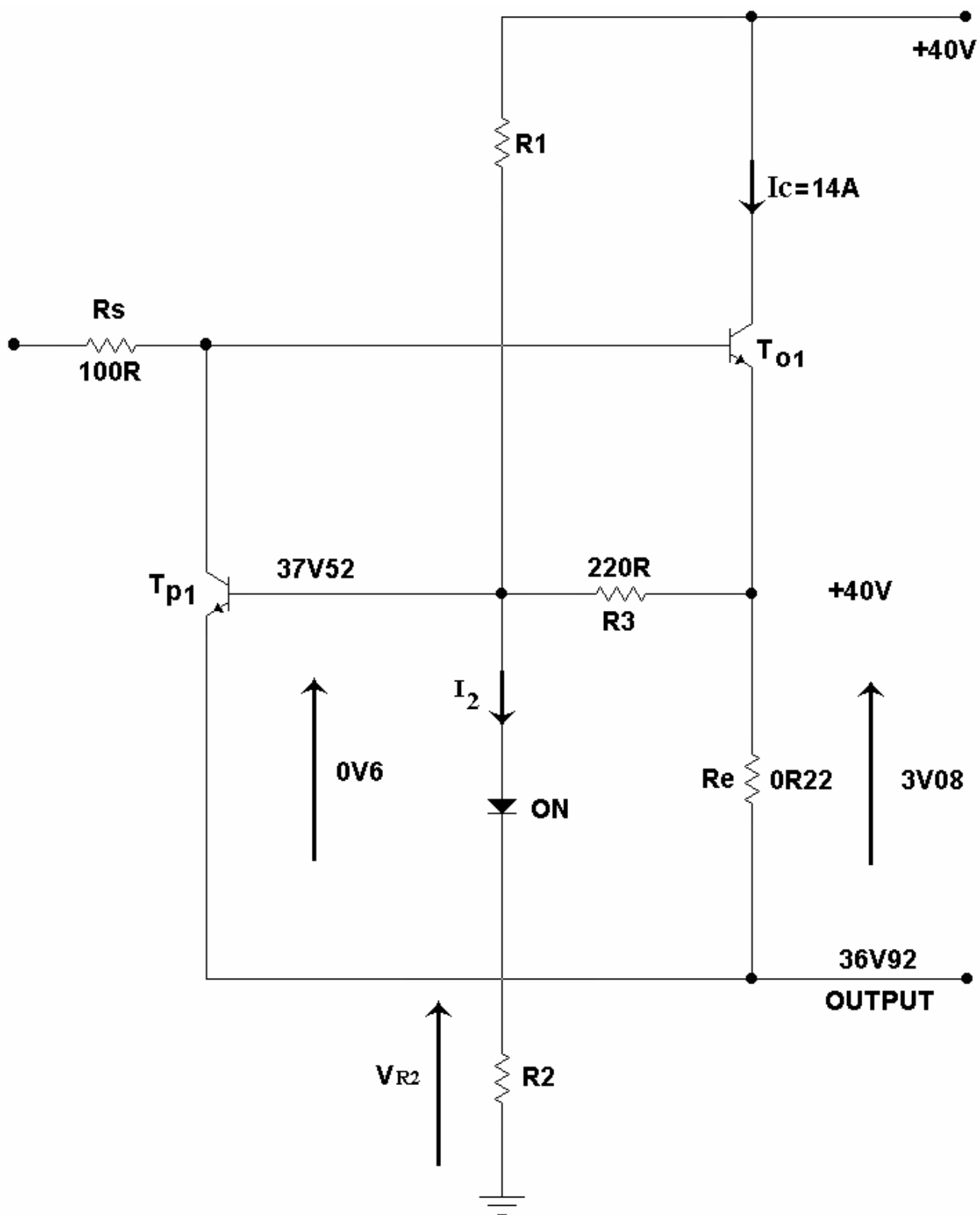
Fig. 36. Output conditions at point A on locus ADEF of figure 34.

As with **figure 23**, the network of **figure 33** may be usefully improved (**fig. 37**) by changing the diode's reference from zero to an arbitrary voltage V_{Ref1} such that $(0V < |V_{Ref1}| < |V_{cc}|)$. This enhances the flexibility of the circuit as the breakpoint can now be moved freely along segment **CF**, giving rise to a more efficient locus **BEF** whose position in the SOA is unaffected by non-ideal fluctuation of the supply rails (**fig. 34**).

The reference voltage is established by determining the output conditions at the breakpoint (**fig. 38**). Therefore, for locus **BEF** in **figure 34**, $V_{Ref1} = -16V33$ and $V_{Ref2} = +16V33$, which calls for a nominal 56V33 zener diode.

With reference to **figure 39**:

$$I_1 \approx I_3$$

Where

$$I_3 = (-39.4 + 39.78)/220R \approx 1.73mA$$

$$\Rightarrow$$

$$R_1 = (40 + 39.4)/1.73mA \approx 46K$$

With reference to **figure 40**:

$$I_2 = (40 - 38.4)/(R_1 \mathbin{/\!/} R_3) = 1.6/219R0 \approx 7.3mA$$

With $V_f \approx 0V65$ at 7mA,

$$R_2 = V_{R2}/I_2 = (38.4 - 0.65 + 16.33)/7.3mA \approx 7K4$$

Note that there is no change in the value of R_1 and R_3 in the circuits of **figures 5**, **33** and **37**, with different values of R_2 required to merely pull the base of the protection transistor low as required when the diode is forward biased.

Although the efficacy of the protection locus is in part ameliorated by the means described above, the gradient of segment **EF**, being part of **CDEF**, is determined by resistors R_1, R_3 and limited by practical values of **Re**-an affliction absent from the circuit of **figure 28**.
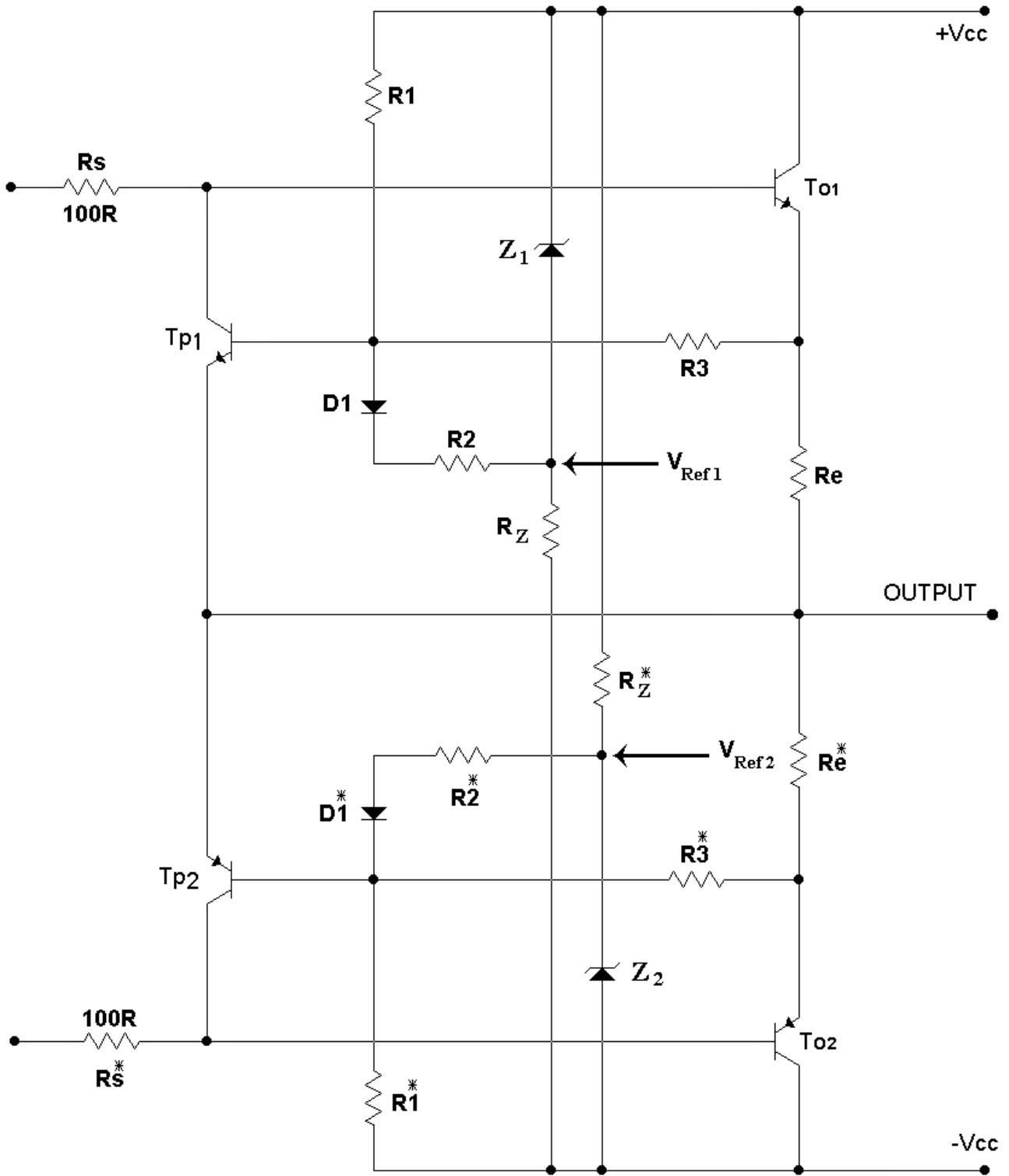
Fig. 37. The efficacy of the compromised dual slope scheme of figure 33 is improved by using arbitrary bootstrapped voltage references of equal magnitude.

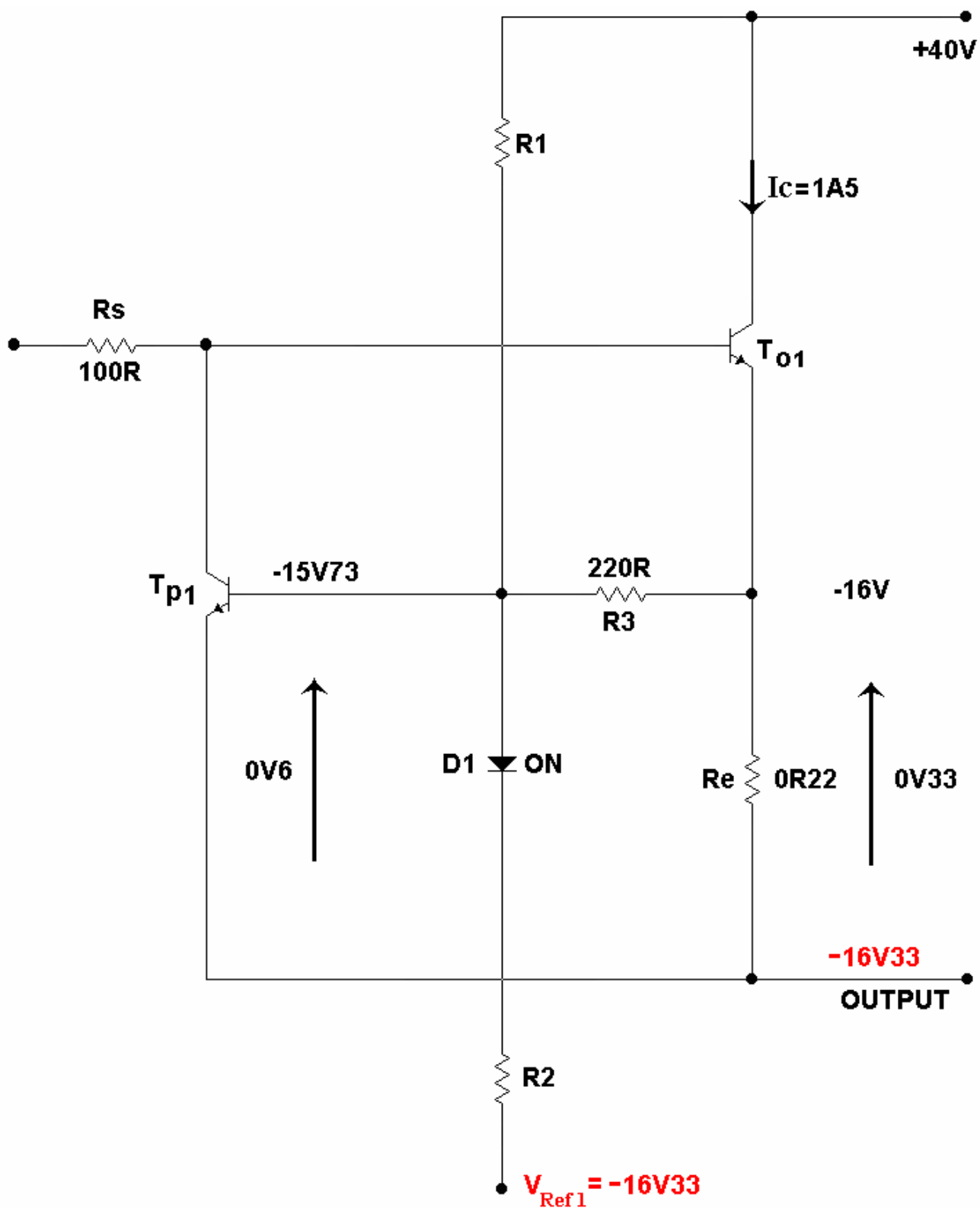**Fig. 38. The reference voltage is made equal in magnitude to the output voltage at the breakpoint (i.e. when Vce=56V); the diode is then at the threshold of conduction.**

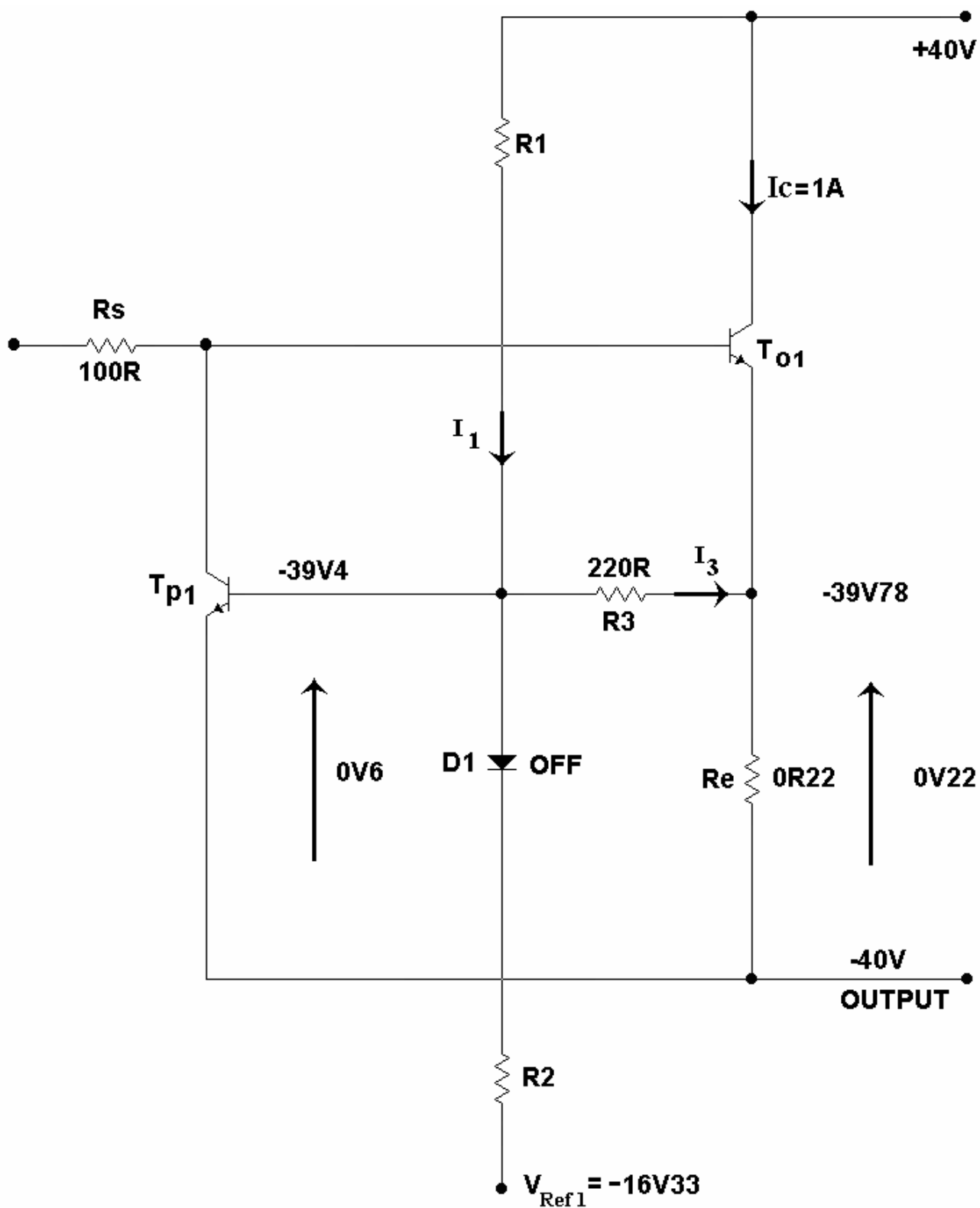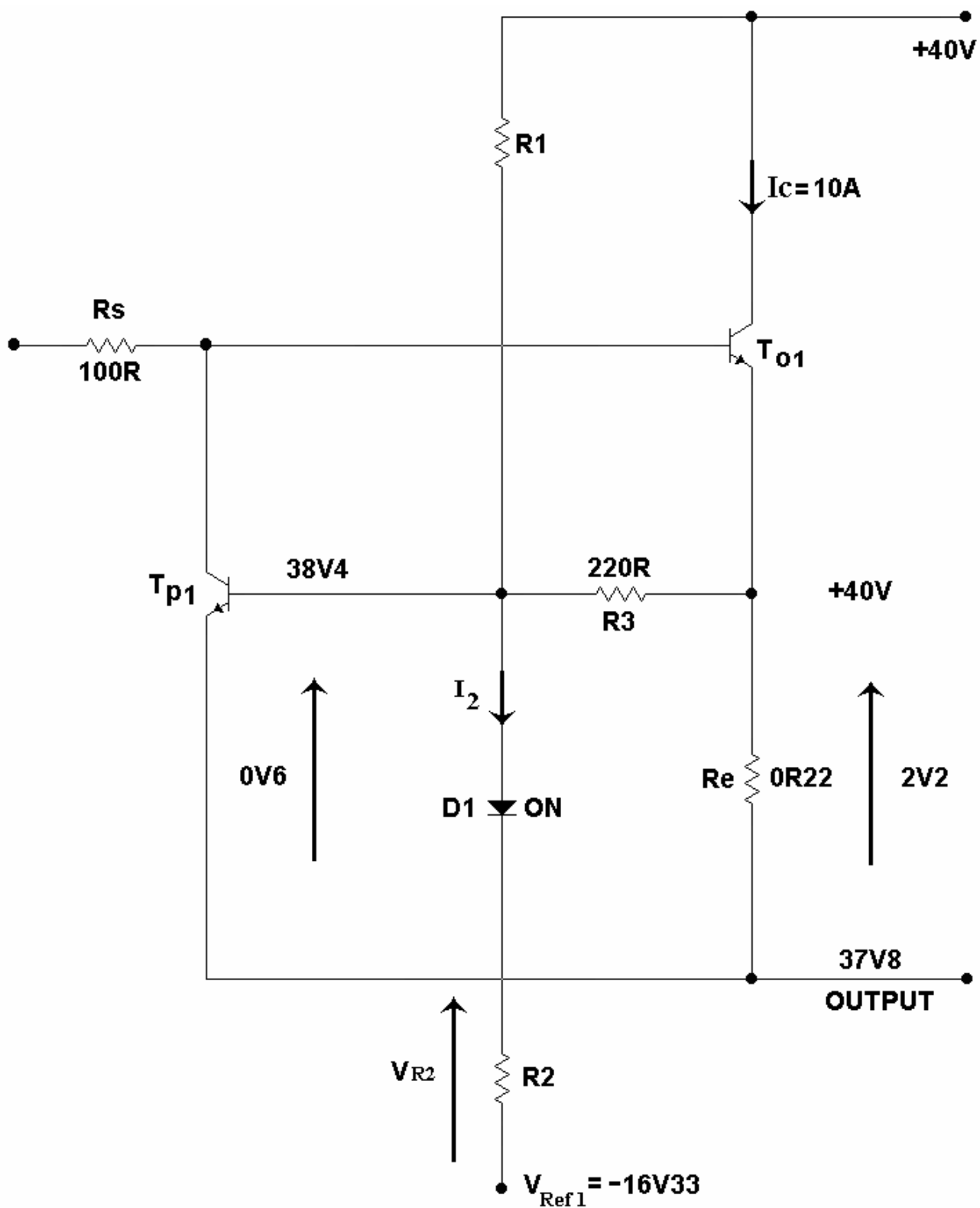**Fig. 39. Output conditions at point F on the protection locus of figure 34.**

Fig. 40. Output conditions at point B on the protection locus of figure 34.

Complete independence from **Re** of both segments of the dual slope protection locus described by the circuit of **figure 37**, may be realised by introducing base-emitter resistors, $\mathbf{R}_2$ and $\mathbf{R}_2^*$, respectively for each protection transistor, $\mathbf{T_{P1}}$ and $\mathbf{T_{P2}}$ (**fig. 41**). The result is, in fact, merely a combination of the linear single slope scheme of **figure 1** and the non-linear single slope circuit of **figure 23**.

The linear single slope locus of **figure 2** is reproduced in **figure 42** as segment **BCD** for which **equations (1)** and **(3)** are valid. Therefore, since, as previously resolved (**equations 1** and **3**) $\mathbf{R}_3 = 220\mathbf{R}$, then $\mathbf{R}_1 = 12\mathbf{K}4$ and $\mathbf{R}_2 = 143\mathbf{R}$ (**fig. 41**). Resistor $\mathbf{R}_4$ pulls the base of the protection transistor low as required for $\{0V \leq v_{ce} \leq 42V\}$ giving segment **AC**.

The reference voltage is equal to the output voltage when $v_{ce} = 42V$, so that $\mathbf{V_{Ref1}} = 40\mathbf{V} - \{42\mathbf{V} + (3\mathbf{A}5 * 0\mathbf{R}22)\} = -2\mathbf{V}77$ and $\mathbf{V_{Ref2}} = +2\mathbf{V}77$.

With reference to **figure 43**:

$$(\mathbf{I}_2 + \mathbf{I}_4) \approx (\mathbf{I}_1 + \mathbf{I}_3)$$

$\Rightarrow$

$$\mathbf{I}_4 \approx (\mathbf{I}_1 + \mathbf{I}_3 - \mathbf{I}_2)$$

$\Rightarrow$

$$\mathbf{I}_4 = (40 - 37.96)/12\mathbf{K}4 + (40 - 37.96)/220\mathbf{R} - 0.6/143\mathbf{R}$$

$\Rightarrow$

$$\mathbf{I}_4 \approx 5.24\mathbf{mA}$$

With $\mathbf{V_f} \approx 0\mathbf{V}6$

$$\mathbf{R}_4 = \mathbf{V_{R4}}/\mathbf{I}_4 = (37.96 - 0.6 + 2.77)/5.24\mathbf{mA}$$

$\Rightarrow$

$$\mathbf{R}_4 \approx 7\mathbf{K}7$$

The flexibility of the scheme of **figure 41** is significantly improved compared to that of **figure 37**. However, the network of **figure 28** achieves the same versatility with a significantly reduced component count.
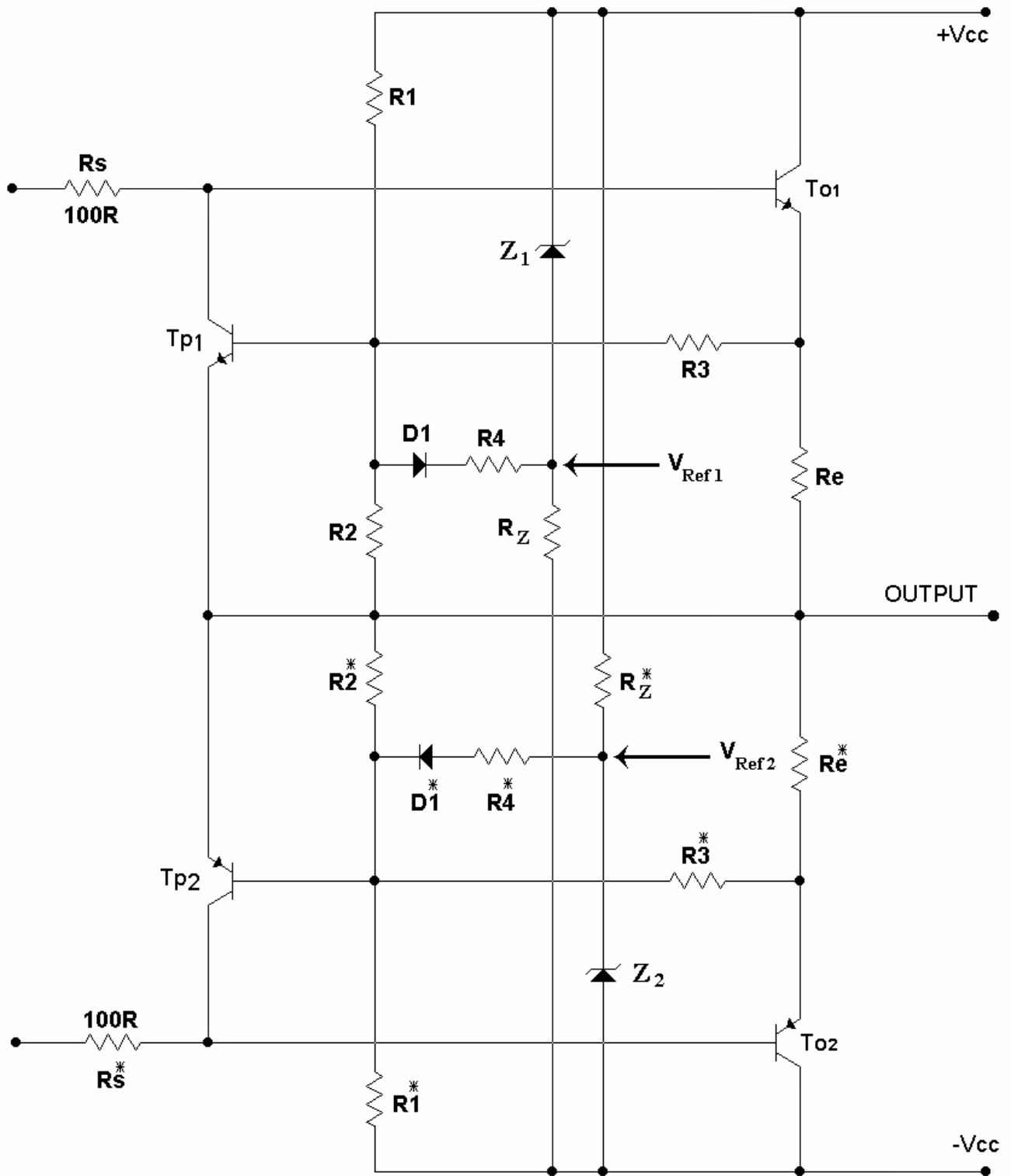
Fig. 41. Introducing resistor R_2 into the circuit of figure 37 facilitates placement of an arbitrary locus in the SOA without undue dependence on the value of R_e.
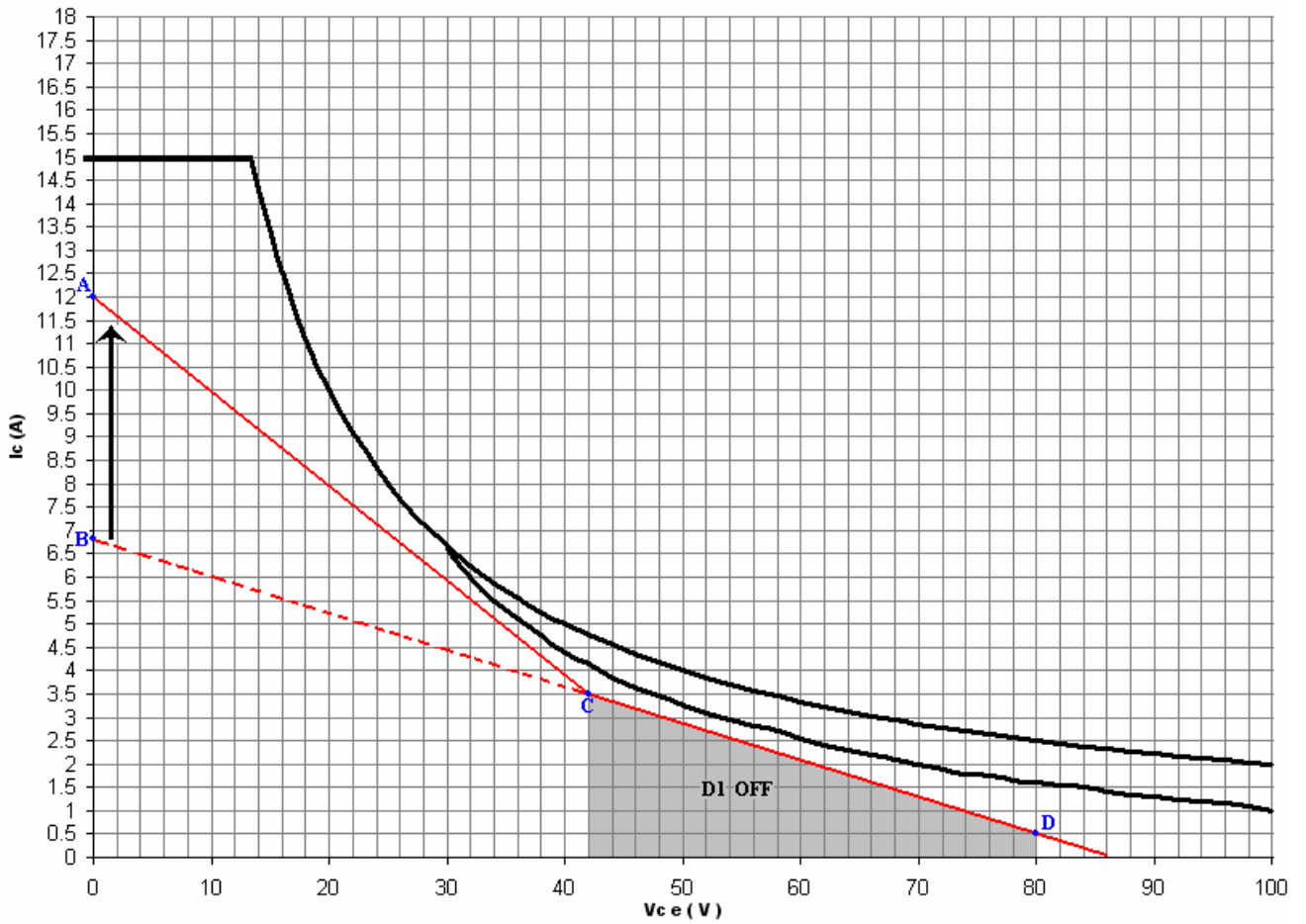
Fig. 42. Dual slope single breakpoint protection locus described by the circuit of figure 41. Resistor R_4 modifies the linear single slope segment BCD of figure 2 by effecting a vertical translation of segment BC about point C.
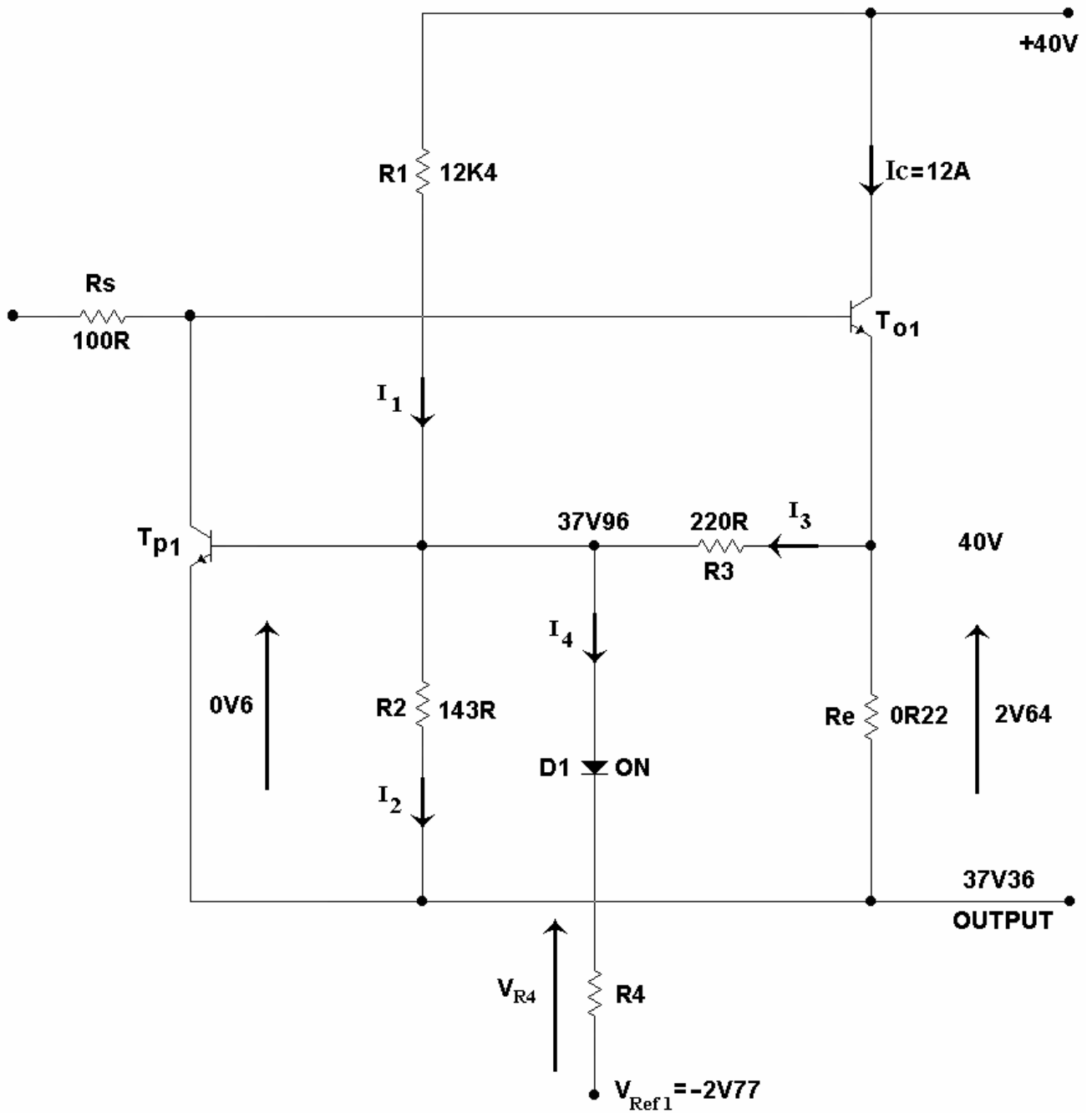
Fig. 43. Output conditions at point A on protection locus ACD of figure 42.

Triple slope dual breakpoint non-linear foldback limiting

With modern power transistors and practical loudspeaker systems, an optimally located dual slope protection locus realised by the limiter of **figure 28** can hardly be improved upon with respect to efficiency in the critical $\left\{\left|V_{cc}\right| \leq v_{ce} < 2\left|V_{cc}\right|\right\}$ region. However, with nominally resistive laboratory loads, with which a power amplifier's published specifications are obtained, the $\left\{0V \leq v_{ce} \leq \left|V_{cc}\right|\right\}$ region of the SOA is of primary interest (**fig. 10**).

Thus, in a competitive market place, even when the truth of the matter is known, an amplifier designed to maintain its rated voltage swing across resistive loads of decreasing magnitude (typically to a minimum of 1 ohm) without limiter intrusion may be commercially rewarding. A suitably robust power supply and conservative thermal management are assumed.

To this end, the triple slope design of **figure 44** is presented. This circuit is a straightforward amalgam of the dual slope scheme of **figure 28** and the single slope single breakpoint network of **figure 23**. Thus, the circuit of **figure 28** is required to produce the dual slope characteristic **BDF** (**fig. 45**), while resistor $\mathbf{R}_4$ pulls the base of protection transistor $\mathbf{T_{P1}}$ low as appropriate for $\left\{0V \leq v_{ce} \leq 42V\right\}$, giving segment **AC**.

Fifty-volt supply rails are assumed; a triple slope locus with $\pm 40\mathbf{V}$ rails is vastly unnecessary. A $(4\Omega \angle \pm 60^0)$ load driven to $\pm 50\mathbf{V}$ rails requires $i_c \approx 9\text{A5}$ when $v_{ce} \approx 59\text{V}$, giving peak transistor dissipation $\mathbf{p_{d(max)}} \approx 561\mathbf{W}$. The triple slope protection locus of **figure 45** allows 2A at $v_{ce} \approx 59\text{V}$ for a single complementary transistor pair. Therefore, *at least* five complementary pairs are required to drive a notional $(4\Omega \angle \pm 60^0)$ loudspeaker system from $\pm 50\mathbf{V}$ supply rails without intrusive limiter activation. The algebra for this arrangement is straightforward if a little tedious and is left to interested readers.
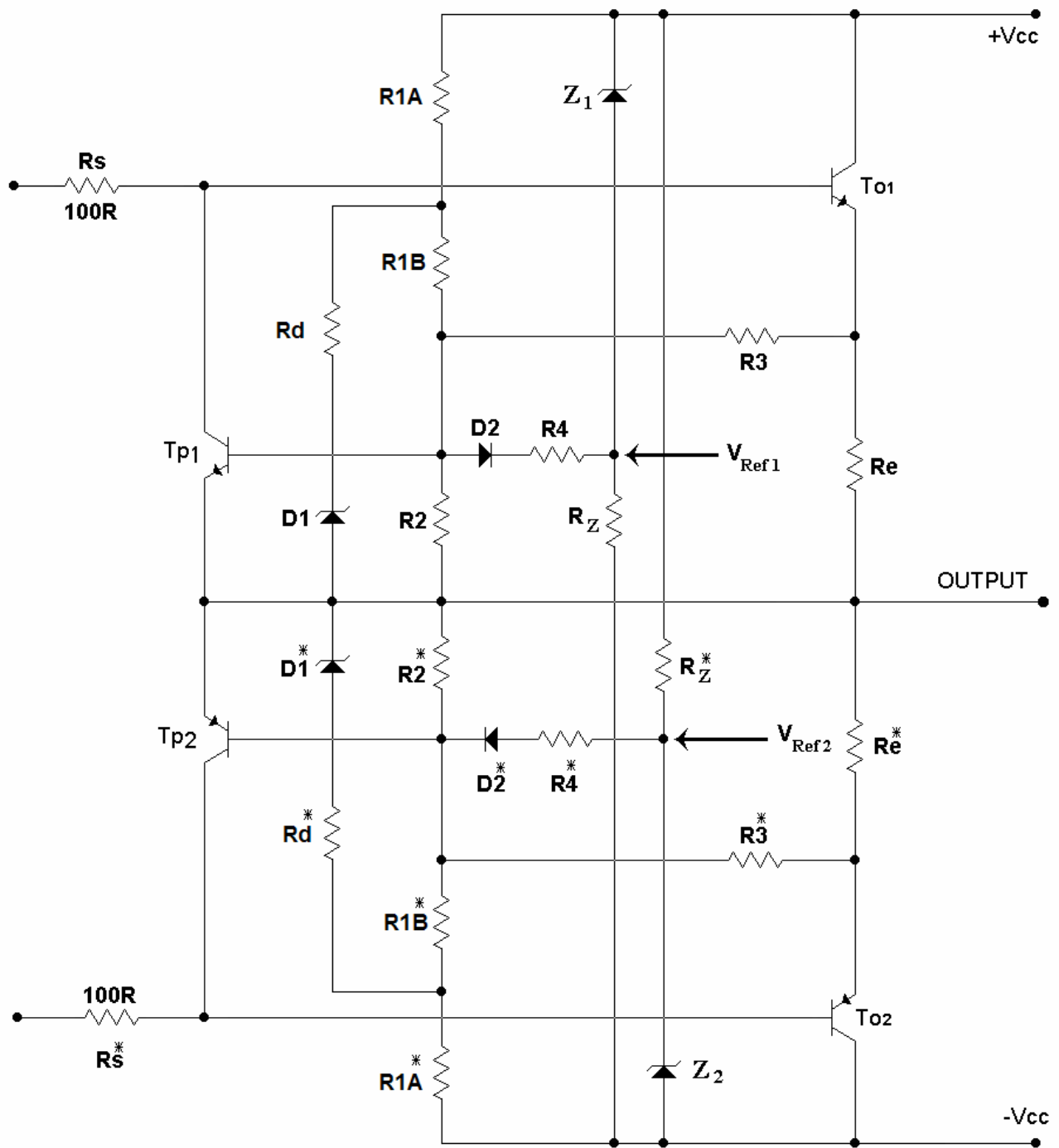
Fig. 44. Triple slope dual breakpoint non-linear foldback limiter.
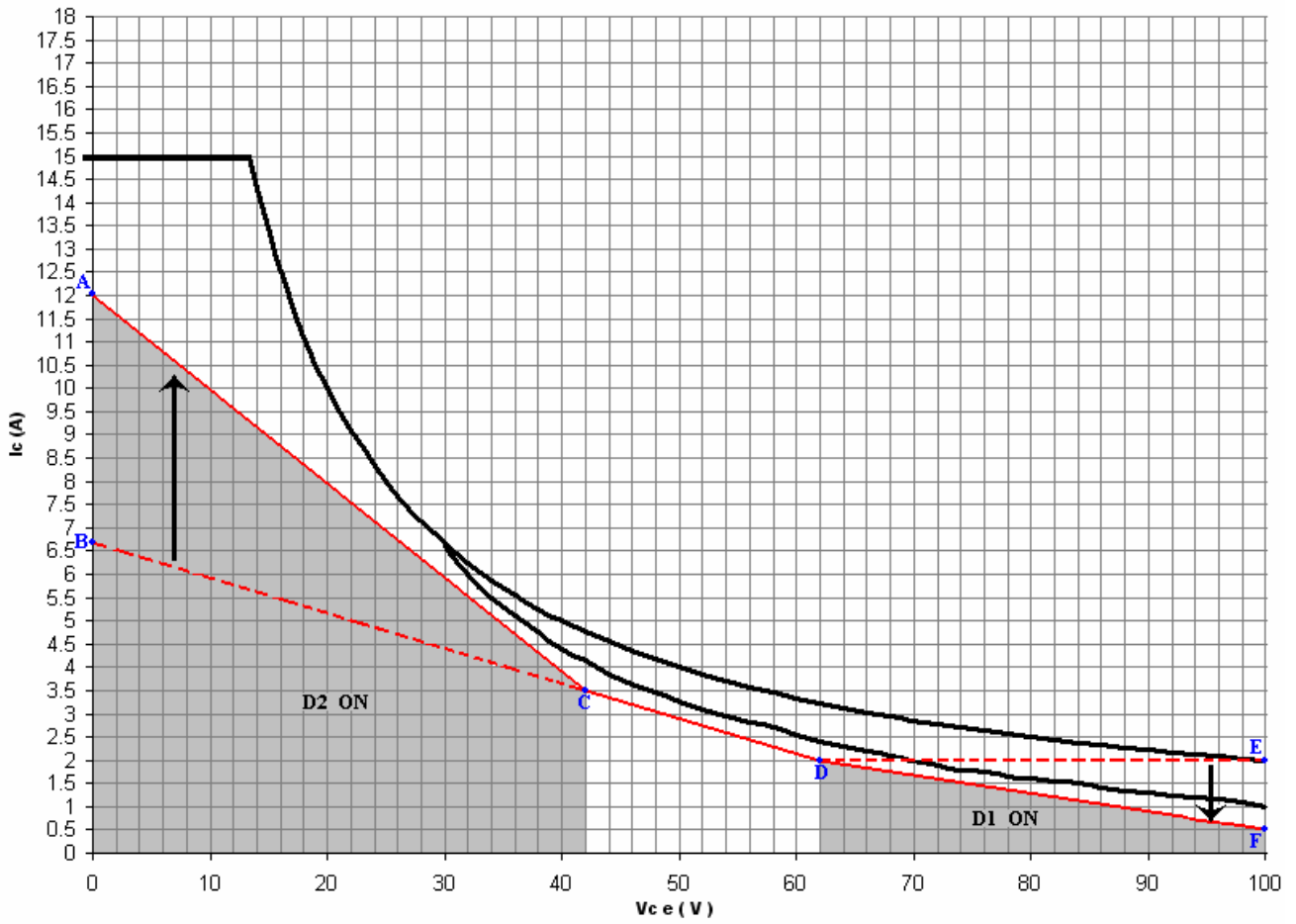
Fig. 45. Triple slope dual breakpoint protection locus described by the circuit of figure 44; resistor R_4 modifies the dual slope characteristic BDF by effecting a vertical translation of segment BC about point C.

Protecting paralleled complementary output transistors

Emitter resistor **Re** performes current-voltage conversion for the SOA limiter, and promotes thermal stability by maintaining equable current distribution in an output stage consisting of multiple paralleled pairs of complementary transistors. For this reason, some designers suggest it is only neccesary to monitor the current of a single complementary pair in such an output stage[1,pg.257.].

Alternatively, the calculated value of the current sensing resistor R_3 for a single complementary transistor pair is multiplied by the number **N** of paralleled output pairs with each resistor of value $N * R_3$ used to monitor the current in each transistor as shown in **figure 46**.

An obvious disadvantage inherent in both schemes is that the open-circuit failure of a rogue transistor in one half of the output stage could result in the disastrous alteration of the protectection locus for the remaining devices in that section. However, with modern power transistors, this condition is unlikely to materialise; the use of an independent SOA limiter for each complementary pair would eliminate this potential flaw, but is financially indefensible in most commercial designs.
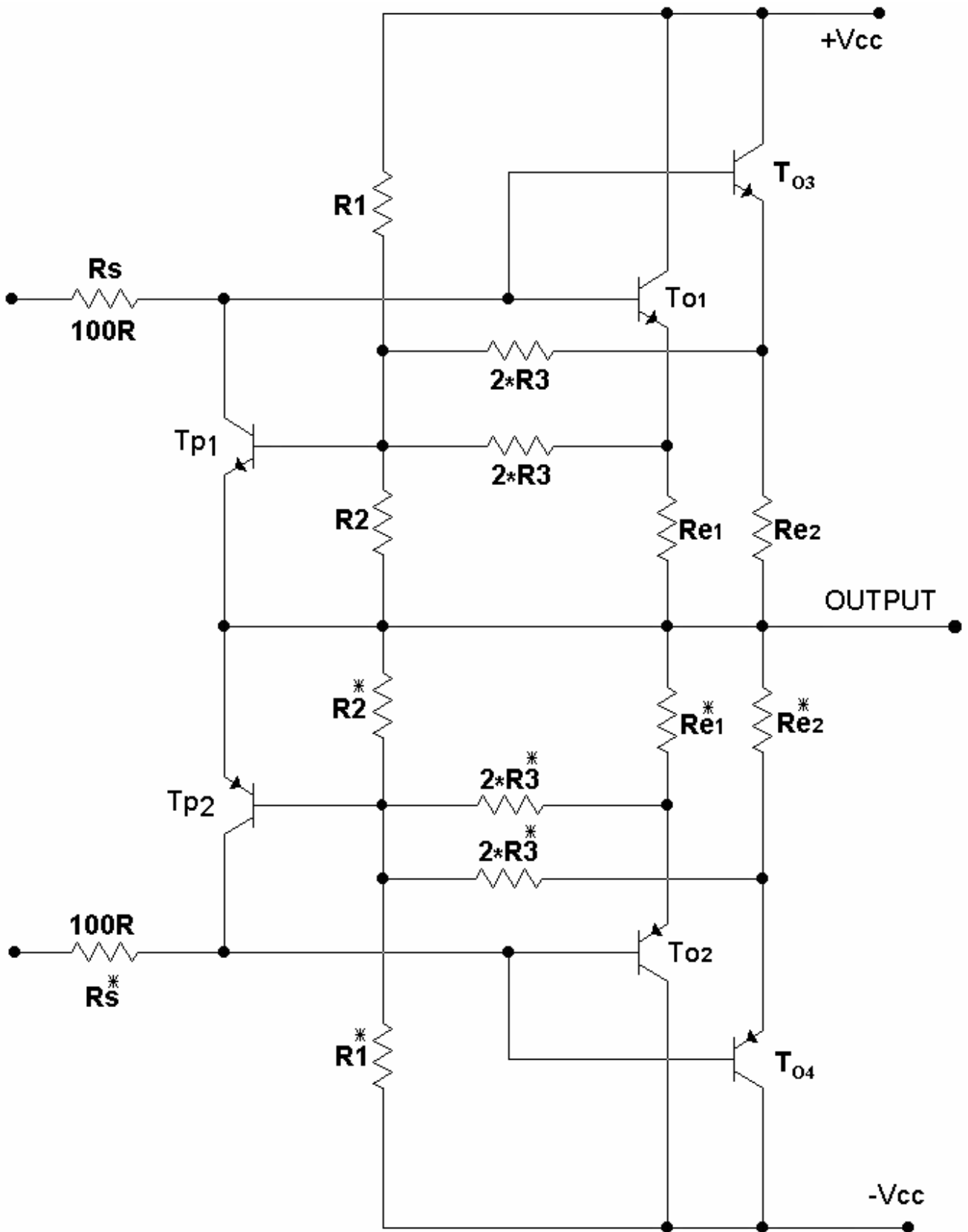
Fig. 46. In this single-slope linear foldback scheme, voltage signals from multiple current sensing resistors are summed algebraically at the base of the protection transistor.

Simulating SOA Protection

SPICE allows the designer to check the results of calculation, to establish whether the deviation from the desired protection locus obtained by using prefered values is significant and to determine the effect of changes in ambient temperature on the position of the protection locus.

The arrangement of **figure 47** is a slightly modified version of the simulation circuit used by Douglas Self[11]. Voltage source **V1** models the output transistors collector-emitter voltage **Vce**, while the unity gain voltage controlled current source **G1** generates the current in the notional output transistor's emitter resistor **R6**. The current produced by **G1** is the quantity that is plotted as **V1** is DC swept. This current is a function of the voltage at the collector of the constant current source loaded protection transistor **Q1**.

Unfortunately, results obtained from this circuit can be grossly misleading unless it is correctly calibrated. This is because an increase in the value of the protection transistor's constant current source **I1** causes the the plotted locus to move upwards, while an increase in **Q1**'s current gain causes the locus to move downwards.

To calibrate the circuit, the single slope linear foldback circuit of **figure 1** is used because it gives inherently more accurate results than the non-linear foldback arrangements whose accuracy is compromised by zener diodes with tolerances no better than 5%. Thus, having obtained the calculated values for a given single slope locus, **I1** must be adjusted (for a given transistor model for **Q1**) until the plotted locus conforms to that predicted by the calculated component values.

Figure 48 shows the effect on the protection locus of increasing the simulation temperature from $27^o\mathbf{C}$ to $45^o\mathbf{C}$. This magnitude increase in temperature may occur in the vicinity of the SOA protection circuitry in, for example, a powerful class-A amplifier.

The drop in threshold voltage (approximately $2\mathbf{mV/^oC}$) of the protection transistor combined with the increase (approximately $6\mathbf{mV/^oC}$ for a 10V zener diode) in the zener diode's breakdown voltage with increasing temperature cause that part of the locus controlled by the zener diode to move downwards by a significant amount. The $45^o\mathbf{C}$ locus can no longer accommodate $\pm40\mathbf{V}$ supply rails without protection being invoked, even with an open circuit load, when the output swings more than about $\pm35\mathbf{V}$.

Clearly this effect may be lessened by using a temperature compensated zener diode. Alternatively a zener diode with negative temperature coefficient may be used to eliminate the downward movement of the locus which would otherwise be occasioned by the use of a positive temperature coefficient zener diode and to compensate for the downward movement of the locus due to the protection transistor's negative temperature coefficient. This calls for a zener diode with **Vz<5V** which typically have a negative temperature coefficient in the range $0\mathbf{mV}-4\mathbf{mV/^oC}$. The potential for overcompensation is insignificant, but may be accommodated by the judicious placement of that part of the locus controlled by the zener diode so that any upward movement of the locus with increasing temperature does not result in the violation of SOA bounds.
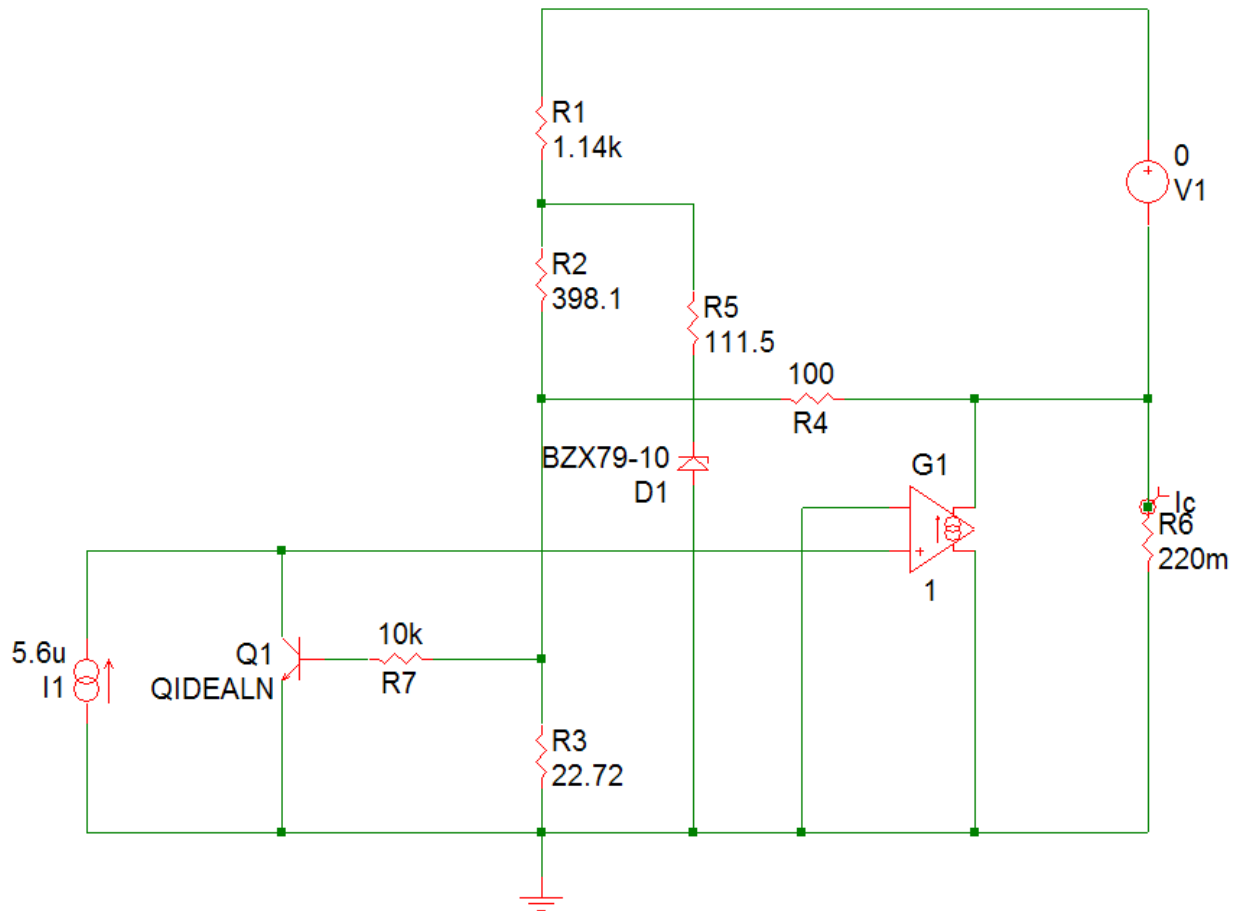
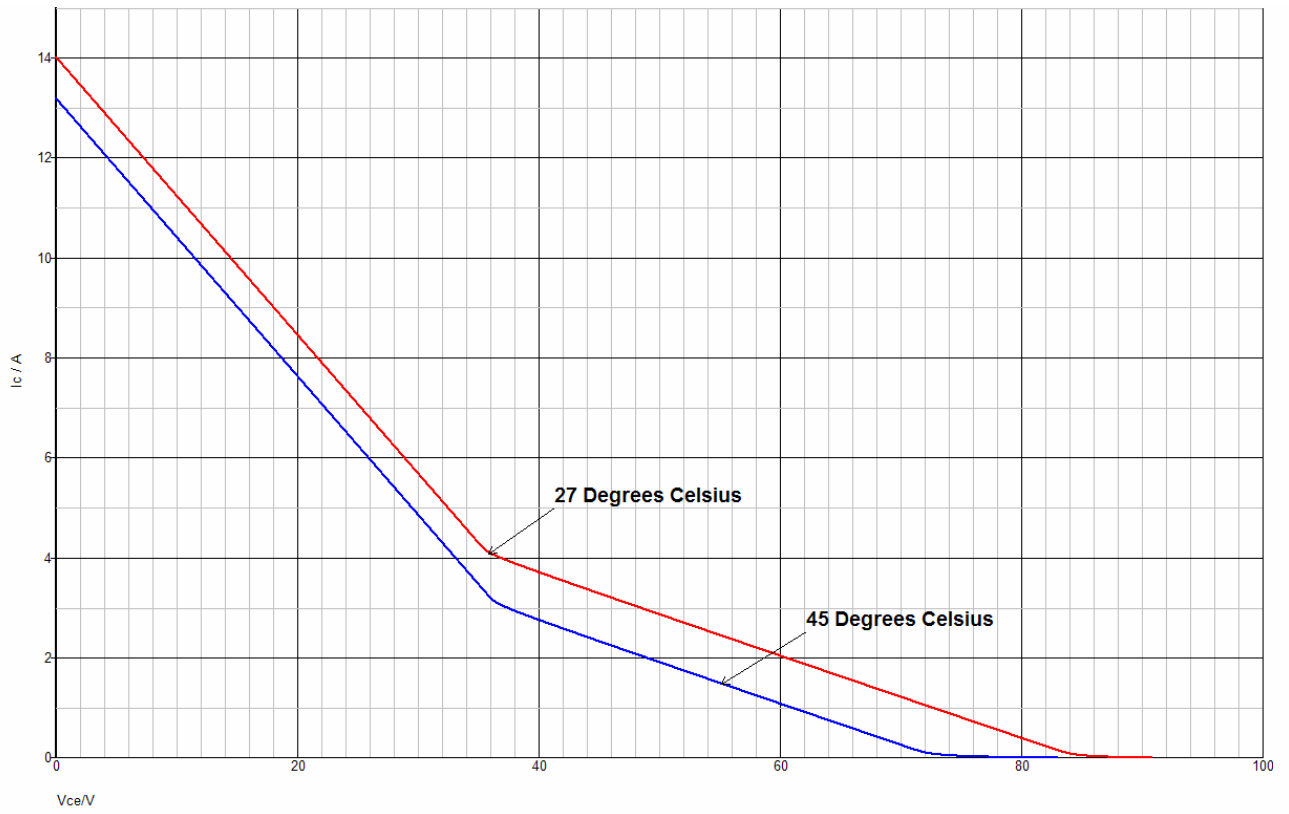**Fig. 47. SPICE circuit for simulating dual slope SOA protection.**

Fig. 48. Simulated loci for the circuit of figure 47 at 27 and 45 degrees Celsius.

Conclusion

On grounds of safety and reliability, it is firmly recommended that all nominally linear complementary semiconductor audio frequency power amplifiers incorporate suitable SOA protection. The aversion cultivated by some designers to such is here shown to be wholly illusory. A competently designed SOA limiter should remain demonstrably inert and therefore completely unobtrusive with virtually all commercial loudspeaker systems provided the output stage consists of sufficient complementary transistors to safely drive a $\left(4\Omega\angle\pm60^{0}\right)$ load to the supply rails.

The dual slope circuit of **figure 28** represents a significant improvement in efficient SOA utilisation compared to the single slope topology of **figure 1**, with no significant penalty with regard to algebraic or physical complexity. Its characteristic locus (**fig. 27**) may be readily optimised to accommodate nominal $\pm50\text{V}$ supply rails with **MJL3281A/MJL1302A** transistors; however, higher supply rails are not recommended for worst-case reactive loads, as available collector current for these devices rapidly falls below 0A5 for $\text{V}_{\text{CE}}>100\text{V}$.

Although e-MOSFETs are at least an order of magnitude less linear than bipolar transistors[11,pg.273.], they provide significantly greater scope for reliable design at high device voltages $\left(\left|\text{V}_{\text{Supply}}\right|>>50\text{V}\right)$, with the promise of even greater efficiency in SOA utilisation due to the absence of secondary breakdown. Nevertheless there is no need to endure the indignity of e-MOSFET non-linearity and on-resistance voltage inefficiency in sub-200W into 8Ω designs.

More elaborate protection schemes are possible, with the use of as many diodes as the number of required breakpoints. However, the increase in available current in the high voltage region $\left\{\left|V_{cc}\right|\le v_{ce}<2\left|V_{cc}\right|\right\}$, where it counts with respect to reactive load drive, is negligible relative to the circuit complexity thus engendered.

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