







```
00001:
00002: /*
00003: *
                     SRC4392 For audio dac
00004: *
                       (c) Copyright 2005 CQ
00005:
00006:
                       All Rights Reserved
00007: *
             SRC4392.c
00008: * File:
00009: * author:
            CQ
00010: * REV :
             00
00011: * Description:
            .This module is used to process
00012: *
00013: *
00014:
00014: *******/
00015:
00016: #include "Includes.h"
00017:
00018:
00019: /*
00019: ******
00020: *
                       Global Variables Definition
00021: *
00022: *******/
00023:
00024:
00025:
00026:
00027: /
00027:
00027: ******
00028:
                       Rom Data Table
00029: *
00030: ******/
00031:
00032:
00033:
00034:
00035: /*
00035: ******
00036: *
                       EEprom Data Table
00037: *
00038: *******/
00039:
00040:
00041:
00042:
00043: /*
00043: ==========
00044:
00045:
                       MAIN CODE
00046:
00047: ==========*/
00048: int main (void)
00049: {
00050:
      INT8U config_data, target_addr;
00051:
00053:
       _delay_ms(100);
      SystemInit();
00054:
00055:
00056:
      //config sm5847
00057:
      SM5847\_CONFIG\_DIR\_PORT = 0xFF;
                                    //port as output;
      SM5847_CONFIG_ENABLE_DIR_PORT | = 0x0c;
                                //bit3,bit3 as output;
00058:
      CLRBIT(SM5847_CONFIG_ENABLE_PORT,BIT(SM5847_EN1));
00059:
00060:
      CLRBIT(SM5847_CONFIG_ENABLE_PORT,BIT(SM5847_EN2));
00061:
      /*config parameter1
00062:
00063:
      CKSLN
           = 1
                 192fs
00064:
      1W1N
           = 0
                 input bit long: 24bit
      1W2N
           = 0
00065:
      OW1N
           = 0
00066:
                 output bit long: 24bit
      OW2N
           = 0
00067:
```

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00068:
            SYNCN
                     = 1
00069:
            CKDV1
                     = 0
                                divider ratio: 1
00070:
            CKDV2
                     = 0
00072:
            SM5847_CONFIG_PORT = BIT(CKSLN) | BIT(SYNCN);
00073:
00074:
            _delay_us(5);
00075:
            SETBIT(SM5847_CONFIG_ENABLE_PORT,BIT(SM5847_EN1));
00076:
            _delay_us(100);
            CLRBIT(SM5847_CONFIG_ENABLE_PORT,BIT(SM5847_EN1));
00077:
00078:
            _delay_us(5);
00079:
00080:
            / *config parameter2
                            disable DEMPL
00081:
            DEMPI
                     = 0
                     = 0
00082:
            DEMPR
                            disable DEMPR
            FSEL1
                     = 0
00083:
            FSEL2
                     = 0
00084:
00085:
            DITHD
                     = 1
            \mathsf{OMD}
                            8FS
00086:
                     = 1
00087:
            SM5847_CONFIG_PORT = BIT(DITHD) | BIT(OMD);
00088:
00089:
            _delay_us(5);
            SETBIT(SM5847_CONFIG_ENABLE_PORT,BIT(SM5847_EN2));
00090:
00091:
            _delay_us(100);
            CLRBIT(SM5847_CONFIG_ENABLE_PORT,BIT(SM5847_EN2));
00092:
00093:
            _delay_us(5);
00094:
00095:
00096:
            //configration SRC4392 with SPI mode
00097:
            //config_data = BIT(PDPB) | BIT(PDPA);
00098:
00099:
00100:
            config_data = BIT(PDSRC) | BIT(PDRX) | BIT(PDPB) | BIT(PDPA);
            target_addr = POWERDOWN;
00101:
00102:
00103:
            WriteDataToSrc4392(target_addr, config_data);
00104:
            _delay_ms(1);
00105:
            //config_data = ReadDataFromSrc4392(target_addr);
            //_delay_ms(1);
00106:
00107:
00108:
            //GLOBINTSTAS (default)
00109:
            // PortA: 24bit I2S MODE , Master mode , SRC output source
00110:
00111:
            //porta ctrl1
00112:
            //config_data = BIT(AFMT0) | BIT(AMS) | BIT(AOUTS1) | BIT(AOUTS0);
            config_data = BIT(AMS) | BIT(AOUTS1);;
00113:
            target_addr = PACTL1
00114:
00115:
            WriteDataToSrc4392(target_addr, config_data);
00116:
            _delay_ms(1);
00117:
            //config_data = ReadDataFromSrc4392(target_addr);
00118:
            //PACTL2:default
00119:
00121:
           //PortB: 24bit I2S MODE ,Slave mode , input mode
00122:
            config_data = BIT(BFMT0) | BIT(BOUTS0);
00123:
            target_addr = PBCTL1
00124:
            WriteDataToSrc4392(target_addr, config_data);
00125:
00126:
            _delay_ms(1);
           //config_data = ReadDataFromSrc4392(target_addr);
00127:
00128:
00129:
            //PBCTL2: default
00130:
00131:
            //TXCTL1
00132:
            //TXCTL2
           //TXCTL3
00133:
00134:
            //SDSTAS
00135:
            //SDINTMASK
00136:
            //SDINTMODE
00137:
00138:
            // RX4 is the default channel, MCLK clock
            config_data = BIT(RXMUX1) | BIT(RXMUX0) | BIT(RXCLK);
00139:
00140:
            target\_addr = RXCTL1
            WriteDataToSrc4392(target_addr, config_data);
00141:
00142:
            _delay_ms(1);
           //config_data = ReadDataFromSrc4392(target_addr);
00143:
00144:
00145:
            //RXCTL2
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00146:
           config_data = BIT(RXCKOE) | BIT(LOL);
00147:
           target_addr = RXCTL2;
00148:
           WriteDataToSrc4392(target_addr, config_data);
00149:
           _delay_ms(1);
00150:
           //RXPLLCFG1
00151:
           config_data = BIT(P1) \mid BIT(J3);
00152:
           target_addr = RXPLLCFG1;
00153:
           WriteDataToSrc4392(target_addr, config_data);
00154:
00155:
           _delay_ms(1);
00156:
00157:
           //RXPLLCFG2
           //RXPLLCFG3
00158:
           //NPCMAUDDET
00159:
00160:
           //RXSTAS1
00161:
           //RXSTAS2
           //RXSTAS3
00162:
00163:
           //RXINTMASK1
00164:
           //RXINTMASK2
           //RXINTMODE1
00165:
00166:
           //RXINTMODE2
00167:
           //RXINTMODE3
           //GPO1
00168:
           //GPO2
00169:
00170:
           //GPO3
00171:
           //GPO4
           //AUDQSUBCODE1
00172:
00173:
           //AUDQSUBCODE2
00174:
           //AUDQSUBCODE3
00175:
           //AUDQSUBCODE4
00176:
           //AUDQSUBCODE5
00177:
           //AUDQSUBCODE6
           //AUDQSUBCODE7
00178:
00179:
           //AUDQSUBCODE8
           //AUDQSUBCODE9
00180:
           //AUDQSUBCODE10
00181:
00182:
           //PCBPH
           //PCBPL
00183:
           //PDBPH
00184:
00185:
           //PDBPL
00186:
00187:
           //SRC input source: DIR
           config_data = BIT(SRCIS1) | BIT(SRCIS0) | BIT(SRCCLK0) | BIT(SRCCLK1);
00188:
           //config_data = BIT(SRCISO);
                                                   //PORTB INPUT
00189:
           target_addr = SRCCTL1
00190:
           WriteDataToSrc4392(target_addr, config_data);
00191:
00192:
           _delay_ms(1);
           //config_data = ReadDataFromSrc4392(target_addr);
00193:
00194:
00195:
           //SRCCTL2
00196:
           //SRCCTL3
           //SRCCTL4
00197:
00198:
           //SRCCTL5
00199:
           //SRCIORATIO1
00200:
           //SRCIORATIO2
00201:
           //PAGESELN
00202:
           while(1)
00203:
00204:
00205:
                _delay_ms(1);
00206:
                _delay_ms(1);
           }
00207:
00208:
00209: } ? end main ?
00210:
00211:
00212:
00213:
00214:
00215:
00216: /
00216: *****
00216: ******
00217:
                        void WriteDataToSRC4392(void)
00218: *
00219: * Description:
00220:
00221: * Input:
                    none
00222: *
00223: *Output:
                    none
00224:
00225: *Globals used:none
```

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00226: *
00227: * Return:
                  none
00228: ********
                                                   ***********
00228: *******
00229: void WriteDataToSrc4392(UINT8 adress, UINT8 data)
00230: {
00231:
          UINT8 write_adress;
00232:
00233:
          write adress = adress;
          SPI_CS_ENABLE();
00234:
00235:
          _delay_us(10);
          SPIWriteData(write_adress);
00236:
          SPIWriteData(0);
00238:
          SPI WriteData(data);
          _delay_us(10);
SPI_CS_DISABLE();
00239:
00240:
00241:
00242: }
00243:
00244: INT8U ReadDataFromSrc4392(UINT8 adress)
00245: {
          UINT8 read_adress, read_data;
00246:
00247:
00248:
          read adress = 0x80 \mid adress;
00249:
          SPI_CS_ENABLE();
00250:
00251:
           _delay_us(10);
          SPI WriteData(read_adress);
00252:
00253:
          SPI WriteData(0)
          read_data = SPIWriteData(0);
00254:
          SPI_CS_DISABLE();
00255:
00256:
00257:
          return read_data;
00258: }
00259:
00260:
00261:
00262:
00263: /*
00263: *****
00263: ******
00264: *
                      void SPIWriteData(void)
00265:
00266: * Description:
00267: *
00268: * Input:
                   none
00269: *
00270: *Output:
                   none
00271:
00272: *Globals used:none
00273: *
00274: * Return:
                   none
00275: **
00275: *******/
00276:
00277: INT8U SPIWriteData(UINT8 data)
00278: {
00279:
          SPDR = data;
          while(! CHECKBIT(SPSR,BIT(SPIF)));
00280:
00281:
00282:
          return SPDR;
00283: }
00284:
00285:
00286:
00287: /*
00287: **********
00287: ******
00288: *
                      void SPIReadData(void)
00289: *
00290: * Description:
00291:
00292: * Input:
                   none
00293: *
00294: *Output:
                  none
00295:
00296: *Globals used:none
00297:
00298: * Return:
                   none
00299: ***
                         *******************
00299: *******/
```

00300:

00301:

00302: 00303: