AKD4137-A
AK4137 Evaluation Board Rev.3

GENERAL DESCRIPTION

The AKD4137-A is the evaluation board for the AK4137, 8k～768kHz asynchronous sample rate converter. This board has the optical connectors to interface with other digital audio equipments and serial interfaces for AKM AD/DA evaluation boards. The AKD4137-A achieves quick evaluation of AK4137

■ **Ordering guide**

AKD4137-A --- Evaluation board for AK4137
Control software included with package

FUNCTION

- ☐ **Optical fiber connectors (for Digital Audio Interface. input x 1, output x 1.)**
- ☐ **10pin Header (for AKM AD/DA evaluation board. input x 1, output x 1.)**
- ☐ **On board X'tal Oscillator (input x 1, output x 1.)**

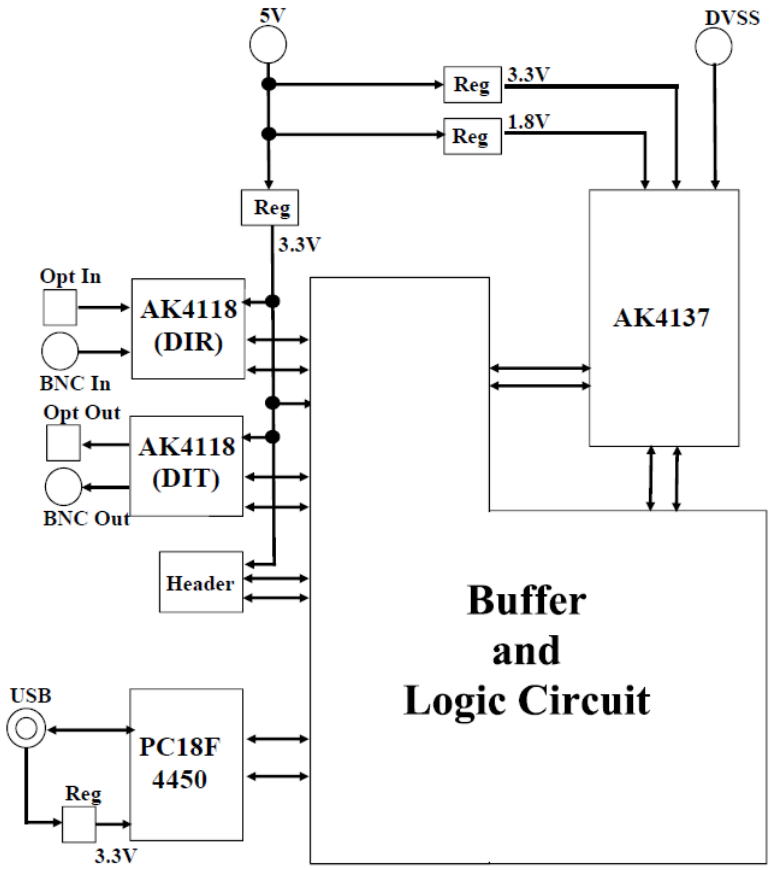

Figure 1. AKD4137-A Block Diagram
*Circuit schematics are attached at the end of this manual.

Evaluation Board Diagram

■ Board Diagram

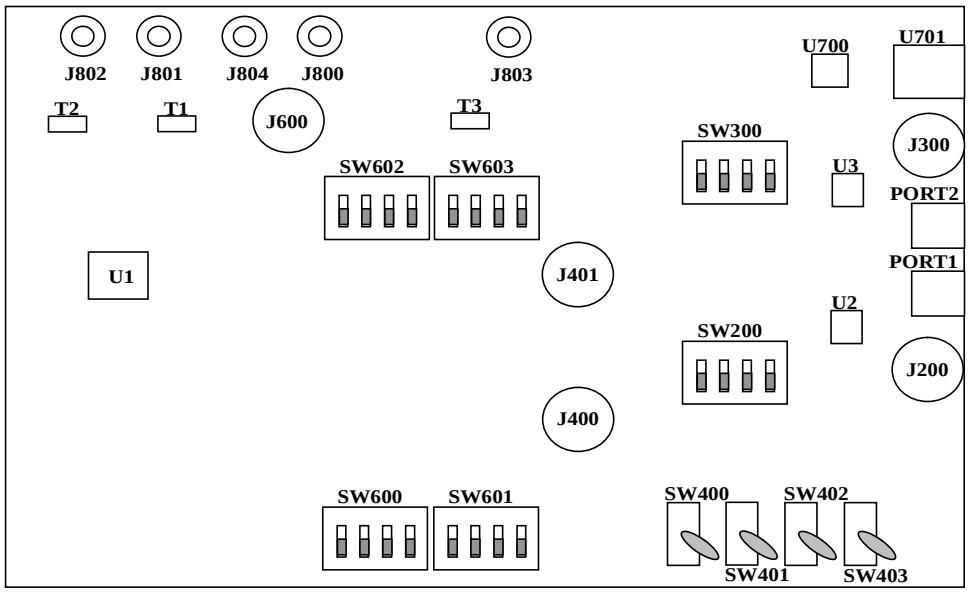

Figure 2. AKD4137-A Board Diagram

■ Description

(1) U1 (AK4137)
2channels input/output Digital Sample Rate Converter (SRC).

(2) J200, J300 (BNC Connector for Digital Input/Output)
J200 BNC connector : Digital Input optical signal to AK4118A(U2).
J300 BNC connector : Digital Output optical signal from AK4118A(U3).

(3) PORT1, PORT2 (Optical Connector)
PORT1 : Digital Input optical signal to AK4118A(U2).
PORT2 : Digital Output optical signal from AK4118A(U3).

(4) J800, J801, J802, J803, J804 (Power supply)
J800 (+5V) : +5V Power Supply
J801 (DVDD) : 3.3V/1.8V Power Supply
J802 (VDD18) : 1.8V Power Supply
J803 (D33V) : 3.3V Power Supply
J804 (DVSS) : GND

(5) U2, U3 (AK4118A)
AK4118A has DIR, DIT and X'tal oscillator.
Transports input data to AK4137 when working in master mode, and output data from AK4137 when working in slave mode.

(6) U700 (PIC18F4550)
USB control chip. Sets up AK4558 registers from PC via USB port (U701).

(7) J400, J401 (BNC Connector)
Input external clock source.

(8) SW200, SW300 (Dip-switch)
DIP type switch. Sets clock and audio format of AK4118A. DIF[2:0] used to set audio interface format and OCKS[1:0] used to master clock frequency.

(9) SW600, SW601, SW602, SW603 (Dip-switch)
DIP type switch. Sets clock and audio format and filter of AK4137.

(10) SW400 (Toggle switch)
Toggle type-switch PDN for AK4137.
"H" : PDN = High
"L" : PDN = Low

(11) SW401, SW402 (Toggle switch)
Toggle type-switch PDN for AK4118A.
"H" : PDN = High
"L" : PDN = Low

(12) SW403 (Toggle switch)
Toggle type-switch SMUTE for AK4137.
"H" : SMUTE = High
"L" : SMUTE = Low

(13) T1, T2, T3 (regulator)
Regulator for AK4137, AK4118A, Logic Circuit.
T1 : Regulated DVDD (3.3V) from +5V.
T2 : Regulated DVDD, DV18 (1.8V) from +5V.
T3 : Regulated D33V (3.3V) from +5V.

■ **Operation sequence**

[1] Power supply line settings

[2] Jumped pins settings

[3] DIP switches settings

[4] Toggle switches settings

[5] Register control (Serial control)

[6] Evaluation modes

[1] Power supply line settings

(1-1) Power supply settings : Used the regulator (T1,T2,T3) <Default>

Set up the power supplied lines :
* Each supply line should be distributed from the power supply unit.

Name		Color	Setting (Typ)	Function	Comments	Default Settings
J800	+5V	Red	+5V	Regulator power supply	Should always be connected	+5V
J801	DVDD	Green	+3.3V/+1.8V	AK4137 DVDD, Logic IC power supply	3.3V regulator is used, JP801=3.3V short and JP800=REG short by default. When jack is used, JP800=JACK short. When 1.8V regulator is used, JP801=1.8V short and JP800=REG short.	OPEN : (JP801=3.3V short and JP800=REG short)
J802	DV18	Green	+1.8V	AK4137 DV18	1.8V regulator is used, JP802=REG short by default. When jack is used, JP802=JACK short.	OPEN : (JP802= open)
J803	D33V	Green	+3.3V	AK4118A 3.3V VDD, Logic IC power supply	3.3V regulator is used, JP803=REG short by default. When jack is used, JP803=JACK short.	OPEN : (JP803=REG short)
J706	DVSS	Black	0V	Ground	Should always be connected	0V

Table 1-1. Power supply line setting (default: used the regulator)

(1-2) About jumper for power supply :

The roles of the jumper for each power supply supplied from the regulator are as follows.

Connection of the jumper for power supply :

Name		Function	Comments	Default Settings
JP800	DVDD-SEL	Select regulator power supply or jack for DVDD.	DVDD for AK4137 and Logic IC: JP800=REG short : 3.3V regulator is used by default. JP800=JACK short : Jack is used.	REG : JP800=REG short
JP801	DVDD-VSEL	Select regulator power supply 3.3V or 1.8V for DVDD.	DVDD for AK4137 and Logic IC: JP801=3.3V short : 3.3V regulator is used by default. JP801=1.8V short : 1.8V regulator is used.	REG : JP801=3.3V short
JP802	DV18-SEL	Select regulator power supply or jack for DV18.	DV18 for AK4137: JP802=REG short : 1.8V regulator is used. JP802=JACK short : Jack is used.	OPEN : JP802=Open
JP803	D33V-SEL	Select regulator power supply or jack for D33V.	D33V for Logic IC: JP803=REG short : 3.3V regulator is used by default. JP803=D3.3V short : Jack is used.	REG : JP803=REG short
JP100	DV18-SEL	Select External power supply or LDO power supply of AK4137 for DV18.	DV18 selector for AK4137: JP100=short and JP802=open : LDO of AK4137 is used by default. JP100=short and JP802=short : External Power supply is used.	LDO power : JP100=short and JP802=open

Table 1-2. Jumper for power supply

[2] Jumper pins and Port pins settings

No	Names		Default	Functions
1	JP100	DV18-SEL	Short	Select Short / Open DV18. Open: DV18 pin of AK4137 open. Short: DV18 pin of AK4137 connect 1.8Vcourse. (default)
2	JP200	RXDATA-SEL	OPT	Select OPT/COAX input for RX data. (DIR:AK4118A) OPT: Optical input COAX: COAX(BNC) input
3	JP300	TXDATA-SEL	OPT	Select OPT/COAX output for TX data. (DIT:AK4118A) OPT: Optical output COAX: COAX(BNC) output
4	JP400	BICK-R-SEL	DIR	Select Rx BICK. DIR: BICK-4118A-R(DIR) (default) PORT400: PORT400-IBICK GND: DVSS short
5	JP401	BICK-R-PHASE	THR	Select polarity (non-inverted output / inverted output) of BICK－R-SEL outputs. THR: Non-inverted output. (default) INV: Inverted output.
6	JP402	LRCK-R-SEL	DIR	Select Rx LRCK. DIR: LRCK-4118A-R(DIR) (default) PORT400: PORT400-ILRCK GND: DVSS short
7	JP403	SDTI-R-SEL	DIR	Select Rx DATA. DIR: SDTO-4118A-R(DIR) (default) PORT400: PORT400-SDTI GND: DVSS short
8	JP404	MCLK-R-SEL	DIR	Select Rx MCLK. DIR: MCLK-4118A-R(DIR) (default) PORT400: PORT400-IMCLK EXT: External MCLK (JACK: J400 EXT-R) input. GND: DVSS short
9	JP405	EXT-R	Open	Open: No input (default) Short: External MCLK (JACK: J400 EXT-R) input.
10	JP406	TDMI-EXT-SEL	Open	Select TDMI data. PORT400: PORT400-SDTI(DIR) PORT401: PORT401-SDTO(DIT) EXT: External TDMI (JP407: TDMI-EXT) input. GND: DVSS short
11	JP407	TDMI-EXT	Open	Open: External TDMI (JP407: TDMI-EXT) input. Short: DVSS short
12	JP408	BICK-T-SEL	DIT	Select Tx BICK. DIT: BICK-4118A-T(DIT) (default) PORT401: PORT401-OBICK GND: DVSS short
13	JP409	BICK-T-PHASE	THR	Select polarity (non-inverted output / inverted output) of BICK-T-SEL outputs. THR: Non-inverted output. (default) INV: Inverted output.

No	Names		Default	Functions
14	JP410	LRCK-T-SEL	DIT	Select Tx LRCK. DIT: LRCK-4118A-T(DIT) (default) PORT401: PORT401-OLRCK GND: DVSS short
15	JP411	SDTO-T-SEL	DIT	Select Tx DATA. DIR: DAUX-4118A-T(DIT) (default) PORT401: PORT401-SDTO GND: DVSS short
16	JP412	MCLK-T-SEL	DIT	Select Tx MCLK. DIT: MCLK-4118A-T(DIT) (default) PORT401: PORT401-OMCLK EXT: External MCLK (JACK: J401 EXT-T) input. GND: DVSS short
17	JP413	EXT-T	Open	Open: No input (default) Short: External MCLK (JACK: J401 EXT-T) input.
18	PORT400	RX-PORT	Open	Open: No input (default) Monitor: PCM(RX) data and Clock input.
19	PORT401	TX-PORT	Open	Open: No input / output (default) Monitor: PCM(TX) data and Clock input / output.
20	PORT402	PCMI-PORT	ALL Short	ALL Short: RX data and Clock input. (default) ALL Open: No data (PCM input data and clock)
21	PORT403	PCM/DSD-SEL	PCM	PCM: PCM data and clock input / output. (default) DSD: DSD data and clock input / output.
22	PORT404	DSDI-PORT	Open	Open: No input (default) Monitor: DSD data and Clock input.
23	PORT405	DSD-PORT	Open	Open: No input / output (default) Monitor: DSD data and Clock input / output.
24	JP500	PCM/DSD-SEL1	PCM	PCM: PCM data (SDTO (TX)) output. (default) DSD: DSD data (DSDOL (TX)) output.
25	JP501	PCM/DSD-SEL2	PCM	PCM: PCM clock (OBICK (TX)) input / output. (default) DSD: DSD clock (ODCLK (TX)) input / output.
26	JP502	PCM/DSD-SEL3	PCM	PCM: PCM clock (OLRCK (TX)) input / output. (default) DSD: DSD data (DSDOR (TX)) output.
27	JP600	DEM0	Short	Short: DEM0 for PCM Mode. (default) Open: DSDIL data for DSD Mode.
28	JP601	DEM1	Short	Short: DEM1 for PCM Mode. (default) Open: DSDIR data for DSD Mode.
29	JP602	CAD0/IDIF0	CAD0	CAD0: Chip address 0 in serial control mode. (default) IDIF0: Digital Input Format 0 in parallel control mode.
30	JP603	CAD1/IDIF1	CAD1	CAD1: Chip address 1 in serial control mode. (default) IDIF1: Digital Input Format 1 in parallel control mode.
31	JP604	IDIF2/TDO0	IDIF2	IDIF2: Digital Input Format 2 in parallel control mode. TDO0: Test Output
32	JP605	TDO0	Open	Test Output TDO0 monitor pin.
33	JP606	SRCE-N	Open	Unlock status SRCE_N monitor pin.
34	JP607	TEST0	VSS	TEST0: TEST0 input TEST00 (SW601-TEST0). VSS: Connected to DVSS.

No	Names		Default	Functions
35	JP608	TEST1	VSS	TEST1: TEST1 input TEST10 (SW601-TEST1). VSS: Connected to DVSS.
36	JP609	XTI/OMCLK/TDMI-SEL	Open	XTI=Open: Normal use. (default) XTI=Short: XTI be connected to DVSS OMCLK: OMCLK be connected to MCLK-Rx or MCLK-Tx. TDMI: TDMI-EXT
37	JP610	OMCLK-SEL	Open	R: MCLK-R (Rx MCLK) T: MCLK-T (Tx MCLK)
38	JP611	SDA/CDTI/SLOW	SDA/CDTI	SDA/CDTI: Control Data Output / Input in serial control mode. (default) SLOW: Digital Filter Select in parallel control mode.
39	JP612	SCL/CCLK/SD	SCL/CCLK	SCL/CCLK: Control Data / Clock Input in serial control mode. (default) SD: Digital Filter Select in parallel control mode.
40	JP613	CSN/SMUTE	CSN	CSN: Chip Select in serial control mode. (default) SMUTE: Soft Mute in parallel control mode.
41	JP614	ODIF1/TDO1	ODIF1	ODIF1: Audio Interface Format 1 for Output PORT. TDO1: Test Output
42	JP615	TDO1	Open	Test Output TDO1 monitor pin.
43	JP616	ODIF0/TDO2	ODIF0	ODIF0: Audio Interface Format 0 for Output PORT. TDO2: Test Output
44	JP617	TDO2	Open	Test Output TDO2 monitor pin.
45	JP618	TDM/TDO3	TDM	TDM: TDM Format select. TDO3: Test Output
46	JP619	TDO3	Open	Test Output TDO3 monitor pin.
47	JP620	OBIT0/TDO4	OBIT0	OBIT0: Bit Length select 0 for Output PORT. TDO4: Test Output
48	JP621	TDO4	Open	Test Output TDO4 monitor pin.
49	JP622	OBIT1	OBIT1-HL	OBIT1-HL: Bit Length select 1 for Output PORT. OBIT1-EXT: External Input Data (JP623 OBIT1EXT)
50	JP623	OBIT1EXT	Open	External Input OBIT1 input pin.
51	JP624	CM0/TDO5	CM0	CM0: Clock select or Mode select 0 for Output PORT. TDO5: Test Output
52	JP625	TDO5	Open	Test Output TDO5 monitor pin.
53	JP626	CM2/TDO6	CM2	CM2: Clock select or Mode select 2 for Output PORT. TDO6: Test Output
54	JP627	TDO6	Open	Test Output TDO6 monitor pin.
55	JP628	MCKO-EXT	Open	Open: No output (default) Short: External MCLK (JACK: J600 EXT-MCKO) output.
56	PORT700	PIC	Open	Pin header for write Firmware of Control soft by USB Interface.
57	PORT701	CTRL-SEL	USB	Control PORT Select. ALL USB short: USB Port U701 used. ALL 10pin short: 10pin Port PORT700 used
58	JP800	DVDD-SEL	REG	Select Regulator or JACK for DVDD REG: Regulator T1 or T2 is used (default) JACK: JACK J801-DVDD is used.
59	JP801	DVDD-VSEL	3.3V	Select Voltage for DVDD 3.3V short: 3.3V regulator T1 is used. (default) 1.8V short: 1.8V regulator T2 is used.

No	Names		Default	Functions
60	JP802	DV18-SEL	Open	Select Regulator or JACK for DV18 REG: Regulator T2 is used. JACK: JACK J802-DV18 is used.
61	JP803	D33V-SEL	REG	Select Regulator or JACK for D33V REG: Regulator T3 is used (default) D3.3V: JACK J803-D3.3V is used.

Table 2-1. Jumper pin setting

[3] DIP switches settings

(3-1). Setting for SW200 / SW300
(Sets AK4118A (U2 / U3) audio format and master clock setting)

No.	Switch Name	Function	default
1	DIF2	Set-up of DIF2 pin.	H
2	DIF1	Set-up of DIF1 pin.	L
3	DIF0	Set-up of DIF0 pin.	H
4	OCKS1	Set-up of OCKS1 pin.	H
5	OCKS0	Set-up of OCKS0 pin.	L

Table 3-1. SW200 / SW300 Setting

Mode	DIF2 pin	DIF1 pin	DIF0 pin	DAUX	SDTO	LRCK		BICK		
	DIF2 bit	DIF1 bit	DIF0 bit				I/O		I/O	
0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
1	0	0	1	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
2	0	1	0	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
3	0	1	1	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
4	1	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	
5	1	0	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	default
6	1	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I	
7	1	1	1	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I	

Table 3-2. Audio format (AK4118A)

OCKS1 pin	OCKS0 pin	(X'tal)	MCKO1	MCKO2	fs (max)	
OCKS1 bit	OCKS0 bit					
0	0	256fs	256fs	256fs	96 kHz	
0	1	256fs	256fs	128fs	96 kHz	
1	0	512fs	512fs	256fs	48 kHz	default
1	1	128fs	128fs	64fs	192 kHz	

Table 3-3. Master Clock Frequency Select (AK4118A)

(3-2). Setting for SW600 / SW601 / SW602 / SW603 (Sets AK4137 (U1))

No.	Switch Name	Function	default
1	DEM1	De-emphasis Control 1 in PCM mode.	L
2	DEM0	De-emphasis Control 0 in PCM mode.	H
3	CAD1	Chip Address 1 in serial control mode.	L
4	CAD0	Chip Address 0 in serial control mode.	L
5	IDIF2	Digital Input Format 2 in Parallel control mode.	L
6	IDIF1	Digital Input Format 1 in Parallel control mode.	H
7	IDIF0	Digital Input Format 0 in Parallel control mode.	H
8	I2C	Select serial mode L: 4-wire serial mode H: I2C mode	H

Table 3-4. SW600 Setting (AK4137)

No.	Switch Name	Function	default
1	TEST1	TEST1 pin setting.	L
2	TEST0	TEST0 pin setting.	L
3	PSN	Parallel / Serial control mode select. L: Serial control mode H: Parallel control mode	L
4	SLOW	Digital Filter select in parallel control mode.	L
5	SD	Digital Filter select in parallel control mode.	L
6	ODIF1	Audio Interface Format 1 for Output PORT.	H
7	ODIF0	Audio Interface Format 0 for Output PORT.	H
8	DITHER	Dither Enable L: Dither OFF H: Dither ON	L

Table 3-5. SW601 Setting (AK4137)

No.	Switch Name	Function	default
1	SMSEMI	Soft Mute Semi Auto mode L: Manual mode H: Semi Auto mode	L
2	SMT1	Soft Mute Timer select 1	L
3	SMT0	Soft Mute Timer select 0	L
4	TDM	TDM Format select L: Stereo mode (connected to DVSS) H: TDM mode for output (connected to DVDD)	L
5	CLKMODE	Master clock select L: X’tal mode (connected to DVSS) H: External master clock or TDM=”H” (connected to DVDD)	L
6	VSEL	Digital Power select L: DV18 is Output H: DV18 is Power supply	L
7	OBIT1	Bit Length select 1 for Output PORT.	L
8	OBIT0	Bit Length select 0 for Output PORT.	L

Table 3-6. SW602 Setting (AK4137)

No.	Switch Name	Function	default
1	CM3	Clock select or Mode setting 3	L
2	CM2	Clock select or Mode setting 2	H
3	CM1	Clock select or Mode setting 1	L
4	CM0	Clock select or Mode setting 0	L
5	-	Not used	-
6	-	Not used	-
7	-	Not used	-
8	-	Not used	-

Table 3-7. SW603 Setting (AK4137)

[4] Toggle switches settings

Up="H", Down="L"

[SW400] (Power Down (PDN) for AK4137):
Power Down (PDN) Switch for AK4137
Reset AK4137 (U1) once by brining SW400 to "L" once upon power-up.
Keep "H" when AK4137 is in use; keep "L" when AK4137 is not in use.

[SW401] (Power Down (PDN) for AK4118A-Rx):
Power Down (PDN) Switch for AK4118A-Rx
Reset AK4118A (U2) once by brining SW401 to "L" once upon power-up.
Keep "H" when AK4118A is in use; keep "L" when AK4118A is not in use.

[SW402] (Power Down (PDN) for AK4118A-Tx):
Power Down (PDN) Switch for AK4118A-Tx
Reset AK4118A (U3) once by brining SW402 to "L" once upon power-up.
Keep "H" when AK4118A is in use; keep "L" when AK4118A is not in use.

[SW403] (Soft Mute (SMUTE) for AK4137):
Soft Mute (SMUTE) Switch for AK4137
When this switch is changed to "H", soft mute cycle is initiated.
When returning "L", the output mute releases.

[5] Register control (Serial control)

AKD4137-A can be controlled via USB (serial port). Connect board to PC using the USB cable (PORT600 - serial) included with the AKD4137-A.

The control software is packed with the evaluation board. The software operation sequence is included in the evaluation board manual.

[6] Evaluation modes

(6-1) PCM Mode (PCMIN → SRC → PCMOUT) (Slave Mode)

■ **Toggle switch setting:**

SW400	SW401	SW402
L→H	L→H	L→H
AK4137(U1) : Used	AK4118A(U2) : Used	AK4118A(U3) : Used

Table 6-1. Toggle switch setting

■ **Start up Control Register Setting**

1: Jumpers and Dip-switches and Toggle-switches are default setting.
2: Port Reset & Write Default.
3: Set Addr: 01h = "13" to setting Audio Data Interface Mode I2S for Input Digital Data on AK4137.
: Other control register settings are default.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	PCMONT0	SLOW	SD	DEM1	DEM0	DITHER	IDIF2	IDIF1	IDIF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	1	0

Table 6-2. Addr 01H control register setting

SLOW bit: Set FIR1 Filter Coefficient
0: Sharp Roll OFF Filter (default)
1: Slow Roll OFF Filter
SD bit: Set FIR1 Filter Coefficient
0: Normal Delay Filter (default)
1: Short Delay Filter
DEM1/0 bit: De-enphasis Control
00: 44.1kHz
01: OFF (default)
10: 48kHz
11: 32kHz
DITHER bit: Add Dither
0: Dither OFF (default)
1: Dither ON
IDIF2/1/0 bit: Set Audio Data Interface Mode for Input Digital Data
000: 32bit, LSB justified
001: 24bit, LSB justified
010: 32bit, MSB justified (default)
011: 32 or 16bit, I2S compatible
100: TDM 32bit, LSB justified
101: TDM 32bit, I2S compatible
110: TDM 32bit, MSB justified
111: TDM 32bit, I2S compatible
SMSEMI bit: Semi Auto Soft Mute
0: Semi Auto Soft Mute OFF (default)
1: Semi Auto Soft Mute ON

(6-2) PCMIN → DSDOUT Mode (PCMIN → SRC → DSDOUT) (PCM → DSD Mode)

■ **Toggle switch setting:**

SW400	SW401	SW402
L→H	L→H	L
AK4137(U1) : Used	AK4118A(U2) : Used	AK4118A(U3) : Not Used

Table 6-3. Toggle switch setting

■ **Start up Control Register Setting**

1: Jumpers and Dip-switches and Toggle-switches are changed for DSD Mode for AK4137 Output.
: PORT403 = "DSD", JP500 = "DSD", JP501 = "DSD", JP502 = "DSD"
: SW600 = "LHLLHHH" (SW600-3,4pin (CAD1,0) = "LL", SW600-8pin (I2C) = "H")
: SW601 = "LLLLLHHL" (SW601-3pin (PSN) = "L")
: SW602 = "LLLLLLLL"
: SW603 = "LLLLLLLL" or "LLLHLLLL" or "LLHLLLLL" or "LLHHLLLL" or "LHLHLLLL"
(SW603-1,2,3,4pin (CM3-0) = Master mode)
: Other settings are default settings.
(JP602 = "CAD0", JP603 = "CAD1")
2: Port Reset & Write Default.
3: Set Addr: 04h = "53" to setting DSD Output Mode on AK4137.
Set Addr: 01h = "13" to setting Audio Data Interface Mode I2S for Input Digital Data on AK4137.
: Other control register settings are default.

Input Data : J200 (RX-COAX) or PORT1 (RX-OPT)
Output Data : PORT405 (DSDO-PORT)

Jumpers Setting: DSD Mode

Names		Change	Functions
PORT403	PCM/DSD-SEL	DSD	PCM: PCM data and clock input / output. (default) DSD: DSD data and clock input / output.
JP500	PCM/DSD-SEL1	DSD	PCM: PCM data (SDTO (TX)) output. (default) DSD: DSD data (DSDOL (TX)) output.
JP501	PCM/DSD-SEL2	DSD	PCM: PCM clock (OBICK (TX)) input / output. (default) DSD: DSD clock (ODCLK (TX)) input / output.
JP502	PCM/DSD-SEL3	DSD	PCM: PCM clock (OLRCK (TX)) input / output. (default) DSD: DSD data (DSDOR (TX)) output.

Table 6-4. Jumper setting

Control Register setting:

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	DSDOCONT	DSDCLP1	DSDCLP0	DSDOFS1	DSDOFS0	ERRMASK	PMO	OCKB	DSDOE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	0	0	0	0

Table 6-5. Addr 04H control register setting

DSDCLP1/0 bit: Set Clip processing
00: no Clip processing
01: Clip processing [-6dB] (default)
10: Clip processing [-9dB]
11: Reserved (Clip processing [-6dB])
DSDOFS1/0 bit: Set DSD Output FS
00: 64fs
01: 128fs (default)
10: 256fs
11: Reserved (128fs)
ERRMASK bit: MASK Reset
0: Error Detect and Reset (default)
1: Error Detect and Not Reset
PMO bit: Set DSD Output Phase Modulation

0: Not Phase Modulation Mode (default)
1: Phase Modulation Mode

ODCKB bit: Polarity of ODCLK (DSD Output)
0: DSD data is output from ODCLK falling edge (default)
1: DSD data is output from ODCLK rising edge

DSDOE bit: DSD Output Enable
0: DSD Output Mode OFF (default)
1: DSD Output Mode ON

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	PCMONT0	SLOW	SD	DEM1	DEM0	DITHER	IDIF2	IDIF1	IDIF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	1	0

Table 6-6. Addr 01H control register setting

IDIF2/1/0 bit: Set Audio Data Interface Mode for Input Digital Data
000: 32bit, LSB justified
001: 24bit, LSB justified
010: 32bit, MSB justified (default)
011: 32 or 16bit, I2S compatible
100: TDM 32bit, LSB justified
101: TDM 32bit, I2S compatible
110: TDM 32bit, MSB justified
111: TDM 32bit, I2S compatible

(6-3) DSDIN → DSDOUT Mode (DSDMIN → SRC → DSDOUT) (DSD → DSD Mode)

■ **Toggle switch setting:**

SW400	SW401	SW402
L→H	H	H
AK4137(U1) : Used	AK4118A(U2) : Not Used	AK4118A(U3) : Not Used

Table 6-7. Toggle switch setting

■ **Start up Control Register Setting**

1: Jumpers and Dip-switches and Toggle-switches are changed for DSD Mode for AK4137 Input / Output.
: PORT403 = "DSD", JP500 = "DSD", JP501 = "DSD", JP502 = "DSD"
: JP600 = open, JP601 = open
: SW600 = "LHLLHHH" (SW600-3,4pin (CAD1,0) = "LL", SW600-8pin (I2C) = "H")
: SW601 = "LLLLLHHL" (SW601-3pin (PSN) = "L")
: SW602 = "LLLLLLLL"
: SW603 = "LLLLLLLL" or "LLLHLLLL" or "LLHLLLLL" or "LLHHLLLL" or "LHLHLLLL"
(SW603-1,2,3,4pin (CM3-0) = Master mode)
: Other settings are default settings.
(JP602 = "CAD0", JP603 = "CAD1")
2: Port Reset & Write Default.
3: Set Addr: 03h = "13" to setting DSD Input Mode on AK4137.
Set Addr: 04h = "53" to setting DSD Output Mode on AK4137.
: Other control register settings are default.

Input Data : PORT404 (DSDI-PORT)
Output Data : PORT405 (DSDO-PORT)

Jumpers Setting: DSD Mode

Names		Change	Functions
PORT403	PCM/DSD-SEL	DSD	PCM: PCM data and clock input / output. (default) DSD: DSD data and clock input / output.
JP500	PCM/DSD-SEL1	DSD	PCM: PCM data (SDTO (TX)) output. (default) DSD: DSD data (DSDOL (TX)) output.
JP501	PCM/DSD-SEL2	DSD	PCM: PCM clock (OBICK (TX)) input / output. (default) DSD: DSD clock (ODCLK (TX)) input / output.
JP502	PCM/DSD-SEL3	DSD	PCM: PCM clock (OLRCK (TX)) input / output. (default) DSD: DSD data (DSDOR (TX)) output.
JP600	DEM0	Open	Short: DEM0 for PCM Mode. (default) Open: DSDIL data for DSD Mode.
JP601	DEM1	Open	Short: DEM1 for PCM Mode. (default) Open: DSDIR data for DSD Mode.

Table 6-8. Jumper setting

Control Register setting:

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	DSDICONT	PCMFSO1	PCMFS0	DSDIFS1	DSDIFS0	DOP	PMI	IDCKB	DSDIE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	0	0

Table 6-9. Addr 04H control register setting

PCMFS1/0 bit: Set PCM Output Sampling Frequency
00: 44.1kHz or 48kHz (Cuo Off 20kHz) (default)
01: 88.2kHz or 96kHz (Cut Off 40kHz)
10: 176.4kHz or 192kHz (Cut Off 80kHz)
11: More than 384kHz

DSDIFS1/0 bit: Set DSD Input FS
00: 64fs
01: 128fs (default)
10: 256fs

11: Reserved (128fs)

DOP bit: Set DSD On PCM Mode
0: OFF (default)
1: ON

PMI bit: Set DSD Iput Phase Modulation
0: Not Phase Modulation Mode (default)
1: Phase Modulation Mode

IDCKB bit: Polarity of IDCLK (DSD Input)
0: DSD data is input from IDCLK falling edge (default)
1: DSD data is input from IDCLK rising edge

DSDIE bit: DSD Input Enable
0: DSD Input Mode OFF (default)
1: DSD Input Mode ON

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	DSDOCONT	DSDCLP1	DSDCLP0	DSDOFS1	DSDOFS0	ERRMASK	PMO	ODCKB	DSDOE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	0	0	0	0

Table 6-10. Addr 04H control register setting

DSDOFS1/0 bit: Set DSD Output FS
00: 64fs
01: 128fs (default)
10: 256fs
11: Reserved (128fs)

ODCKB bit: Polarity of ODCLK (DSD Output)
0: DSD data is output from ODCLK falling edge (default)
1: DSD data is output from ODCLK rising edge

DSDOE bit: DSD Output Enable
0: DSD Output Mode OFF (default)
1: DSD Output Mode ON

Control Software Manual

■ Set-up evaluation board and control software

1. Set up the evaluation board as needed, according to the previous terms.
2. Connect the evaluation board to a PC with USB cable.
3. USB control is recognized as HID (Human Interface Device) on PC. When it is not recognized properly, please reconnect the evaluation board to PC.
4. Insert the CD-ROM labeled “AKD137-A Evaluation Kit” into the CD-ROM drive.
5. Access the CD-ROM drive and double-click the icon “akd4137-A.exe” to open the control program.
6. Begin evaluation by following the procedure below.

The following operation screen will be shown. (Default setting)

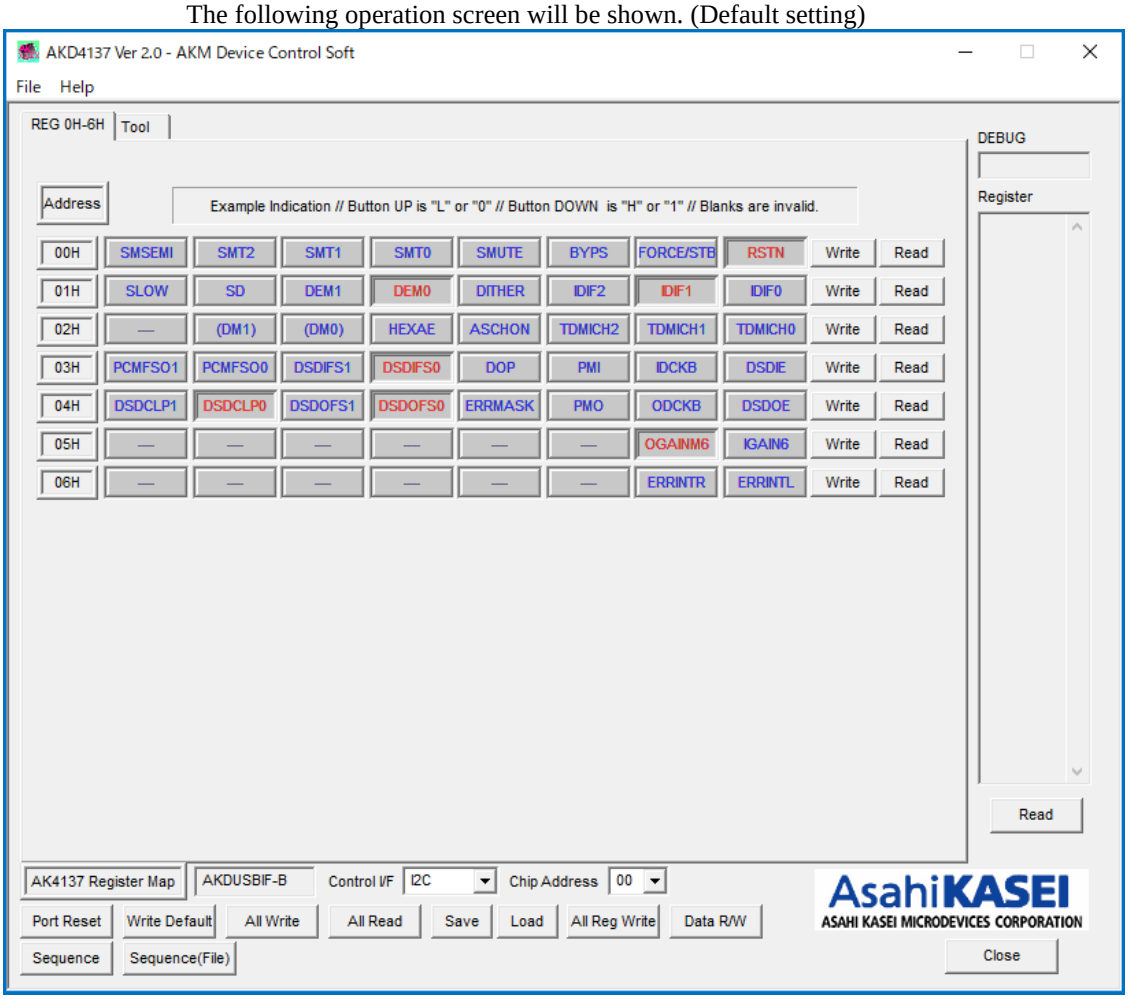

Figure7-1. Control software window

■ Operation Overview

Register map is controlled by this control software.

Frequently used buttons, such as the register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “Dialog Box” section for details of each dialog box setting.

1. [Port Reset] : Reset connection to PC. (Set up USB interface board (AKDUSBIF-B).)
   Click this button after the control software starts up and the evaluation board is connected to the PC via USB cable.
2. [Write Default] : Register Initialization.
   Use this button to initialize the registers when the device is reset by a hardware reset.
3. [All Write] : Execute write command for all registers displayed.
4. [All Read] : Execute read command for all registers displayed. (Note.100)
5. [Save] : Save current register settings to a file.
6. [Load] : Execute data write from a saved file.
7. [All Reg Write] : [All Reg Write] dialog box pops up.
8. [Data R/W] : [Data R/W] dialog box pops up.
9. [Sequence] : [Sequence] dialog box pops up.
10. [Sequence(File)] : [Sequence(File)] dialog box pops up.
11. [Read] : Read and display current register setting in register window (on right side of main window).
    Different from [All Read] as it does not reflect to the register map.
12. [Close] : Close Control Software window.

Note 100. The [All Read] button is only valid when the interface mode for register control is in I²C bus control mode.

When input dummy command settings to AK4137 and the connection error by the evaluation board to a PC with USB cable, the following No Ack error message will pop up. Click “OK”.

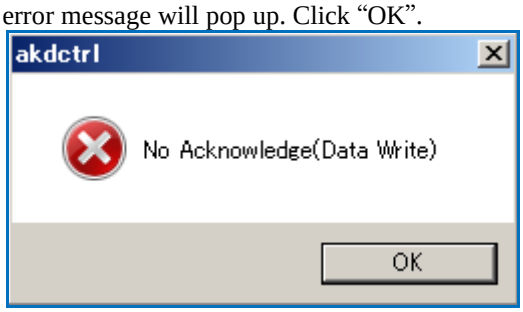

Figure 7-2. No ack message window

Tab Functions

1. [REG] Tab: Register Map

This tab is for register read and write.

Each bit on the register map is a push-button switch.
Button Down indicates “1” and the bit name is shown in red (when read-only the name is shown in dark red).
Button Up indicates “0” and the bit name is shown in blue (when read-only the name is shown in gray)

Grayed out registers are Read-Only registers. They cannot be controlled.

The registers which are not defined on the datasheet are indicated as “---”.

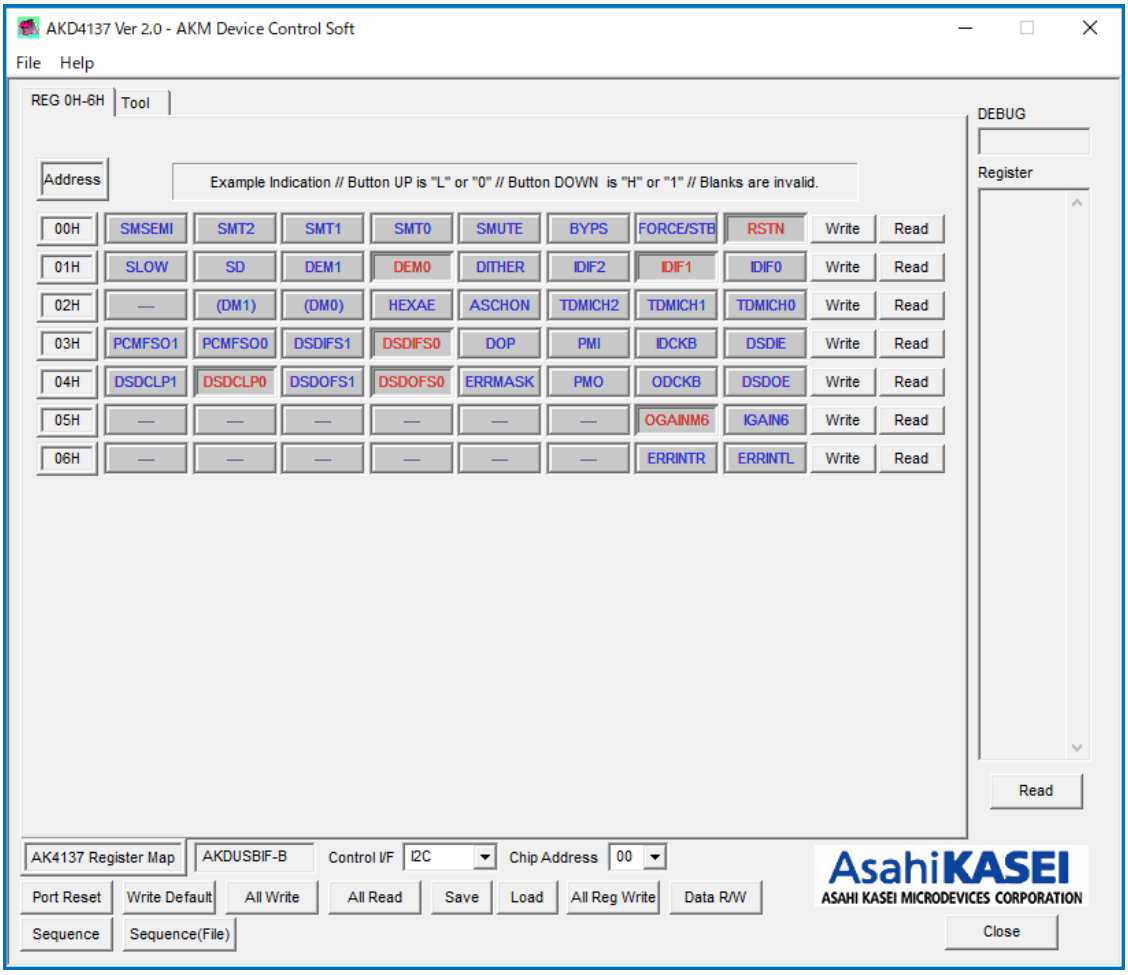

Figure 7-3. [REG] window (REG 00H-06H)

2. [Tool] Tab: Testing Tools

This tab screen is for the evaluation testing tool.
Click button for each testing tool.

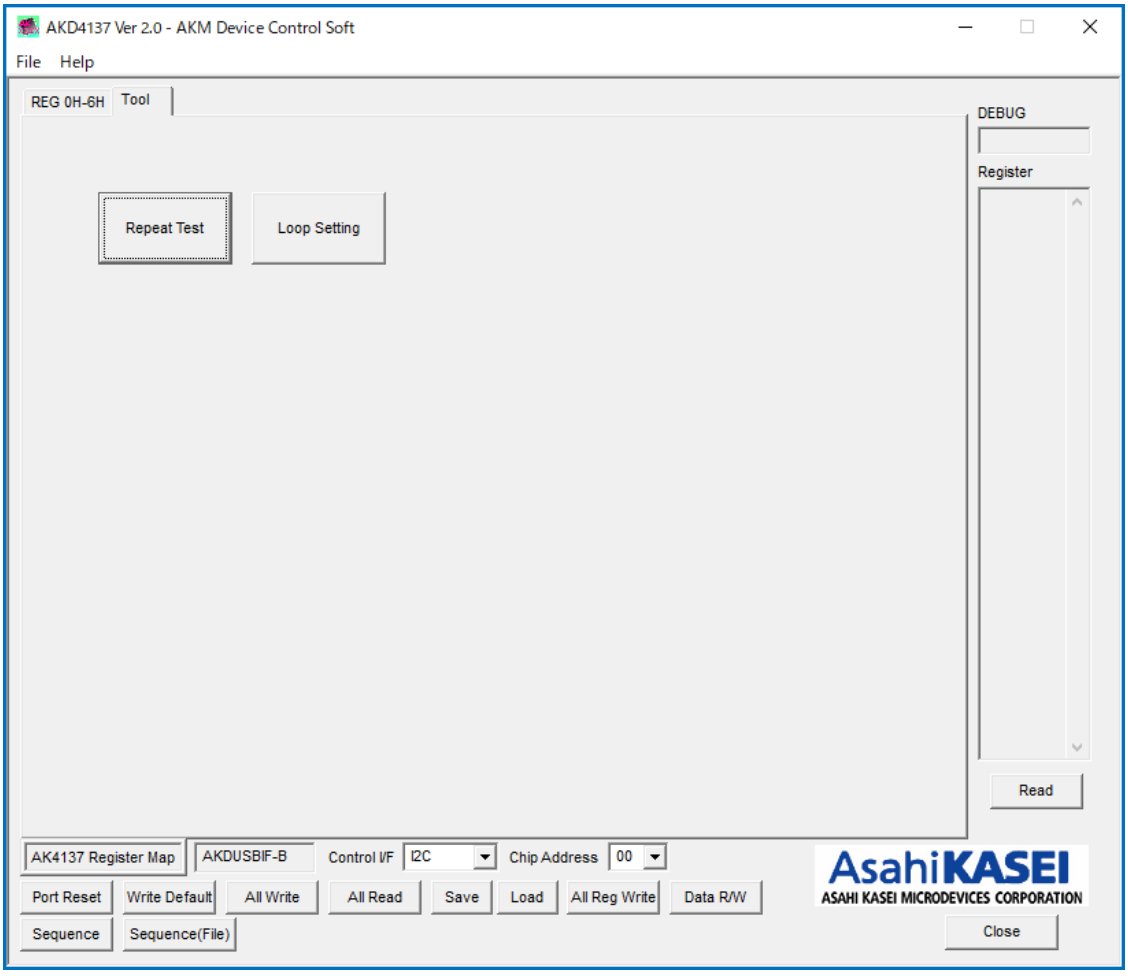

Figure 7-4. [Tool] window

■ Dialog boxes

1. [Write] button: Data Write Dialog

Select the [Write] button located on the right of the each corresponding address when changing two or more bits on the same address simultaneously.

Click the [Write] button for the register pop-up dialog box shown below.

When the checkbox next to the register is checked, the data will become “1”. When the checkbox is not checked, the data will become “0”. Click [OK] to write the set values to the registers, or click [Cancel] to cancel this setting.

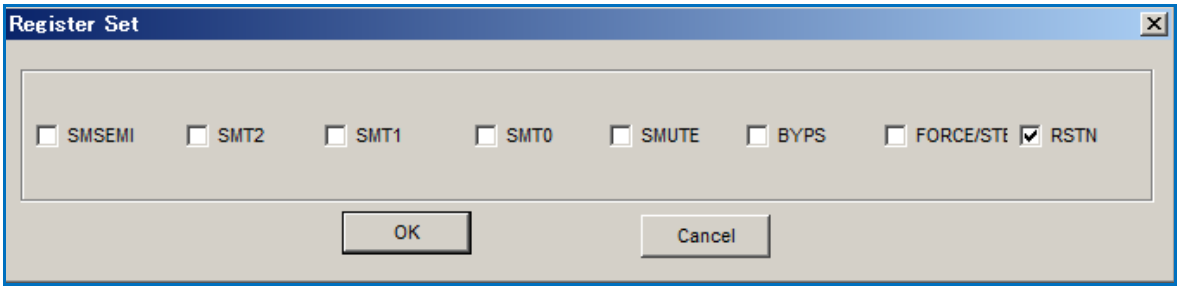

Figure 7-5. Register set window

2. [Read] button: Data Read (Only in I²C-bus Control Mode)

Click the [Read] button located on the right of the each corresponding address to execute a register read.

The current register value will be displayed in the register window as well as in the upper right hand DEBUG window.
Button Down indicates “1” and the bit name is shown in red (when read only the bit name is shown in dark red).
Button Up indicates “0” and the bit name is shown in blue (when read only the bit name is shown in gray)

3. [All Register Write]: All Register Write dialog box

Click [All Reg Write] button in the main window to open register setting file window shown below.
Register setting files saved by [SAVE] button may be applied.

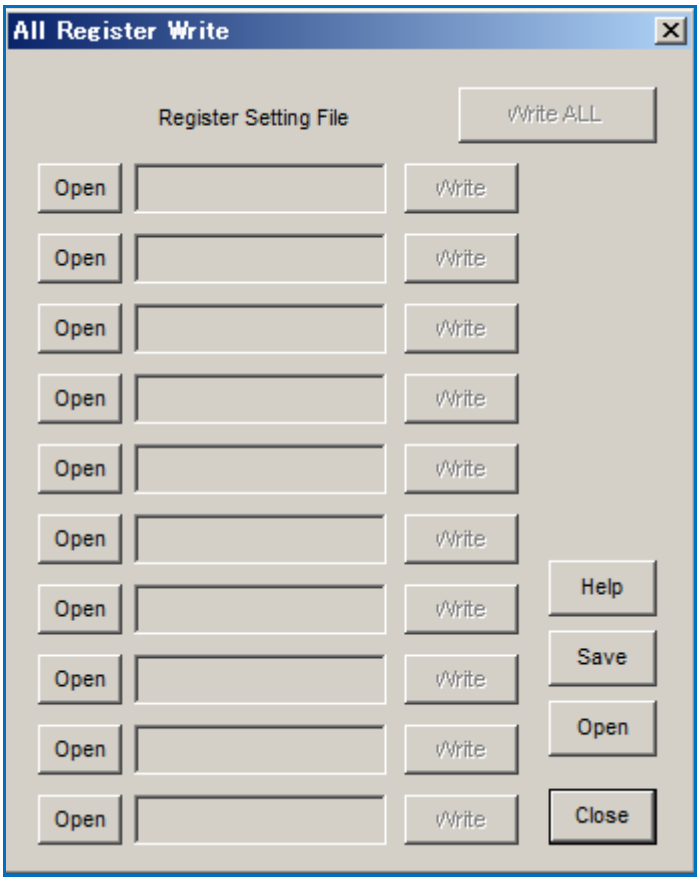

Figure 7-6. Window of [All Reg Write]

[Open (left)] : Select a register setting file (*.akr).
[Write] : Execute register write with selected setting file.
[Write All] : Execute register write with all selected setting files.
Selected files are executed in descending order.
[Help] : Open help window.
[Save] : Save register setting file assignment. File name is “*.mar”.
[Open (right)]: Open saved register setting file assignment “*. mar”.
[Close] : Close dialog box and finish process.

~ Operating Suggestions ~

1. Files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mar” should be stored in the same folder.
2. When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

4. [Data Read/Write]: Data R/W Dialog Box

Click the [Data R/W] button in the main window for data read/write dialog box.
Data is written to the specified address.

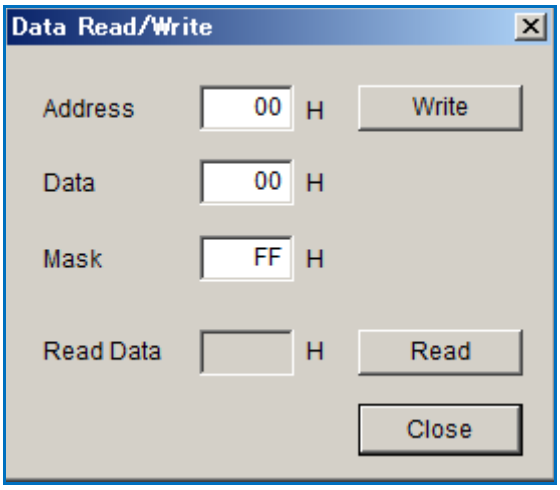

Figure 7-7. Window of [Data R/W]

[Address] Box : Input data write address in hexadecimal numbers.
[Data] Box : Input write data in hexadecimal numbers.
[Mask] Box : Input mask data in hexadecimal numbers.
This value "ANDed" with the write data becomes the input data.
[Write] : Write data generated from Data and Mask value is written to the address specified in "Address" box. (Note.102)
[Read] : Read data from the address specified in "Address" box. (Note.103)
[Close] : Close dialog box and finish process.
Data write will not be executed unless [Write] is clicked.

Note 102. The register map will be updated after executing the [Write] command.
Note 103. The [Read] button is only valid when the interface mode for register control is in I^2C bus control mode.

5. [Sequence]: Sequence Dialog Box

Click the [Sequence] button in the main window for Sequence dialog box.
Register sequence may be set and executed.

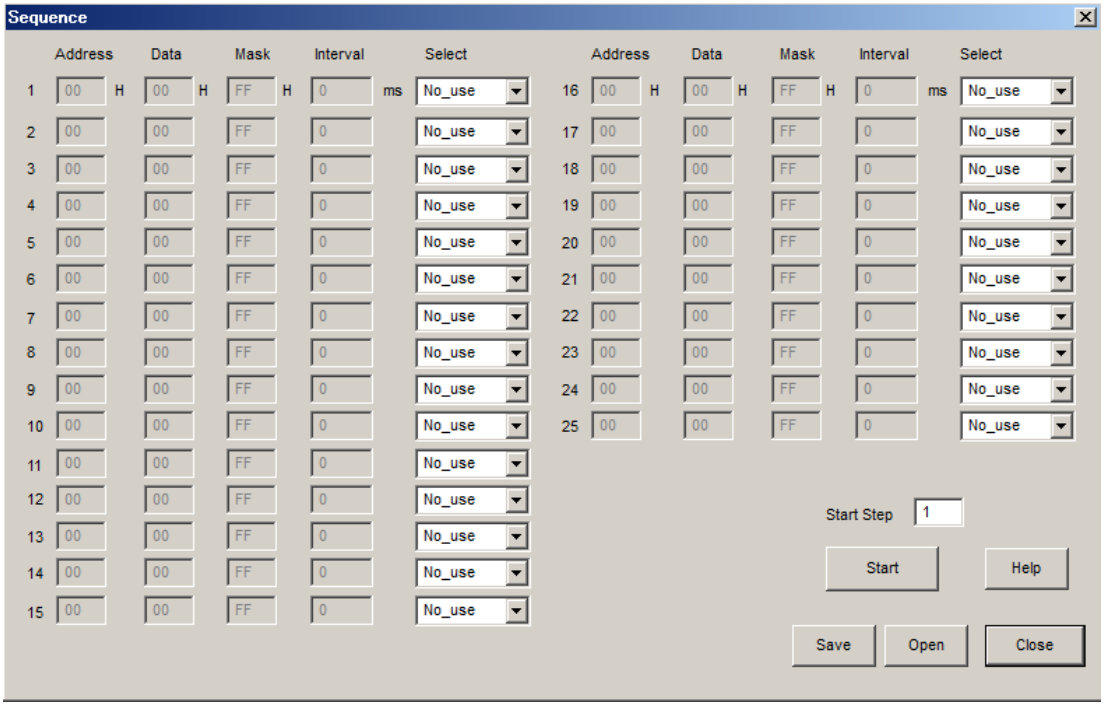

Figure 7-8. Window of [Sequence]

~ Sequence Setting ~

Set register sequence according to the following process.

1. Select a command
   Use [Select] pull-down box to choose commands.
   Corresponding input boxes will be valid.

<Combo Box>

- No_use : Not using this address
- Register : Register write
- Reg(Mask) : Register write (Masked)
- Interval : Take an interval
- Stop : Pause the sequence
- End : End the sequence

2. Input Sequence

[Address] : Data Address
[Data] : Write Data
[Mask] : Mask
This value “ANDed” with the write data becomes the input data.
When Mask = 0x00, current setting is hold.
When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.
When Mask = 0x0F, lower 4bit data which is set in the [Data] box is written.
Upper 4bit is hold to current setting.
[Interval]: Interval Time

Valid boxes for each process command are shown below.

- No_use : None
- Register : [Address], [Data], [Interval]
- Reg(Mask) : [Address], [Data], [Mask], [Interval]
- Interval : [Interval]
- Stop : None

・End : None

~ Control Buttons ~

Functions of Control Buttons are shown below.

[Start] button : Execute the sequence.
[Help] button : Open a help window.
[Save] button : Save sequence settings as a file. The file name is “*.aks”.
[Open] button : Open a sequence setting file “*.aks”.
[Close] button : Close the dialog box and finishes the process.

Stop Sequence

When “Stop” command is selected in the sequence, the process is paused at this step. It is resumed by clicking the [Start] button. The process starts from the step shown in [Start Step] box. This step number returns to “1” when the sequence is executed until the end. Input arbitrary step number to the [Start Step] box to start the process from the middle of sequence.

The process sequence can be restarted from the beginning by writing “1” to the [Start Step] box and click the [Start] button during the process.

6. [Sequence(File)]: Sequence(File) Dialog

Click the [Sequence(File)] button to open sequence setting file dialog box shown below.
Files saved in the “Sequence setting dialog” can be applied in this dialog.

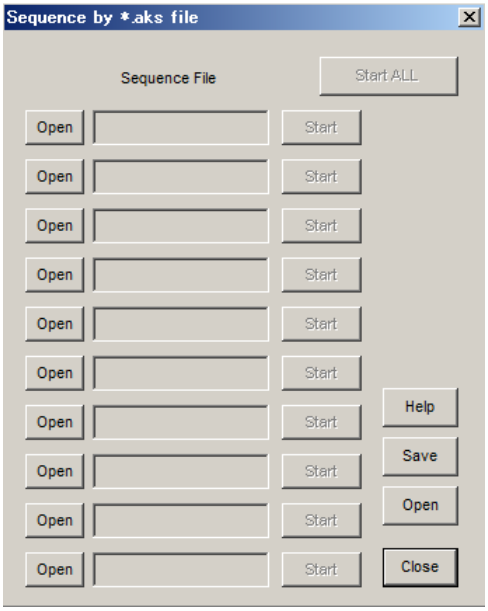

Figure 7-9. Window of [Sequence(File)]

[Open (left)] button : Select a sequence setting file (*.aks)
[Start] button : Execute the sequence by the setting of selected file.
[Start All] button : Execute sequence with all selected setting files.
Selected files are executed in descending order.
[Help] button : Open help window.
[Save] button : Save register setting file assignment. File name is “*.mas”.
[Open (right)] button : Open saved sequence setting file assignment “*. mas”.
[Close] button : Close dialog box and finish process.

~ Operating Suggestions ~

1. Files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mas” should be stored in the same folder.
2. When “Stop” command is selected in the sequence, the process is paused at this step and a message shown below pops up. The sequence is resumed by clicking “OK” button.

Measurement Results

[Measurement condition]

- Measurement unit : Audio Precision, System Two Cascade
- Power Supply : DVDD=3.3V (VSEL=L)
- Band width : 20Hz ~ FSO/2
- Resolution (Bit) : 24bit
- XTI Input : Use X'Tal (X1)
- Output PORT : Slave Mode
- Temperature : Room

[Measurement Result]

SRC Characteristics	SDTO		Unit
	Lch	Rch	
THD+N (Input = 1kHz, 0dBFS)			
FSO/FSI = 48kHz/48kHz	140.9	140.9	dB
FSO/FSI = 48kHz/44.1kHz	132.4	132.4	dB
FSO/FSI = 48kHz/192kHz	142.8	142.8	dB
FSO/FSI = 192kHz/48kHz	130.4	130.4	dB
Worst Case (FSO/FSI = 32kHz/176.4kHz)	113.8	113.8	dB
Dynamic Range (Input = 1kHz, –60dBFS)			
FSO/FSI = 48kHz/48kHz	141.7	141.7	dB
FSO/FSI = 48kHz/44.1kHz	141.4	141.3	dB
FSO/FSI = 48kHz/192kHz	143.1	143.1	dB
FSO/FSI = 192kHz/48kHz	133.8	133.7	dB
Worst Case(FSO/FSI = 48kHz/32kHz)	141.5	141.5	dB
Dynamic Range (Input = 1kHz, –60dBFS, A-weighted)			
FSO/FSI = 44.1kHz/48kHz	146.2	146.2	dB

[Plots]

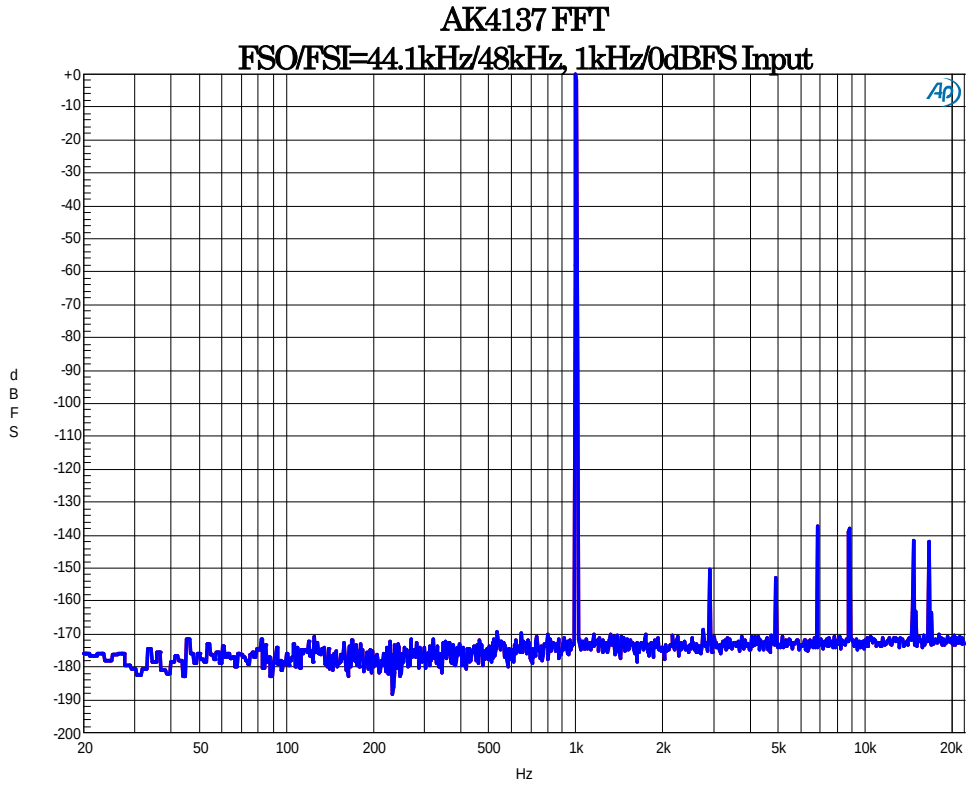

Figure 8-1. FFT Plot (Input = 0dBFS)

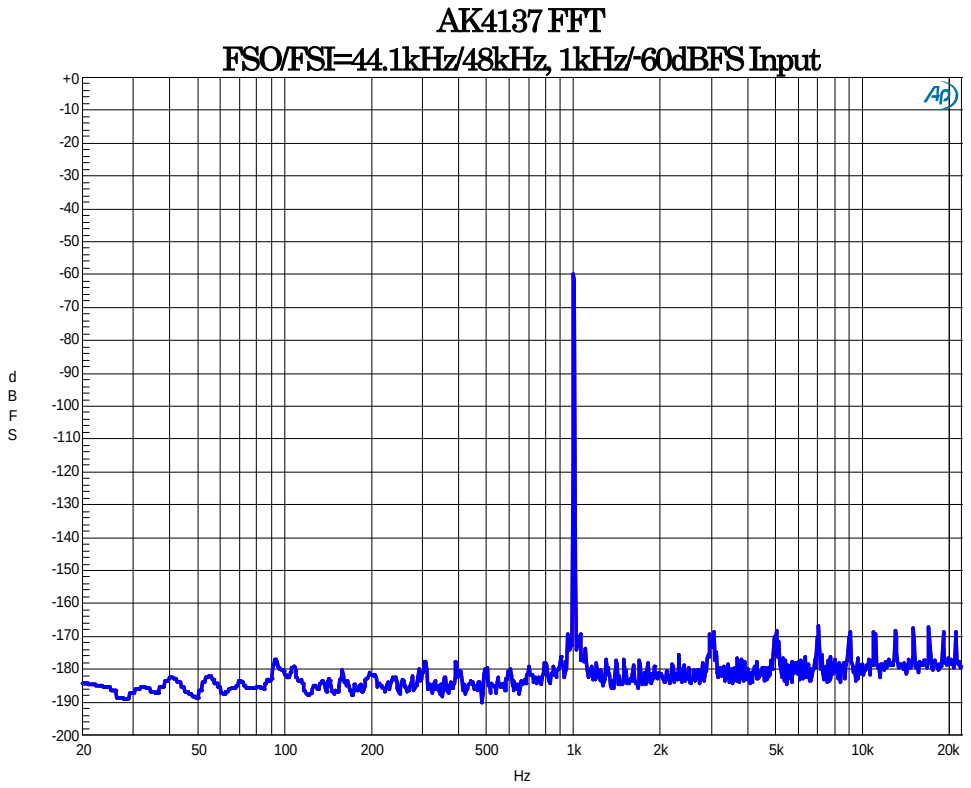

Figure 8-2. FFT Plot (Input = -60dBFS)

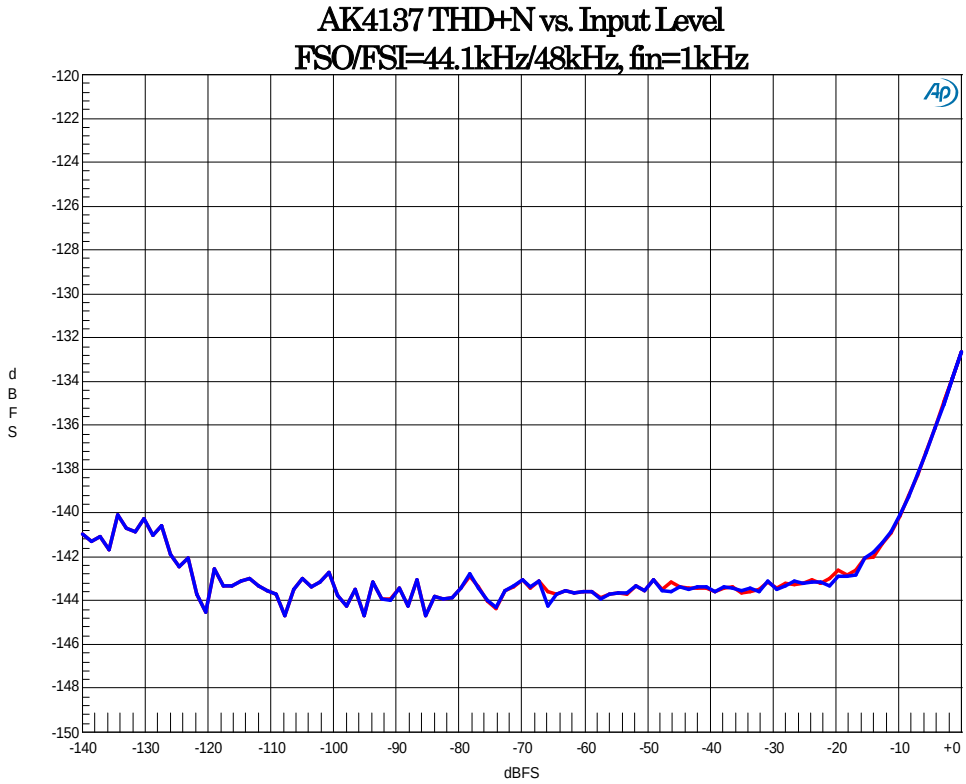

Figure 8-3. THD+N vs. Input Level

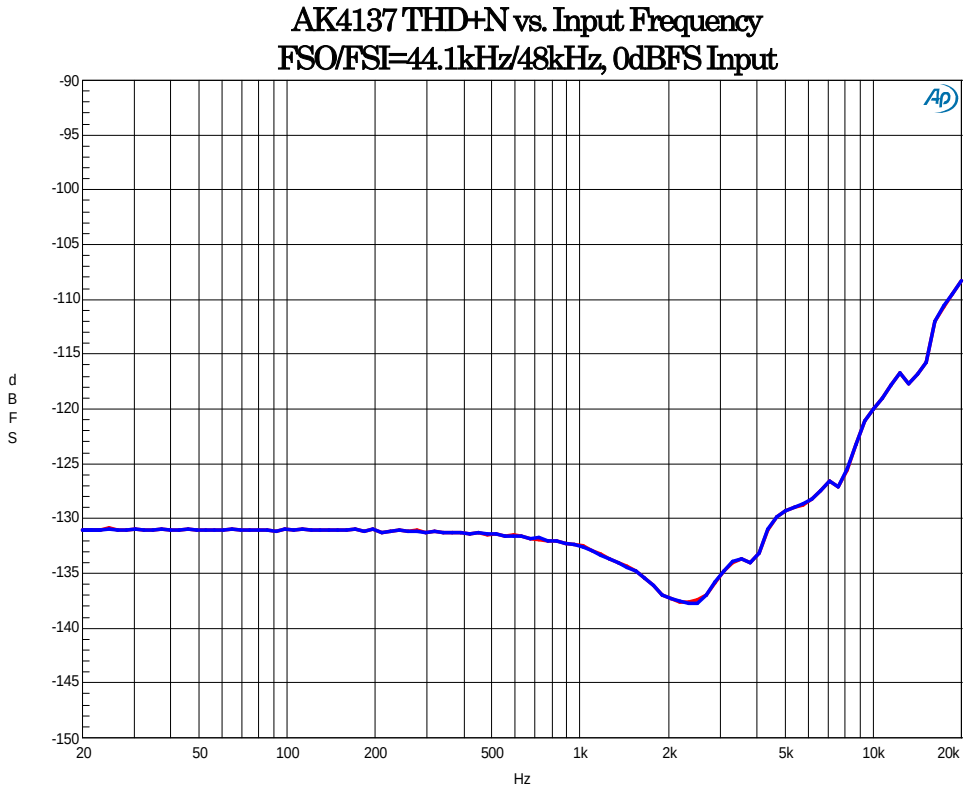

Figure 8-4. THD+N vs. Input Frequency (Input = 0dBFS)

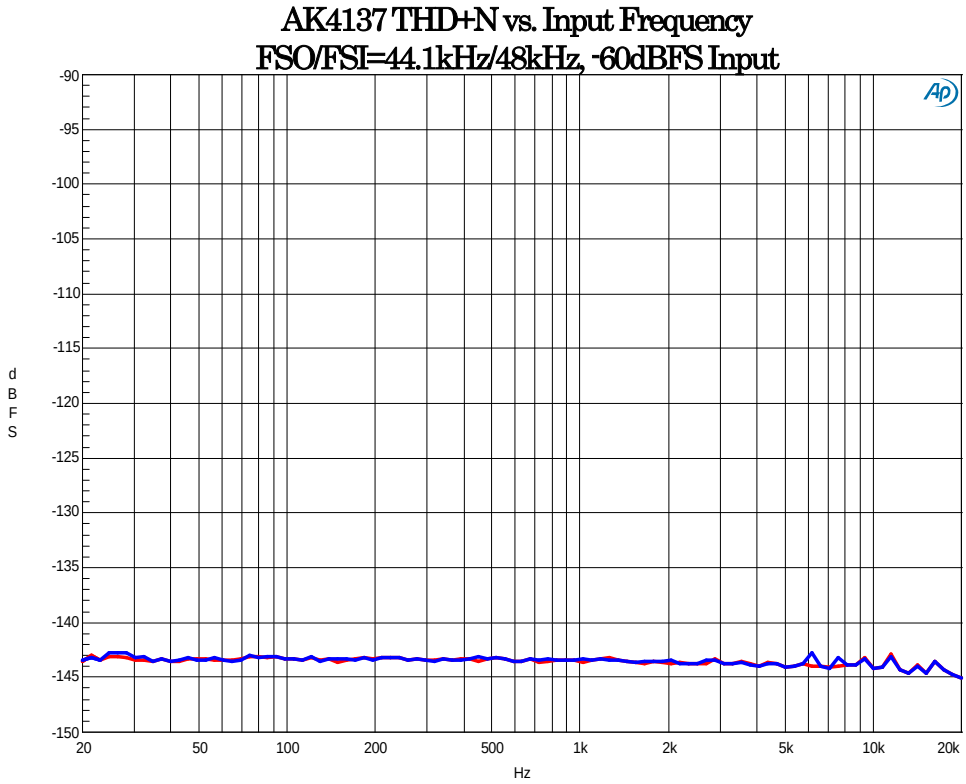

Figure 8-5. THD+N vs. Input Frequency (Input = -60dBFS)

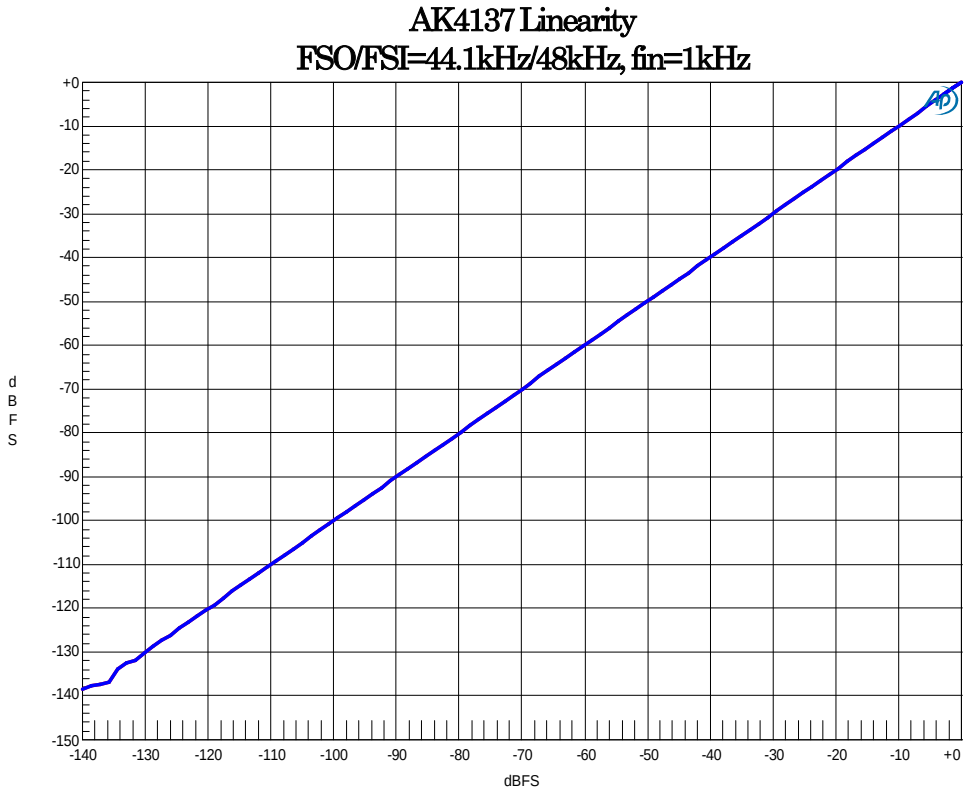

Figure 8-6. Linearity

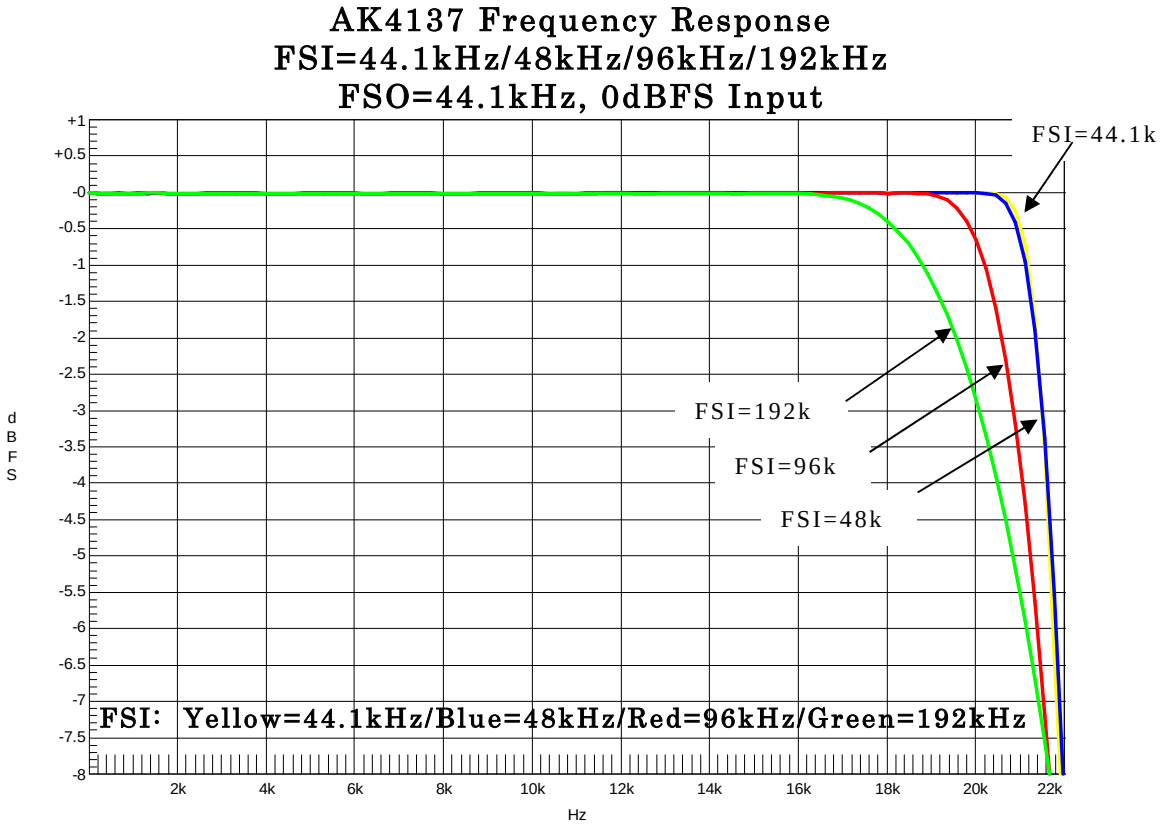

Figure8-7. Frequency Response (FSO=44.1kHz)

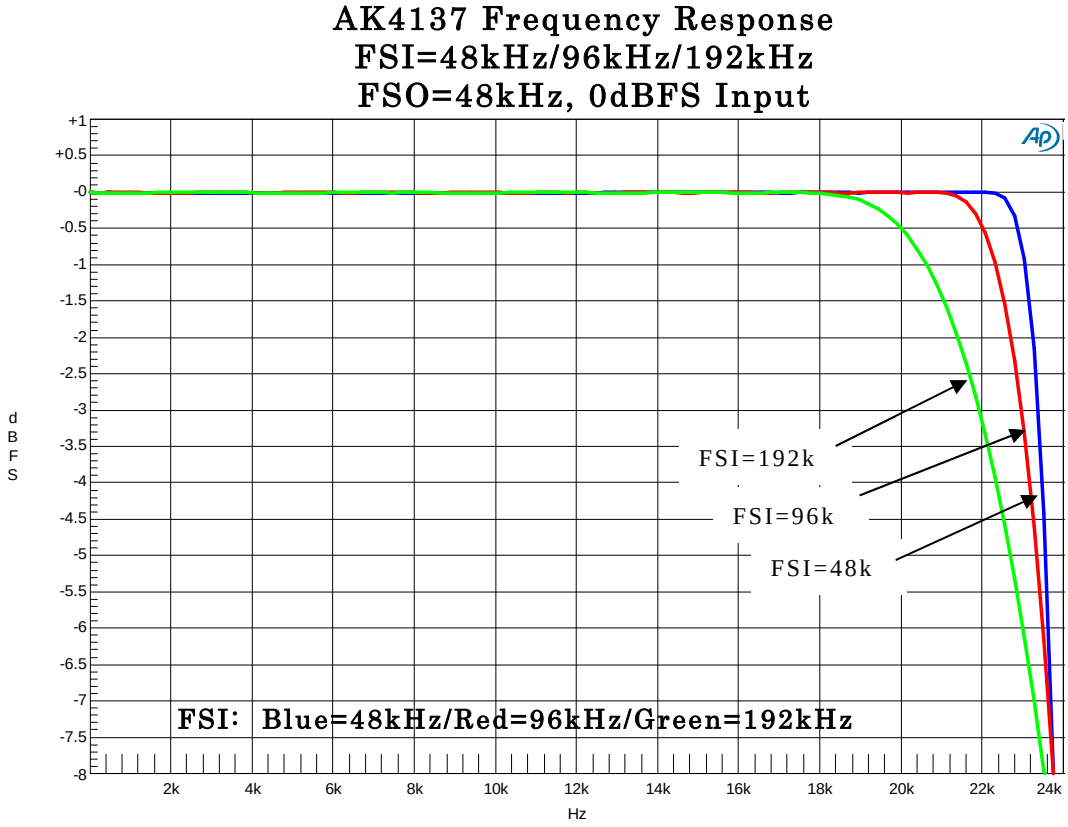

Figure8-8. Frequency Response (FSO=48kHz)

REVISION HISTORY

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Page	Contents
14/07/02	KM117200	0	First edition	-	
15/03/10	KM117201	1	Change	-	Board Revision changed
15/04/17	KM117202	2	Change	-	Board Revision changed
19/07/10	KM117203	2	Change	-	Control Soft Version Up
22/04/20	KM117204	3	Change	-	Device Revision Up

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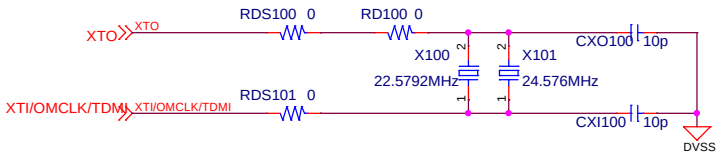
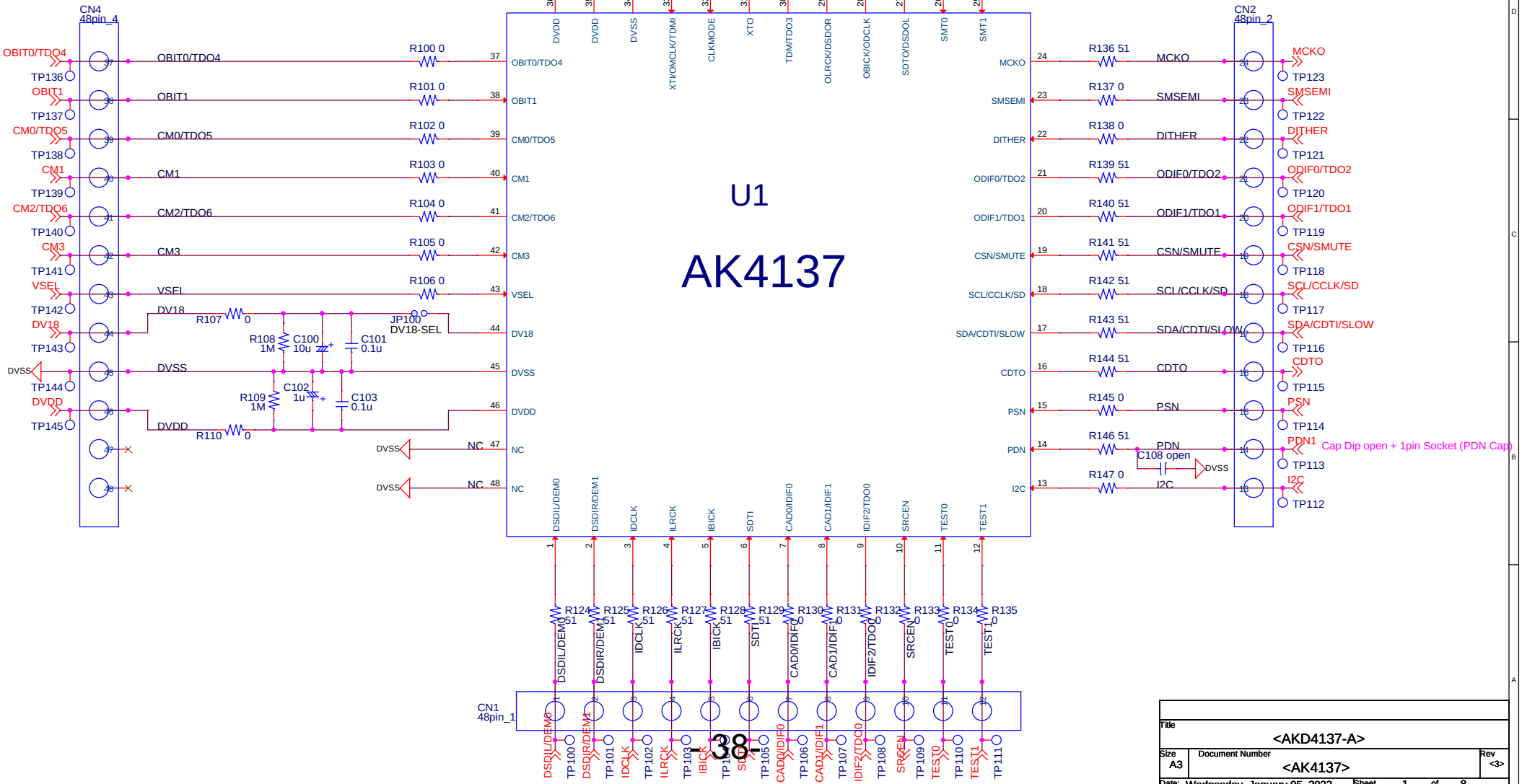
Rev.1

X100, X101 = open, NX5032GA
X100 Frequency Check -> Xtal=Daishinku
X101 Frequency Check -> Xtal=NDK (NX5032GA)
RDS100, RDS101 = 0ohm, 0ohm
RD100 = 0ohm
CXO100, CXI100 = 10pF, 10pF





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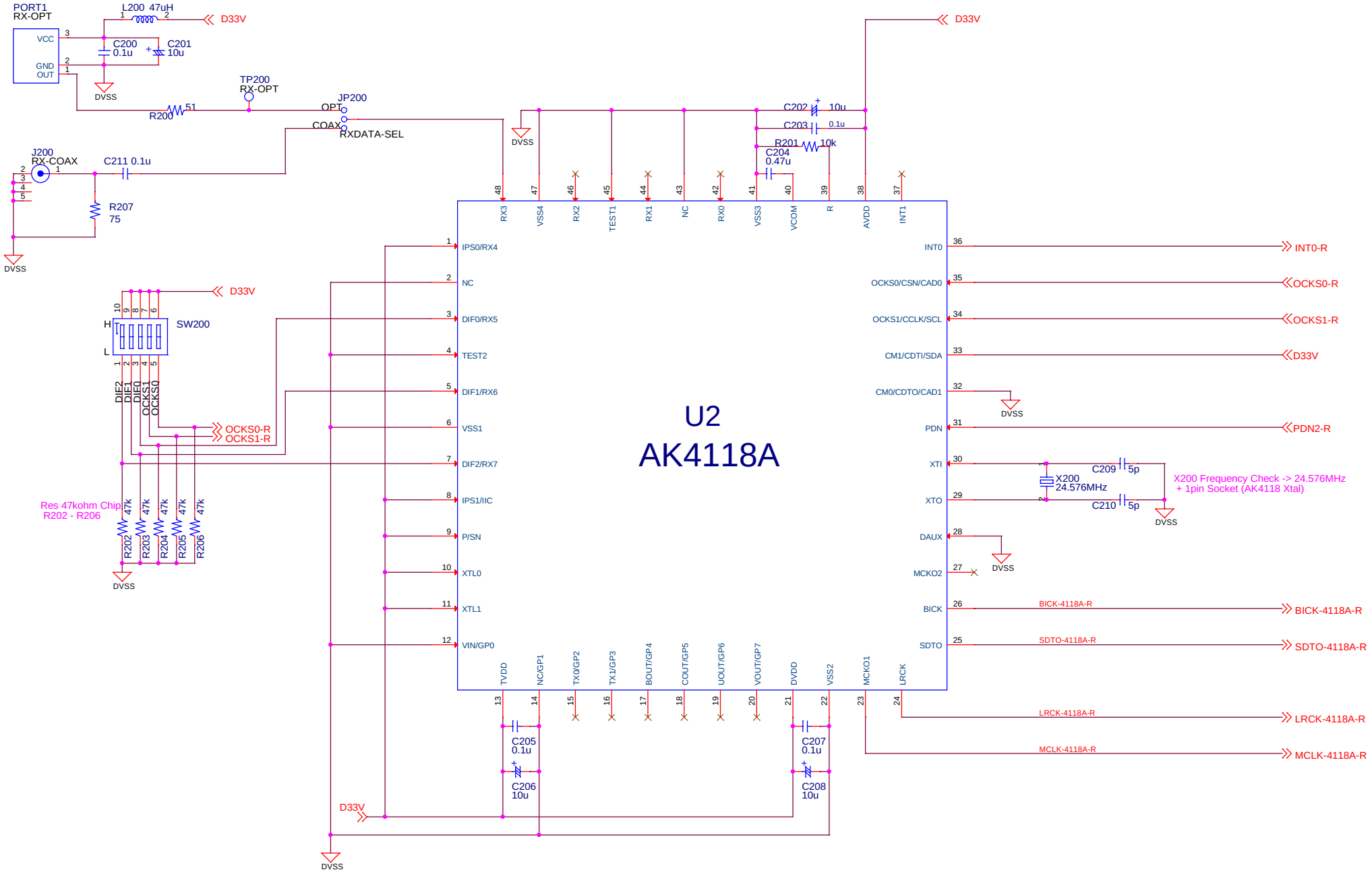

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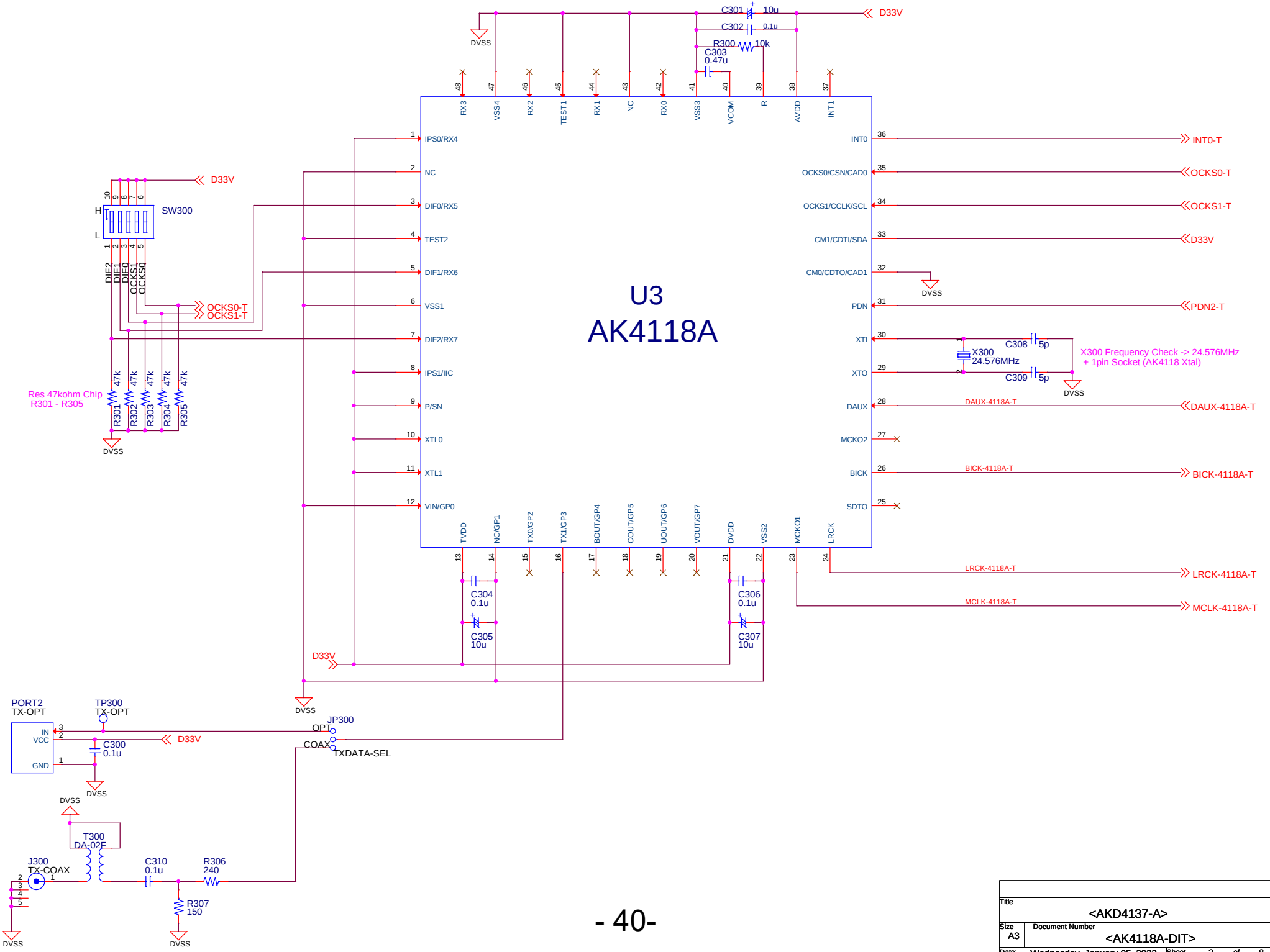

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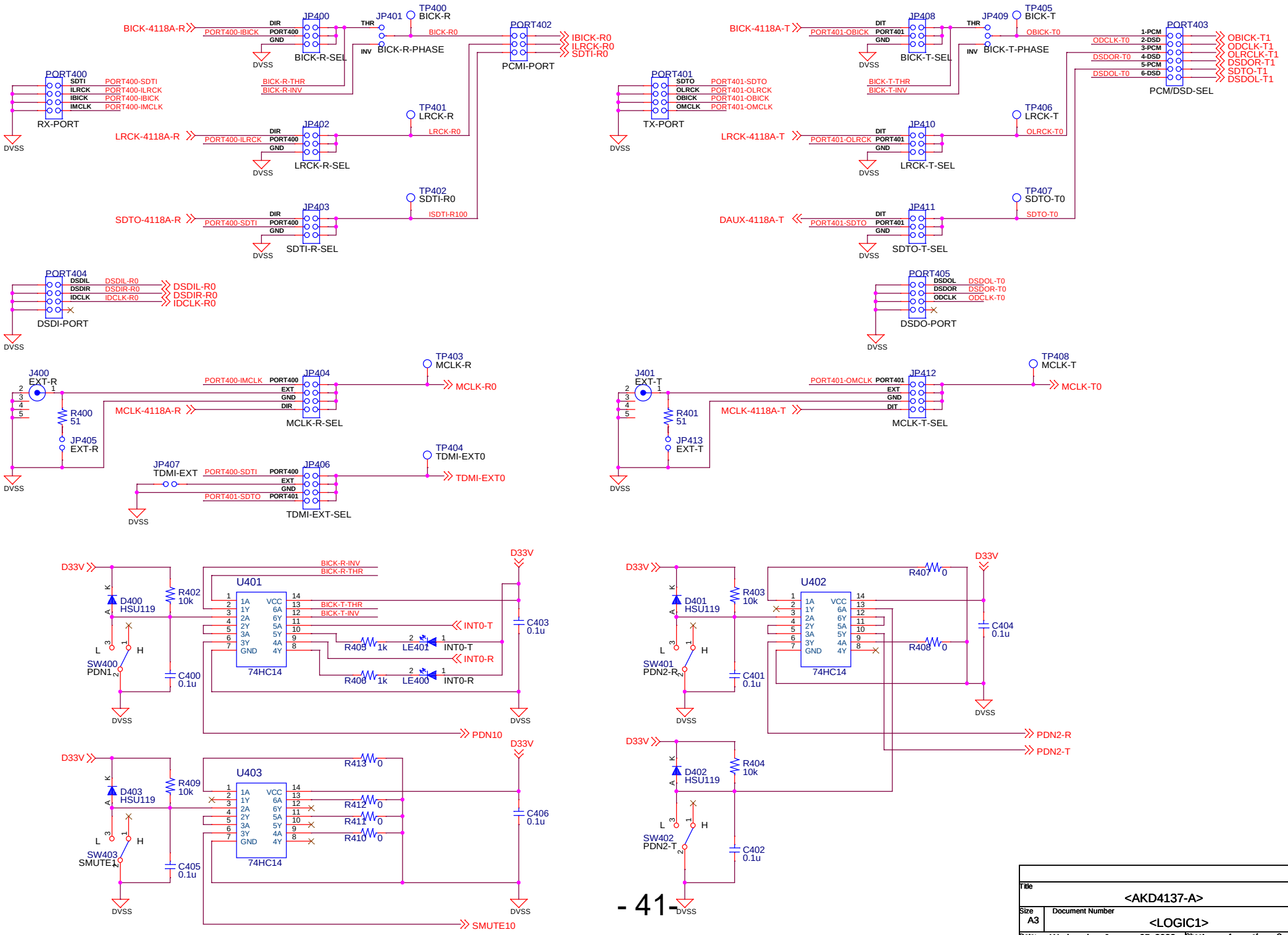
BICK-4118A-R
PORT400-IBICK
DIR
PORT400
GND
JP400
JP401
THR
INV
TP400
BICK-R
BICK-R0
BICK-R-SEL
BICK-R-PHASE
BICK-R-THR
BICK-R-INV
PORT402
IBICK-R0
ILRCK-R0
SDTI-R0
PCMI-PORT
PORT400
SDTI
ILRCK
IBICK
IMCLK
PORT400-SDTI
PORT400-ILRCK
PORT400-IBICK
PORT400-IMCLK
RX-PORT
DVSS
LRCK-4118A-R
JP402
TP401
LRCK-R
LRCK-R0
LRCK-R-SEL
SDTO-4118A-R
JP403
TP402
SDTI-R0
ISDTI-R100
SDTI-R-SEL
BICK-4118A-T
PORT401-OBICK
JP408
JP409
TP405
BICK-T
OBICK-T0
BICK-T-SEL
BICK-T-PHASE
BICK-T-THR
BICK-T-INV
PORT403
1-PCM
2-DSD
3-PCM
4-DSD
5-PCM
6-DSD
ODCLK-T0
DSDOR-T0
DSDOL-T0
OBICK-T1
ODCLK-T1
OLRCLK-T1
DSDOR-T1
SDTO-T1
DSDOL-T1
PCM/DSD-SEL
PORT401
SDTO
OLRCK
OBICK
OMCLK
PORT401-SDTO
PORT401-OLRCK
PORT401-OBICK
PORT401-OMCLK
TX-PORT
LRCK-4118A-T
JP410
TP406
LRCK-T
OLRCK-T0
LRCK-T-SEL
DAUX-4118A-T
JP411
TP407
SDTO-T0
SDTO-T
SDTO-T-SEL
PORT404
DSDIL
DSDIR
IDCLK
DSDIL-R0
DSDIR-R0
IDCLK-R0
DSDI-PORT
PORT405
DSDOL
DSDOR
ODCLK
DSDOL-T0
DSDOR-T0
ODCLK-T0
DSDO-PORT
J400
EXT-R
R400
51
JP405
MCLK-4118A-R
JP404
TP403
MCLK-R
MCLK-R0
MCLK-R-SEL
JP407
TDMI-EXT
JP406
TP404
TDMI-EXT0
TDMI-EXT-SEL
EXT
GND
DIR
J401
EXT-T
R401
JP413
MCLK-4118A-T
JP412
TP408
MCLK-T
MCLK-T0
MCLK-T-SEL
D33V
D400
HSU119
R402
10k
C400
0.1u
SW400
PDN1
U401
74HC14
BICK-R-INV
BICK-R-THR
BICK-T-THR
BICK-T-INV
INT0-T
INT0-R
R405
1k
R406
LE401
LE400
C403
PDN10
D403
HSU119
R409
SW403
SMUTE1
U403
R413
0
R412
R411
R410
C406
C405
SMUTE10
D401
HSU119
R403
SW401
PDN2-R
U402
R407
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C402
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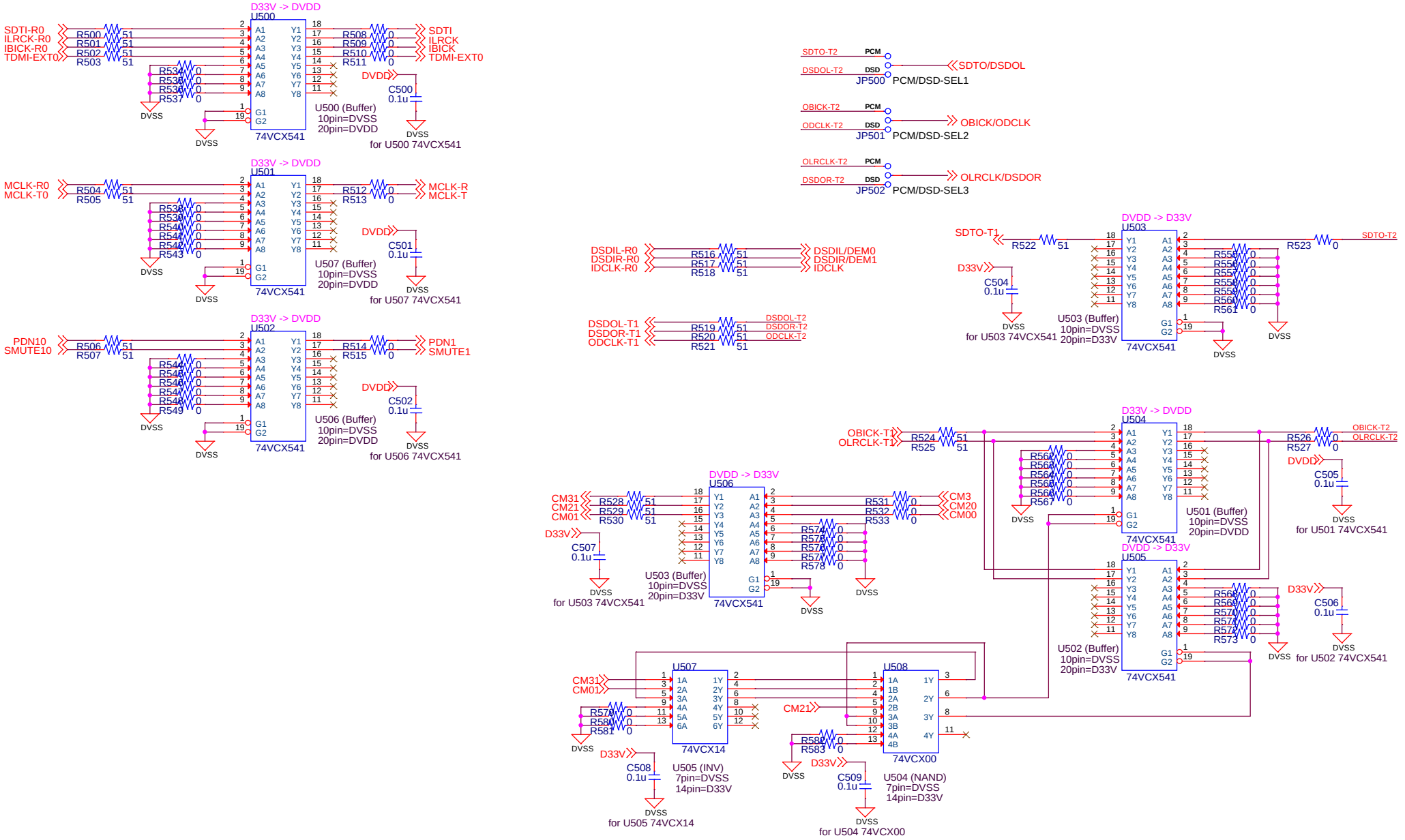

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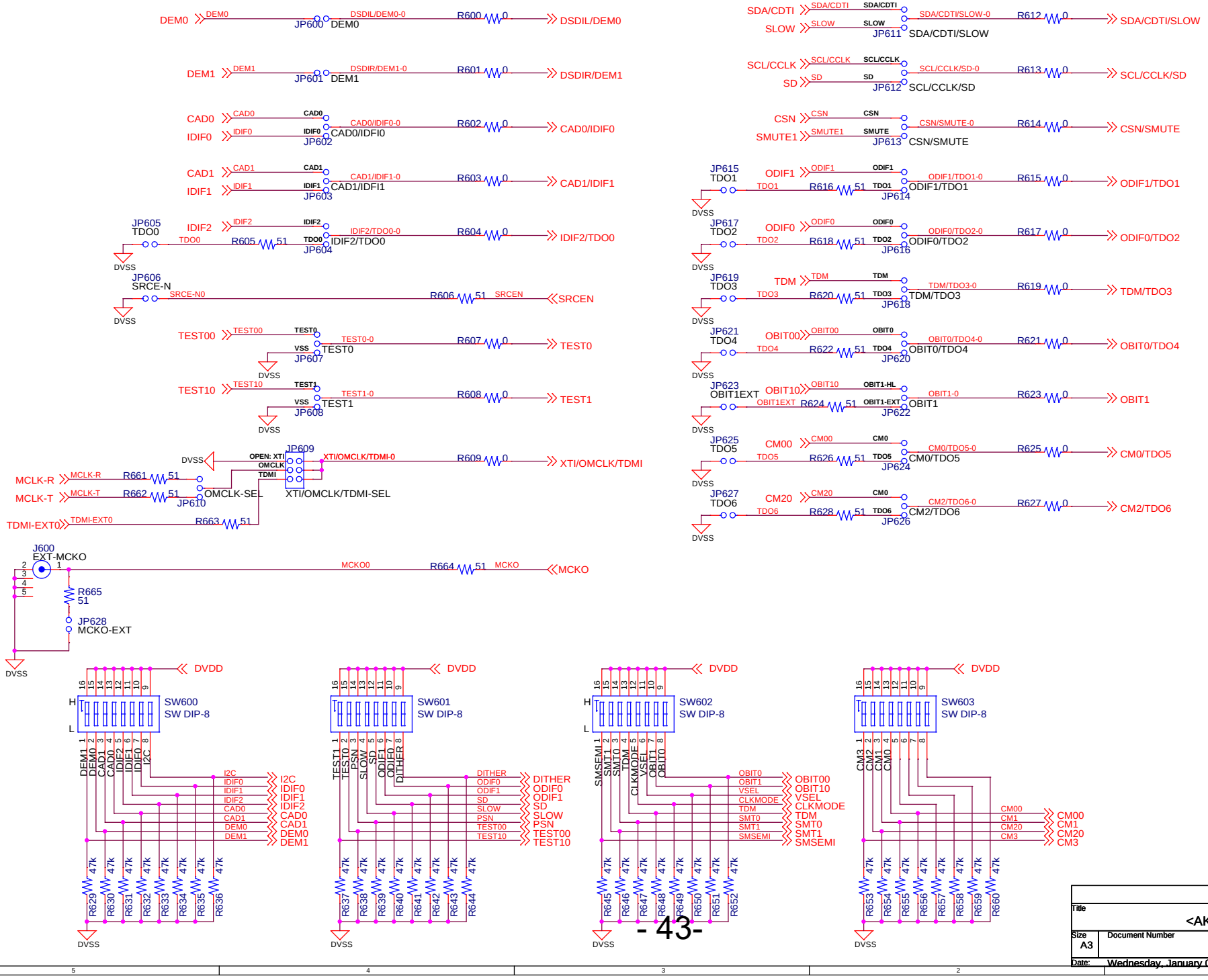
DEM0
DSDIL/DEM0-0
R600 0
DSDIL/DEM0
JP600
DEM1
DSDIR/DEM1-0
R601 0
DSDIR/DEM1
JP601
CAD0
IDIF0
CAD0/IDIF0-0
R602 0
CAD0/IDIF0
JP602
CAD1
IDIF1
CAD1/IDIF1-0
R603 0
CAD1/IDIF1
JP603
JP605
TDO0
IDIF2
IDIF2/TDO0-0
R604 0
R605 51
IDIF2/TDO0
JP604
DVSS
JP606
SRCE-N
SRCE-N0
R606 51
SRCEN
TEST00
TEST0-0
R607 0
TEST0
JP607
TEST10
TEST1-0
R608 0
TEST1
JP608
DVSS
JP609
OPEN: XTI
OMCLK
TDMI
XTI/OMCLK/TDMI-0
R609 0
XTI/OMCLK/TDMI
MCLK-R
MCLK-T
TDMI-EXT0
R661 51
R662 51
R663 51
OMCLK-SEL
JP610
XTI/OMCLK/TDMI-SEL
J600
EXT-MCKO
MCKO0
R664 51
MCKO
R665
51
JP628
MCKO-EXT
SDA/CDTI
SLOW
SDA/CDTI/SLOW-0
R612 0
SDA/CDTI/SLOW
JP611
SCL/CCLK
SD
SCL/CCLK/SD-0
R613 0
SCL/CCLK/SD
JP612
CSN
SMUTE1
CSN/SMUTE-0
R614 0
CSN/SMUTE
JP613
JP615
TDO1
ODIF1
ODIF1/TDO1-0
R615 0
R616 51
ODIF1/TDO1
JP614
JP617
TDO2
ODIF0
ODIF0/TDO2-0
R617 0
R618 51
ODIF0/TDO2
JP616
JP619
TDO3
TDM
TDM/TDO3-0
R619 0
R620 51
TDM/TDO3
JP618
JP621
TDO4
OBIT00
OBIT0/TDO4-0
R621 0
R622 51
OBIT0/TDO4
JP620
JP623
OBIT1EXT
OBIT10
OBIT1-0
R623 0
R624 51
OBIT1
JP622
JP625
TDO5
CM00
CM0/TDO5-0
R625 0
R626 51
CM0/TDO5
JP624
JP627
TDO6
CM20
CM2/TDO6-0
R627 0
R628 51
CM2/TDO6
JP626
DVDD
SW600
SW DIP-8
DEM1 DEM0 CAD1 CAD0 IDIF2 IDIF1 IDIF0 I2C
I2C IDIF0 IDIF1 IDIF2 CAD0 CAD1 DEM0 DEM1
R629 R630 R631 R632 R633 R634 R635 R636 47k
SW601
SW DIP-8
TEST1 TEST0 PSN SLOW SD ODIF1 ODIF0 DITHER
DITHER ODIF0 ODIF1 SD SLOW PSN TEST00 TEST10
R637 R638 R639 R640 R641 R642 R643 R644 47k
SW602
SW DIP-8
SMSEMI SMT1 SMT0 TDM CLKMODE VSEL OBIT1 OBIT0
OBIT0 OBIT1 VSEL CLKMODE TDM SMT0 SMT1 SMSEMI
R645 R646 R647 R648 R649 R650 R651 R652 47k
SW603
SW DIP-8
CM3 CM2 CM1 CM0
CM00 CM1 CM20 CM3
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DVSS
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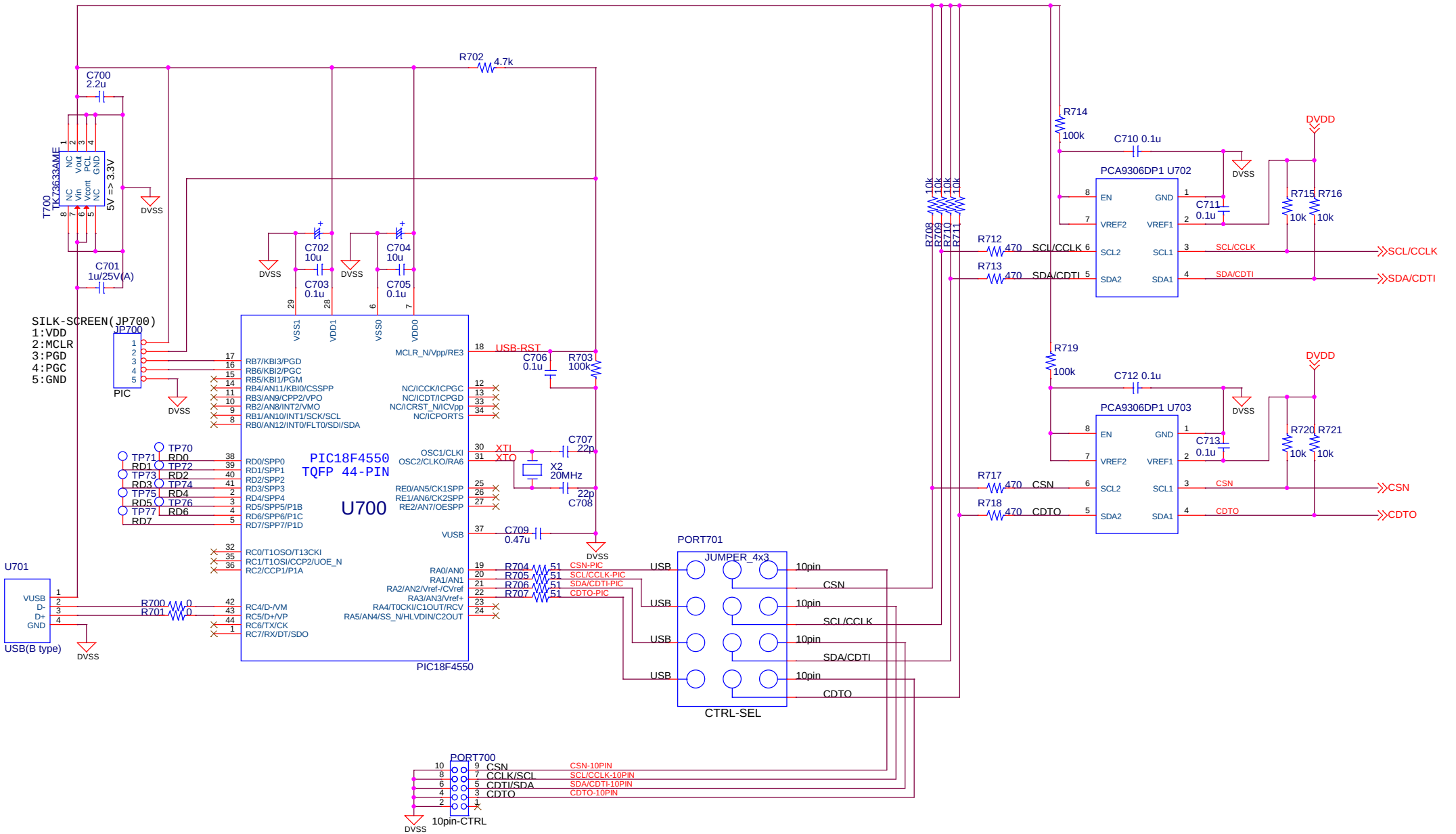

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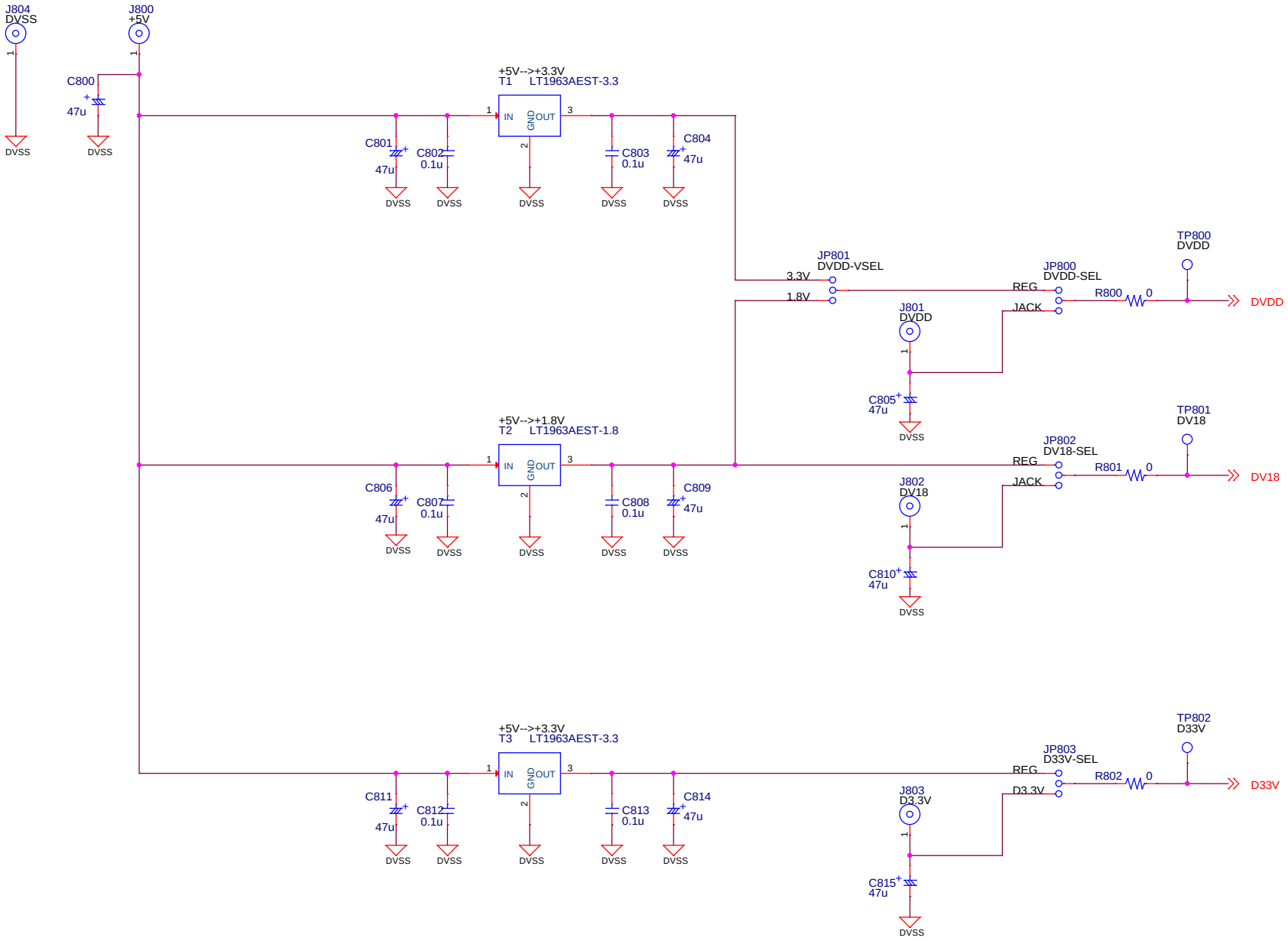

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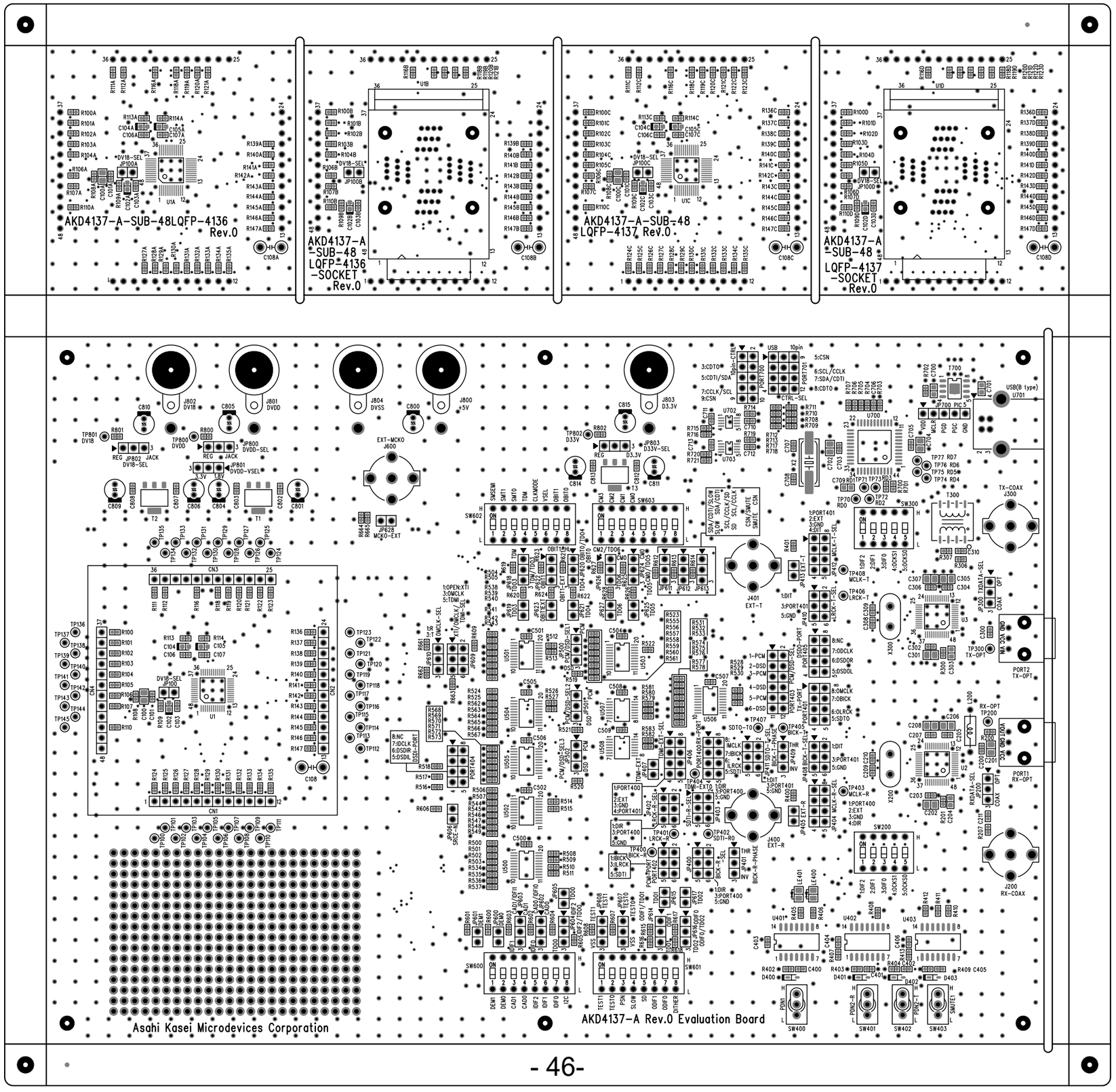
部品面シルク図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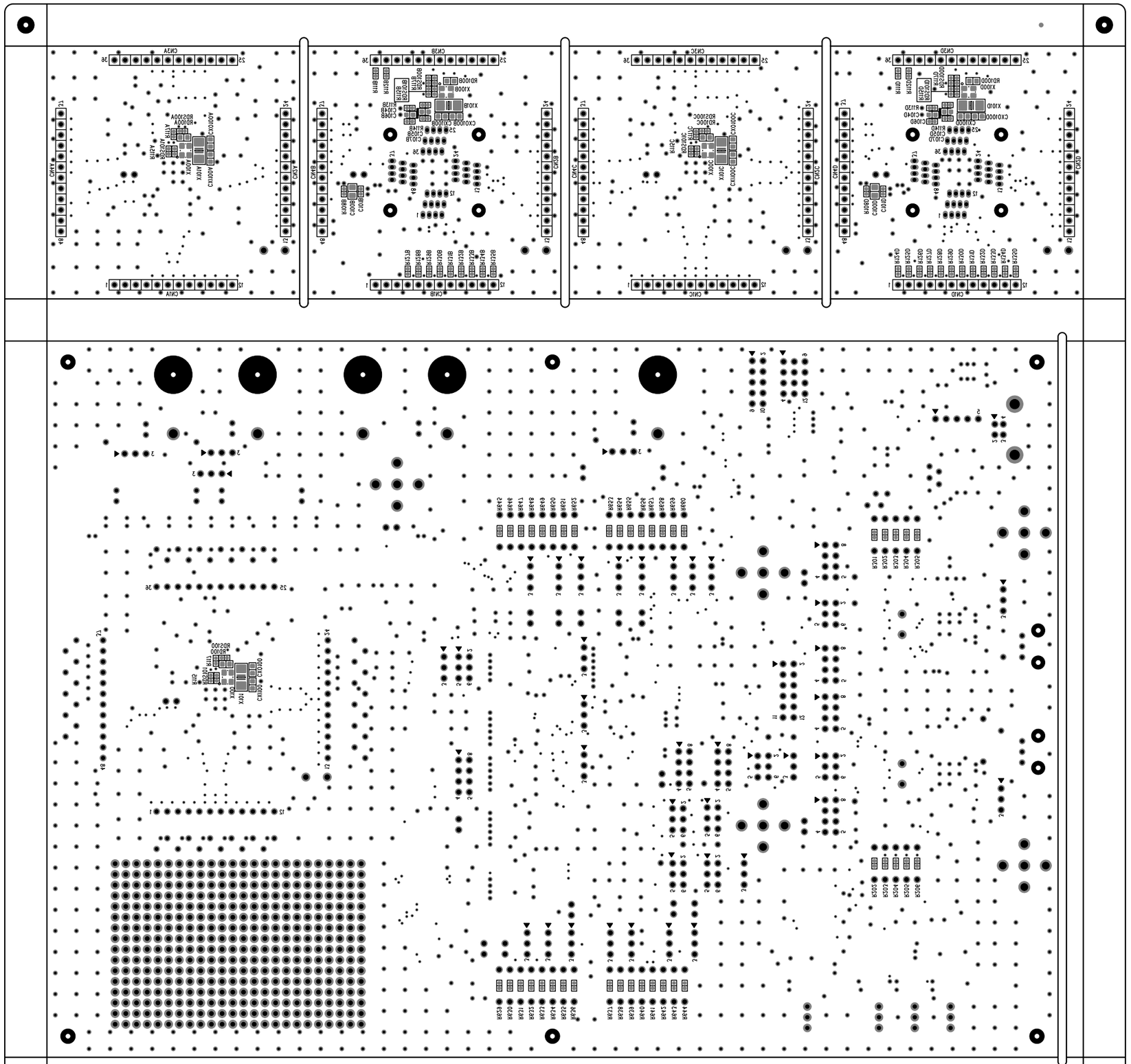
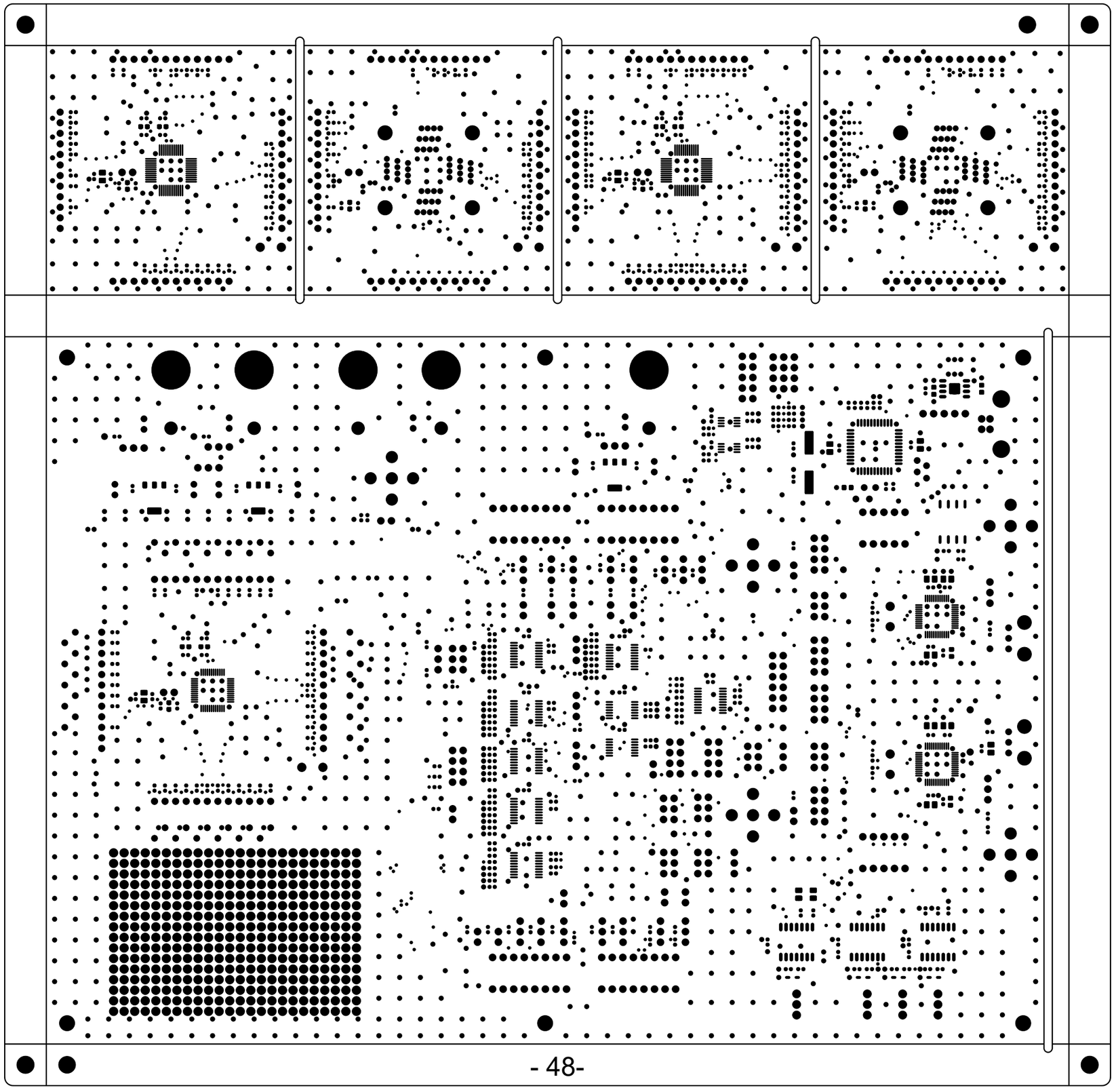
AKD4137-A-SUB-48 LQFP-4136 -SOCKET Rev.0
AKD4137-A-SUB-48 LQFP-4137 Rev.0
AKD4137-A-SUB-48 LQFP-4137 -SOCKET Rev.0
Asahi Kasei Microdevices Corporation
AKD4137-A Rev.0 Evaluation Board

半田面シルク図



部品面レジスト 図



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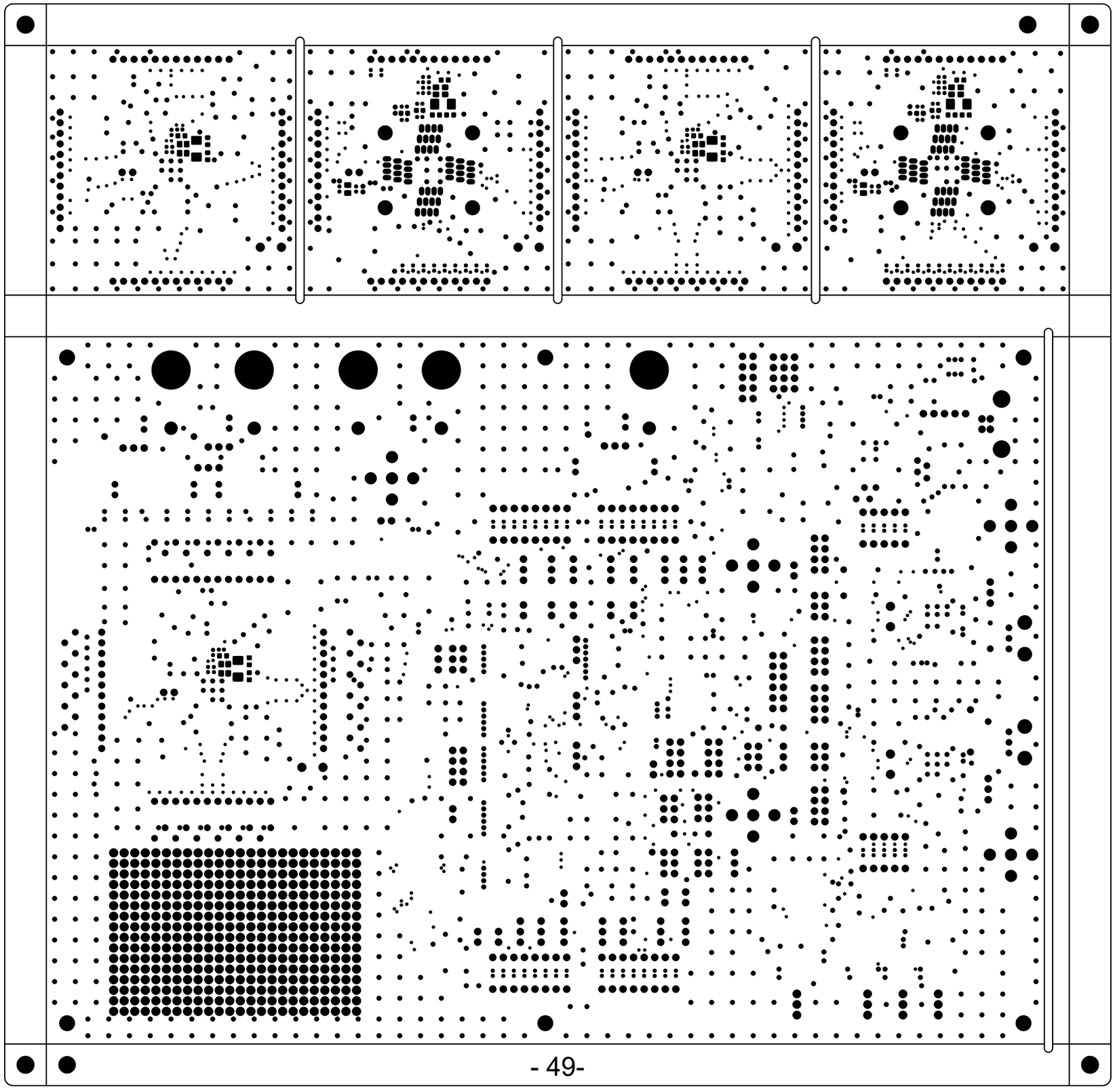
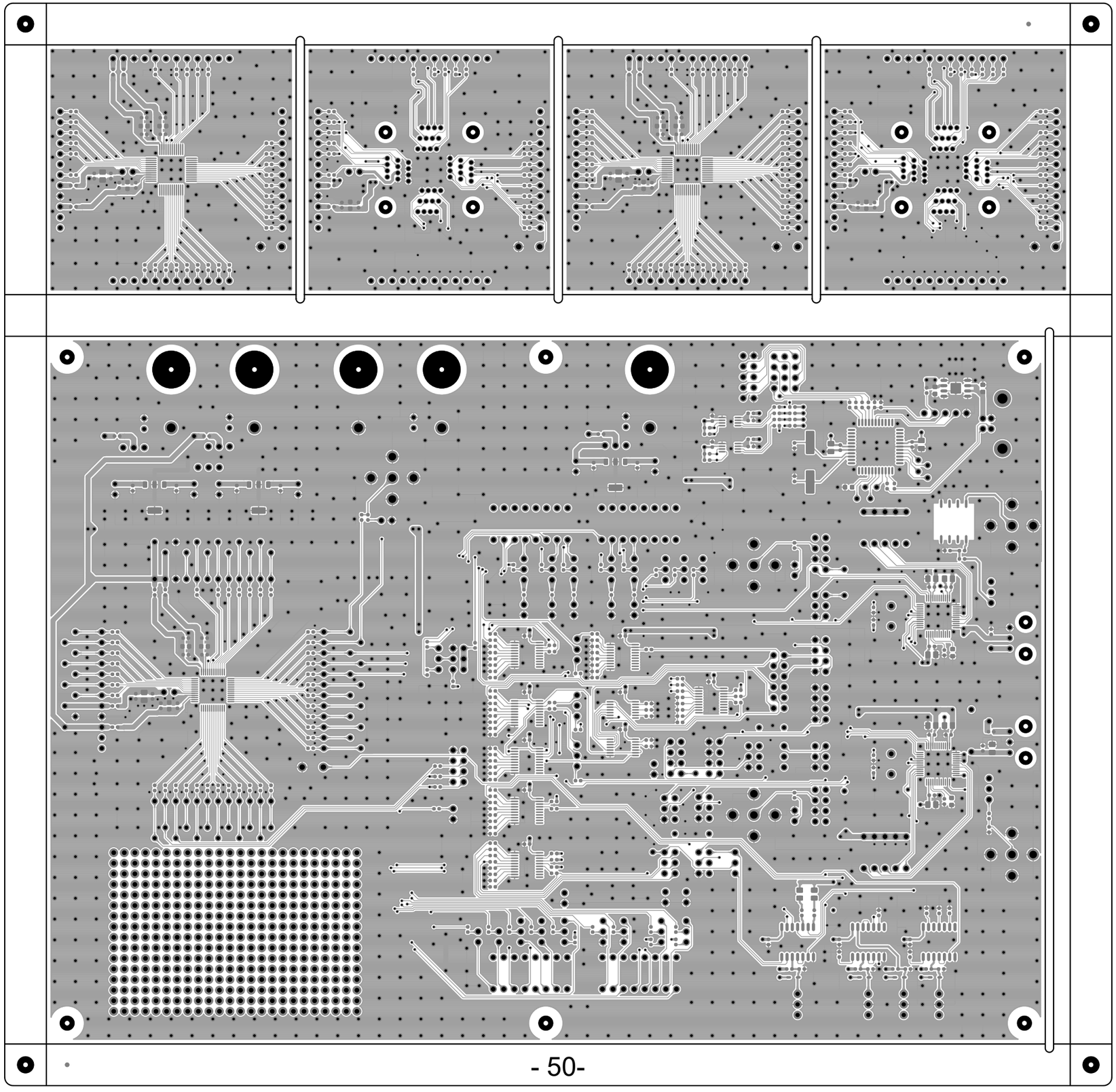
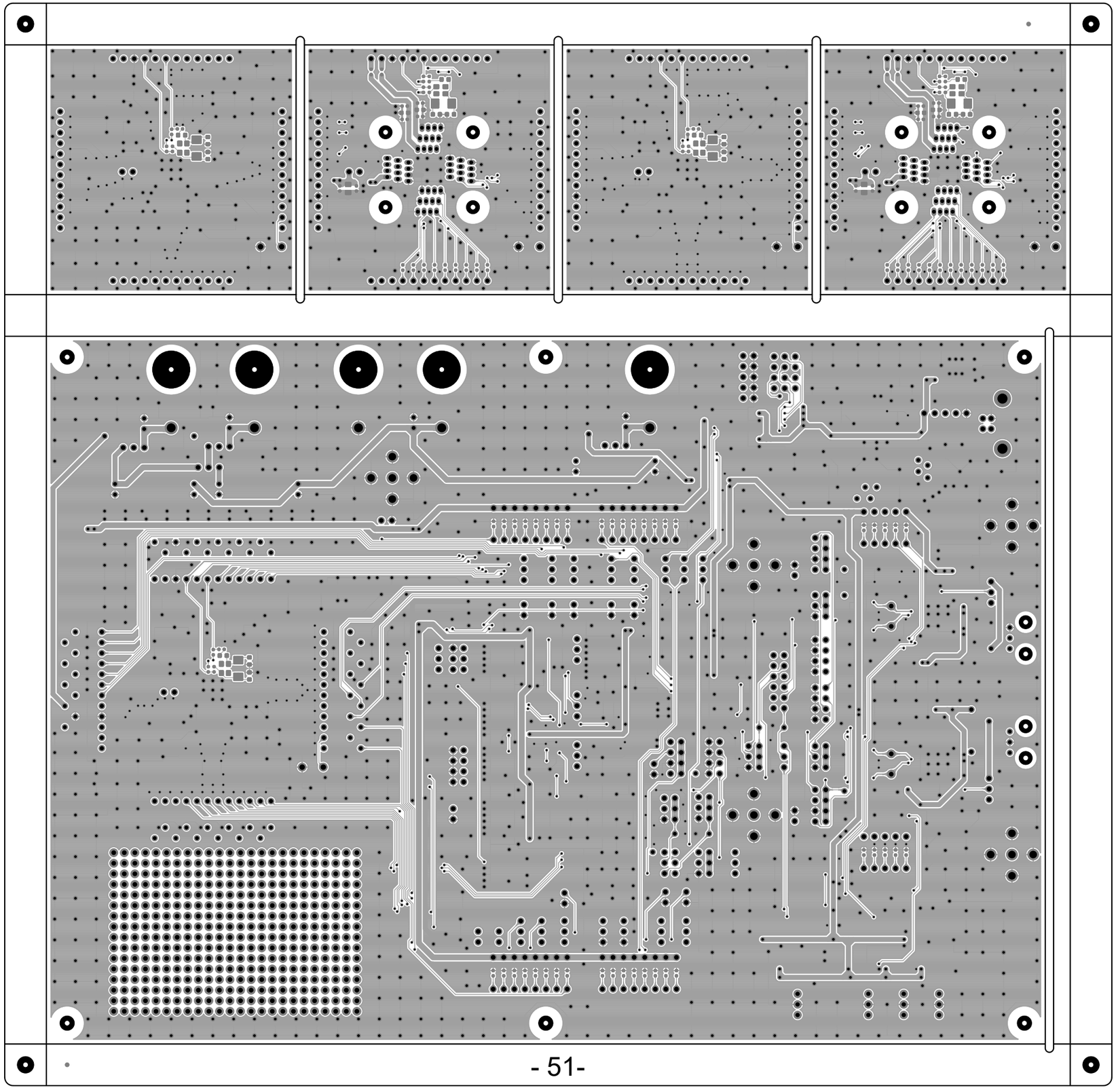
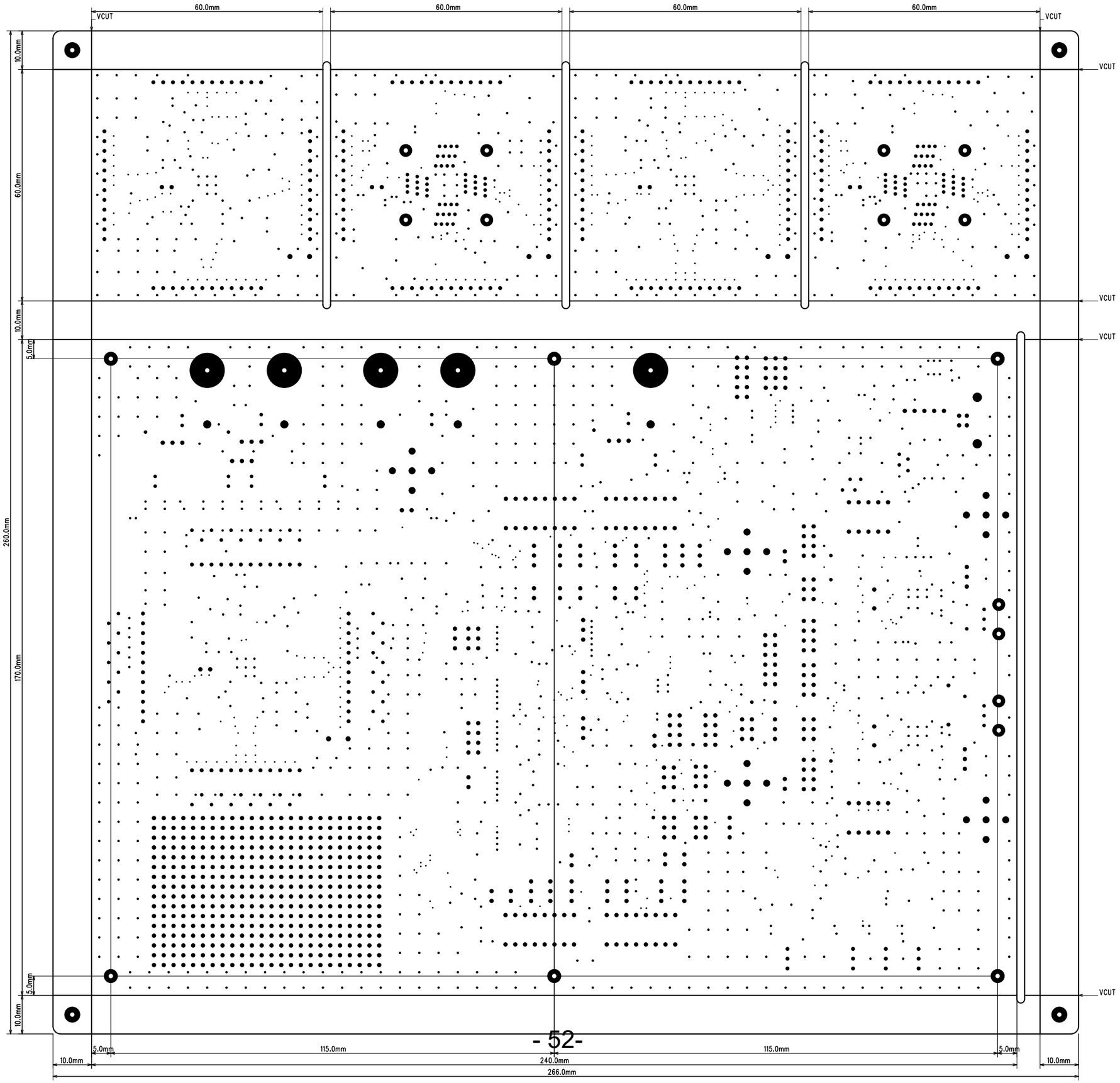






外形図、寸法図


60.0mm
60.0mm
60.0mm
60.0mm
VCUT
VCUT
VCUT
VCUT
VCUT
10.0mm
60.0mm
10.0mm
5.0mm
260.0mm
170.0mm
5.0mm
10.0mm
5.0mm
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115.0mm
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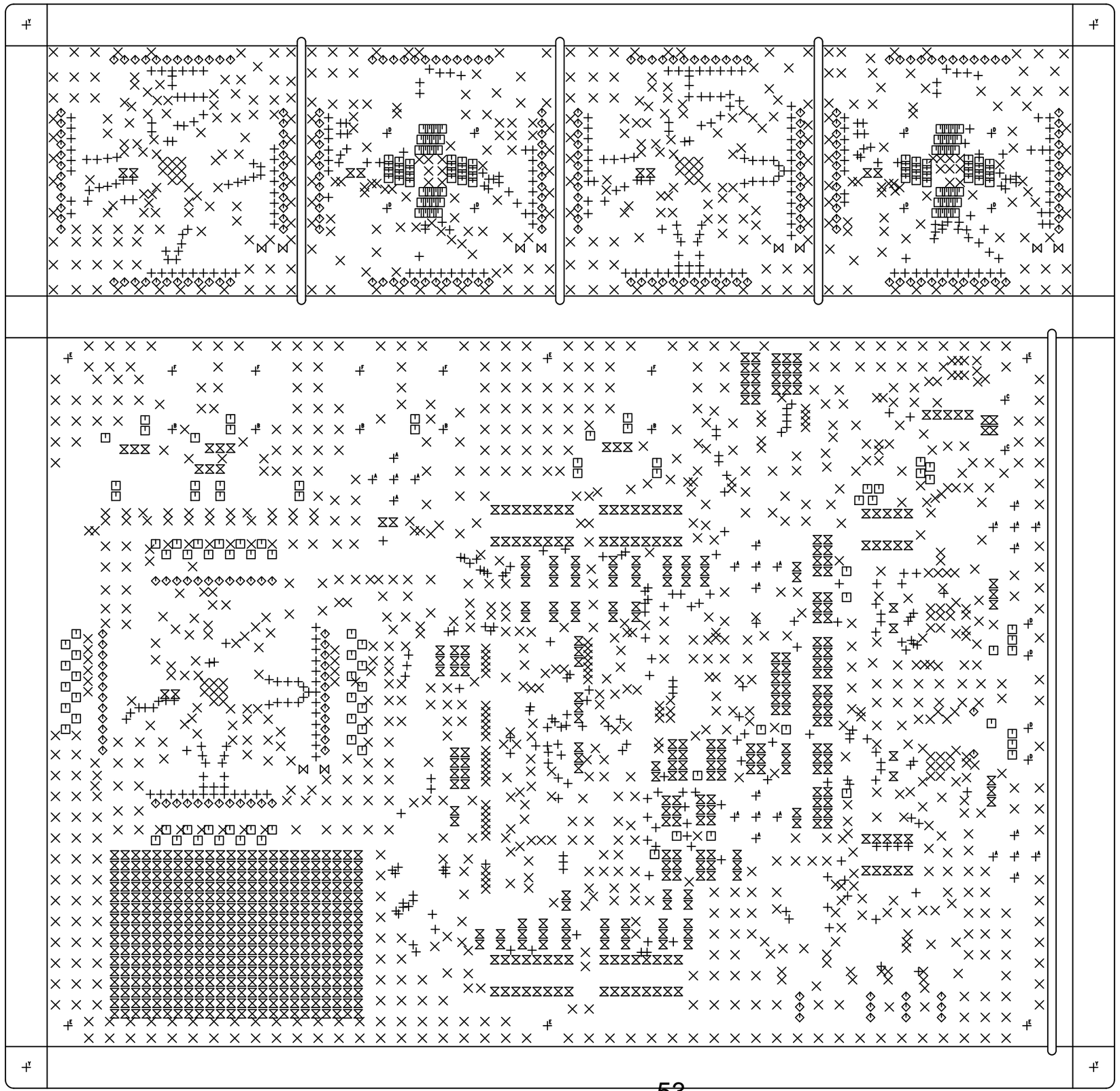
10.0mm
240.0mm
10.0mm
266.0mm

穴径図



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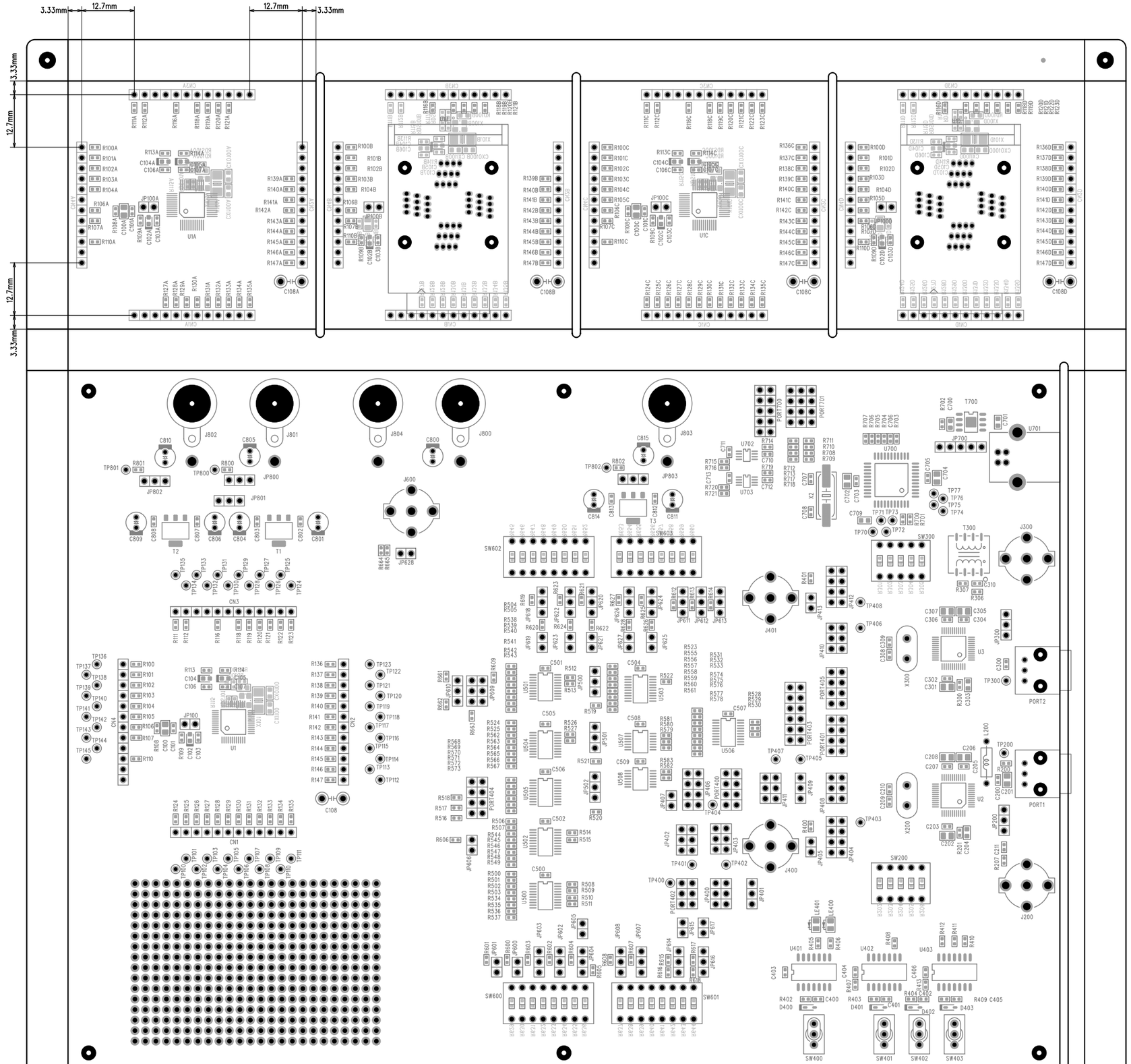
0.5	1467	×	PLTD
0.8	190	□	PLTD
0.9	254	◇	PLTD
1	740	⧖	PLTD
1.2	10	⋈	PLTD
1.7	25	A	PLTD
2	5	B	PLTD
2.3	2	C	PLTD
3.2	12	D	NPLTD
3.5	6	E	NPLTD
9	5	F	NPLTD
4	4	Y	NPLTD
1.99	3	Z	PLTD

※　ＰＬＴＤはスルーホールです。
※　ＮＰＬＴＤはノンスルーホールです。
※　φ１．９９は合わせランドです。
※　穴径は全て仕上がり径でお願いいたします。
※　指示なき穴径公差は±0.05mm


3.33mm
12.7mm
12.7mm
3.33mm
3.33mm
12.7mm
12.7mm
3.33mm
U1A
U1B
U1C
U1D
C108A
C108B
C108C
C108D
J802
J801
J804
J800
J600
J803
J401
J400
J300
J200
T2
T1
T3
T700
U700
U701
U702
U703
U1
U2
U3
X700
X100
X200
X300
SW600
SW601
SW602
SW603
SW200
SW300
SW400
SW401
SW402
SW403
PORT1
PORT2
PORT400
PORT401
PORT402
PORT403
PORT404
PORT405
PORT700
PORT701
CN1
CN2
CN3
CN4
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TP75
TP76
TP77
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U403
U500
U501
U502
U503
U504
U505
U506
U507
U508
U509