Click here for production status of specific part numbers.

MAX12930/MAX12931

Two-Channel, Low-Power, 3kV$_{RMS}$ and 5kV$_{RMS}$ Digital Isolators

General Description

The MAX12930/MAX12931 are a family of 2-channel, 3kV/5kV$_{RMS}$ digital galvanic isolators using Maxim's proprietary process technology. These devices transfer digital signals between circuits with different power domains while using as little as 0.65mW per channel at 1Mbps with 1.8V.

The two channels of the MAX12931 transfer data in opposite directions, and this makes the MAX12931 ideal for isolating the TX and RX lines of a transceiver. The MAX12930 features two channels transferring data in the same direction.

Both devices are available with a maximum data rate of either 25Mbps or 150Mbps and with the default outputs that are either high or low. The default is the state the output assumes when the input is not powered, or if the input is open-circuit. See the *Ordering Information* for suffixes associated with each option. Independent 1.71V to 5.5V supplies on each side of the isolator also make the devices suitable for use as level translators.

The MAX12930/MAX12931 are available in an 8-pin, narrow-body SOIC package. In addition, the MAX12931 is available in a 16-pin, wide-body SOIC package. The package material has a minimum comparative tracking index (CTI) of 600V, which gives it a group 1 rating in creepage tables. All devices are rated for operation at ambient temperatures of -40°C to +125°C.

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Robust Galvanic Isolation of Digital Signals
  - Withstands 5kV$_{RMS}$ for 60s (VISO) Wide-Body
  - Withstands 3kV$_{RMS}$ for 60s (VISO) Narrow-Body
  - Continuously Withstands 848V$_{RMS}$ (VIOWM) Wide-Body
  - Continuously Withstands 445V$_{RMS}$ (VIOWM) Narrow-Body
  - Withstands ±10kV Surge Between GNDA and GNDB with 1.2/50µs Waveform
  - High CMTI (50kV/µs, typ)
- Options to Support a Broad Range of Applications
  - 2 Data Rates (25Mbps/150Mbps)
  - 2 Channel Direction Configurations
  - 2 Output Default States (High or Low)
- Low Power Consumption
  - 1.3mW per Channel at 1Mbps with V_{DD} = 3.3V
  - 3.3mW per Channel at 100Mbps with V_{DD} = 1.8V

Safety Regulatory Approvals

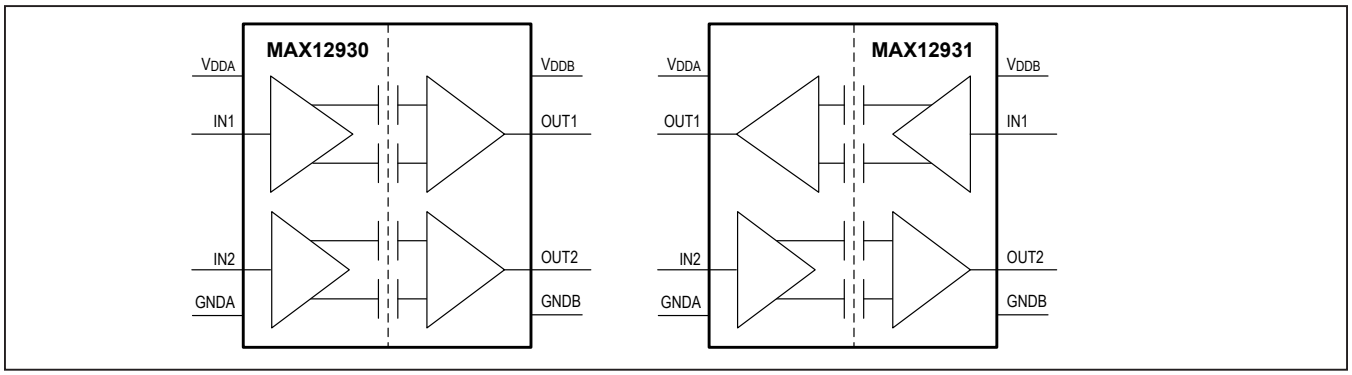
(see *Safety Regulatory Approvals*)

- UL According to UL1577
- cUL According to CSA Bulletin 5A

Applications

- Fieldbus Communications for Industrial Automation
- Isolated RS232, RS-485/RS-422, CAN
- General Isolation Application
- Battery Management
- Medical Systems

Functional Diagrams



maxim integrated™

Absolute Maximum Ratings

V_{DDA} to GNDA .....-0.3V to +6V
V_{DDB} to GNDB .....-0.3V to +6V
IN_ on SIDE A to GNDA .....-0.3V to +6V
IN_ on SIDE B to GNDB .....-0.3V to +6V
OUT_ on SIDE A to GNDA ..... -0.3V to V_{DDA} + 0.3V
OUT_ on SIDE B to GNDB ..... -0.3V to V_{DDB} + 0.3V
Short-Circuit Duration
OUT_ on SIDE A to GNDA, OUT_ on SIDE B to GNDB
.....Continuous

Continuous Power Dissipation (T_A = +70°C)
Wide SOIC (derate 14.1mW/°C above +70°C) 1126.8mW
Narrow SOIC (derate 5.9mW/°C above +70°C) 470.6mW
Operating Temperature Range ..... -40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range ..... -60°C to +150°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 8 NARROW SOIC	
Package Code	S8MS-22
Outline Number	**21-0041**
Land Pattern Number	**90-0096**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	170°C/W
Junction to Case (θ_{JC})	38°C/W

PACKAGE TYPE: 16 WIDE SOIC	
Package Code	W16MS-11
Outline Number	**21-0042**
Land Pattern Number	**90-0107**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	71°C/W
Junction to Case (θ_{JC})	23°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, GNDA = GNDB, T_A = 25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage	V_{DDA}	Relative to GNDA		1.71		5.5	V
	V_{DDB}	Relative to GNDB		1.71		5.5	
Undervoltage-Lockout Threshold	$V_{UVLO\_}$	$V_{DD\_}$ rising		1.5	1.6	1.66	V
Undervoltage-Lockout Threshold Hysteresis	V_{UVLO_HYST}				45		mV
Supply Current (MAX12930_) (Note 2)	I_{DDA}	1MHz square wave, C_L = 0pF	V_{DDA} = 5V		0.32	0.58	mA
			V_{DDA} = 3.3V		0.31	0.54	
			V_{DDA} = 2.5V		0.3	0.53	
			V_{DDA} = 1.8V		0.29	0.39	
		12.5MHz square wave, C_L = 0pF	V_{DDA} = 5V		0.81	1.26	
			V_{DDA} = 3.3V		0.8	1.20	
			V_{DDA} = 2.5V		0.78	1.18	
			V_{DDA} = 1.8V		0.77	1.01	
		50MHz square wave, C_L = 0pF	V_{DDA} = 5V		2.15	3.00	
			V_{DDA} = 3.3V		2.09	2.91	
			V_{DDA} = 2.5V		2.06	2.88	
			V_{DDA} = 1.8V		2	2.62	
	I_{DDB}	1MHz square wave, C_L = 0pF	V_{DDB} = 5V		0.5	0.83	mA
			V_{DDB} = 3.3V		0.47	0.79	
			V_{DDB} = 2.5V		0.45	0.76	
			V_{DDB} = 1.8V		0.4	0.67	
		12.5MHz square wave, C_L = 0pF	V_{DDB} = 5V		1.37	1.83	
			V_{DDB} = 3.3V		1.02	1.40	
			V_{DDB} = 2.5V		0.87	1.22	
			V_{DDB} = 1.8V		0.71	1.00	
		50MHz square wave, C_L = 0pF	V_{DDB} = 5V		4.21	4.99	
			V_{DDB} = 3.3V		2.81	3.39	
			V_{DDB} = 2.5V		2.21	2.69	
			V_{DDB} = 1.8V		1.69	2.04	

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, GNDA = GNDB, T_A = 25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current (MAX12931_) (Note 2)	I_{DDA}	1MHz square wave, C_L = 0pF	V_{DDA} = 5V		0.42	0.70	mA
			V_{DDA} = 3.3V		0.39	0.67	
			V_{DDA} = 2.5V		0.38	0.64	
			V_{DDA} = 1.8V		0.36	0.56	
		12.5MHz square wave, C_L = 0pF	V_{DDA} = 5V		1.07	1.52	
			V_{DDA} = 3.3V		0.89	1.29	
			V_{DDA} = 2.5V		0.81	1.19	
			V_{DDA} = 1.8V		0.73	1.03	
		50MHz square wave, C_L = 0pF	V_{DDA} = 5V		3.06	3.87	
			V_{DDA} = 3.3V		2.37	3.06	
			V_{DDA} = 2.5V		2.08	2.72	
			V_{DDA} = 1.8V		1.82	2.33	
	I_{DDB}	1MHz square wave, C_L = 0pF	V_{DDB} = 5V		0.42	0.70	mA
			V_{DDB} = 3.3V		0.39	0.67	
			V_{DDB} = 2.5V		0.38	0.64	
			V_{DDB} = 1.8V		0.36	0.56	
		12.5MHz square wave, C_L = 0pF	V_{DDB} = 5V		1.07	1.52	
			V_{DDB} = 3.3V		0.89	1.29	
			V_{DDB} = 2.5V		0.81	1.19	
			V_{DDB} = 1.8V		0.73	1.03	
		50MHz square wave, C_L = 0pF	V_{DDB} = 5V		3.06	3.87	
			V_{DDB} = 3.3V		2.37	3.06	
			V_{DDB} = 2.5V		2.08	2.72	
			V_{DDB} = 1.8V		1.82	2.33	
LOGIC INPUTS AND OUTPUTS							
Input High Voltage	V_{IH}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V		0.7 x $V_{DD\_}$			V
		1.71V ≤ $V_{DD\_}$ < 2.25V		0.75 x $V_{DD\_}$			
Input Low Voltage	V_{IL}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V				0.8	V
		1.71V ≤ $V_{DD\_}$ < 2.25V				0.7	
Input Hysteresis	V_{HYS}	MAX1293_B/E			410		mV
		MAX1293_C/F			80		
Input Pullup Current (Note 3)	I_{PU}	IN_, MAX1293_B/C		-10	-5	-1.5	µA
Input Pulldown Current (Note 3)	I_{PD}	IN_, MAX1293_E/F		1.5	5	10	µA
Input Capacitance	C_{IN}	IN_, f_{SW} = 1MHz			2		pF

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, GNDA = GNDB, T_A = 25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage High (Note 3)	V_{OH}	I_{OUT} = 4mA source	$V_{DD\_}$ - 0.4			V
Output Voltage Low (Note 3)	V_{OL}	I_{OUT} = 4mA sink			0.4	V

Dynamic Characteristics MAX1293_B/E

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, GNDA = GNDB, T_A = 25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	IN_ = GND_ or $V_{DD\_}$ (Note 4)		50		kV/µs
Maximum Data Rate	DR_{MAX}		25			Mbps
Minimum Pulse Width	PW_{MIN}				40	ns
Glitch Rejection			10	17	29	ns
Propagation Delay (Figure 1)	t_{PLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	17.4	23.9	32.5	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V	17.6	24.4	33.7	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V	18.3	25.8	36.7	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V	20.7	29.6	43.5	
	t_{PHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	16.9	23.4	33.6	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V	17.2	24.2	35.1	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V	17.8	25.4	38.2	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V	19.8	29.3	45.8	
Pulse Width Distortion	PWD			0.4	4	ns
Propagation Delay Skew Part-to-Part (same channel)	t_{SPLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			15.1	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V			15	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V			15.4	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V			20.5	
	t_{SPHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			13.9	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V			14.2	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V			16	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V			21.8	
Propagation Delay Skew Channel-to-Channel (Same Direction) MAX12930 only	t_{SCSLH}				2	ns
	t_{SCSHL}				2	

Dynamic Characteristics MAX1293_B/E (continued)

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, GNDA = GNDB, T_A = 25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Skew Channel-to-Channel (Opposite Direction) MAX12931 Only	t_{SCOLH}				2	ns
	t_{SCOHL}				2	
Peak Eye Diagram Jitter	$T_{JIT(PK)}$	25Mbps		250		ps
Rise Time	t_R	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			1.6	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V			2.2	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V			3	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V			4.5	
Fall Time	t_F	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			1.4	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V			2	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V			2.8	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V			5.1	

Dynamic Characteristics MAX1293_C/F

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, GNDA = GNDB, T_A = 25°C, unless otherwise noted.) (Notes 2,3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	IN_ = GND_ or $V_{DD\_}$ (Note 4)		50		kV/µs
Maximum Data Rate	DR_{MAX}		150			Mbps
Minimum Pulse Width	PW_{MIN}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V			5	ns
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V			6.67	
Propagation Delay (Figure 1)	t_{PLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	4.1	5.4	9.2	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V	4.2	5.9	10.2	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V	4.9	7.1	13.4	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V	7.1	10.9	20.3	
	t_{PHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	4.3	5.6	9.4	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V	4.4	6.2	10.5	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V	5.1	7.3	14.1	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V	7.2	10.9	21.7	
Pulse Width Distortion	PWD			0.3	2	ns
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			3.7	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V			4.3	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V			6	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V			10.3	
	t_{SPHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			3.8	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V			4.7	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V			6.5	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V			11.5	
Propagation Delay Skew Channel-to-Channel (Same Direction) MAX12930 Only	t_{SCSLH}				2	ns
	t_{SCSHL}				2	
Propagation Delay Skew Channel-to-Channel (Opposite Direction) MAX12931 Only	t_{SCOLH}				2	ns
	t_{SCOHL}				2	
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	150Mbps		90		ps
Clock Jitter RMS	$t_{JCLK(RMS)}$	500kHz Clock Input Rising/Falling Edges		6.5		ps

Dynamic Characteristics MAX1293_C/F (continued)

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, GNDA = GNDB, T_A = 25°C, unless otherwise noted.) (Notes 2,3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time	t_R	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			1.6	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V			2.2	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V			3	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V			4.5	
Fall Time	t_F	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			1.4	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V			2	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V			2.8	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V			5.1	

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: Not production tested. Guaranteed by design and characterization.
Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDA or GNDB), unless otherwise noted.
Note 4: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage sedges. Tested with the transient generator connected between GNDA and GNDB (V_{CM} = 1000V).

ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD		Human Body Model, all pins		±3		kV

Safety Regulatory Approvals

UL
The MAX12930–MAX12931 narrow-body SOIC are certified under UL1577. For more details, refer to file E351759.
Rated up to 3000V$_{RMS}$ isolation voltage for single protection.
cUL (Equivalent to CSA Notice 5A)
The MAX12930–MAX12931 narrow-body SOIC are certified up to 3000V$_{RMS}$ for single protection. For more details, refer to file E351759.

UL
The MAX12931 wide-body SOIC is certified under UL1577. For more details, refer to file E351759.
Rated up to 5000V$_{RMS}$ isolation voltage for single protection.
cUL (Equivalent to CSA notice 5A)
The MAX12931 wide-body SOIC is certified up to 5000V$_{RMS}$ for single protection. For more details, refer to file E351759.

Insulation Characteristics

Table 1. Narrow SOIC Insulation Characteristic

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	1182	V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(Note 5)	630	V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (Note 5)	445	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s	6000	V_P
Maximum Withstand Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (Note 6)	3000	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Basic Insulation, 1.2/50µs pulse per IEC61000-4-5	10	kV
Insulation Resistance	R_S	T_A = 150°C, V_{IO} = 500V	>10^9	Ω
Barrier Capacitance Side A to Side B	CIO	f_{SW} = 1MHz (Note 7)	2	pF
Minimum Creepage Distance	CPG	Narrow SOIC	4	mm
Minimum Clearance Distance	CLR	Narrow SOIC	4	mm
Internal Clearance		Distance through insulation	0.015	mm
Comparative Tracking Index	CTI	Material Group I (IEC60112)	>600	
Climate Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Table 2. Wide SOIC Insulation Characteristic

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	2250	V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(Note 5)	1200	V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (Note 5)	848	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s	8400	V_P
Maximum Withstand Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (Note 6)	5000	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Basic Insulation, 1.2/50µs pulse per IEC61000-4-5	10	kV
Insulation Resistance	R_S	T_A = 150°C, V_{IO} = 500V	>10^9	Ω
Barrier Capacitance Side A to Side B	CIO	f_{SW} = 1MHz (Note 7)	2	pF
Minimum Creepage Distance	CPG	Wide SOIC	8	mm
Minimum Clearance Distance	CLR	Wide SOIC	8	mm
Internal Clearance		Distance through insulation	0.015	mm
Comparative Tracking Index	CTI	Material Group I (IEC60112)	>600	
Climate Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 5: VISO, VIOWM and VIORM are defined by the IEC 60747-5-5 standard.
Note 6: Product is qualified at VISO for 60s and 100% production tested at 120% of VISO for 1s.
Note 7: Capacitance is measured with all pins on side A and side B tied together.

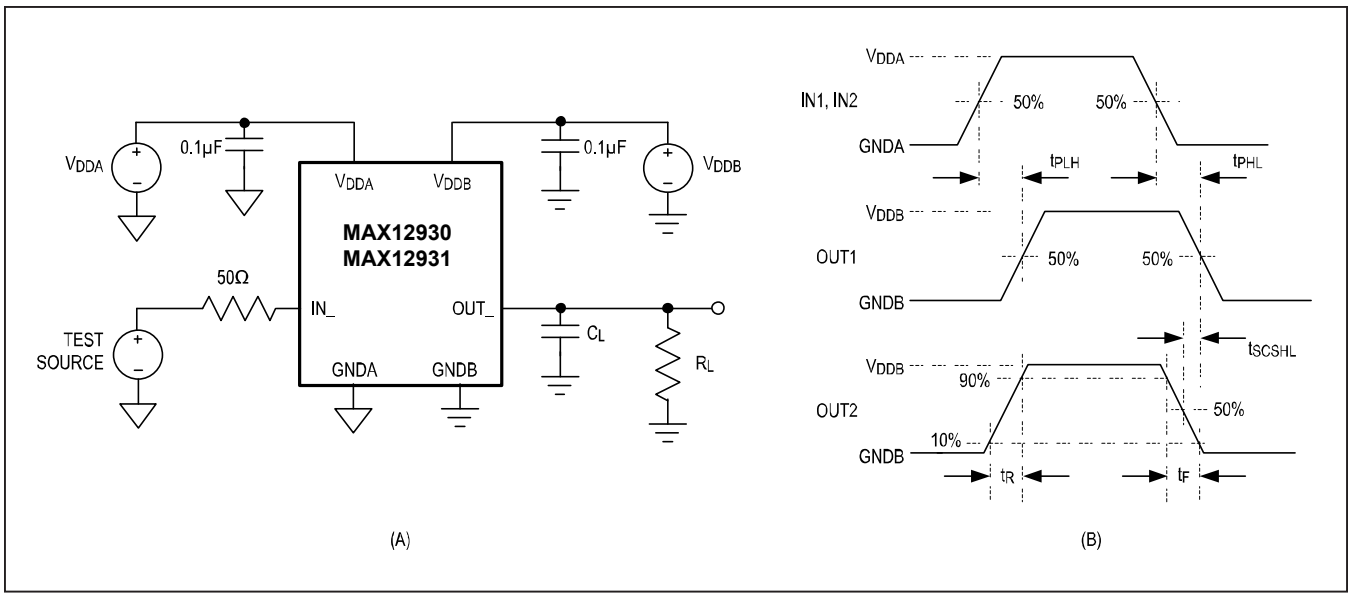
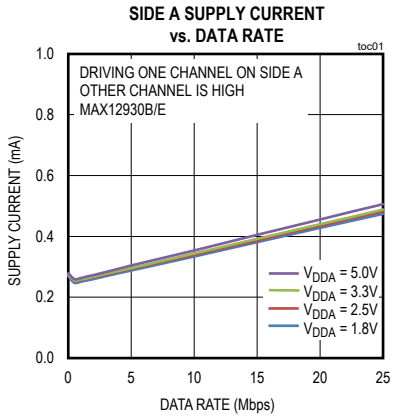
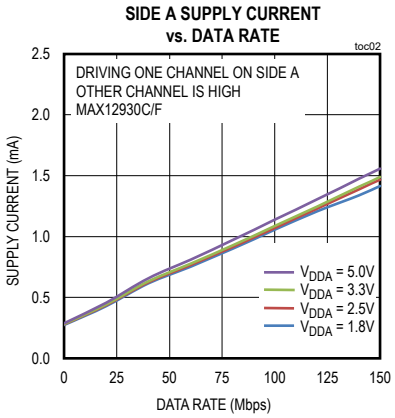


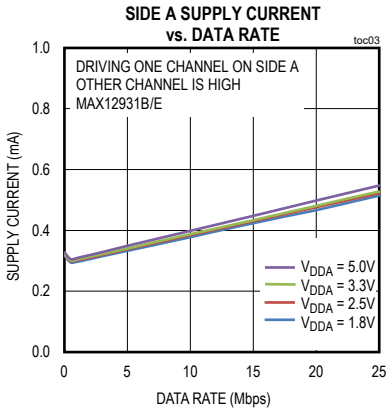
Figure 1. Test Circuit (A) and Timing Diagram (B)

Typical Operating Characteristics

(V_{VDDA} - V_{GNDA} = +3.3V, V_{VDDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)



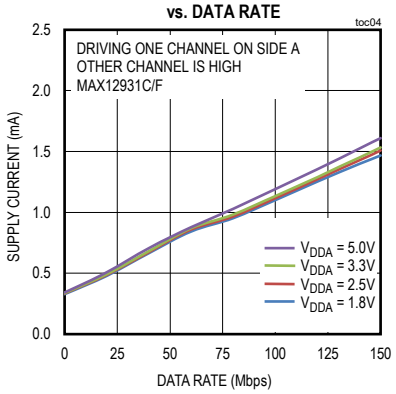




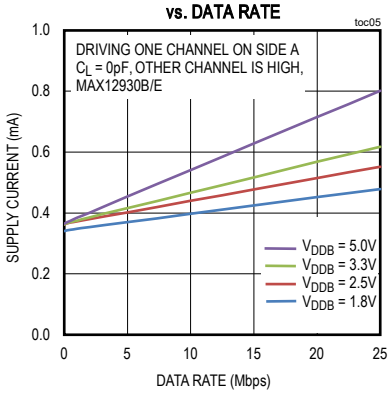
Typical Operating Characteristics (continued)

(V_{VDDA} - V_{GNDA} = +3.3V, V_{VDDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

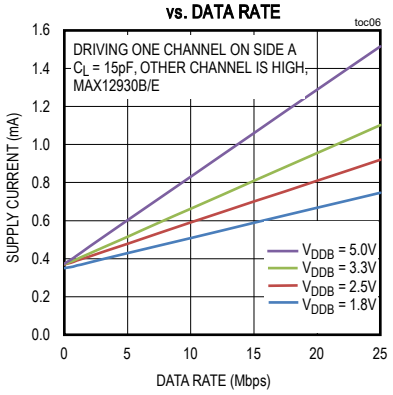
SIDE A SUPPLY CURRENT vs. DATA RATE



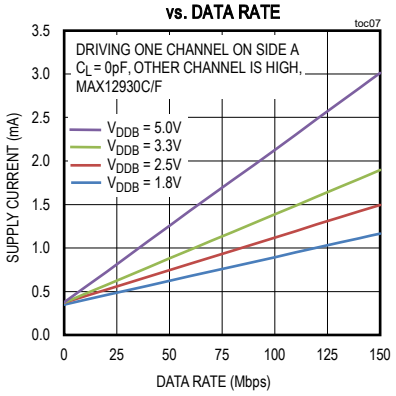
SIDE B SUPPLY CURRENT vs. DATA RATE



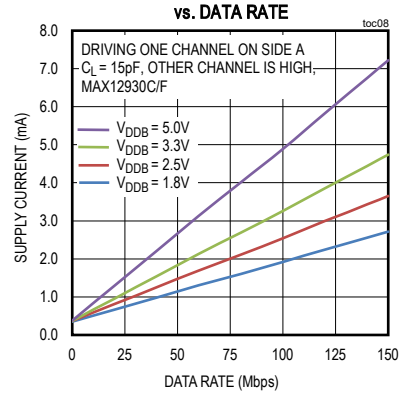
SIDE B SUPPLY CURRENT vs. DATA RATE



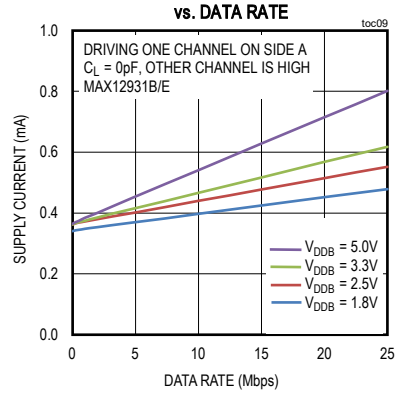
SIDE B SUPPLY CURRENT vs. DATA RATE



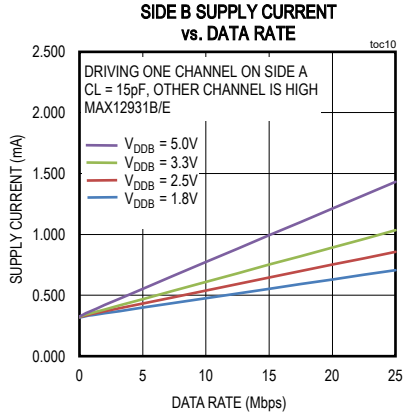
SIDE B SUPPLY CURRENT vs. DATA RATE



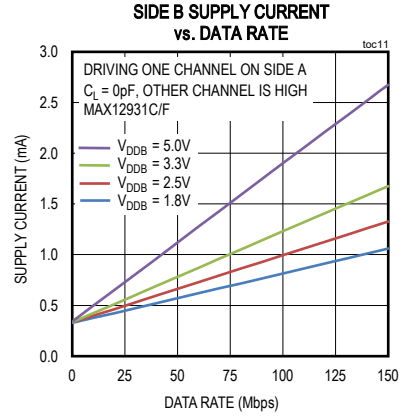
SIDE B SUPPLY CURRENT vs. DATA RATE



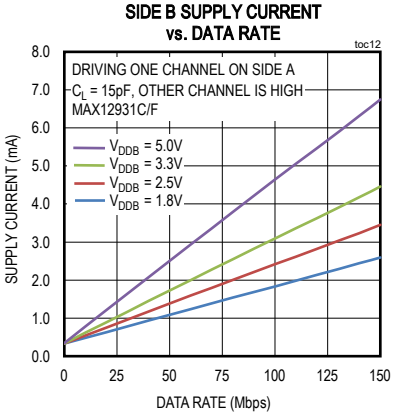
SIDE B SUPPLY CURRENT vs. DATA RATE



SIDE B SUPPLY CURRENT vs. DATA RATE



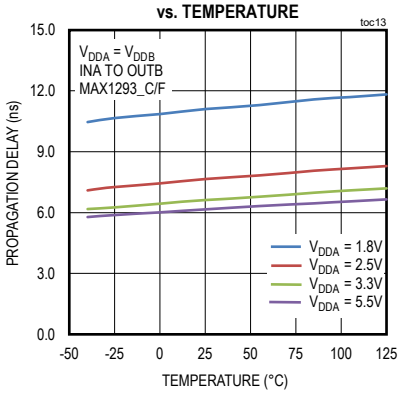
SIDE B SUPPLY CURRENT vs. DATA RATE



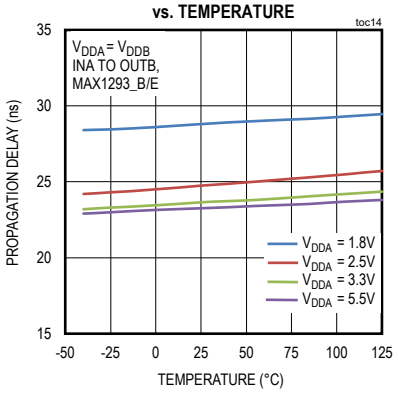
Typical Operating Characteristics (continued)

(V_{VDDA} - V_{GNDA} = +3.3V, V_{VDDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

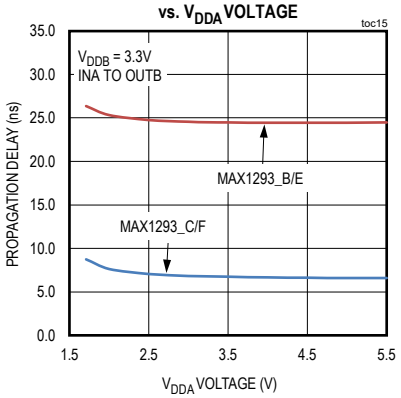
PROPAGATION DELAY vs. TEMPERATURE



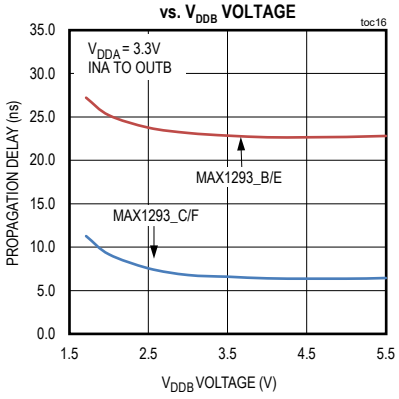
PROPAGATION DELAY vs. TEMPERATURE



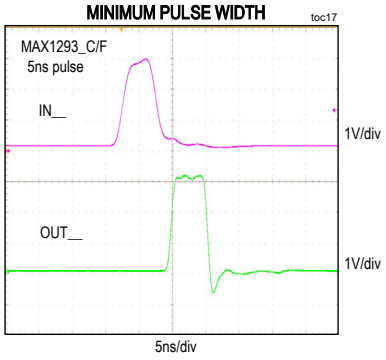
PROPAGATION DELAY vs. V_{DDA} VOLTAGE



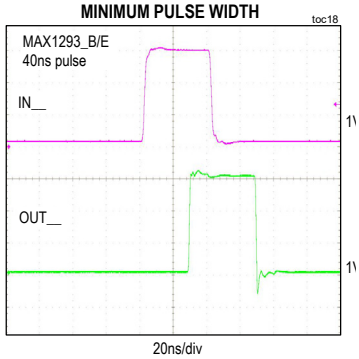
PROPAGATION DELAY vs. V_{DDB} VOLTAGE



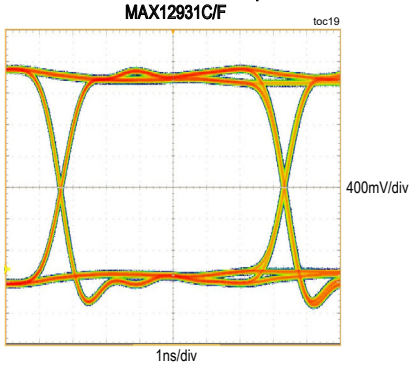
MINIMUM PULSE WIDTH



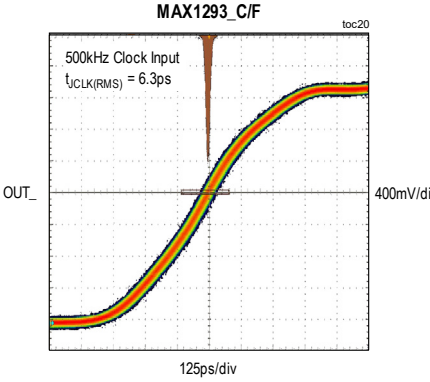
MINIMUM PULSE WIDTH



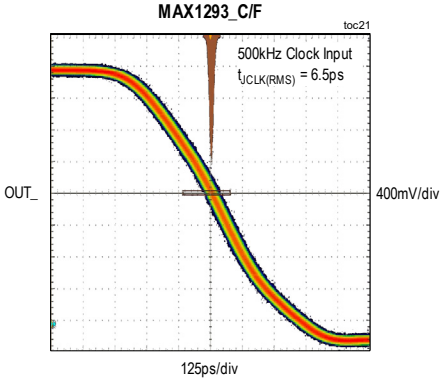
EYE DIAGRAM at 150Mbps
MAX12931C/F



CLOCK JITTER RMS ON RISING EDGE
MAX1293_C/F

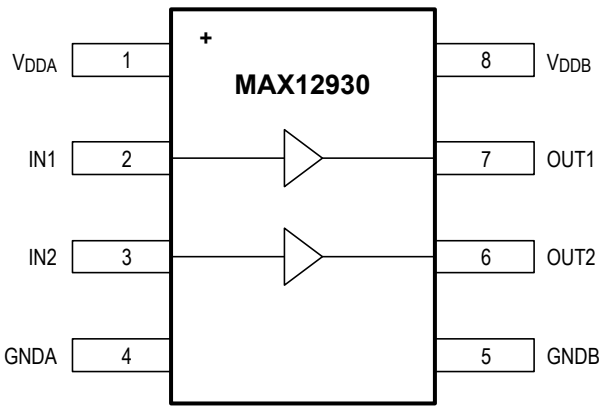


CLOCK JITTER RMS ON FALLING EDGE
MAX1293_C/F

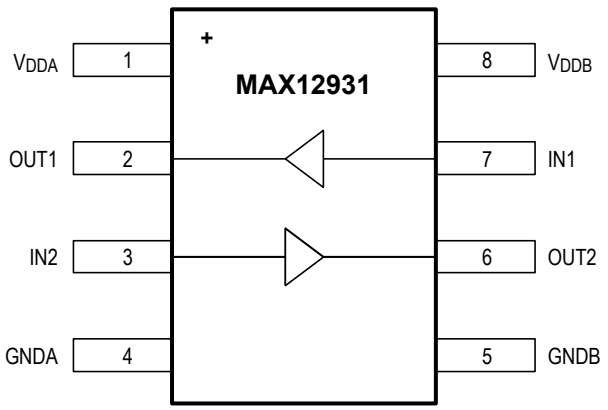


Pin Configurations

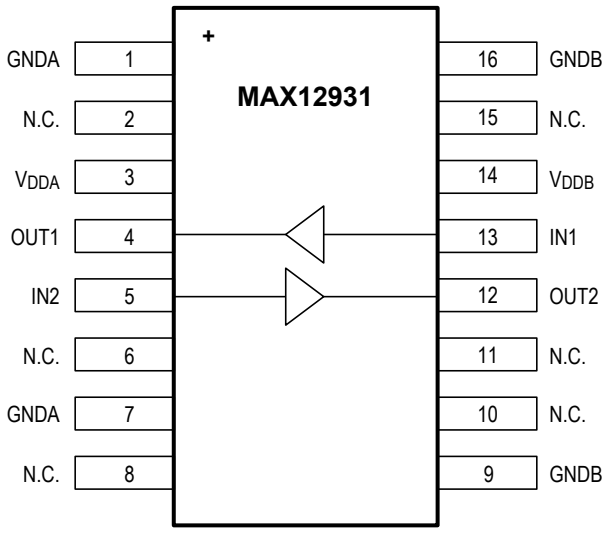
TOP VIEW



NARROW SOIC



NARROW SOIC

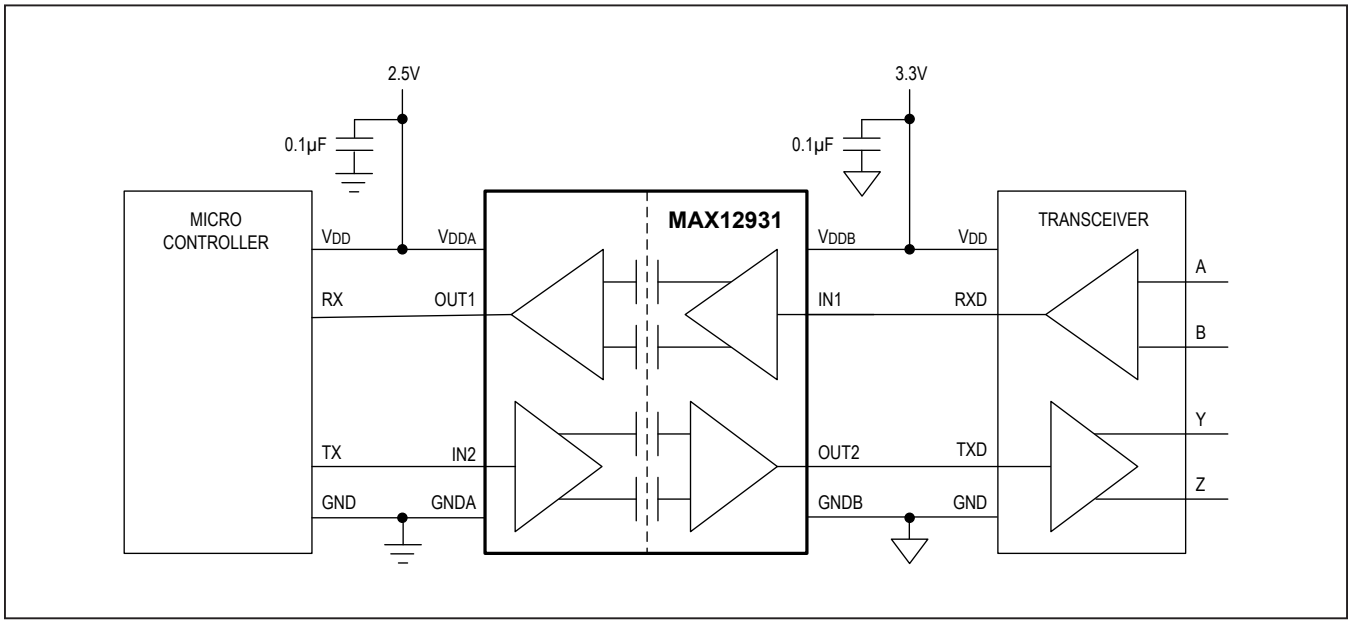


WIDE SOIC

Pin Description

PIN			NAME	FUNCTION	REFERENCE
MAX12930 8-PIN SOIC	MAX12931 8-PIN SOIC	MAX12931 16-PIN SOIC			
1	1	3	V_{DDA}	Power Supply for side A. Bypass V_{DDA} with a 0.1µF ceramic capacitor to GNDA.	GNDA
2	—	—	IN1	Logic input for channel 1	GNDA
—	2	4	OUT1	Logic output of channel 1	GNDA
3	3	5	IN2	Logic input for channel 2	GNDA
4	4	1, 7	GNDA	Ground reference for side A	—
5	5	9, 16	GNDB	Ground reference for side B	—
6	6	12	OUT2	Logic output of channel 2	GNDB
7	—	—	OUT1	Logic output of channel 1	GNDB
—	7	13	IN1	Logic input for channel 1	GNDB
8	8	14	V_{DDB}	Power Supply for side B. Bypass V_{DDB} with a 0.1µF ceramic capacitor to GNDB.	GNDB
—	—	2, 6, 8, 10, 11, 15	N.C.	Not internally connected	—

Typical Operating Circuit



Detailed Description

The MAX12930/MAX12931 are a family of 2-channel digital isolators. The MAX12930 transfers digital signals between circuits with different power domain in one direction, which is convenient for applications such as digital I/O. The MAX12931 transfers digital signals in opposite directions, which is necessary for isolated RS-485 or other UART applications.

Devices available in the 8-pin narrow body SOIC package are rated for up to 3kV$_{RMS}$ isolation voltage for 60 seconds and the device in the 16-pin wide body SOIC package is rated for up to 5kV$_{RMS}$. This family of digital isolators offers low-power operation, high electromagnetic interference (EMI) immunity, and stable temperature performance through Maxim's proprietary process technology. The devices isolate different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry.

Devices are available with data rates from DC to 25Mbps (B/E versions) or 150Mbps (C/F versions). Each device can be ordered with default-high or default-low outputs. The default is the state the output assumes when the input is not powered, or if the input is open circuit.

The devices have two supply inputs (V_{DDA} and V_{DDB}) that independently set the logic levels on either side of device. V_{DDA} and V_{DDB} are referenced to GNDA and GNDB, respectively. The MAX12930/MAX12931 family also features a refresh circuit to ensure output accuracy when an input remains in the same state indefinitely.

Digital Isolation

The device family provides galvanic isolation for digital signals that are transmitted between two ground domains. Up to 630V$_{PEAK}$ of continuous isolation is supported in the narrow SOIC package and up to 1200V$_{PEAK}$ of continuous isolation is supported in the wide SOIC package. The devices withstand differences of up to 3kV$_{RMS}$ in the 8-pin narrow SOIC package or 5kV$_{RMS}$ in the 16-pin wide SOIC package for up to 60 seconds.

Level-Shifting

The wide supply voltage range of both V_{DDA} and V_{DDB} allows the MAX12930/MAX12931 family to be used for level translation in addition to isolation. V_{DDA} and V_{DDB} can be independently set to any voltage from 1.71V to 5.5V. The supply voltage sets the logic level on the corresponding side of the isolator.

Unidirectional Channels

Each channel of the MAX12930/MAX12931 is unidirectional; it only passes data in one direction, as indicated in the functional diagram. Each device features two unidirectional channels that operate independently with guaranteed data rates from DC up to 25Mbps (B/E versions), or DC to 150Mbps (C/F versions). The output driver of each channel is push-pull, eliminating the need for pullup resistors. The outputs are able to drive both TTL and CMOS logic inputs.

Startup and Undervoltage-Lockout

The V_{DDA} and V_{DDB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage condition is detected on either supply, all outputs go to their default states regardless of the state of the inputs (Table 3). Figure 2 through Figure 5 show the behavior of the outputs during power-up and power-down.

Table 3. Output Behavior During Undervoltage Conditions

$V_{IN\_}$	V_{VDDA}	V_{VDDB}	$V_{OUTA\_}$	$V_{OUTB\_}$
1	Powered	Powered	1	1
0	Powered	Powered	0	0
X	Undervoltage	Powered	Default	Default
X	Powered	Undervoltage	Default	Default

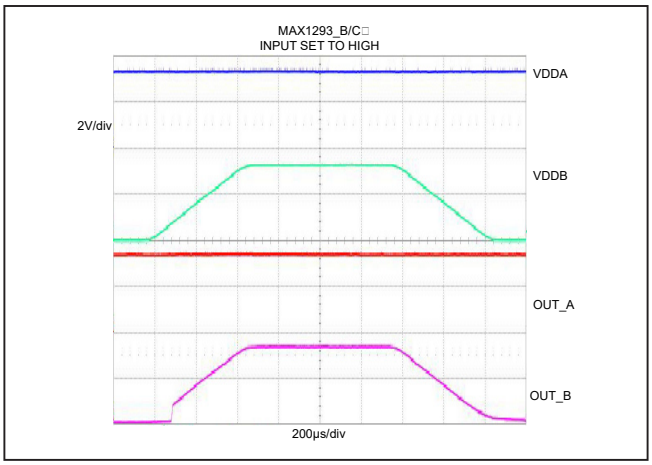


Figure 2. Undervoltage Lockout Behavior (MAX1293_B/C High)

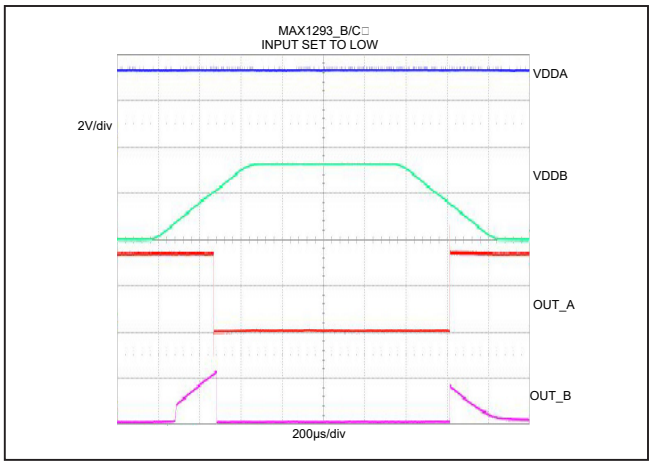


Figure 3. Undervoltage Lockout Behavior (MAX1293_B/C Low)

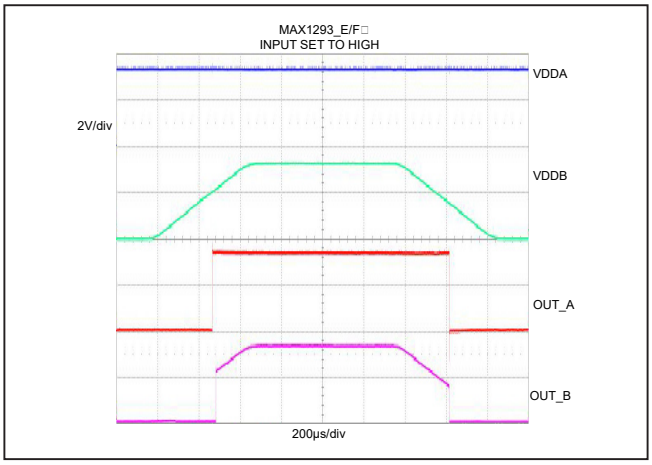


Figure 4. Undervoltage Lockout Behavior (MAX1293_E/F High)

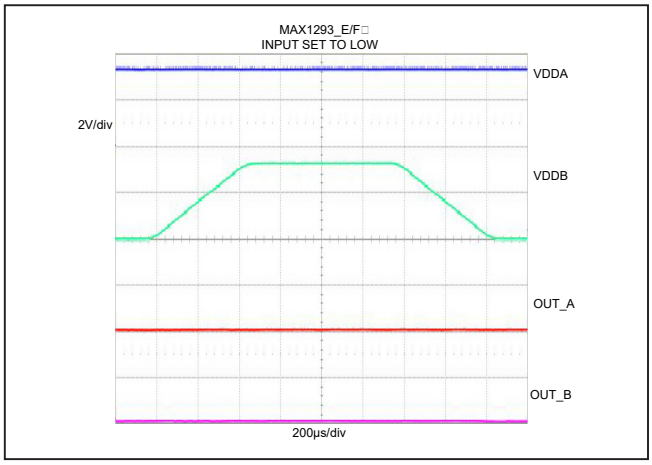


Figure 5. Undervoltage Lockout Behavior (MAX1293_E/F Low)

Application Information

Power-Supply Sequencing

The MAX12930/MAX12931 do not require special power supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB}. Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with 0.1µF low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power supply input pins as possible.

Layout Considerations

The PCB designer should follow some critical recommendation in order to get the best performance from the design.

- Keep the input/output traces as short as possible. Avoid using vias to make low-inductance paths for the signals.
- Have a solid ground plane underneath the high-speed signal layer.
- Keep the area underneath the MAX12930/MAX12931 free from ground and signal planes. Any galvanic or metallic connection between the field-side and logic-side defeats the isolation.

Calculating Power Dissipation

The required current for a given supply (VDDA or VDDB) can be estimated by summing the current required for each channel. The supply current for a channel depends on whether the channel is an input or an output, the channel's data rate, and the capacitive or resistive load if it is an output. The typical current for an input or output at any data rate can be estimated from the graphs in Figure 6 and Figure 7. Please note that the data in Figure 6 and Figure 7 are extrapolated from the supply current measurements in a typical operating condition.

The total current for a single channel is the sum of the "no load" current (shown in Figure 6 and Figure 7) which is a function of Voltage and Data Rate, and the "load current" which depends upon the type of load. Current into a capacitive load is a function of the load capacitance, the switching frequency, and the supply voltage.

$$I_{CL} = C_L \times f_{SW} \times V_{DD}$$

where,

I_{CL} = Current required to drive the capacitive load.

C_L = Load capacitance on the isolator's output pin.

f_{SW} = Switching frequency (bits per second/2).

V_{DD} = Supply voltage on the output side of the isolator.

Current into a resistive load depends on the load resistance, the supply voltage and the average duty cycle of the data waveform. The DC load current can be conservatively estimated by assuming the output is always high.

$$I_{RL} = V_{DD} \div R_L$$

where,

I_{RL} = Current required to drive the resistive load.

V_{DD} = Supply voltage on the output side of the isolator.

R_L = Load resistance on the isolator's output pin.

Example (shown in Figure 8): A MAX12931F is operating with V_{DDA} = 2.5V, V_{DDB} = 3.3V, channel 1 operating at 100Mbps with a 15pF capacitive load, and channel 2 operating at 20Mbps with a 10pF capacitive load. Refer to Table 4 and Table 5 for V_{DDA} and V_{DDB} supply current calculation worksheets.

V_{DDA} must supply:

Channel 1 is an output channel operating at 2.5V and 100Mbps, consuming 1.02mA, estimated from Figure 7. Channel 2 is an input channel operating at 2.5V and 20Mbps, consuming 0.33mA, estimated from Figure 6. ICL on channel 1 for 15pF capacitor at 2.5V and 100Mbps is 1.875mA.

Total current for side A = 1.02+ 0.33 + 1.875 = 3.225mA, typical

V_{DDB} must supply:

Channel 1 is an input channel operating at 3.3V and 100Mbps, consuming 1.13mA, estimated from Figure 6. Channel 2 is an output channel operating at 3.3V and 20Mbps, consuming 0.42mA, estimated from Figure 7. ICL on channel 2 for 10pF capacitor at 3.3V and 20Mbps is 0.33mA.

Total current for side B = 1.13 + 0.42 + 0.33 = 1.88mA, typical

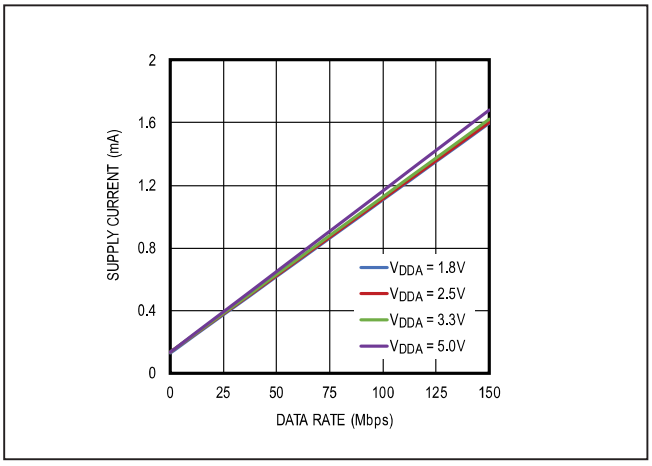


Figure 6. Supply Current per Input Channel Versus Data Rate

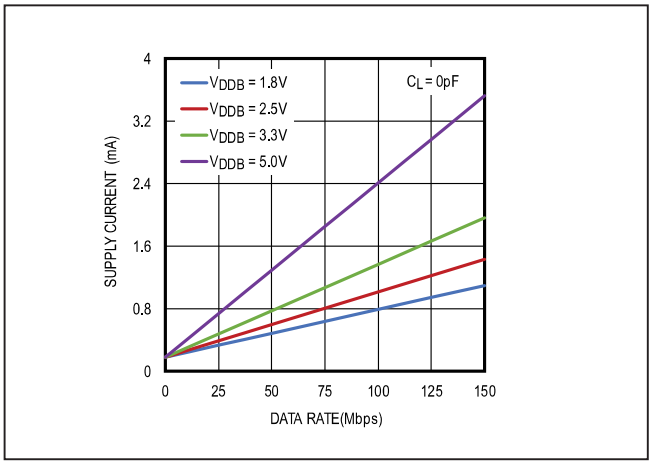


Figure 7. Supply Current per Output Channel Versus Data Rate

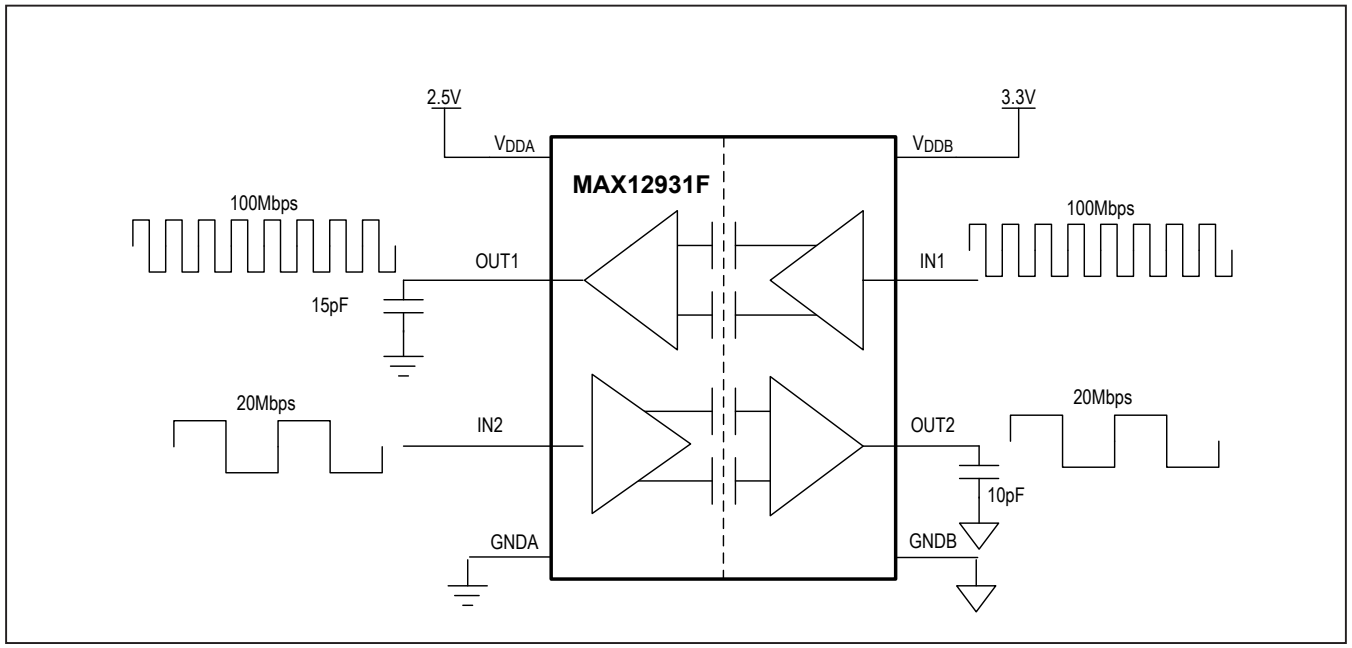


Figure 8. Example Circuit for Supply Current Calculation

Table 4. Side A Supply Current Calculation Worksheet

SIDE A	V_{DDA} = 2.5V					
CHANNEL	IN/OUT	FREQUENCY (Mbps)	LOAD TYPE	LOAD	"NO LOAD" CURRENT (mA)	LOAD CURRENT (mA)
1	OUT	100	Capacitive	15pF	1.02	2.5V x 50MHz x 15pF = 1.875mA
2	IN	20			0.33	
Total:						3.225mA

Table 5. Side B Supply Current Calculation Worksheet

SIDE B	V_{DDB} = 3.3V					
CHANNEL	IN/OUT	FREQUENCY (Mbps)	LOAD TYPE	LOAD	"NO LOAD" CURRENT (mA)	LOAD CURRENT (mA)
1	IN	100			1.13	
2	OUT	20	Capacitive	10pF	0.42	3.3V x 10MHz x 10pF = 0.33mA
Total:						1.88mA

Ordering Information

PART	CHANNEL CONFIGURATION	DATA RATE (Mbps)	DEFAULT OUTPUT	ISOLATION VOLTAGE (kV$_{RMS}$)	TEMP RANGE	PIN-PACKAGE
MAX12930BASA+	2/0	25	High	3	-40°C to 125°C	8 Narrow SOIC
MAX12930CASA+*	2/0	150	High	3	-40°C to 125°C	8 Narrow SOIC
MAX12930EASA+	2/0	25	Low	3	-40°C to 125°C	8 Narrow SOIC
MAX12930FASA+	2/0	150	Low	3	-40°C to 125°C	8 Narrow SOIC
MAX12931BASA+	1/1	25	High	3	-40°C to 125°C	8 Narrow SOIC
MAX12931CASA+*	1/1	150	High	3	-40°C to 125°C	8 Narrow SOIC
MAX12931EASA+	1/1	25	Low	3	-40°C to 125°C	8 Narrow SOIC
MAX12931FASA+	1/1	150	Low	3	-40°C to 125°C	8 Narrow SOIC
MAX12931BAWE+	1/1	25	High	5	-40°C to 125°C	16 Wide SOIC

**Future Product—Contact factory for availability.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/16	Initial release	—
1	3/17	Added *Safety Regulatory Approvals* section, updated *Absolute Maximum Rating*, *Package Thermal Characteristics,* and *Electrical Characteristics* sections, and removed future product status from MAX12930FASA+ and MAX12931BASA+	1, 2, 5, 7–13, 15–19
2	8/17	Removed future asterisk from MAX12931FASA+ in *Ordering Information* table	21
3	10/17	Removed future asterisk from MAX12930BASA+ in *Ordering Information* table	21
4	11/18	Removed future asterisk from MAX12930EASA+ and MAX12931EASA+ in *Ordering Information* table	21

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