Report Modelsim: Digital Systems

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1 Simulating

- The signal a are active four times on the rising edge of the clock.
- It must be ingnord one time (the second intance of active a) during the simulation period since the macro-cycle is already running. The third time a is high, the new macro cycle does not start, and that is not the correct behaviour according to the spesifications.
- The bug in the g1.vhd got fixed by:

```
if a='0' then
       clk = '1' and clk'event and a = '1' ;
   end if;
```

  One could also use:

```
 if not(clk='1' and clk'event a='1') then
```

- As expected the signal assignments are exceuted on the same physical duration, but with one delta-cycle delay.

2 Bonus

- The g1.vhd with synchronous, active high, reset signal is added in directory.