Report Lab DC: Digital Systems

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1 Refinement of a VHDL model for synthesis

- The target clock period is 2.0 nm, so the clock freq is 1/2.0 = 5e+8 = 500 MHz.
- The input and output delay is 0.5 ns
- The synthesis gives the following errors Error: ../g1.vhd:27: WAIT statement inside FOR loop is not supported. (ELAB-996) Error: ../g1.vhd:27: WAIT statement inside FOR loop is not supported. (ELAB-996)

  There are wait statements on several occations in the process. These lines needs to be rewritten to be synthesizable. I did the following.

```
p: process(clk)
  begin
    -- First, if the condition to start a macro-cycle does not
        hold, synchronize
    -- on a rising edge of clock where a is active. Else, start a
        macro-cycle.

    if clk = '1' and clk'event then
      if a = '1' then
        -- if not (clk = '1' and clk'event and a = '1') then
        --  wait until clk = '1' and clk'event and a = '1';
        -- end if;
        s_local <= '1'; -- a macro-cycle starts (set s_local)
        for i in 4 downto 0 loop -- a macro-cycle is made of 5
            sequences
          for j in 1 to 2 ** i loop -- wait for 2^i cycles

          end loop;
          s_local <= not s_local; -- invert s_local
        end loop;
      end if;
    end if;
  end process p;
```

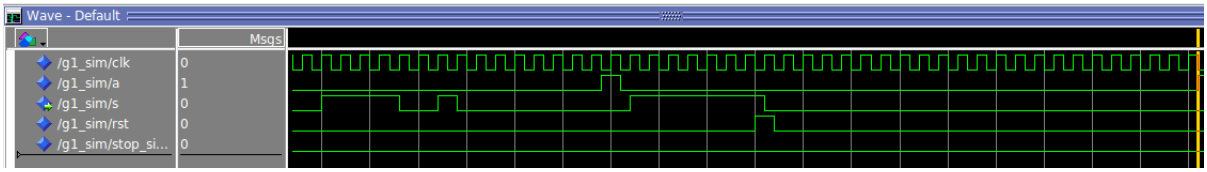

Figure 1: wave diagram showing sync reset

2 Synthesis reports

- The silicon area of the synthesized circuit is 102 μm^2 .