

[illegible]

The diagram illustrates a 74LS259 decoder circuit. The inputs are A12-A18 (5-bit address) and SS[1:0] (2-bit select). The circuit uses a 74LS153 3-to-8 decoder and a 74LS154 4-to-16 decoder to generate 16 outputs (Net129-Net144). The outputs are connected to a 74LS259 3-to-8 decoder, which produces 8 outputs (SS_HIRES[0:7]). The circuit is powered by a 5V supply and includes pull-up resistors on the address lines.

The diagram illustrates a bypass capacitor chain. A VCC supply is connected to a resistor R3 (1K) and a pullup resistor. A chain of 13 capacitors (C3 to C13) is connected in series between the VCC line and ground. Each capacitor has a value of 0.047. The final capacitor C13 is labeled as 22uF 25V.

The diagram illustrates three cascaded 74LS95 shift registers. The top register (U6) has inputs Ds (Net56), P0 (Net55), P1 (Net54), P2 (Net53), and P3 (Net52). Its outputs are Q0 (Net56), Q1 (Net55), Q2 (Net54), Q3 (Net53), and Q4 (Net52). The middle register (U7) has inputs Ds (Net56), P0 (Net55), P1 (Net54), P2 (Net53), and P3 (Net52). Its outputs are Q0 (Net55), Q1 (Net54), Q2 (Net53), Q3 (Net52), and Q4 (Net51). The bottom register (U8) has inputs Ds (Net56), P0 (Net55), P1 (Net54), P2 (Net53), and P3 (Net52). Its outputs are Q0 (Net54), Q1 (Net53), Q2 (Net52), Q3 (Net51), and Q4 (Net50). The registers are connected such that the Q0 output of one register feeds the D input of the next.

The diagram illustrates the internal logic of a video mux and output connector. It is organized into three main functional blocks:

- SYNC MUX:** This block handles the synchronization signals. It takes inputs from the camera (HSYNC_BD_IN_1, VSYNC_BD_IN_5) and the system (SS_EN_RQ_9, SS_EN_R_11, SS_EN_B_2, SS_EN_BD_4). These signals are processed through a series of AND and OR gates to produce the final HSYNC and VSYNC outputs.
- VIDEO MUX:** This block handles the video signals. It takes inputs from the camera (Mux_HIRIS_1, Mux_A2_11, Mux_LORES_12) and the system (SS_ENL_B_9, SS_ENL_R_10, SS_ENL_G_11). These signals are processed through a series of AND and OR gates to produce the final VIDEO, B_OUT, G_OUT, and R_OUT signals.
- OUTPUT CONNECTOR:** This block shows the final output signals (HSYNC, VSYNC, VIDEO, B_OUT, G_OUT, R_OUT, VSYNC, B_IN, G_IN, R_IN) connected to the system. It also includes a GND connection.

The diagram uses various logic gates (AND, OR, NOT) and multiplexers (MUX) to route the signals. The system signals are labeled with 'U34A' and 'U34B' and '74LS01'.

[illegible]

Sheet: /
File: AmdekDVM.kicad_sch

Title:	
Size: A1	Date:
KiCad E.D.A. 9.0.1	Id: 1/1